THESIS

MEASUREMENT OF CADMIUM TELLURIDE BILAYER SOLAR CELLS

Submitted by

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ABSTRACT

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Photovoltaic (PV) technology is a green technology that uses devices and semiconducting materials to generate power by converting the absorbed energy from solar to electrical energy. Understanding the performance and behavior of a fabricated device is essential for enhancing their efficiency for future commercialization. Cadmium-telluride (CdTe) technology is a PV technology that uses CdTe as the semiconductor layer for absorbing and converting sunlight into electricity. Incorporating a bilayer of cadmium selenium telluride ($CdSe_xTe_{1-x}$) alloy and CdTe into solar cell devices have shown particularly good performance, enhanced passivation, and higher efficiency.

In this research, cadmium telluride solar cells were fabricated with a focus on improving the performance of the absorber layers. Radio frequency (RF) magnetron sputtering and close-space sublimation were adopted in preparing the front and back contact layers respectively. The fabricated device comprises of Tec-10 glass/100-nm magnesium-doped zinc oxide (MZO)/0.5-μm CST40/2.5-μm CdTe/ cadmium-chloride passivation/ Cu-doping/ 40-nm Te/ carbon and nickel paint back contact. As part of the performance improvement measures, the bilayer surface was passivated with cadmium chloride ($CdCl_2$) and doped afterwards with copper. The fabricated $CdSe_xTe_{1-x}$/CdTe device was subjected to room temperature and low temperature current density-voltage (J-V), capacitance, phase angle, quantum efficiency (QE), reflectance, electroluminescence (EL), and photoluminescence (PL) measurements. The J-V characteristics gave 15% device efficiency and showed diode curves which rolled over at lower temperatures,

but were more ideal at higher temperatures. Capacitance measurements gave a hole density of $4x10^{14}$ cm^{-3} and a phase angle of 88^{o}. The cells recorded high quantum efficiency of about 85% which is indicative of reduced recombination rate. Few defects were observed from the EL images while the PL emission peaks were obtained at 875 nm corresponding to an approximate energy band gap value of 1.42 eV. The measurement results show good performance for use in commercial solar cells for energy sustainability. Future implications encompass module fabrication, flexible devices, and affordability for enhancing green energy production and minimizing environmental pollution. Prospects envisage fabricating CdTe devices with higher efficiencies which would continue to compete successfully with other solar cell technologies.

Key words: CST; CdTe; Solar cell; Rollover effect; Band gap; Efficiency.

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I want to say a big thank you to God for His Grace that was sufficient, even in my downtimes. To my children: Chinedum Jason and Chidiebube Nathan, words would fail me to express how much I appreciate your shows of love, support, and understanding that kept me strong regardless of the distance apart, I love you so much. Thank you to my parents, siblings, friends, and colleagues for the support and encouragement that helped me attain this height.

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Introduction

1.1 Green Energy Technology

Green energy refers to energy acquired from natural resources like wind, sun, geothermal, water, and biomass [1]. Green-energy technology is advantageous because it replaces the negative impacts associated with using fossil fuels, there is no pollution or water consumption during operation, there are minimal greenhouse gas emissions, future sustainability of power, and no associated noise [2], [3]. Solar energy is a green and relatively affordable source of renewable energy used for electricity generation. A good way of harnessing solar energy is through the use of solar panels to generate electricity. The wattage of a panel is defined by how much electricity is generated by the solar panel under standard illumination and temperature conditions. The average power rating of a panel for residential purposes that would generate about 1.5 kWh of electricity per day ranges between 250 – 400 watts [4]. The panel output is dependent on the size of the panel, angle of tilt, amount of solar irradiation, shading, weather conditions, dust accumulation, etc. To improve energy sustainability and the rate of power utilization in solar panels, energy storage is sometimes incorporated into the panel setup. One of the most practical applications of green-energy technology is using solar panels for electricity production through the photovoltaic process.

1.2 Photovoltaic Technology

Photovoltaics (PV) generally involve the use of semiconducting materials in PV devices for solar-energy conversion into electric current [5]. These materials could be monocrystalline or multi/poly crystalline. Monocrystalline devices are typically fabricated with a single material and are usually more efficient and have fewer defects than the polycrystalline form. Polycrystalline devices are made from several materials, are more cost-effective, but commonly have more defects present in their structure. The performance of PV modules can be rated under ideal testing conditions of 1000 W/m^2 irradiance with the use of a solar spectrum of air mass (AM) 1.5G, and a temperature of 25 ^oC. The actual performance of each panel depends on the location, amount of solar irradiance, time of the day, shading, temperature, and various other factors [6].

1.3 Background of the Study

Solar energy is energy from solar radiation that is emitted at a range of wavelengths in the spectral irradiance as illustrated in Figure 1.1. The solar spectrum shows that the maximum solar energy that is utilized is typically absorbed in the visible spectrum [7]. Overall, the solar radiation is composed of about 5%, 42%, and 53% ultraviolet, visible, and infra-red radiations, respectively. The different colors of light seen in the visible spectrum are blue (400 to 495 nm), green (495 to 570 nm), yellow (570 to 600 nm), and red (620 to 750 nm). The red and gray shadings show the spectral irradiation as a function of wavelength within the ultraviolet (below 380 nm) and infrared (above 750 nm) regions. To estimate the band gap energy of a material that would be used to absorb energy from the sun, the wavelengths in the solar spectrum can be converted to photon energy. As light from the sun falls on a PV panel, carriers within the individual solar cells are spontaneously energized, become mobile, and could be collected for

electricity generation. The concentration of the carriers is affected by the dopant concentration, temperature, band gap of the semiconducting material, and is often reduced in materials with high band gap and under low operating temperatures [8].

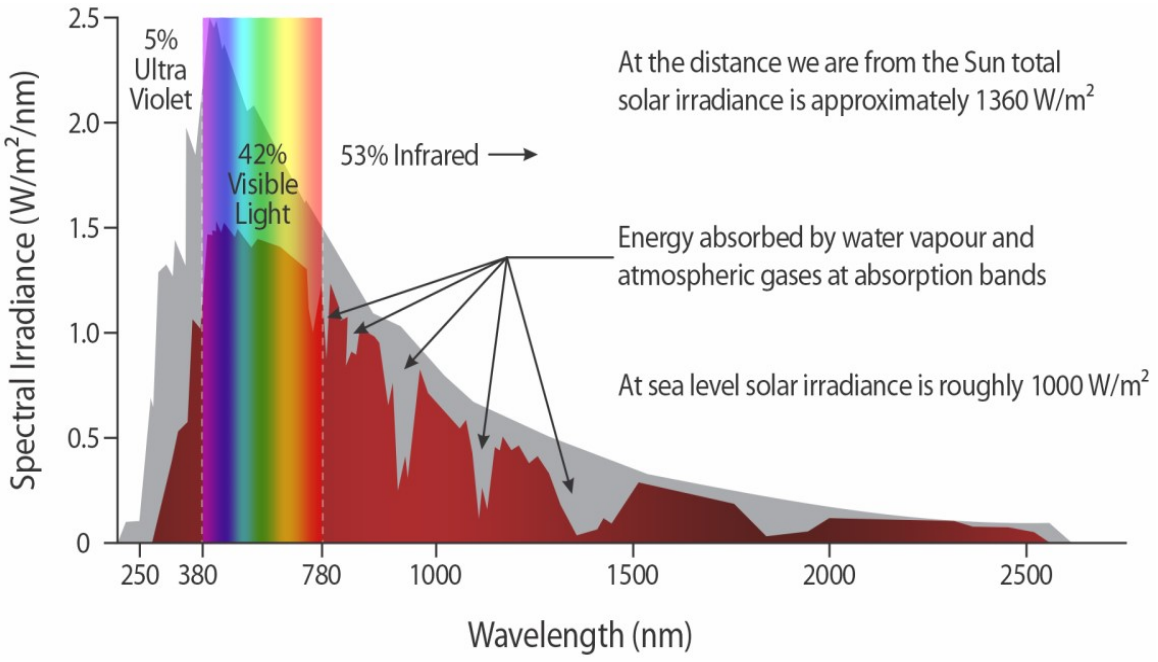

Figure 1.1: Image showing the spectrum of solar radiation [7].

Doping is an effective method of introducing impurities to a semiconductor to increase carrier concentration and improve the material properties of the semiconductor. The doping material may also improve the quality of the device interface and impact defects at the grain boundaries. Primary interfaces in the device are found at the buffer/absorber and absorber/back metal contact. The polycrystalline nature of the device encourages the growth of grains and subsequent defects at the boundaries; which often reduce the device efficiency. The dopant introduces more carriers, referred to as extrinsic carriers which diffuse across the junction and actively participate in conduction.

The diode junction is the region between electron-and-hole-dominated carriers in a semiconductor such that a built-in potential opposes the flow of the carriers across such junction. As the carriers enter the junction, recombination of oppositely charged carriers is likely to occur. The distance a carrier travels after it is generated until it recombines is its diffusion length and is a function of its lifetime. This recombination is associated with the lifetime and diffusion length of the minority carrier, and it reduces the carriers available for external current. The higher the doping density, the greater the recombination rate in general and the shorter the diffusion length in a semiconductor material [9]. Recombination can be radiative, which is prevalent in direct band gap materials where oppositely-charged carriers recombine, giving off electromagnetic radiation with an energy that is approximately the energy band gap, defect recombination where a carrier recombines through an impurity state within the band gap, or Auger recombination where carriers recombine and give off energy to another charge in the conduction band.

1.3.1 Semiconductor Materials

Semiconductors are materials whose electrical conductivities lie midway between those of a conducting and insulating material. The energy band gap of a semiconducting material is the lowest energy needed for valence-to-conduction band excitation of an electron. It gives the energy range where no electronic states or defects from dopants exist within a solid and should typically be less than 3.0 eV under room temperature. The band structure describes the insulating property of semiconductors at absolute zero temperature, beyond which the metal acts as a semiconductor. Some of the semiconductors used in photovoltaic devices are silicon (Si), germanium (Ge), cadmium telluride (CdTe), gallium arsenide (GaAs), and cadmium sulphide (CdS); as well as several others and various alloys. These semiconductor materials contain

conductive electrons and/or holes, have tunable electrical conductivities, and in some cases have variable energy band gap values which determine the electrical conductivity. The conductivity range is a consequence of the band structure which describes the behavior of electrons in the semiconducting material. The applications of semiconductors in photovoltaics are related to the band gap energies which best match the solar spectrum, while their electronic and optical properties can be altered by doping in a controlled process.

1.3.2 Semiconductor Diodes

Semiconductor diodes are electronic devices that limit the flow of current to one direction. These diodes are connected in series to create solar panels. The forward-bias condition is when the positive terminal of the diode receives a voltage generated by the solar photons. Here, the built-in potential, depletion width, and barrier height decreases. The built-in potential, V_{bi} is the potential difference generated across the depletion region of a semiconductor device in thermal equilibrium due to the diffusion of electrons across the junction. The depletion region is an insulating region within the hole/p-type-electron/n-type (p-n) junction with no mobile charge carriers. It is a space-charge region that acts as a barrier to carrier transport. Barrier height (Φ_b) is the energy that an electron at the Fermi level needs to transition into the conduction band of the semiconductor. The overall barrier voltage (V_b) becomes the difference between the built-in potential (V_{bi}) and the applied potential (V).

1.4 Solar Cell Parameters

The electrical properties of solar cell devices allow for better insight into the factors which contribute to their behavior when exposed to solar irradiation. They include maximum power (P_{max}, measured in watts), open-circuit voltage (V_{OC}, measured in volts), short-circuit current

density (J_{SC}, measured in milliamps per cm^2), efficiency (η in %), and shunt/series resistance (R_{Sh}/R_S in ohm/cm^2). The current density-voltage (J-V) measurements are generally done first to get useful solar cell parameters from each cell in the fabricated device. A schematic J-V curve and circuit diagram are shown in Figure 1.2 [10].

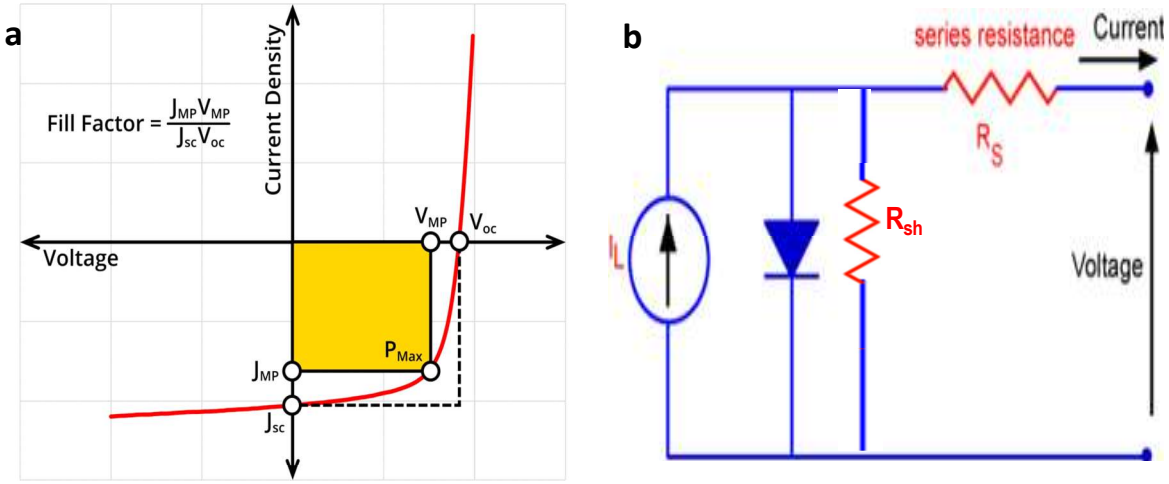

Figure 1.2: Graphical illustration of a) J-V parameters b) series/shunt resistance circuit [10].

1.4.1 Short circuit current-density

Short circuit current-density or J_{SC} is the current generated in a solar cell per unit area when the voltage is zero. It represents the highest current that is generated by a solar cell under standard testing conditions. The J_{SC} is approximately proportional to the illumination.

1.4.2 Open-circuit voltage

Open-circuit voltage (V_{OC}) is the voltage obtained in the absence of an external load connected to the output circuit; thus the current produced at this point is zero. It describes the maximum voltage that can be generated under standard testing conditions. The V_{OC} of a device is negatively affected by higher temperatures.

1.4.3 Maximum Power

The maximum power (P_{max}) is the highest power gotten from multiplying the voltage and current. This occurs at a voltage that is less than the V_{OC} as shown in Figure 1.2a [11]. It is the maximum power point obtainable from the J-V curve. The current and voltage at this point are referred to as J_{MP} and V_{MP}. This $P_{max} = J_{MP}V_{MP}$.

1.4.4 Fill factor

The fill factor (FF) represents the extent of squareness of the current-density curve and it is another component of the cell's efficiency. It gives the ratio of the cell's maximum power to the product of its open circuit voltage and short circuit current density [$Pmax/(V_{oc}*J_{sc})$] and is a key factor in determining the power output. FF decreases with higher series resistance and in turn decreases the efficiency of the device.

1.4.5 Efficiency

Efficiency (η) is the ratio of the power generated under standard testing conditions to the incident solar power. The efficiency value can be obtained by dividing the product of FF, J_{SC}, and V_{OC} by an input power of 100 mW/cm^2. As temperature increases, the cell's voltage and fill factor will decrease and the efficiency will be smaller.

1.4.6 Cell Resistances

The resistances affecting solar-cell performance are series and shunt resistances. Series resistance, R_S is caused by the movement of current through the cell, movement of carriers through the top layer, and resistance at the contact [12]. The main influence of R_S is to reduce the fill factor which can be seen as a decrease in the squareness of the J-V curve. R_S does not affect

the cell at V_{OC} since the current there is zero. Shunt resistance, R_{SH} results from leakage through the diode. R_{SH} creates a lower-resistance path to current from this conductance. The junction could have a partial shorting due to the recombination of the carriers at the junction which reduces their lifetime [13]. Conductance, G is the inverse of shunt resistance ($1/R_{SH}$). As the length of the conductor increases, the conductance decreases with increasing resistance [14]. Conductance has units of Siemens (S) or inverse ohms (Ω^{-1}). The circuit with solar-generated current (I_L), the diode, series and shunt resistances have been shown in Figure 1.2b.

Chapter 2

Cadmium Telluride (CdTe) Solar Cells

2.1 Overview of CdTe Technology

Cadmium telluride (CdTe) is a PV device material that allows for affordable means of producing panels with high conversion efficiency [15]. Currently, it is the second commercialized PV technology after silicon and represents 30% of the US PV market [16]. It is a polycrystalline device that is relatively affordable and chemically stable with a rapid manufacturing process, high absorption coefficient, wide tunable direct bandgap of about 1.4 to 1.5 eV, robust (mechanically resistant) absorber material, lower ionization energy (energy useful for removing an electron from an atom to make it p-type) of about 4.4 eV for every exciton pair, and mobile carriers with relatively long lifetimes [17].

When compared to silicon technology, CdTe has shorter processing time, easier fabrication process, and slower rate of degradation [18]. To enhance the efficiency and V_{OC} of cadmium telluride devices; the minority carrier lifetime, absorber material, and the recombination occurring at the interface and boundaries are the important factors to consider. Cadmium selenium telluride (CST) having a lower band gap energy of about 1.39 eV is often added as a bilayer by directly depositing $CdSe_xTe_{1-x}$ (x=0.4) in front of the CdTe absorber material. This addition has proven useful in improving the minority carrier lifetime, photon absorption, photocurrent/J_{sc} value, and device efficiency.

2.2 Fabrication of CST/CdTe Devices

CST/CdTe absorbers are deposited in the Advanced Research and Development System (ARDS) shown in Figure 2.1 at the Engineering Research Center (ERC) at Colorado State University. Prior to the deposition of the absorber materials, magnesium-doped zinc oxide (MZO) is deposited at the front by radio frequency sputtering technique. It has a wide bandgap value of about 3.6 eV and serves as a window/emitter layer which allows the passage of longer wavelength photons without recombination. CST and CdTe are the primary absorber layers deposited by a rapid and temperature-dependent close-spaced sublimation (CSS) process. This process used to deposit the absorber layer is based on the dissociation of source material while maintaining the source and substrate temperatures within a vacuum pressure of about 40 mTorr. An automated transfer arm undergoes a linear and rotational motion in moving the substrate around the inline sources in the chamber [17]. The close spacing between the source and the substrate provides quick transport of each source through the space and directly deposited onto the substrate. The rate of deposition is influenced by the source and substrate temperatures, pressure in the reaction chamber, separation distance, and the composition of sources. The higher the temperature of the substrate, the larger the grain sizes, which typically result in reduced grain boundary defects [17].

Cadmium chloride ($CdCl_2$) treatment is a good technique for passivating the grain boundaries with chlorine so that defect recombination is reduced. Copper chloride (CuCl) treatment is useful for doping the bulk absorber and reducing the barrier height at the back. Chlorine passivation and copper treatment assist with reducing band bending at the back which would reduce the energy barrier at the back interface. Tellurium is then deposited at the back of the absorber material by thermal evaporation to form a metal back contact and increase hole collection at the back.

Afterward, nickel and carbon paints are sprayed at the back of the layers to serve as the external contact. The devices are then stored in desiccators for subsequent measurements.

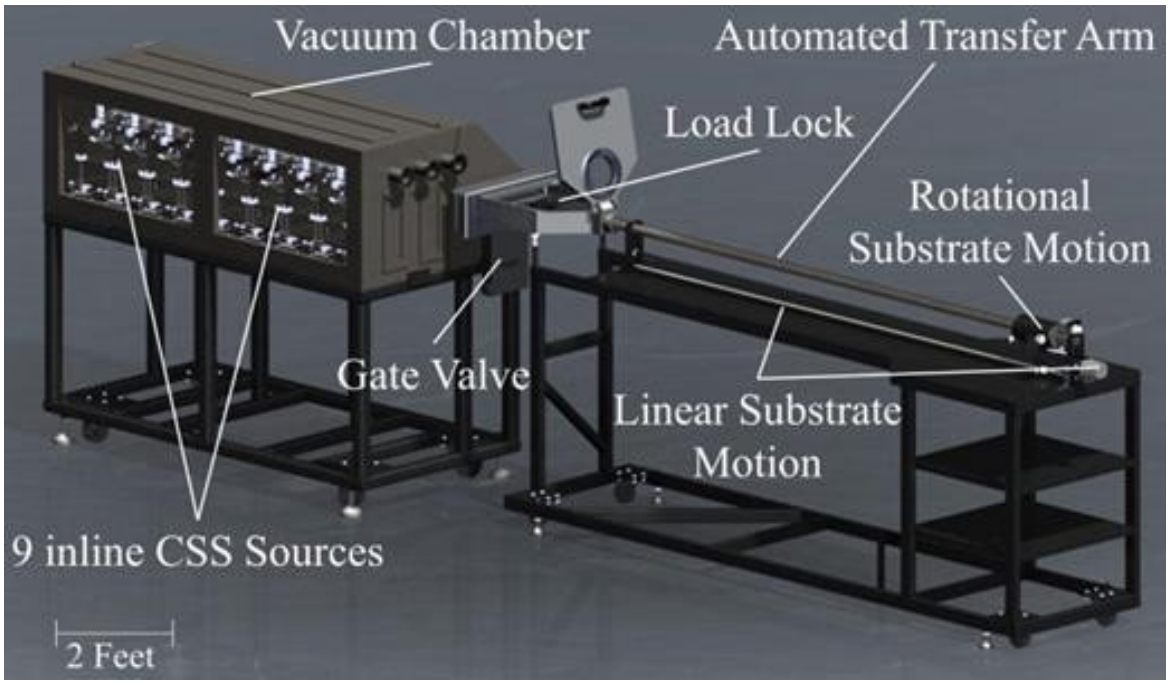

Figure 2.1: Diagram showing the ARDS deposition chamber used at ERC [15].

2.3 Typical CdTe Cell Structure

The schematic structure of a typical CST/CdTe device is shown in Figure 2.2. Tec 10 glass coated with a transparent conducting substrate which is transparent to visible light and is conductive for efficient current transport [17]. Magnesium zinc oxide (MZO) is the n-type front-contact layer and conductive semiconductor that allows light to pass through to the absorber material. This window/buffer layer has a high energy band gap of about 3.6 eV and is highly transparent to solar radiation which increases the photocurrent obtained from the absorber [19], [20].

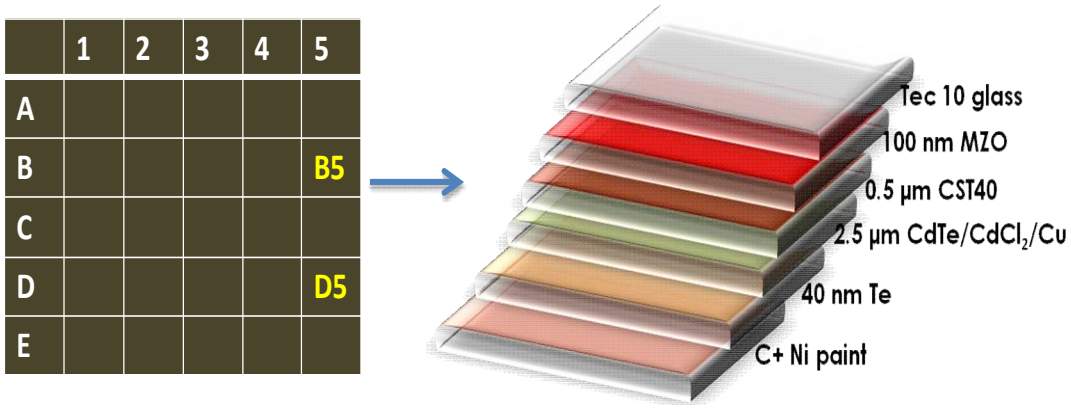

Figure 2.2: Schematic illustration of the CST/CdTe solar cell devices fabricated at Colorado State University.

Cadmium selenium telluride (CST) serves a co-absorber material deposited before the CdTe material and helps to increase the photocurrent and electrical characteristics between the transparent conducting oxide and the CdTe absorber [19]. Most of the light absorption takes place in the CST material which forms a bilayer with CdTe as a p-type bulk absorber layer. For the device shown in Figure 2.2, a 0.5 µm CST material is able to absorb about 72% of the generated photons. CST alloy has a lower band gap energy of ~1.4 eV that increases current collection from the absorber and reduces non-radiative recombination rate. Cadmium chloride ($CdCl_2$) is deposited after the CdTe. It is used for passivating the grain boundaries to minimize structural defects, and re-crystallize the grains [17]. This passivation is a re-crystallization method that involves depositing the $CdCl_2$ material and annealing in vacuum at a temperature of 370 ^{o}C such that the chlorine diffuses along the grain boundaries into the absorber layer. This would minimize majority carrier loss, reduce recombination centers and the concentration of defects, enhancing the grain size, and improving the device efficiency [17]. Copper (Cu) is then deposited and used as a dopant to increase hole carrier concentration and minimize the potential barrier that forms between the absorber and the metal. Copper is a useful dopant for yielding

more conductive holes, reducing energy barrier at the back, and enhancing the p-type density level. This high doping level shortens the diffusion length, reduces recombination, and the concentration of the minority carriers at equilibrium.

The back contact metal (tellurium) is deposited by thermal evaporation while device completion is done outside the vacuum chamber. The tellurium (Te) layer forms a metal-semiconductor interface with the absorber and assists the back electrical contact so that a good contact is established between the CdTe and the external circuit. It is also useful for band alignment, which minimizes the energy barrier at the back for easy hole collection, and to improve ohmic contact at the back. The carbon and nickel paints sprayed on the device serve as back electrode to improve conductivity and enhance the robust nature such that moving the device during measurements does not have any negative impact on the cells.

The cell structure is delineated into squares about 0.6 cm^2 in area by removing the material outside the cell area with small, high-velocity beads. The active areas are protected using a stainless steel mask. Soldering with indium is done around each cell to improve the front contact. Each substrate is typically formed into 25 cells in a 5-by-5 pattern as illustrated in Figure 2.2. The B5 and D5 cells are the primary cells used in this measurement based on their efficiencies.

2.4 Description of CST/CdTe Device Measurements

Several measurements were done to measure the performance and efficiency of each device. Descriptions of the optical, electrical, capacitance, phase angle, electroluminescence, and photoluminescence measurements are presented in this section.

2.4.1 Current-Density versus Voltage Measurements

Current-density versus voltage (J-V) measurement involves externally biasing a device by sweeping different voltage values while measuring the current in the dark and under illumination. These measurements are used to obtain cell parameters like short-circuit current density, J_{SC}, open-circuit voltage, $V_{OC,}$ fill factor, FF, maximum power, and efficiency. The measuring arrangement is a 4-point measurement (two for voltage and two for current) which helps to reduce losses from resistance encountered in the external circuit. Dark measurements inject only electrically-generated carriers into the circuit, while light measurements also inject light-generated carriers that shift the J-V curve in the reverse-current pathway. However, at low temperatures, the J-V curve deviates from the normal diode curve due to a phenomenon called the rollover effect. This roll-over effect is a consequence of a Schottky energy barrier created at the absorber and metal contact interface. It is a current-limiting effect that can hinder hole transport due to a back-contact barrier. The J-V setup used for this measurement with an exaggerated image of the device mount showing the connected pins is shown in Figure 2.3.

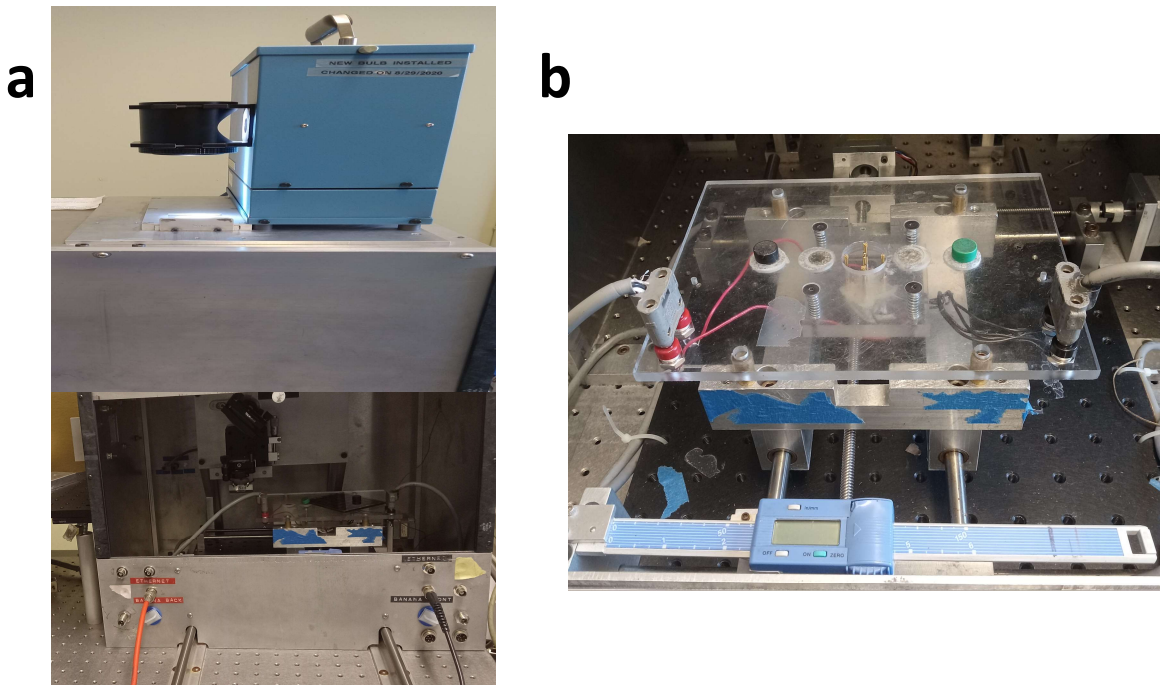

Figure 2.3: a) J-V setup having a solar simulator light source mounted on the lightbox measurement chamber and b) the device mount showing the connection leads used during the measurement.

2.4.2 Capacitance Measurements

A capacitance measurement with a bias across the cell is useful for evaluating the density of carriers, holes for the p-type CdTe. The cell can be modeled as a parallel-plate capacitor with a dielectric in-between and a potential difference across the plates as shown in Figure 2.4. A capacitive circuit dominates when an increase in frequency drops the resistive component to near zero. Capacitance-frequency (C-f) measurements are useful for obtaining the capacitance of the cells as different frequencies are applied. A frequency in the range where the capacitance is relatively constant with frequency is chosen as the measurement frequency for the capacitance-voltage (C-V) measurement which gives the capacitance of the cell as different DC bias voltages are applied. It is then useful for the determination of hole density.

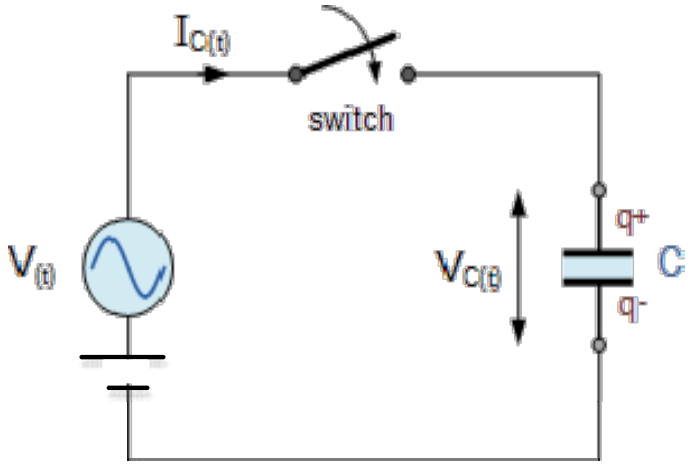

Figure 2.4: Schematic of a parallel-plate capacitor with a biased sinusoidal voltage supply [21].

2.4.3 Phase Angle Measurement

The phase angle of an alternating current (AC) response shows the time difference between voltage and current waveforms in the circuit. Since the device is initially modeled as a capacitor, the resulting waveforms illustrated in Figure 2.5 show the current leading the voltage by 90 degrees in the ideal case. It is important to monitor this measurement because at low phase angle values, the capacitance measurement is no longer accurate. The phase angle is 90 ^{o} for pure capacitors, but is smaller if there is a DC current path (leakage or forward current) in parallel with the capacitance. These measurements utilize an alternating voltage superimposed on a bias voltage.

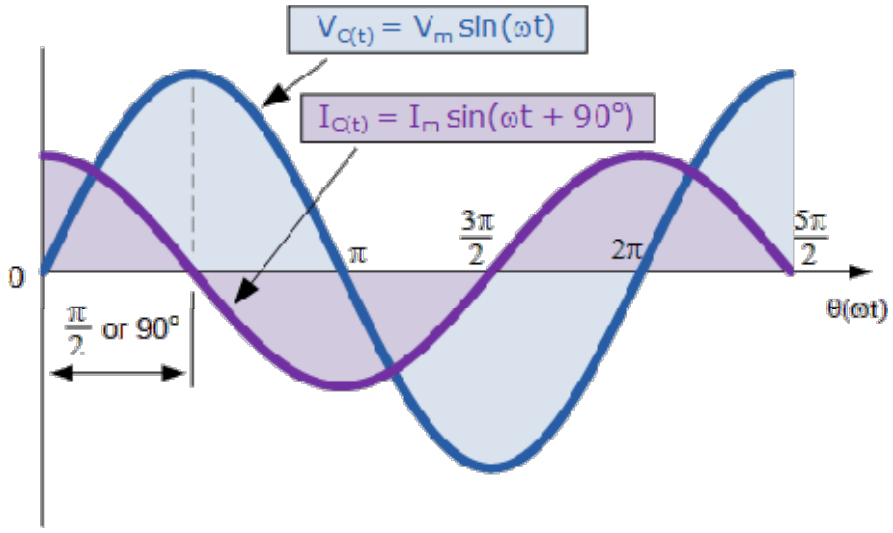

Figure 2.5: Waveforms showing sinusoidal current response to alternating voltage supply in a capacitor [21].

2.4.4 Quantum Efficiency

Quantum efficiency (QE) measurements compare the current generated by an external optical source at specific wavelengths with the incident photons generated at defined wavelengths. QE response is generally measured under short-circuit conditions and is useful in determining the solar cell quality. Internal QE gives the amount of current-carrying charges extracted from the incident photons while external QE measures how well a solar cell converts incident light into electrical current by measuring the free mobile carriers that get transported from the absorber to an external circuit. The QE setup is shown in Figure 2.6 with the light source coming from a halogen lamp. The magnet holds the device firm so that the active cell being measured makes good contact with the pins and electrode.

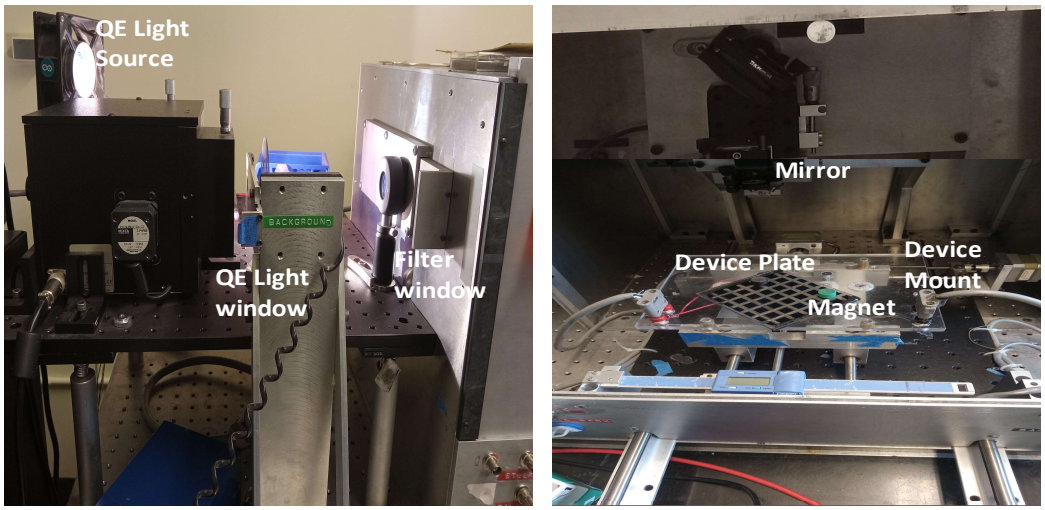

Figure 2.6: QE measurement setup showing the optical and measurement chamber with the same device mount used for the J-V measurement.

2.4.5 Reflectance

Reflectance measurement gives the percentage of incident solar light that is reflected from a solar cell as a function of wavelength. This is done through the ratio of the reflected light to the incident light relative to a reference standard. This measurement is useful in determining how efficiently the device absorbs incident radiation by measuring how much light is reflected from the device.

2.4.6 Electroluminescence (EL) Imaging

Electroluminescence involves emitting light when carriers are injected into an active cell by an external current source. The measurement is carried out in a constant DC current mode with a forward current density (which can be varied, but is typically near J_{sc} around 20 mA/cm^2) in a dark enclosure to avoid light interference. The injected current result in light emission from the cell, and an image is taken of the cell. It is a non-destructive method which compiles spatial

images and shows defects that may be present in the device. The EL intensity among other factors depends on the amount of current injected and the radiative recombination rate. During the EL process, internal losses due to charge injection/recombination and losses due to the absorption of the emitted light are used to reveal defect states. As current through the cell increases, the rate at which the electrons are ejected from the cell increases and leads to increased luminescence.

2.4.7 Spectral Photoluminescence (PL) Measurements

PL is also a non-destructive process used to probe the electronic properties of a device by measuring the intensity of the emitted radiation as a function of wavelength. Here, a laser light shines on the cell through the front to generate photocarriers which get excited to higher energy levels. The excited photons/electron-hole pairs are able to emit light when they radiatively recombine. The intensity of the emitted light and its spectral dependence are important features that help in estimating the energy band gap value at the PL peak emission wavelengths. The intensity and broadening of the primary PL peak, and the presence of additional peaks reveal how much defects are present in the cell.

2.5 Goal of the Research

This research aims at characterizing cadmium selenium telluride/cadmium telluride (CST/CdTe) solar cell bilayer devices. The best performing cells (B5 and D5 as illustrated in Figure 2.2) were measured to obtain their current-density (J-V), quantum efficiency, reflectance, capacitance, phase angle, electroluminescence and photoluminescence characteristics. The results obtained were useful in investigating the performance of these devices.

Chapter Three

Characterization of CST/CdTe Devices

Several cadmium selenium telluride/cadmium telluride (CST/CdTe) bilayer devices were fabricated and basic solar cell measurements were made on the cells. The two cells labeled B5 and D5 according to their position on the deposition plate illustrated in Figure 2.2 were chosen for detailed measurement and analysis. This selection was based on the efficiencies obtained from the array of cells.

3.1 Cell Preparation

Prior to film deposition, TEC10 substrates were cleaned with ultrasonic detergent and isopropyl alcohol, rinsed in water, dried, and stored in desiccators. The CST/CdTe bilayers were deposited in an Advanced Research and Development System (ARDS) while the MZO front-contact layer was made in a radio frequency (RF) sputtering system. Details of the fabricated layers, treatments done, device completion, and the role played by each layer have been described in sections 2.2 and 2.3.

3.2 Measurement Equipment

The current-density (J-V), capacitance, and quantum efficiency measurements were done in a lightbox chamber with the device mounted within. J-V light and dark data were obtained using a calibrated gallium arsenide (GaAs) reference cell. Keithley 2401 source meter generates a bias

which gets measured using a Hewlett Packard 34401A DC mode multimeter. A Solar Light Company model XPS of 400 Xenon lamp served as the source of illumination. For the low temperature J-V measurement; a Piezzoelectric transducer and a thermocouple were used to drive and monitor the temperature while cold nitrogen gas was flown into the chamber to cool the cell during the measurement. The thermocouple is taped to the front where the back contact of the device makes contact with the copper block while two pieces of metal were also used to improve electrical conductivity with the device. A 60% neutral density filter was also inserted to account for the height difference and reduce the light intensity by blocking some of the incoming light. The phase angle and capacitance two-point measurements were done using a Keithley 230 DC power supply, Hewlett Packard (HP) 4192A impedance analyzer, HP 33401A multimeter with 20 seconds pre-bias cell at a measurement frequency of 100 kHz. The front, back, and front-to-back contacts should record resistance values of $\leq 1\ \Omega$, $\leq 5\ \Omega$, and $k\Omega$ values respectively. The devices were set at a measurement frequency of 100 kHz and biased at -2 V, -1 V, 0 V, and 0.2 V for the capacitance measurement.

The QE two-point measurement was done using a silicon UV reference for re-calibration of the cell without bias voltage at a frequency of 10 Hz, and a 620 nm long-pass 6-decibels filter. Reflectance data were obtained within 350 – 900 nm wavelengths by mounting the device in a Perkin Elmer spectrometer box having a halogen lamp after recalibrating with a ThorLabs mirror of UV-enhanced aluminum. EL measurement was made under constant forward current using Micromanager 1.4 software for data acquisition, Image J software for image processing, a Hewlett Packard 34401A multimeter and an Agilent E3611A DC power supply. PL measurement was done using a S2000 Photoluminescence spectrophotometer synchronized with

a silicon detector, 520-nm laser, a filter to block reflected light, and a constant power mode of 15 mW.

3.3 Cell Measurements and Analysis

3.3.1 Current-density (J-V) measurements

Current-density measurement allows a direct voltage sweep across the device at different biases under dark and light measurement conditions to obtain current per unit area. The J-V plot in Figure 3.1 shows increasing current-density values as voltage is increased with forward bias. The D5 cell recorded slightly more J_{SC} value as compared to the B5 cell. Losses in J_{SC} can be accounted for in the QE measurement. The short circuit current density, open circuit voltage, fill factor, and efficiency values obtained from the D5 and B5 cells as given in Table 3.1. The parameters outlined are useful for evaluating the performance of the device and can be obtained directly from Figure 3.1. It can be observed that the D5 cell recorded slightly higher V_{OC}, FF, J_{SC}, and efficiency values. The fill factor is also seen to increase with efficiency. The limitation in V_{OC} is largely due to recombination occurring in the absorber and at the back interface, while the reduction in the J_{SC} is primarily due to optical losses as light enters through the window layer. The limiting hole current, J_h is determined using the diode equation shown in Eq. 3.1 [18], [22].

$$J_h = J_o\,(\exp\,(qV/AkT) - 1) \tag{3.1}$$

J_o is the saturation current at the back contact, q is the electronic charge, V is the voltage applied, k is the Boltzmann constant, T is the cell temperature, A is a dimensionless diode quantity factor that is a measure of the recombination loss. Series and shunt resistance will modify Eq. (3.1) to some degree depending on the device quality.

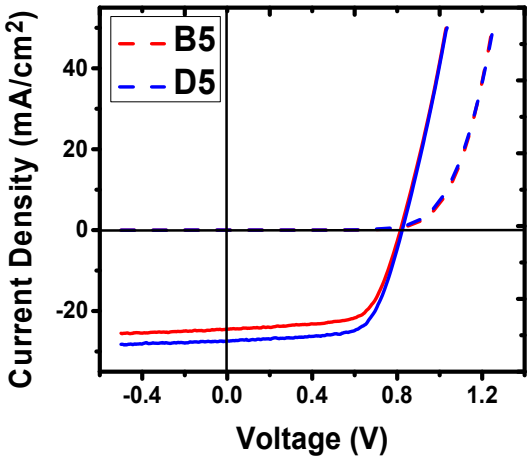

Figure 3.1: J-V plots of the measured CST/CdTe devices.

Table 3.1: Obtained J-V parameters of the measured CST/CdTe device.

Samples	Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
2150-3-B5	0.629	0.819	24.6	66.5	13.4
2150-3-D5	0.636	0.824	27.4	67.3	15.2

3.3.2 Low Temperature Current Density (J-V-T) Measurement

This measurement describes the cell's response to low-temperature variations ranging from 323 K to 213 K. Cold nitrogen gas was flowed into the light box chamber to keep the measurement temperature low and minimize frosting. At low temperatures, a rollover effect was observed in Figure 3.2 as a result of the energy barrier evident at the absorber/back-contact interface that limits current [23]. It is likely explained as a weak diode at the back in series with the primary diode. The carriers become less energized at lower temperatures and have the ability to overcome small barriers; thus, limiting current densities at higher forward bias. Hence, current transport at higher voltages exists within the low barrier rollover region. Table 3.2 outlines the J-

V-T parameters obtained from the low-temperature measurements and shows that 273 K is the approximate temperature at which the rollover sets in as highlighted. It can be observed that as the temperature drops, the V_{OC} increases to about 1 V due to reduced recombination. This value is close to the maximum theoretical value of 1.2 V for CdTe devices. At these low temperatures, fewer carriers participate in the external current as they have less energy to overcome high-energy barriers, hence accounting for J_{sc} losses. At increasing temperatures, J_{SC} increases as more photons gain enough energy to overcome the barrier and be conducted. Lower temperatures also increase series resistance which also drop the fill factor and device efficiency. The solar cell parameters obtained at room temperature (about 293 K) from this J-V-T measurement are less than those gotten during the J-V measurement. This is because a filter is added to block some of the incoming solar light and account for a height difference since a higher mount is used during the J-V-T measurement.

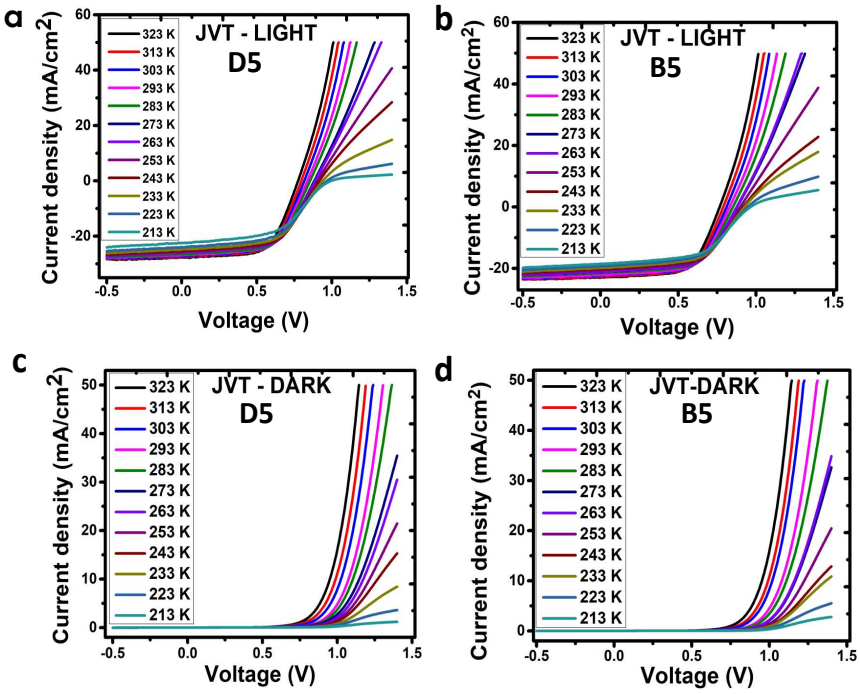

Figure 3.2: J-V-T plots for the cells measured under (a-b) light and (c-d) dark conditions.

Table 3.2: J-V-T parameters obtained from the (a) D5 and (b) B5 cells

a

Temp. (K)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
323	775	27.6	63.0	13.5
313	796	27.5	62.8	13.7
303	816	27.3	62.1	13.8
293	837	26.9	61.6	13.9
283	855	26.5	61.1	13.9
273	883	26.3	60.8	13.8
263	889	25.8	60.0	13.8
253	904	25.6	59.0	13.6
243	917	25.4	57.9	13.5
233	939	24.7	56.4	13.1
223	967	24.0	54.0	12.5
213	996	22.4	50.9	11.4

b

Temp. (K)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
323	766	27.6	62.8	11.0
313	789	27.5	62.9	11.3
303	811	27.3	62.8	11.4
293	831	26.9	61.9	11.3
283	852	26.5	61.7	11.3
273	876	26.3	60.1	11.2
263	879	25.8	60.7	11.2
253	889	25.6	59.7	11.0
243	918	25.4	58.1	10.8
233	926	24.7	57.5	10.5
223	946	24.0	55.9	10.2
213	966	18.5	54.5	9.7

3.3.3 Barrier Height Determination at 213 K and 233 K

To estimate the barrier height of CdTe devices from Eq. 3.2, the transport of carriers at the semiconductor-metal interface is modeled as a thermionic emission process while ignoring effects from other forms of current transport. During the thermionic process, the barriers at the back of the cell can suppress hole transport and produce a second depletion region at the semiconductor surface [24]. The barrier height for p-type devices is influenced to a small degree by temperature and gives the difference in energy from the valence band edge to the Fermi level. Figure 3.3 gives a relationship between the current density and voltage at the lowest rollover-observed temperatures. This analysis is useful in determining the barrier heights using the thermionic emission equation shown in Eq.3.2 [24]. The point of intersection of the linear fits as the current density transits from the positive to the negative slope of the J-V curve gives the turning current density, J_t [25].

$$J_t = A^* T^2 \, e^{-\left(\frac{q\Phi_b}{kT}\right)} \qquad (3.2)$$

where Φ_b, k, q, T, J_t, A^* represent the barrier height, Boltzmann's constant (1.38×10^{-23} J/K), charge, temperature, turning current density, and effective Richardson constant in A/cm^2K^2.

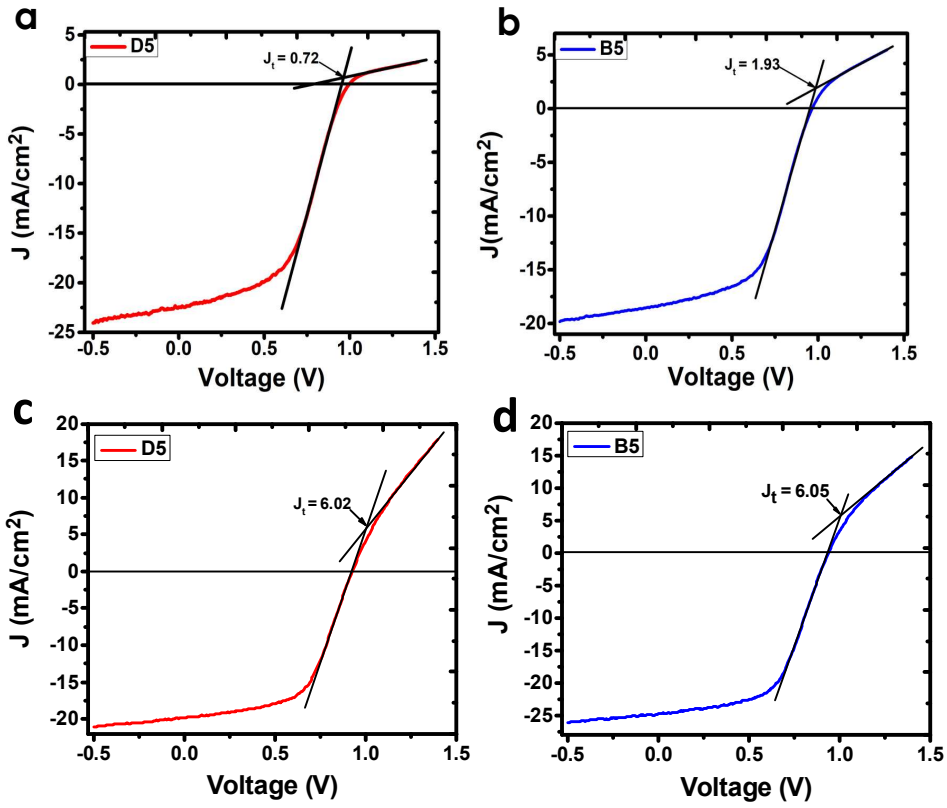

Figure 3.3: Determination of J_t from the J-V plots for the D5 and B5 cells measured at (a-b) 213 K and (c-d) 233 K.

Table 3.3 shows the turning current densities and barrier heights obtained from the cells at 213 K and 233 K. The Schottky barrier evident at the back is a potential energy barrier for the minority carriers and regulates electron transport across the metal-semiconductor surface. It originates from a mismatch in the energy levels of the majority carriers (holes) at the interface between the metal and semiconductor. p-type semiconductor devices have been reported to need

barrier heights that are less than 0.6 eV, for a cell to be effective at room temperature [26]. The values obtained for the barrier height in Table 3.3 agree with this general rule as D5 gave lower barrier heights as compared to B5. The lower barrier heights allow greater transport of the minority carriers (electrons) across the barrier.

Table 3.3: J_t and Φ_b values obtained from the D5 and B5 cells obtained at 213 K and 233 K.

Temp. (K)	Cell	J_t (mA/cm ^{2})	Φ_b (eV)
213	D5	0.72	0.37
	B5	1.93	0.39
233	D5	6.02	0.37
	B5	6.05	0.38

Lower barrier heights obtained at higher temperatures are also indications of the reduced resistivity at the contacts which gives room for increased minority carrier transport. Incorporating copper as a p-type dopant also accounts for the reduced barrier heights at the back. The cells recorded some variation in the barrier height due to the reduced band bending at varying temperatures [27]. The relatively low barrier height values positively impacts the two cells by minimizing resistance to hole collection at the back [28].

3.3.4 V_{OC} versus Temperature Plots

The relationship between V_{OC} and temperature is plotted in Figure 3.4 and shows increasing open circuit voltage values as the temperature decreases. The slopes and intercepts of

the D5 and B5 cells were estimated by linearly extrapolating the plot to 0 K. As the temperature drops towards 0 K, the V_{OC} extrapolation is useful in validating the accuracy of the low temperature measurement as the values should be close to the band gap of the absorber. Intercept values of 1.39 eV gotten for D5 and 1.34 eV for B5 are in fact reasonably close to the band gap of the CST absorber. The slopes obtained were approximately -2 mV/K and correspond to what should be expected during the measurement. The point of inflection observed near 273 K is the point where the rollover effect is first observed as shown in Figure 3.2 discussed earlier.

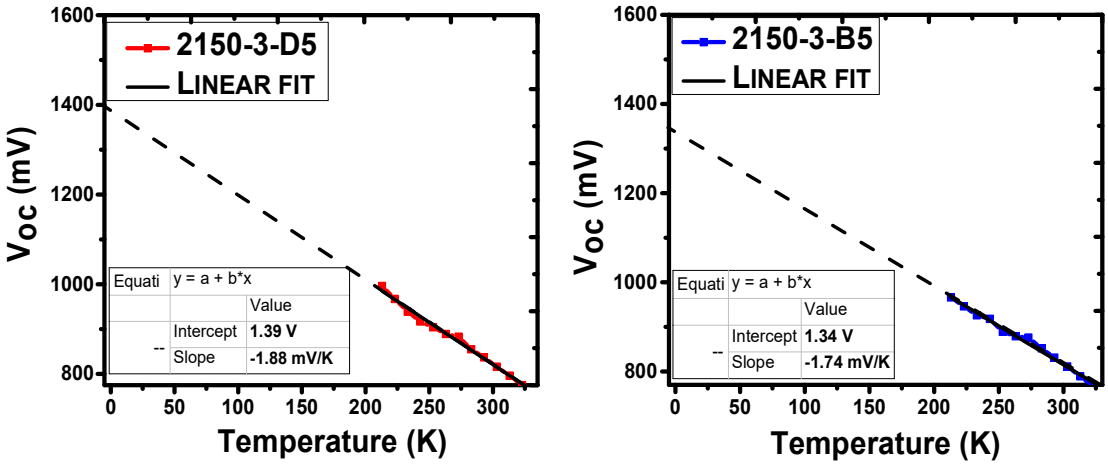

Figure 3.4: V_{OC} versus temperature plots of the (a) D5 and (b) B5 cells.

3.3.5 Capacitance measurements

Capacitance measurement is done by modeling a diode as a parallel-plate capacitor with a dielectric in-between and as a one-sided junction where the depletion is on the CdTe side. Each plate is considered as a conductive metal with the negative plate having many free electrons within. The capacitance of a diode measures its capacity to store electrical charge when connected to an alternating current supply. Since the depletion region will vary with voltage,

application of an external bias can be used to determine the carrier density (holes in this case) of the solar cell absorber.

3.3.5.1 Capacitance-Frequency (C-f)

The C-F measurement was done to show the frequency range where the capacitance of the cell is nearly constant with frequency. Figure 3.5 shows that this is the case for frequencies from 10 to 300 kHz. This convenient range is possible because of minimal resistance in the cells and minimal impact of trapping states. 100 kHz frequency was chosen as the usual frequency for capacitance-voltage (C-V) measurement.

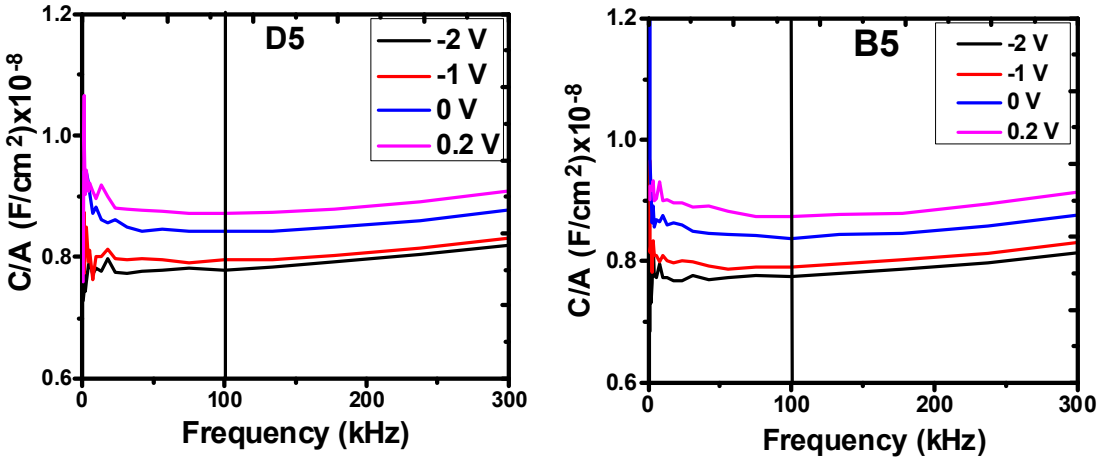

Figure 3.5: Capacitance-Frequency plots of the measured CST/CdTe device.

3.3.5.2 Capacitance-Voltage (C-V)

This C-V measurement relates the capacitance of the solar-cell diode to the voltage across it as shown in Figure 3.6. The plot gave constant capacitance values in reverse bias values due to wider depletion width. A steady increase in the capacitance values were recorded at the forward-biased regions. The capacitance, C was obtained at different biases using the capacitor formula of a one-sided junction shown in Eq. 3.3 [29].

$$C(V) = \varepsilon A/W = Q/V \tag{3.3}$$

where ε, A, Q, V represent the dielectric constant, cell area, amount of stored charge, applied voltage respectively. The dielectric constant, ε measures the extent to which the device can store electrical energy.

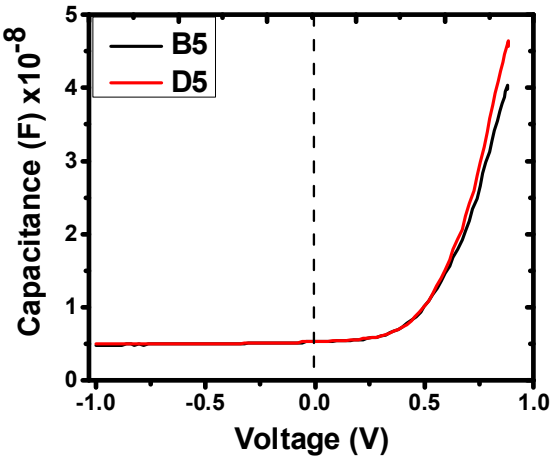

Figure 3.6: Capacitance versus voltage plot of the cells.

To estimate the hole carrier density, p(W) and further understand the relationship between the area per unit capacitance of the cells at different applied DC voltages, the Mott-Schottky plot in Figure 3.7 was made using Eq. 3.4 [30] and the data from Figure 3.6. The non-linear curve reflects imperfections and defects in the fabricated device which takes the shape away from the ideal linear pattern [25]. The capacitance values increase as we sweep from reverse to forward bias values. The dotted line at zero bias is highlighted for reference to differentiate the capacitive behavior of the material in forward and reversed bias conditions.

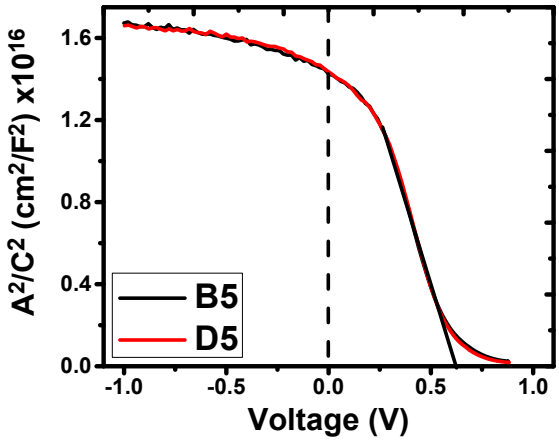

Figure 3.7: Mott-Schottky plots of the measured CST/CdTe device.

The slope of the solid line in the Mott-Schottky plot gives the carrier density at the edge of the depletion region as a function of voltage. A hole carrier density of $4x10^{14}$ cm^{-3} was gotten from the slope in the region between 0.2 V and 0.5 V. To determine the potential difference due to uneven carrier concentration as the electrons diffuse across the depletion region, the diffusion voltage, V_D was estimated. A diffusion voltage (V_D) of 0.63 V was obtained from the intercept on the voltage axis by extrapolating the linear portion of the curve. The voltage at which no electrical charge is measured at zero capacitance during the prebias stage could be taken as the built-in potential near 0.9 V. The diffusion voltage can also be inserted into Eq 3.5 to calculate the built-in potential, V_{bi} of the diode [25].

$$\left(\frac{A^2}{C(V)^2}\right) = \frac{2(V+V_D)}{q\varepsilon p(W)} \tag{3.4}$$

$$qV_{bi} = \varphi_b = E_{F,p} + qV_D \tag{3.5}$$

where A is the active area of the cell, C (V) is the capacitance due to the applied voltage, V_{bi} is the built-in potential, V is the applied voltage, q is the electronic charge, ε is the dielectric

constant, p (W) is the hole carrier density as a function of the depletion width, $E_{F,p}$ is the hole Fermi level of the donor material, φ_b is the barrier height.

3.3.6 Carrier Density Measurement

The hole carrier density, p(W) estimated over different distances from the junction is given in Figure 3.8. The distance from the one-sided junction shown on the x-axis corresponds to the depletion width, W. It is voltage-dependent and describes the region of charge accumulation around the junction. Near the junction, the high carrier density could also be due to high conductance of the carriers. As the distance from the junction increases; the electric field becomes stronger, depletion width increases and the carrier density drops over longer distances. This diffusion causes the density of majority carriers to drop as they recombine with the minority carriers and hence, leads to slight reduction in the hole carrier density [31]. The hole carrier density, p(W) and depletion width (W) were calculated using Eq. 3.6 and Eq. 3.7 [30].

$$p(W) \sim \frac{C^3 \Delta V}{q \varepsilon A^2 \Delta C} \tag{3.6}$$

$$W = \sqrt{\frac{2\varepsilon(V_{bi} - V_D)}{qp(W)}} \tag{3.7}$$

CdTe devices usually have a U-shaped carrier density curve which is prevalent in thin absorber layers with deep levels [32]. The left side of the curve represents the C-V forward bias region with reduced depletion width and is due to the presence of shallow levels present at the front junction. The rightmost side obtained at greater distances/wider depletion widths corresponds to the C-V reverse bias region. The right side can be seen as nearly vertical if full depletion occurs especially for thin absorbers with deep defect levels. This is clearly not the case for our measured cells as the Mott-Schottky plot did not show any flat-band around the zero bias

regions to depict full depletion. Transiting from the forward to the bias region produces a trough at the middle portion which corresponds to deep levels prevalent at the back. By tracing the base of the trough to the vertical axis gives a hole carrier density value of $4x10^{14}$ cm^{-3} near 0.7-µm distance from the junction as seen in Figure 3.8. The high apparent carrier density of the holes at larger distances from the front is in agreement with the low barrier heights obtained earlier and could also be due to a low phase angle which will be discussed subsequently.

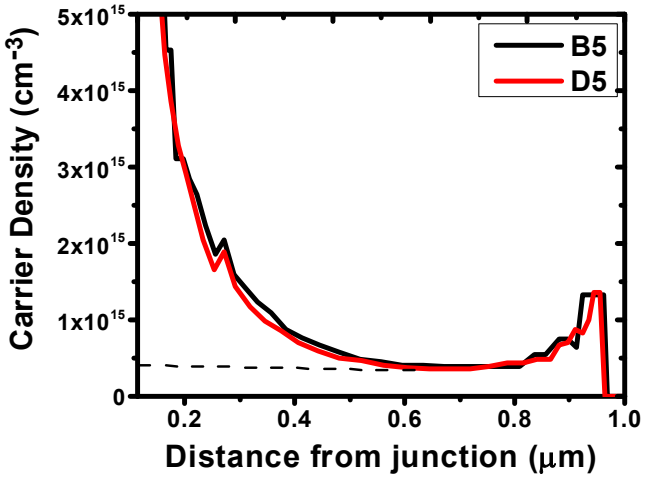

Figure 3.8: Carrier density plot versus distance from the junction.

3.3.7 Phase Angle measurement

The phase angle of the impedance as a function of frequency and voltage is plotted in Figure 3.9 and Figure 3.10 [31]. This phase angle emanates from the time delay to alternating current response during capacitance measurement [21]. For AC capacitance, the maximum possible phase shift for ideal capacitors is 90 ^{o} as the sinusoidal current (I) leads the voltage (V) as shown in Eq. 3.8. For reliable impedance measurements, the phase angles should not be below 50 ^{o} as it reflects high conductance. The maximum current, I_{max} flowing through the AC circuit is given by Eq. 3.9. The total impedance, Z of an AC capacitive circuit is commonly described as a

real resistive component, R and an imaginary impedance called capacitive reactance, X_c as described in Eq. 3.10 and Eq. 3.11. These parameters combine to give a phase angle relation shown in Eq. 3.12.

$$V_c(t) = V_{max}\sin(\omega t) \text{ and } I_c(t) = I_{max}\sin(\omega t + 90^o) \quad (3.8)$$

$$I_{max} = \omega C V_{max} \quad (3.9)$$

$$Z^2 = R^2 + (jX_C)^2 \quad (3.10)$$

$$X_c = \frac{1}{2\pi fC} = \frac{1}{\omega C} \quad (3.11)$$

$$\phi = \tan^{-1}\left(\frac{X_c}{Z}\right) \quad (3.12)$$

where $V_c(t)/I_c(t)$ is the voltage/current flowing through the capacitor in volts/amperes, V_{max}/I_{max} is maximum voltage/current, $\omega=2\pi f$ is the angular frequency in radians per second, Z is the total impedance in Ohms, R is the resistance flowing through a resistor in ohms, f is the frequency in radians, X_c is the capacitive reactance in ohms, and ϕ is the phase angle in degrees.

3.3.7.1 Phase Angle versus Frequency

Figure 3.9 gives the relationship between the phase angle and frequency by determining the alternating current response to applied voltage. The phase angle is induced by the impedance and gives the phase difference between the voltage and current. At low frequency values, the phase angle is high to reveal information about the capacitive nature of the material. The cells recorded a maximum phase angle of about 88 ^{o} that is slightly lower than the maximum due to a small shunt resistance that could cause current leakage through the plates. The high phase angles were observed for the different biases due to low conductance [33].

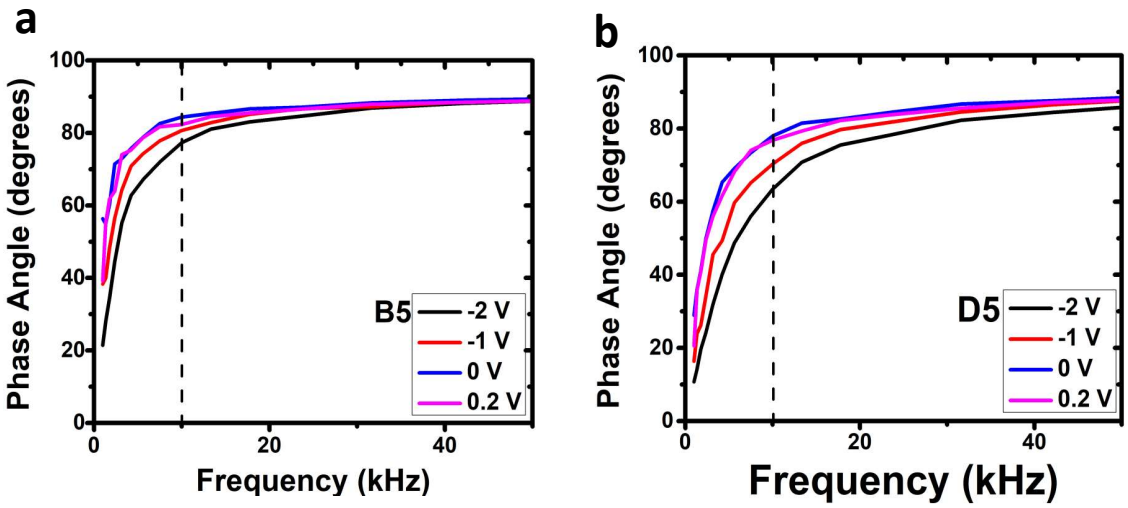

Figure 3.9: Phase angle versus frequency plots of the measured CST/CdTe device.

3.3.7.2 Phase Angle versus Voltage

The relationship between the phase angles as a function of voltage measured at 100 kHz is shown in Figure 3.10. Applying different biases gave phase angle values of 88 ^{o} that are near their ideal value and corresponds to the phase angle values earlier gotten as a function of frequency. As more positive AC voltage is supplied, the phase angle is maintained until about 0.4 V where the diode current turns on and drops the phase angle due to high conductance until no phase angle is recorded near 0.9 V. The voltage corresponding to the phase angle limit of 50 ^{o} is 0.8 V. This drop in the phase angle is due to high conductance at increasing voltages.

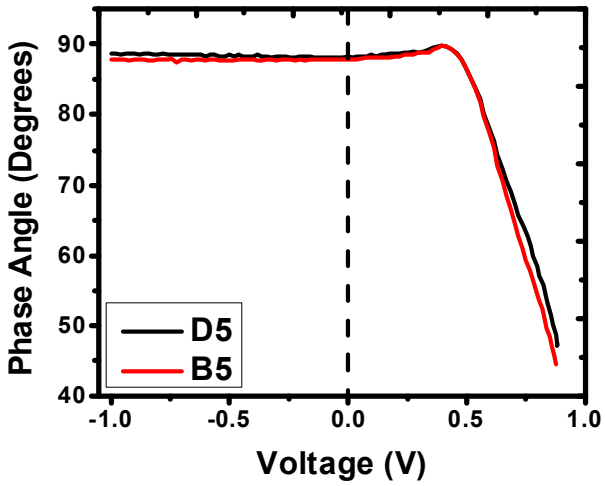

Figure 3.10: Phase angle versus voltage plots for the measured CST/CdTe devices.

3.3.8 Reflectance and Quantum Efficiency (QE) Measurements

The reflectance and external QE measurements plotted in Figure 3.11 were taken at wavelengths from 350 nm to 900 nm. The reflectance plot gives the percentage of light that gets reflected from the device upon exposure to light. Maximum reflectance values of 12.6% and 11.2% were recorded for the B5 and D5 cells. These percentages show reflectance losses from the glass and conducting substrate which reduce the amount of incident light reaching the cell. These losses directly account for reduction in J_{SC} values.

Figure 3.11 also shows the external quantum-efficiency plots. As light falls on the cell, absorption restricts the QE response at wavelengths below 380 nm. This accounts for the losses encountered within this region as the minority carriers recombine before collection. The high external quantum efficiency (EQE) observed between 400 and 830 nm is due to increased photon absorption in the bulk absorber which allows for high current collection from the device. The QE curve within the center region appears relatively flat with small fluctuations due to glass and TCO reflections. At longer wavelengths, the gap between reflectance and QE curves indicates

additional photon losses due to deeper penetration into the absorber. Contributions from these losses are responsible for the modest drop in the EQE. More importantly, the QE starts dropping near 830 nm as one approaches the energy band gap (~1.4 eV) of the CST portion of the absorber above a wavelength of 830 nm. Beyond this wavelength, the absorption of photons by the absorber drops significantly at 900 nm as observed in Figure 3.11.

Under short circuit conditions, the quantum efficiency was integrated over the solar spectrum using Eq. 3.13 [29] to yield a short-circuit current density which should be very close to the measured J_{SC} values as outlined in Table 3.4 for comparison.

$$J_{SC} = q\int QE(\lambda)N_{ph}(\lambda)d\lambda \tag{3.13}$$

where q, λ, and N_{ph} represent the fundamental charge, wavelength, and the number of photons at given wavelengths within the spectrum of the sun. Slight variations in the measured and ideal J_{SC} values are associated with optical losses shown in the QE plot.

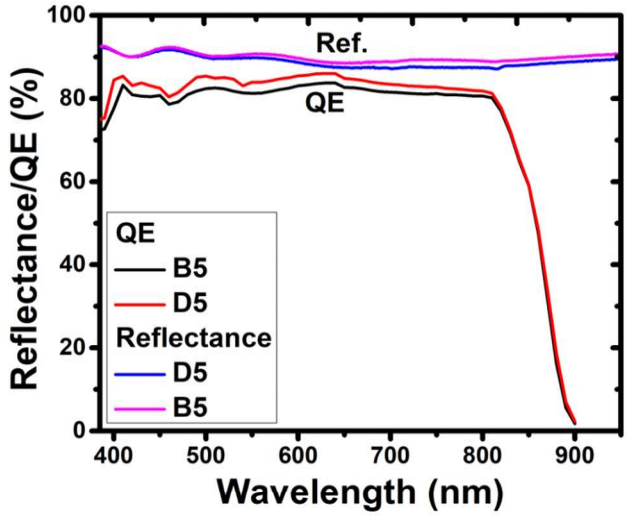

Figure 3.11: QE and reflectance plots of the measured CST/CdTe device. The reflectance is plotted downward from the top.

Table 3.4: Reflectance, QE and measured/integrated J_{SC} values of the cells.

Room temp. (293K)	D5	B5
Maximum QE (%)	85.4	83.2
Reflectance (%)	11.2	12.6
J_{sc} Measured	27.4	24.6
J_{sc} Integrated	27.9	25.2

3.3.9 Electroluminescence (EL) Imaging

Electroluminescence (EL) measurements were made to expose optical and electrical effects related to non-uniformity across the cells. EL measurements are the similar to dark J-V measurements but has the solar cell behaving as a light emitting diode as a forward current of about 12 mA is injected into the cell at different biases. The electrically-generated photons radiatively recombine with the carriers in the cell and lead to luminescence where the photons generated are emitted as light. The emitted photons are captured on a silicon charge-coupled-device (CCD) camera which produces a spatial image of the cell alongside a logarithmic scale showing color mapping from Image J software processing. The EL images with outlined dimension per cell in Figure 3.12 show two distinct EL intensities with more luminescence obtained from the rightmost part of the cells. The D5 cell reveals higher luminescence which is likely due to reduced surface recombination [34] and agrees with the higher V_{oc} value recorded from the J-V measurement as compared to the B5 cell. The intensity of the emitted light is linearly proportional to the amount of current injected. Non-uniformity during the EL emission

accounts for the non-homogeneities observed during the device fabrication [35]. The dark spots seen are also evidence of defects present in the device while the stretches seen are likely scratches on the glass surface. Regardless of the large variations in luminescence uniformity, the performances of these two-cells were relatively good, though they would benefit from greater uniformity.

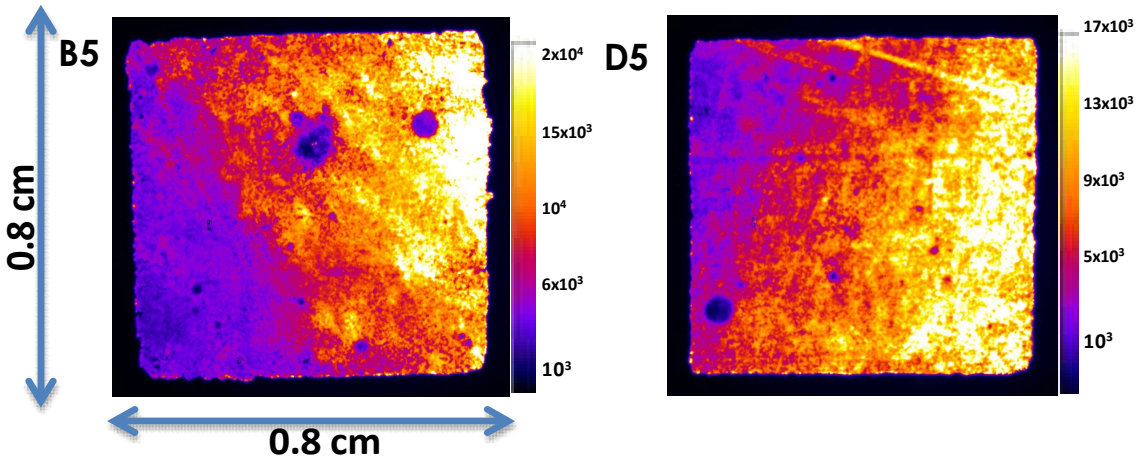

Figure 3.12: EL images of the measured CST/CdTe device.

3.3.10 Photoluminescence (PL) Measurement

Figure 3.13 gives a plot of the PL intensities as a function of wavelength. The D5 cells recorded very slightly higher PL counts than the B5 cell. The maximum PL peak was obtained at 875 nm wavelength which corresponds to a band gap energy of 1.41 eV. This band-gap value corresponds to the approximate band gap of the CST part of the absorber because the absorption depth of the 520 nm laser primarily excites the CST carriers. The PL counts for these cells are somewhat limited due to defects present in the solar cell devices and a weak radiative recombination signal which got picked up by the silicon detector during the measurement.

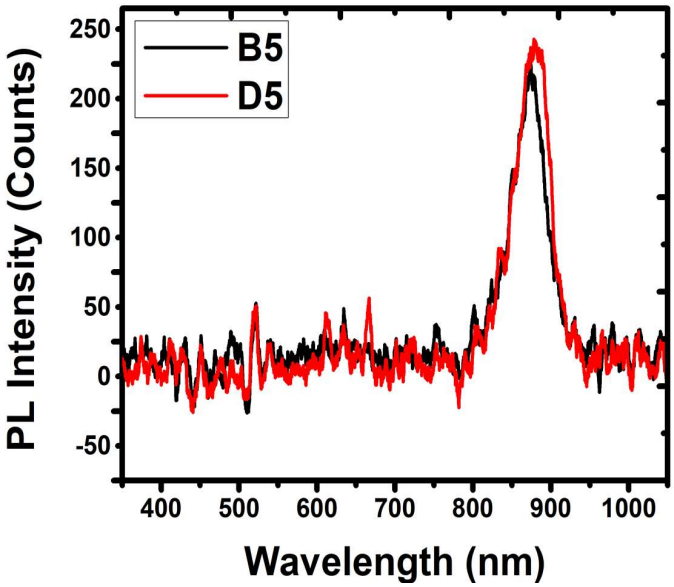

Figure 3.13: PL plots of the measured CST/CdTe device.

Chapter Four

Conclusions

This chapter summarizes this written work with more emphasis on the results obtained from the measured device. The beginning chapters gave an overview on green energy and PV technologies, semiconductor devices, solar cell parameters, and CdTe technology. Brief descriptions on the fabrication, structure, and measurements carried out on the CST/CdTe device were also discussed. The goal of this research was met through the successful measurement of the current density, capacitance, phase angle, quantum efficiency, reflectance, electroluminescent, and photo luminescent characteristics of the most efficient cells (D5 and B5) in the CSS-fabricated CST/CdTe device.

Room-temperature current density measurement was useful in extracting useful parameters such as the open-circuit voltage, fill factor, short-circuit current density, and efficiency of the device. The D5 cell recorded slightly better values as compared to the B5 cell with V_{oc} value of ~1 V with about 0.2 V offset. At low temperatures, a rollover effect due to an energy barrier at the back was observed in the J-V curves from 273 K. The rollover caused an increase in the V_{oc} but led to a reduction in the FF, J_{sc}, and efficiency at lower temperatures. The barrier heights calculated at 213 K and 233 K were about 0.4 eV with the B5 cell recording slightly higher values.

The capacitance measurement modeled the device as a parallel-plate capacitor with good stability gotten at 100 kHz. The cells exhibited similar trends from the C-V measurement which gave increasing capacitance values at forward bias and a built-in voltage near 0.9 V. The device gave a hole carrier density of $4x10^{14}$ cm^{-3} as a function of the distance from the junction. At low frequencies and different biases, high phase angle of 88 ^{o} was obtained. The phase angle dropped beyond 0.4 V as the turn-on of the diode current reduced the circuit resistance.

EL-imaging of the active cell areas revealed non-homogeneities and defects present in the device. Reflectance measurement gave reflectance percentages of 12.6 and 11.2 for the B5 and D5 cells respectively. High quantum efficiency of over 80% was observed and dropped off at a wavelength of about 830 nm. Photoluminescent measurement gave emission peaks at 875 nm which is approximately the band gap of the CST part of the absorber.

Overall, the D5 cell with a 15.2% efficiency exhibited better measurement characteristics than the B5 cell with 13.4% efficiency. These efficiencies are reasonable compared to the 20% and 23% devices made at CSU and First Solar companies respectively. Future prospects should aim at increasing the V_{oc} and efficiency of CST/CdTe devices for energy sustainability.

Project Collaborators

Chinecherem Chime measured the fabricated devices and drafted this Thesis.

James Sites is my research advisor who initiated this research project and proofread the Thesis.

Jennifer Drayton pioneered the device fabrication process.

Katherine Zaunbrecher and Camden Kasik were good guides for the measurement analysis.

Bibliography

[1] L. S. Alqarni, M. D. Alghamdi, A. A. Alshahrani, and A. M. Nassar, "Green Nanotechnology: Recent Research on Bioresource-Based Nanoparticle Synthesis and Applications," *Journal of Chemistry*, vol. 2022, p. e4030999, Aug. 2022, doi: 10.1155/2022/4030999.

[2] A. Sharif, S. Kocak, H. H. A. Khan, G. Uzuner, and S. Tiwari, "Demystifying the links between green technology innovation, economic growth, and environmental tax in ASEAN-6 countries: The dynamic role of green energy and green investment," *Gondwana Research*, vol. 115, pp. 98–106, 2023.

[3] A. N. Abdalla, W. Jing, M. S. Nazir, M. Jiang, and H. Tao, "Socio-economic impacts of solar energy technologies for sustainable green energy: A review," *Environment, Development and Sustainability*, vol. 25, no. 12, pp. 13695–13732, 2023.

[4] "How Much Power Does A Solar Panel Produce? (2024)," MarketWatch. Accessed: Jan. 30, 2024. [Online]. Available: https://www.marketwatch.com/guides/solar/power-solar-panels-produce/

[5] H. Zhang, Z. Yu, C. Zhu, R. Yang, B. Yan, and G. Jiang, "Green or not? Environmental challenges from photovoltaic technology," *Environmental Pollution*, p. 121066, 2023.

[6] Y. Li, X. Huang, H. K. Sheriff Jr, and S. R. Forrest, "Semitransparent organic photovoltaics for building-integrated photovoltaic applications," *Nature Reviews Materials*, vol. 8, no. 3, pp. 186–201, 2023.

[7] SunWindSolar, “Solar Radiation Spectrum • SunWind Solar,” SunWind Solar. Accessed: Feb. 08, 2024. [Online]. Available: https://sunwindsolar.com/blog/solar-radiation-spectrum/

[8] J. Wang, X. Zhang, X. Song, Y. Fan, Z. Zhang, and M. Zhao, “Insights into Photoinduced Carrier Dynamics and Overall Water Splitting of Z-Scheme van der Waals Heterostructures with Intrinsic Electric Polarization,” *The Journal of Physical Chemistry Letters*, vol. 14, no. 3, pp. 798–808, 2023.

[9] H. Xue *et al.*, “Recombination Rate Analysis of InGaN-Based Red-Emitting Light-Emitting Diodes,” *IEEE Journal of Quantum Electronics*, vol. 59, no. 2, pp. 1–9, 2023.

[10] “Series Resistance | PVEducation.” Accessed: Jan. 30, 2024. [Online]. Available: https://www.pveducation.org/pvcdrom/solar-cell-operation/series-resistance

[11] Y. Wang *et al.*, “Research progress in doped absorber layer of CdTe solar cells,” *Renewable and Sustainable Energy Reviews*, p. 113427, 2023.

[12] N. K. Jayswal, D. Adhikari, I. Subedi, A. Shan, and N. J. Podraza, “Role of CdTe Interface Structure on CdS/CdTe Photovoltaic Device Performance,” *Materials*, vol. 16, no. 20, p. 6812, 2023.

[13] P. Shah, A. K. Patel, R. Mishra, P. K. Rao, and O. Mishra, “Impact of electrical and optical parameters on performance of CdTe solar cell with a-Si as a hole transport layer,” *Journal of Optics*, pp. 1–10, 2023.

[14] W. Zheng, C. Shao, Q. Wang, G. Li, and H. Li, “Understanding and Engineering Interfacial Thermal Conductance of Two-Dimensional Materials,” *Surfaces and Interfaces*, p. 103538, 2023.

[15] D. E. Swanson *et al.*, "Single vacuum chamber with multiple close space sublimation sources to fabricate CdTe solar cells," *Journal of Vacuum Science & Technology A*, vol. 34, no. 2, 2016.

[16] "Department of Energy: 2014 Is the 'Year of Concentrating Solar Power.'" Accessed: May 24, 2023. [Online]. Available: https://www.triplepundit.com/story/2014/department-energy-2014-year-concentrating-solar-power/43631

[17] A. Romeo and E. Artegiani, "CdTe-Based Thin Film Solar Cells: Present Status and Future Developments," in *Recent Advances in Thin Film Photovoltaics*, U. P. Singh and N. B. Chaure, Eds., in Advances in Sustainability Science and Technology. , Singapore: Springer Nature, 2022, pp. 67–104. doi: 10.1007/978-981-19-3724-8_4.

[18] M. A. Scarpulla *et al.*, "CdTe-based thin film photovoltaics: Recent advances, current challenges and future prospects," *Solar Energy Materials and Solar Cells*, vol. 255, p. 112289, 2023.

[19] R. Pandey, T. Shimpi, A. Munshi, and J. R. Sites, "Impact of carrier concentration and carrier lifetime on MgZnO/CdSeTe/CdTe solar cells," *IEEE Journal of Photovoltaics*, vol. 10, no. 6, pp. 1918–1925, 2020.

[20] R. Pandey *et al.*, "CdTe-Based Solar Cells with Variations in Mg Concentration in the MgZnO Emitter," *Solar RRL*, vol. 5, no. 7, p. 2100126, 2021, doi: 10.1002/solr.202100126.

[21] W. Storr, "AC Capacitance and Capacitive Reactance in AC Circuit," Basic Electronics Tutorials. Accessed: Mar. 12, 2024. [Online]. Available: https://www.electronics-tutorials.ws/accircuits/ac-capacitance.html

[22] M. Zghaibeh *et al.*, "CdTe solar cells fabrication and examination techniques: a focused review," *International Journal of Green Energy*, vol. 20, no. 5, pp. 555–570, 2023.

[23] T. L. Chu and S. S. Chu, “Recent progress in thin-film cadmium telluride solar cells,” *Progress in Photovoltaics: Research and Applications*, vol. 1, no. 1, pp. 31–42, 1993.

[24] G. T. Koishiyev, J. R. Sites, S. S. Kulkarni, and N. G. Dhere, “Determination of back contact barrier height in Cu(In,Ga)(Se,S)2 and CdTe solar cells,” in *2008 33rd IEEE Photovoltaic Specialists Conference*, May 2008, pp. 1–3. doi: 10.1109/PVSC.2008.4922886.

[25] H. Li *et al.*, “Temperature-dependent Schottky barrier in high-performance organic solar cells,” *Sci Rep*, vol. 7, no. 1, p. 40134, Jan. 2017, doi: 10.1038/srep40134.

[26] B. L. Smith and E. H. Rhoderick, “Schottky barriers on *p*-type silicon,” *Solid-State Electronics*, vol. 14, no. 1, pp. 71–75, Jan. 1971, doi: 10.1016/0038-1101(71)90049-9.

[27] M. Soylu and F. Yakuphanoglu, “Barrier height enhancement and temperature dependence of the electrical characteristics of Al Schottky contacts on p-GaAs with organic Rhodamine B interfacial layer,” *Superlattices and Microstructures*, vol. 52, no. 3, pp. 470–483, Sep. 2012, doi: 10.1016/j.spmi.2012.05.022.

[28] A. A. Turturici, L. Abbene, G. Gerardi, and F. Principato, “Electrical characterization of CdTe pixel detectors with Al Schottky anode,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 763, pp. 476–482, Nov. 2014, doi: 10.1016/j.nima.2014.07.011.

[29] R. M. Geisthardt, “Device characterization of cadmium telluride photovoltaics,” Colorado State University, 2014.

[30] S. S. Hegedus and W. N. Shafarman, “Thin-film solar cells: device measurements and analysis,” *Progress in Photovoltaics: Research and Applications*, vol. 12, no. 2-3, pp. 155–176, 2004.

[31] N. O. Laschuk, E. Bradley Easton, and O. V. Zenkina, “Reducing the resistance for the use of electrochemical impedance spectroscopy analysis in materials chemistry,” *RSC Advances*, vol. 11, no. 45, pp. 27925–27936, 2021, doi: 10.1039/D1RA03785D.

[32] J. V. Li *et al.*, “Theoretical analysis of effects of deep level, back contact, and absorber thickness on capacitance–voltage profiling of CdTe thin-film solar cells,” *Solar Energy Materials and Solar Cells*, vol. 100, pp. 126–131, 2012.

[33] E. von Hauff, “Impedance Spectroscopy for Emerging Photovoltaics,” *J. Phys. Chem. C*, vol. 123, no. 18, pp. 11329–11346, May 2019, doi: 10.1021/acs.jpcc.9b00892.

[34] J. M. Raguse and J. R. Sites, “Correlation of Electroluminescence With Open-Circuit Voltage From Thin-Film CdTe Solar Cells,” *IEEE Journal of Photovoltaics*, vol. 5, no. 4, pp. 1175–1178, Jul. 2015, doi: 10.1109/JPHOTOV.2015.2417761.

[35] M. Bokalič, J. Raguse, J. R. Sites, and M. Topič, “Analysis of electroluminescence images in small-area circular CdTe solar cells,” *Journal of Applied Physics*, vol. 114, no. 12, p. 123102, Sep. 2013, doi: 10.1063/1.4820392.