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DISSERTATION

FABRICATION AND CHARACTERIZATION OF VCSEL BASED SMART PIXELS

Submitted by

Rui Pu

Electrical and Computer Engineering

In partial fulfillment of the requirements

For the Degree of Doctor of Philosophy

Colorado State University

Fort Collins, Colorado

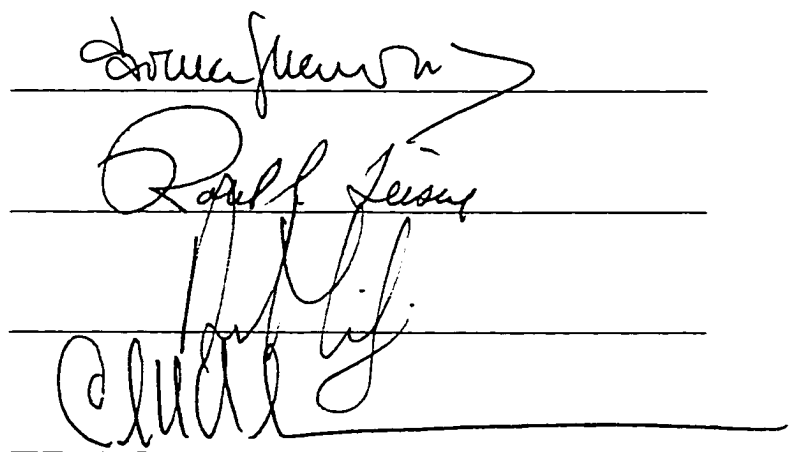
Summer, 1999

COLORADO STATE UNIVERSITY

Summer. 1999

WE HEREBY RECOMMEND THAT THE THESIS PREPAIRED UNDER OUR SUPERVISION BY RUI PU ENTITLED FABRICATION AND CHARACTERIZATION OF VCSEL BASED SMART PIXELS BE ACCEPTED AS FULFILLING IN PART REQUIREMENT FOR THE DEGREE OF DOCTOR OF PHILOSOPHY.

Committee on Graduate Work



Advisor

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ABSTRACT OF DISSERTATION

FABRICATION AND CHARACTERIZATION OF VCSEL BASED SMART PIXELS

Vertical-cavity surface-emitting laser (VCSEL)-based smart pixel arrays are very well suited for parallel optoelectronic processing and board-to-board interconnection. The integration of VCSELs with foundry fabricated integrated circuits is the key technology required to fabricate the smart pixels needed for these applications.

In the research of this dissertation, three hybrid integration techniques for bonding VCSELs to foundry fabricated microelectronic integrated circuit chips have been developed, characterized and compared. Each of the three bonding techniques used different ways of attaching the VCSEL to the integrated circuits and making electrical contacts. All three techniques remove the substrate from the VCSEL wafer leaving an array of individual VCSELs bonded to individual pixels.

This dissertation presents the successfully bonding of 8x8 and/or 4x4 VCSEL arrays to CMOS, MESFET and GaAs dummy chips using these three different bonding techniques. The electrical, optical and thermal characteristics of the bonded VCSEL arrays were measured in order to evaluate these bonding techniques. The functionality of the smart pixels with bonded VCSELs was also demonstrated.

The measured threshold voltage of the bonded VCSEL is as low as 1.5V and the series resistance is as low as 60Ω, indicating good electrical contacts. Optical power of 3mW for a VCSEL with a 14μm oxide-confined aperture was also observed indicating good thermal contact. The VCSELs were operated at 200Mb/s (our equipment limit) with the rise and fall times of the optical output being<1nS. The thermal resistance of the VCSELs bonded to a GaAs substrate was found to be as low as 1100K/W, indicating a high quality contact. Less than 100K/W thermal crosstalk was also observed in the VCSEL arrays with a 250μm pitch.

A two-dimensional thermal transfer model was constructed to analyze the heat transfer of the bonded VCSELs. The model predicted a rapid increase of thermal resistance when the size of the solder bonding pads is less than 10μm. The simulation also verified that the thermal resistance of the VCSEL bonded to a CMOS chip could be reduced by adding vias through the dielectric layers of the CMOS chip or increasing the thickness of the top gold traces.

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ACKNOWLEDGEMENTS

My special thanks go to Kent Choquette of Sandia National Laboratories for providing the VCSEL wafers. Kent Geib of Sandia and Arkadi Goulakov of Colorado State University for performing dry etching on some of the VCSEL arrays.

Also, I would like to thank the current and former members of the group for their supports. It was Rick Snyder and Randy Jurrat who taught me how to use cleanroom. Especially Randy Jurrat gave me a great help when I first came to a new country. With the help of Patrick Stanko and Daryl Pulver for maintaining the cleanroom, I could concentrate on my research. Should be mentioned together with them are Mari Ochiai and Dinesh Patel for helping set up the oxidation system and the spectrometer.

Certainly I am most indebted to Dr. Carl Wilmsen for his understanding and supports. His knowledge has always been a good resource for me when problems come up during my research. While gently nudging them when they get off track, he gives his students the freedom to tackle problems their own way.

Finally, I would like to thank my husband Chunjie Duan. Although we always argue who should do the housework, he is always willing to help me in the laboratory. His help of dealing with computers saved me a lot time.

The research was performed with funding from the National Science Foundation (Grant # 9408371) and Colorado State University through the Program of Research and Scholarly Excellence.

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CHAPTER 1

INTRODUCTION

1.1 Background

Photons are high frequency electromagnetic waves. It is well known that photons are less interacting than electrons and can propagate through waveguide, fiber or free space without appreciable attenuation or power dissipation. Therefore, utilizing photons rather than electrons as information carriers can be expected to achieve faster data rate, lower crosstalk and less dissipation of power. However, all optical devices, where photons control photons, are presently very difficult to realize, particularly in the case of small devices [1]. On the other hand, the performance of microelectronic integrated circuits has increased dramatically as the channel length has decreased. This situation provides a strong incentive to devise and study integrated circuits, which merge electronic and photonic operation. These integrated circuits are the so called "smart pixels" and combine electronic processing with optical interconnections.

The most successful demonstration of inserting optical components and interconnections into an electronic system is the use of fiber optics for long haul communication. However, the optoelectronic components and module assemblies have relatively high costs for small, localized systems because of the high cost of combining

the optical and electronic devices. For practical purposes, the cost/performance benefit justifies the use of optical technology only when the system clock frequency approaches 1GHz or when there are a large number of complex I/O interconnects [2]. Therefore, in order to justify replacing the electronic I/O pins with optical interconnections, a smart pixel array should be large and operate at high speed.

The key problem to fabricating smart pixels is integrating large arrays of photonic devices with electronic devices. This is not an easy task because of the material and structure incompatibility between photonic and electronic devices. Choosing the proper devices for integration is the other important issue. The next two sections compare monolithic with hybrid integration techniques, and vertical cavity surface emitting lasers (VCSEL) with modulator based smart pixels.

1.1.1 Monolithic versus hybrid integration

Smart pixels are composed of electronic integrated circuits, which perform electronic processing, and photonic devices for optical inputs and/or optical outputs. Si CMOS and GaAs metal-semiconductor field-effect transistor (MESFET) foundries can easily provide the electronic circuits, however, suitably mating these electronic technologies with optical transmitters and photodetectors has not been adequately developed, either by monolithic integration or by hybrid integration.

Monolithically integrated smart pixels are expected to be more reliable and faster than hybrid integrated pixels. However, there are material and structure incompatibilities between electronic devices and photonic devices. Also, the density of electronic components is severely limited. The most mature electronic integrated circuit technology is based on Si. Unfortunately, Si is an indirect bandgap material, which means that it can

not generate photons efficiently and can not efficiently absorb the photons near its bandgap wavelength. Thus, Si can not be used to fabricate a laser or efficient long wavelength (850nm) detectors. GaAs is an ideal material for both electronic and photonic devices, although it is more expensive than Si. However, GaAs integrated circuits are not as advanced as Si CMOS and have not been commonly used.

The structure incompatibility includes many factors. For example, a photonic component is normally fabricated on a doped substrate with metal contacts on both surfaces, while FETs are fabricated on a semi-insulating substrate with all contacts on the top. Furthermore, laser diodes or photodetectors (PD) are generally thicker and have more complicated structures than FETs. Thus, most photonic devices can not share the same layers with electronic components. The widely used solution [4][7][8] is to simply grow all the layers which are required for one device on a semi-insulating substrate, followed by the layers for the other devices. The lower device can be exposed by etching in selected areas, generally with the cooperation of an etch stop layer. This results in a nonplanar structure which limits the minimum feature size and component density as well as making the interconnect metalization difficult. The stacked device structure also leads to problems of electrical isolation between the devices. Isolation is sometimes accomplished by etching the layers into mesas which adds to the non-planarity of the chip [3].

Despite all the difficulties of monolithic integration of photonic devices and electronic devices, the great success of large scale electronic integrated circuits still encourages people to follow this example and monolithically integrate the input photodetectors, electronic processing, and the output VCSELs onto single chips.

Most of the monolithic integration has been done on GaAs substrates where all of these device layers are stacked on top of each other. Cheng's group at University of New Mexico fabricated binary switch arrays with heterojunction phototransistors (HPTs)[4] or photothyristors (PNPNs)[5] on top of the VCSEL structure, which can perform simple AND or OR logic functions. The threshold of the VCSELs is about 2.8mA. However, they are slow devices with a data rate of ~20Mb/s [4], due to their low gain and weak positive feedback. A higher data rate (~100Mb/s) was obtained with separate PIN/HBT inputs and VCSEL outputs [6].

Monolithic integration of a VCSEL with single MESFET has been accomplished by Yang et. al. in 1993 [7]. The device was grown on a n-doped GaAs substrate with the MESFET channel on the top of the undoped VCSEL top mirror. The VCSELs with a 10μm diameter active region exhibit an average threshold current of 6mA. The gate length of the MESFET is 3μm.

Matsuo and his co-workers with NTT Opto-electronics Laboratories monolithically integrated a MSM PD, three MESFETs, and a VCSEL on a single chip, which performs the OR function [8]. Different from Yang's work, the device was grown on a semi-insulating GaAs substrate with the VCSEL layers on top of the MESFET and MSM layers. 1μm MESFET gate length was obtained by non-contact photolithography. The threshold current of the VCSEL is 3.2mA with a 15μm mesa diameter. The smart pixel has a 220MHz 3-dB bandwidth with 300μW optical input.

Yue Liu and his coworkers at Honeywell also reported monolithically integrating VCSELs, MSM PDs, and GaAs MESFETs [9]. They grew the MESFET and MSM PD

layers on the top of the VCSEL layers. The typical threshold current of the VCSELs is 3.5-4mA for a 15μm diameter aperture.

Because the most mature electronic integrated circuit technology is based on Si, people are also working on growing III-V photonic devices on Si substrates, although the lattice mismatch is large. The development of new epitaxial growth technology has aided this research. Egawa et. al. used MOCVD to grow GaAs/AlGaAs n-mirror DBRs for a VCSEL on a Si substrate. Semi-transparent Au was used for the p-mirror [10]. The device lased under CW operation at 100K. Although it is an encouraging development, the threshold current is as high as 73mA and the external differential quantum efficiency is as low as 0.8% at 100K.

It is obvious that all these attempts, although promising, are still at their infancy and far from practical use. The functionality of the demonstrated smart pixels is simple, e.g. a basic Boolean function, and the speed is less than 200Mb/s which is not competitive with hybrid integration.

Hybrid integration, on the other hand, offers a more flexible choice of components and materials in which they are formed, since the photonic devices and electronic devices can be optimized and fabricated independently. Because of the huge market for electronic integrated circuits, the industry has invested billions of dollars in the development of the silicon integrated circuit. Therefore, it is wise for optoelectronics to develop a technology which is compatible with foundry fabricated Si or GaAs integrated circuits[11]. The task for hybrid integration is to make electrical connections between photonic devices and foundry fabricated electronic devices. This is the topic of this dissertation research.

The most straightforward hybrid integration method is wire bonding [12], however, it is not suitable for large scale integration since it requires large bonding pads and introduces a large capacitive/inductive load. We and others have suggested that the most space saving and the highest speed can be obtained by mounting individual VCSELs on the surface of the pixel [13] [14] [15]. This hybrid integration structure is similar to monolithic integration and is sometimes called hetero-integration. The circuit paths of this approach are shorter and the total area, which the smart pixel occupies, is also reduced due to the 3-D assembly. Thus, the performance characteristics should be similar to monolithic integration, e.g. better control of parasitics, better optical alignment and higher scalability can be obtained without the disadvantages of material and structural incompatibility.

1.1.2. VCSEL-based versus modulator-based smart pixel

Smart pixels can be broadly categorized as passive modulator based and active emitter-based. When the concept of a smart pixel was first introduced in the earlier 90's, it was directed more towards modulator-based devices, because surface-normal multiple-quantum well (MQW) modulators had been developed, and VCSELs had not. However, VCSELs are good optoelectronic component for smart pixels, since they emit a low divergent column of light normal to the wafer surface. Unlike an edge-emitting laser, a VCSEL does not require cleaved facets. Therefore, it offers the possibility of large 2-dimentsional arrays of coherent light source for 3-dimensional optical interconnections. In addition, the low divergent angle and the symmetry of the beam make it easier to couple the light into fibers or waveguides. Since the VCSEL has a very short cavity, it can operate with ultralow threshold current, high wall plug efficiency and single

longitudinal mode, which are all important characteristics for the integration of photonic and electronic devices. The threshold of a VCSEL can be as low as 9.0μA[16] and the wall plug efficiency can be as high as 50%[17], which enables low power consumption of the smart pixel. The VCSEL can also be easily modulated at a speed up to a few gigabits [18] [19] because of the single longitudinal characteristic.

Because of its earlier development, modulator-based smart pixels have been extensively investigated and utilized in prototype systems [20]. They also have the advantage of low on chip electric-power consumption because the MQW modulator is operated in reverse bias and thus requires very low current. But this advantage is offset when the total power consumption, including the bias-light source, is added. MQW modulators also have a thinner structure than VCSELs, which makes the hybrid integration easier. However, the easier fabrication of the pixel is offset by the need for complex optical assembly for its bias-light array and the wavelength requirements for the bias-light are very critical. The wavelengths of the bias-light must be well tuned to the MQW excitonic resonant peak with only 2-3 nm FWHM. Furthermore, the contrast ratio of surface-normal MQW normally is only 5dB [21]. In contrast, VCSEL-based smart pixel systems are easier to construct because the bias-light arrays are not necessary and, a large contrast ratio can be obtained by the active VCSEL device.

The dynamic response of VCSEL's are limited by the lasing delay time given by [21]:

$$\tau_{delay} = \tau_n \ln\left(\frac{\Delta I_{VCSEL}}{\Delta I_{VCSEL} + I_{bias} - I_{th}}\right) \qquad \left(I_{bias} < I_{th}\right) \tag{1.1}$$

Where τ_n is the carrier lifetime. Therefore, in VCSEL-based smart pixels, the switching time is limited by the characteristics of VCSELs such as external efficiency

and threshold current. On the other hand, the dynamic response of the modulator is capacitance-resistance limited [21]. The switch time of a modulator-based smart pixel, can be improved by increasing the input current of the MQW modulator in order to reach the required electric charge in a shorter time.

In summary, the MQW modulator is a simpler device than the VCSEL and it can also be used as a photodetector, but its narrow wavelength characteristics and bias-light requirement make it a much more difficult device to use in a practical system.

1.1.3 Review of hybrid integration of VCSELs and electronic circuits

Hybrid integration of components is a very broad field, which has been primarily used to attach electronic components to ceramic submounts. For most applications, this is a relatively simple process involving the soldering of previously fabricated (and often fully packaged) components to a small insulating substrate containing thin film electrical interconnects [11].

The hybrid integration of large arrays of VCSELs to integrated circuits is a much more challenging process since VCSELs are small, have a complex structure and must be integrated with a much greater density than the electronic components mounted on the ceramic substrates. The VCSELs require relatively small bonding pads which adds to the processing difficulties. Furthermore, the VCSELs are not completely fabricated before bonding and both they and the IC's require post fabrication processing.

A number of research laboratories have attempted to accomplish this task, and great progress has been made during the period of my Ph. D. research. However, due to the complexity of the problem, few have succeeded to integrate VCSEL arrays into foundry fabricated microelectronic integrated circuits. My own work was the first to bond an 8x8

VCSEL array to GaAs MESFET ICs[13]. After that, Krishnamoorthy and his coworker at Lucent Technology reported bonding a 2x10 array of 970nm VCSELs to a CMOS chip[23]. Despite several differences in details, both of these works are based on coplanar flip chip bonding technique, which had been used to make SEED arrays [24] [25].

Previously, Mathine et. al. [26] at Arizona State University developed the appliqué technique to transfer each individual VCSELs to its corresponding metal pad on the CMOS chip using a mechanical probe tip. The electrical contacts between the VCSEL and the CMOS chip were then formed. The applique technique is similar to that developed by Jokest and co-workers at Gal Tech for photodetectors [27]. Because each VCSEL is aligned separately, this process is not yet suitable for commercial or large array applications.

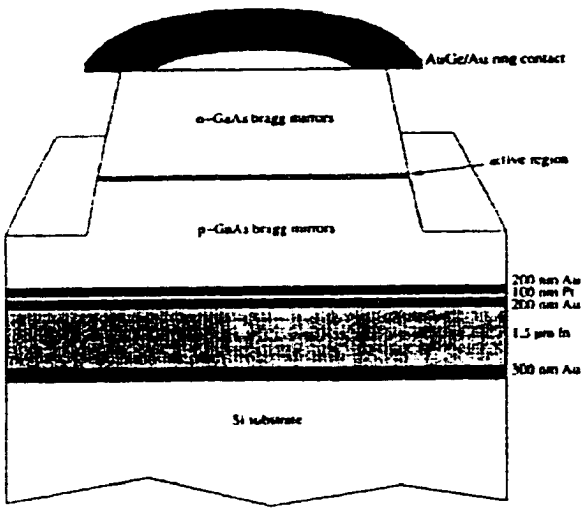


Figure 1.1 Wafer bonding with alloy [28]

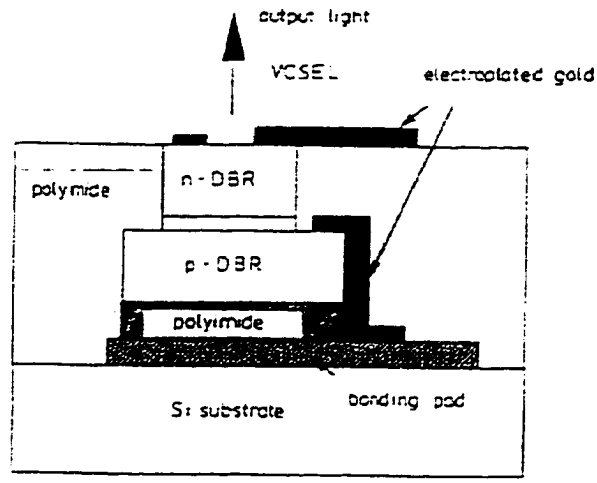


Figure 1.2 Wafer bonding with poly[29]

Yeh and Smith at UC Berkeley used an In/Au alloy to bond a VCSEL wafer and a Si substrate, as shown in Figure 1.1 [28]. After the substrate of the VCSEL wafer is removed, the VCSEL wafer is processed into individual devices. Although the conducive

wafer bonding material provides the VCSELs electrical contacts, the VCSELs are not individually addressable. Matsuo et. al. at NTT Optoelectronic Laboratories used polyimide to replace the In/Au, as shown in Figure 1.2 [29]. Polyimide is IR light transparent, therefore, one can view through the VCSEL layers and electronic circuits with an IR light source. Unfortunately, polyimide has low thermal conductivity which may effect the performance of VCSELs.

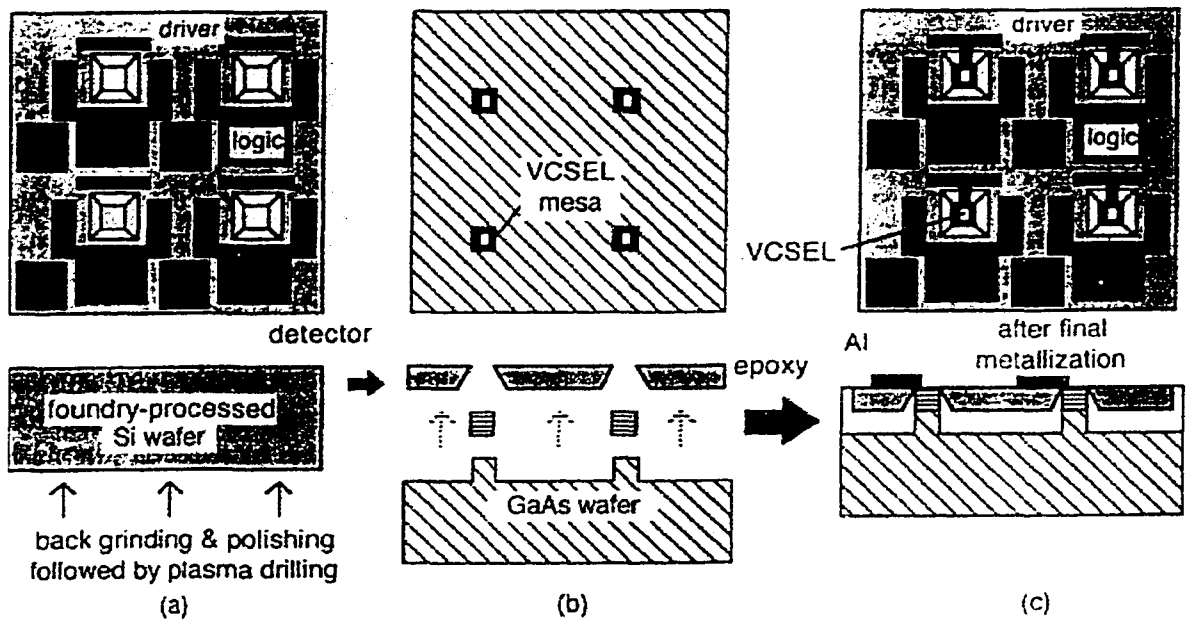


Figure 1.3 Etched hole technique developed by UCSD [30]

Lee et. al. at UC San Diego etched large holes in the CMOS chips and then placed the VCSEL array which is still attached to the substrate through the holes, as shown in Figure 1.3 [30]. They reasoned that the grafting of silicon device layer is less critical and easier than the grafting of GaAs devices. However, drilling holes on a CMOS chip occupies a large area of the electronic circuits and may affect the yield of the CMOS chip. The

etching of these large holes is not allowed in standard CMOS design, therefore, this technique is not compatible to CMOS foundry fabrication.

Although various hybrid integration techniques have been proposed, none of them can yet be considered as a mature technique. Table 1. compares all these techniques. We can see that the bonded wafer and flip chip bonding are among the most promising techniques. Due to the complex structure of VCSELs, the effects introduced by the integration need further investigation, in order to determine which are detrimental to VCSELs' performance.

Table 1 Summary of previous reported hybrid integration of VCSELs to ICs

Technique [reference]	Appliqué [26]	Bonded wafer		Thinned CMOS [30]	Flip chip bonding	
		alloy [28]	polyimide [29]		common ground [31]	coplanar [12]
VCSEL array size	individual			4x4	8x8	8x8
IC type	NMOS driver	Si substrate	Si substrate	Si CMOS	GaAlAs substrate	GaAs MESFET
Scalability	poor	excellent	excellent	fair	good	excellent
Compatibility	excellent	poor	good	poor	excellent	excellent
Simplicity	poor	good	good	good	excellent	good

1.2. Overview

The overall objective of the research presented in this dissertation is to investigate the hybrid technologies required to fabricate VCSEL-based smart pixels for application to chip to chip interconnects and the development of free space optoelectronic processing systems. A smart pixel combines an optical output device (such as a VCSEL or modulator) with an electronic processing circuit. Often the smart pixel also contains a photodetector (PD) for optical input. Since the hybrid integration of PDs is similar, but easier than VCSELs, the present research concentrates on the hybrid integration of

VCSELs to foundry fabricated electronic chips, either GaAs MESFETs or Si CMOS. The goal is to establish the bases for obtaining integration density >1000 VCSELs/cm^2 in order to meet the requirements of practical applications.

Chapter 2 details the three hybrid integration techniques developed by this research. Each of the three bonding techniques used different ways of attaching the VCSEL to the micro-electronic integrated circuits and making electrical contacts to the n- and p-mirrors. All of these techniques remove the substrate from the VCSEL wafer leaving an array of individual VCSELs bonded to individual pixels. The three technologies are 1) coplanar flip chip, 2) conductive attachment top-bottom contacts, and 3) non-conductive attachment top contact bonding.

Aiming at hybrid integration of foundry fabricated electronic chips, we first used GaAs substrates with thin film traces as test structures. Then VCSEL arrays were bonded to MESFET and CMOS chips. The VCSEL pitch is 250μm, equal to a VCSEL density of 1600/cm^2. 4x4 and 8x8 arrays were fabricated.

Chapter 3 describes the measurements of the electrical, optical and thermal characteristics of the VCSELs bonded by these three techniques. The threshold of the bonded VCSELs is about 3mA when the aperture size is about 15μm. The static series resistance is about 100Ω. Thermal effects are known to limit the VCSEL output optical power and efficiency and thus, the scalability of integrated arrays. Thermal resistant and thermal cross talk were defined [32] and measured [33] to give such information.

In chapter 4, a two-dimensional thermal transfer model was constructed to analyze the structure of the three bonding techniques and show the thermal limits of the integration scalability and density.

Chapter 5 compared the processing, mechanical, electronic, optical, and thermal characteristics of these three different bonding techniques, in order to determine the optimum method of fabricating VCSEL based smart pixel. To evaluate the bonding techniques, the bonded VCSELs are also compared with typical unbonded VCSELs.

Conclusions and suggestions for future work are given in Chapter 6. The details of the fabrication process and the thermal transfer model are described in Appendix A and B respectively.

CHAPTER 2

FABRICATION OF VCSEL BASED SMART PIXELS

There are two general application types for VCSEL based smart pixels; 1) guided wave applications which require only a few VCSELs, e.g., data links which require 10 to 16 VCSELs and 2) free space optical processing and interconnection applications which require >1000 VCSELs. Since the research of this dissertation is primarily concerned with the later, emphasis of the research has been placed on developing and evaluating techniques of bonding large arrays of VCSELs to standard foundry fabricated CMOS and/or MESFET ICs.

2.1. General considerations

The fabrication of VCSEL based mart pixels requires the resolution to three main questions:

a. How to fabricate the VCSELs.

b. How to integrate (attach) the VCSELs to the ICs, and

c. Should the VCSEL substrate be removed.

This section discusses each of these questions.

2.1.1. Method of integration

The required hybrid integration technology includes attaching the VCSEL to the electronic chip array and making the electrical connection between the VCSELs and the electronic circuits. The best method for attachment and electrical connection is not obvious and thus, several techniques must be investigated. The attachment can be conductive, using solder or solder paste [12] or nonconductive using polyimide or epoxy. The conductive attachment also provides electrical connection. Depositing thin film traces is another way of obtaining the electrical connection. This dissertation research investigated three combinations of these approaches.

It seems that the conductive attachment is the simplest way to accomplish the hybrid integration because it provides both attachment and electrical connection. However, it is hard to stencil a fine pattern ($<60^2$ μm^2) with solder paste because very high paste viscosity is required in order to prevent the paste from flowing off the small pads ($\leq$ 30μm x 30μm)[34]. In addition solder bonding is also not a mature technique for the small bonding pads required for high density arrays. On the other hand, solder bonding normally requires reflow which may reduces the bonding yield since an intermetallic reaction may occur between the solder and the metal pad during reflow [25]. Therefore, a solder bonding technique, which uses thermal compression without reflow, has been developed and used in this research.

Although the nonconductive attachment requires more processing steps, the process is easy to accomplish. It is hard to determine a priori whether the conductive or the nonconductive attachment would have a higher yield and lower cost. The disadvantage of

nonconductive attachment is the increased thermal resistance because the VCSEL is placed on a high thermal resistant material.

2.1.2 Substrate removal

The bonding of large arrays of VCSELs to electronic chips is best accomplished with the VCSELs still attached to its substrate. With the substrate attached, the structure is robust and the substrate can serve as a common electrode. Thus, only one electrode per VCSEL needs to be flip-chip-bonded to a metal pad on the electronic chip. However, this technique requires VCSELs operating at a wavelength transparent to the substrate since the flip chip bonded VCSELs must be back emitting. There are two ways to achieve this goal;

1) Changing the VCSEL lasing wavelength from 850nm to ≥980nm since the GaAs substrate is mot transparent to the shorter wavelength. Also using a 980nm wavelength VCSEL requires long wavelength photodetectors, which limits the PD materials, e.g. Si is a poor detector for long wavelengths. The question arises as to whether the substrate should be removed. [23]
2) Using an AlGaAs substrate instead of GaAs which allows the VCSELs to still emit at 850nm [31]. However, AlGaAs substrates are much more expensive than GaAs. The most critical issue related to substrate removal is, the thermal expansion mismatch between the VCSEL array and the CMOS circuitry. The mismatch may break the solder attaching the VCSELs to the CMOS chip or reduce the lifetime of solder bonds. Removing the substrate of the integrated VCSELs can solve these problems and is used in the present research.

2.1.3 VCSEL fabrication

The VCSELs used in the hybrid integration bonding process can be of a standard oxide, proton implantation-defined design, or have an air post structure. We have chosen to use oxide confinement since it appears to be best suited for the present integrated bonding techniques and generally results in a lower threshold current.

An ideal VCSEL wafer design for this research should be similar to that of a standard 850nm oxide confined VCSEL wafer, except the n-mirror has fewer layers than the p-mirror. This allows emission from the bottom side of the VCSEL stack after substrate removal. In order to fabricate substrate removal, the VCSEL wafer also should have an AlAs stop-etch layer between the VCSEL stack and the substrate. In addition, the VCSEL wafer should have intra-cavity contact layers for both p- and n-contacts.

Although, limited by the VCSEL wafer source, the VCSEL wafers used in this research are not perfect for bonding. Fortunately, the bonded VCSELs fabricated from these VCSEL wafers still lased and have reasonable characteristics, such as low threshold current. However, the series resistance varied and the output optical power was sometimes low. We believe that investigating their characteristics is still very helpful to understand the integration techniques.

A 250μm pitch was used for all of the VCSEL arrays, this equals to the density of 1600VCSEL/cm^2. The bonding pads can be made as small as 10x10μm^2 [31]. However, considering that a reasonable mesa size for oxide confined VCSELs is 40x40 μm^2 and small bonding pad size increases the difficulty of heat dissipation, the bonding pads we designed are 30x30 μm^2. Arrays of either 4x4 or 8x8 were used in this research.

Aiming at hybrid integration of foundry fabricated electronic chips, we first used GaAs substrates with thin film traces as the test structure in order to develop the bonding techniques, after which VCSEL arrays were bonded to MESFETs and CMOS chips. There appears to be no significant difference between bonding VCSELs to a GaAs dummy chip or a foundry fabricated micro-electronic chip. Furthermore, it is unlikely that the integration process will effect the foundry fabricated chip as long as high temperature (>500°C) or a large force are not applied to the chip.

Three types of hybrid integration techniques with both conductive and nonconductive attachment were investigated in this research. All of these technologies require substrate removal. The three technologies are 1) coplanar flip chip, 2) conductive attachment top-bottom contacts, and 3) non-conductive attachment top contacts. In this chapter, these three fabrication techniques are described in details.

2.2. Coplanar flip chip bonding

The coplanar bonding process is illustrated in figure 2.1.

The oxide-confined VCSELs were fabricated by dry-etching the device mesa down to the n-mirror and wet oxidizing the confinement layers (figure 2.1 (a)). The mesas were oxidized at 430°C for 25 minutes in water vapor resulting from N_2 bubbled through 75°C water. The oxidation resulted in approximately $15x15\mu m^2$ apertures when the mesa was $40x40\mu m^2$. All of the aperture sizes were not exactly the same, probably because of the non-uniform composition of the oxidation confinement layer. After etching, the wafer surface has 4-5μm steps. While this decreases the resolution of subsequent photolithography, VCSEL processing only requires a few micrometer resolution which is readily obtainable. Furthermore, the coplanar flip chip structure does not require a metal

aperture (this is the smallest feature of the VCSEL). Thus the resolution requirement is even less critical.

The p- and n-contacts were then deposited and annealed (figure 2.1 (b)). 500Å Ti/1500Å Au layers were deposited for the p-contacts, while the n-contacts are composed of 250Å Ge/520Å Au/150Å Ni/1000Å Au. These contacts were annealed at 375°C for 40 seconds. The metal contacts were deposited after oxidation to avoid the corrosive atmosphere and high temperature, both of which could degrade the contact resistance. When better alignment and fine structure are required, the metal contacts need to be deposited before the mesa etch, therefore before the oxidation. Then special design of the metal contacts is necessary in order to protect the metal from the corrosive atmosphere and prevent the Au diffuse into the VCSEL deeply during high temperature.

After contact annealing, a Au post was electroplated on the n-contact to a height approximately level with the p-contact and then additional Au posts were electroplated on both p- and n-contacts in order to enhance the bonding (figure 2.1 (c)). The accuracy of the electroplated coplanar Au posts must be controlled within 0.5μm, otherwise the bonding process has a low yield or the bonded VCSEL has non-uniform characteristics. Even if electrical contact is achieved, a barely touching contact would result in high thermal resistance and low mechanical strength. Therefore, the quantum efficiency and the maximum optical output power and other characteristic of the VCSELs could vary over a large range. In addition, the electroplating rate also depends on the size of the sample, the pattern on the sample, electroplating current, and temperature. While the latter two are easy to control, the other two cause the electroplating rate to vary and

repeatability is difficult. With similar samples, the rate can be estimated, however, it's seldom exactly the same.

Another mesa surrounding this structure was then formed by wet-etching down to the substrate (figure 2.1 (d)). Although wet-etch results in an under cut, a smooth surface can be obtained. The smooth surface is very helpful for viewing through the VCSELs for the alignment of the subsequence bonding process.

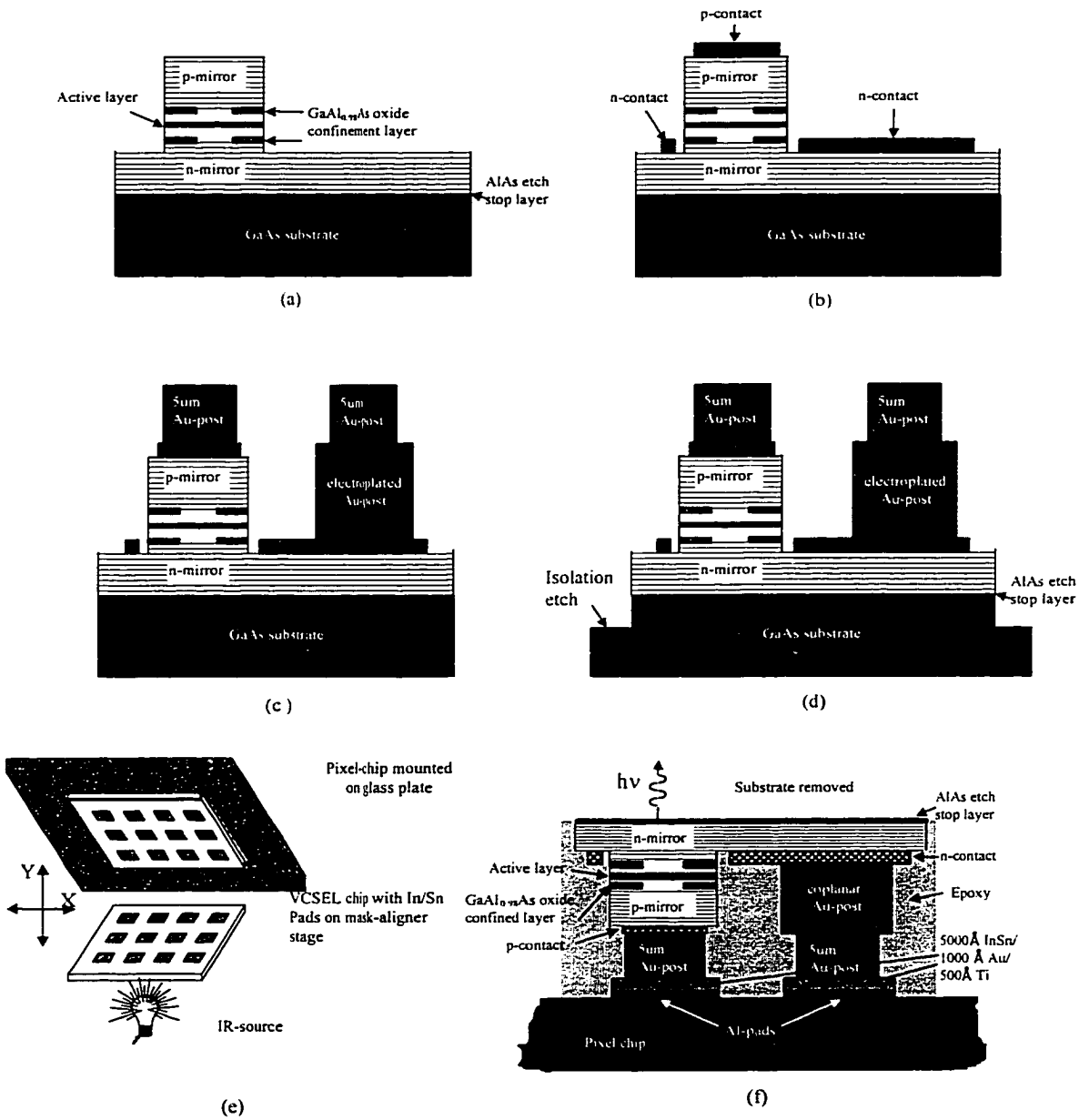


Figure 2.1. Process of coplanar flip chip bonding

The fabricated VCSEL before flip chip bonding is shown in figure 2.2.

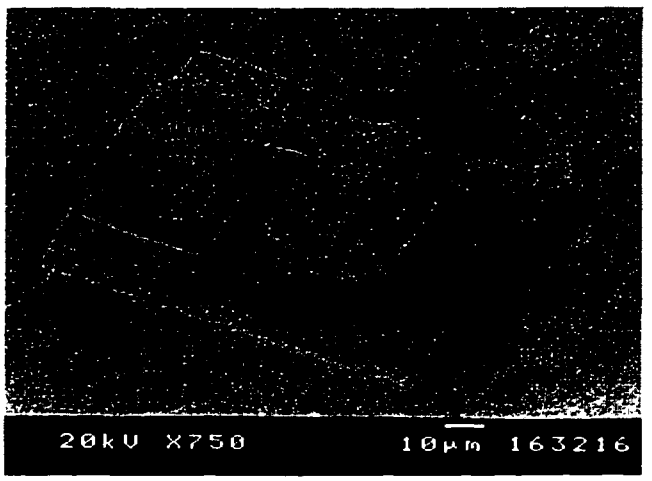


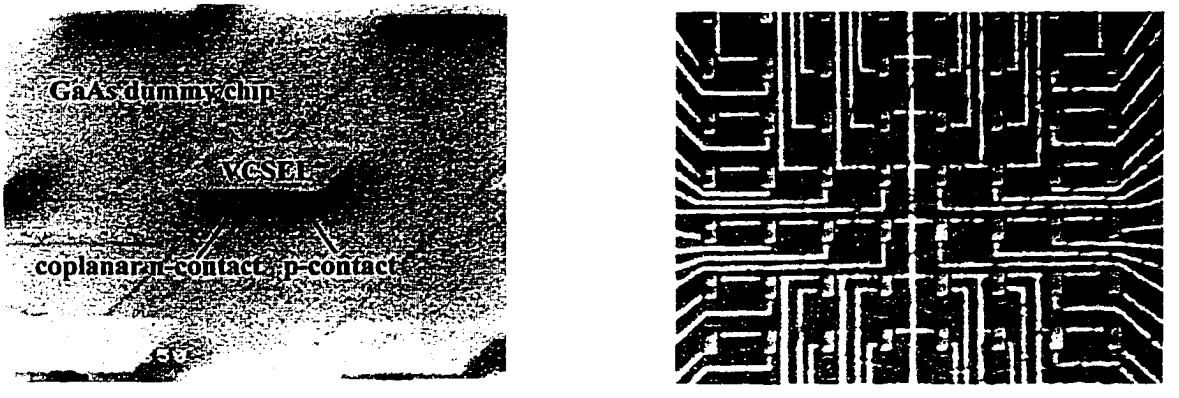
Figure 2.2 SEM photomicrograph of a coplanar VCSEL

Since the bonding pads of foundry-fabricated ICs are Aluminum, 500Å Ti/1500Å Au/6000Å InSn was deposited onto these pads. Ti is the adhesive layer and the Au serves as a solder-wettable layer for the InSn solder. The flip chip bonding of the VCSELs to the IC chip was accomplished by mounting the VCSEL chip onto a glass plate with crystal bond, aligning it with the pixel chip in a mask aligner using IR to view the two structures and then bonding the two chips together by applying pressure (figure 2.1 (e)). If this part of the process is done properly, then the unit can be easily transferred to a hotplate and heated to 180°C for 12 minutes, which melts the InSn and forms an eutectic with the Au pads. Since the present volume of the InSn is small we believe that alloying of the InSn with Au occurs, and not reflow. The yield of the bonding is limited by the tilt between the VCSEL arrays and the pixel chip. To improve the yield, the mask aligner can be well calibrated so that the two glass plates are parallel. However, the crystal bond can also introduce a tilt. In order to reduce this problem, a very thin crystal bonding layer can be

used by melting it at a slightly higher temperature, such as 200°C. According to our experience, the tilt is mainly from the polishing of the VCSEL substrate. VCSELs are normally grown on an unpolished wafer, however, in order to view through the chips, we polished the VCSEL wafer. The quality of polishing was limited by the available lapping facility.

After the bonding, epoxy is wicked in between the chips to enhance the robustness of the structure and protect the pixel chip from attack by the subsequent polish and the selective etch used to remove the GaAs substrate (figure 2.1 (f)). To remove the substrate, it is first polished to ~100μm thick, then selectively etched away. This process leaves free-standing VCSEL mesas bonded to the electronic chip. We have found that a PA solution (H_2O_2:NH_4OH=250ml:8ml) spray etch provides extremely good selectivity at the AlAs etch-stop layer and consequently a very smooth top-emitting surface. The epoxy can be removed by plasma etch if necessary.

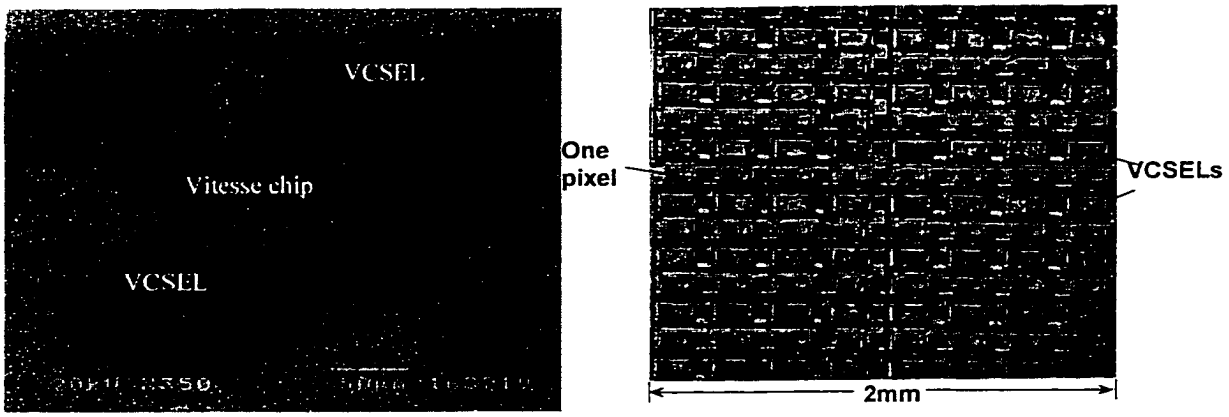
We developed the coplanar flip chip technique by bonding the 8x8 VCSEL array onto a GaAs dummy chip, as shown in figure 2.3. The yield was about 50%.



(a) SEM photomicrophy (b) Optical photomicrograph

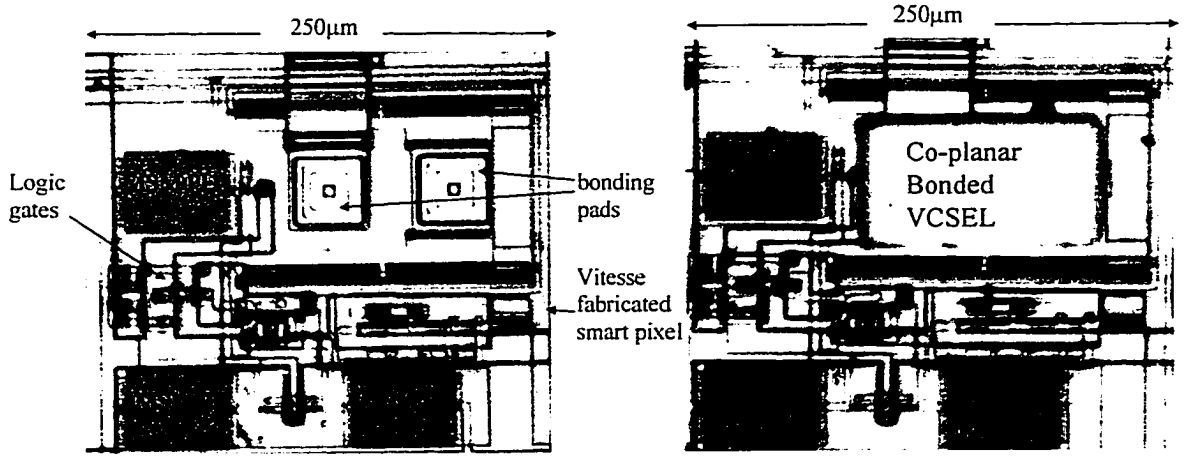
Figure 2.3. 8x8 VCSEL array coplanar flip chip bonded to a GaAs dummy chip

Then we used this technique to bond an 8x8 VCSEL array onto a MESFET chip as illustrated in figure 2.4. The MESFET chip was designed with the Vitesse Semiconductor 1.0-μm E/D MESFET process and fabricated by Vitesse through the MOSIS Foundry Service. The smart pixel circuit contained 32 MESFETs and 3 MSM photodetectors, which perform the selection function of a data filter [11] [12] and also provides the current drive for the VCSEL. Figure 2.5 shows a fabricated pixel with and without a co-planar bonded VCSEL.



(a) SEM photomicrograph (b) Optical photomicrograph

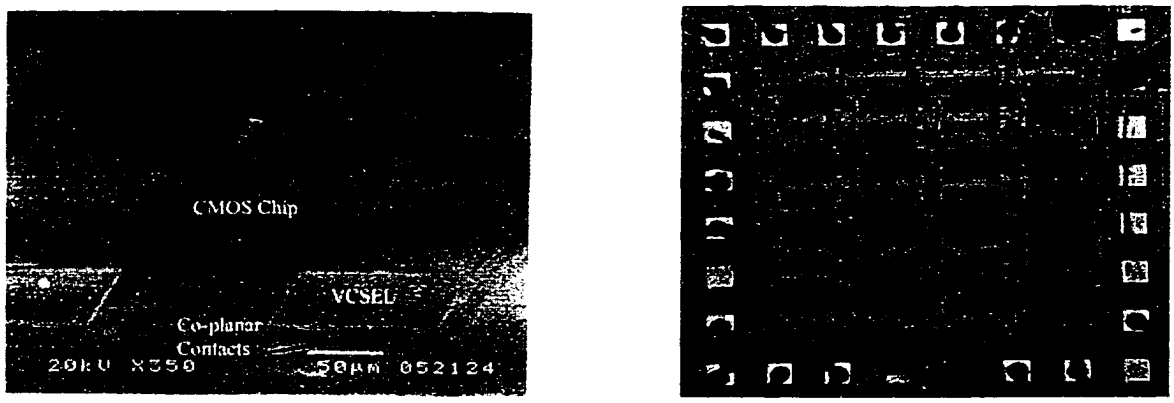
Figure 2.4. 8x8 VCSEL array coplanar flip chip bonded to a MESFET chip



(a) Without a coplanar bonded VCSEL (b) With a coplanar bonded VCSEL

Figure 2.5. Optical photograph of a Vitesse fabricated smart pixel

A 4x4 VCSEL array was also bonded to a CMOS chip, as shown in figure 2.6. The CMOS chips were designed with 0.5μm design rules and fabricated by Hewlett Packard through the MOSIS Foundry Service. Each pixel contained a four-stage CMOS amplifier and an NMOS single-stage current driver with a parallel pre-biasing transistor.



(a) SEM photomicrograph (b) Optical photomicrograph

Figure 2.6. 4x4 VCSEL array coplanar flip chip bonded to a CMOS chip

2.3. Top-bottom contact bonding

The top-bottom contact bonding process is illustrated in figure 2.7.

Depositing the p-contacts is the first step in the process, followed by electroplating Au posts (figure 2.7.(a)). The VCSEL's mesas were then isolated by dry etching into the substrate and the confinement layers oxidized by heating in steam at 430°C (figure 2.7.(b)). The Au posts served as the etch mask. The mesas have the same size as those of co-planar flip chip bonding discussed previously and were oxidized under the same condition. The metallizations were carried out before the etching, therefore before the oxidation, because these VCSEL mesas are about 9μm high which reduces the resolution of the photolithography. Furthermore, using the Au posts as the mask for mesa etching can also save one photolithography step. 400Å Ti/200Å Pt/1500Å Au metallization was

used for the p-contact instead of Ti/Au. The Pt serves as a diffusion barrier to prevent Au diffusing deeply into the device during the 430°C oxidation. The electroplated Au post also protects the ohmic contact from the corrosive environment.

Ti/Au/InSn was deposited onto the Al p-contact pads of the pixel chip. An additional Au post was electroplated to the approximate height of the VCSEL's on the n-contact Al pad of the pixel chip in order to form the top contact (figure 2.7.(c)). The height tolerance of this post is greater than that with the coplanar technique, because this post does not contribute to solder bonding.

The bonding (figure 2.7.(d))and substrate removal process (figure 2.7.(e)) is similar to that used in the coplanar flip chip, except the bonding alignment is not as critical, because there is only one solder bonding pad for each VCSEL. Furthermore, there is no coplanar height accuracy problem. Therefore, higher bonding yield can be expected compared with co-planar flip chip bonding.

If the Au posts on the pixel chip were lower than the VCSEL mesas then epoxy will cover the top of the Au posts on the pixel chip. This can be removed with an oxygen plasma etch (figure 2.7.(f)). Then, the n-contacts of the VCSELs were deposited and the contact traces between the VCSEL n-contacts and the Au posts of the pixel chip were electroplated in order improve the step coverage and make the electrical connection more reliable. The final step was annealing.

The aperture on the n-contact is the smallest pattern within this technique. Therefore, it is the most critical photolithography step. Since this photolithography step was performed on the back of the bonded VCSEL, a non-planar surface is unavoidable. According to our experience, the radii of the patterned apertures are normally 2μm

smaller than the mask. Thus, designing a bigger aperture size mask can solve this problem. Step coverage with this process is not a serious problem since the epoxy provides a bridge between the VCSEL. In addition, increasing the thickness of the metal trace by electroplating also helps the step coverage problem.

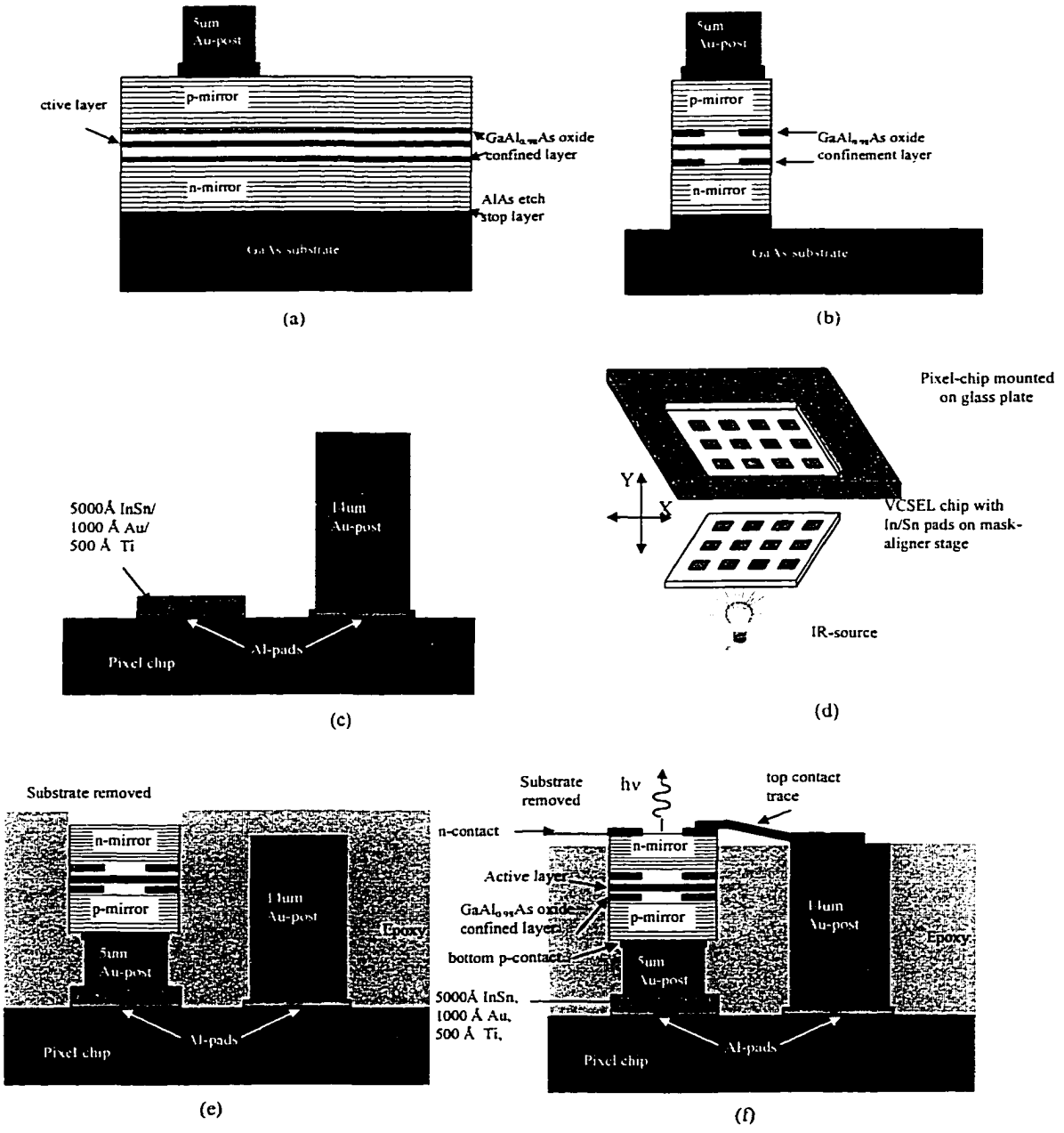
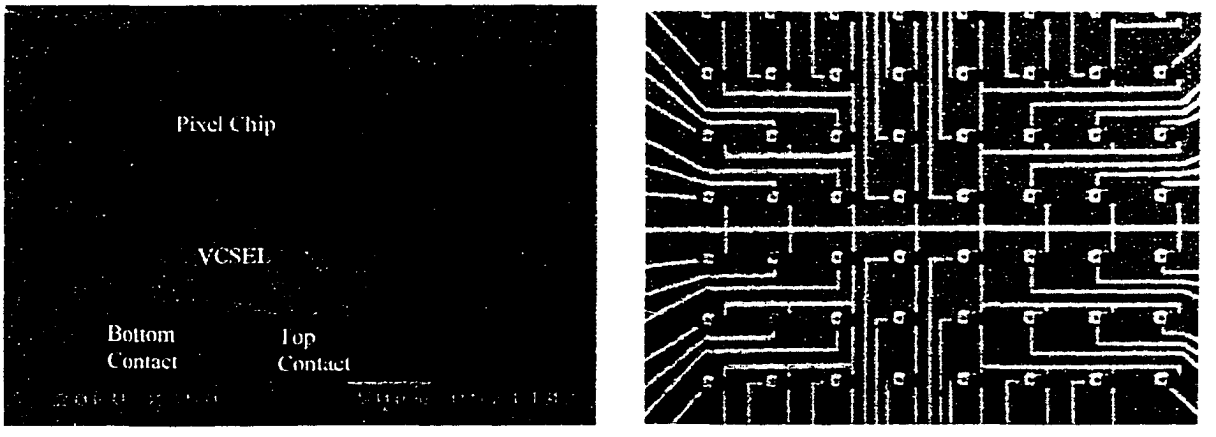


Figure 2.7. Process of top-bottom contact bonding

The SEM photomicrograph of figure 2.8 (a) illustrates part of an 8x8 array of VCSELs bonded by this technique to a GaAs dummy chip. Figure 2.8 (b) is an optical photomicrograph of this 8x8 bonded array.



(a) SEM photomicrograph (b)Optical photomicrograph

Figure 2.8. 8x8 VCSEL array top-bottom bonded to a GaAs dummy chip

2.4. Top-contact bonding

Another approach to attaching individual VCSELs to an electronic chip is to "glue" the entire VCSEL to the electronic chip, removing the VCSEL substrate and processing the remaining layers into individual VCSELs. Figure 2.9 illustrates the process of top-contact bonding with this kind of attachment.

The VCSEL wafer was first glued face down onto the electronic wafer, using a non-conducting material such as epoxy or polyimide [15] as shown in figure 2.9 (a). The non-conductive material should have low shrinkage after curing, otherwise the very thin epitaxial layers will be distorted by the bonding material. Also nonconductive materials normally are not good thermal conductors, a thin layer is preferred in order to reduce the thermal resistance. In order to obtain a thin uniform layer of bonding material low

viscosity is required. Epoxy was chosen as the bonding material for this research since it has low viscosity. Our experiments also verified that better bonding is easier to be accomplished with epoxy than with polyimide. Even though epoxy data sheets do not recommend heating above 150°C, the VCSELs were firmly attached after the 430°C oxidation.

After the substrate was removed, the processing steps for this technique are similar to the first two techniques as outlined below. First, n-contacts were deposited on the exposed n-mirror and the device mesas were dry-etched down to the p-mirror as shown in figure 2.8 (b). Since the metal aperture is the smallest pattern in this technique, the required photolithography for this step was performed first.

The p-contacts were then deposited and isolation mesas were wet etched with the epoxy serving as the wet-etch stop layer (figure 2.9 (c)). The oxidation was carried out after these etching steps which left individual VCSEL mesas on the surface of the pixel chip. Oxidation before the isolation etch could cause the layers to break due to the difference in thermal expansion.

The very thin layer of epoxy or polyimide used in this bonding (<1μm) can not protect the Al bonding pads on the pixel chip from the corrosive environment during the oxidation. Therefore, the Al bonding pads need to be protected before oxidation by other methods, such as depositing Au on it, or be treated after oxidation.

After the VCSEL apertures were formed by wet oxidization, and the epoxy not under the VCSEL mesas was removed with an oxygen plasma etch (figure 2.9 (c)).

Polyimide was spun to cover the VCSEL mesas and then patterned (figure 2.8 (d)) to provide an insulating layer. In addition, the polyimide better holds the VCSEL mesas in

place. Au traces were then electroplated to connect the p- and n- contacts to their corresponding bonding pads on the pixel chip. The Au trace step coverage is reliable, since the polyimide planarizes the surface and the side walls of the contact holes in the polyimide are 45°.

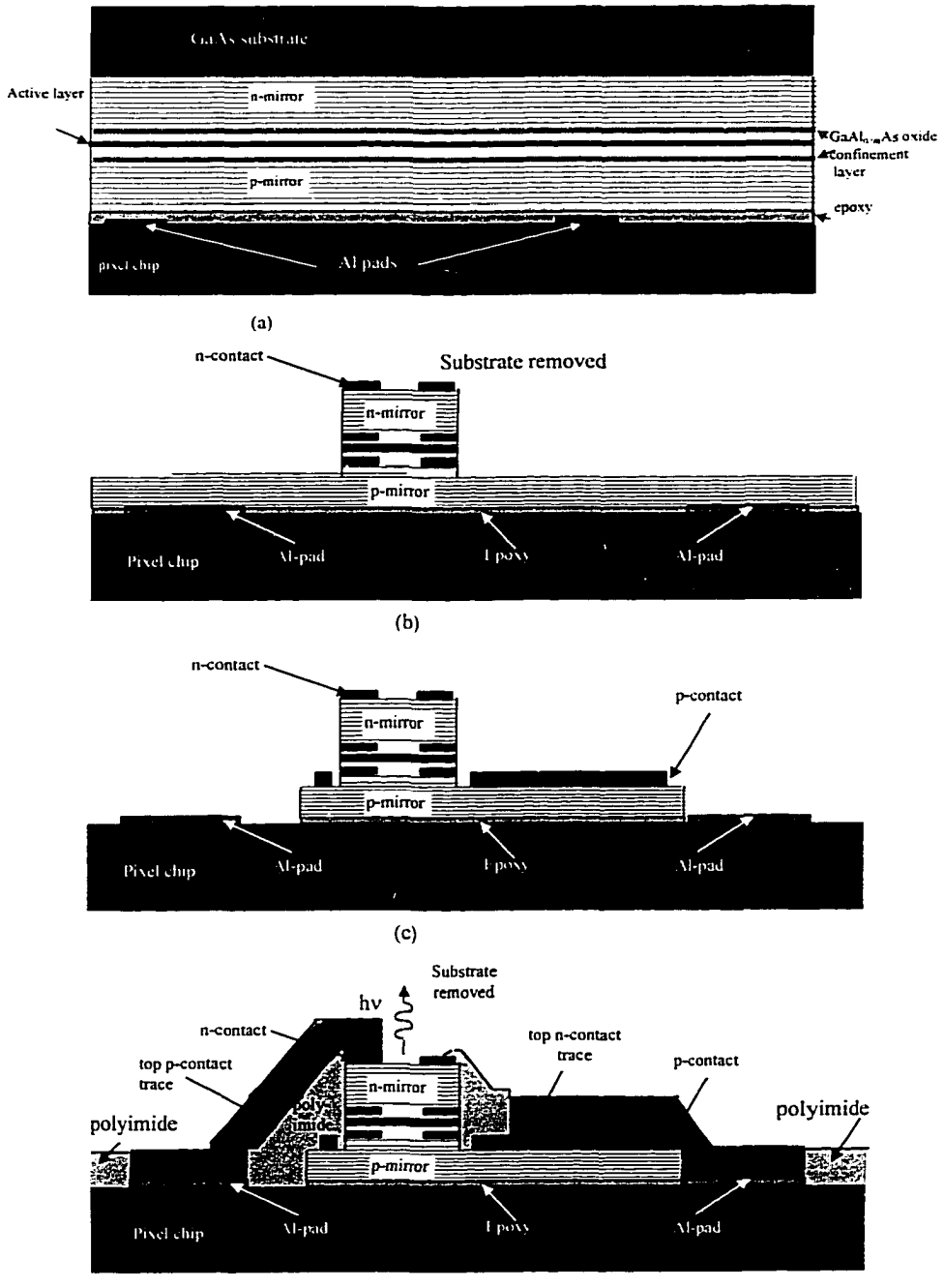
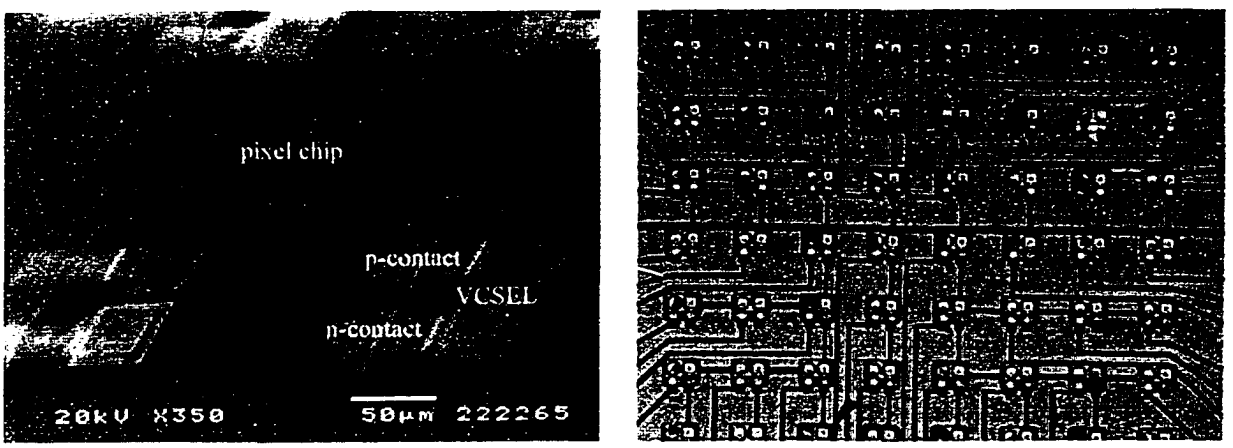


Figure 2.9 Process of top-contact bonding

The SEM photomicrograph of figure 2.10 shows individual VCSEL's of an 8x8 array bonded to a specially prepared GaAs dummy substrate using the top-contact technique. The optical photomicrograph illustrates this 8x8 array.



(a) SEM photomicrograph (b) Optical photomicrograph

Figure 2.10. 8x8 VCSEL array top-contact bonded to a GaAs dummy substrate

CHAPTER 3

ELECTRICAL AND OPTICAL CHARACTERISTICS OF VCSEL BASED SMART PIXELS

Since the goal of this dissertation research is to develop a new hybrid integration technique, the measurements focused on the evaluation of the bonding technique. An ideal bonding technique should not affect the performance of the VCSELs. Therefore, the basic electrical and optical characteristics of the bonded VCSELs were measured first.

After realizing that the VCSELs bonded by all these three techniques can lase, in order to make a better comparison of these three techniques, we measured bonded VCSEL arrays fabricated from the same VCSEL wafer and with the same aperture size. The functionality of the smart pixel was then demonstrated.

The bonding pads for the integration not only provide the electrical connection between the electronic chip and the VCSELs, but also provide the heat path for the VCSELs, which might be the most power consuming devices in the circuits. Thus, the quality of the bonding also effects the maximum output optical power of the bonded VCSELs.

3.1. Basic electrical and optical characteristics of the bonded VCSEL

The characteristics of the bonded VCSELs depend on the initial quality of the VCSEL wafer, the VCSEL processing and the bonding processing. Since the VCSEL wafer we used emitted at 850nm and was grown on a GaAs substrate, which absorbs 850nm wavelength light, the on-wafer test could only be top-emitting. However, the bonded VCSELs are bottom emitting after the substrate was removed. Therefore, the characteristics of the bonded VCSEL, e.g. threshold current and output optical power, could be quite different from the on-wafer test.

The difference of the threshold current between the top and back emitting VCSELs is due to the changing of the reflectivity of the mirrors during integration. In coplanar flip chip bonding and top-bottom contact bonding, the p-contact metal served as a reflective layer, thereby, increasing the reflectivity of the p-mirror. Substrate removal also changed the reflectivity of the n-mirror. Considering the relationship between threshold and VCSEL mirror reflectivity, the characteristics of bonded VCSELs can be predicted from the on-wafer test.

The reflectivity R of the quarter wavelength DBR mirror at the resonant wavelength is given by [35]:

$$R=\left[\frac{1-\frac{n_s}{n_0}\cdot\frac{n_1}{n_2}^{2m}}{1+\frac{n_s}{n_0}\cdot\frac{n_1}{n_2}^{2m}}\right]^2, \tag{3.1}$$

where m is the number of the non-absorbing DBR pairs, n_1 and n_2 are the reflective index of the low and high reflection layer of the DBR mirror, n_s and n_0 are the reflective index of the materials at each side of the DBR mirror.

If the cavity and mirror losses are ignored, the relation between the mirror reflectivity R_1, R_2 and the threshold gain g_{th} is given by [35]:

$$g_{th} = \frac{1}{2 \cdot l} \cdot ln \cdot \frac{1}{R_1 \cdot R_2}, \tag{3.2}$$

where l is the length of the active region.

Three VCSEL wafers were used in this research, EMC1632, EMC1584 and EMC1148. All of them are 850nm oxide-confined VCSELs with $Al_{0.98}GaAs$ oxide confinement layers on each side of the active layer. There are no inter-cavity contact layers in these wafers. The DBR pairs are composed of $Al_{0.92}GaAs/Al_{0.16}GaAs$ with grading interfaces.

The difference is that EMC1632 and EMC1584 are designed for back emitting while EMC1148 is a normal top emitting VCSEL wafer. Since the VCSEL epitaxial layers were grown on the n-doped substrates, back emitting design means that the n-mirror has fewer DBR pairs than the p-mirror. Table 3.1 summarized the structure of these VCSEL wafers.

Table 3.1 Summary of the VCSEL wafer involved in this research

VCSEL wafer	EMC1632	EMC1584	EMC1148
number of p-mirror DBR pairs	23	19	25
number of n-mirror DBR pairs	19	19	39
number of oxide confinement layers	5	5	1
number of quantum wells in active region	5	5	3

The on wafer test showed that EMC1632 and EMC1148 can lase, while EMC1584 can not. The mirror reflectivity and the threshold gain of the VCSEL wafer and the bonded VCSELs were estimated in order to predict the operation of the bonded VCSELs. Table

3.2 summarizes the calculated results. The reflective index of AlGaAs alloy used in this calculation are shown in table 3.3 [35].

Table 3.2 Mirror reflectivity and required threshold gain of VCSEL wafer and bonded VCSEL

	$R_{p\text{-mirror}}$	$R_{n\text{-mirror}}$	$g_{th}(cm^{-1})$
EMC1632			
VCSEL wafer	0.99853	0.98970	(lase)1478
coplanar flip chip and top-bottom bonded VCSEL	1.0	0.99625	(lase)470
top-contact bonded VCSEL	0.99595	0.99625	(lase)977
EMC1584			
VCSEL wafer	0.99625	0.98970	**(not)**1764
coplanar flip chip and top-bottom bonded VCSEL	1.0	0.99625	(lase)470
top-contact bonded VCSEL	0.98970	0.99625	**(not)**1764
EMC1148			
VCSEL wafer	0.99747	0.99973	(lase)583
coplanar flip chip and top-bottom bonded VCSEL	1.0	0.99997	(lase)7
top-contact bonded VCSEL	0.99303	0.99997	(lase)1463

Table 3.3 Reflective indices of AlGaAs alloy [35]

$Al_{0.16}GaAs$	$Al_{0.92}GaAs$	$Al_{0.98}GaAs$	GaAs
3.493	3.104	3.077	3.501

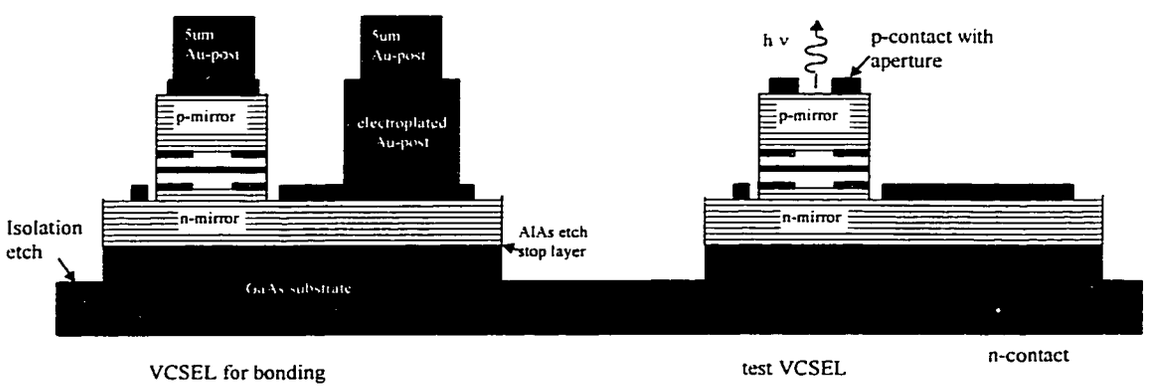
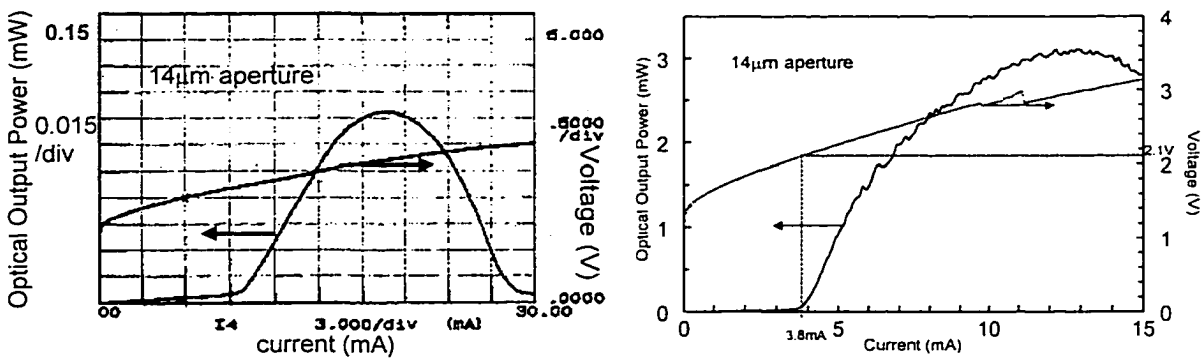


Figure 3.1 Coplanar flip chip bonding VCSEL and test VCSEL

Since the coplanar flip chip bonding technique fully processed the VCSELs before bonding, we designed a top emitting test VCSEL on the VCSEL arrays which were

fabricated for later coplanar flip chip bonding, as shown in figure 3.1. Therefore, the test VCSEL and the bonding VCSELs are fabricated simultaneously.

Figure 3.2(a) shows the I-V-L characteristics of the top emitting test VCSEL. The threshold current is 10mA when the aperture size is 14μm. After the VCSEL arrays were coplanar flip chip bonded to a GaAs dummy chip and the substrate of the VCSEL array was removed, the back emitting VCSEL was tested and the results are shown in figure 3.2(b). The threshold current reduced to 4mA with the same aperture size. The dramatic reduction of the threshold current fits very well with the calculation results. According to the calculation, the threshold gain of the coplanar flip chip bonded VCSEL is about one third of the top-emitting VCSEL. Therefore, except changing the reflectivity of the mirrors, the process itself will not impose any significant change on the characteristics of the VCSELs.



(a) top-emitting test VCSEL (b) coplanar flip chip bonded

Figure 3.2 I-V-L of the VCSELs made from EMC1632

With VCSEL wafer EMC1632, the top-emitting test VCSEL has the highest threshold gain and the experimental results showed that it can lase. Therefore, EMC1632 can be used for all of these three bonding techniques.

Although VCSEL wafer EMC1584 does not lase for top-emitting test VCSEL, the dramatic decrease of the threshold of the coplanar flip chip bonded VCSEL encouraged us to use this wafer for the top-bottom contact bonding. EMC1584 was top-bottom contact bonded to a GaAs dummy chip. The I-V-L characteristics were then measured, as shown in Figure 3.3. This time we tried a smaller aperture size of 6μm. The output optical power is quite low, approximately 70μW.

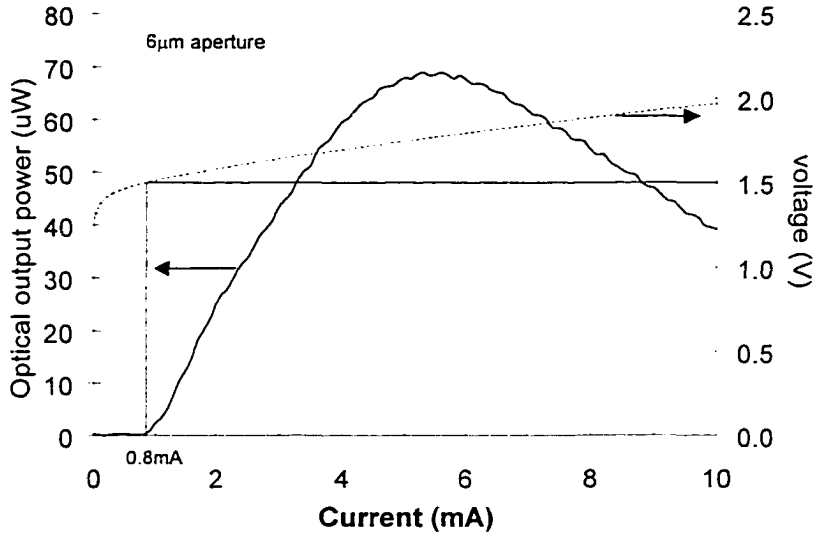


Figure 3.3 I-V-L characteristics of the top-bottom contact bonded VCSEL made from EMC1584

Therefore, both coplanar flip chip and top-bottom bonded VCSELs will have lower threshold current than the on wafer test VCSELs, mainly due to the gold layer on top of the p-mirror, which increases the reflectivity of the p-mirror. However, in top-contact bonding, the VCSEL wafer is glued to the pixel chip. There is no such advantage. We believe that the VCSEL wafer EMC1584 still can not lase after top-contact bonding, since the threshold gain will not change after bonding.

The threshold change of the top-contact bonded VCSEL from the test VCSEL is due to the substrate removal. According to equation 3.1, the reflectivity of the DBR mirror also depends on the terminating material. Since the GaAs substrate has a much higher reflective index than air, the DBR mirror has lower reflectivity when it is on the GaAs substrate than when it is exposed to the air. This situation also raises another concern, the surface material, which the VCSEL will be top-contact bonded to, may effect the threshold current of the bonded VCSEL. The calculation in this research assumed the VCSEL is top-contact bonded to a GaAs dummy chip.

According to the calculated results, the worst case was a VCSEL wafer EMC1148 with top-contact bonding. Therefore, EMC1148 was processed into top-contact bonded VCSELs on a GaAs dummy chip. In order to obtain higher output optical power (the very high reflectivity of its n-mirror may let almost nothing go out), a 20μm aperture was used. Figure 3.4 shows the I-V-L characteristics of the top-contact bonded VCSEL made from EMC1148. It does lase, although the enhanced spontaneous emission is significant.

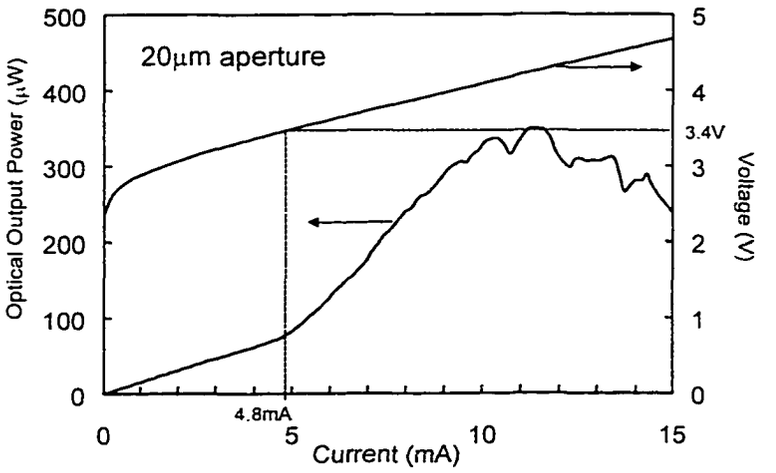


Figure 3.4 I-V-L characteristics of the top-contact bonded VCSEL made from EMC1148

Table 3.4 summarizes the experimental results with these three VCSEL wafers. EMC1632 and EMC1148 can be used for all three bonding techniques we developed, while EMC1584 can not be used for top-contact bonding.

Table 3.4 Summary of the experimental results

VCSEL wafer	p-mirror pairs	n-mirror pairs	Aperture size	threshold of top-emitting	threshold of bottom emitting
EMC1632	23	19	14μm	10mA	3.8mA coplanar flip chip bonding
EMC1584	19	19	6μm	does not lase	0.8mA top-bottom bonding
EMC1148	25	39	20μm	lase	4.8mA top-contact bonding

3.2. Characteristics of the bonded VCSEL arrays

In order to measure the bonded VCSEL arrays directly, the VCSEL arrays were first bonded to a GaAs substrate with Au-traces on it, i.e. a dummy chip. The same VCSEL wafer EMC1148 had been used in this measurement in favor of better comparison. The reason for us to choose EMC1148 is that we had a larger piece of EMC1148 than EMC1632. VCSEL wafer EMC1632 is too small to be processed with three integration techniques. 15μm aperture size was chosen to obtain a fair optical output power. Although we tried to obtain exactly the same aperture size, it is hard to accurately control the oxidation rate. The non-uniformity of the composition of the oxide confinement layer is one of the reasons. The aperture size varies from 14-17μm.

Figure 3.5 shows the I-V and I-L curves of the VCSEL array coplanar flip chip bonded to a GaAs substrate. The threshold current is in the range of 1.7-2.1mA, and the threshold voltage between 2.7 to 2.9V.

The average series resistance is 100Ω. The non-uniformity of the series resistance is due to the lack of intra-cavity contact layers. The n-contacts were deposited on the n-mirror layers. Since the mirror layers are only a few hundred Å thick and the non-uniformity of the dry-etch is 2000 Å, the device mesa etch can not be controlled to stop at the GaAs layer rather than the AlGaAs layer. Furthermore, the AlGaAs layer was also exposed to the corrosive environment for the oxidation and the Al_2O_3 is hard to remove. Therefore the n-contacts on the AlGaAs layer are not stable. Some of them even fell off during the following process. The unstable n-contact also contributes to the variation of threshold voltage.

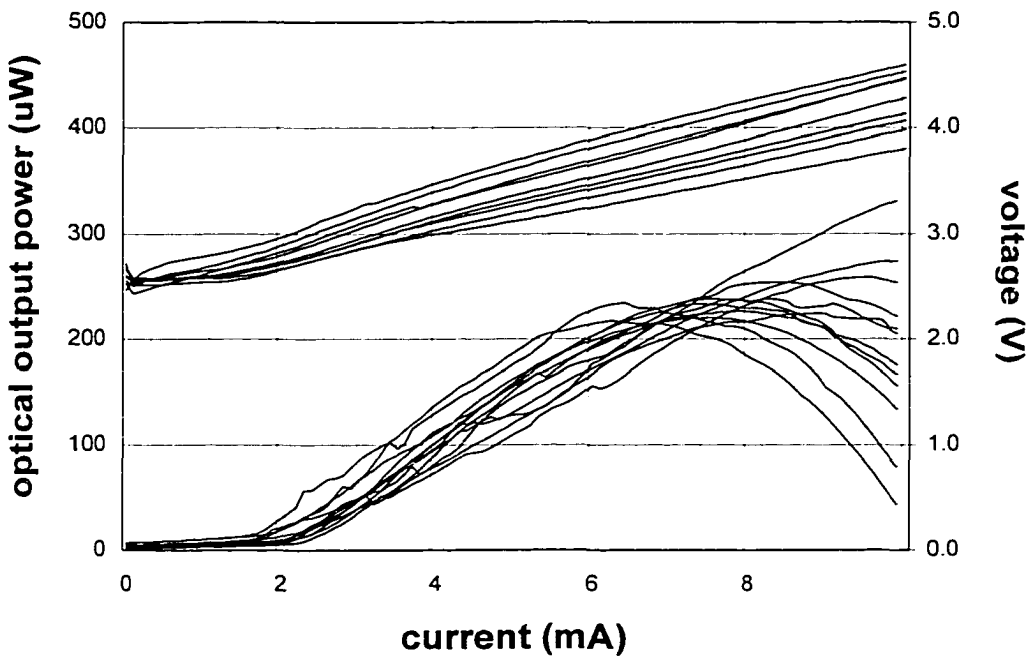


Figure 3.5 I-V-L curves for the VCSEL array
coplanar flip chip bonded to the GaAs substrate

As expected the maximum output optical power is low, approximately 200μW, because of the high reflectivity of the n-mirror. The non-uniformity of the maximum

optical output power also shows that the thermal properties of the bonded VCSEL are not the same as shown in the experimental results in the next chapter. The reason may be that the bonding process did not result in good contacts on all of the bonding pads due to the tilt, as show in figure 3.6. Since the volume of InSn we used is very small and no flux has been used during the heating, the InSn did not fill the air gap during heating. The non-uniform thermal property also contributes to the threshold current variation.

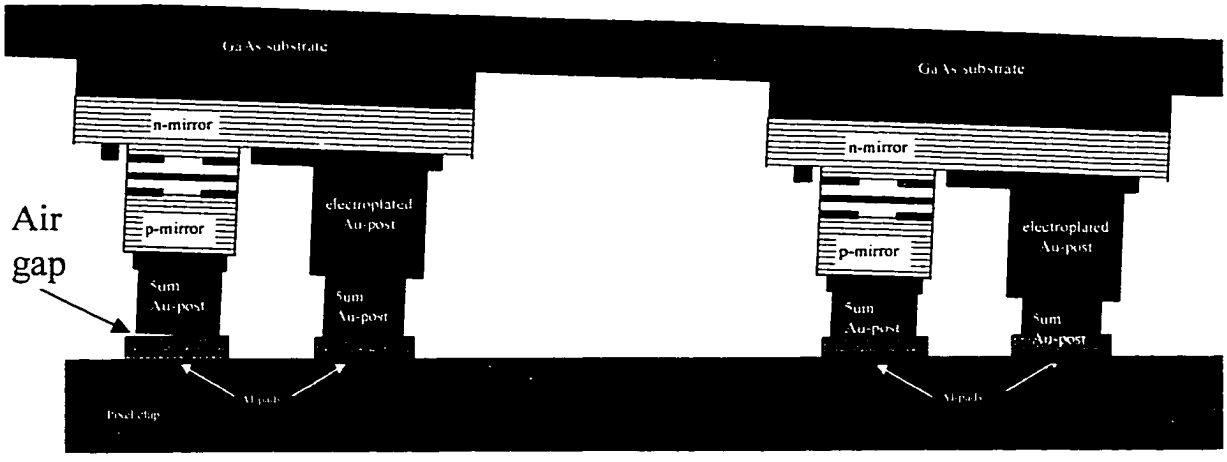


Figure 3.6 The contact which provides electronic connecting but poor thermal conduct

A map of an 8x8 array indicates the position of the lasing VCSELs, where ¤ indicates lasing. Most of the VCSELs can not lase because there is no electrical connection. All the lasing VCSELs are on the same side of the array. Therefore, tilt does exist during bonding processing. Obviously, other factors also effected the bonding yield. One of them is that, as we mentioned, the instability of the n-contact is not stable and the subsequent two electroplating process carried out on top of it. Therefore, some of the electroplated Au posts fell off during the processing.

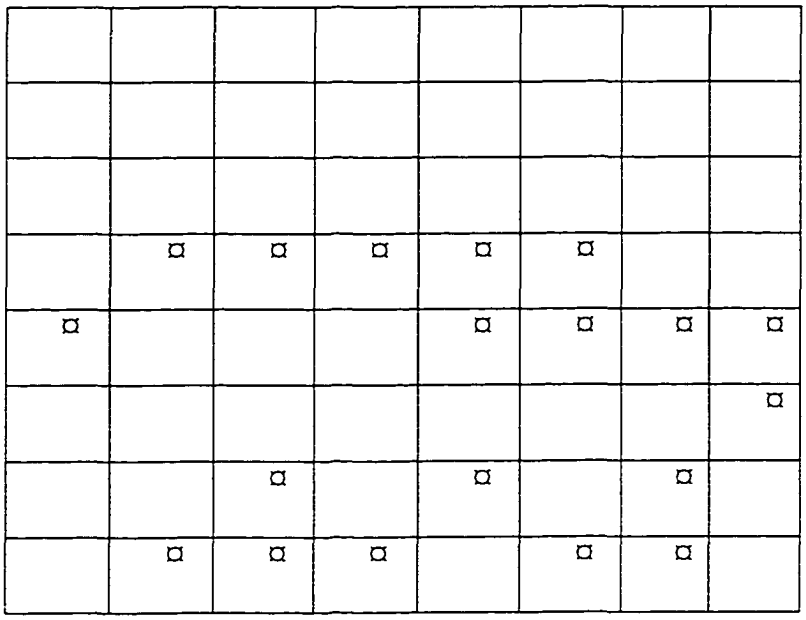
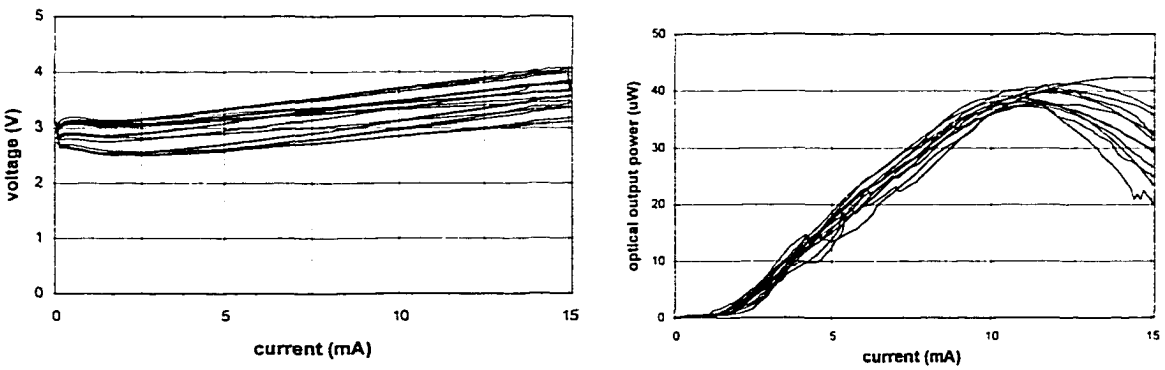


Figure 3.7 The lasing VCSELs' position on the coplanar flip chip bonded VCSEL array

Figure 3.8 shows the I-V and I-L curves of the VCSEL array top-bottom contact bonded to a GaAs substrate. The threshold current is about 2mA and shows better uniformity than the coplanar flip chip bonded VCSEL array. The optical output power also shows good uniformity. This means the bonded VCSELs have uniform thermal property and suggests that it is easier to make better contacts with top-bottom contact bonding than with coplanar flip chip bonding.



(a) I-V curves (b) I-L curves

Figure 3.8 Characteristics for the VCSEL array top-bottom contact boded to the GaAs substrate

The optical output power of top-bottom bonded VCSELs is smaller than coplanar flip chip bonded VCSELs, because the top metal contacts may block some of the output light. The metal aperture size is only 16μm, which is similar to the oxide confined aperture, thus if there is any misalignment the top metal contacts may block some of the output light.

The series resistance is approximately 70Ω, which is smaller than coplanar flip chip bonding, because top-bottom contact bonding does not require inter-cavity contacts.

Figure 3.9 illustrated the location of lasing VCSELs' for the top-bottom contact bonded VCSEL array. Most of the VCSELs which do not lase because there are no electrical connections. From the location map, we can see that the bonding yield of the top-bottom contact bonding technique mainly depends on the tilt during bonding.

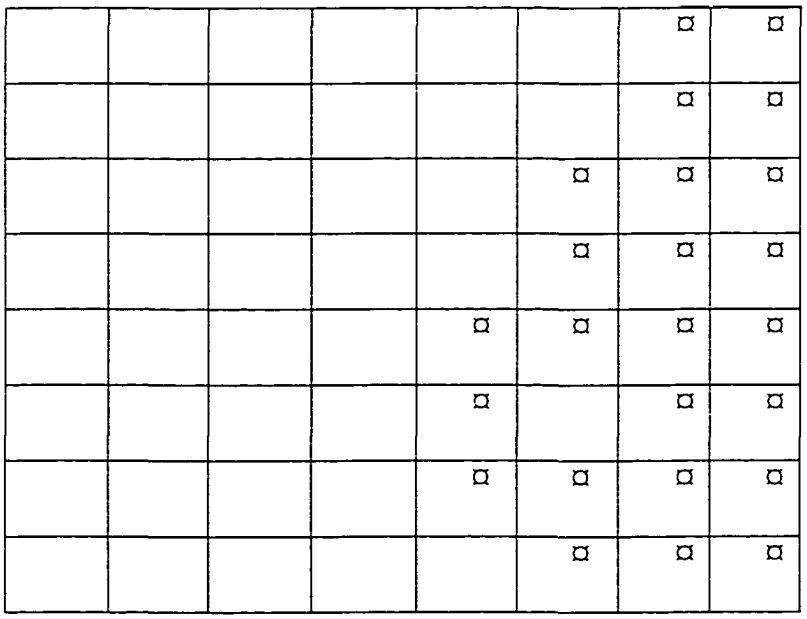
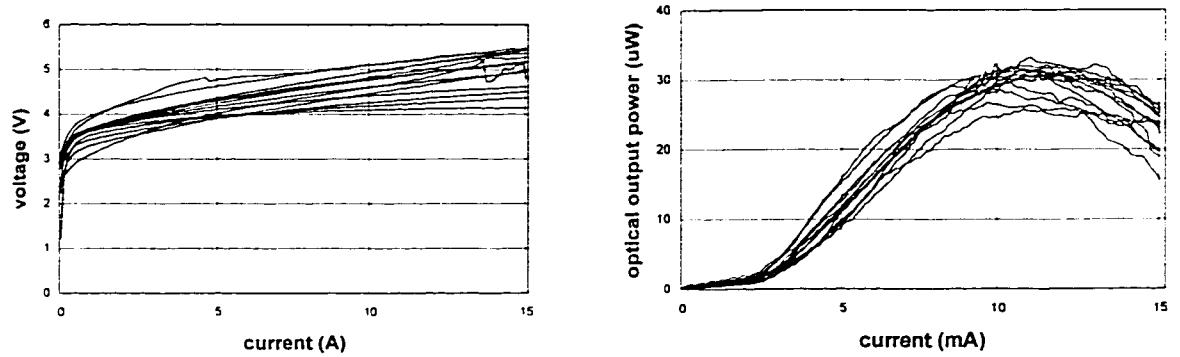


Figure 3.9 The lasing VCSELs' position on
the top-bottom contact bonded VCSEL array

Figure 3.10 shows the I-V and I-L curves of the VCSEL array top contact bonded to a GaAs substrate. The threshold current is about 2.5mA. The threshold voltages varies from 3.5 to 4.5 volts. The relatively high voltage is due to the lack of contact layers for both p- and n-contact. The series resistance is approximately 120Ω, which is also larger than coplanar flip chip bonding.



(a) I-V curves (b) I-L curves

Figure 3.10 Characteristics for the VCSEL array top contact boded to the GaAs substrate

Figure 3.11 illustrated the lasing VCSELs' position for the top contact bonded VCSEL array. Since the VCSEL wafer was "glued" to the pixel chip, there is no tilt problem in top-contact bonding technique. Unlike the other two bonding techniques, the VCSEL can not lase not only because the circuits were shorted but also because the circuits were open. The polyimide served as the step coverage layer. The over-developed polyimide pattern, which did not cover the side wall of the VCSEL mesa, resulted in the shorted circuits. Therefore, the yield of the top contact bonded VCSEL mainly depends on the isolation layer.

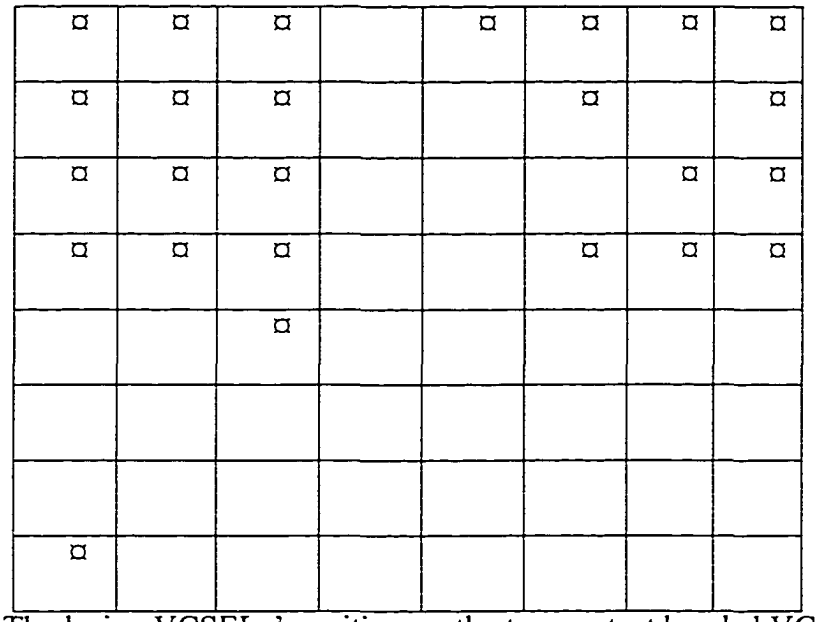


Figure 3.11 The lasing VCSELs' position on the top contact bonded VCSEL array

3.3. Smart pixel functionality

The results discussed in the previous two sections were obtained from VCSELs bonded to dummy GaAs substrates to evaluate the quality of the VCSEL after bonding. This section presents results and discusses issues for VCSELs bonded to foundry fabricated Si CMOS and GaAs MESFET integrated circuit chips to evaluate the smart pixel.

These smart pixels were fabricated only with the coplanar flip chip bonding technique. The coplanar flip chip bonding technique requires the least processing steps on the electronic chip among these three techniques. The VCSEL array was fully processed before bonding. The only photolithography that needs to be done on the electronic chip is for depositing Au on the Al bonding pads of the electronic chip. On the other hand, the Au-posts are required to be electroplated on the electronic chip, which requires two photolithography steps, in the top-bottom bonding technique. An additional n-contact

deposition is also required after the VCSEL array is bonded to the electronic chip. In the top-contact bonding technique, all the processing steps are carried out after the VCSEL wafer is bonded to the electronic chip.

Unlike the dummy GaAs substrate, which we can cut as big as we want, the foundry fabricated electronic chips we used are very small (<3x3mm^2). Therefore, it is hard to process them. For example, normally photolithography requires removing the edge bead of photoresist in order to obtain a flat surface, as shown in figure 3.12. The very small die does not have sufficient margin for performing this task.

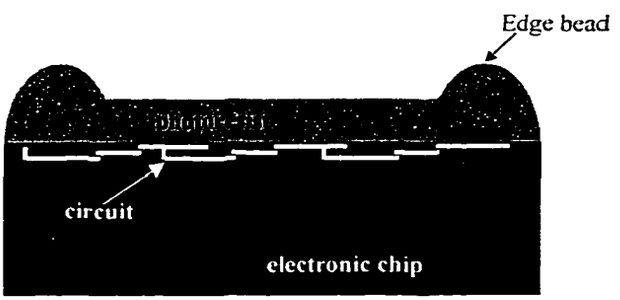


Figure 3.12 The edge bead of the photoresist after spinning

Although they have not been accomplished on foundry fabricated chips, the last two techniques are still interesting, if the bonding can be performed before the electronic chip has been cut to small die.

The smart pixels were fabricated with VCSEL wafer EMC1632 to obtain higher optical output power, which made the testing of the smart pixel easier.

An 8x8 VCSEL array was coplanar flip chip bonded to a foundry fabricated MESFET chip. The chip performs the selection function of a data filter. The chip was designed by Eric Hayes and fabricated by Vitesse through the MOSIS foundry service. The logic

function performed by this smart pixel is shown in the block diagram of figure 3.13. Following the truth table 3.1, MSM C was illuminated with a fiber, A and B were off as shown in figure 3.14, the bright area above the VCSEL is the reflection from the fiber providing the optical input. As the input optical power increases, the output VCSEL turned on from below threshold (figure 3.14 (a)) to above threshold (figure 3.14 (b)). Therefore, the optical-in optical-out smart pixel array operates correctly and bonding to a foundry fabricated chip is demonstrated.

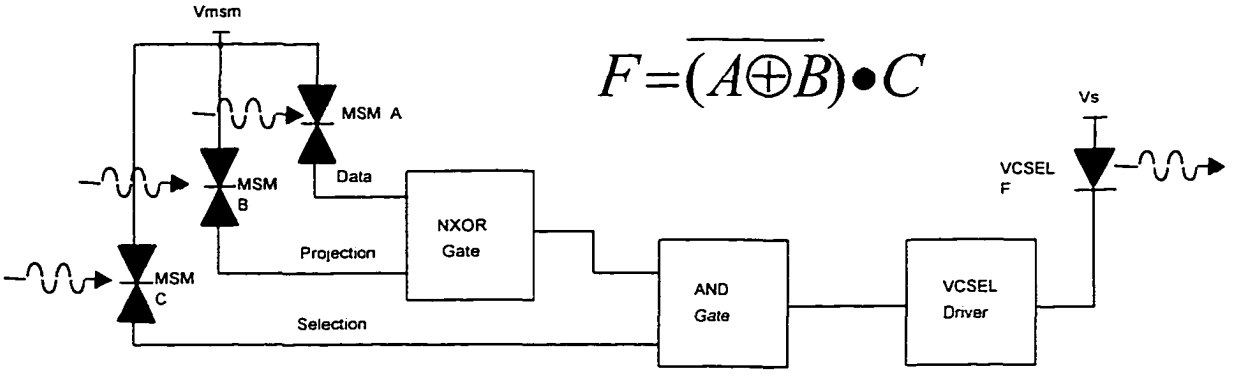
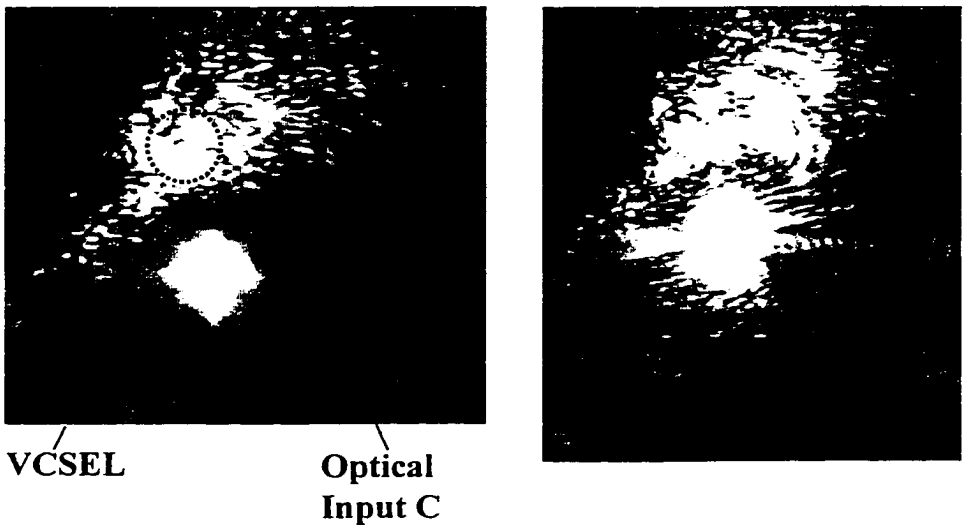


Figure 3.13 Logic function of the smart pixel for a data filter system

Table 3.1 Truth table of the smart pixel for a data filter system

A	B	C	F
0	0	1	1
1	1	1	1



(a) VCSEL was below threshold (b) VCSEL was above threshold

Figure 3.14 CCD camera image of the output of a
VCSEL-MESFET smart pixel with the pixel photo-actived

A 4x4 VCSEL array was also coplanar flip chip bonded to a CMOS chip to form a transmitter array for an optical ATM switch. The CMOS chip was designed by David Duan and fabricated by HP through the MOSIS foundry service. Figure 3.15 shows the 4x4 transmitter array with 9 of the VCSELs turned on. Preliminary high speed measurement shows that the transmitter has ~0.7ns rise time and ~1.5ns fall time approximately independent of the VCSEL bias voltage, as shown in figure 3.16. The longer fall time is probably due to the long discharge time of the photodetector that we used in this measurement or the reflection due to the impedance mismatch.

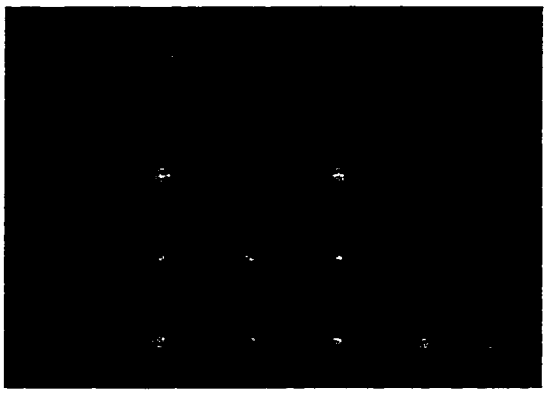


Fig.3.15 CCD camera image of the 4x4 VCSEL-CMOS smart pixel array with some of the VCSELs turned on

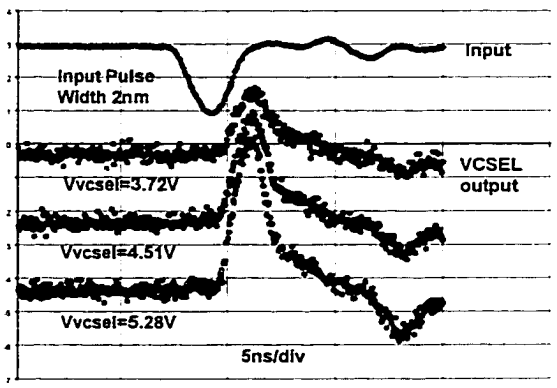


Figure 3.16 High speed measurement of the VCSEL-CMOS smart pixel

3.4. Summary

The results present in this chapter demonstrate that VCSEL arrays can be bonded to a variety of substrates without degrading the VCSEL performance or affecting the foundry fabricated integrated circuits.

CHAPTER 4

THERMAL PROPERTIES OF VCSEL BASED SMART PIXELS

Along with the rapid development of VCSELs and VCSEL arrays [16][17][18], the techniques for bonding VCSEL arrays to microelectronic circuits have attracted enormous interests and great progress has recently been reported. After the first 8x8 VCSEL array was bonded to a MESFET chip in 1997[13], VCSEL arrays bonded to a CMOS chips have been reported several times [23] [27]. The size of the bonded arrays have grown from 4x4[36], 2x10[23] to 16x16[37], the solder size has decreased from 30μm[13] to 10μm[23] and the pitch of the array reduced from 250μm[13] to 125μm[23]. However, the ability to remove the heat generated by the VCSEL, which will limit the density of the array, has not been investigated.

Thermal effects are also known to limit the output optical power and efficiency of VCSELs as well as the scalability and density of the integrated arrays. Thermal resistance and thermal crosstalk are indicators of the thermal properties of the integrated structure. In this chapter, the results of thermal resistance and crosstalk measurements are reported. The experimental results show the relationship between the thermal property and the I-V-L characteristics of the bonded VCSELs.

In addition, a two-dimensional thermal transfer model was constructed to analyze the three bonding techniques. The real three-dimensional structure was simplified to a two-dimensional cylindrically symmetric structure based on equivalent thermal resistance and provided results comparable to the experimental results. Furthermore, we are not strictly interested in the exact values obtained from the simulation, but the trends, which point the direction for optimizing these bonding structures and show the thermal limits of the integration density.

4.1. Thermal resistance and crosstalk measurement

The thermal resistance R_{th} of a device is generally defined as the temperature rise ΔT in the device with the change of power dissipation, ΔP:

$$R_{th}=\Delta T/\Delta P \tag{4.1}$$

Since the index of refraction changes with temperature, the longitudinal-mode spectrum of the VCSEL will also change. By first measuring the wavelength change with temperature $\Delta\lambda/\Delta T$, and then measuring the effect that dissipated power has on wavelength $\Delta\lambda/\Delta P$, we can correlate temperature change to dissipated electrical input power change [33].

The thermal crosstalk R_{12} can be described as the temperature change of device 1, ΔT_1 with the power dissipation change of device 2, ΔP_2:

$$R_{12}=\Delta T_1/\Delta P_2 \tag{4.2}$$

The thermal crosstalk can be measured by driving VCSEL1 at constant input power and varying the electrical input power of its neighbor [32].

The set up for the thermal resistance and crosstalk measurements is illustrated in Figure 4.1. The temperature of the VCSEL is controlled by a temperature controller with

a thermoelectric cooler. The wavelength of the VCSEL emission was measured with a spectrometer.

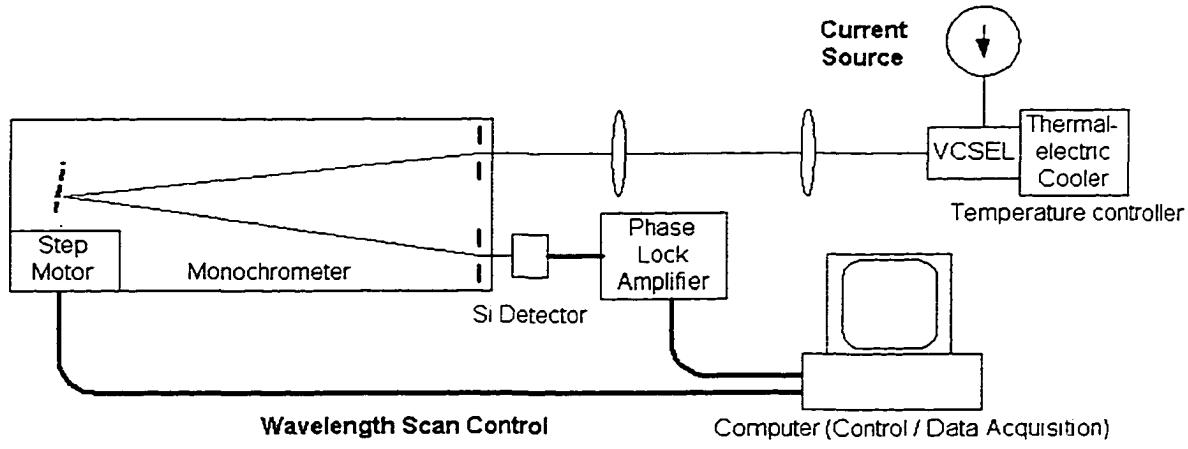


Figure 4.1 Set up for thermal resistance and crosstalk measurement

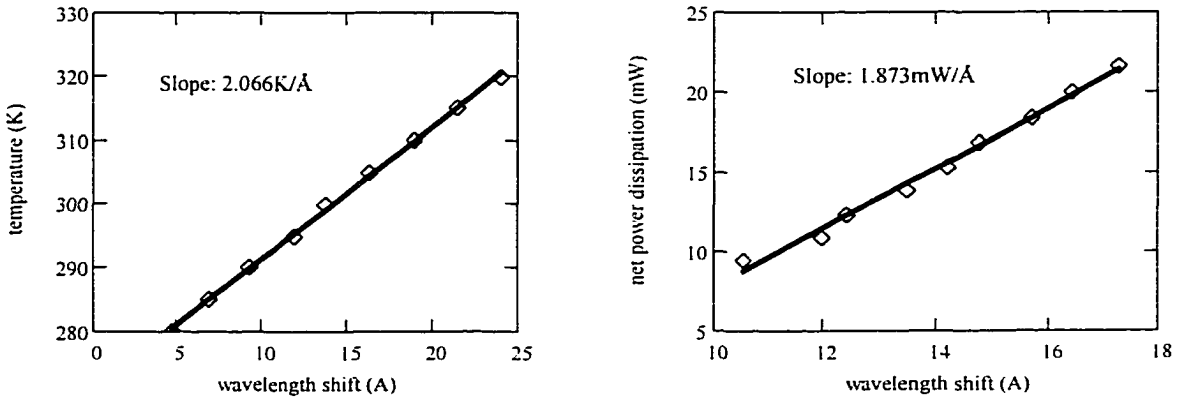
In order to isolate the thermal resistance of the bonding from the thermal resistance of the CMOS or MESFET chip, the thermal resistance of VCSELs bonded to a GaAs dummy substrate have been measured. The results show that if the bonding process was not properly done, the thermal resistance could be increased significantly. The thermal resistance of a VCSEL bonded on Si CMOS or GaAs MESFET chips was then measured. Since the thermal crosstalk is very small, the measurement is not very accurate. However, it still gives us the general idea about the range of the thermal crosstalk.

All of the VCSELs used for bonding were made from VCSEL wafer EMC1148 and have approximately 15um apertures. The thickness of the p-mirror and n-mirror of EMC1148 is 3.5 μm and 5.0μm respectively. Normally, if the VCSELs have similar I-V-L characteristics, the VCSELs have similar thermal properties, because the thermal properties influence the maximum output optical power and efficiency of VCSELs. Therefore, although the measurements only show one typical device on each bonded array, similar thermal properties can be expected for the devices on the same array.

4.1.1 Thermal resistance measurement of the VCSEL array bonded to GaAs substrates

Two pieces of VCSEL arrays were prepared for coplanar flip chip bonding to a dummy GaAs substrates. One of them has very accurate coplanar n-contacts, i.e. the Au post height is within ±0.1μm of the p-mirror height. We call this "sample coplanar A". The n-contact of the second sample is 1μm higher than the p-contact. We call it "coplanar B".

The measurement of coplanar A VCSEL bonded to GaAs is shown in figure 4.2. The wavelength of the fundamental mode is measured as a function of temperature at 4mA drive current (figure 4.2(a)), which is 2mA above the threshold. The temperature of the VCSEL was controlled by a thermoelectric cooler. This results in a straight line with a slope (wavelength shift) of 2.066K/Å. The dissipated power of the VCSEL is taken as the input electrical power minus the output optical power. The wavelength shift dependence on power dissipation is 1.873mW/Å (figure 4.2(b)). By dividing the temperature dependence by the power dependence, we obtain 1100K/W for the thermal resistance.



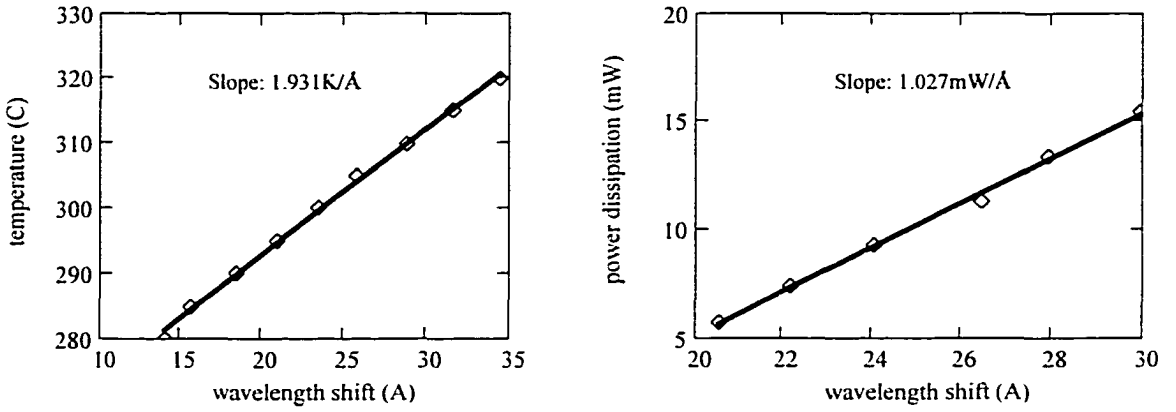
(a) wavelength versus temperature (b) wavelength versus dissipated power

Figure 4.2 Thermal resistance measurement of the coplanar A VCSEL properly coplanar flip chip bonded to GaAs substrate

Since the spectrum analyzer was not calibrated, only the wavelength shifts have been measured. Fortunately, in the thermal resistance measurement, the wavelength shift gives us enough information. Therefore, the absolute value of the lasing wavelength is not important.

Among all the instruments used for the thermal measurements, e.g. temperature controller, ampmeter, and optical power meter, the spectrometer is the most inaccurate because the motor of the monochrometer and the detective system needed to be turned on simultaneously. By measuring the same point several times, we found that the accuracy of the wavelength is within 0.2Å. The total wavelength shift in the thermal resistance measurement is 20Å and 6Å for the temperature dependence and the power dissipation dependence, respectively. 0.2Å is 3.3% of 6Å. Therefore, the accuracy of the thermal resistance measurement is approximately 3.3%.

Figure 4.3 shows the thermal resistance measurement data for coplanar B VCSELs bonded to a GaAs substrate. Unsurprisingly, these two devices have similar wavelength shift with temperature, about 2K/Å. However, the thermal resistance of coplanar B is 1880K/W, which is 70% higher than coplanar A. This is due to the poor contact caused by the large difference in the n- and p- contact post height.



(a) wavelength versus temperature (b) wavelength versus dissipated power

Figure 4.3 Thermal resistance measurement of the coplanar B VCSEL not properly coplanar flip chip bonded to GaAs substrate

A large non-uniformity also appeared on the bonded coplanar B VCSEL array. Figure 4.4 shows the I-V-L curves of two VCSELs on the bonded coplanar B VCSEL array with their measured thermal resistance. The most significant difference between these two VCSELs is the drive current for the maximum output optical power. If the device is designed to align the lasing wavelength to the gain peak at certain temperature, the VCSEL with the lower thermal resistance will reach that temperature with a higher drive current.

The VCSEL with the smaller thermal resistance also has a lower threshold current and higher optical output power than the other one. The output optical power does not show a great difference because the high reflectivity of the n-mirror limits the optical output power. The presented results verifies that the thermal property affects the characteristics of the VCSEL.

On the other hand, the VCSEL with the smaller thermal resistance shows higher series resistance. The smaller thermal resistance means higher quality of the bonding. The serial resistance resulted from the bonding should also be lower. Thus, there must be other facts

increasing the serial resistance. We believe it is the unstable metal-semiconductor contact due to the lack of intra-cavity contact layer.

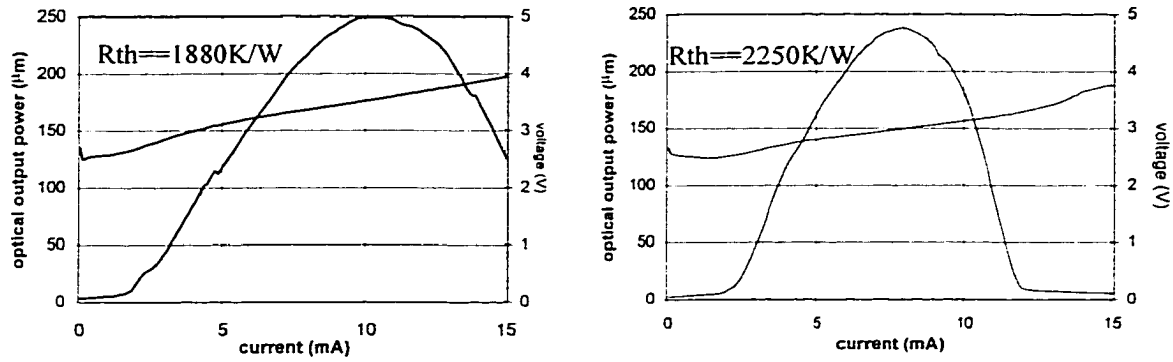
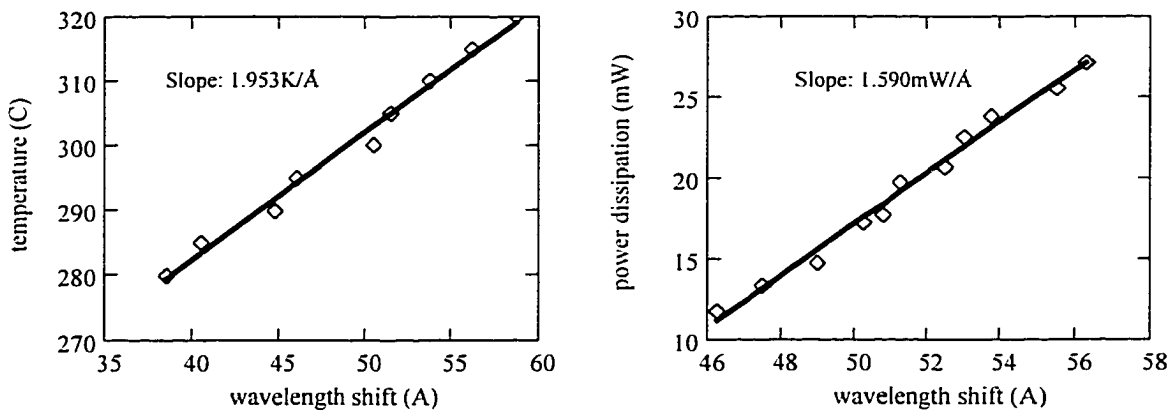


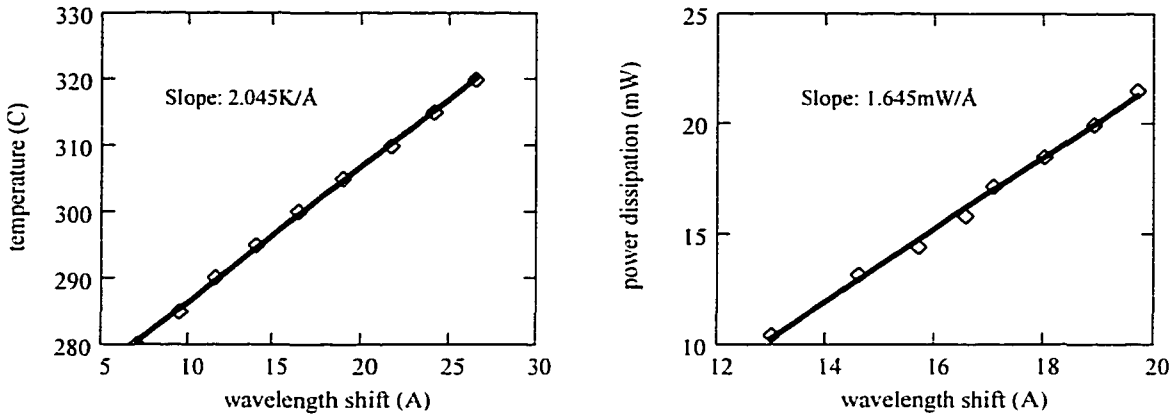
Figure 4.4 I-V-L characteristics of VCSELs with different thermal resistance

The thermal resistance measurements of the VCSELs top-bottom and top-contact bonded to the GaAs substrates are shown in figure 4.5 and 4.6 respectively. The thermal resistance of top-bottom bonded VCSELs is 1230K/W, as is the thermal resistance with top-contact bonding 1240K/W. Top-contact bonding did not show significantly higher thermal resistance than the other two bonding techniques because the epoxy layer between the VCSEL and the GaAs substrate is very thin.



(a) wavelength versus temperature (b) wavelength versus dissipated power

Figure 4.5 Thermal resistance measurement of the VCSEL top-bottom bonded to GaAs substrate



(a) wavelength versus temperature (b) wavelength versus dissipated power

Figure 4.6 Thermal resistance measurement of the VCSEL top-contact bonded to GaAs substrate

Table 4.1 summarized our thermal resistance measurements. They are similar to most of the reported measurements of the VCSEL devices or bonded VCSELs. Matsuo and his coworkers at NTT developed a bonding technique using polyimide to attach the VCSELs onto the Si substrate [10]. The thermal resistance of the VCSEL bonded with 0.25μm polyimide is 1600K/W. Thermal resistance of 1200-1500K/W for oxide confined VCSELs was also reported by Lascola and his coworkers at UC Berkley [11]. The thermal resistance of the unbonded VCSEL mainly depends on the mirror layers underneath the active region. Different VCSEL mirror designs can result in quiet a different thermal resistance. Therefore, this comparison only shows a reasonable range of the thermal resistance of a working VCSEL.

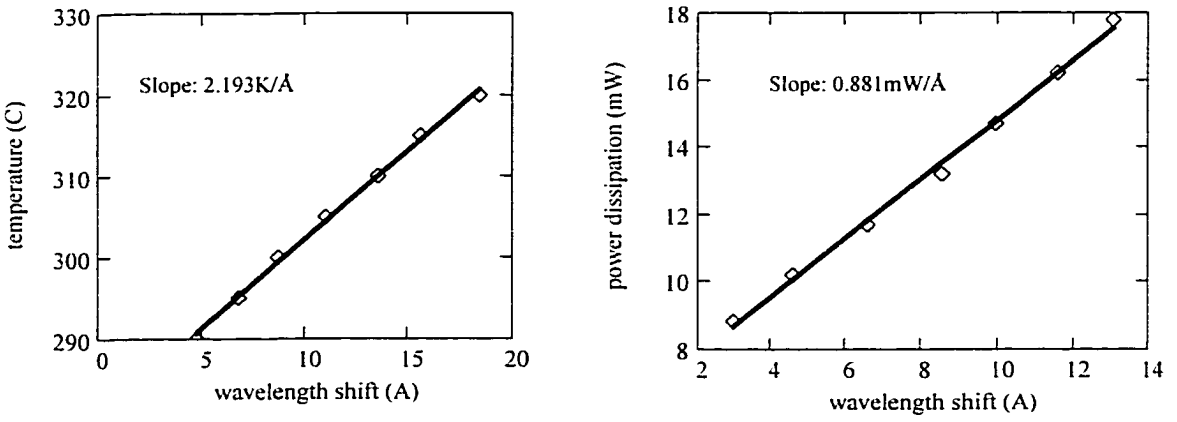
Table 4.1 thermal resistance of the bonded and standard VCSELs

Author	Bonding technique	thermal resistance
Present work	coplanar flip chip (properly bonded)	1100 K/W
	coplanar flip chip (not properly bonded)	1880-2250K/W
	top-bottom	1230 K/W
	top-contact	1240 K/W
NTT[38]	polyimide bonded	1600K/W
UC Berkley[39]	Un-bonded standard oxide confined VCSEL	1200-1500K/W
UCSB	Un-bonded standard air post VCSEL	2720K/W
USC	Un-bonded standard oxide confined VCSEL	2500

4.1.2 Thermal resistance measurement of the VCSEL array bonded to MESFET and CMOS chips

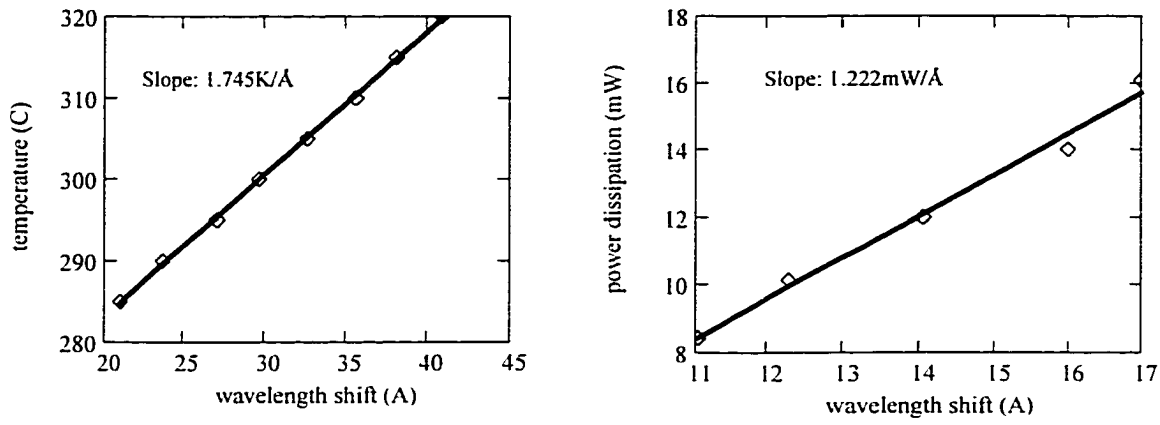
In addition to the investigation of VCSELs bonded to dummy GaAs chips discussed in the previous section, VCSELs coplanar flip chip bonded to the MESFET and CMOS have also been measured and compared to VCSELs bonded to GaAs dummy substrates. In fact, since the coplanar flip chip and the top-bottom bonding have similar thermal transfer path, we can also predict the thermal properties of the VCSELs top-bottom bonded to the electronic chips by these measurements.

The thermal resistance measurements of the VCSELs coplanar flip chip bonded to the CMOS and MESFET chips are shown in figure 4.7 and 4.8 respectively. The thermal resistance of the VCSEL bonded to the Si CMOS chip is 2490K/W, and the thermal resistance of the VCSEL bonded to the GaAs MESFET chip is 1430K/W. Table 4.2 summarizes the thermal resistance of the coplanar flip chip bonded VCSELs.



(a) wavelength versus temperature (b) wavelength versus dissipated power

Figure 4.7 Thermal resistance measurement of the VCSEL coplanar flip chip bonded to a Si CMOS chip



(a) wavelength versus temperature (b) wavelength versus dissipated power

Figure 4.8Thermal resistance measurement of the VCSEL coplanar flip chip bonded to a GaAs MESFET chip

Table 4.2 Thermal resistance of the coplanar flip chip bonded VCSELs

pixel chip	GaAs	Si CMOS	GaAs MESFET
thermal resistance	1100 K/W	2490 K/W	1430 K/W

The high thermal resistance of the VCSEL bonded to the Si CMOS chip is caused by the dielectric layers underneath the bonding pads, as shown in figure 4.9. Standard CMOS pads were used on the chips. There are three dielectric layers between metal layer 3, 2, 1 and the Si substrate. For a better power dissipation and lower thermal resistance, as many Al vias as the design rules allow can be put directly underneath the bonding pads (as shown underneath the right bonding pad). The number of the vias is also limited by the available room at each metal layer.

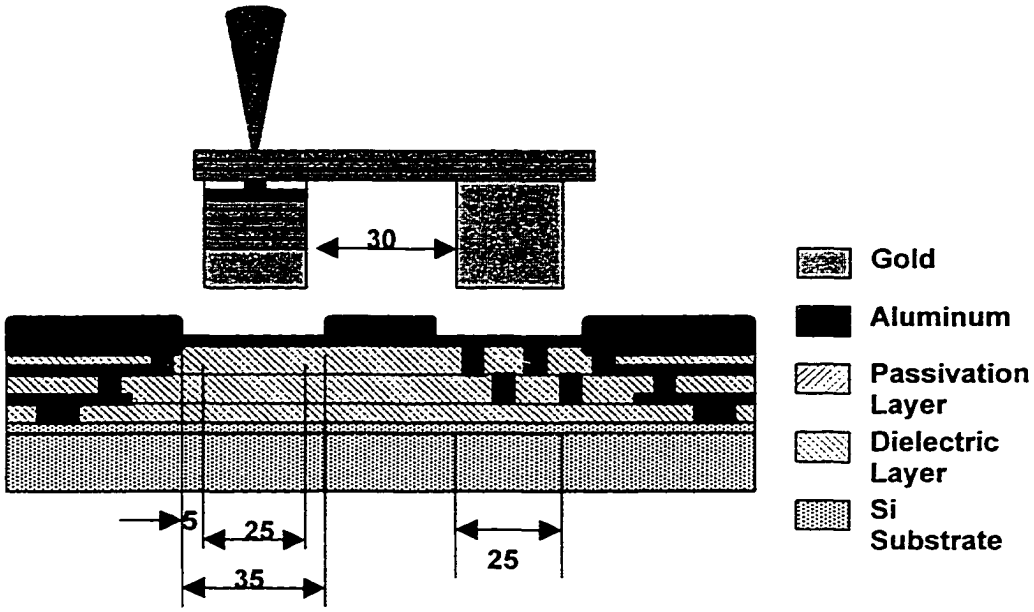
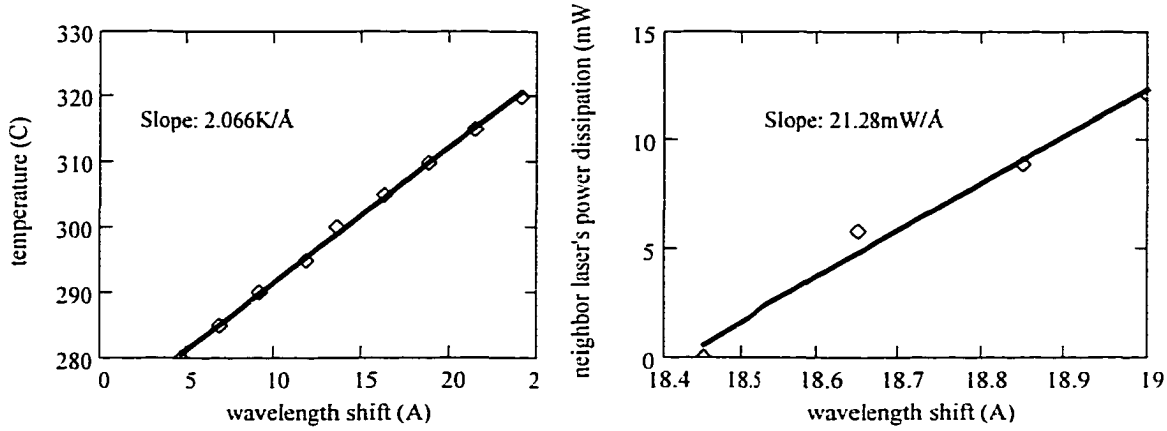


Figure 4.9 Schematic drawing of a VCSEL flip chip bonded to a CMOS chip

4.1.3 Thermal crosstalk measurement

The thermal crosstalk mainly depends on the pitch of the VCSEL arrays. The VCSEL arrays bonded by all three techniques have a 250μm pitch. Therefore, the thermal crosstalk should be the same for all three and was only measured between coplanar flip chip bonded VCSELs.

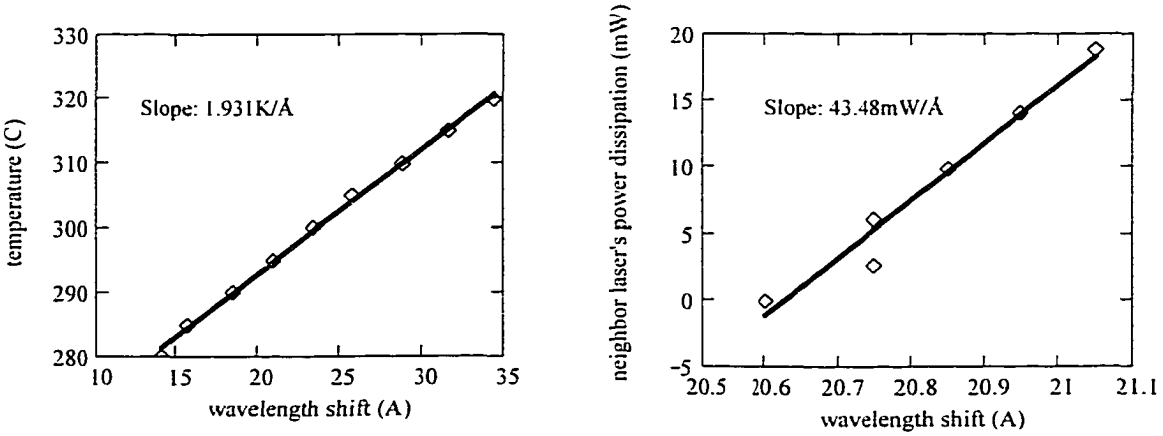
The thermal crosstalk measurement of the coplanar A VCSEL coplanar flip chip bonded to GaAs substrate is shown in figure 4.10. The measurement of the wavelength shift as a function of temperature is the same as the thermal resistance measurement, shown in figure 4.10(a). The wavelength shift dependence on the power dissipation of the nearest neighbor VCSEL was measured (figure 4.10(b)). The total wavelength shift in this measurement is as small as 0.5Å. We have already stated that the accuracy of the spectrum we used is only 0.2 Å, therefore, the error of this measurement can be as large as 40%. The thermal crosstalk obtain from figure 4.10 is 97K/W.



(a) wavelength versus temperature (b) wavelength versus dissipated power of neighbor

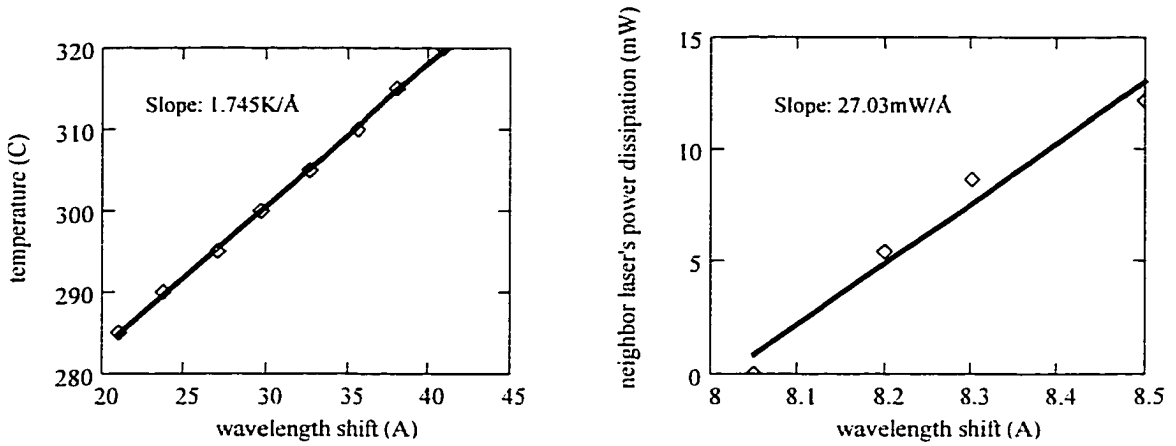
Figure 4.10 Thermal crosstalk measurement of the coplanar A VCSEL coplanar flip chip bonded to a GaAs substrate

The thermal crosstalk measurements of the coplanar B VCSEL coplanar flip chip bonded to a GaAs substrate and the VCSEL coplanar flip chip bonded to a MESFET chip are shown in figure 4.11 and 4.12 respectively. The thermal crosstalk of the coplanar VCSEL A bonded to the GaAs substrate is 45K/W, and the thermal crosstalk of the VCSEL bonded to the GaAs MESFET chip is 65K/W.



(a) wavelength versus temperature (b) wavelength versus dissipated power of neighbor

Figure 4.11 Thermal crosstalk measurement of the coplanar B VCSEL coplanar flip chip bonded to a GaAs substrate



(a) wavelength versus temperature (b) wavelength versus dissipated power of neighbor

Figure 4.12 Thermal crosstalk measurement of the VCSEL coplanar flip chip bonded to a GaAs MESFET chip

Table 4.3 summarized the thermal crosstalk and resistance measurements of the coplanar flip chip bonded VCSELs. It shows that the higher the thermal resistance of the individual device, the lower the thermal crosstalk. However, a higher thermal resistance will result in higher temperature with the same power dissipation, therefore higher thermal crosstalk. The error might be from the measurement.

The information that we obtained from this measurement is that an array with 250μm pitch has less than 100K/W thermal crosstalk. This number corresponds to a 1K temperature rise of the laser when its nearest neighbor laser operates with 10mW dissipated power. T. Wipiejewski and his coworkers at UCSB reported the thermal crosstalk saturated at 16mW/K when the pitch is larger than 100μm [9]. 16mW/K equals to 62.5K/W, which is close to the value of our measured thermal crosstalk.

Table 4.3 thermal resistance and crosstalk of the coplanar flip chip bonded VCSELs

	GaAs substrate (properly bonded)	GaAs substrate (not properly bonded)	GaAs MESFET
thermal resistance	1100 K/W	1880 K/W	1430 K/W
thermal crosstalk	96	45	65

4.2. Two-dimensional cylindrically symmetric model of the three bonding structure

This section describes a simplified thermal model of the bonded VCSEL. This model was used in a finite element analysis investigation of the thermal resistance. The whole idea of the simplified model is to divide the real structure into several parts according to the approximate heat flow direction and using a cylindrically symmetric structure, which has the equivalent thermal resistance.

We consider the heat to be generated only in the active region. Since the series resistance of the VCSELs bonded by these three techniques does not show a big difference, between 70- 120Ω, ignoring the heat generated by the series resistance will not significantly affect the following comparison. Furthermore, after the processing is optimized, the series resistance will be reduced. The series resistance of an unbonded VCSEL can be as low as 30Ω.

The surface radiation and convection are also ignored since they only contribute a very small portion of the heat loss, less than 1%[40]. The surface radiation and convection can also be estimated under normal condition. The measured thermal resistance of the bonded VCSEL is less than 2500K/W, which means the temperature of the VCSEL is no more than 50K higher than the surrounding air when the VCSEL is operating at 20mW input

electrical power. Assuming the VCSEL operates in an environment of room temperature, T_∞=295K, and the free convection heat transfer coefficient h is 15W/m^2·K, then the net heat loss by radiation is prescribed by the *Stefan-Boltzmann* law [41];

$E=\sigma(T_{surface}^4-T_\infty^4)=(5.67\text{x}10^{-8}\text{W/m}^2\cdot\text{K}^4)[(345\text{K})^4-(295\text{K})^4]=374\text{W/m}^2$

Where σ is the *Stefan-Boltzmann* constant,

and the heat loss by convection to the room air q is

$q=h\,(T_{surface}-T_\infty)=(15\text{W/m}^2\cdot\text{K})(50\text{K})=750\text{W/m}^2$

The surface area of the VCSEL we fabricated is less than $4\text{x}10^{-8}\text{m}^2$. Therefore the heat loss from the surface is less than 0.05mW, which is far less than the total heat generated by the VCSEL, 20mW.

Although the model is very simple, what we are interested in is not the exact value of the simulation, but the trends. In this case, the model is good enough for the analysis.

4.2.1 Thermal transfer model of a coplanar flip chip bonded VCSEL

The simplification of the theoretical mode is based on equivalent thermal resistance. The two fundamental equations of the thermal resistance are described as follows;

The thermal resistance R_{th} of a planar wall is defined by[13]

$$R_{th} = L/kA \tag{4.3}$$

where L is the length of the heat path, A is the area of cross section, and k is the material conductivity. The thermal resistance R_{th} of a cylindrical wall is prescribed by [13]

$$R_{th} = \ln(R2/R1)/2\pi L_{thick}k \tag{4.4}$$

It is easy to understand that there are two paths for the heat generated by the active region to go to the substrate, as shown in figure 4.13;

1) going through the p-mirror and the solder in the vertical direction,

2) going through the n-mirror in the transverse direction, then through the coplanar p-contact in the vertical direction.

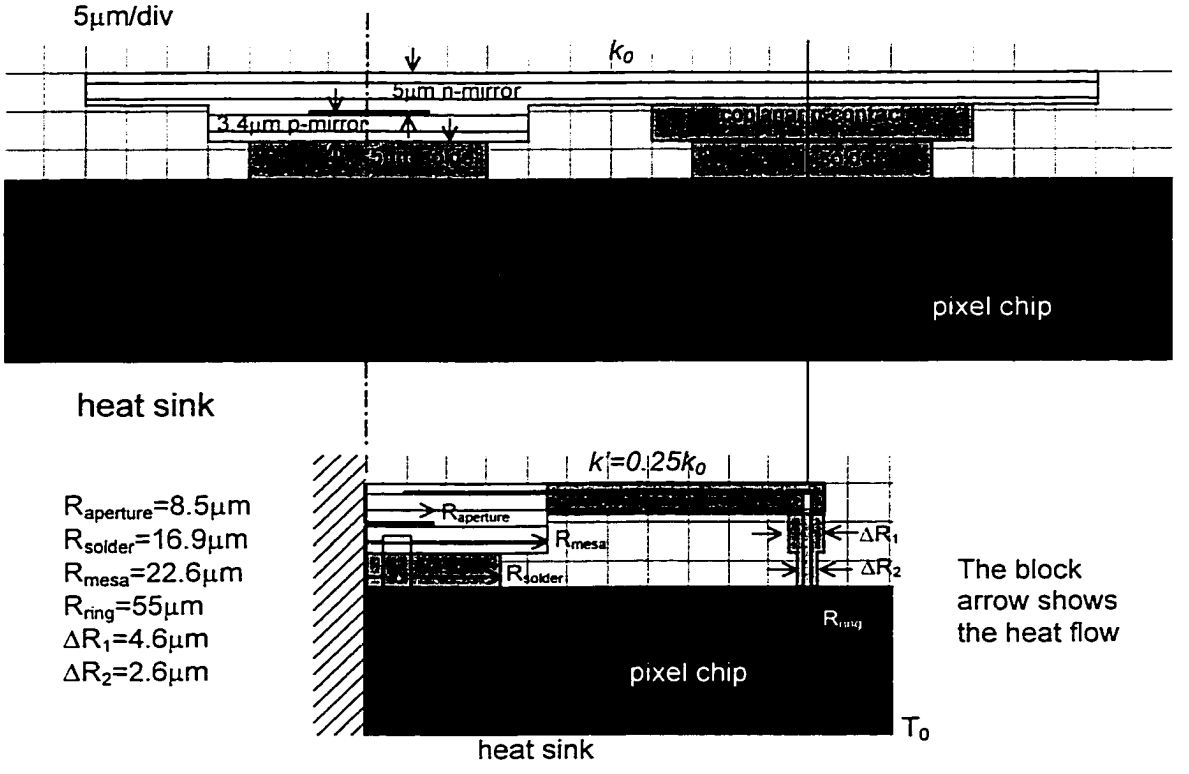


Figure 4.13 Cross section of the coplanar flip chip bonded VCSEL, the real structure (upper) and the model (lower)

When the heat flow is in the vertical direction, the heat is going through a planar wall. According to equation (4.3), the area of the cross section should be the same in both the real structure and the model, in order to obtain the same thermal resistance.

The axis of the cylindrical coordinator was selected at the center of the VCSEL device mesa. The 40x40μm^2 VCSEL mesa area is equal to a circle with radius R_{mesa} = 2.6μm, and so on.

The coplanar n-contact was described as a ring surrounding the VCSEL mesa. The average distance between the VCSEL mesa and the coplanar n-contact is 55μm in the real structure. Therefore, the radius of the ring R_{ring} is 55μm. The thickness of the ring $\Delta R_1.\Delta R_2$ is 4.6μm and 2.6μm for the 40x40μm^2 coplanar n-contact and the 30x30μm^2 solder respectively.

Since the shape of the bonded VCSEL in the cylindrical coordinator has already been determined by the vertical heat flow, equivalent thermal conductivity was used to balance the transverse heat flow.

In the real VCSEL structure, the heat passes through a planar wall in the transverse direction. According to equation (4.3), the average thermal resistance between these two solder bonds in the transverse direction is

$$R_{th} = L/kA = (55\mu m)/[k_0 L_{thick} (70\mu m)] \quad (4.5)$$

In the model, the heat is going through a cylindrical wall in the transverse direction. According to equation (4.4), the transverse thermal resistance of the model is

$$R_{th} = \ln(R_{mesa}/R_{aperture})/2\pi L_{thcik}k_0 + \ln(R_{ring}/R_{mesa})/2\pi L_{thick}k'$$

$$= \ln(22.6/8.5)/ 2\pi L_{thick}k_0 + \ln(55/22.6)/2\pi L_{thick}k' \quad (4.6)$$

To make equation 4.5 and 4.6 equal, the equivalent thermal conductivity k' is used for the material between the VCSEL mesa and the coplanar contact ring. The value of k' is 0.25 times that of its original thermal conductivity k_0.

4.2.2 Thermal transfer model of a top-bottom bonded VCSEL

The thermal transfer in a top-bottom bonded VCSEL is similar to that in a coplanar flip chip bonded VCSEL, except that the gold trace rather than the n-mirror connects the

VCSEL mesa to the other bonding pad on the pixel chip. The thermal transfer model is shown in figure 4.14.

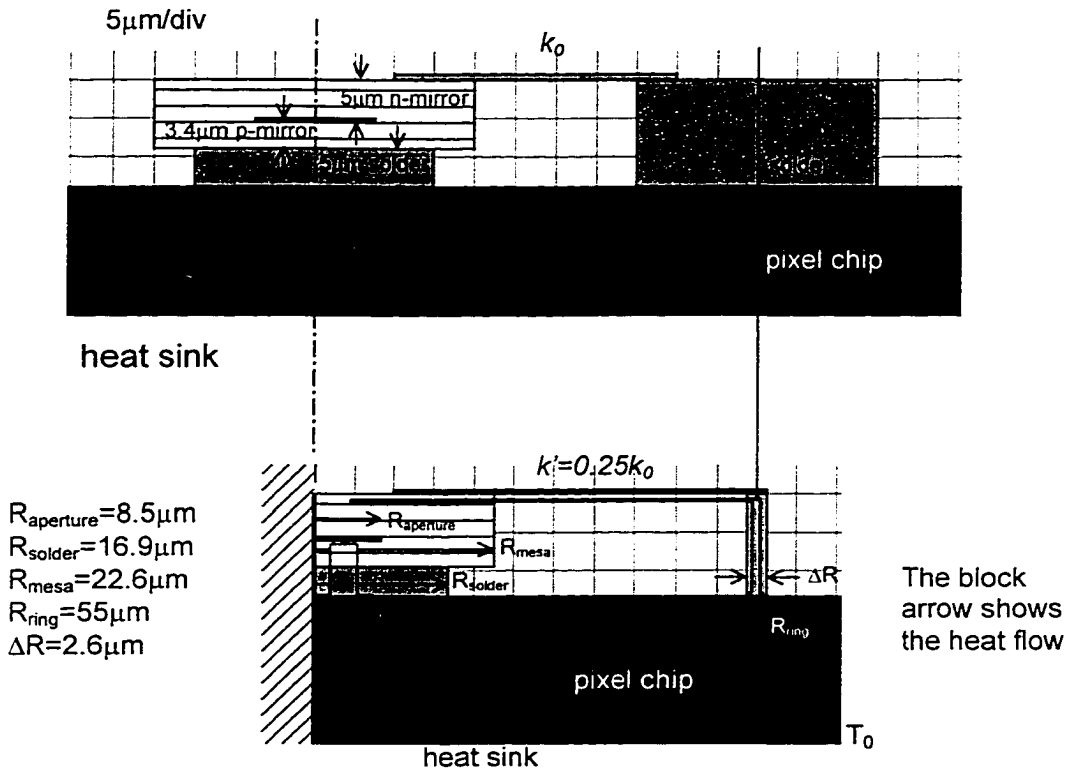


Figure 4.14 Cross section of the top-bottom contact bonded VCSEL, the real structure (upper) and the model (lower)

4.2.3 Thermal transfer model of a top-contact bonded VCSEL

A similar strategy has been used to simplify the top-contact bonded VCSEL (figure 4.15). The VCSEL mesa part is the same as the coplanar flip chip bonded VCSEL. The step coverage polyimide was ignored, since it is not a good thermal conductor. The most difficult part is how to simulate the top gold traces which connect the VCSEL contacts to the bonding pads on the pixel chip.

The thermal transfer model was first constructed without the gold traces. The simulation results show that the temperature at the top of the VCSEL mesa is higher than

that at the side of the VCSEL mesa. Therefore, only one gold trace was included in the model, i.e. the one on top of the VCSEL mesa. This gold trace contributes more to the heat transfer than the other one.

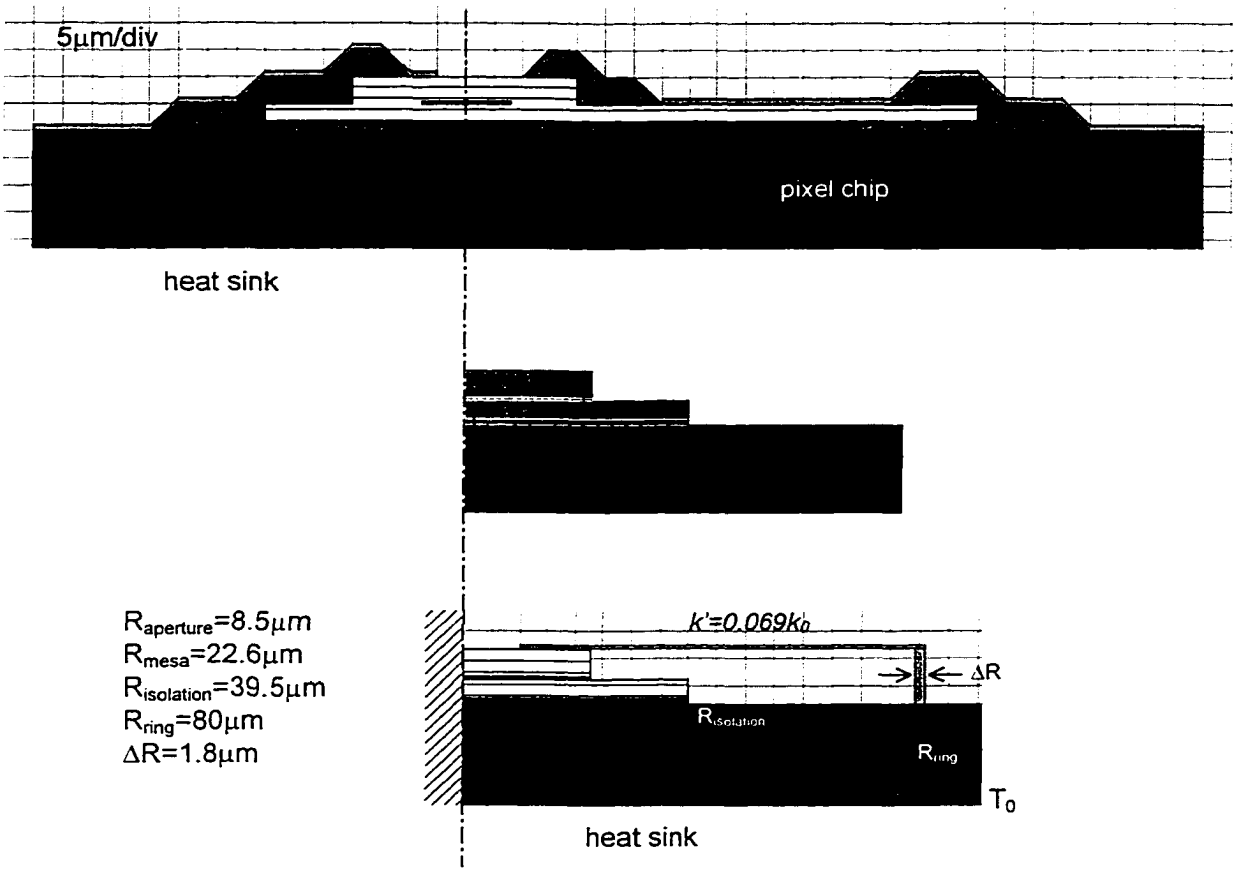


Figure 4.15 Cross section of the top contact bonded VCSEL, the real structure (upper) and the model (lower)

4.3. Simulation results

The static thermal transfer was simulated with the finite element analysis software FEHT using the models discussed above. The thermal conductivity of the materials used in this model are listed in Table 4.4. These values differ from the bulk material thermal conductivity, since experimental results have shown that the conductivity of the DBR mirror is lower than the thermal conductivity of the same average composition [14].

Because the layers of the DBR mirrors are only a few hundred nm thick, interface scattering contributes a large portion of the thermal transfer mechanism. The thermal conductivity of the polyimide and epoxy are the same. Although we only use the polyimide in the following simulation, the results will be same with the epoxy.

Table 4.4 thermal conductivity of the materials

Material	Thermal conductivity ($W K^{-1} m^{-1}$)	Reference
Au	315	[43]
$Al_{0.16}GaAs/Al_{0.92}GaAs$ mirror	25	[32]
GaAs	45	[43]
polyimide and epoxy	0.2	[44]
Si	141	[43]
SiO_2	1.02	[43]

During the measurements presented in the previous sections, the temperature of the VCSEL was controlled by a temperature controller through a thermoelectric cooler, which maintained the bottom of the substrate at a constant temperature. The same condition was used in the simulation. Heat generated in the active region of the simulation model and the temperature distribution in the VCSEL and the substrate were calculated. Using these data, the thermal resistance could be calculated using eq. 4.1.

4.3.1 Thermal resistance versus aperture size

Since the aperture size of the oxide confined VCSEL is hard to controll precisely, the thermal resistance of the VCSELs bonded to GaAs substrate verse aperture size was calculated, as show in figure 4.16. The calculations were made with a solder size of 30μm. The thickness of the polyimide in top-contact bonded VCSEL is 0.25μm. The measured thermal resistance of VCSELs bonded onto the GaAs substrate by the three techniques is also shown in figure 4.16.

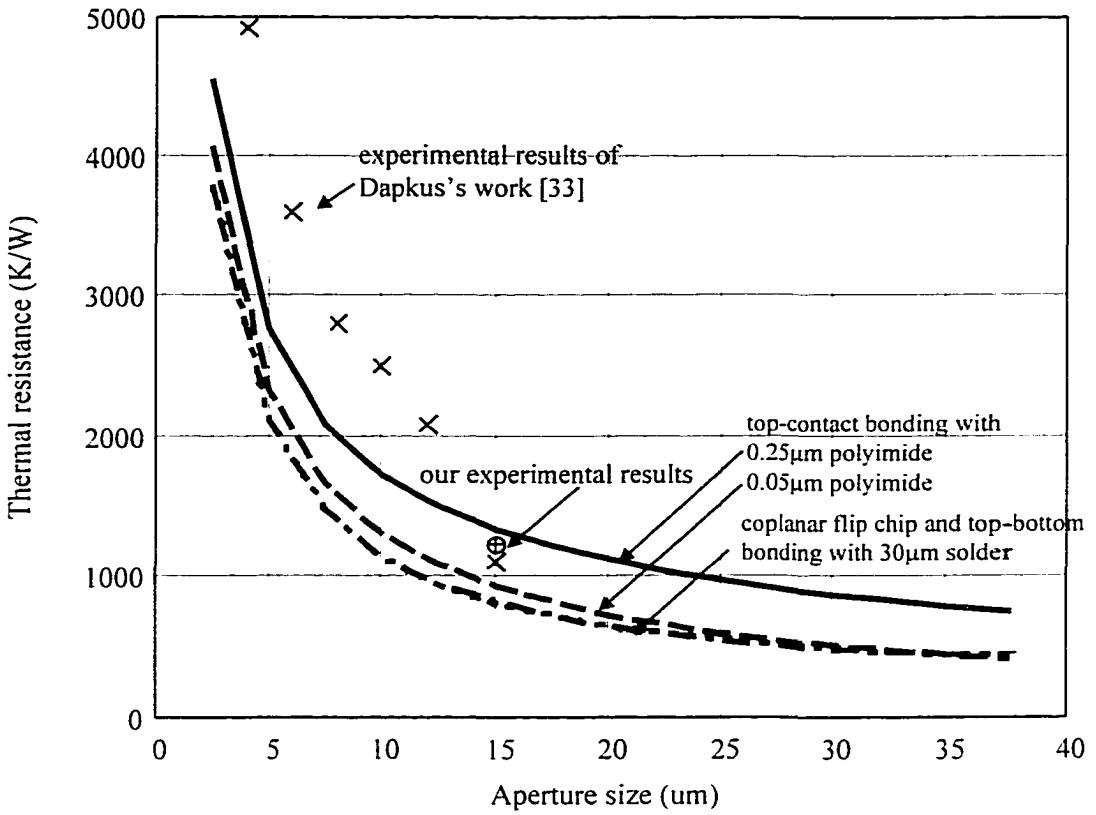


Figure 4.16 thermal resistance of bonded VCSEL versus aperture size

The simulation results show that the coplanar flip chip and top-contact bonded VCSELs have almost exactly the same thermal properties. This is because the Au post on the n-contact only contributes a small portion to the heat flow. The thermal resistance of the top-contact bonded VCSEL approach that of the other two techniques when the thickness of the polyimide is deduced to 0.05μm. The measured thermal resistance of the top-contact bonded VCSEL also shows similar values to that of the VCSELs bonded with the other two techniques.

The measured thermal resistance is in the same range of the simulation results. However, the measured thermal resistance of the coplanar flip chip and top-bottom

bonded VCSELs are higher than the simulation results. The reason may be due to value of the thermal conductivity of the VCSEL mirror we used in the simulation, since the VCSEL used in this research does not have exactly same composition as that in the reference.

Since the simulation results show little thermal resistance variation with the aperture size around 15μm (particularly for larger size), variation in the VCSEL fabrication will not result in signification thermal resistance variation and is probably not the cause of the difference in the measured and simulated results.

4.3.2 The limit of bonding density

Since the thermal properties of the bonded VCSELs with three techniques are similar, the simulation in this section is based on coplanar flip chip bonded VCSELs. In order to accomplish higher bonding density, smaller solder bonding pads size are desirable. Figure 4.17 shows the thermal resistance versus the solder size. When solder size is smaller than 10μm, the thermal resistance of the VCSEL increases very rapidly.

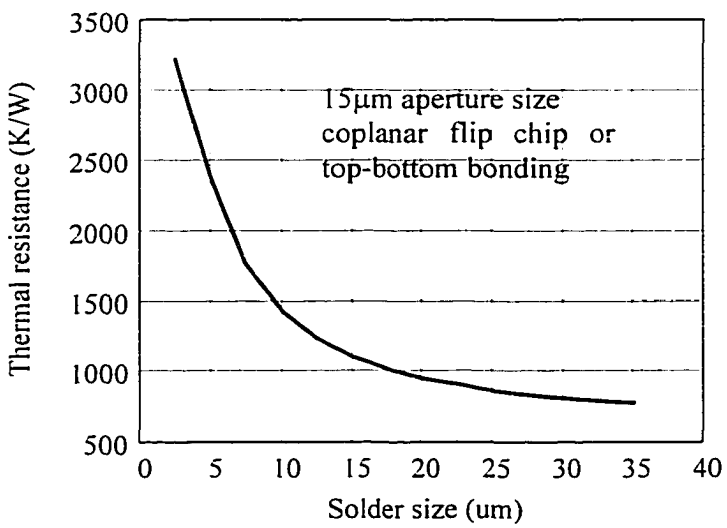


Figure 4.17 thermal resistance versus the solder size

The thermal crosstalk versus pitch was also calculated, as shown in figure 4.18. Considering the size of the oxide confined VCSEL, the pitch can not be smaller than 40μm. The thermal cross talk is already less than 100K/W, when the pitch is larger than 40μm according to the simulation. Therefore, the thermal cross talk is not a limit of the VCSEL array density.

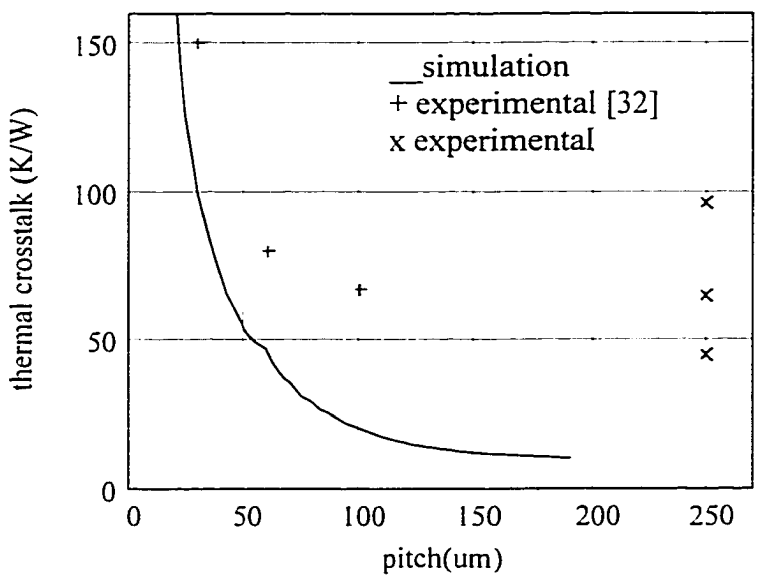


Figure 4.18 Thermal crosstalk versus the pitch of VCSEL array

4.3.3 Thermal resistance reduction with top-contact bonded VCSEL

When the VCSEL is bonded to a CMOS chip with the top-contact technique, the VCSEL is attached to the surface of the CMOS chip with polyimide or epoxy, since there is about 1μm thick passivation layer on the surface of the CMOS chip, the thermal resistance can not be reduced by reducing the thickness of the polyimide/epoxy.

However, the thermal resistance of top-contact bonded VCSELs can be reduced by increasing the thickness of the top gold trace. Figure 4.19 shows the thermal resistance versus the thickness of the gold trace. We assume that:

the polyimide layer is so thin that it can be ignored,

the passivation layer is 1μm,

the aperture of the VCSEL is 15μm.

The simulation indicates that the thermal resistance can be reduced 30% by increasing the thickness of the gold traces from 0.5 to 5μm. The thermal resistance can be further reduced by increasing the width of the gold traces.

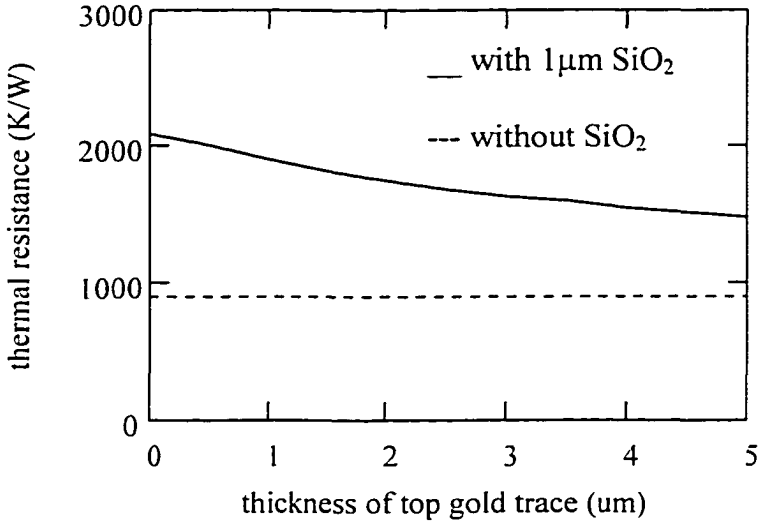


Figure 4.19 Thermal resistance versus the thickness of the top gold trace in top-contact bonded VCSELs

4.3.4 VCSELs on CMOS

The thermal resistance of the VCSEL coplanar flip chip bonded to a CMOS chip was also calculated with the same parameters as the fabricated device, e.g., 15μm aperture and 30μm solder. The dielectric layer underneath the bonding pads (refer to chapter 3),

increases the thermal resistance to as high as 2150K/W. This compares favorably with the measured thermal resistance of 2450K/W.

In order to reduce the thermal resistance, as many vias can be placed underneath the bonding pads as the design rules allow. In the best case, which means there is enough room on metal layer two and one, the thermal resistance can be reduced by about 1000K/W to 1165K/W.

4.4 Summary

The thermal resistance of the VCSEL bonded to GaAs substrate has been measured. The values are compatible to the standard VCSELs. Therefore, these three bonding techniques do not introduce significant thermal resistance if the process is properly done.

The thermal resistance of the VCSEL coplanar flip chip bonded to GaAs substrate, GaAs MESFET and Si CMOS have also been measured. The CMOS chip adds additional thermal resistance due to the SiO_2 layer, but it can be reduced by a special bonding pad design.

The measurements and simulation show little thermal crosstalk with the 250μm pitch of the VCSEL array. The simulation also shows that the thermal crosstalk does not limit the density of the array.

A two-dimensional cylindrically symmetric model was constructed for the simulation which provides the following:

1) similar thermal properties for the coplanar flip chip and top-bottom bonded VCSELs, and the top-contact bonded VCSELs when the polyimide layer between the VCSEL and the pixel chip is thinner than 0.05μm,

2) when the aperture size is approximately 15 μm, a small variation of the aperture size will not effect the thermal resistance significantly,
3) thermal resistance will limit the solder size, since the thermal resistance increases very fast when the solder size is smaller than 10μm,
4) the thermal resistance of the top-contact bonded VCSEL can be reduced by increasing the thickness of the top gold trace, when the VCSEL array is bonded to a CMOS chip.

CHAPTER 5

COMPARISON OF TECHNIQUES FOR FABRICATING VCSEL BASED SMART PIXELS

An ideal hybrid integration technique should have the ability to be scaled to large size with high yield and low cost. In addition, the integration induced parasitics should be minimized and the high quality performance of the discrete devices should be maintained after integration.

This dissertation research has developed three hybrid integration techniques for the fabrication of VCSEL-based smart pixels. Since the VCSELs are attached directly on top of the pixel chip in all three techniques, the distance between the VCSEL contacts and the bonding pads of the pixel chip is very short. Thus, very small parasitics can be expected and measurements have shown that all three techniques maintain the high quality of the VCSELs. However, techniques differ in other respects and this chapter provides a comparison of the three techniques, based on the processing and the electrical, optical and thermal characteristics of the bonded VCSELs.

5.1. Comparison of the processing

Generally, the number of mask levels is taken as a measure of the complexity and yield of a process. In addition, there are critical processing steps which effect bonding yield.

The coplanar flip chip technique requires the most mask levels and had the lowest yield as shown in Table 5.1. However, the coplanar flip chip bonding technique fully processes the VCSEL array before bonding and is therefore the most compatible technique with foundry fabrication. This advantage makes it the most promising technique of the three.

Table 5.1 Comparison of three VCSEL bonding techniques

Structure	Coplanar flip chip	Top-bottom contact	Top-contact
Number of mask levels	7	5	5
Yield	30%	40%	40%
Compatibility	excellent	good	fair

All of the bonding techniques require many processing steps. However, the majority of the processing steps are routine, e.g., rinsing, plasma ashing, dry etching, metal deposition, etc. These are common to all three of the techniques and do not provide a basis for differentiating the difficulty and/or scalability of the processes. The more critical processing steps and processing characteristics are listed in Table 5.2.

Although these critical steps were chosen based on our experience using our equipment and processing facilities, most of the processing steps are independent of the equipment. An exception is the initial attachment and the solder bonding. Since we use a mask aligner to align and perform the initial attachment, the tilt between the VCSEL array and pixel chip can not be adjusted. This prevents contacting all of the devices of the

array. In contrast, a solder bonding machine can adjust the tile between these two chips. Therefore, the accuracy of parallelization will not a problem for an industrial production line.

Normally, the yield of solder bonding step performed in our laboratory is about 50%, depending on the degree of tilt. Tilt was determined to be the main cause of reduced yield since the non-lasing VCSELs were not randomly located but occurred on one side of the die. In addition, there were a few random non-functional VCSELs due to other processing steps.

Table 5.2 Comparison of the important processing steps for the three VCSEL bonding techniques

Structure	Coplanar flip chip	Top-bottom contact	Top-contact
required accuracy of attachment parallelization	critical yield 50%	critical yield 50%	not as critical
Height tolerance of electroplated Au	0.3 μm	1 μm	N/A
Metal step coverage	N/A	not as critical yield 90%	critical yield 50%
critical photolithography	many mask levels yield 80%	metal aperture yield 90%	metal aperture yield 90%
Number of mask levels	7	5	5
Sequence of metal deposition	after oxidation yield 80%	before oxidation	before oxidation
Sequence of attachment	after oxidation	after oxidation	before oxidation yield 90%

5.1.1. Coplanar flip chip bonding

The difficult processing steps that may limit the yield of the smart pixel arrays are different for each of the three techniques. For coplanar flip chip bonding, besides the low solder bonding yield due to tilt, the difficulties include:

1) Many processing steps carried out on a non-planar surface topography. Although the other two techniques also require processing steps carried out on a non-planar surface topography, the number of the mask levels are less than with coplanar flip chip bonding. This results in 80% yield.

2) Unstable metal-semiconductor contacts. The present VCSEL wafer does not have an intra-cavity contact layer for the metal contact. The metal contact is deposited on the n-mirror layers. The composition of Al in the mirror layers is very easily oxidized and the oxide is hard to remove. Therefore, unstable metal-semiconductor contact results in that some of the contacts fall off after electroplating. The yield is about 80%. This problem can be corrected by adding the contact layers..

3) The coplanar flip chip bonding technique requires electroplating the n-mirror contact to the same level as the p-mirror contact. Although the required accuracy is within 0.3μm, this can be obtained by careful control.

5.1.2. Top-bottom contact bonding

The solder bonding yield due to tilt is the most significant limit on the total yield with the top-bottom bonding technique, but this can be overcome by using a solder bonding machine. The other problem associated with top-bottom bonding technique are:

1) A deposit metal aperture is required. This is the smallest feature among the bonding structures and since this step occurs after bonding and substrate removal, the surface is a combination of VCSEL mesas, Au posts and epoxy. Tilt also adds to the problem. Furthermore, the die is small, thus it is hard to perform edge photoresist removal, as mentioned in Chapter 3. The non-planar surface makes the contact between the surface and the mask poor. Thus, the patterned metal aperture is smaller than the mask. In our

fabrication, a few of the metal apertures could not even be lifted off, which left about 90% yield after this processing step.

2) The epoxy serves as a bed upon which the contact metal sets up a bridge between the Au post and the VCSEL mesa. However, the oxygen plasma etching of the remaining epoxy is not uniform as shown in Figure 5.1. The yield of this processing step is about 90%.

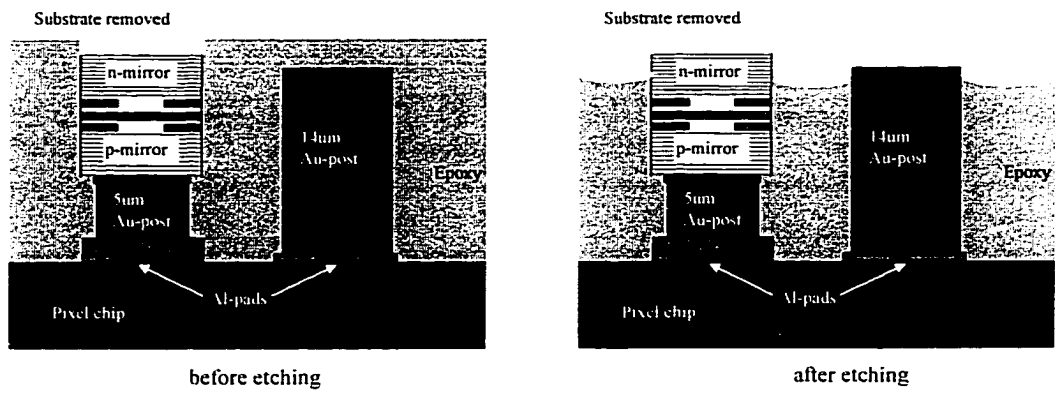


Figure 5.1 Epoxy etch with top-bottom bonding technique

5.1.3. Top-top contact bonding

Top-top contact bonding is different from the other two bonding techniques, since it does not require solder bonding, thus no problem with tilt. The problem steps are:

1) The most critical processing step is patterning the insulation layer for the step coverage of the metal traces for the n-mirror contact. Polyimide was chosen to serve as the insulation layer, since a few micrometer thick layer can be obtained with polyimide. The thicker layer not only provides better insulation, but also reduces the parasitic capacitance. In addition, polyimide forms 45° side-wall after patterning, which makes the following metal step coverage easier. However, patterning the polyimide on a non-planar surface topography is difficult since the polyimide tends to smooth the non-planar

surface. Therefore, the thickness of the polyimide is not uniform and the etching of the polyimide is not uniform either. The over etched polyimide layer can not provide a good insulation layer for the following metal step coverage, as shown in Figure 5.2. The yield of the step is only 50%. A better polyimide and process condition might be found with more experience. This problem can also be solved by depositing SiO_2 instead of polyimide. Although deposited SiO_2 layer normally is thin, the parasitic capacitance can be further reduced by proton implanting the VCSEL mesa [22].

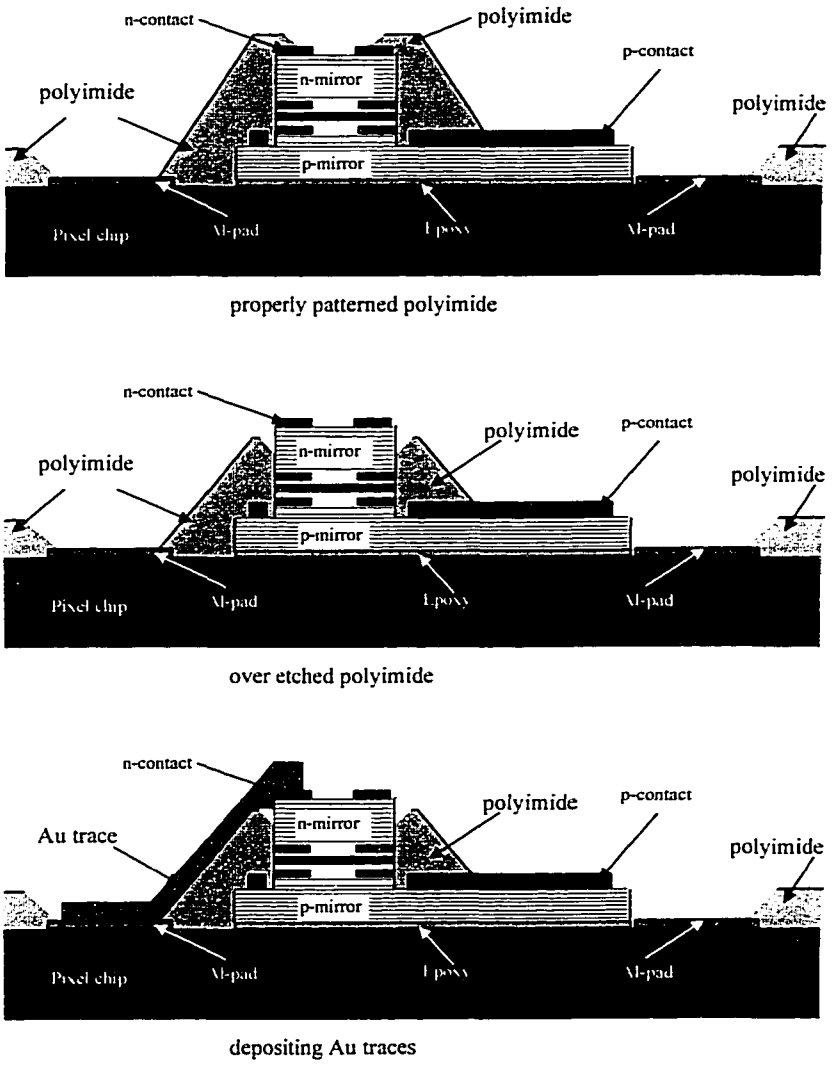


Figure 5.2 Insulate layer for top-top contact bonding technique

2) The top-contact technique requires attaching the VCSEL wafer to the pixel chip with a nonconductive adhesive such as epoxy or polyimide. After removal of the VCSEL wafer substrate and the formation of the VCSEL mesa, the bonded VCSEL and pixel chip, must be exposed to steam at 430°C for 25 min. As a result the bonding pads are also oxidized, since the very thin nonconductive adhesive layer does not provide sufficient protection. The oxide on the surface of the bonding pad effects the resistance and yield of the subsequent metal contacts. Therefore, a better protection before the oxidation or treatment after the oxidation needs to be designed to overcome this problem.

3) Top-contact bonding technique also requires depositing a metal aperture on a non-planar surface topology. This processing step has the same yield ~90% as the similar processing step in top-bottom bonding technique.

Most of the limits on the fabrication yield can be overcome by using suitable equipment or optimized design. Therefore, much better yield can be expected from a commercial fabrication facility. Although our fabrication was based on small scale fabrication, such as 4x4 and 8x8 arrays, there are no obviously limits of the bonding techniques going to large scale.

5.2. Comparison of electrical and optical characteristics

All three bonding techniques resulted in working VCSEL's with reasonable electrical and optical characteristics. This indicates that all of these techniques are possible candidates for large-scale hybrid integration of VCSEL's. In an attempt to obtain a more meaningful comparison of the bonding technique, the characteristics listed in Table 5.3

are measured from the bonded VCSELs fabricated from the same VCSEL wafer, EMC1148, and with similar aperture size.

Among electrical characteristics, the series resistance and threshold voltage depend on:

1) the metal-semiconductor contacts of the p- and n-contacts of the VCSEL,

2) the series resistance of the p- and n-mirror of the VCSEL,

3) the bonding metal contacts.

Since there are no intra-cavity contact layers in the VCSEL wafer for the semiconductor-metal contacts, the changing of the series resistance and threshold voltage VCSELs from run to run reflects the quality of the semiconductor-metal contact rather than the bonding contact.

The VCSEL bonded with top-contact technique has the highest series resistance and threshold voltage among the three bonding structures, because its p-contact may be on the AlGaAs layer of the p-mirror as well as its n-contact could be on the AlAs etch stop layer after substrate removal. The coplanar flip chip bond VCSEL has smaller series and threshold voltage resistance than the top-contact bonded VCSEL, because it only has n-contact on the n-mirror. The top-bottom bonded VCSEL has the smallest series resistance and threshold voltage among the three bonding structures, since it does not require intra-cavity contacts for either the n- or p- mirror.

As we mentioned in Chapter 3, the threshold current of the bonded VCSEL depends on the mirror reflectivity and each of the bonding techniques results in different mirror reflectivity. According to the calculation, the coplanar flip chip and top-bottom contact bonded VCSELs should have much lower threshold than the top-contact bonded VCSEL.

The measured results showed a larger threshold current of the top-contact bonded VCSEL, although it is not as small as the calculation predicted. The reason could be that, when the reflectivity of the mirror is getting very small, the mirror and cavity loss can not be ignored.

The optical output power of the VCSELs we bonded is low, because the VCSEL wafer we used, EMC1148, is not design for back emitting. Its n-mirror has many DBR pairs (39), which results in very high reflectivity and less optical output power.

The top-bottom and top-contact bonded VCSELs have even smaller optical output power, because the metal aperture blocked part of the optical output. The difficulty of processing the metal aperture has been discussed in last section.

Table 5.3 also listed published values for bonded VCSELs from other research groups, data from a package Honeywell commercial product and VCSELs from standard VCSEL arrays. These parameters for our VCSELs are in the same range as reported for bonded VCSELs by other groups.

It is also observed that the series resistance of all of the flip chip bonded VCSELs shown in the table are higher (50-200Ω) than the standard/commercial VCSELs (20-32Ω) and the threshold voltage of the bonded VCSELs is also usually higher. There are several possible causes for the higher values for the bonded VCSELs

1) the VCSEL wafers for flip chip bonding were not designed properly to reduce the contact/mirror resistance,
2) the ohmic contacts were not annealed properly,
3) the contact metallurgy is introducing a voltage drop/resistance due to the oxidation of one or more of the metal layers,

4) the bonding metals are introducing a junction.

This is an area of research of all types for flip chip bonding of VCSELs.

Table 5.3 Comparison of the electrical and optical characteristics of the three bonding techniques with those of other researchers

Group		Resistance (Ω)	Threshold current (mA)	Threshold voltage (V)	Aperture (μm)	Optical output power (mW)
presented works	1632 coplanar	90	3.8	2.1	14	3.0
	1584 top-bottom	60	0.8	1.5	6	0.07
	1148 coplanar	100	2.0	2.8	~15	0.25
	1148 top-bottom	70	2.0	2.5-3.1	~15	0.04
	1148 top-contact	120	2.5	3.5-4.5	~15	0.03
Kishnamoorthy[23] Lucent		150	0.9-1.0	1.4-1.5	N/A	5.0
Matsuo[45] NTT		70	3.5	2.3	15	1.2
Maracas[14] Arizona State		90	5.5-6.4	3.0	40	1.0
McLaren[46] Univerity of Colorado		200	1.5	1.9		>0.4
Smith[28] UC Berkeley		70	30	17.0	40	0.03
Morgan[47] Honeywell (proton-implanted)		29	2.7	1.55		8.0
Choquette[48] Sandia (oxide-confined)		32	4.0	2.0	14	5.0
Honeywell product HFE 4080-321		20	3.8	1.5		5.0

5.3. Comparison of the thermal properties of the VCSEL-based smart pixel

Since the VCSELs are bonded as individual device, the heat generated by each VCSEL must by removed through the attachment to the substrate. Therefore, the thermal properties of the bonded VCSEL indicate the quality of the bonding.

The thermal transfer model of Chapter 4 shows that coplanar flip chip and top-bottom bonding techniques have similar thermal properties. With both bonding techniques, the VCSELs are attached to the bonding pads on the pixel chip with an Au post Therefore, the limits of the thermal properties of the bonded VCSEL include,

1) the size of the Au post,

2) the quality of the solder bonding,

3) the thermal property of the bonding pads on the pixel chip.

According to the simulation, when the size of the Au post is <10μm, the thermal resistance of the bonded VCSEL increases rapidly. The experimental results demonstrate that when the bonding is not properly done, the thermal resistance can be as high as 2250K/W, while the thermal resistance of a properly bonded VCSEL is only 1100K/W.

The material underneath the bonding pads on the pixel chip also influences the thermal resistance of the bonded VCSEL, e.g., when the VCSEL was bonded to a CMOS chip. In a standard CMOS bonding pad design, there are three dielectric layers underneath the bonding pads. This causes the thermal resistance of the VCSEL bonded to a CMOS chip increased to 2450K/W. On the other hand, the thermal resistance of a VCSEL bonded to a GaAs substrate is only 1100K/W. The thermal resistance of the VCSEL bonded to a CMOS chip can be reduced by putting many Al vias underneath the bonding pads.

With top-contact bonding technique, the VCSELs are attached to the surface of the pixel chip with non-conductive adhesive, such as epoxy and polyimide. The electrical connection between the VCSEL and the pixel is provided by the gold traces on the top of the VCSEL. Therefore, the limits of the thermal properties of the top-contact bonded VCSEL include,

1) the thickness of the non-conductive adhesive layer,

2) the uniformity of the non-conductive adhesive layer,

3) the thickness of the passivation layer on the surface of the pixel chip,

4) the thickness of the top gold traces.

In order to obtain low thermal resistance, the thickness of the non-conductive adhesive layer should be as thin as possible. Very thin layer can be obtained with epoxy, because of its very low viscosity. The measured thermal resistance of the VCSEL bonded with epoxy, which is 1250K/W, is close to the thermal resistance of the VCSEL bonded with the other two techniques. Thus, the epoxy layer does not significantly increase the thermal resistance. However, non-uniformity of the epoxy or polyimide layer will effect the uniformity of the thermal resistance of the bonded VCSEL, especially when the layer becomes thick.

Although we did not bond the VCSEL array to a foundry fabricated microelectronic chip with top-top contact technique, there is a problem that we can predict. When the VCSEL is attached on the surface of the microelectronic chip, either on a CMOS or a MESFET chip, the surface has a passivation layer, which is not a good thermal conductor. This will increase the thermal resistance. If we open a window in the passivation layer underneath the VCSEL, the window will be filled up with the epoxy or polyimide when it is applied. Therefore, this problem can not be avoided in this method.

When the heat path underneath the VCSEL is blocked by the passivation layer, the gold traces on the top of the VCSEL, which connect the VCSEL to the bonding pads on the microelectronic chip, become important. The thermal resistance can be reduced by increasing the thickness of the gold traces, but the reduces the thermal resistance by only 20~40%.

CHAPTER 6

CONCLUSIONS AND SUGGESTOINS FOR FUTURE WORK

This chapter summarizes the achievements of the research work of this dissertation. The conclusions and suggestions for the future work are given based on these achievements

6.1 Accomplishments

The goal of this dissertation research is to develop reliable techniques to fabricate large-scale VCSEL-based smart pixel arrays for application to parallel optoelectronic processing. The accomplishments include:

1) Three different hybrid integration techniques for bonding VCSEL arrays have been developed.
2) First to successfully bond VCSEL arrays to foundry fabricated microelectronic chips,
3) 4x4 and/or 8x8 VCSEL arrays were successfully bonded to GaAs dummy chips, GaAs MESFET and/or Si CMOS chips with these techniques, although the yield is still low.
4) The critical processing steps, which effect the bonding yield, were determined.

5) The electrical, optical and thermal characteristics of the bonded VCSELs have been measured. The threshold voltage of the bonded VCSEL as low as 1.5V and the series resistance down to 60Ω was measured. Optical power of 3mW for a VCSEL with a 14μm oxide-confined aperture was also observed. The thermal resistance of the VCSELs bonded to a GaAs substrate is as low as 1100K/W. The thermal crosstalk is less than 100K/W

6) The functionality of the smart pixels with the bonded VCSEL arrays was also demonstrated. The CMOS transmitter chip with bonded VCSELs was operated at 200Mb/s (our equipment limit) with rise and fall times of the optical output <1nS.

7) A two-dimensional thermal transfer model was constructed to analyze the heat transfer of the bonded VCSELs. The simulation shows a rapid increasing of thermal resistance when the size of the solder bonding pads is less than 10μm. The simulation also predicts that the thermal resistance of the VCSEL bonded to a CMOS chip could be reduced by adding vias through the dielectric layers of the CMOS chip or increasing the thickness of the top gold traces

6.2 Conclusions

1) Bonding VCSELs to CMOS & MESFET circuits is viable. The proper functioning of the smart pixel with the bonded VCSEL array verifies that the bonding process can maintain the high quality of not only the VCSEL, but also the foundry fabricated microelectronic integrated circuit chip, such as GaAs MESFET and Si CMOS chips.

2) While the bonding yield is low for the present research, the yield can be improved significantly by using commercial facilities and optimizing the processing. Solder

bonding is the major limit of the yield of the coplanar flip chip and top-bottom bonded VCSEL array. Since we used a mask aligner to carry out the solder bonding, much higher bonding yield can be expected with a suitable solder bonding machine. Step coverage is the main problem with top-contact bonding. It can be overcome by optimizing the processing of polyimide.

3) The bonding processes do not significantly degrade the quality of the VCSELs.
4) The measured thermal resistance of the VCSELs bonded to GaAs substrates is also comparable with unbonded VCSELs.
5) Partially attached bonding can provide good electrical connection but not thermal conduction, thus, the thermal properties of the bonded VCSELs can reflect the quality of the bonding better than electric characteristics.
6) The measured thermal crosstalk is not as low as expected for the pitch of 250μm, but is the same range as with 100μm pitch. Therefore, the thermal crosstalk will not limit the density of the array down to a pitch of 100μm.
7) The measured series resistance and threshold voltage of the bonded VCSELs are comparable with previously reported bonding results but higher than that for unbonded VCSELs. The series resistance should be reduced by adding an intra-cavity contact layer into the VCSEL wafer for the metal contact.
8) The thermal transfer simulation results show that the size of the bonding pads may be determined more by the need to heat sink the VCSELs than other factors.
9) The simulations indicate methods to reduce the thermal resistance of VCSELs bonded to a CMOS chip.

10) Although the bonding qualities need further investigation to lead these techniques into practice, the techniques have the potential to make large optoelectronic arrays and maintain the high quality of the VCSELs.

6.3 Suggestions for future work

1) Investigate the effects of intra-cavity contact layers.
2) Investigate the bonding metallurgy.
3) Additional fabrication runs should be investigated optimizing the process and improving the bonding yield.
4) Although the parasitic capacitance of the attachment bonding is small, when the speed of smart pixels increases to >1Gb/s, the measurement of the exact value of the parasitic capacitance will be helpful for the circuit design.
5) Although the two-dimensional model has given good results, a three-dimensional thermal transfer model should be investigated.

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APPENDIX A

PROCESSING STEPS

1.Coplanar flip chip bonding technique

1.1 Process on the VCSEL wafer

p-contact

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	p-contact mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
Oxygen plasma	2min	50W	
oxide etch	1min		buffered HF
evaporation	Ti/Pt/Au	200A/200A/2000A	
lift-off			air-brush

Device etch

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	device etch mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
RIE	till n-mirror(~4um)		
rinse photoresist with air brush (or plasma etch PR)			
measure mesa			α-step

n-contact electroplating

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	p-contact mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
oxide etch	1min		buffered HF
evaporation	Ge/Pt/Ni/Au	250A/520A/150A/1500A	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	1min	95C	look at it during baking, no bubble
expose	30s	15mJ/cm2	bonding mask (transparent)
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
post-bake	1min	95C	look at it during baking, no bubble
measure the thickness of PR			α-step
electroplate	as necessary (~5um/12min)	4.5mA	We prefer gold pats are higher than the mesa, within .5um
rinse PR			
lift off Au			
measure gold pads			α-step

Anneal	45s	370°C	

Oxidize *430°C(set 360), water~75°C(set at 6), flue~60*

test oxide rate when using different wafer (rate might be different in the middle from the edge)

measure oxidized region with IR source on the mask aligner

EMC1632	27min	aperture~7um with 40um mesa	

Isolation etch

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
double spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	
expose	45s	20mJ/cm2	Isolation mask
develop	as necessary (~50s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
wet etch	till the ring disappear	5°C	H_2SO_4:H_2O_2:H_2O

Electroplate 10μm Au on bonth p- and n-contact

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	

expose	30s	15mJ/cm2	In lift mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	3min	95°C	
hard bake	2min	120°C	
plasma etch	2min		50W
evaporation	Ti/Au	400A/800A/	
double spine PR	30s	5000rpm	AZ4620
post-bake	1min	95°C	look at it during baking, no bubble
expose	45s	15mJ/cm2	bonding mask (transparent)
develop	as necessary (~45s)		1 Hoechst-Celanese AZ400K:3DI
post-bake	1min	95°C	look at it during baking, no bubble
measure the thickness of PR			α-step
electroplate	as necessary (15min~10um)	4.5mA	
rinse PR			
lift off Au			
measure gold pads			α-step
scribe the letters			

Polishing	till the sub is shining(1mil=2000um)	low percentage Br
Cleave	to arrays	

1.2.Pixel preparation

Evaporation			
rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
double spine photoresist(PR)	30s	5000rpm	AZ4620
post-bake	2min	95°C	
expose	30s	15mJ/cm2	bonding mask(no letters)
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
oxide etch	5s		HCl1:DI 5
evaporation	Ti/Au/InSn	400A/1000A/6000A	
lift-off			air-brush

1.3.Flip Chip Solder(InSn) Bonding

1. crystal bond the chip on a piece of mask glass, use higher temperature to reduce the viscosity of crystal. Making the bonding very uniform is very important.
2. put the VCSEL array on the IR stage, align the VCSEL array with the chip with IR source
3. raise the holder till the two chips stuck together

4. remove the bonded chips from the stage, heat to 200°C for 15min in 15%H2, to let InSn melt with bonding pads
5. drop epoxy at the edge of the bonded chip with fiber. (Don't tough it. Don't use sweeper clean it.), heat to 100°C to reduce the viscosity of the crystal
6. thermal cure for 15min at 125°C.
7. use crystal cover the edge of the bonded chip
8. polish the sample as thin as possible
9. selective spray etch ($NH_4OH:H_2O_2$=8ml:250ml), till all sub is gone
10. etch the AlAs layer with buffered HF
11. oxygen plasma etch for a few hours at 100W to remove the epoxy
12. test

2.Top-bottom contact bonding technique

2.1 Process on the VCSEL wafer

Electroplate 5μm Au on p-contact

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	In lift mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	3min	95°C	
hard bake	2min	120°C	
plasma etch	2min		50W
evaporation	Ti/Au 400A/800A/		
double spine PR	30s	5000rpm	AZ4620
post-bake	1min	95°C	look at it during baking, no bubble
expose	45s	15mJ/cm2	bonding mask (transparent)
develop	as necessary (~45s)		1 Hoechst-Celanese AZ400K:3DI
post-bake	1min	95°C	look at it during baking, no bubble
measure the thickness of PR			α-step
electroplate	as necessary (15min~10um)	4.5mA	
rinse PR			
lift off Au			
measure gold pads			α-step

Device etch

RIE	till the substrate(~9um)	
measure mesa		α-step

Anneal	45s	370°C

Oxidize *430°C(set 360), water~75°C(set at 6), flue~60*

test oxide rate when using different wafer (rate might be different in the middle from the edge)

measure oxidized region with IR source on the mask aligner

EMC1632	27min	aperture~7um with 40um mesa

Polishing till the sub is shining(1mil=2000um) low percentage Br

Cleave to arrays

2.2.Pixel preparation

Evaporation on p-contact

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
double spine photoresist(PR)	30s	5000rpm	AZ4620
post-bake	2min	95°C	
expose	30s	15mJ/cm2	bonding mask(no letters)
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
oxide etch	5s		HCL1:DI 5
evaporation	Ti/Au/InSn	400A/1000A/6000A	
lift-off			air-brush

Electroplate ~14μm Au on n-contact

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	In lift mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	3min	95°C	
hard bake	2min	120°C	
plasma etch	2min		50W
evaporation	Ti/Au	400A/800A/	
double spine PR	30s	5000rpm	AZ4620
post-bake	1min	95°C	look at it during baking, no bubble
expose	45s	15mJ/cm2	bonding mask (transparent)
develop	as necessary (~45s)		1 Hoechst-Celanese AZ400K:3DI
post-bake	1min	95°C	look at it during baking, no bubble
measure the thickness of PR			α-step
electroplate	till 3um lower than the VCSEL		
rinse PR			
lift off Au			
measure gold posts			α-step

2.3.Flip Chip Solder(InSn)Bump Bonding

1. crystal bond the chip on a piece of mask glass, use higher temperature to reduce the viscosity of crystal. Making the bonding very uniform is very important.
2. put the VCSEL array on the IR stage, align the VCSEL array with the chip with IR source
3. raise the holder till the two chips stuck together
4. remove the bonded chips from the stage, heat to 200°C for 15min to let InSn melt with bonding pads
5. drop epoxy at the edge of the bonded chip with fiber. (Don't tough it. Don't use sweeper clean it.), heat to 100°C to reduce the viscosity of the crystal
6. thermal cure for 15min at 125°C.
7. use crystal cover the edge of the bonded chip
8. polish the sample as thin as possible
9. selective spray etch ($NH4OH:H_2O_2$=8ml:250ml), till all sub is gone
10. etch the AlAs layer with buffered HF
11. oxygen plasma etch the epoxy till no epoxy on top of the Au post on the pixel chip.

n-contact electroplating

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	p-contact mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
oxide etch	1min		buffered HF
evaporation	Ge/Au/Ni/Au	250A/520A/150A/1500A	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	1min	95°C	look at it during baking, no bubble
expose	30s	15mJ/cm2	bonding mask (transparent)
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
post-bake	1min	95°C	look at it during baking, no bubble
measure the thickness of PR			α-step
electroplate	as necessary (~5um/12min)	4.5mA	
rinse PR			
lift off Au			
measure gold traces			α-step

Anneal 45s 370°C

test

3.Top-top contact bonding technique

3.1 VCSEL wafer bonding

1) prepare the pixel chip

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
plasma etch	10min		
spine epoxy	30s	5000rpm	H81(Norland Products Inc.)

2) put VCSEL wafer face down to the pixel chip,
3) compress the bonded system with the mask aligner,
4) cure the epoxy at 150°C for 15min,
5) polish the sample as thin as possible
6) selective spray etch ($NH_4OH:H_2O_2$=8ml:250ml), till all sub is gone
7) etch the AlAs layer with buffered HF.

3.2 Fabricate the VCSEL

p-contact deposition

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	p-contact mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
Oxygen plasma	2min	50W	
oxide etch	1min		buffered HF
evaporation	Ti/Pt/Au	400A/200A/2000A	
lift-off			air-brush

Device etch

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	device etch mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
RIE	till n-mirror(~4um)		

rinse photoresist with air brush (or plasma etch PR)
measure mesa α-step

n-contact deposition

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	p-contact mask
develop	as necessary (~30s)	1 Hoechst-Celanese AZ400K:4DI	
soft bake	2min	95°C	
hard bake	2min	120°C	
oxide etch	1min		buffered HF
evaporation	Ge/Au/Ni/Au	250A/520A/150A/1500A	
lift off Au			

Isolation etch

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	
expose	45s	20mJ/cm2	Isolation mask
develop	as necessary (~20s)	1 Hoechst-Celanese AZ400K:4DI	
soft bake	2min	95°C	
hard bake	2min	120°C	
wet etch	as necessary	5°C	H_2O_2:H_2SO_4:H_2O

Anneal 45s 370°C

Oxidize *430°C(set 360), water~75°C(set at 6), flue~60*

test oxide rate when using different wafer (rate might be different in the middle from the edge)

measure oxidized region with IR source on the mask aligner

EMC1632 27min aperture~7um with 40um mesa

Polyimide

epoxy etch	Oxygen plasma		
rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine adhesive	30s	5000rpm	95mlMethanal:5DI wafter:0.1-1VM-651
spine polyimide	30s	5000rpm	PI-2555
soft cure	10min	120°C	
cool down the sample			
spine photoresist(PR)30s		5000rpm	AZ4400
post-bake	2min	95°C	
expose	45s	20mJ/cm2	Isolation mask
develop PR&poly	as necessary (~6min)	1 Hoechst-Celanese AZ400K:4DI	
rinse PR quickly	Acetone will attack uncured PI-2555		
hard cure PI-2555	1hr. ramp to 200°C, 4hr @200°C, 1hr ramp to room temperature		

Au-trace electroplating

rinse	Acetone, Methanol, DI water		
pre-bake	2min	120°C	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	2min	95°C	
expose	30s	15mJ/cm2	p-contact mask
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
soft bake	2min	95°C	
hard bake	2min	120°C	
oxide etch	1min		buffered HF
evaporation	Ti/Au	400A/1000A	
spine photoresist(PR)	30s	5000rpm	AZ4400
post-bake	1min	95°C	look at it during baking, no bubble
expose	30s	15mJ/cm2	bonding mask (transparent)
develop	as necessary (~30s)		1 Hoechst-Celanese AZ400K:4DI
post-bake	1min	95°C	look at it during baking, no bubble
measure the thickness of PR			α-step
electroplate	as necessary (~5um/12min)	4.5mA	
rinse PR			
lift off Au			
measure gold traces			α-step

test

APPENDIX B

THERMAL TRANSFER SOFTWARE FEHT

The model of the three VCSEL bonding structure is saved in FEHT file:

1) Coplanar flip chip Dudley\\user data (F:)\ray\feht\coplanar cy.fet

2) Top-bottom contact Dudley\\user data (F:)\ray\feht\top-bottom cy.fet

3) Top-top contact Dudley\\user data (F:)\ray\feht\topcontact cy.fet

About FEHT

FEHT is a friendly finite element analysis software with menu commands. The online help describes how to use this software. However, the software can only define volume heat generation and does not have powerful tools to make the drawing. Here are a few tips to help draw the structures:

1) Save your drawing without or with only a few elementary lines as a separate file. It is hard to delete elementary lines since you must select them one by one.
2) Be careful when you make any changing, you may screw up the whole drawing. When you draw an outline along the outline of the other object, if you do not finish it, the outline and the outline of the other object will be gone simultaneously.
3) If you need to draw an object inside another one, draw the outside object first.

4) If you need to change the size of an object, besides removing the nodes, you can also divide this object to several parts and define different material of these parts later.