THESIS

FAST ELECTRONIC DRIVER FOR OPTICAL SWITCHES

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ABSTRACT

FAST ELECTRONIC DRIVER FOR OPTICAL SWITCHES

Electronically controlled optical switches are critical components in many optical systems, including pulsed lasers. Solid-state optical switches based upon the Pockels effect are widely utilized in research and industry, however Pockels cells require electronic drivers capable of switching several kilovolts quickly and cleanly. This thesis reviews Pockels cell designs and their typical applications in laser systems, discusses common drive circuit topologies found in literature, and describes the development of a fast, stable electronic driver for half-wave configured Pockels cell optical switches.

In a crowded optical environment, it is frequently desirable to locate the Pockels cell at some distance from the driver electronics. The driver was developed to be capable of 1.4 ns optical transition times when connected to a 6 pF Pockels cell via 1.2 meters of 50 ohm coaxial cable. The driver is designed to operate in colliding-pulse mode at 6-8 kV, with 80 ampere typical switch currents. Total switch propagation delay is less than 100 ns, and thermal drift has been measured at less than $50ps/C^o$. These pulsers are currently used to drive Pockels cells in colliding pulse mode in pulse picking and slicing applications where optical rise times of < 2 ns and low drift are needed. Novel non-invasive diagnostic techniques for measuring and graphing pulse propagation in a repeatable manner along collapsing avalanche transistor chains are presented.

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-Mark R. Woolston

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Chapter 1

FUNDAMENTALS OF POCKELS CELLS

1.1 Introduction

The ever increasing number of applications for lasers in scientific research and industry is well known. In many of these applications there is a need to "gate" or modulate the intensity or polarization of the light.

In 1875, Scottish physicist John Kerr discovered the electro-optical effect which now bears his name [1]. The induced birefringence of the Kerr effect was the first electro-optical effect discovered, and can be used to make optical switches by placing a suitably constructed cell between crossed polarizers and subjecting it to a strong electric field. The difference in index of refraction between the parallel and perpendicular components in a Kerr material is proportional to the square of the electric field. The Kerr coefficients are weak, however, and the voltages required are generally in the tens of kilovolts [1]. In addition, the liquids used in Kerr cells are usually toxic, and some are even potentially explosive. Fortunately, another option exists.

1.2 Pockels Effect

The Pockels effect was documented in 1893 by German physicist Friedrich Carl Alwin Pockels [1]. Like the Kerr effect, it manifests as an induced birefringence in the presence of an electric field. However, unlike the Kerr effect, the Pockels effect

is linear with respect to electric field, and affects not primarily liquids, but solids of certain crystal classes without a center of symmetry. Commonly used crystals are ADP (ammonium dihydrogen phosphate, $NH_4H_2PO_4$), KDP (potassium dihydrogen phosphate, KH_2PO_4), and KD*P (potassium dideuterium phosphate, KD_2PO_4) [2].

These crystals are normally aligned with their optical axis inline with the propagation direction of the light beam, and are uniaxial with no external electric field present. Due to the birefringence of the crystal material, a properly constructed Pockels cell behaves as an optical retardation plate. Linearly polarized light entering the crystal along the optical axis is split into ordinary and extraordinary rays, each with different indices of refraction and therefore wavelengths in the crystal medium (Figure 1.1). The phase relationship, and hence the polarization of the light as it exits the crystal, can be determined by the length of the crystal. The beauty of the Pockels effect is that the ratios of ordinary and extraordinary indices of refraction are a function of the electric field. In essence, a Pockels cell is an electrically variable wave plate.

When placed between two crossed linear polarizers (Figure 1.2), the Pockels cell can be used as a switch or modulator. The response time is very fast, typically a nanosecond or less, depending essentially on how quickly and uniformly the electric field can be established. However, even though the required voltages turn out to be five to ten times less than for a Kerr cell, establishing the electric field quickly and smoothly is non-trivial. In addition, the exact retardation versus applied voltage functions are slightly different depending on which of two cell configurations the crystal was mounted in.

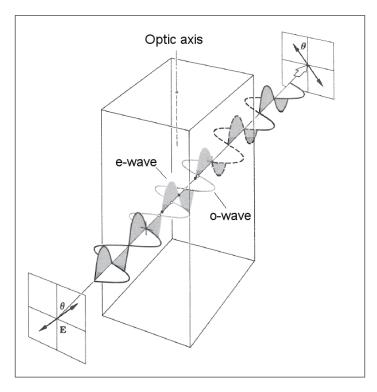


Figure 1.1: $\lambda/2$ waveplate showing 90° rotation caused by successive retardation of the ordinary wave over the crystal length. Transverse orientation shown. Image from Hecht. [1]

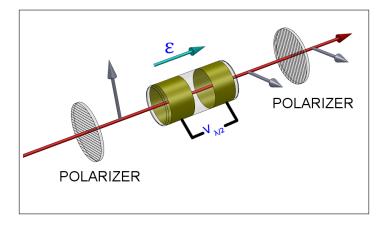


Figure 1.2: An optical switch based upon a longitudinal Pockels cell placed between two crossed wire-grid polarizers.

1.3 Pockels Cell Configurations

There are two basic configurations for applying an excitation voltage across a Pockels cell crystal; longitudinal and transverse. Of the two, longitudinal excitation is the more common. In this configuration, the electric field is set up parallel to the optical beam path via ring electrodes at the two optical faces of the crystal, or via a transparent, conductive facial coating such as a layer of SnO, InO, or CdO [2]. For extremely large facial surface surface areas, plasma electrodes in form of an ionized gas have been used, as is the case in the National Ignition Facility's beamlines [3]. However, the more typical opaque ring electrode is comprised of a soft metal layer, for instance In, Al, Au or Cu, coated onto the surface of the crystal itself. Simple and robust, ring electrodes are usually used with cylindrical crystals in higher power applications, as the absorption in transparent facial electrodes renders them unusable above some power density level. In addition, the higher resistivity of transparent layers can cause heating problems at very high repetition rates. Ring electrodes are not without flaws though, as they exhibit fringing effects that increase the voltages required by 10 to 15 percent and produce a less uniform electric field [2].

In a transverse Pockels cell, the electric field is established perpendicular (transverse) to the optical beam path, utilizing a crystal with electrodes on opposite sides of the optical beam path. Most commonly the crystal itself is of a rectangular cross-section. In a transverse Pockels cell, the effective rotation a beam experiences is proportional not only to the electrical field strength, but also to the length of the crystal itself. This allows the use of longer crystals, or even multiple crystals in optical series and electrical parallel configuration, to achieve optical rotations with lower applied voltages than with longitudinal cells. Unfortunately, transverse Pockels cells have the disadvantage of being limited in the beam size they can accept due to the electrical field strength decreasing with increasing cell width, necessitating ever higher drive voltages. Moreover, the relatively large electrode surface areas required

cause transverse cells to have higher capacitances than equivalent longitudinal cells, which translates into slower switching times due to increased RC time constants.

For an ideal longitudinal cell, the retardation achieved as a function of voltage, δ , in units of wavelengths is [2]:

$$\delta = \frac{\eta_o^3 r_{63} V}{\lambda_0}$$

The half-wave voltage is therefore given by [1]:

$$V_{\lambda/2} = \frac{\lambda_0}{2\eta_o^3 r_{63}}$$

where V= voltage across the cell, $V_{\lambda/2}=$ voltage required for a half-wave retardation, $r_{63}=$ electro-optic tensor coefficient in m/V, $\eta_o=$ ordinary index of refraction, and $\delta=$ number of wavelengths retarded. For KD*P, $\eta_o\approx 1.52$ and $r_{63}\approx 23.3$ [1] or 26.4 pm/V [2], depending on the source. If $\lambda_0=1064$ nm, and assuming a 15 % extra voltage necessary for the fringing fields of ring electrodes, this results in a half-wave voltage $V_{\lambda/2}\approx 7.4$ kV.

The intensity modulation of a monochromatic, collimated light beam caused by a properly aligned Pockels cell placed between two crossed polarizers is

$$\frac{I_{out}}{I_{in}} = \sin^2\left(\pi\delta\right) = \sin^2\left(\frac{\pi\eta_o^3 r_{63}V}{\lambda_0}\right)$$

where I_{in} is the input intensity and I_{out} is the output intensity [2]. Writing the transmissivity in terms of voltage results in

$$T = \sin^2\left(\frac{\pi V}{2V_{\lambda/2}}\right)$$

where $T = \frac{I_{out}}{I_{in}}$. The sin^2 dependence on voltage turns out to have quite important implications in relaxing voltage flatness requirements for Pockels cell drivers.

For a transverse Pockels cell, the retardation equation contains a linear term l

corresponding to the length of cell. The retardation achieved as a function of voltage, δ , in units of wavelengths is [4]:

$$\delta = \frac{l}{\lambda_0} \left[(\eta_o - \eta_e) + \frac{\eta_o^3 r_{63} V}{2d} \right]$$

where l is the length of cell in the direction of optical propagation, and d is the thickness of the cell in the direction of the applied electric field.

A more complete treatment of Pockels cell fundamentals can be found in "Pockels Cell Primer" by Robert Goldstein, listed as Reference [2], and "Optical Electronics" by Amnon Yariv [4].

1.4 Typical Applications in Laser Systems

1.4.1 Pulse Picking

A typical use for a Pockels cell is the selection of a single pulse from a train of multiple pulses, such as picking a single pulse from a master oscillator for further amplification. This can be accomplished by a polarizer - Pockels cell - polarizing beam splitter combination (Figure 1.3) arranged such that only when the Pockels cell has voltage across it the laser pulse polarization is rotated by 90 degrees, consequently causing the ejection of the pulse by the polarizing beam splitter.

Depending on the temporal pulse spacing, the switching speed requirements for a pulse picking application may not be very severe, allowing relatively slow, low-cost, poor stability driver electronics to perform quite adequately. For instance, the task of selecting a single 1 ns wide pulse out of a 10 Hz train of pulses could easily be performed by a Pockels cell driver with a $10\mu s$ rise/fall time and more than $10\mu s$ of timing error. On the other hand, for an application such as the regenerative amplifier shown in Figure 1.4, selecting a 1 ns pulse from a 100 MHz train of pulses leaves only

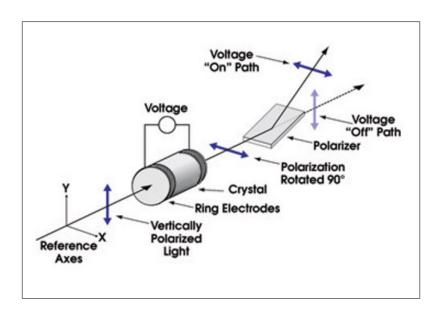


Figure 1.3: Typical gating application of a Pockels cell. Longitudinal cell configuration in half-wave mode shown. Image from Photonics.com [5]. Figure edited for clarity.

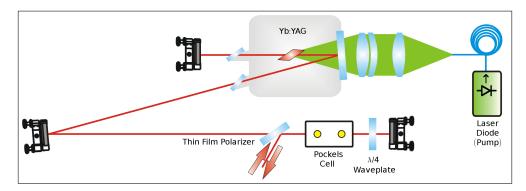


Figure 1.4: A Pockels cell used for pulse-picking in a regenerative amplifier. A longitudinal cell configuration in quarter-wave mode is shown.

9 ns available between pulses to fully switch, making any timing drift or jitter critical. If the width of the 1 ns pulse is a full-width half-maximum specification, even less than 9 ns would be available. For this application a driver capable of switching the Pockels cell completely in less than 5 ns is required.

1.4.2 Inter-Stage Isolation, and Removal of Spurious Pulses and Pedestals

There are some cases where it is important to optically isolate two stages of a complex system, for instance to prevent a reflection from an element in a second stage from returning to the first stage. In such "optical diode" applications an extremely fast Pockels cell driver may be necessary, as the transit time between stages may be only a few nanoseconds, depending on the physical separation between the stages. In high-power, short pulse laser systems parasitic reflections on optics such as the switchout polarizers in a regenerative amplifier, or scattered light off of optics in a folded multipass amplifier may cause temporally shifted low energy pulses to lead or trail the main pulse. These can get amplified by subsequent stages and cause a number of problems ranging from poor efficiency to destruction of components. For example, White et al. describes the importance of Pockels cells for both pulse picking and preventing target destruction due to amplification of temporally leading noise pulses [6]. A sketch of such a laser system is shown in Figure 1.5. Moreover, they limit the contrast of the laser pulses, which is critical in many high power density laser-matter interactions.

Pedestals are temporary increases in the optical "noise floor" surrounding a main pulse. They cause many of the same problems as the temporal glitches already described, but come from different sources. Possible sources are spontaneous emission in an amplifier stage, and in-band pump light leakage, among others. Pedestals can be particularly difficult to deal with because they overlap the main pulse, requiring

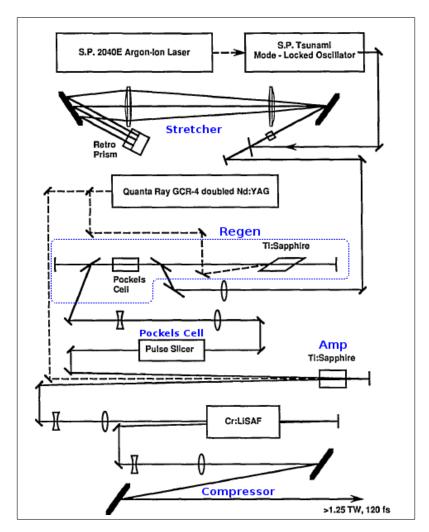


Figure 1.5: Example of a system in which a Pockels cell (labeled "Pulse Slicer") is used for temporal artefact removal after a regenerative amplifier. The regenerative amplifier uses another Pockels cell for pulse-picking. Longitudinal cell configuration in half-wave mode shown. Figure from White et al [6].

the utmost in driver speed and stability to avoid cutting into the main pulse itself. However, Pockels cells cannot completely eliminate pedestals and other techniques must be used to this effect. As one example, a frequency-doubling non-linear crystal could be used to enhance the contrast between the pedestal and the main pulse.

1.4.3 Intracavity Q-switching

Q-switching is a method of achieving high intensity laser pulses by deliberately keeping the round trip loss within a laser cavity high until the laser media has absorbed sufficient pump energy to build a population inversion far in excess of that normally required to reach the lasing threshold. The block in the cavity is then suddenly released, raising the 'Q' of the cavity, and the cavity gain suddenly jumps to very high levels, resulting in a "giant" laser pulse [2]. As shown in Figure 1.6, Pockels cells are often used for this purpose.

Q-switching usually requires quarter-wave switching. This relaxes the drive voltage requirements considerably, and that in turn raises the maximum repetition rate achievable by practical drivers. Q-switch drivers also may only be concerned with leading-edge sharpness, since there is no gain left behind for some time after the "giant" pulse has passed and before the pump source has rebuilt the population inversion. As such, simpler driver designs that would likely prove insufficient for many of the prior applications may work reasonably well as Q-switch drivers. As an example, see reference [7].

1.5 Driver Electronics

The electrical engineering challenges in designing a Pockels cell driver are significant. Due to its construction, a crystalline dielectric with an electrode on each end, a Pockels cell appears to its driver circuit essentially as a pure capacitance. Each time

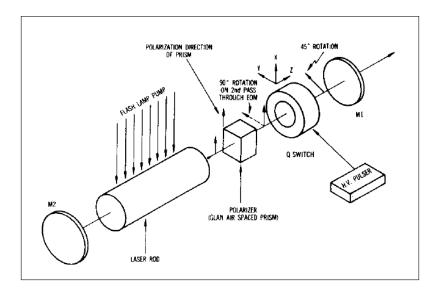


Figure 1.6: A Pockels cell used inside a laser cavity for Q-switching. Figure from Goldstein. [2]

the Pockels cell is to be excited, the driver electronics must switch several kilovolts quickly and cleanly into this capacitive load, sometimes through coaxial cables of relatively low impedance. For 1/2 and 1/4 wave switching applications the driver must also be highly stable in output voltage, which affects optical contrast, as well as pulse width and pulse shape. Controlling timing jitter and drift is of major importance for most applications as well.

1.5.1 Circuit Topologies

Several basic circuit topologies have been used to implement Pockels cell drivers. The key elements in all Pockels cell driver topologies are one or more high speed, high voltage switches. Depending on how the switches, source and load (Pockels cell) are connected, the output pulse seen by each terminal of the load cell can take many forms. An excellent overview is given in Reference [8].

Five topologies in particular warrant a brief review. These are the MOSFET single stack [9], the MOSFET push-pull driver [10] [11], two variations of the avalanche transistor stack [12] [13], and the avalanche Marx stack [14].

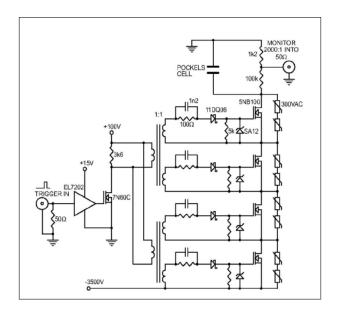


Figure 1.7: Schematic of a MOSFET single-stack Pockels cell driver. Figure from Rutten et al. [9]

The MOSFET Single Stack

Ideally, a high voltage Pockels cell driver would maintain zero volts DC on its outputs at all times until the time of triggering. At that moment, it would emit an essentially perfect rectangular pulse of the exact high voltage value required, regardless of the capacitance of the Pockels cell being driven. Unfortunately, this can be quite difficult to achieve in practice, especially when nanosecond switching speeds are desired. The MOSFET single stack method (Figure 1.7) used by Rutten et al. [9] abandons the idea of a truly rectangular pulse and instead focuses on a high quality leading edge and long, smooth, flat "on" period at the expense of a very slow falling edge (Figure 1.8). A slow falling edge is indeed acceptable for Q-switching, but renders the design unsuitable for spurious pulse and pedestal removal, as well as for some pulse-picking applications. Nevertheless, the MOSFET single stack design is fairly robust, low noise, and remains popular. Switching speeds for MOSFET stacks are typically on the order of several ns [8] [9] [15] [16] [17]. More information, examples, and theory can be found in References [15], [16], and [18].

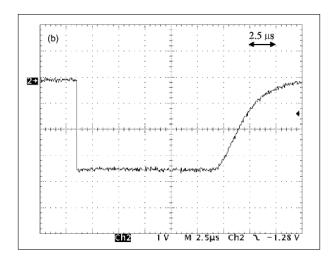


Figure 1.8: Waveshape produced by the MOSFET single-stack Pockels cell driver. Leading edge transition time is 9ns (10%-90%). Trailing edge is 5us. 1kV/div. Figure from Rutten et al. [9]

The slow trailing edge of the single stack MOSFET driver in Figure 1.7 is due to the RC time constant involved in discharging the capacitance of the Pockels cell through the resistor across it once the MOSFET stack turns off. By using a second high voltage switch to perform the discharging operation, the trailing edge can be sped up significantly. However, this is not without complications.

The Push-Pull Stack

One such method of achieving both a rapid turn-on and turn-off that initially appears quite attractive is the push-pull topology (Figure 1.9). The upper switch, Sw1, is turned on first, charging the Pockels cell's inherent capacitance Cp through the switch "on" resistance Rsw1. At the end of the window, Sw1 is turned off, and Sw2 is turned on, discharging the Pockels cell to ground just as quickly. Unfortunately, the apparent simplicity rapidly dissolves when the necessary isolated switch drive circuitry is designed, as the upper switch Sw1 also needs to be turned off quickly as the lower switch Sw2 is turned on [19]. This immediately seems to rule out any pulse-triggered high voltage switch device that "latches on", while a design using

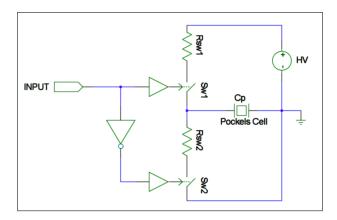


Figure 1.9: Driving a Pockels cell with a push-pull switch arrangement. The upper switch requires a well-isolated driver capable of both turn-on and turn-off. Note the two switches must never be on at the same time.

MOSFETs would typically require heavily isolated, floating gate drive circuitry capable of charging and discharging the gate capacitance of each gate in the switch stack simultaneously. To convert the single MOSFET stack of Figure 1.7 to a push-pull design would not double, but triple the complexity [11]. Furthermore, as additional stages are added to increase the voltage range up to that necessary for 1/2 wave operation, synchronization and load balancing between the large number of trigger transformers needed to trigger each stage becomes a problem. Lastly, the second switch Sw2 would need to withstand the direct transient from the first switch turning on without ill effects. Besides simple voltage sharing issues, the Miller capacitances [20] inherent in all three-terminal switching devices causes problems in this regard. A fast rising edge on the drain of an N-channel MOSFET will couple through the gate-drain capacitance to the gate, attempting to turn the device on. At best, this results in slower switching times.

The Avalanche Transistor Stack

Variations of the avalanche transistor stack have been extensively documented in the literature. Of particular interest are two papers by Fulkerson et al. [12] [13].

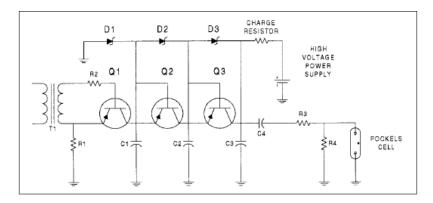


Figure 1.10: Simplified schematic of a single stack avalanche transistor switch used for 1/4 wave applications. Only three stages are shown. Figure from [13].

The former discusses the avalanche switch stack in detail, while the latter expands on the use of the avalanche stacks for driving Pockels cells. Two configurations are discussed, a single stack switch intended for driving quarter-wave cells, and a split polarity dual stack intended for half-wave applications. These are shown in Figure 1.10 and Figure 1.12 respectively. While both of these designs put out non-rectangular pulses (Figure 1.11), Fulkerson et al. have achieved remarkable leading edge speeds, reportedly less than 100ps under some conditions. Normal operating voltages are 4.5 kV for the single stack [12], and 9 kV for the split polarity double-stack of Figure 1.12. It is important to note that although Fulkerson et al. call the circuit of Figure 1.12 "push-pull", it is a non-standard use of the term. Both sides switch to ground simultaneously, but from opposite potentials on opposite ends of the load, whereas in a classic push-pull circuit the switches are both at one end of a ground-referenced load and alternate their conduction, reversing current flow through the load. The former doubles the voltage across the load, while the latter produces symmetrical rising and falling edges.

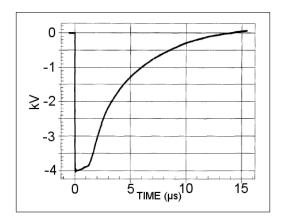


Figure 1.11: Output voltage from 1/4 wave circuit of Figure 1.10. Leading edge transition times below 100 ps have been reported [13]. Figure from [13]. Figure edited for readability.

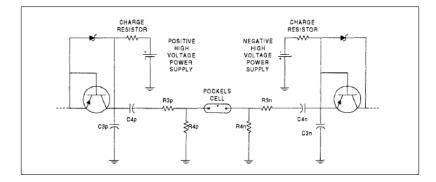


Figure 1.12: Simplified schematic of a split polarity dual stack avalanche transistor switch used for 1/2 wave applications. Both sides switch to ground simultaneously, but from opposite potentials. Only the last stage is shown. Figure edited slightly for clarity. Original figure from [13].

The Avalanche Transistor Marx Pulser

The high voltages required by Pockels cells cause difficulties with corona and flashover that are further exacerbated by the need for small geometries in extremely high speed circuits. All the topologies considered so far maintain the full switching voltage as a DC potential. One popular way to alleviate the threat of corona induced breakdown is to use a Marx bank configuration to reduce the necessary DC supply voltage. In a Marx bank, a lower voltage is stored upon several paralleled capacitors which are then rapidly switched into a series configuration. This allows the output voltage to pulse to a value several times greater than the DC supply voltage. The use of avalanche transistors in Marx bank pulsers has been extensively analysed by Mallik [21] and Chatterjee et al. [22].

Bishop and Barker [14] achieved 238ps leading edge optical transition times utilizing a 4 kV avalanche transistor Marx pulser coupled to a Leysop dual-crystal KD*P Pockels cell through a 50 ohm coaxial cable. Achieving transition times shorter than the RC time constant of the cable impedance and cell capacitance required a Pockels cell built into a matched transmission line structure. The circuit is shown in Figure 1.13 and the optical transmission profile is shown in Figure 1.14. Note that the circuit diagram shows the Pockels cell as a discrete capacitance, however it is constructed as part of a 50 ohm transmission line section, and does not present as a lumped complex impedance.

1.5.2 Advantages of Avalanche Transistors for High Speed Switching

Various devices have been used as high-speed, high-voltage switches for Pockels cells over the years, including MOSFETs [9] [10] [11] [17], avalanche bipolar junction transistors (BJTs) [7] [12] [13] [14], planar RF triodes [23], krytrons, thyratrons [24]

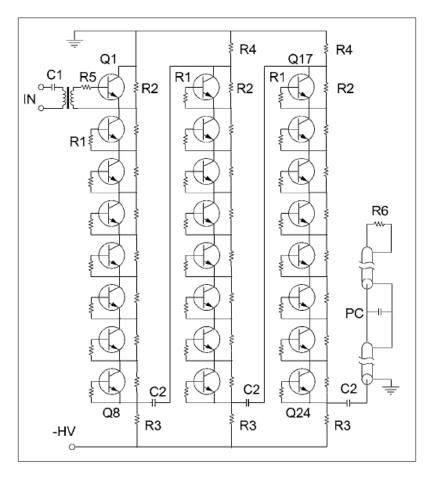


Figure 1.13: Avalanche transistor Marx pulser. Note the Pockels cell was actually matched to the transmission line rather than a discrete capacitance as it appears here. Figure from [14].

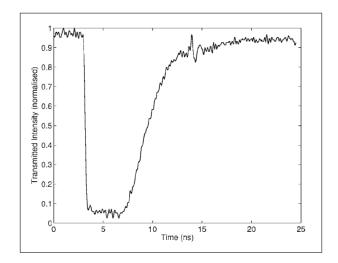


Figure 1.14: Avalanche transistor Marx pulser optical transmission vs. time. From [14].

[25], SCRs, spark gaps, photoconductors, and drift-step-recovery diodes (DSRDs) [26]. Each presents their own set of advantages and disadvantages. References [8] and especially [26] briefly summarize some of the relative merits, however the latter is now quite out of date with respect to modern MOSFET and avalanche transistor driver capabilities.

Modern commercially available Pockels cell drivers for laser applications tend to be based on the MOSFET and the avalanche BJT. MOSFET drivers use familiar switch devices and produce clean, quiet output pulses, in a large part because they are the slower of the two. Typical switching times are 3-10 ns. MOSFET drivers are also adjustable over a very wide operating voltage range and can easily be used for either quarter wave or half wave applications. Avalanche bipolar junction transistor drivers cannot be used over a wide voltage range, however they switch an order of magnitude faster, typically between 0.3 and 2 ns. Since they are bipolar devices, they also exhibit very low forward voltage drop once switched on, becoming closer to an ideal closed switch under high current conditions.

A qualitative explanation is as follows. In an N-channel MOSFET device, conductivity between the N-doped drain and source regions is modulated by an electric field from the positively biased gate driving away holes (attracting electrons) in the P-doped gate region. This establishes an N-like conductive channel between the drain and the source along which electrons can flow. How quickly this channel can be established is primarily a function of how fast the external gate drive circuit can charge the capacitance of the gate. It is critical to note that even with an ideal, zero-impedance gate driver, the internal inductances and resistances of the MOSFET device package and silicon would prevent arbitrarily short turn-on times [18]. Further hampering rapid turn-on is the so-called Miller capacitance between drain and gate. The falling drain voltage with respect to the source and gate induces a displacement current through the drain-gate capacitance, attempting to turn off the device and multiply-

ing the effective drain-gate capacitance by the gain of the device [20]. In addition, the need for sub-nanosecond synchronization coupled with the necessity of independent high-voltage isolation for the gate drive circuit of every MOSFET in the stack makes it quite difficult to achieve a truly low impedance gate drive. The net effect is a slower transition. Baker et al. [18] do present a conceptually elegant method of capacitively driving the MOSFET gates, however since pure capacitances exist in theory only, the method they describe leaves the MOSFETs vulnerable to gate oxide layer punctures from voltage transients.

Avalanche transistors work in a fundamentally different way. Although a complete analysis of avalanche transistor switching is beyond the scope of this thesis, a rough explanation is still in order. It is first necessary to examine the behaviour of a reversebiased P-N diode [20]. When the electric field across a reverse-biased N-P junction reaches a critical strength, the energy attained by free electrons accelerating over their mean-free-path distance is great enough that they are able to create additional electron-hole pairs upon collision with the lattice. The newly liberated electrons are in turn accelerated and collide, creating an "avalanche" of carriers as the process repeats. This avalanche, or "ionization wave", ceases only when the electric field across the junction is reduced below the critical strength, either by external means or as a result of this sudden generation of free charge carriers. Although the heat generated is potentially destructive to the crystal lattice if uncontrolled, this is the mechanism behind the operation of avalanche voltage regulating diodes, as well as the avalanchebased overvoltage protection built into many modern power MOSFETs. Avalanche multiplication in two-layer PN junction devices is interesting enough, however for the three-layer NPN avalanche bipolar junction transistor with bipolar current gain, it is only half the story.

There are two readily available datasheet parameters given for a BJT that indicate the minimum collector-emitter voltage at which avalanche breakdown is likely to occur: V_{CBO} and V_{CEO} (Figure 1.15). V_{CBO} is the collector-base breakdown voltage with the emitter open, representing the breakdown voltage of the reverse-biased collector-base junction alone. All holes injected from the collector are removed through the base, and although avalanche current multiplication occurs, no additional transistor gain is observed. V_{CEO} is the collector-emitter breakdown voltage with the base terminal floating. In such a situation, the holes injected at the collector-base junction forward bias the base-emitter junction, and the avalanche current is further multiplied by the gain of the device. Due to this additional multiplication, V_{CEO} is always lower in magnitude than V_{CBO} . A transistor can be triggered to switch between the two levels with the application of a fast-rising base-emitter pulse.

If the resulting avalanche current is large enough, such as when sufficient external capacitance is present across the collector and emitter, the transistor enters current-mode secondary breakdown (CMSB). CMSB appears to be a different phenomenon than the thermal second breakdown that most transistor designers are familiar with. In this mode, the I-V behavior follows the dashed line indicated in Figure 1.15 from point A' to point C, outside the safe operating area, rather than stopping at point B. This ability to switch completely "on" such that the collector-emitter voltage drops below the steady-state value needed to sustain avalanche injection is particular to the bipolar junction transistor, and to the author's knowledge is not seen in simple two-layer devices. One can intuitively see how the sudden injection of a very large number of holes into the base region far faster than they can be cleared out or recombine could potentially leave the transistor in a solidly "on" state despite the electric field strength across the collector region dropping below that needed to sustain avalanche multiplication. For a more rigorous treatment of this subject, consult references [21], [22], [28], [29], and their references.

The critical concept when comparing the switching behaviour of the MOSFET and the avalanche BJT is that the MOSFET's switching rate is driven by its external

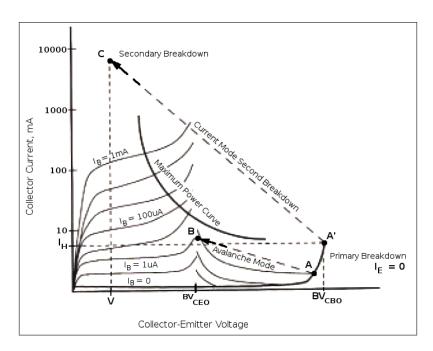


Figure 1.15: I-V curves of an epitaxial planar bipolar junction transistor. Figure from Baker [27]. I_B labels added.

gate signal and limited by its internal makeup, whereas the avalanche BJT obtains its switching speed via the inherently faster internal feedback mechanism of avalanche current multiplication.

Bipolar transistors used for avalanche mode switching are typically small signal planar epitaxial devices. Standard commercial devices such as the 2N2222A, 2N3904, and 2N5551 are often used in low cost designs. However they generally require time-consuming individual characterization and matching of avalanche parameters such as leakage current, breakdown voltage, avalanche gain and maximum avalanche conduction current. Burn-in is often performed to weed out infant mortalities. Several articles have been published which address selection of suitable transistors, however a commonality between all "re-purposed" standard devices is a relatively low "robustness" as well as somewhat low peak current capabilities.

Another option is to use a transistor specifically designed for avalanche mode operation such as the FMMT413, FMMT415, or FMMT417. These devices are man-

ufactured by the Zetex division of Diodes Incorporated precisely for high-speed, high-current avalanche switch applications [30], and have been pre-tested and pre-qualified at the factory. They are available in tiny SOT-23 surface mount packages, can switch 50 A for 25 ns, and have been reported to provide transition times as low as 100 ps [12]. The V_{CBO} ranges from 150 V for the FFMT413 to 320 V for the FMMT417. The drawback is higher cost and restriction to a single manufacturer.

1.5.3 Transmission Line Effects

It is well known that an electromagnetic wavefront propagating through a media will experience some degree of reflection whenever there is a change in the media impedance. The sign, magnitude and phase of the reflected and transmitted portions will depend on the exact nature of the change. The spatial distribution of the impedance change relative to the spread of the impinging wavefront in the direction of propagation will greatly affect the frequency response of the reflection, with sharp discontinuities having a much more pronounced effect than gradual transitions. Likewise, since the reflected wave is essentially a convolution of the impinging wave with the impedance change, quickly transitioning signals will faithfully imprint the shape of the impedance change onto the resulting reflections. Wideband distributed electronic circuits rely on either working at wavelengths much longer than the component sizes and spacings, or utilizing matched transmission line structures. Narrowband circuits can be tuned such that the reflections sum to zero, for instance, but sharp-edged pulse circuits are by nature wideband. In an unmatched complex, high speed pulse system, overlapping reflections and re-reflections not only quickly obscure the original sources of the reflections, but can cause severe signal distortion, performance degradation, and even device failure due to local current and voltage excesses. Severe signal distortions that appear across the driven electro-optic cell may cause significant optical performance degradation via undesired modulation, even if no failures occur.

In an electro-optic switch system, there are many potential impedance mismatches to consider. The most obvious is the electro-optic switch itself, which usually presents as a nearly pure capacitance of some small value. Consequently, the very highest frequency components of the driving pulse pass right through the capacitance of the cell, while most of the remainder is reflected right back into the driver electronics of the high voltage switch. In colliding-pulse systems, the high frequency portion of the pulse that passed through the cell from the first switch encounters the electronics of the second high voltage switch, which may still be in the "off" state. There, a portion may be re-reflected back towards the electro-optic switch, while the rest could enter the second switch, perhaps causing it to trigger prematurely or even damaging it. In grounded-cell systems, the high-frequency portion simply reflects off ground and returns back through the cell to the originating switch, with similar potentially damaging results. Terminating the far side of the cell with an appropriate load can prevent the latter problem, but only building the electro-optic switch cell into a transmission line structure to completely eliminate impedance mismatches will remove the problem of reflections. Due to the very high dielectric constant of typical Pockels cell materials ($\epsilon_r \approx 55$), this is easier said than done. However, the highest speed Pockels cells are built in such a manner.

Far more insidious are mismatches in the high voltage switches themselves. High voltages require large clearances, so components tend to be large, with relatively high parasitic inductance, creating problems with impedance mismatches, resonances, pulse arrival times, and switching speed. In addition, many series-stacked switch stages are needed if semiconductor devices are used. This become increasingly difficult to manage as switching times become of the order of transit times between impedance discontinuities.

Ideally, the switches would be located infinitely closely together and switched simultaneously. Since this is impossible, the next best situation for an extreme-speed

driver is that each switch closes at the exact instant that the wavefront from the previous switch closure arrives, creating a high-quality wavefront that propagates towards the output of the driver. Each switch closure will also produce a backwards-propagating pulse that moves towards the opposite end of the switch stack, resulting in a series of backwards-propagating pulses that must be absorbed. Reflections off of impedance mismatches in each stage further complicates the issue. Impedance mismatches must be minimized as much as possible, for instance by embedding the switches into an appropriate transmission line structure.

1.5.4 Discussion of Timing, Jitter and Drift

It is clear that the synchronization of an electro-optical switch with external events is of critical importance, and that the faster the switch required for a task, the tighter the timing requirements will likely be. For instance, a Pockels cell utilized before a laser amplifier as a pedestal removal chopper/pulse-slicer will have its turn-on window edge positioned as close in time as possible to the main laser pulse that will be amplified. If the Pockels cell and driver combination has an optical transition time of 2 ns, and the window is positioned such that full turn on occurs 1 ns before the main laser pulse, then clearly less than 1 ns of timing shifts can be tolerated before the main pulse begins to be clipped, and even before then the variation in amplified pedestal light is likely to cause some problems. On the other hand, a pulse-picking application may be quite tolerant to timing shifts due to the relatively wide temporal spacing between adjacent laser pulses.

In these situations the timing of concern is the delay between the receipt of a trigger signal and the high voltage transition at the Pockels cell. For the purposes of this discussion, it will be assumed that the Pockels cell itself is completely stable. In the digital world, such an input-to-output transition delay is termed propagation time.

The timing shifts that affect electronic instruments come in two principle forms: drift and jitter. Drift is a relatively slow variation in input-to-output propagation time that is most commonly caused by temperature variations, but is also due in part to component ageing and other incremental degradation. Another less common cause is leakage currents through corrosion due to improper cleaning of flux from circuit boards or even outright contamination from an external source. The sources of drift are relatively easy to identify by correlating the drift with environmental conditions. For instance, higher humidity will worsen drift caused by improper cleaning.

Since the dominant source of drift is usually temperature variations, using low temperature coefficient components, adding thermal compensation circuitry, improving heat extraction from heat generating components and segregating thermally sensitive components from heat generating components all help reduce drift. Temperature stabilization of the Pockels cell driver is also effective. Fortunately, since complex optical systems tend to be very temperature sensitive, the environment in which a Pockels cell driver must operate may be fairly temperature stable already, with multiple cooling options available.

Whatever the source of drift, the rate of drift almost always scales linearly with the total propagation time of the most sensitive part of the circuit. Therefore, the surest way to reduce drift is to reduce input-to-output delays. As a simple example, consider a Pockels cell driver utilizing a string of MOSFETs with their gates driven by the simultaneous flyback of small ferrite gate transformers. If the gate transformers require $10\mu s$ to store the required energy in their magnetic field before flyback, and the $10\mu s$ is controlled by an RC timer circuit using a $100ppm/^{o}C$ temperature coefficient resistor, then it may only take a $1^{o}C$ change of resistor temperature to cause a 1 ns drift in the optical window position. On the other hand, an avalanche transistor driver with a 100 ns input-to-output propagation delay could tolerate one hundred times worse temperature coefficients to achieve the same drift performance.

Jitter is shot-to-shot variation in timing. It often appears nearly random in nature, and in some physical systems truly is a random phenomenon. However, in electronic instruments the dominant source of jitter is electrical noise superimposed upon trigger or clock signals, or injected into power and ground planes. In high speed integrated circuits, the sudden switching of an output (for example) can draw enough current through internal metallization or ground bond wires to momentarily shift the effective level of the signals on other input pins. This is a form of crosstalk, and is related to jitter in the following way: a slight shift in level of a transitioning signal becomes a time shift as the signal crosses the internal logic threshold level slightly earlier or later than normal. The slower the rise and fall times of the "real" input signal in the vicinity of the threshold level, the worse the jitter. Observed jitter therefore can be highly dependent on the transition speed of the trigger signals into a Pockels cell driver, and care must be taken to ensure that the trigger signals transition quickly and cleanly through the logic threshold regions before drawing any conclusions about a driver's jitter performance.

Jitter is less likely than drift to scale with total propagation time, however it can appear to do so if the change in propagation time is performed by slowing signal transition rates somewhere in the system under test. The degree to which the jitter does scale with localized changes in propagation time can potentially help identify the most sensitive areas of an existing design. Methods of improving jitter performance include proper grounding and power supply bypassing techniques, physically separating high speed circuits that will receive nearly identically timed trigger edges, and the use of isolation and shielding. Slowly transitioning internal signals should be avoided, although excessively fast switching signals contribute to a noisy environment and may worsen overall jitter problems if the generated noise is allowed to couple into other areas of the circuit that are switching at approximately the same time.

Chapter 2

DESIGN, CONSTRUCTION AND CHARACTERIZATION

2.1 Introduction

This chapter describes the development of a robust, high voltage (8 kV), high stability, source terminated, dual-channel, fast avalanche transistor pulser designed for use with unterminated 50 ohm coaxial cables. These pulsers are currently used to drive Pockels cells in colliding pulse mode in 1/2-wave pulse picking and slicing applications where optical rise times of < 2 ns and low drift are needed. Novel non-invasive diagnostic techniques for measuring and graphing pulse propagation in a repeatable manner along collapsing avalanche transistor chains are presented.

2.2 Electrical Design and Considerations

2.2.1 Overview

A block diagram of the complete avalanche transistor Pockels cell driver is shown in Figure 2.2. The driver consists of: two independent, source-terminated avalanche transistor switch boards; individually adjustable, short propagation time trigger amplifiers; a stable, adjustable high-voltage power supply; low voltage filtering and point-of-load regulation. It also includes a dual channel, 4-digit, microcontroller-based voltmeter with backlit LCD dot-matrix graphical display. Special attention

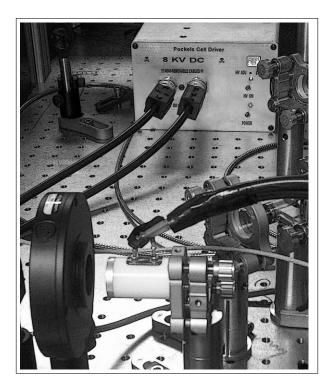


Figure 2.1: Pockels cell driver driving an Impact 13 cell at 8 kV.

has been paid to thermal stability, corona prevention, and EMI shielding. The entire assembly is constructed in a smooth-surfaced extruded aluminium housing intended for direct contact with a grounded, thermally stable surface such as an optical table. High-voltage coaxial cables 1.2 m long allow for the driver to be located far from the Pockels cell itself. An example installation is pictured in Figure 2.1.

The unit is designed to drive each side of a 1/2 wave configured Pockels cell in colliding-pulse mode by applying 6 to 8 kV DC voltage to each of the two Pockels cell electrodes and switching them to ground in turn. The time difference between the two edges establishes a well-defined nominally rectangular window during which the full 6-8 kV potential appears across the cell.

Unlike prior reported implementations of avalanche transistor Pockels cell drivers, this design is undamaged by the pulse collisions and the portion of each pulse that couples through the Pockels cell capacitance. Each avalanche transistor switch, composed in turn of two parallel transistor strings, is source-terminated with distributed impedance matching networks. Rather than attempt to absorb reflections at the Pockels cell, at the cost of a large stored charge on a DC-blocking capacitor, the current design utilizes the impedance mismatch reflection at the coaxial cable-Pockels cell interface to achieve the full voltage swing. The 50 ohm coaxial cables serve multiple duties, not only physically separating the driver from the Pockels cell, but also providing temporal isolation between the two channels, providing a constant-impedance source of charge, and serving to "prop up" the not-yet-switched side of the Pockels cell.

2.2.2 Theory of Operation

A brief theory of operation for an 8 kV configured driver is as follows. Referring to Figure 2.3, before the leading edge triggers, the full 8 kV is present at both outputs, leaving a differential voltage across the Pockels cell of zero volts. When the first switch turns on, its 50 ohm line (cable X1) is connected to ground through its 50 ohm source termination, launching a 4 kV negative-going wave towards the Pockels cell. Upon reaching the Pockels cell, a portion of the wave passes through the small capacitance of the cell, but the majority reflects off the cell back towards the initiating switch, where it is absorbed. The reflection causes the voltage across the cell to rise from 0 V to 8 kV in a time determined predominantly by the larger of either the switch transition time or 2 times the R-C time constant formed by the cable impedance and the Pockels cell capacitance. The wave generated by the second switch closing behaves similarly, however since the voltage on the first side of the cell is now zero, the reflection of the second wave causes the voltage across the cell to drop from 8 kV back to zero.

The dominant source of current carried by each switch is the charge stored in the capacitance of the 1.2 m long coaxial output cables X1 and X2. The cables are

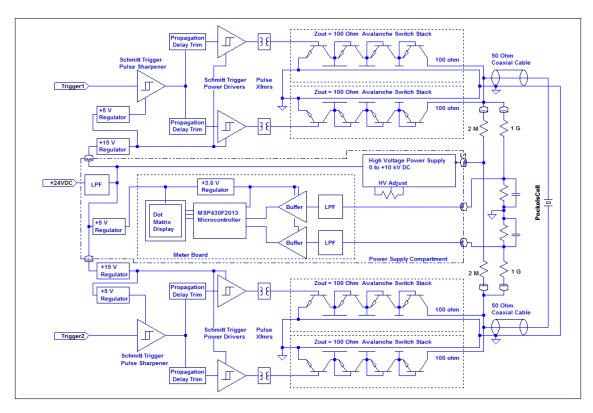


Figure 2.2: Block diagram of dual-channel colliding-pulse avalanche transistor pulser.

non-removable, with a capacitance of approximately 120 pF, or roughly 20x that of an Impact13 Pockels cell. With an 8 kV bias, the $Z_0 \approx 50\Omega$ impedance of the cables and the driver's matching source termination impedance (R_{sw}) results in each switch carrying a rectangular current pulse of $V_{bias}/2Z_0 \approx 80$ A for ≈ 15 ns.

2.2.3 High Voltage Switch Design

The avalanche transistors chosen for the current design are FMMT417 devices by the Zetex division of Diodes Incorporated. They are specifically designed for avalanche-mode switching operation, have a minimum $V_{BR(CES)}$ of 320 V, and a rated maximum avalanche current of 60 A for a 20 ns wide pulse. The FMMT417 devices have proven themselves to be substantially more rugged in this application than other avalanche-capable planar BJTs, such as the 2N2222A or the 2N5551.

Since the current handling necessary is greater than a single transistor can support,

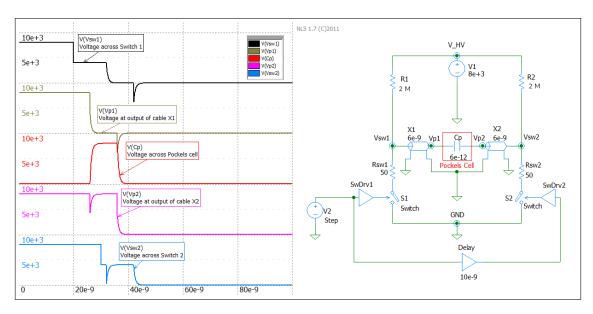


Figure 2.3: Simplified diagram of colliding-pulse mode of operation as utilized by the current Pockels cell driver design. Voltages and times are representative only.

multiple paralleled transistors are required. Prior avalanche transistor pulser designs paralleled the transistors in each stage. As an example, see Fulkerson and Booth's well known design, shown in Figure 2.5. Although simpler, the direct-paralleling method suffers from current sharing issues in the over-voltage triggered stages. Due to the avalanche current multiplication effect in the transistors as they begin switching, the first transistor to enter current mode second breakdown (CMSB) appears to be able to "hog" the current, depleting the available charge and dropping V_{CE} quickly enough that the remaining paralleled transistors may fail to enter (or remain in) CMSB. This situation can occur if there is any mismatch in avalanche parameters between the paralleled transistors, and was easily observed in Spice simulations once each transistor was provided with its own independent and very slightly differing model card. The Spice simulations utilized FMMT417 models provided by the Zetex division of Diodes, Inc. Prototype designs constructed with directly paralleled transistors also began to fail as bias voltages increased beyond about 5 kV. It should be noted that no attempt was made to match the individual transistor parameters beyond the screening

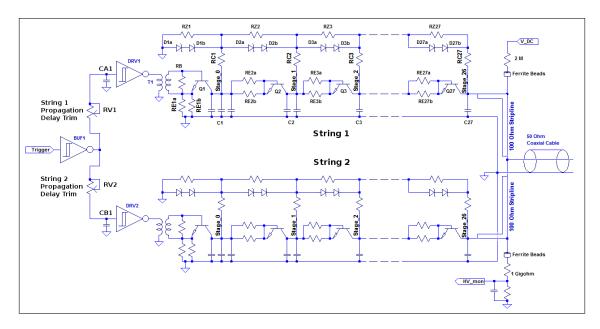


Figure 2.4: Conceptual sketch of one half of the avalanche transistor switch. Each parallel string is designed for 100 ohms. The trigger signal to the two strings is split and individually trimmed for simultaneous HV pulse arrival at the 50 ohm cable connection.

performed at the factory.

As shown in Figure 2.2, there are two paralleled high voltage switch stacks for each output channel of the half-wave Pockels cell driver. Figure 2.4 is a more detailed schematic of one output channel. Each string is designed as a lumped-element transmission line which gradually steps the impedance from $Z=100\Omega$ at the high voltage end to $Z\approx 3.7\Omega$ at the ground end. A 100 ohm stripline from each switch stack connects them in parallel to a common junction at the 50 ohm output cable.

By utilizing two completely independent parallel avalanche transistor strings, the problem of current "hogging" by individual transistors is completely eliminated. Distributed resistances at each stage reduce and dampen reflections that could otherwise cause localized voltage and current excesses along the string. It is important to note that the electrical length of such a series switch stack is greater than the dominant wavelengths generated by the switching of a single transistor. Significant components

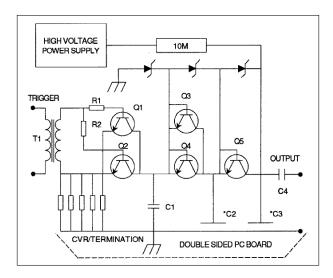


Figure 2.5: Example of "prior art" avalanche transistor pulser design. Note direct paralleling of transistors in lower stages. Figure from Fulkerson et al. [12]

exist well into the GHz region. The distributed resistances also allow the switched-on stack to appear as a source termination for frequency components with wavelengths longer than the electrical length of the stack, such as those generated by the discharge of the attached coaxial cables.

2.2.4 Stability and Triggering

Several methods are used to keep the Pockels cell driver's window stable in magnitude and temporal position. Electronic methods include pre-regulating and filtering the supply voltage to the high voltage bias supply, utilizing high-speed, low propagation time Schmitt-trigger input buffers, overdriving the first-stage base-emitter triggers, and the use of voltage balancing resistor networks in the switch stacks. Mechanical and thermal methods include separate EMI shielding compartments for different circuit subsections, and mounting both high voltage switch circuit boards directly to a single thick aluminium heat sink plate.

The total switching times of the avalanche transistor stacks are affected by the bias voltage present in a nonlinear manner. For the current design, the input-tooutput "propagation" delay decreases by approximately 2.2 picoseconds per volt at 8 kV nominal bias. This coefficient itself varies roughly linearly between 6 kV and 8 kV, increasing in magnitude as the bias voltage decreases, to 3.85 ps / V at 6 kV bias. As the bias voltage is reduced below 6 kV the switching time begins to increase dramatically until switching stops altogether, therefore operating the current design below 6 kV is not recommended. In order to minimize drift caused by bias voltage fluctuations, the input power to the bias HV DC-DC module is sourced from a well-regulated, electrically-quiet switching power supply and extensively filtered, as described in the next section.

2.2.5 Power Supplies

An operational overview of the power supplies is as follows. 24 VDC regulated power is supplied to the unit's power supply compartment through a standard barrel-type DC power connector. The 24 V passes through a low pass filter network (LPF) consisting of ferrite beads, bypass capacitors, and a 2nd-order Butterworth L-C low-pass filter. Electrolytic and ceramic capacitors are used in parallel to keep the capacitive elements effective over as wide a frequency range as possible. The filtered DC is then supplied to the high voltage power supply (HVPS) module, to a 5 V linear regulator for the voltmeter circuit, and to the high-voltage compartments via filtered feed-through terminals.

The HVPS module converts 24 VDC to the 6-9 kV HVDC needed by the avalanche transistor switches. Inside the independent high voltage compartments, the HVDC is filtered through ferrite beads and fed to the top of each of the avalanche transistor strings via 2 megohm thick-film high voltage resistors. The 24 V output is regulated down to 15 V for the Schmitt-trigger power drivers, and from 15 V to 5 V for the Schmitt-trigger input buffers. Point-of-load regulation serves to enhance isolation between the two high-voltage compartments, reducing the likelihood of noise generated

by the leading-edge switch causing timing jitter or false triggering in the trailing edge switch.

2.2.6 High Resolution Dual Digital Voltmeter

DC bias voltage levels on each output are monitored by a custom built dual-channel digital voltmeter. The voltmeter is intended to provide the user with aid in adjusting the half-wave voltage on the Pockels cell and an indication of device health. Since it directly measures the high voltage seen by the Pockels cell, it has also proven to be a time saver when troubleshooting laser system problems that could potentially be caused by a malfunctioning Pockels cell driver.

The voltmeter is based around a Texas Instruments MSP430F2013 microcontroller with a multi-channel 16-bit sigma-delta analog-to-digital converter module. Voltage at the top of each avalanche transistor stack is divided down via a voltage divider comprised of a 1000 megohm thick-film high voltage resistor and R-C pair. The divided and pre-filtered voltage is then routed via Teflon coaxial cables to filtered feedthroughs and into the EMI shielded power supply compartment. Coaxial cables bring the signal to the voltmeter printed circuit board, where it undergoes further filtering and scaling. The fully filtered signal is buffered by a unity-gain National Semiconductor LMV832 EMI-hardened low input bias current op-amp before reaching the ADC pins of the microcontroller. A voltage of 400 mV at the microcontroller corresponds to 8 kV at the driver output. Since the sense current is only 1 microamp per kilovolt, rigorous and thorough cleaning of the printed circuit boards between the 1000 megohm resistor and the buffer amplifier is necessary to prevent surface leakage currents from introducing significant measurement errors. Guard traces driven by the buffered unity-gain op-amp outputs are used where appropriate to help reduce leakage currents.

The firmware in the MSP430F2013 microcontroller is written completely from

scratch in assembly language. Both 16-bit ADC channels are configured for 256x oversampling and $\pm 600 mV$ input range. 600 individual conversions are averaged for each reading, and linear slope and offset corrections are applied to compensate for component tolerance variations. For each channel, the resulting value is converted into 4-digit binary-coded-decimal and each character is then used to index into a bitmapped font table. The indexed characters in the font table are then rasterscanned row-by-row, pixel-by-pixel and transmitted serially to an NKK IS01DBFRGB dot-matrix display. The IS01DBFRGB is a micro-miniature 64 x 32 pixel LCD dotmatrix display with a 13.9 x 10.6 mm display area and an RGB backlight. It is capable of displaying 8 characters by 4 lines with an 8-pixel by 8-pixel font. The voltmeter displays the output bias voltage of both channels in the range from 0 to 9999 V in increments of 1 V, where a 1 volt reading change corresponds to a 1 nano-ampere change in sense current. The display update rate is several times per second, comparable to commercial digital panel meters. A firmware compile date is also displayed, and one blank line remains which may be used in the future to display enclosure temperature. The RGB backlight color is programmed to a color that is visible through the laser safety goggles used in whichever laboratory the Pockels cell driver is deployed. Programming and calibration of the meter board microcontroller is accomplished in-system using a 4-pin header compatible with the target-board connector of the Texas Instruments eZ430-F2013 development kit. The meter board is constructed with all surface mount components on a standard FR4 epoxy-fiberglass double-sided printed circuit board. The bottom layer of the board is a nearly completely solid ground plane, and an insulating solder-mask layer reduces exposed surface area which would otherwise contribute towards leakage currents. The voltmeter has proven itself to be stable and reliable, in spite of the extremely low-level signals in a harsh noise environment.

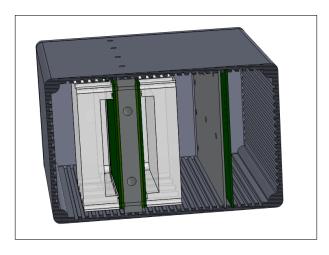


Figure 2.6: Schematic cutaway end view of the Pockels cell driver housing showing compartmented structure and oil enclosures.

2.3 Physical Design and Construction

The dual-channel Pockels cell driver is enclosed in an extruded aluminium chassis 165 mm wide by 105 mm tall by 318 mm long. The front and back covers are CNC machined from aluminium plate and sealed with EMI gaskets. Openings in the enclosure are kept as small as possible to minimize EMI leakage. Internally, the chassis is divided into three EMI isolated compartments, one for each output channel and a power supply compartment (Figure 2.6). The DVM and control switches reside in the power supply compartment (Figure 2.7). Each avalanche transistor stack is covered with a thick acrylic box filled with highly refined transformer oil and sealed to the FR4 printed circuit board itself with a slightly over-compressed silicone O-ring. Machine screws pass through the acrylic box and sandwich the PCB rigidly to the dividing heatsink and ground plate. Units constructed in this manner have been in service for over one year with no trace of oil leakage.

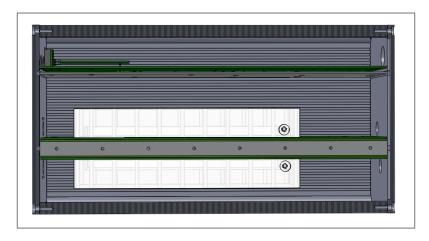


Figure 2.7: Schematic cutaway top view of the Pockels cell driver housing showing compartmented structure and DVM board. O-ring sealed acrylic oil enclosures shown in white. Circles are O-ring sealed oil fill holes.

Chapter 3

RESULTS

3.1 Electrical Pulse Measurements

Electrical measurements of avalanche transistor pulser output waveforms are difficult to make accurately, due to the conflicting physical requirements of high speed (small size, low impedances) and high voltage probes (large clearances, high impedances). An industry-standard Tektronix P6015A high voltage probe was used extensively for development and testing of the Pockels cell drivers, however its 75 MHz bandwidth and large physical size rendered it unable to fully resolve the high speed transitions produced by the drivers. The P6015A was also unsuitable for probing within the avalanche transistor strings themselves, as the probe's impedance would disrupt the off-state voltage balance among the transistors. Any imbalance potentially lead to uncontrolled self-triggering, with occasionally catastrophic results.

The use of the first-stage impedance matching resistors (RE1a and RE1b in Figure 2.4) as current-viewing resistors was suggested by Fulkerson et al. [12]. Such an approach indeed proves highly informative, although ultimately insufficient for resolving the behaviour of the string in sufficient detail beyond the first few stages. The use of a small loop of wire as a B-field probe allows more localized probing of currents, however this approach is extremely sensitive to the exact position of the probe in four dimensions (X, Y, Z, and rotation), producing results that were not repeatable enough for meaningful comparisons. In addition, the probe tip needs to be quite close to the circuit traces and components, and capacitive coupling to the probe tip

both introduces distortion and raises the risk of short circuits. Although an improved B-field probe design and fixture would likely mitigate those difficulties, a new measurement method utilizing the electric field component was developed instead. This method is described below.

The avalanche transistor strings are constructed completely from surface mount components and laid out in a linear manner, such that the wavefront is initiated at one end and propagates in a straight line towards the output end. The printed circuit layout is only on the top layer, with the bottom layer consisting of ground plane in direct contact with the thick aluminium heatsink plate. This allowed the construction of a carriage assembly that rode along the plate while maintaining a low-inductance ground via wide-area wiping contacts. Two insulated probe tips were mounted to the carriage, suspended several mm above the strings of avalanche transistors that comprised both 100 ohm paralleled switch stacks. The carriage was then methodically moved to clearly marked positions above each stage, and traces recorded on a 1 GHz oscilloscope. The probe tips connected to the oscilloscope's 50 ohm inputs via 50 ohm double-shielded coaxial cables of the same length, within 1 cm. The oscilloscope was triggered from same TTL level trigger pulse that initiated switching. In this manner, it was possible to make repeatable, directly comparable measurements of the switching of the avalanche transistor stacks.

In Figure 3.1, intensity corresponds to relative dV/dt in arbitrary units, with darker colors represent higher dV/dt. The figure allows direct comparisons of the "collapse" of the avalanche transistor chain vs. time between the two paralleled 100 ohm halves of one switch. The horizontal axes are time with an arbitrary zero. The vertical axis corresponds to stage number, which is roughly analogous to physical distance between each stage. The stages are not uniformly spaced, however the variation is small and does not cause difficulty interpreting the plot.

In the upper plot, pulse propagation starts at the top left and proceeds downward

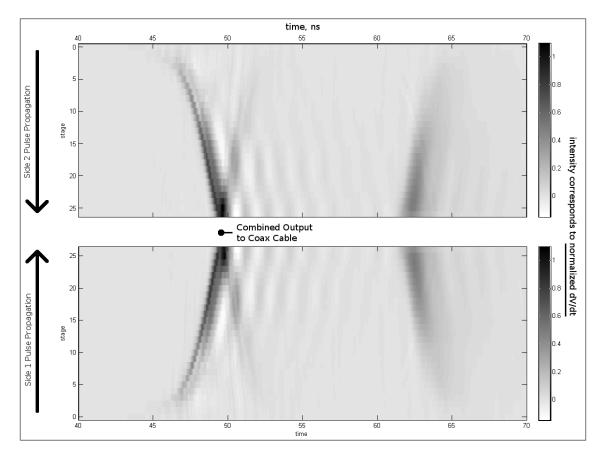


Figure 3.1: Normalized intensity plot of dV/dt at each stage for both avalanche strings in one half of a dual switch pulser. In each pane, the left-most dark band represents sequential conduction of the transistor string, propagating from trigger at upper and lower left corners to the common output at center. Pulse collision from the opposite transistor string and impedance mismatch at board-to-cable transition, as well as other discontinuities, result in identifiable back-propagating reflections. Differences in propagation velocities through air, FR4 epoxy-fiberglass, and lumped elements are visible. The rightmost dark band is the reflection from cable end returning to switch stacks; propagation is in reverse direction. Switch voltage is 8 kV. Load is 4 feet of open-ended RG223 50 ohm cable. Darker colors correspond to higher dV/dt. Time is measured from input trigger pulse.

(increasing distance and stage number), while in the lower plot propagation starts at the bottom left and propagates upward (increasing distance and stage number). The two pulses meet at the cable connection near the center. The vertical gap between the two plots roughly corresponds to the electrical distance between the output ends of the two 100 ohm stacks. The two plots appear nearly identical, indicating that very good matching has been achieved between the two paralleled strings.

Examining Figure 3.1, the base-triggered first stages (Y=0) switch near the upper and lower left corners of the plots, near the 43 ns mark. There the dV/dt is relatively low due to the large capacitance of the stage, and is not easily discernible in the graph. The second stage self-triggers approximately at the 44.5 ns mark, and the third near 45.5 ns. Switching of each stage proceeds with increasing rapidity until the wavefront is propagating down the chain at nearly the velocity of a freely propagating pulse, creating the dark band that slopes towards the cable output near the center of the figure.

As the pulse exits each string, slight mismatches allow a small portion to enter the opposite string, and some reflection from the imperfect junction with the coaxial output cable is produced. These undesired signals are apparent as faint bands sloping in the opposite direction. The slope is proportional to the velocity of propagation, with nearly vertical slopes indicating propagation through air directly from the radiating source to the probe, and slightly less vertical slopes propagating through the FR4 dielectric. Non-linear slopes with a faint "hook" near the lower numbered stages propagate through the discrete elements of each string. These interpretations have been verified to a first order through modeling.

The rightmost dark band represents the pulse returning from reflection at the open end of the RG223 output cable. At this point all the transistors are "on", and the reflected pulse propagates smoothly into the decreasing impedance of the switch stack pair. The lack of re-reflection indicates that the distributed resistances present

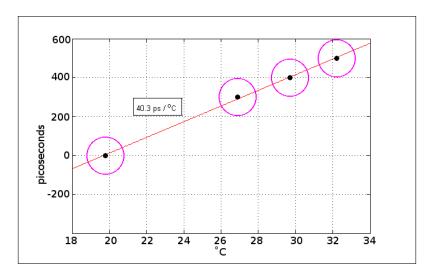


Figure 3.2: Input-to-output propagation delay change vs. temperature for one half of a dual switch pulser. Linear fit gives $40.3ps/^{o}C$ temperature drift coefficient.

at each stage are permitting the switch stack to function as a proper termination.

3.2 Jitter and Drift Measurements

Thermal drift was measured by comparing input-to-output propagation delay before and after heating a complete Pockels cell driver unit by more than 10 degrees Celsius. Temperature was measured with an RTD temperature probe at multiple points on the aluminium enclosure, as well as the internal heatsink plate upon which both channel's high voltage switch boards are mounted. Heat was applied over roughly half an hour, then shut off and ample time given to allow reasonable thermal equilibrium. When all points indicated within $0.1^{\circ}C$, the driver was enabled and propagation delay measurements were recorded. Additional points were recorded as the driver gradually cooled back to ambient. The thermal drift coefficient was found to be $40.3ps/^{\circ}C$ by a linear fit of points (Figure 3.2).

As mentioned in Section 2.2.4, the input-to-output propagation delay shifts with bias voltage. The high voltage power supply module used in the Pockels cell driver is

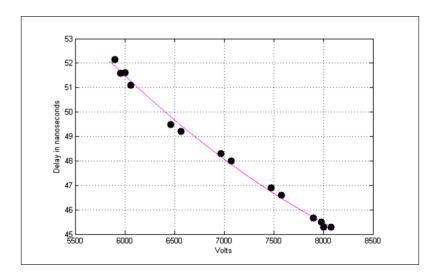


Figure 3.3: Typical input-to-output propagation delay vs. bias voltage for one half of a dual switch pulser.

specified for 0.02% stability over an 8 hour period, after a 30 minute warm-up time, or less than 2 volts. Measuring the change in propagation delay with voltage allows the stability over time to be estimated. In addition, the timing shift associated with user adjustments to the bias voltage can be easily determined. A graph of typical input-to-output propagation delay vs. bias voltage in shown in Figure 3.3. The delay coefficient was calculated by differentiating a quadratic fit of the data, and varies from $\approx 2.2ps/V$ at 8 kV bias voltage to $\approx 3.85ps/V$ at 6 kV bias. The expected drift over 8 hours time due to the high voltage power supply is therefore less than 8 ps after the 30 minute warm-up time, assuming the temperature remains constant.

The driver's jitter is low enough that it is difficult to separate it's performance from systemic measurement errors, such as oscilloscope triggering uncertainty. However, the jitter has been observed to be substantially less than 100 ps with the use of an appropriate trigger signal. For the current design, an "appropriate" trigger signal is a 0 to 4 V TTL-like signal with 10% to 90% rise and fall times of less than 4 ns.

3.3 Optical Measurements

Optical window measurements were performed using a 1030 nm Yb:KYW modelocked laser with an Impact13 KD*P Pockels cell placed between crossed polarisers and connected to the dual-channel Pockels cell driver via 1.2 m high voltage coaxial cables (Figure 2.1). The window width was set to 10 ns by using a Stanford Research Systems DG535 delay generator to produce the triggers for each channel of the Pockels cell driver. Since the 200 fs laser pulse was much narrower than the 10 ns window width, a "walking window" approach was used. A fast diode detector was placed after the output polariser, and the timing of the Pockels cell driver trigger window was shifted in relation to the laser pulse to "walk" the window across the pulse in 100 ps steps. At each time step, the peak photodiode signal was recorded. The oscilloscope recording the detector output was synchronized to the generation of the original laser pulse. The Pockels cell was adjusted for maximum contrast before beginning the test. In order to reduce the noise floor of the detector, several shots were averaged for each point. The photodetector zero offset was measured several times during the test run by blocking the beam, and this "floor" was subtracted from the measurements.

The resulting optical window is shown in Figure 3.4. The graph has been normalized such that peak maximum detector amplitude corresponds to 1.0. However, laser output power was uncontrolled, allowing laser power drift to introduce a slight slope in the resulting window profile. 10% to 90% optical transition times of approximately 1.4 ns were observed, with nearly symmetrical rising and falling edges.

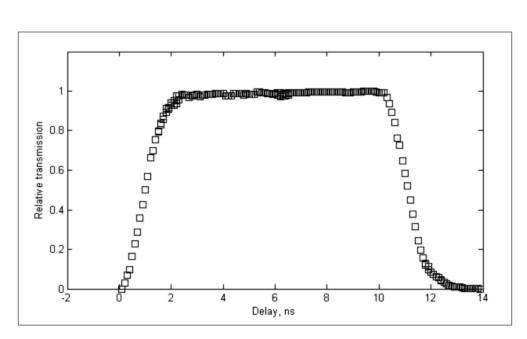


Figure 3.4: Relative transmission through Impact13 Pockels cell placed between crossed polarisers. Half-wave mode, $8~\rm kV$, $1030~\rm nm$. Uncorrected for laser power drift during measurements.

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