



# SerIOS: Enhancing Hardware Security in Integrated Optoelectronic Systems

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## ABSTRACT

Silicon photonics (SiPh) has different applications, from enabling fast and high-bandwidth communication for high-performance computing systems to realizing energy-efficient optical computation for AI hardware accelerators. However, integrating SiPh with electronic sub-systems can introduce new security vulnerabilities that cannot be adequately addressed using existing hardware security solutions for electronic systems. This paper introduces SerIOS, the first framework aimed at enhancing hardware security in optoelectronic systems by leveraging the unique properties of optical lithography. SerIOS employs cryptographic keys generated based on imperfections in the optical lithography process and an online detection mechanism to detect attacks. Simulation and synthesis results demonstrate SerIOS's effectiveness in detecting and preventing attacks, with a small area footprint of less than 15% and a 100% detection rate across various attack scenarios and optoelectronic architectures, including photonic AI accelerators.

## CCS CONCEPTS

- **Hardware** → **Emerging optical and photonic technologies;**
- **Security and privacy** → **Embedded systems security; Intrusion detection systems.**

## KEYWORDS

Integrated Photonics, Security, Hardware, PUF

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## 1 INTRODUCTION

Silicon photonic (SiPh) integrated circuits and interconnects exploit the fast throughput of light-speed data transmission to realize ultra-high bandwidth communication with low-power dissipation in high-performance computing systems. In any optoelectronic

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system, such as an electronically programmable SiPh neural networks, the integration (i.e., monolithic, intra-chip, or inter-chip) of electronic and photonic sub-systems is necessary to deal with signals from different domains (i.e., optical and electrical). Such an integration also requires signal conversions and adaptations, as well as SiPh node reconfiguration for routing and computation [1].

Systems integrating different technologies (e.g., an optoelectronic system) are more susceptible to malicious attacks where data can be stolen or system's normal behavior can be impacted [2]. Attacks can be inserted by hardware Trojans (HT), which are malicious pieces of hardware designed to mischievously act and interfere with the targeted system. The impacts of attacks can include data leakage and manipulation, service and sleep-denial, irreversible losses, systemic abnormal behavior, and permanent breakdown [3].

In optoelectronic systems with SiPh and CMOS electronic integration, attackers can take advantage of multiple signal conversions required to exchange data between the two domains and act on the integration interfaces. Furthermore, as the optical transmission behavior is directly related to SiPh device design characteristics (e.g., a waveguide width) and temperature, minimal changes in these characteristics can affect the transmission quality, where attackers have different ways to interfere with the underlying SiPh circuit. For example, considering the thermal sensitivity of SiPh devices, in the photonic accelerator proposed in [4], an attacker (e.g., an IP integrated in the system) can increase its own temperature (e.g., by performing heavy mathematical operations). Consequently, this can impose thermal crosstalk [5], generating noise or affect the neighboring SiPh devices (e.g., by imposing phase noise or frequency deviations) in proximity.

Existing techniques to address purely electronic hardware Trojan (e-HT) attacks might be explored for optoelectronic systems, but most will fail to address the hardware security concerns in optoelectronic systems [6]. While e-HTs target the IPs and electrical paths, optical HTs (o-HTs) target the optoelectronic interfaces and introduce disturbances to the SiPh sub-system. Prior efforts such as [2] took a step further on presenting solutions to enhance the security of optoelectronic systems by taking into account the characteristics of the underlying optical path, adding an extra layer of security to the system design. However, these solutions are still limited because of their complex integration methods, limited applicability, and dependence on electronic sub-systems.

The novel contribution in this paper is on developing the first framework for enhancing hardware Security in Integrated Optoelectronic Systems, called SerIOS. SerIOS is designed to benefit from the unique characteristics of optical lithography processes to create

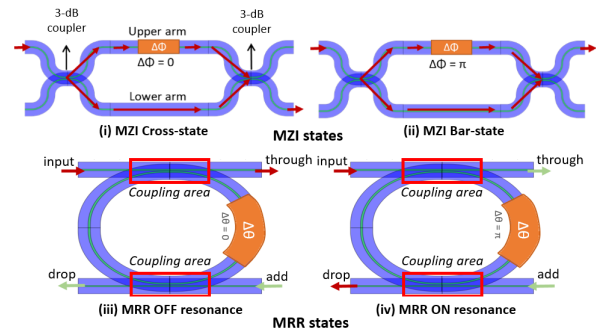
unique seeds to generate unique keys. Furthermore, SerIOS interacts directly with the SiPh sub-system to enhance the signal transmission quality (e.g., by reducing noise). By dynamically analyzing transmitted optical power in the output, SerIOS is capable of detecting disturbances on an optical channel. Compared to similar prior efforts—such as [2], which benefits from physical unclonable functions (PUFs) and lithography process characteristics—SerIOS stands as the only solution that does not rely on error-prone off-line analyses, nor complex neural networks for pattern recognition. Results, obtained from both simulation and FPGA prototyping, show that the online detection method has an area overhead of less than 15% when the entire system’s implementation (i.e., IPs, interface controllers, and SerIOS) is considered. Reported power consumption for target FPGA is as low as 200 mW and real-time executing latency is about 200 ns. More importantly, when randomly inserting o-HTs on a system for creating different attacks such as black-hole, sink-hole, and flooding, we show that SerIOS can achieve 100% attack detection during runtime.

## 2 BACKGROUND AND RELATED WORK

### 2.1 Silicon Photonic Devices and Configuration

Mach–Zehnder interferometers (MZIs) and microring resonators (MRRs) are commonly used building blocks in optoelectronic systems. Fig. 1 illustrates conventional MZI and MRR designs. MZIs are interferometric devices that consist of two 3-dB couplers and phase shifters on the arms [7]. By applying a phase shift, the optical signals passing through the MZI arms can experience destructive or constructive interference. For example, in the 2×2 MZI shown in Fig. 1, a phase difference of 0 results in constructive interference (Cross state), while a phase difference of  $\pi$  leads to destructive interference (Bar state). Intermediate phase differences allow the signal to be split between output ports. MZIs find applications in optical switched networks and SiPh neural networks [4]. MRRs are compact optical resonators formed by a closed loop waveguide, where light can be trapped and resonantly coupled. They can be used for filtering, modulation, and switching functionalities in optoelectronic systems. MRRs are particularly useful in wavelength division multiplexing (WDM) systems and integrated photonic circuits. These devices, MZIs and MRRs, play important roles in various optoelectronic applications, providing functionalities such as interference-based signal manipulation, wavelength filtering, and routing [8].

SiPh nodes operate based on their parameter configuration, which includes induced optical phase and tuned resonant wavelengths. These parameters can be dynamically and electronically adjusted to meet the requirements of the application. Usually, the controller node connects to each SiPh node and configures its operation accordingly. In the context of a coherent SiPh neural network [9], the underlying SiPh nodes (e.g., MZIs in [9]) are adjusted in terms of optical phases by the electronic controller. These phase values represent the weight parameters in the neural network and can be determined using training and decomposition algorithms [4]. The electronic controller, designed for specific target applications, performs the necessary actions to achieve the desired system functionality [1]. It interacts with the SiPh sub-system through electro-optic interfaces, utilizing methods like thermal tuning (e.g.,



**Figure 1: SiPh building blocks. MZI in two operation states: (i) Cross and (ii) Bar. MRR in two operation states: (iii) OFF resonance and (iv) ON resonance.**

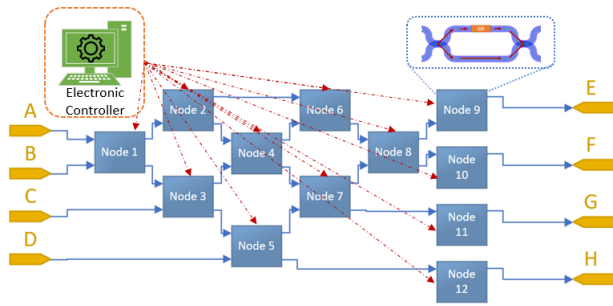
microheaters) or carrier injection (e.g., PN junctions). For instance, by applying a specific voltage to a microheater placed on top of an MZI arm (Fig. 1, an electronic controller can configure the SiPh sub-system to alter the optical signal phase in the MZI.

### 2.2 Fabrication-Process Variations in Silicon Photonics

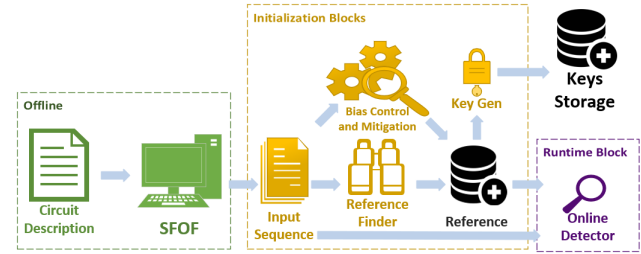
Critical dimensions like width and thickness in SiPh devices, such as MZIs and MRRs, are affected by fabrication-process variations (PVs), leading to performance impact. PVs introduce deviations in power and phase output, compromising the behavior of SiPh sub-systems [10]. Systematic and random PVs pose challenges for accurate modeling, requiring runtime compensation solutions like active bias control [11]. SiPh waveguide thickness, MRR response, and directional couplers are affected by PVs, causing malfunctions and performance degradation [10]. To mitigate PV impact, statistical modeling during the design phase or runtime approaches like dynamic bias control are employed [12]. In SerIOS, we propose a real-time integrated method to detect and correct intentional deviations and attacks, reducing errors in optoelectronic systems.

### 2.3 Physically Unclonable Functions (PUFs)

A physical unclonable function is a component that utilizes the inherent randomness introduced during circuit manufacturing to generate a unique fingerprint for a physical entity [13]. In the case of fabricated SiPh circuits, variations in their parameters and performance, as discussed in Section 2.2, result from unpredictable factors such as random physical deviations. When designing SiPh-based PUFs, there are different approaches to consider. Some works, such as [14], focus on designing SiPh sub-systems specifically engineered to produce PUFs. Another approach is to utilize the impact of PVs on the SiPh sub-system, such as optical interconnects and accelerators, and extract the unique characteristics of transmitted signals (e.g., optical intensity) to create PUFs. SerIOS adopts the latter approach, avoiding the need to modify the SiPh sub-system with specific PUF modules.



(a) An optical linear multiplier based on MZI nodes to perform optical-domain matrix-vector multiplication [9].



(b) An overview of different building blocks in SerIOS.

Figure 2: (a) SiPh optical linear multiplier and (b) SerIOS overview.

## 2.4 Security Breaches and Threat Models in Optoelectronic Systems

Threats to optoelectronic systems can arise from both software and hardware components. The hardware block can be compromised by a Hardware Trojan (HT) designed to maliciously impact the system. These HTs can be inserted by a malicious engineer during the design phase or in compromised foundries by modifying the design layouts. Software attacks can originate from infected IPs integrated with the SiPh sub-system. HT attacks on an optoelectronic system typically involve four phases: Design Phase, Activation Phase, Operation Phase, and Idle Phase [15].

We consider HTs introduced in the foundry, affecting the entire system. Malicious applications at the IP level can also introduce various types of attacks. Side-channel attacks exploit one-way interference to cause information leakage by analyzing the impact of interference on the system. As an example architecture, we consider the SiPh-based optical multiplier depicted in Fig. 2(a), based on the accelerator architecture proposed in [9]. Each SiPh node is based on MZI, similar to the one shown in Fig. 1. The architecture includes connections between nodes, I/Os, and an electronic controller connected to each MZI node. In this system, attackers can launch attacks from different perspectives. For example, a neighboring IP integrated with the SiPh sub-system can manipulate the signal phase values by increasing its temperature and affecting the nearby SiPh MZIs. In the presence of a HT, the propagation direction of the optical signals can be manipulated, thereby altering the signal phase values. These attacks directly impact the output readings, leading to interference with the application behavior and potentially degrading system performance. Such deviations can lower the system's inferring accuracy [16].

To mitigate these attacks, various solutions can be employed, such as fingerprinting and active detection mechanisms. In SerIOS, we adopt an online detection strategy where a baseline system operation is established. Periodic verification is performed on the SiPh sub-system to ensure its security and correctness.

## 3 SerIOS SECURITY FRAMEWORK

Security in Integrated Optoelectronic Systems (SerIOS) framework, enables an online detection of anomalies on the SiPh sub-system and provides a method for unique cryptographic key generation

and proper tuning of the underlying SiPh devices. It operates as a standalone hardware unit, enabling agnostic surveillance of the SiPh sub-system. Due to its modular design, SerIOS can be easily integrated with FPGA designs as a security layer.

Fig. 2(b) shows a global overview of the different building blocks and integrated modules in SerIOS. SerIOS execution is divided between offline, initialization blocks, and runtime blocks. Initialization and runtime blocks are the hardware blocks that constitute SerIOS, while offline execution is performed during design time and is not part of the integrated hardware blocks. Initialization blocks are executed once during system initialization and then are put in idle, while runtime blocks are responsible for attack detection. The rest of this section describes the different building blocks of SerIOS.

### 3.1 Straightforward Order Finder

The Straightforward Order Finder (*SFOF*) analyzes the SiPh sub-system, looking for the correct tuning order of SiPh devices and nodes. This order is important because, as the optical signal travels through the SiPh sub-system, the effects of PVs will be accumulated through each subsequent SiPh node on the path. For instance, considering Fig. 2(a) and input A, SiPh node 1 deviations will affect not only node 1, but also subsequent SiPh nodes to its right (e.g., if we consider MZIs in Bar state in all the nodes, the following nodes will be affected: 1, 2, 4, 6, 8, and 9). This way, *SFOF* works based on a high-level description of the circuit and simulates the possible routes and paths to establish the optimized detection order.

*SFOF* performs two main tasks: sequence generation and finding baseline communication patterns. For the **sequence generation**, *SFOF* analyzes the SiPh sub-system topology based on the high-level circuit description. It determines the sequences that the Bias control and mitigation module should follow to find the readjusting tuning parameters of the SiPh nodes during runtime. To find the sequence, *SFOF* simulates the SiPh sub-system offline by emulating SiPh node transmissions while changing the tuning/configuration parameters of each node. The simulation is performed in reverse order, from the rightmost to the leftmost SiPh nodes, to capture the transmission path of each node based on the output triggered by that node. The generated sequence includes tuples of "node-output(s)" associations, capturing the relationships between nodes and the affected outputs.

**Listing 1: SerIOS BCM execution flow.**

```

1 tuningValue = [0]*numberOfNodes
2 for each node i in SiP_Circuit:
3     outputPort = affectedPort(node_i)
4     referenceMetric = nodeMetric(outputPort)
5     tuningValue[node_i] += 1
6     while referenceMetric < nodeMetric(outputPort):
7         tuningValue[node_i] += 1
8     saveValue(node_i, tuningValue[node_i])

```

For the **Baseline Communication Patterns**, SFOF identifies the communication patterns used later by the Reference Finder. It aims to find a set of communication pairs where each input is associated with at least one output. These patterns reflect the passive behavior of the SiPh sub-system when nodes are not tuned. For example, in the circuit of Fig. 2(a), assuming each SiPh node connects its inputs straight to its outputs (nodes in Bar state), the identified communication patterns are input A triggering output E, input B triggering output G, input C triggering output F, and input D triggering output H. These patterns represent the expected behavior of the SiPh sub-system and serve as a reference for detecting anomalies.

The goal of SFOF is to reduce runtime complexity and logic hardware overhead. By performing offline analysis and storing relevant information in a secure memory, SFOF facilitates its integration with the target system while minimizing runtime processing. However, these offline steps are not mandatory during design time and can be integrated into SerIOS initialization blocks for analysis during the initialization process, albeit resulting in longer initialization time.

### 3.2 Bias Control and Mitigation Unit

In SerIOS, the *Bias Control and Mitigation (BCM)* module is utilized to determine the appropriate configuration parameters for each SiPh node, taking into account the impact of PVs. The BCM module continuously monitors the operation of nodes within the SiPh sub-system and dynamically adjusts the node tuning parameters to compensate for the effects of PVs during runtime. While the BCM module can also address thermal variations, this work focuses specifically on PVs. The configuration parameters chosen by the designer, such as current/voltage requirements or phase shifts, are individually adjusted for each SiPh node. Real-time readings from the output ports, specifically the photodetector readings, are used to identify the optimal configuration values that mitigate the influence of PVs. It is important to note that SerIOS does not require readings from every individual node but relies on output port readings to achieve its objectives.

The BCM module in SerIOS is fed by the *Input Sequence* generated by the SFOF block. It collects relevant information and incorporates it into the online blocks to optimize their operation and reduce overhead. Pseudo-code for the BCM module is provided in Listing 1. The module iterates through each node, noting the affected port(s) based on the SFOF sequencer, and the desired metric (e.g., phase shift) on those port(s). Next, the module incrementally increases the metric under evaluation by its minimal step (e.g., incrementing the temperature by 0.1° C for a microheater) and assesses the resulting output of the SiPh sub-system. This process is repeated until a defined condition is met, which could be a predetermined

optical power requirement on an output port. The tuning value obtained during this procedure is then stored in the *References* database. This initialization process considers the conditions, such as temperature, at the time of execution. If these conditions change, the same procedure can be repeated to update the tuning values accordingly.

### 3.3 Unique Key Generation

The module responsible for key generation takes as input the values annotated by the BCM module and utilizes mixing functions to create unique keys. This is possible because the PV-induced deviations in the SiPh sub-system are unique, resulting in unique tuning values (as discussed in Section 2.2). The validation functions used are designed for simple *hardware* implementation, requiring minimal resources and relying on shift and logical operations only.

The **key uniqueness** is ensured by the nature of PVs in SiPh integrated circuits, as extensively analyzed and quantified in prior work [17]. PVs introduce unpredictable changes to the circuit, leading to unpredictable system behaviors. As discussed in Section 3.2, the impact of PVs can be directly observed in the transmitted signals, which can be measured during runtime and are unique to each SiPh sub-system. The keys are generated based on these unique and unpredictable changes. Since these variations differ from one SiPh node to another (even within the same device, such as the two arms of an MZI), each circuit composed of a series of these nodes will have a unique set of variations and affected behavior. As demonstrated in previous work [13], leveraging these unique PVs for each circuit allows the generation of unique seeds, thereby justifying the reliability of the keys.

For the **key generation** process, shift and logical operators are used to simplify the hardware implementation. These functions can be easily modified and function as standalone blocks. An example of key generation function is  $h(x) \leftarrow \forall b_i, b_i \neq b_{(i+1)}, XOR(b_i, b_{i-1}) \ll OR(b_i, b_{i+1})$ , where each bit of a tuning parameter is evaluated, and their concatenation is performed using defined logical functions. Despite its simplicity, this function can generate unique keys thanks to the unique input seed used.

In SerIOS, different keys are generated using different functions and stored in the *Secure Storage*. The *Secure Storage* can be an isolated memory accessible only by SerIOS or a memory with additional security layers [18]. SerIOS can generate keys dynamically during runtime, considering the low latency overhead. The *Key Gen* module creates keys for each communicating pair, allowing IPs to encrypt their transmissions. The number of keys generated and their usage can vary based on application requirements. SerIOS can generate keys based on implemented functions and different input seeds. Simple key generation functions are used to minimize hardware and execution overhead. In the studies conducted, one key function per transmitting pair was used, generating keys once and storing them. However, key generation can be done differently, such as generating keys each time they are used or using the same function for multiple scenarios. The security relies on the uniqueness of the seed. Implementing different functions has negligible impact on hardware and execution time. The key generation functions are designed to be simple, using basic operators, and their footprint is small compared to the entire SerIOS circuitry.

**Listing 2: SerIOS online detection execution flow.**

```

1 for each pattern i in referenceValues:
2   outputPort = affectedPort(pattern_i)
3   reference = referenceValues(pattern_i)
4   config = configuration(pattern_i)
5   configureCircuit(config)
6   reading = readMetric(outputPort)
7   if difference(reference, reading) > threshold:
8     reportIssue(pattern_i)

```

This is why a function per transmitting pair was chosen, providing flexibility without significant overhead.

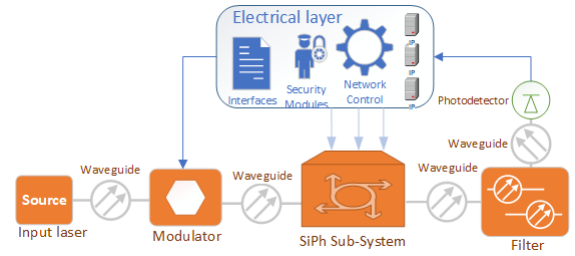
### 3.4 Golden Values

SerIOS’s detection mechanism utilizes baseline execution scenarios, known as *golden values*, which are defined during the design phase. These scenarios provide predetermined operational conditions, inputs, outputs, and configuration parameters. During system initialization, SerIOS captures these golden values by executing the predefined scenarios generated by the SFOF block, as discussed in Section 3.1. By configuring the SiPh sub-system accordingly, SerIOS obtains readings of optical signal powers and phases. Executing this step during system initialization ensures the isolation of the SiPh sub-system from other IPs, minimizing potential interference and preserving the integrity of the readings. While it is possible to repeat this step if the SiPh sub-system undergoes rearrangement, such as node failure or deactivation, re-initializing the sub-system with the same parameters is not explored in this paper. The focus of this work is on obtaining the initial golden values for future reference, rather than addressing specific scenarios of reconfiguration.

### 3.5 Online Detection Methodology

The online detection mechanism in SerIOS can be configured to operate continuously in parallel with ongoing transmissions or at predefined intervals. In this paper, the online detection is executed at specific intervals. To ensure compatibility with regular system operation, the same transmission wavelength is used for both data transmission and checking. This allows the system to verify different scenarios within the same wavelength band. The pseudo-code in Listing 2 outlines the methodology of the online detection module. It compares runtime readings with the reference values stored in the *reference* database. The module iterates through each stored scenario, replicating the same inputs and following the same SiPh sub-system path. The output port used for comparison is also the same. If the difference between the new reading and the corresponding golden value exceeds a predefined threshold, SerIOS triggers an alarm to indicate an unusual situation. The threshold can be defined based on application-specific metrics, such as precision reduction in a multiplier circuit or the signal-to-noise ratio (SNR) at the SiPh sub-system output in a communication context.

To ensure the validity of readings and comparisons, the threshold should not be affected by external factors. For example, in a multiplier circuit, the MZI phases and inputs are used to establish the threshold, isolating it from potential external influences. However, it should be noted that thermal variations in the SiPh circuit can still result in false positives, impacting system operation. One possible solution to detect and adapt to temperature variations is to employ MRR-based thermal sensing, as described in [6]. This



**Figure 3: Validation environment presenting the main blocks composing the testbed.**

technique estimates temperature variance and considers its impact on the readings. However, mitigating thermal variations is not the primary focus of this work. Additionally, white noise attacks can interfere with the accuracy of the results. Nevertheless, SerIOS, being aware of the nature of such attacks and the original state of the circuit, can identify them as threats and report them accordingly.

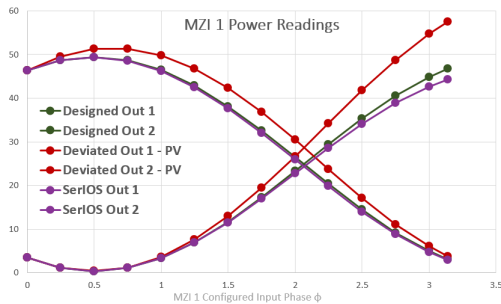
## 4 RESULTS AND DISCUSSIONS

In this section, we consider different case studies to verify various aspects of SerIOS, based on different attacks that impact the system differently: **Black-hole**: The SiPh node is configured in such a way that all traffic is dropped; **Sink-hole**: All transmission is directed to a target node, saturating the transmission; **Flooding**: Non-stop inputs flood the optical channels, compromising the transmission; **Rerouting**: The SiPh nodes’ tuning parameters are altered to route the transmission differently; and, **IP Hick-jacking**: An IP integrated to the SiPh sub-system maliciously interferes with it (i.e., increasing its own temperature). Lumerical Interconnect [19] is used for modeling and simulation of the case studies. The evaluation scenarios are designed to simulate the validation platform presented in Fig. 3. To insert the variations on SiPh nodes, we have used canonical random generators to emulate the impacts of PVs for each node.

### 4.1 SerIOS Validation

To illustrate SerIOS flow and performance, we use the SiPh sub-system presented in Fig. 2(a) for discussion. SiPh nodes are manipulated—e.g., MZI nodes are modified such that the phase shifter operates wrongly, emulating variations—and the affected output signals are measured. The SiPh sub-system in Fig. 2(a) is composed of 12 identical MZIs, similar to the one presented in Fig. 1. To control each MZI, a phase shifter is used. Fig 4 presents the optical power readings for one out of the 12 MZIs in the SiPh sub-system in Fig. 2(a), chosen arbitrarily to illustrate SerIOS impact on the node tuning. As it can be seen, SerIOS’ tuned outputs are much closer to the ideal ones, when compared with deviated outputs.

Bias control and mitigation and initial analysis are executed once during system initialization, and hence the latency of these do not impact execution time. The execution time to perform these initial steps is directly related to the evaluation of configuration parameters and the number of SiPh nodes that has to be analyzed. Another aspect affecting the latency is the delay for opto-electrical interface conversions. Furthermore, the delay for SiPh node stabilization after tuning should be considered. Accordingly, the overall latency can be modeled as  $t_{run}(i) = \sum_0^n \rho \cdot (v + \zeta)$ , in which  $\rho$  is the number of executions needed for the used configuration parameter,  $v$  is the



**Figure 4: Optical output readings for one MZI (Nodes 1, considered as an example) composing the architecture in Fig. 2(a).**

delay for SiPh node stabilization,  $\zeta$  is the opto-electrical conversion delay, and  $n$  is the total number of reconfigurable SiPh nodes in the system. Taking as an example the circuit in Fig. 2(a), if the tuned parameter is the phase change and the phases window varies from  $-\pi$  to  $\pi$  in intervals of 0.1 rad, 629 different values should be verified for each one of the MZI nodes (7548 in total). Assuming the MZI switch time of 6 ns [1] and the opto-electrical conversion delay of 4 ns (one clock cycle in our validation environment), the overall latency to find the SiPh sub-system tuning parameters is 75.48  $\mu$ s. Note that the module execution time can be ignored as it can execute in parallel with the signal converters and during stabilization time.

Next, golden values are collected. In this case, four transmission scenarios (i.e., four different phase configurations for the MZIs) are used as the configuration baseline. These scenarios are randomly chosen and each configuration parameter is arbitrarily chosen. For the creation of unique seeds, values collected by the *BCM* unit are used. In this validation scenario, we have opted to create four different seeds, one associated with each input. This way, four seeds and four key-creation equations are used. Generated keys are internally stored within SerIOS and will be used later for encrypting the transmitted signals. For evaluating SerIOS performance and detection mechanism, we have manually inserted different types of attacks in the system, as presented in the introduction of this section. We insert each of these attacks at an arbitrary simulation time and verify SerIOS' responses. Table 1 illustrates the output readings for each scenario, as well as the expected readings. As it can be seen, each attack interferes in a different manner with the SiPh sub-system. With this information, SerIOS is able to detect the anomaly and detect a possible attack situation. Encrypting messages with they generated keys, SerIOS protected transmissions against eavesdropping and spoofing attacks. PRBS sequences were used to validate it, where even for situations when attackers could retrieve the transmitted information, it was encrypted and hence useless to the attacker.

## 4.2 SerIOS Detection Efficiency and Overhead

We evaluate SerIOS using different photonic switch architectures [20] [21] ranging in size from  $2 \times 2$  to  $12 \times 12$ , as well as state-of-the-art optical neural network architectures [9][4][22]. To generate the scenarios, we use canonical random generators to introduce variations in the system and simulate the impact of attacks. We focus on

**Table 1: Impacts on the output readings for SerIOS attacks detection. Each attack interferes with different output readings. The number in parentheses show the targeted SiPh node.**

	Outputs (dBm)			
	E	F	G	H
<b>Golden Value</b>	29.46	30.57	28.60	34.60
<b>Black-hole (4)</b>	26.67	31.84	31.02	34.60
<b>Sink-hole (5)</b>	25.54	27.73	23.36	39.12
<b>Flooding (1)</b>	29.19	31.60	28.59	34.03
<b>Rerouting (9)</b>	0.0	30.57	28.60	34.60
<b>IP Hijacking</b>	30.17	30.68	26.87	34.70

the direct consequences and outcomes of the attacks on the SiPh sub-system rather than the underlying causes. Each scenario is simulated 100 times to ensure accuracy and stability in the performance of SerIOS modules.

**4.2.1 HT Attacks and Detection.** For evaluating the runtime detection efficiency of SerIOS, five attack scenarios are created using a random seed. These attacks simulate the impact of malicious nodes on the circuit. The SiPh sub-systems are modified to include the following attacks: black-hole, sink-hole, flooding, IP hijacking, and rerouting. Rather than having continuous attacks, each attack is randomly triggered to affect the SiPh sub-system. This creates asynchronous behaviors, emulating attackers that act under certain conditions. To achieve this, an execution window is defined (e.g., 10 seconds of system execution), and attacks are randomly triggered within this window. This means that an attack can occur at any time, multiple times during each window.

During both automated and manual tests, SerIOS successfully detects 100% of the anomalies. False positives can happen, and acknowledging that it could lead to unwanted alarms, a solution to detect and adapt to the temperature variation is to use MRR-based thermal sensing [6]. It's important to note that SerIOS does not precisely locate the exact SiPh node under attack. The goal of SerIOS is to be agnostic to access and configuration controls of the SiPh sub-system, such as a network routing controller for a SiPh network sub-system. However, by integrating a network routing controller and configuring different transmission setups, it becomes possible to isolate and identify the specific node causing the issue by transmitting data while avoiding that node.

**4.2.2 Overhead Analysis.** As most of the processing in SerIOS is performed offline by *SFOF*, the integrated modules remain simple circuits and can be scaled up for large-scale SiPh sub-systems (i.e., larger number of integrated nodes). The information for the golden values can be stored in a few registers and the remaining information locally within the integrated circuit. To evaluate the area overhead, two different scenarios are considered: first, SerIOS integration with an electronic controller and as part of an integrated system (i.e., a system-on-chip (SoC)); second, SerIOS scalability considering a higher number of I/Os and SiPh nodes in the circuit. For this, [20, 21] switch architectures with sizes varying from  $2 \times 2$  to  $12 \times 12$ , and optical neural network architectures presented in [4, 9, 22] are considered. SerIOS is synthesized for Xilinx Kintex 7 FPGA with a target 4 ns clock period for all the designs. Optimization was set to balance between area and speed.

Table 2 shows SerIOS SoC integration with an electronic controller [23] and low-area processing IPs [24]. As illustrated, the

**Table 2: SerIOS SoC integration footprint analysis. FPGA LUT and Flip-flop usage is considered for SerIOS, an electronic controller [23], and a processing core [24].**

	Integrated System Area Overhead			
	SerIOS	Others	Total	%
SerIOS + [23]	1811	1695	3506	51 %
SerIOS + [23] + [24]	1811	9587	11398	15 %

footprint to integrate SerIOS accounts for less than 15% of the entire system. Considering SerIOS scalability, Table 3 presents the synthesis results for different SerIOS configurations as well as the static and dynamic power consumption. Different SiPh switch fabric circuits are used where the overhead increases with the number of secured nodes as well as with the number of I/Os. This is due to the fact that SerIOS stores the golden values for each I/O transmission pair which grows with the number of I/Os.

To evaluate execution time overhead, three modules should be considered: the *BCM*, the *online detection*, and the *key generation*. The *BCM* latency is observed only during system initialization, as this module is not to be executed continuously. Nevertheless, if it is to re-execute for a given reason (i.e., system re-calibration),  $t_{tun}(i) = \sum_0^n \rho \cdot (v + \zeta)$  can be used to compute the execution time. Concerning the *key generation*, in our studies, thanks to the fact that simple operators are used, the *key generation* takes one clock cycle per function (i.e., in our environment, each clock cycle is 4 ns). For the *online detection*, its execution overhead is related to the number of I/Os such as that the same communication combinations found by *SFOF* (see Section 3.1) are used. Accordingly, SerIOS latency can be defined as  $t_{det} = \sum_0^n \iota + v + \zeta$ , where  $v$  is the SiPh node stabilization time,  $\zeta$  is the opto-electrical conversion time,  $n$  is the number of communication combinations, and  $\iota$  is the time overhead to access the golden value storage (i.e., *Reference* database). Taking as an example the circuit in Fig. 2(a), assuming the MZI stabilization delay is 6 ns and the opto-electrical conversion takes 4 ns, and considering four communication combinations and the delay to access the golden values to be two clock cycles (i.e., using our environment, each clock cycle is 4 ns), the total time to check the system is 228 ns (i.e., 57 clock cycles).

## 5 CONCLUSION

Silicon photonics (SiPh) is emerging to boost the communication and computation performance in high-performance computing systems. Nevertheless, SiPh and CMOS electronic integration opens new doors for attackers, making the optoelectronic systems prone to security attacks. This work presented a novel framework comprising security breaches detection allied with mitigation techniques for process variations in optoelectronic systems. The proposed *Security in Integrated Optoelectronic Systems (SerIOS)* framework enables real-time detection and unique key generation for encryption algorithms. Results showed that SerIOS is able to dynamically evaluate SiPh nodes and properly set the tuning parameters for each of them. Furthermore, SerIOS real-time detection demonstrated 100% detection of test cases during execution time. This work shows the importance of hardware security in emerging optoelectronic systems and highlights the need for interdisciplinary research efforts to address security concerns in such systems.

**Table 3: SerIOS scalability analysis. FPGA LUT and Flip-flop (FF) usage is considered for SerIOS as it scales with the SiPh sub-system.**

	SerIOS Scalability Analysis				
	I/Os	Nodes	LUTs	FFs	Power (mW)
SiPh SW [21]	4	5	843	972	215
SiPh SW [20]	4	6	822	989	216
SiPh ACC [9]	4	12	1107	1158	202
SiPh ACC [22]	4	10	1081	1124	201
SiPh SW [20]	6	12	1795	2239	247
SiPh ACC [4]	9	36	4814	7069	442
SiPh SW [20]	12	28	7100	10817	610

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