DISSERTATION

# BACK-CONTACT LAYERS ON CdTe SOLAR CELLS AND LOSS ANALYSIS OF TOP-PERFORMING DEVICES

Submitted by

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ABSTRACT

BACK-CONTACT LAYERS ON CdTe SOLAR CELLS AND LOSS ANALYSIS OF TOP-PERFORMING DEVICES

Photovoltaic technologies provide a nearly infinite energy source and have become cost competitive in recent years, driving them to be the most installed energy source. Cadmium telluride (CdTe) thin-film photovoltaics has the advantage of a well matched energy band-gap to the solar spectrum, as well as rapid production capabilities, making it the second most adopted solar-energy technology. Relatively low realized power conversion efficiencies, with the record being 23.1% (compared to the limit of 33%), has held CdTe back from expanding its market share. For comparison, silicon photovoltaics has reached an efficiency of 26.6% and has ∼95% of the solar energy market share. The limited efficiency for CdTe is attributed in large part to the voltage deficit, which is a problem CdTe researcher have struggled with for years. Analysis to better understand the loss contributions in CdTe, and other technologies, as well as the addition of back-buffer layers will be presented in this work.

Understanding the losses limiting solar-cell performance is essential to determining pathways to increased efficiencies. Comparisons to the theoretical limits of different parameters, which vary depending on the band-gap of the absorbing material, show which parameters cause different devices to have the most loss in efficiency, and thus the most room for improvement. These comparisons are done on record-efficiency devices, both single and multi-junction, from different technologies to determine which technologies have the most room for efficiency growth, and what parameter is the limiting factor.

Detailed diode analysis was done to quantify the parasitic losses that negatively impact device performance. Determining these parameters produced valuable information from current-voltage data that is already available, allowing for more comparisons to be made when investigating the losses for different devices. Fill-factor losses were further analyzed

using the diode parameters. The losses in fill-factor were quantified by splitting the total loss into its different diode parameter contributions. This detailed diode and fill-factor analysis gave a better understanding of what parameters caused the larger losses in photovoltaic devices. The results of this analysis on the best single-junction cells from different technologies, different CdTe laboratories, and for CdTe record devices over time are discussed.

In addition to detailed loss analysis, back-buffer layers for CdTe devices were also investigated. A deposited layer of tellurium oxide was added to the native oxide present on the CdTe in the device structure as a dopant free passivating layer. Including a second $CdCl_2$ passivation treatment was found to be crucial for good performance from the tellurium-oxide devices. Copper-doping treatments negatively impacted the device performance when additional tellurium oxide was included, with temperature-dependent current-voltage measurements suggesting the formation of an energy barrier which limited performance. Photoluminescence measurements on tellurium-oxide devices showed the impact of high-temperature treatments on absorbers with dopants already present, and the formation of defect states after an energetic sputtering deposition.

Cadmium zinc telluride was also investigated as an electron-reflection layer to reduce recombination at the back surface. Optimization of the CdZnTe layer, including doping and substrate temperature, was investigated to create the best possible devices. Photoluminescence measurements, and the fact that devices including the CdZnTe layer outperformed control devices, indicated reduced recombination at the back surface. Film characterization measurements showed small crystal formation in the CdZnTe layer which highlights the importance of doping in this layer to improve conductivity for hole extraction. Experiments on First Solar absorbers again showed the impact that high-temperature processes can have on previously doped absorbers. The limitations of these back-contact layers are discussed, along with suggestions for future research to overcome them.

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# Chapter 1

INTRODUCTION

## 1.1 Status of World Energy

World energy consumption has increased ever since the industrial revolution. Historically, this energy demand has been satisfied by fossil-fuel sources such as coal, oil, and recently natural gas. These resources have multiple problems associated with them, including the harmful impacts of climate change caused by green house gas emissions and the fundamental limitation of these resources being finite [1, 2]. The greenhouse gas emissions that come from the use of fossil fuels have been attributed not only to the increase in average earth temperature, but also to poor air qualities that have harmful impacts on human health [3].

As the demand for energy consumption continues to grow, alternative methods of power generation have been developed to meet energy demand without the negative effects to climate change. These renewable energy technologies include geothermal, wind, hydro, and photovoltaics. In recent years the majority of new energy installations in the world has come from renewable energy, with 56% of these coming from photovoltaics in 2022 [4]. Despite growing efforts and installations, only 12% of global energy produced in 2022 comes from wind and photovoltaics. One driving force behind the success of photovoltaics in recent years is the large reduction in cost, where its levelized cost of energy (LCOE) has been reduced to under 10¢ per kilowatt-hour in utility scale markets as shown in Fig. 1.1 [5].

Not only is solar energy cost competitive with the historic fossil fuels, but it is also renewable and widely available as shown in Fig. 1.2. Fossil fuels have only a finite amount of energy available, whereas renewables such as solar will not run out, even with large increases in energy demand. In order for the world to continue meeting the growing energy

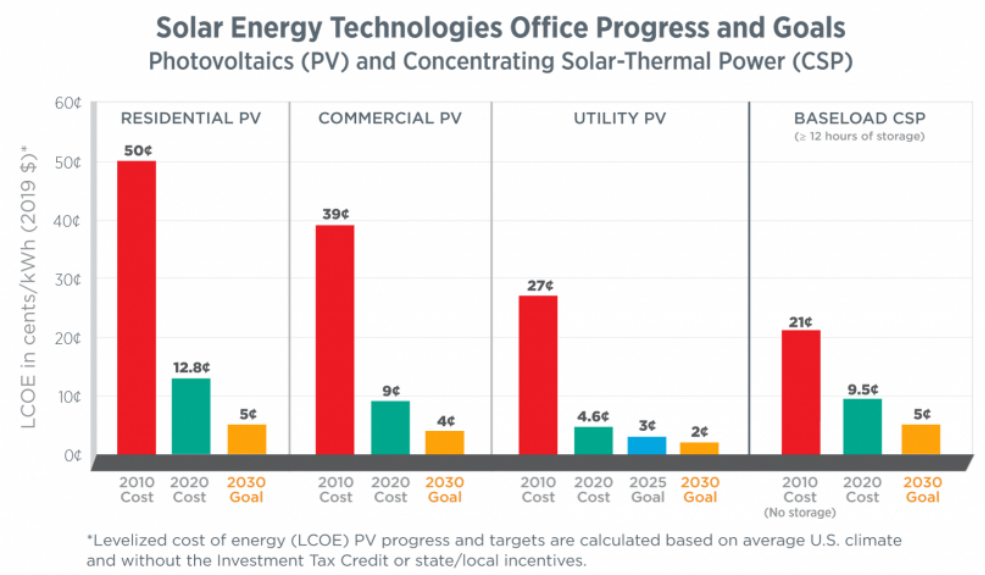


**Figure 1.1:** The Levelized cost of energy for different photovoltaic markets. Taken from [5]

demand while combating climate change, renewable technologies will be required to work together. In this renewable collaboration photovoltaics will play a major role.

## 1.2 Photovoltaic Technologies

The photovoltaic effect was discovered in 1839 by Edmond Becquerel showing that a voltage can be formed in material when exposed to solar radiation [6, 7]. About 40 years later in 1883 Charles Fritts constructed the first functioning solar cell [6, 7]. This solar cell was less than 1% efficient and used selenium as the absorber layer. The first practical silicon solar cells were developed by bell labs in 1954 [7]. Due to low efficiencies and high cost, only niche applications, such as powering spacecraft, were the initial uses for solar cells.

Photovoltaics has seen remarkable improvement since then with record single-junction devices reaching up to 29.1% efficiency [8]. With this increase of efficiency, the world has also seen a very large increase in commercial use. Solar modules now are not only used for space applications, but also for personal homes, utility scale power farms, and many new niche applications such as agrivoltaics. These different applications tend to use different solar technologies that utilize various different materials. Silicon dominates the market share,

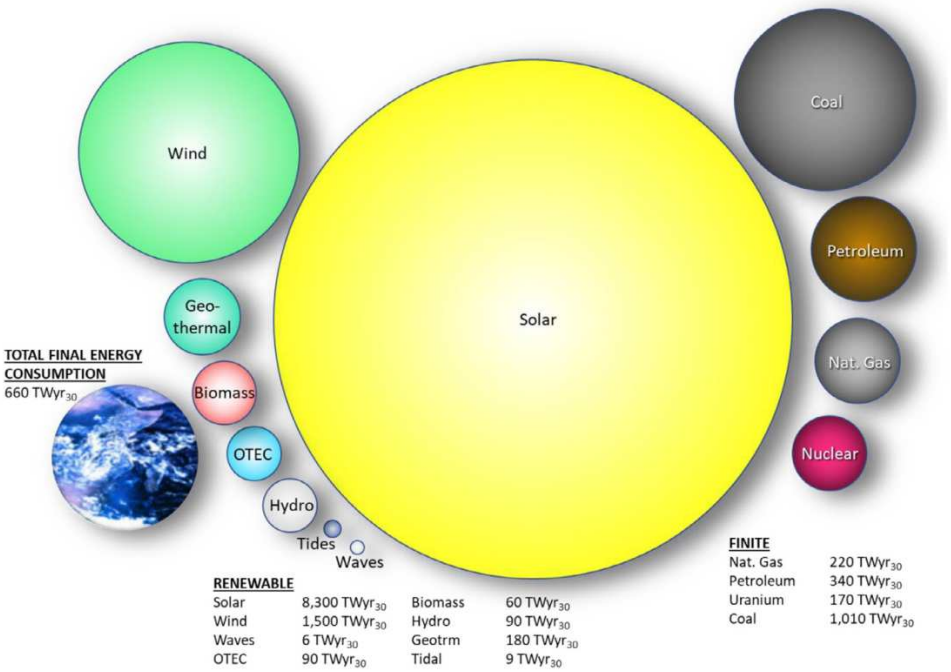


**Figure 1.2:** Energy availability from different renewable and finite energy sources. Taken from [2].

producing ∼90% of the world's photovoltaic energy. The highest efficiency material gallium arsenide (GaAs) is only used at any scale in tandem applications with other semiconductors for space applications due to the high cost of the fabrication process. Thin-film technologies like cadmium telluride (CdTe) and copper indium gallium selenide (CIGS) have lower power conversion efficiency (PCE), but their rapid production capabilities allow for high throughput and cheaper modules [9].

There are also emerging materials and technologies that show promise as photovoltaic research continues to move forward. Perovskites are a thin-film material that produces high efficiencies and allows for control of the band-gap of the absorber, making it an attractive candidate for tandem applications [10]. Tandem solar cells are more complicated to fabricate, and thus more expensive, but can produce a higher efficiency. This makes them highly attractive for space applications and for cost reduction research going forward.

Photovoltaics has grown to the point where many technologies are used both in research and in commercial applications. They all utilize the same fundamental physics in order to extract power from incoming sunlight.

## 1.3 Cadmium Telluride Technology

Cadmium telluride, generally including some degree of alloying with selenium, is a thin-film technology with record devices reaching 23.1% PCE and modules, produced by the company First Solar, greater than 19% [11, 12]. Due to CdTe having a direct band-gap, device absorbers are only a few micrometers thick as opposed to Si devices that have wafers on the order of millimeters [13]. This allows CdTe to use relatively small amounts of material to produce modules and allows CdTe to have a shorter energy payback time [14]. The thin-film nature of CdTe allows for rapid production capabilities using various physical vapor deposition (PVD) techniques. These production capabilities allow for low cost modules and help make CdTe a prime candidate for the growing energy demand.

The direct band-gap of approximately 1.4 eV, when incorporating selenium as all modern designs do, is closely matched to the AM 1.5G solar spectrum. This allows CdTe to have one of the highest theoretical efficiencies possible at $\sim 33\%$ [15]. Despite the high theoretical limit, often called the Shockley-Queisser limit, CdTe has a somewhat lower device efficiency than many of its competitors. This differential is often attributed to the open-circuit voltage $V_{oc}$ parameter having had limited improvement in recent years and remaining well below the theoretical limit [16, 17]. This work focuses on improving CdTe device efficiencies by introducing changes to back buffer layers as well as comparing CdTe's performance to other technologies in an effort to shed light on the cause of efficiency losses.

# Chapter 2

BACKGROUND

## 2.1 Semiconductor Fundamentals

Semiconductor physics is essential for photovoltaic device operation. Semiconductors consist of a repeating crystal lattice of atoms that are highly structured with closely-spaced electron states. When atoms are brought together into a crystal lattice, the overlapping electron orbitals form a continuous energy band rather than individual levels. Due to the Pauli Exclusion Principle, electrons in this lattice fill the allowed energy states up to a certain energy, the Fermi energy $E_F$ which is defined as the energy level at which there is a 50% chance of the state being occupied by an electron [18]. As temperature increases, the energy of electrons changes leading to the Fermi-Dirac energy distribution function in Eqn. 2.1 where k is Boltzmann's constant and T is the temperature in Kelvin.

$$f(E) = \frac{1}{1 + \exp\left(E - E_F\right)/kT} \tag{2.1}$$

When an energy band is fully occupied, electrons are not able to move freely, but when the Fermi-level is within a band, as is the case for metals due to the overlapping bands making one continuous band, electrons are able to flow freely [13]. In an insulator material there is a large energy gap, called the band gap, between the bands such that almost no electrons can be thermally excited to the higher band, and thus one band is fully occupied and the other is empty of electrons. In this case, the Fermi-level is placed between the energy bands in the forbidden energy region. Semiconductor materials have a smaller band gap such that it is possible for some electrons to be thermally excited into the upper energy band, called the conduction band. Once in the conduction band the electron is free to move, allowing

for a current to be produced. The ability for electrons to be excited across the band-gap is what constitutes a semiconductor and is essential for photovoltaic device function.

The last band filled with electrons is called the valence band. The energy between the highest energy state in the valence band and the lowest state in the conduction band is defined as the band gap of the material. When an electron is excited to the conduction band, it leaves behind an empty energy state. This empty energy state behaves the same as a positively charged electron and is referred to as a hole in the semiconductor community. Holes are free to move within the valence band just as electrons are in the conduction band and both of these carriers are crucial to solar-cell function.

### 2.1.1 Carrier Concentrations and Doping

The carrier density in a material depends directly on the energetic location of the Fermi-level. The closer the Fermi-level is to the conduction band, the more electron carriers will be present and visa versa for hole carriers. The carrier density for electrons, n, and holes, p, are given by:

$$n = N_C exp(-\frac{E_C - E_F}{kT}) \tag{2.2}$$

$$p = N_V exp(-\frac{E_F - E_V}{kT}) \tag{2.3}$$

where $N_C$ and $N_V$ are the density of states in the conduction and valence band respectively described by:

$$N_C = 2(\frac{2\pi m_e^* kT}{h^2})^{3/2} \tag{2.4}$$

$$N_V = 2(\frac{2\pi m_e^* kT}{h^2})^{3/2} \tag{2.5}$$

where $m_e^*$ and $m_h^*$ are the effective electron and hole mass respectively and h is Plank's constant.

The carrier density within each band is very important for solar cell design and function. One method used to control the carrier density within semiconductors is referred to as doping. Doping is the process of purposefully replacing atoms within the crystal lattice with a different element to introduce an extra electron, for n-type doping, or hole, for p-type

doping. N-type doping occurs when an atom with an extra electron is placed within the lattice. The other electrons bind with the neighboring atoms, but the extra electron will remain nearly unbounded. This doping leads to an energy state just within the band-gap so that the electron is easily thermally excitable to become a carrier in the conduction band. P-type doping follows this same process but with an atom containing one less electron than the lattice atoms.

When a lattice is free from dopant impurities it is referred to as an intrinsic material, as opposed to an n-type or p-type material. This generally means the Fermi-level of the material is close to the center of the forbidden energy region. In a non-degenerate semiconductor, which is defined as having a doping concentration far below the density of states in the conduction band [9], the intrinsic carrier density is always equal to the product of hole and electron carriers as shown here:

$$pn = n_i^2 \tag{2.6}$$

All materials discussed in this thesis are considered to be non-degenerate semiconductor and thus follow the relationship laid out in equation 2.6.

The doping process shifts the Fermi-level closer to the valence band for the case of p-type doping, or to the conduction band for n-type doping. This introduction of carriers and the shifting of the Fermi-level is very important in photovoltaic device physics. In practice, introducing dopants into the lattice does not necessarily mean that additional carriers will be activated. In current CdTe devices, dopant activation is less than 10% [19, 20] with most devices being closer to 1%. Increasing this activation ratio is an active area of research that is beyond the scope of this thesis. It is mentioned because non-activated dopants can lead to defect states within the band gap that result in a reduction in performance.

### 2.1.2 Recombination and Carrier Transport

When electrons are excited from the valence band into the conduction band they are in a meta-stable state. They will eventually decay back down to the valence band releasing

energy as either heat or as a photon. This decay is known as recombination, which can only occur when an electron and a hole are in the same location. There are three main types of recombination: radiative, defect-assisted, and Augur. Radiative recombination occurs when an electron goes straight from the conduction band to the valence band releasing energy as a photon with the energy of the band-gap. This photon can then be reabsorbed to excite a new electron, so radiative recombination is often not a major concern for solar cell research. Defect-assisted recombination, also known as non-radiative recombination, occurs when a carrier becomes trapped by a defect state within the band-gap and the oppositely charged carrier also moves to the same defect state causing recombination. This process releases either heat or two photons of lower energy than the band-gap that have insufficient energy to be reabsorbed and are considered a loss. In Augur recombination the energy from recombination is given to an electron already in the conduction band, which then immediately relaxes down to the conduction band-edge releasing that energy as heat resulting in an efficiency loss. Augur recombination occurs when there is either high doping concentrations or high injection which is not a usual concern for current CdTe solar cells.

The average amount of time a carrier stays in an excited state is called the carrier lifetime, which is crucial to carrier transport. Excited carriers are free to move throughout the cell by two main mechanisms, drift and diffusion. When carriers are generated near the front of the absorber, which is the case for most solar cells, there is an uneven distribution of carrier throughout the absorber. These carriers then spread out through the diffusion process and generate a current defined by:

$$J_n = qD_n\frac{d\Delta n}{dx} \quad \text{and} \quad J_p = -qD_p\frac{d\Delta p}{dx} \tag{2.7}$$

where D is the diffusion constant defined by:

$$D_n = (\frac{kT}{q})\mu_n \quad \text{and} \quad D_p = (\frac{kT}{q})\mu_p \tag{2.8}$$

where $\mu$ is the carrier mobility, which is affected by things such as scattering and impurity density. The diffusion constant and the carrier lifetime, $\tau$ determined by the minority carrier,

are used to define a diffusion length:

$$L_d = \sqrt{D\tau} \tag{2.9}$$

Physically, the diffusion length is the average distance an excited minority carrier will diffuse through the material before recombination occurs.

The other carrier transport mechanism is drift, which is driven by the electric field strength ($\mathcal{E}$) and restricted by the carrier mobility ($\mu$) resulting in an average drift velocity:

$$\nu_d = \mu\mathcal{E} \tag{2.10}$$

Considering both electron and hole mobilities, the current due to drift is:

$$J_{drift} = q(\mu_n n + \mu_p p)\mathcal{E} \tag{2.11}$$

The sum of the drift and diffusion currents is the total current through a region of the solar cell. Generally, drift will be the stronger component at locations with stronger electric fields such as diode junctions.

Other contributors to carrier transport and current flow are thermionic emission and tunneling. Thermionic emission occurs when there is an energy barrier in the device as depicted in Fig. 2.1. A barrier like this limits current flow and requires the carrier to have thermal energy to overcome the barrier. The current that overcomes the barrier is given by:

$$J = A^* T^2 exp(-\frac{q\Phi_B}{kT}) \tag{2.12}$$

where $\Phi_B$ is the barrier height and $A^*$ is known as the Richardson constant. Tunneling is the transport mechanism where the carrier goes through a thin energy barrier rather than over it. This requires the energy barrier to be very thin, generally on the order of a few nanometers. While thermionic emission over barriers harm solar cell performance, tunneling can be purposefully incorporated into the device design for various reasons.

### 2.1.3 P-N Junction

Doping and carrier transport are both important aspects of semiconductors and are used to form a p-n junction. When and n-type and p-type semiconductor are brought into contact,

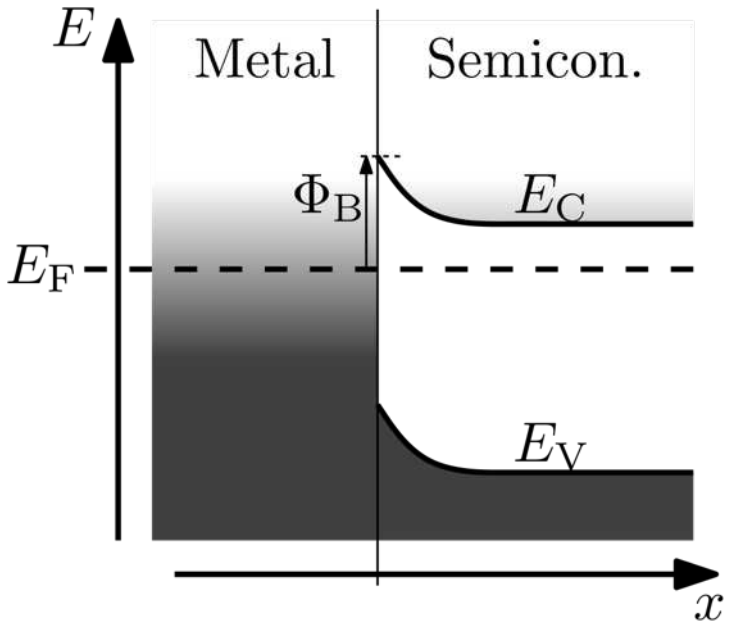


**Figure 2.1:** An example of the formation of an energy barrier when a semiconductor is brought into contact with a metal.

electrons and holes will move via diffusion to the opposite side of the device, leaving behind negative and positive ion cores in the process. Since these ion cores in the lattice have opposite charges they cause an electric potential to form, which affects the movement of the electrons and holes and results in what is called the built in potential, $\Psi_{bi}$:

$$\Psi_{bi} = \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{2.13}$$

When two materials are brought together and are in equilibrium, the Fermi-level must remain constant throughout the device. In order to compensate for this, the energy bands shift, resulting in band-bending and a gradient in the band diagram as shown in Fig. 2.2.

This band-bending represents the built in electric field in the p-n junction and leads to electrons in the region being swept to the n-type and holes to the p-type side. This gradient region is called the depletion region due to the electric field depleting the region of carriers. The section of flat bands is called the quasi-neutral region (QNR) because there is no electric

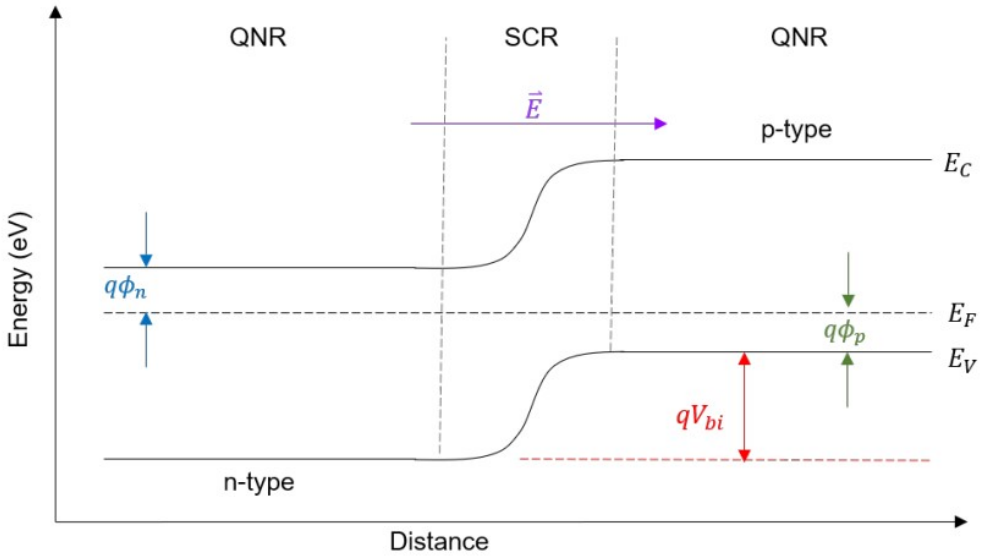


**Figure 2.2:** Band diagram of a p-n junction showing the depletion region, or space-charge region (SCR), and quasi-neutral regions (QNR). $\Phi_p$ and $\Phi_n$ represent energy difference between the Fermi-level and the valence and conduction bands respectively.

field and carriers move only though diffusion. The length of the QNR is important to carrier extraction because on average the carriers will only move a single diffusion length, $L_d$, before recombination. The length of the depletion region depends on the dopant density and the built in voltage:

$$W_D = \sqrt{\frac{2\varepsilon_s}{qN}(\Psi_{bi} - \frac{2kT}{q})} \tag{2.14}$$

Where $\varepsilon_s$ is the permittivity of the semiconductor and N is either $N_A$ or $N_D$ depending on which is larger.

### 2.1.4 Diode Equation

Carrier transport in the depletion region is dominated by drift, whereas in the QNR, it is dominated by diffusion. When not under equilibrium conditions, such as an applied voltage or under illumination, the band diagram differs from Fig. 2.2 causing the drift and diffusion currents to no longer be balanced and a net current to flow. The total current flow for an

ideal diode depends on the doping profile and assumptions are made to find a solution. The major assumptions are a constant doping profile, and the depletion approximation, which assumes that the electric field ends abruptly and is contained in the depletion region. Using these assumptions, the total current becomes:

$$J = J_p + J_n = J_o(\exp(\frac{qV}{kT}) - 1) \tag{2.15}$$

where $J_0$ is the saturation current, which is the value the current saturates at in reverse current. Equation 2.15 is known as the Shockley equation, or the ideal-diode law.

When under illumination carrier generation and recombination must be taken into account. This generally increases the carriers moving in the device, increasing the current. This light generated current must be taken into account in the diode equation which becomes:

$$J = J_o(\exp(\frac{qV}{kT}) - 1) - J_L \tag{2.16}$$

where $J_L$ is the light generated current.

This is an idealized equation for the current flow in a diode. When incorporating parasitic and recombination losses Eqn. 2.17 becomes:

$$J = J_o\exp[(\frac{q}{AkT})(V - RJ)] + GV - J_L \tag{2.17}$$

where R is the series resistance, G is the shunt conductance in appropriate units, and A is the diode quality factor, which is a recombination-related loss parameter. Use of the ideal-diode equation shows how the current coming out of a solar cell should behave and can provide insight into what is limiting performance.

## 2.2 CdTe Solar-Cell Structure

CdTe solar cells of commercial interest are thin-film devices deposited on a glass substrate. The glass substrate has a conductive coating to function as one electrical contact, while the last deposited layer will be a metal, or other conductive material, to be the other

electrical contact as shown in Fig. 2.3. In between it is typical to have an n-type buffer layer, approximately 100 nm thick, to help create the p-n junction and to reduce interface defect states. The absorber is generally a graded cadmium selenium telluride (CdSeTe)/CdTe bi-layer, a few micrometers thick, usually p-type doping at the rear of the absorber. CdTe devices are poly-crystalline in structure, and in order to get meaningful performance out of the device, a passivating $CdCl_2$ treatment is performed. This treatment is used to passivate grain boundary defect states and to increase the CdTe grain sizes [21, 22]. After the passivation step there is generally a thinner hole-selective layer meant to help extract holes out the back of the device. In many cases there is also a p-type doping treatment done at the back of the absorber and on the hole-selective layer to improve carrier concentration and hole extraction. The device is finished with a metal or other conductive electrode to establish an electrical contact as shown in Fig. 2.3.

Due to the direct band-gap of the CdTe absorber, the device can be quite thin, on the order of a few micrometers. This requires the device layers to be constructed by types of various physical vapor deposition, and it allows industrial modules to be constructed all on one conveyor belt. These depositions include close-space sublimation, thermal evaporation, and radio frequency sputtering, which are all used in device fabrication at Colorado State University (CSU).

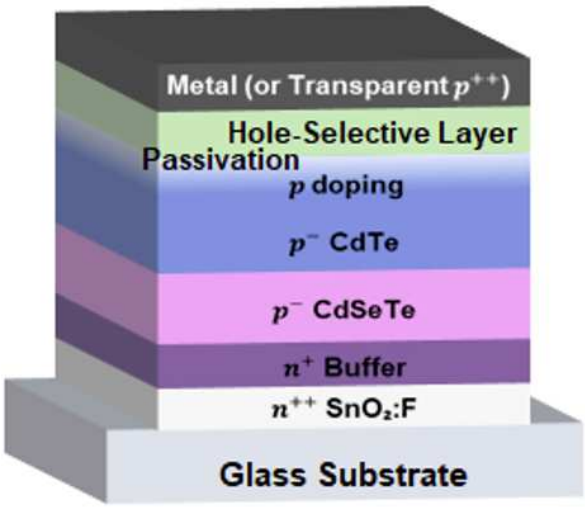


**Figure 2.3:** Generic CdTe device structure showing doping level and buffer layers.

### 2.2.1 Close-Space Sublimation

The main deposition system at CSU is known as the advanced research deposition system (ARDS), which deposits via close-space sublimation (CSS). This system has nine process stations, as shown in Fig. 2.4, to deposit layers and allow treatments without breaking vacuum.

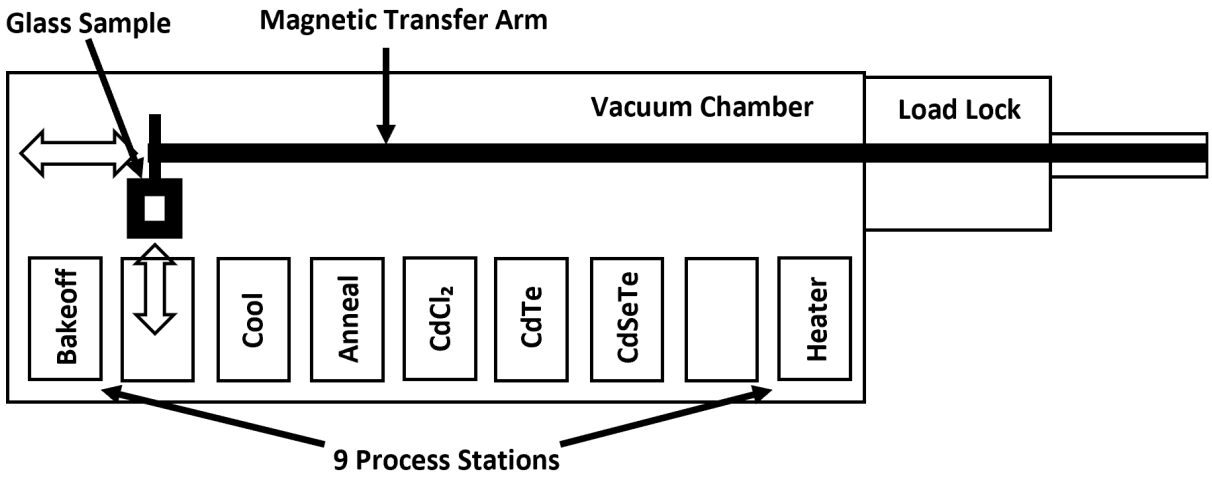


**Figure 2.4:** Diagram of the advanced research deposition system showing the transfer arm, sample holder, and different deposition stations.

The source holder is filled with the deposition material and is placed between a top and bottom heater. These heaters are controlled separately so that a temperature gradient is created. The substrate, in a holding arm, is exposed to the material facing downward so the material sublimates upward, following the temperature gradient. As the sublimated material comes into contact with the substrate, which is already preheated, it sticks to the surface and builds up the absorber layer. The $CdCl_2$ treatment does not deposit a layer, but the chlorine moves between the grain boundaries such that the absorber thickness does not change after this treatment. Chambers for pre-heating, annealing, and cooling are also available in the ARDS.

### 2.2.2 Thermal Evaporation

Thermal evaporation involves placing material in a conductive holder, in this case facing upward. A substrate is placed above the holder some distance facing downward. Once the background vacuum is at a low enough pressure, usually $\sim 10^{-5}$ Torr, an electrical current is passed though the holder heating the material. Once the material is hot enough it will begin to sublimate upward and adhere to the substrate creating the film. This method generally has a crystal quartz monitor active in the system to have real time monitoring of the deposition rate and total thickness of the deposition. At CSU, it has been only used for one of the thin back buffer layers present in devices, but the National Renewable Energy Lab (NREL) uses it for the absorber deposition.

One advantage of this deposition technique is the ability to co-deposit material. This is when two separate materials, such as CdTe and CdSe separately, are placed in different holders. The current to each holder is controlled separately and allows for control of the composition of a ternary compound layer, such as CdSeTe, and control of the composition and deposition rate.

### 2.2.3 Sputtering

Sputtering is a technique that uses ionic bombardment to eject atoms from a target to deposit on a substrate. The material being deposited is packed into a dense disc called the target which, at CSU, is placed facing upward and connected to a cathode. The substrate is placed above the target near the anode. When the power supply is turned on, the background gas becomes ionized creating a plasma. These ions are attracted to the negatively charged cathode and rapidly move towards it, smashing into it. This collision transfers energy to a target atom, ejecting it in a random radial direction, with some of the atoms going upward to adhere to the substrate creating a film. The plasma is often contained and shaped by magnetic fields to improve collision efficiency and deposition rate as shown in Fig. 2.5.

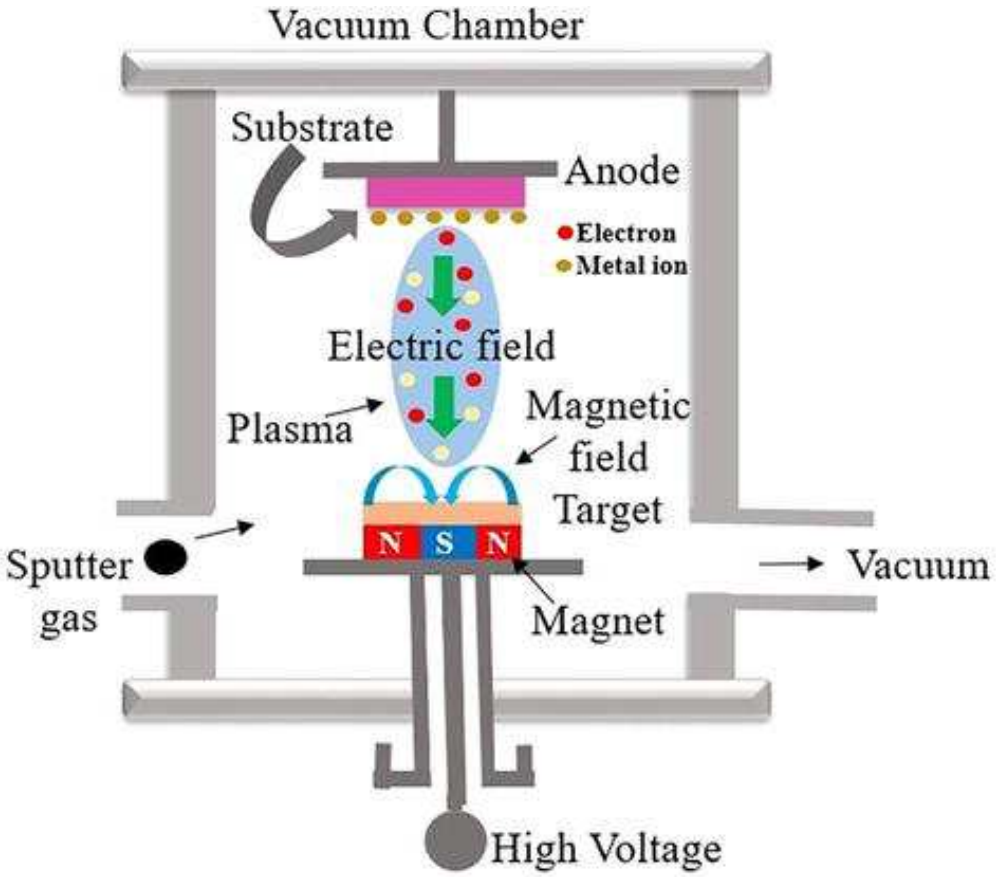


**Figure 2.5:** Diagram of a magnetron sputtering system including plasma field and magnetic field. Figure from [23].

One problem that can arise with direct-current (DC) sputtering, especially with oxides, is a charge buildup on the target surface. To avoid this issue, the most common sputtering technique used for semiconductors is radio-frequency (RF) sputtering. Instead of applying a direct current to the target, an alternating current, typically at 13.56 MHz, is applied to the target. This allows for any charge build up to dissipate before causing problems with the deposition process. Some sputter chambers also allow for dry etching of the substrate, where a small voltage is applied to the substrate allowing for the plasma to sputter the substrate, rather than the target, before the deposition. This is used to clean the substrate surface of any oxidation or other surface material that may cause performance issues.

One advantage of sputtering is the option of co-sputtering two targets at once. This allows different compositional mixes to be tested in experiments. Reactive sputtering is also

a popular use of the sputtering deposition. This is when a reactive gas, such as oxygen, is mixed into the plasma along with the typical argon to create a chemical reaction during the flight time to the substrate. This can be used to create an oxide film on the surface, such as tellurium oxide. Reactive sputtering does, however, require RF sputtering to avoid charge buildup from the reactive gas.

One issue that comes up with sputtering techniques is that it is a highly energetic. In order for target atoms to reach the substrate it must have sufficient kinetic energy, and often the atoms still have a notable amount of energy when they reach the substrate. This energy can damage the interface creating defect states that are undesirable. In production, which must have rapid depositions, this is a major concern. The power applied must be high to eject many target atoms, but this leads to performance issues in devices. Nevertheless sputtering is commonly used in industry depositions, namely for films less than 25 nm thick due to the relatively slow deposition rate of sputtering.

### 2.2.4 Completed Devices

The standard device fabricated at CSU uses all the deposition methods mentioned above. The glass substrate used has a thin layer of fluorine-doped tin oxide as a transparent-conductive-oxide (TCO) contact. The high band-gap of the TCO allows light to pass though without unwanted absorption and thus is used as a front contact that allows most light to pass through to the semiconductor absorber. In this case, devices are in a superstrate configuration where the light passes through the glass before getting to the device as opposed to a substrate configuration where light first goes through the film before the glass [24]. The TCO used in CSU samples has a low sheet resistance of $10 - 12\ \Omega/\text{cm}^2$ to minimize the resistive effect on device performance. A $\sim$100 nm layer of magnesium zinc oxide (MZO), with approximately 8% zinc concentration by weight, is RF sputter deposited onto the TCO to act as an n-type buffer layer with the front contact. This is done by reactive sputtering with argon as the background gas and 3% oxygen as the reactive gas.

The substrate is then taken to the ARDS to deposit, by CSS, the absorber layers and the cadmium chloride ($CdCl_2$) passivation treatment. A 0.5 μm ternary compound of cadmium selenium telluride (CdSeTe), with $\sim$ 30% Se compared to Se + Te, is deposited as the first section of the absorber. This is followed by a $1-3$ μm layer of CdTe. The absorber is then given the $CdCl_2$ passivation treatment which helps passivate grain boundaries and increases grain sizes. This treatment requires a deposition and an anneal to diffuse the $CdCl_2$ through the grain boundaries to reach all the way to the front of the device.

After the absorber deposition, a copper-doping treatment with copper chloride (CuCl) is done in a different CSS tool in the laboratory. This is followed by a thin layer of elemental tellurium, $\sim$40 nm, which helps with hole extraction at the back of the cell [25]. Carbon and nickle paint polymers are then sprayed on to form a back electrode for the device.

Other devices presented in this work use absorbers deposited by the company First Solar and back contacts deposited at CSU. The specific process for First Solar's front contact and absorber is proprietary, but they also have an n-type window layer on top of a conductive oxide before depositing the absorber layer. The First Solar absorber is deposited by vapor transport depositions and involves a thin layer of cadmium selenide (CdSe) then CdTe, using annealing to create a grated CdSeTe/ CdTe bi-layer absorber. These absorbers are then passivated with a $CdCl_2$ treatment and, in this case, doped with arsenic.

## 2.3 Device Characterization

Once devices are fabricated they must be characterized to determine performance. Different optical and electrical measurements are performed to gain information on the fundamental workings of the device. The completed device has the ability to be integrated into a completed circuit, allowing for electrical measurements. Optical measurements can be done on both completed and non-completed devices.

### 2.3.1 Current-Voltage Characteristics

Current-voltage, or I-V, measurements are the backbone of photovoltaic characterization. To account for the area of the device, current density (J) is generally used, resulting in J-V curves. I-V curves use the total current measured, whereas J-V curves divide I by the area of the cell to get a result per unit area. The term current-voltage is used to represent current density-voltage curves for brevity. Under dark conditions a voltage is applied to the solar cell and the resulting current is measured. More importantly, solar cells are also measured under illumination, where the standard test conditions are at 25$^{o}$ C at one sun illumination with an AM 1.5G solar spectrum. AM 1.5G refers to the spectrum of sunlight after passing through 1.5 atmospheres to earth, where the AM stands for air mass.

Well-behaved J-V curves follow a standard diode curve, with an example shown in Fig. 2.6. Four main parameters are found from this curve, the short-circuit current ($J_{sc}$), open-circuit voltage ($V_{oc}$), fill-factor (FF), and power conversion efficiency (PCE) as shown in Fig. 2.6. The $J_{sc}$ occurs at the y-intercept and is representative of the current that is extracted when the cell is under illumination at short circuit with no external voltage bias applied to it. The $V_{oc}$ occurs at the x-intercept and represents the maximum voltage that can be extracted out of the cell. Physically this occurs when the light induced current counterbalances the forward current of the diode.

Between $J_{sc}$ and $V_{oc}$ there is a point on the J-V curve where the power extraction is at a maximum. This occurs when the product of the current density and voltage is at its highest. This is the optimal point for the solar cell to be held when being used to produce power. It is also the point that determines the fill-factor parameter as shown in equation 2.18. Using the three parameters discussed so far the power conversion efficiency is determined as shown in equation 2.19 where $P_{in}$ is the power density [W/cm$^2$] of the light shining on the cell which is $\sim$ 1000 W/m$^2$ for the AM1.5G spectrum.

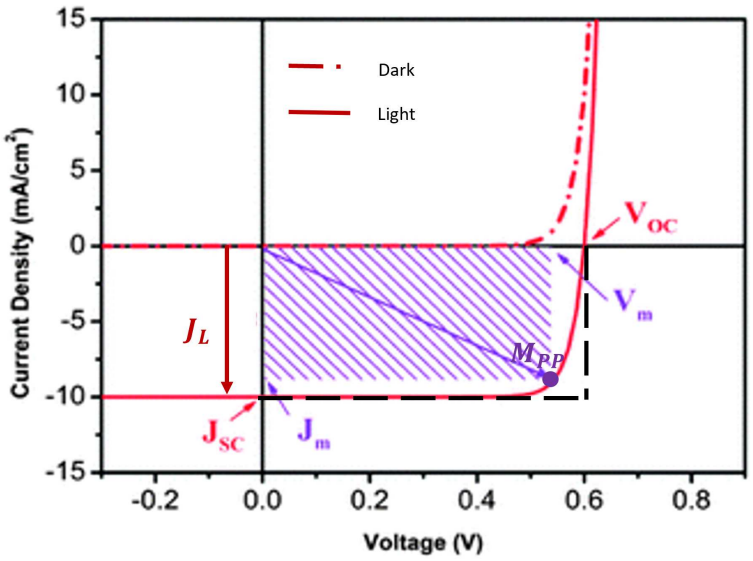


**Figure 2.6:** Light and dark current-voltage curves. Marks on the light curve show important parameters used to define the device efficiency.

$$\mathrm{FF} = \frac{\mathrm{V_{mp}J_{mp}}}{\mathrm{V_{oc}J_{sc}}} \tag{2.18}$$

$$\mathrm{PCE} = \frac{\mathrm{V_{oc}J_{sc}FF}}{\mathrm{P_{in}}} \tag{2.19}$$

For J-V measurements presented in this work, devices were measured in a light-tight box for dark measurements and at standard test conditions for light measurements unless otherwise stated. CSU has a GaAs calibration cell measured and certified at NREL that is used to calibrate the intensity of the light shining on the devices. The light is produced by a xenon arc-lamp solar simulator that approximates the solar spectrum.

### Temperature-Dependent Current-Voltage Characteristics

Much can be learned from measuring solar cells under standard conditions, but varying the temperature during measurements allows for further investigation into barrier energy inside the device, particularly at the back contact [26, 27]. The back contact of CdTe

devices is known to be a major problem for CdTe advancement [28]. One of the reasons for this is the deep energy level of the CdTe valence band at 5.8 eV [29], which is significantly greater than the work function of almost any metal that can be used for contacting, with examples shown in Fig. 2.7.

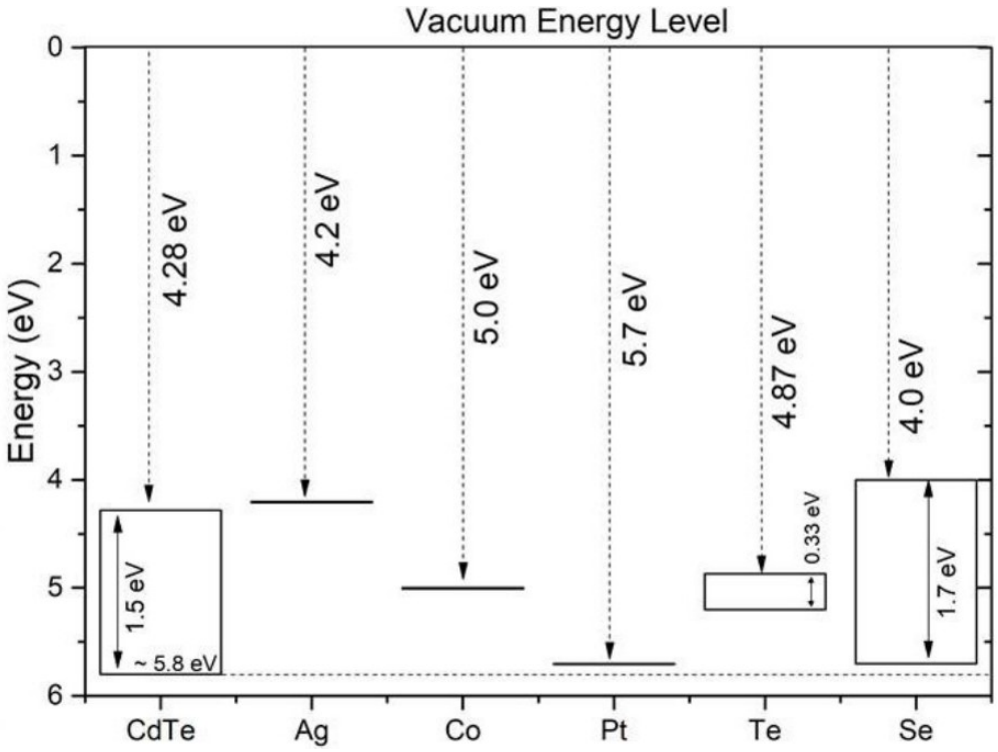


**Figure 2.7:** The ionization potential of CdTe compared to possible metal contacts. Figure from [30].

The deep energy level of CdTe causes downward band bending near the back interface in order to match the CdTe and metal Fermi-levels, creating an energy barrier for holes at the back of the cell as shown in Fig. 2.8.

To overcome this energy barrier the carrier transport will be dominated by thermionic emission at the interface, so the hole current is:

$$J_h = J_o(e^{qV_b/kT} - 1) \tag{2.20}$$

where $V_b$ is the voltage across the back contact and $J_o$ is the saturation current which is determined by:

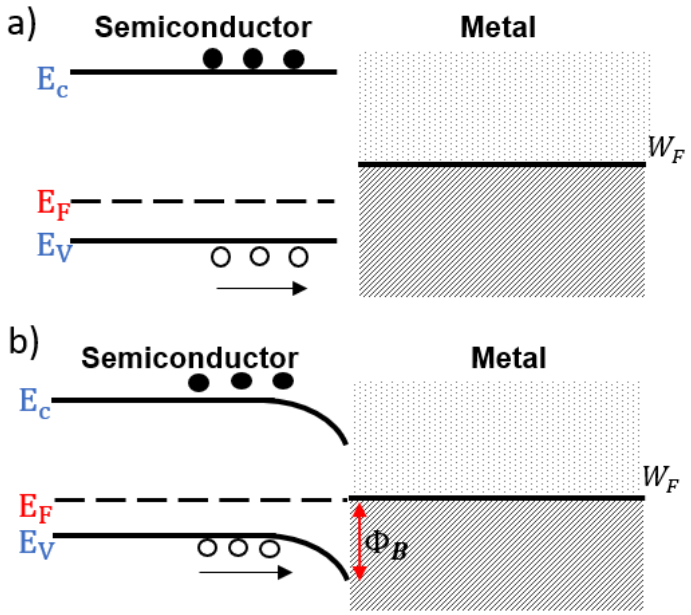


**Figure 2.8:** Energy band diagram showing: a) How energy levels of a semiconductor and metal match up before contact. b) The band-bending that occurs when a semiconductor and metal are brought into contact.

$$J_o = A^* T^2 e^{-q\Phi_b/kT} \tag{2.21}$$

where $A^*$ is the effective Richardson constant and $\Phi_b$ is the barrier height.

By lowering the temperature during a current voltage measurement, the saturation current is reduced and can be seen as a roll-over point in the J-V curve. By determining the saturation current at different temperatures, one can then find the barrier height by rearranging Eqn. 2.21 to get:

$$\Phi_B = -\frac{kT}{q} \ln \frac{J_o}{A^* T^2} \tag{2.22}$$

This allows the effective back barrier height of devices to be accurately measured.

### 2.3.2 Quantum Efficiency

Quantum efficiency (QE) determines the number of electrons extracted out of the device compared to the number of photons hitting the cell at different wavelengths. There are both internal and external QE measurements. Internal takes the reflection off the glass into account and only reports the quantum efficiency with respect to the photons that go through the glass whereas external QE (EQE) compares the all photons hitting the glass to electrons extracted. This difference is important when experimenting with anti-reflection coatings and different glasses.

The QE measurement is performed by shining white light through a monochromator to separate the different wavelengths of light. These wavelengths are shown on the cell and stepped though to measure the QE at different wavelengths, usually between 350 and 950 nm at 10 nm increments for CSU devices. Shorter wavelengths have a shorter penetration depth and are absorbed close to the front interface, whereas longer wavelengths penetrate further into the absorber. This is useful when determining possible issues at the front interface of the device. The energy spectrum of QE measurements is also useful when experimenting with different band-gap material in a solar cell. Figure 2.9 shows the parasitic absorption effect of the cadmium-sulfide window layer which contributed to the change to a wider band-gap MZO being used as the window layer [31] and how QE measurements were also crucial to the understanding of how incorporating selenium into the absorber impacts the increased absorption of low energy photons [32, 33].

### 2.3.3 Photoluminescence

Photoluminescence (PL) utilizes carrier recombination to learn about the absorber quality and defect states in PV devices. It can be measured on both completed devices and on absorber films. A laser is directed onto the film with sufficient energy to excite electrons into the conduction band and holes into the valence band. During recombination processes

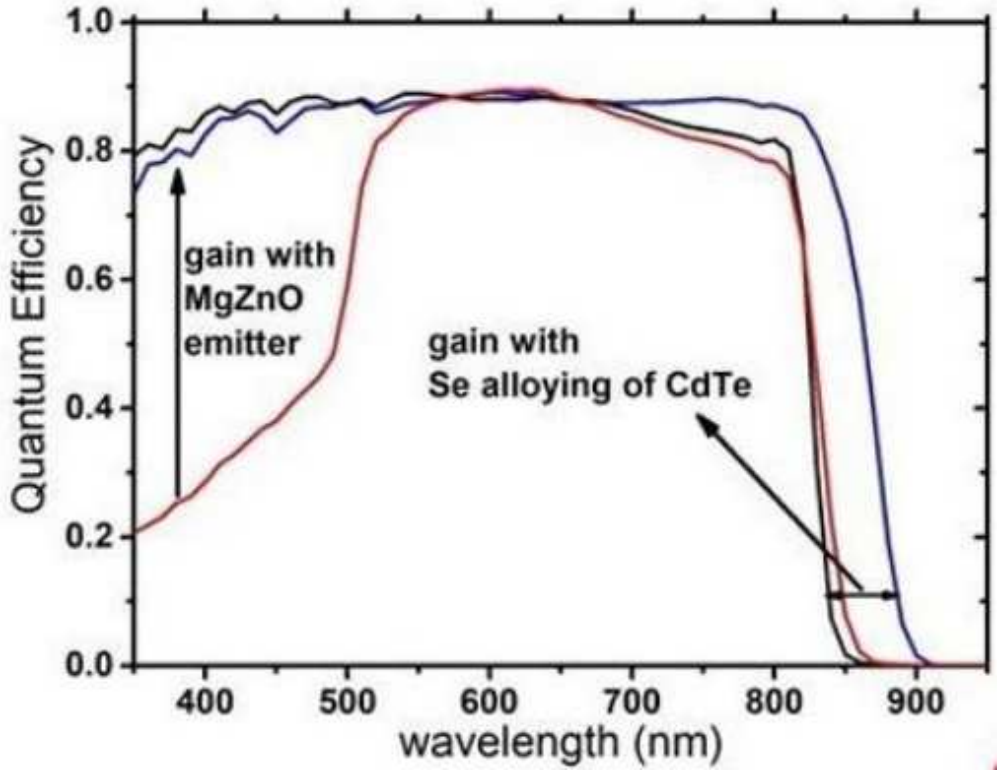


**Figure 2.9:** Quantum efficiency graph showing the effects of replacing the CdS layer with MgZnO and effects of incorporating Se into the absorber [30].

a photon may be emitted which is then detected, measuring its energy. The intensity of emission is proportional to the defect density in the film [34]. Band-to-band recombination emits photons at the energy of the band-gap, but defect-assisted recombination can also emit photons, just at a lower energy. With a proper detector setup that is sensitive to the proper wavelengths, a broad energy spectrum can be detected and plotted with an example spectrum shown in Fig. 2.10. The ratio of the band-to-band emission peak to other defect peaks is used to qualitatively understand the absorber quality and defect states. The energetic position of peaks can also give useful information about the defect position in the band gap.

With proper calibration and measurement control, along with material property understanding, the PL yield and internal voltage can quantitatively be determined. In this work, the PL system used was not set up for accurate quantitative measurements, so the results will be analyzed qualitatively. By comparing the PL spectrum of two different device structures,

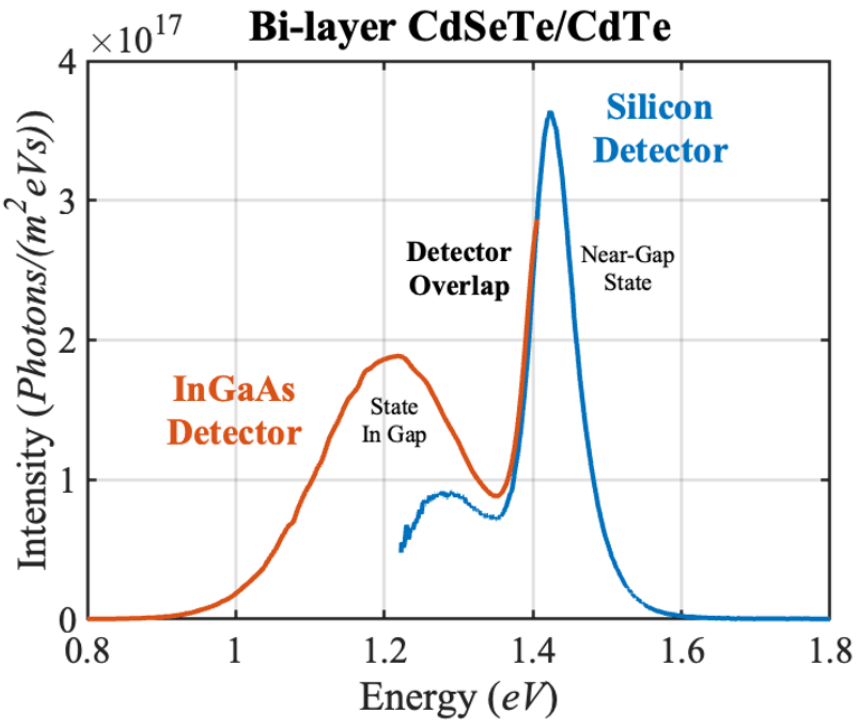


**Figure 2.10:** Example PL spectrum showing the energy range each detector can see.

information on the relative difference between their defect states can be gained. Depending on the excitation energy the laser will penetrate further into the device. Higher-energy photons are absorbed closer to the front interface, making it a good way to investigate the defect states at the front of the device. Longer wavelengths will penetrate further into the bulk allowing for investigation of the bulk properties. For films without an opaque back contact, measurements illuminating the back of the cell can be used to investigate the back interface of devices. Photoluminescence measurements provide a variety of options to investigate the defect properties of devices.

In this work two different systems were primarily used for photoluminescence. The first had has only silicon detector which only has sensitivity in the vicinity of the band-to-band recombination energy in CdTe. The second setup, constructed and calibrated by Daniel Shaw, has both the silicon detector and an indium-gallium-arsenide detector that has sensitivity down to about 0.8 eV, capable of detecting sub-band-gap recombination. Data from both setups will be discussed qualitatively to gain an understanding of defect states and absorber

quality. PL measurements from the first setup were measured with a 520-nm diode laser at $\sim$ 25 suns intensity. The second setup, shown in Fig. 2.11, used a 638-nm diode laser but with its intensity calibrated to correspond to approximately 1-sun illumination. With both a Si and InGaAs detector, the second setup is capable of measuring the luminescence form both the band-to-band recombination as well as defect assisted recombination. The second setup also has the capability to change intensity and to take voltage-biased PL. This system can be further modified to include longer wavelength excitation lasers to probe further into the device.

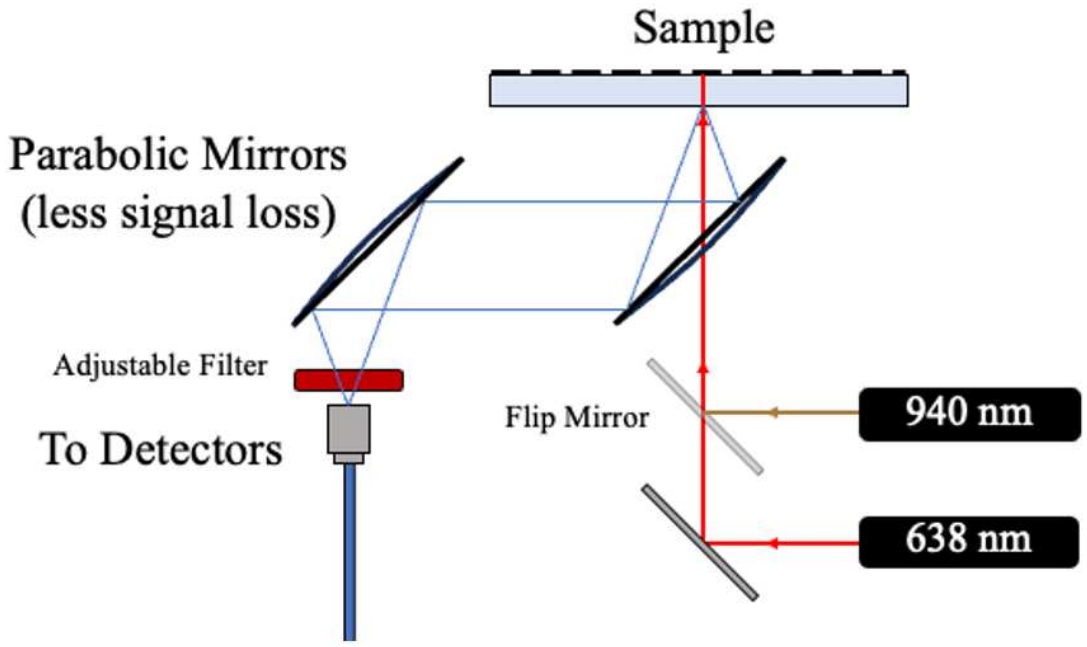


**Figure 2.11:** Diagram of the PL optical setup used for the full spectrum PL data presented in this work.

### 2.3.4 Capacitance

Capacitance measurements are done by applying an AC voltage to the device and measuring the current response with an impedance analyzer. Based on the response form the cell a complex impedance is calculated which is used to find the capacitance. This measurement can be used to extract information on the defect states, depletion widths, and carrier

densities. In this work, however, only the depletion width (W) and carrier densities were investigated.

Capacitance should be measured as a function of both frequency and voltage across the cell. The capacitance-voltage measurement is performed at a single frequency, usually 100 MHz, with a $\sim$ 10 mV signal amplitude. The voltage applied is sweep from -1 V to 1 V, with the 10 mV modulation, and the capacitance is measured. Using the depletion approximation the device is assumed to have two conductive regions separated by a region depleted of all carriers. Using this the device is modeled as a parallel plate capacitor and the depletion width (W) can be calculated by:

$$C = \frac{\varepsilon A}{W} \tag{2.23}$$

where A is the area of the device and $\varepsilon$ is the dielectric constant of the material. As the voltage changes, the charge buildup on either side of the depletion region responds and alters W. Assuming a uniform distribution of ionized dopants, analysis of the electrostatics shows:

$$\frac{C^2}{A^2} = \frac{q\varepsilon N(W)}{2(V + V_D)} \tag{2.24}$$

where N(W) is the carrier density at the depletion edge and $V_D$ is the diffusion potential [9]. The diffusion potential is not usually known so in order to find N(W) a discrete derivative is taken giving:

$$N(W) = \frac{C^3}{q\varepsilon A^2}\frac{\Delta V}{\Delta C} \tag{2.25}$$

The change in voltage for each measurement step is compared to the change in capacitance and expressed by Eqn. 2.25. By plotting the carrier density against the depletion width for CdTe devices a U-shaped curve, example shown in Fig. 2.12, is generally seen. The right branch of the curve represents the device in reverse bias and the carrier density goes higher due to a "punch-though" effect of the device being fully depleted [35]. When this happens

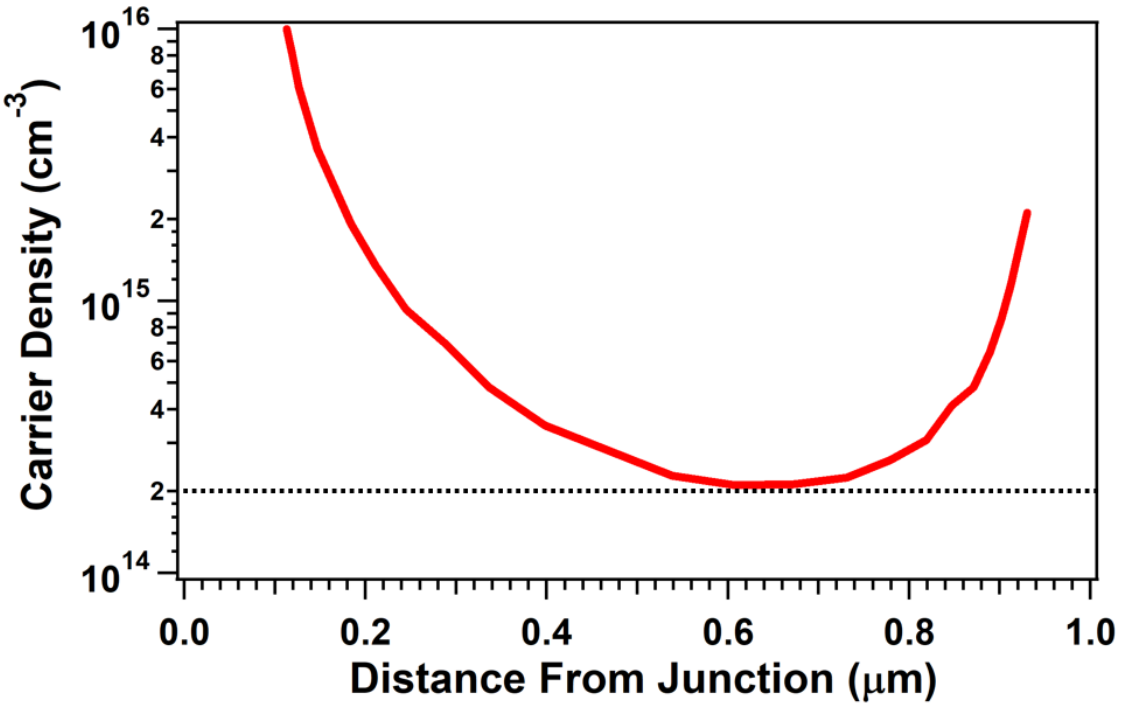


**Figure 2.12:** Example of carrier density plot made with data from capacitance voltage measurements. The reported carrier density is generally measured from the bottom of the U-shape curve.

the charges on either side of the depletion region are the layers outside of the absorber which generally have a higher carrier concentration leading to an increased N value. As mentioned in section 2.1.2, these is often an energy barrier at the back of the device. This energy barrier acts as a backward facing diode which becomes more noticeable in forward bias, corresponding to the left branch of the curve and leads to a false increase in N. One must also be aware of defect states contributing to the capacitance measurement at all biases which slightly raises the bottom of the curve.

Due to these complications, the value for carrier density is generally reported as the value at the bottom of the U-shaped curve, though it is sometimes reported as the value at zero voltage bias. Thus care should be taken to point out what value is being reported and provide a mark on the graph indicating the zero bias point.

## 2.4 Materials Characterization

### 2.4.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is an imaging technique that produces an image of the sample surface by scanning an electron beam across the sample. This can be done on the surface of samples or on a cleaved cross-section. This measurement is used to gain information about grain structure and size, film thickness, and surface topography. By cleaving and polishing the sample a cross-sectional measurement can be taken giving information about film thickness and surface roughness at interfaces.

An electron beam, typically 10-30 keV, is scanned across the surface in a raster scanning pattern exciting secondary electrons which are then detected to produce a signal. The position of the electron beam and the strength of the signal are used to stitch together an image, example in Fig. 2.13, where grain boundaries and topography are visible. SEM has resolution, depending on the sample, down to below 1 nm making it incredibly useful for gaining information on all grain sizes present in PV samples.

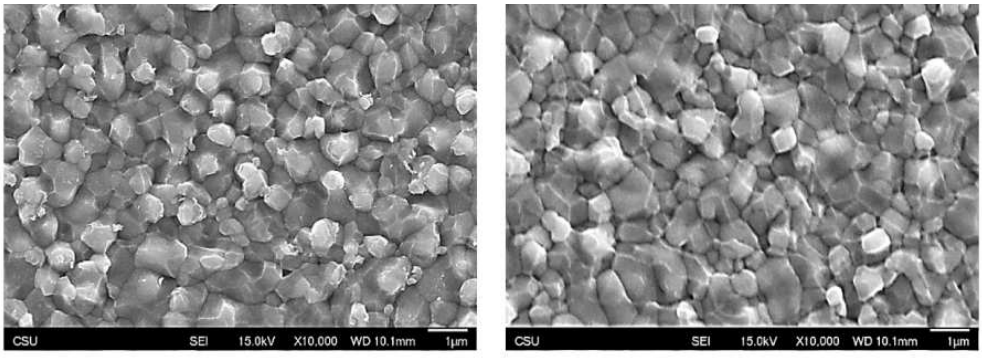


**Figure 2.13:** Example SEM images, taken from [36], of CdTe surfaces.

Both the energy of incoming electrons and the electron-beam current are important to the SEM measurements determining the penetration depth and injection level respectively [37]. The penetration depth for the electron beam is typically 10 nm, which can be changed depending on the angle of incidence of the electron beam or the electron-beam energy. The electron-beam current can be adjusted by changing the current sent through filaments of the

electron gun. The resolution is determined by changing the focus of the electron-beam using a series of electromagnetic lenses, allowing for a large range of magnification adjustment in SEM images. Measurements shown in this work were performed with a JEOL IT800HL field emission scanning electron microscope at the analytical resources core (ARC) facility at CSU.

### 2.4.2 Glancing Angle X-Ray Diffraction

Imagine techniques like SEM give information about grain size, but do not provide any insight into the crystal orientation of those grains. When X-rays interact with a crystalline material diffraction can occur. During an X-ray Diffraction (XRD) measurement diffraction of X-rays off of the crystal lattice is used to determine the crystal orientation. When X-rays are scattered off of a family of lattice planes hkl, it can be considered a reflection from a series of parallel planes [37]. When two parallel X-rays are incident on these planes at angle $\vartheta$ a maximum signal, of detected reflected X-rays, will be detected if the two rays are in phase. This happens when the difference in path length of the rays is a multiple of the wavelength $\lambda$. This relationship can be used to determine the distance $d_{hkl}$ between the atoms in the lattice by using Bragg's Law:

$$n\lambda = 2d_{hkl}\sin\vartheta \tag{2.26}$$

where $d_{hkl}$ is the lattice plane distance. Detection of these intensity peaks as a function of the X-ray angles of incidence on the surface can be used to gain information about the crystal orientation.

XRD measurements presented in this work were done at the ARC at CSU on a Bruker D8 Series 2 - Thin Film (TRXRD) system. Measurements were done using a copper anode with $2\vartheta$ scans from 20 to 80 degrees at a step size of 0.02 degrees and a scanning speed of 1 second per step.

# Chapter 3

EFFICIENCY LIMIT COMPARISON AND LOSS ANALYSIS

The efficiency of a solar cell is defined as the electrical power out of the cell compared to the power of all incident photons. The incident power is dependent on the spectrum and intensity of the light. Standard test conditions measure the solar spectrum at 1-sun intensity with the AM1.5G spectrum. AM1.5G refers to the light passing through 1.5 of earth's atmospheres and the G incorporates both direct sunlight and diffuse light caused from scattering, as opposed to AM1.5D, which only takes into account direct sunlight. When passing through earth's atmosphere, light is absorbed by particles such as carbon dioxide, water, and oxygen, which results an overall reduction of intensity and dips in photon intensity at certain wavelengths as shown in Fig. 3.1. Other test conditions are used for various purposes, AM0 as an example for space application, but in this work only AM1.5G will be discussed.

Photovoltaic devices have fundamental efficiency limitations due to the solar spectrum and the band-gap of the absorber. The three main fundamental limitations are non-absorption, thermalization, and diode limitations. In practice, there is also a limitation due to photon reflection and absorption before they reach the cell's absorber. Non-absorption refers to all the photons that have an energy below the band-gap of the absorber that will pass though it without any absorption. This primarily limits the ideal $J_{sc}$ that can be extracted from the device. Thermalization refers to the process of electrons absorbing a photon of higher energy than the band-gap, then relaxing down to the conduction band edge releasing the excess energy as heat. This limits the ideal $V_{oc}$ of the device because the energy difference of electrons and holes at extraction, not absorption, determines the voltage. The fill-factor is determined by the maximum power point of a J-V curve compared to the $J_{sc}$ and $V_{oc}$ as discussed in Eqn. 2.18. The theoretical maximum FF can be determined by finding were, on the voltage axis, the power is the greatest. This can be done by taking the derivative of

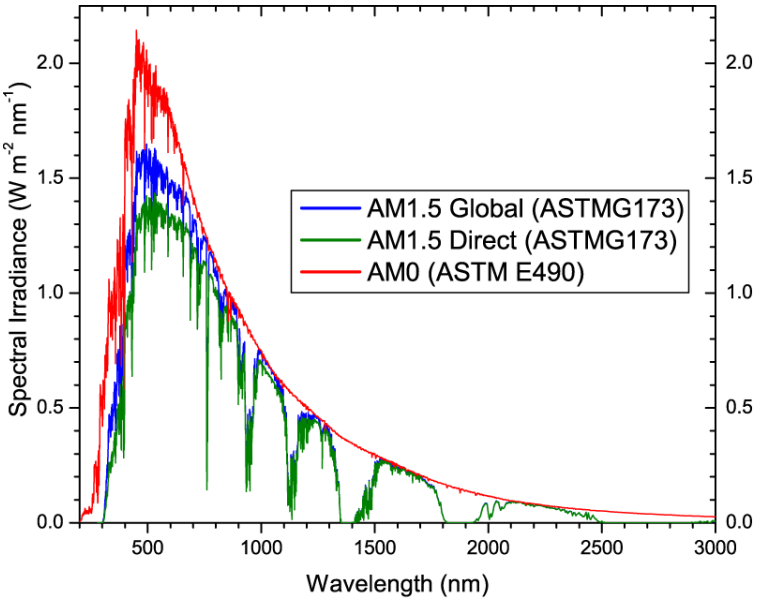


**Figure 3.1:** The solar spectrum after passing through different amounts of atmosphere. AM1.5G and AM1.5D show the difference between including the diffuse light and just the direct light.

the power and setting it equal to zero:

$$\frac{dP}{dV} = \frac{d(I_{diode}V)}{dV} = 0 \tag{3.1}$$

Solving for voltage gives the maximum power voltage ($V_{mp}$):

$$V_{mp} = V_{oc} - \frac{kT}{q}\ln(\frac{qV_{mp}}{kT} + 1) \tag{3.2}$$

This can be solved iteratively and must be below $V_{oc}$ at standard test conditions causing FF $< 1$. This limitation on $V_{mp}$ is how diode limitations affect the theoretical maximum PCE a solar cell can produce.

These different fundamental losses are all dependent on the band-gap of the absorber. The smaller the band-gap the less non-absorption will occur, but there will be more losses due to thermalization. A higher band-bap will have the opposite effect, and these competing losses create an optimal energy conversation band-gap at a point where the combination of losses are minimized. This optimal point occurs at 1.34 eV and the theoretical limit for any band-gap is known as the Shockley-Queisser limit (SQ limit).

Shockley and Queisser took these limitations into account and performed calculations to find the efficiency limit depending on the band-gap of the material [38]. This involves calculating the absorption and emission flux for the AM1.5G spectrum, taking into account the band-gap and quasi-Fermi-level separation of the device, and determining the maximum power point. These calculations have been done many times and published tables comparing the parameter limits, PCE and other major parameters such as $V_{oc}$, $J_{sc}$, and FF, for each band-gap can be found and referenced as is done in this work with the table in [15]. The theoretical limit for CdTe based devices, assuming a CdSeTe 1.4 eV band gap, is 32.9% compared to 33.2% using the overall optimal band gap of 1.34 eV.

## 3.1 SQ Limit Comparisons

When comparing the record efficiencies of different-material solar cells, it is useful to take the theoretical limit into account, not just the overall PCE. Photovoltaic (PV) technologies use different absorber materials that have different band-gaps. These different band-gaps will affect the limit of what that technology can achieve with a single-junction solar cell. By comparing devices to the theoretical limit one gets a better understanding of what technologies still have room for large PCE growth.

Not only does comparing the the SQ limit provide an insight to a technology's use of potential PCE, it also allows for analysis of J-V parameters such as $J_{sc}$, $V_{oc}$, and FF. Each of these parameters has a theoretical maximum, based on the band-gap of the absorber, that can be compared against and is available in [15]. Comparing with these parameter limits provides insight into where each technology performs well and identifies areas of potential improvement.

In this work, the performance of top research devices from different technologies, selected from Martin Green's version-63 efficiency table [8], are compared to their SQ limit. This is done for top-performing single-junction research devices. The limits and losses were separated into different parameters to parse out where the different technologies have room for improvement.

### 3.1.1 Record Single-Junction Cells

The technologies compared were gallium arsenide (GaAs), silicon (Si), copper indium gallium selenide (CIGS), perovskites, and cadmium telluride (CdTe). These technologies represent nearly all the single-junction PV currently being manufactured for commercial use and provide a comprehensive understanding on where the photovoltaic research community stands. Si and GaAs are single-crystal technologies, while CdTe, CIGS, and perovskites are poly-crystalline. Data for known devices in mid-2024 was either provided by the research group of taken from publications [39, 40, 41, 42, 43]. The primary J-V parameters for these record devices are shown in Table 3.1.

| Technology | $V_{oc}$ [V] | $J_{sc}$ [mA/cm$^2$] | FF [%] | PCE [%] | Band Gap [eV] |
|---|---|---|---|---|---|
| GaAs (single-x) | 1.130 | 29.9 | 86.9 | 29.4 | 1.42 |
| Si (single-x) | 0.749 | 41.1 | 86.3 | 26.6 | 1.12 |
| Perovskite (poly-x) | 1.194 | 26.1 | 82.2 | 25.6 | 1.55 |
| CIGS (poly-x) | 0.767 | 38.2 | 80.4 | 23.6 | 1.12 |
| CdTe (poly-x) | 0.904 | 31.8 | 81.1 | 23.3 | 1.39 |

**Table 3.1:** Primary J-V parameters for record research devices from different technologies. Note that the effective CdTe band gap is determined by a CdSeTe layer at the front

The band gap used for SQ limit comparison was determined here, by Dr. Ishwor Khatri, by taking the wavelength were QE was at 30% of its maximum and using that photon energy. These different materials had different band gaps, causing the theoretical efficiency limit to vary from 31.3 to 33.2% for the devices analyzed, as shown in Fig. 3.2. GaAs had the highest PCE at 29.4%, followed by Si at 26.6%, perovskites at 25.6%, CIGS at 23.6%, and CdTe with the lowest at 23.3%. It is worth noting that record devices must be certified by

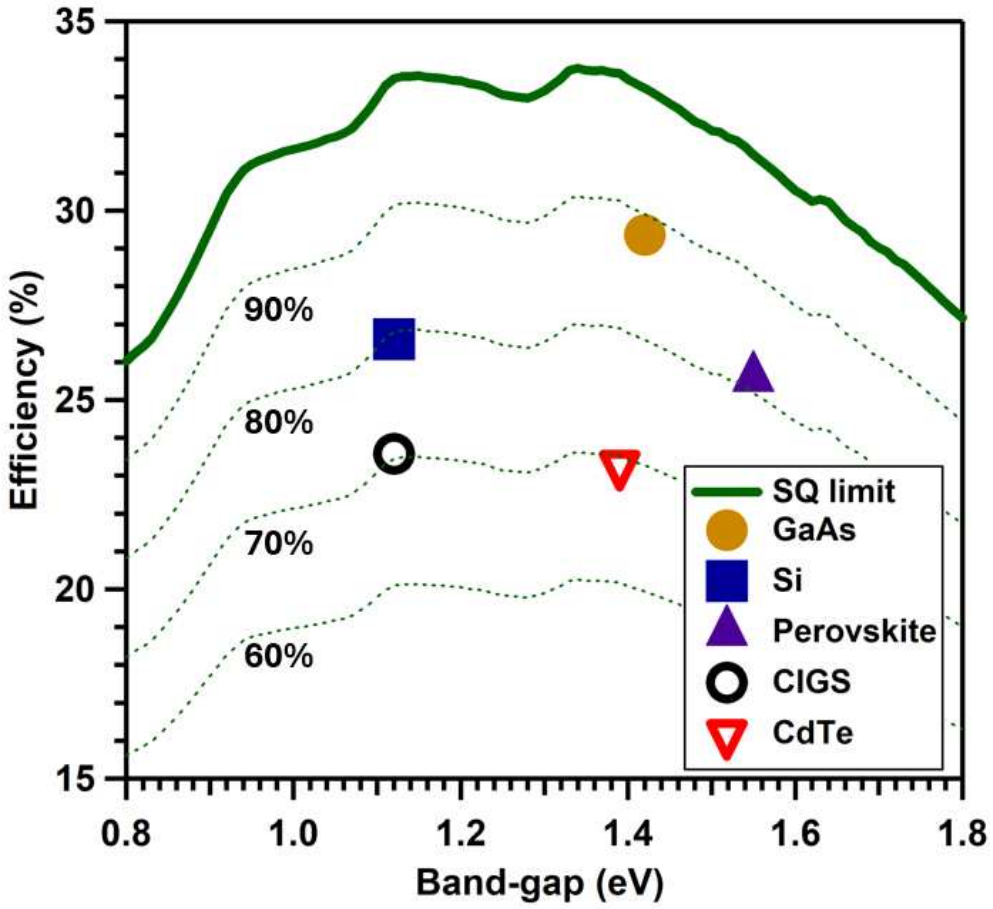


**Figure 3.2:** The SQ limit plotted against the band-gap of the absorber with percentages of the limit shown with dotted lines. Top-performing device efficiencies are plotted for comparison.

specific institutions, such as NREL, which may give a lower PCE than that measured at the fabricating lab. The values used here were those reported from internal measurements form the fabricating labs. All these devices had a FF above 80%, with the highest, GaAs, at 86.9% and CIGS with the lowest at 80.4%. Due to these different band gaps, the voltage and currents for top-performing devices varied significantly from 26.1 to 41.1 mA/cm$^2$ and 0.767 to 1.194 V as shown in Fig. 3.3.

Figure 3.2 not only shows the PCE of each device in comparison to the SQ limit, but demonstrates the variance in possible efficiency depending on the band-gap of the absorber. The majority of single-junction PV research is done on materials with band-gaps near 1.1 eV or near 1.4 eV because that is where the SQ limit is the highest, as Fig. 3.2 shows.

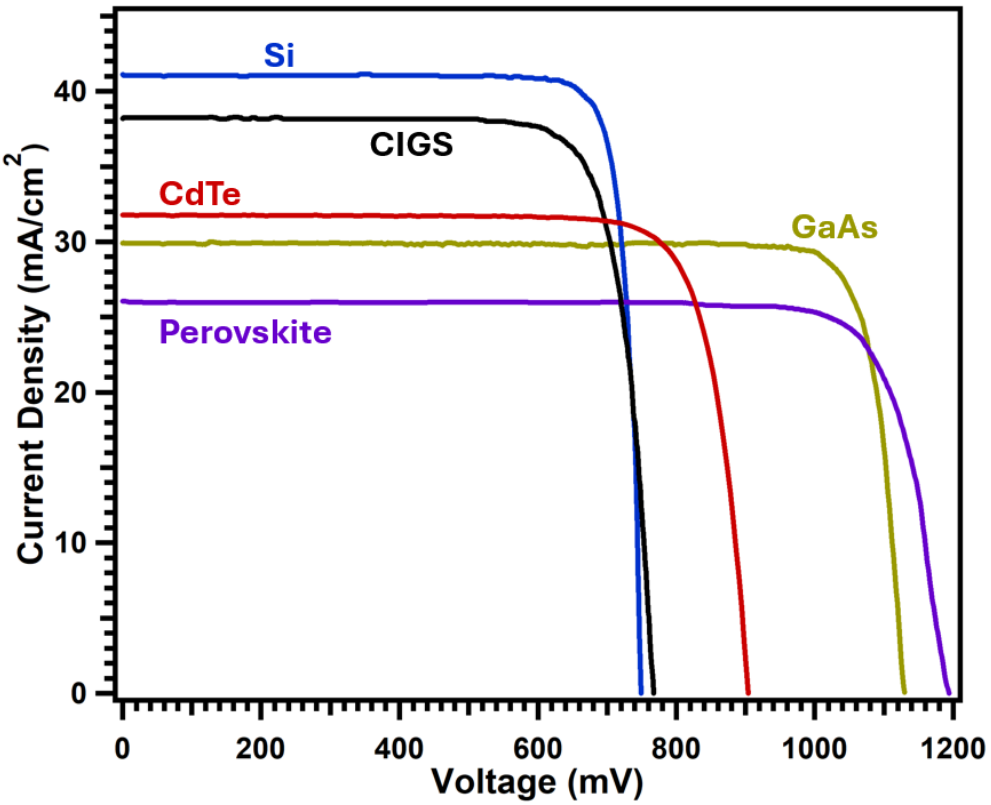


**Figure 3.3:** J-V curves for record research devices. The large discrepancies in currents and voltages are due in large part to different band gaps.

Perovskites are a relatively new technology, only gaining major traction in the recent decade [44], with a tuneable band-gap which helps explain why the record cell is not currently around the optimal band gaps.

Current-voltage curves are generally the main plot used to compare device performance, but this becomes more difficult when comparing between different band gaps. Variations in current and voltage cannot easily be attributed to failures of the device because the theoretical limits are significantly different. Figure 3.3 shows how these variations make it difficult to directly compare device performance using standard J-V curves.

By dividing the current and voltage by their SQ limits for a specific band gap, the J-V curves can be normalized, which gives a more useful visual comparison of the record research cell's J-V curves as shown in Fig. 3.4. Using these normalized J-V curves, comparison of currents and voltages becomes more clear. The current for most all these record devices is

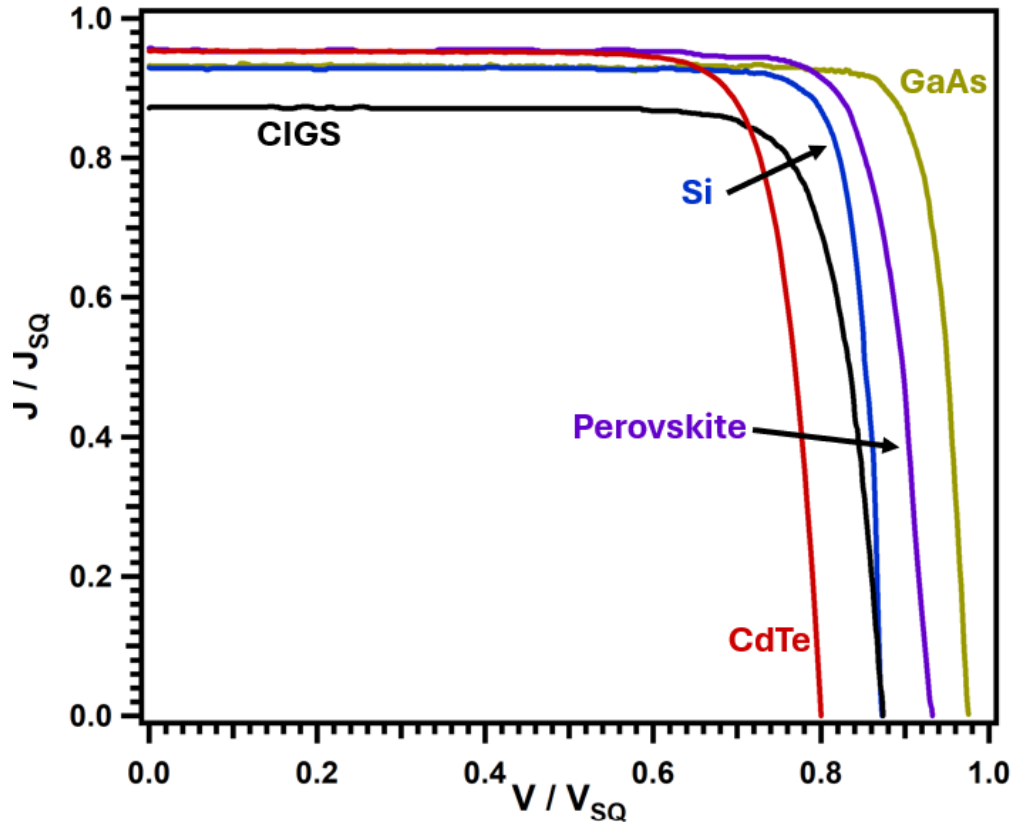


**Figure 3.4:** Normalized J-V curves for record single-junction research cells to compare each technology to the SQ limit.

near the SQ limit, with CIGS being the only technology notably below the others. This indicated that these technologies all extracted nearly all the current possible, and the remaining current, generally from reflection, can be well understood. The voltages of all these normalized curves were spread further apart, which indicated some technologies did a better job extracting voltage than others. GaAs utilized the most of its possible $V_{oc}$, while CdTe used the least among these devices.

Specific parameter comparisons to the SQ limit are given in Fig. 3.5, allowing for a more quantitative comparison between technologies. All the technologies explored in this analysis had a $J_{sc}$ value greater than or equal to 87% of the SQ limit. The record perovskite cell utilized the highest fraction of its current-density potential close to 96%, followed closely by CdTe over 95%, Si at 94%, and GaAs at 93% of their current limits. CIGS lagged somewhat

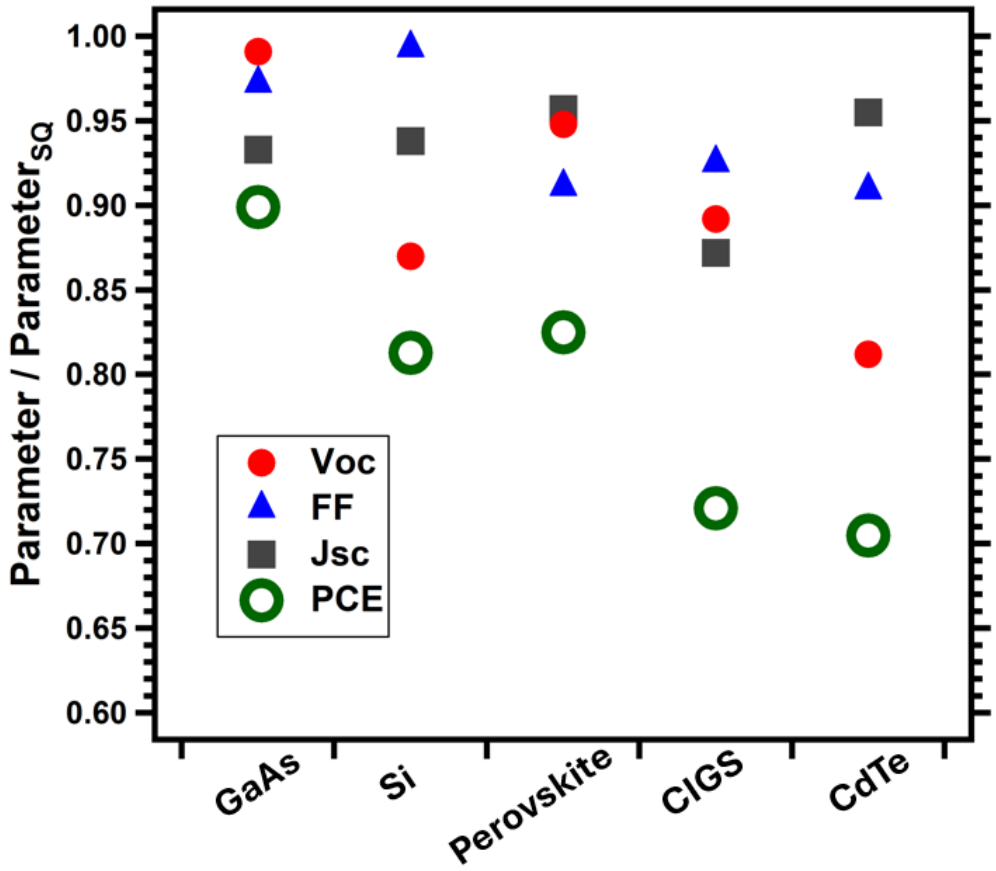


**Figure 3.5:** Comparison of different parameters normalized to the SQ limit. Gives a clear view of where individual parameters are compared to the SQ limit.

behind with only 87% its current limit, possibly due to the commonly used cadmium-sulfide window layer with a 2.4 eV band-gap that causes some parasitic absorption. While CIGS has room to improve, the other major technologies do not have significant room to further increase their current.

GaAs utilized the most of its voltage potential, reaching 99% of its limit, followed by perovskites at 95%, and CIGS at 89%. The primary utility-scale-market contributors, silicon and CdTe, are notably lower than GaAs with 87% and 81% of their SQ limit respectively. These low normalized $V_{oc}$ values show technologies such as CdTe have the potential to significantly increase their voltage. This plays a part as to why the CdTe research community has put a heavy focus on improving the $V_{oc}$ of devices and why current leaders in the community emphasize its importance moving forward [28].

Most of these top-performing devices had a high FF fraction of their ideal, the lowest being CdTe at 91%, while Si has a near ideal FF with 99% of its ideal limit. Si is followed closely by GaAs using 97% of its SQ limit. Both Si and GaAs are single-crystal technologies, whereas perovskites, CIGS, and CdTe are all poly-crystalline. Overall, Fig. 3.5 shows that single-crystalline GaAs had the highest normalized PCE, achieving 90% of its SQ limit. Perovskites and Si utilized the next most amount of PCE at 83% and 81% of their SQ limits respectively. CIGS used just 72% of its possible PCE, while CdTe is at 71%.

While normalized comparisons of the main J-V parameters for record devices gives important insight into the state of each technology, J-V curves provide additional information in the form of secondary diode parameters that come from parasitic effects occurring withing the device.

## 3.2 Parasitic Effects

One such effect, parasitic absorption, was briefly mentioned in section 2.3.2 on quantum efficiency. If photons are absorbed, or reflected, by layers prior to the absorber, fewer will be available to produce electron hole pairs resulting in less current generation. This is mainly due to optical properties of the glass and a window layer such as cadmium-sulfide, and they are generally investigated by QE and optical measurements as in [31, 36, 45]. This parasitic effect causes the $J_{sc}$ value to be lower than the SQ limit.

The other main parameters, $V_{oc}$ and FF, are reduced primarily due to parasitic electronic effects. Effects can include, but are not limited to, series resistance, shunt conductance, and a poor diode quality factor. These parasitic effects can be represented using a single diode model shown in Fig. 3.6. This models the solar cell as a single diode with a varying diode quality factor in a circuit that also has some degree of series and shunt resistance.

Shunt conductance in PV devices is often attributed to leakage around the edges, crystal defects, and pinholes in the semiconductor material [46], allowing for current to take a less resistive route through the circuit. This is especially a problem when device layers are made thinner to test specific properties or to conserve material. Series resistance occurs within a

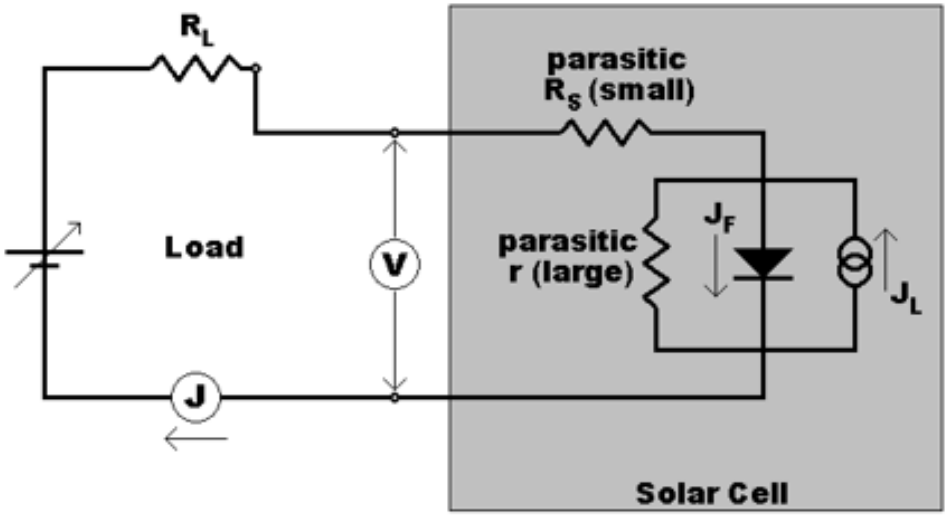


**Figure 3.6:** Representation of the single diode model. Shows shunt and series resistances, the central diode, and electronic considerations outside the solar cell.

solar cell when at least one material layer has insufficient conductivity through the device or lateral conductivity at the contacts, preventing current from flowing to the measurement system freely. Series resistance can also result from lead resistance or that internal to the measurement equipment, which must be monitored periodically. Both the series resistance and shunt conductance impact device performance electronically, which primarily manifests in a reduction in FF.

One other parasitic effect applicable to this work is a poor diode quality factor. The diode quality factor can generally range from one to two. One represents only radiative recombination occurring in the device, specifically within the depletion region, and two represents radiative recombination occurring in the depletion region or due to high injection levels [46, 47], the latter of which is not of general concern for CdTe devices. Separating the effect non-radiative recombination has on voltage compared to diode quality factor is non-trivial and requires careful analysis.

## 3.3 Diode Analysis

In order to extract quantitative information about the parasitic losses, J-V curve data is used and compared to the diode equation:

$$\mathrm{J} = \mathrm{J_o exp}[(\frac{\mathrm{q}}{\mathrm{AkT}})(\mathrm{V} - \mathrm{RJ})] + \mathrm{GV} - \mathrm{J_L} \tag{3.3}$$

which includes the loss parameters of shunt conductance (G), series resistance (R), and diode quality factor (A). The analysis used to extract these diode parameters from the J-V curve data is described in detail by Hegedus and Shafarman [48] and also laid out in [49].

This method is done by taking the derivative of the J-V data and plotting it in three different ways, with example graphs shown in Fig. 3.7, and requires the J-V curve to reasonably fit the diode equation to produce reliable results. In practice this requires the fill-factor to be greater than 70%. Determining the conductance is done by plotting dJ/dV near $\mathrm{J_{sc}}$ and taking the y-intercept. Assuming $\mathrm{J_L}$ is constant and G is ohmic, this will yield the shunt conductance. The value is chosen around the y-intercept to avoid any interference of possible voltage-dependent current collection.

To determine R and A the dV/dJ is taken of Eqn. 3.3 which gives:

$$\frac{dV}{dJ} = R + \frac{AkT}{q}(J + J_L)^{-1} \tag{3.4}$$

which is then used to plot dV/dJ against $(\mathrm{J} + \mathrm{J_L})^{-1}$, as shown in Fig. 3.7 (c). This plot yields a straight line where the slope and y-intercept determine A and R. This works best when $\mathrm{RG} << 1$, but plotting against $(\mathrm{J} + \mathrm{J_L} - \mathrm{GV})^{-1}$ corrects for when G is non-negligible.

Rearranging Eqn. 3.3, using R and G found from previous graphs, to get:

$$ln(J + J_L - GV) = \frac{q}{AkT}(V - RJ) + ln\, J_o \tag{3.5}$$

allows one to plot $ln(J + J_L - GV)$ against $(V - RJ)$, shown in Fig. 3.7 (d). Making sure there is a good linear fit over 1-2 orders of magnitude in current is a good indication the J-V

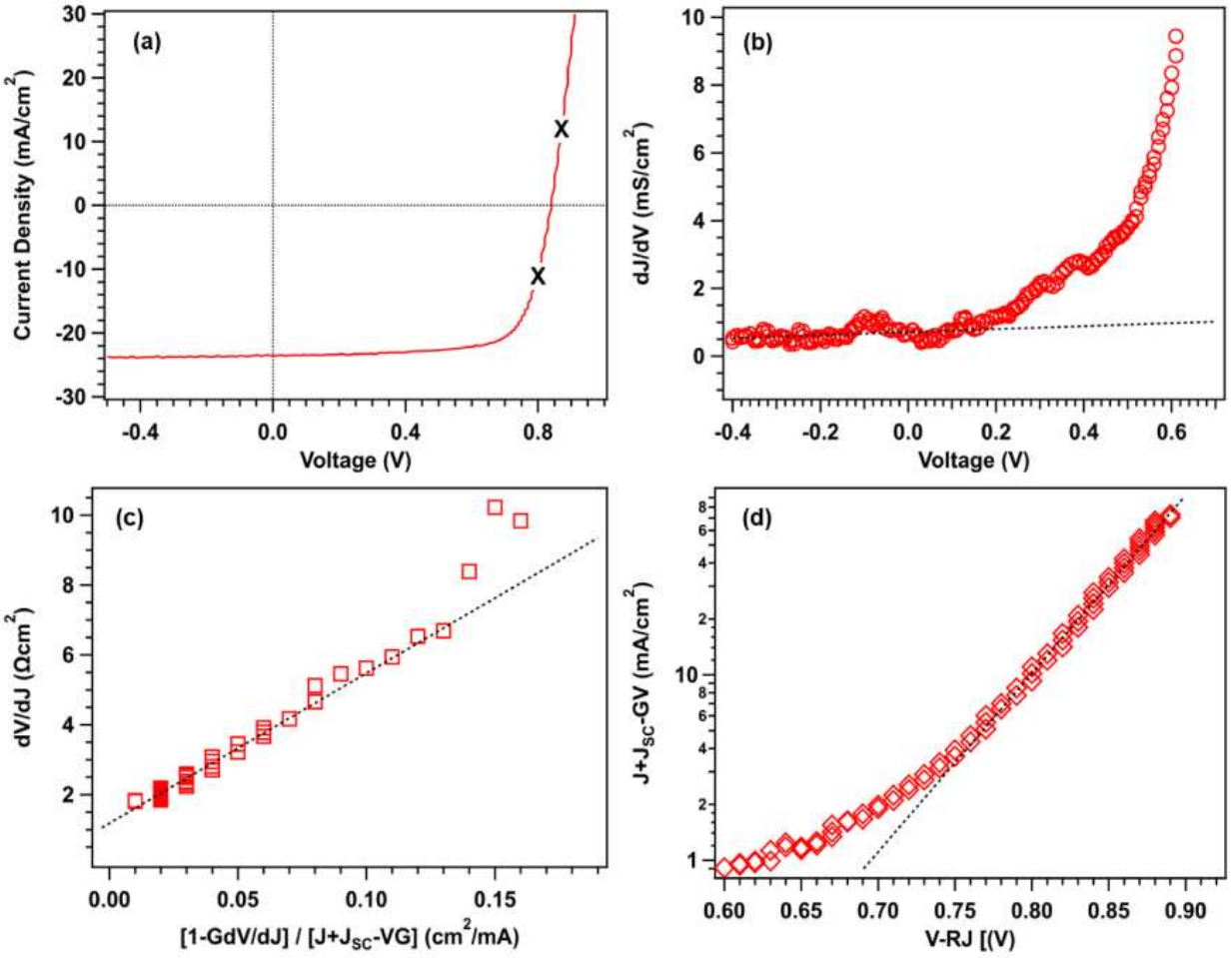


**Figure 3.7:** Example graphs used during diode analysis to determine diode parameters. Figure from Alex Bothwell's PhD thesis [36]

data is a good fit to the diode equation. The slope and y-intersect of this plot are then used to find the saturation current ($J_0$) and independently determine the diode quality factor.

The diode quality factor can be voltage dependent, so having A determined from both Fig. 3.7 (c) and (d) allows for a check on the analysis precision and diode quality. When the two values for A reasonably agree, the average is take to determine the reported value, and when they do not reasonably agree it is attributed to poor diode quality where the analysis is likely invalid. To minimize contributions from voltage dependence, linear fits for Fig. 3.7 (c) and (d) are performed from just past the maximum power point to just past the $V_{oc}$. A general region of this fit is shown in Fig. 3.7 (a) by the x marks on the curve.

In this work diode analysis was done using the CurVa software developed at CSU by Markus Gloeckler. This program allows the user to choose the fit range on each graph to limit any voltage dependent contributions. Since the user determines the fit ranges, this process is not necessarily consistent for different users. It is generally consistent for the same user, but comparisons between parameters fit by different people can show variations. Parameters presented in this work where done by the author unless otherwise stated.

Determining these parameters from J-V curves produces valuable information from data that is already available, allowing for more parameter comparisons when determining the losses for different devices. These parameters not only allow for numerical comparison, but can also be used to determine the cause of fill-factor loss in devices.

### 3.3.1 Fill-Factor Loss Analysis

In addition to comparing the $J_{sc}$, $V_{oc}$, and PCE to the SQ limit, the fill-factor is also compared to the limit. The secondary diode parameters are then used to separate the FF loss, compared to the SQ limit, into specific contributions to better understand what is contributing to issues within the device. The analysis, described below, follows the procedure laid out in [32, 46, 49]. The measured FF ($FF_{measured}$) can be considered to be a combination of the ideal FF ($FF_{ideal}$) and a loss parameter $\alpha$ such that $0 \leq \alpha \leq 1$:

$$FF_{measured} = \alpha FF_{ideal} \tag{3.6}$$

$FF_{ideal}$ is based on the SQ limit and thus dependent on the band-gap of the absorber. $FF_{ideal}$ can be found using:

$$FF_{ideal} = \frac{v_{ideal} - \ln(v_{ideal} + 0.72)}{v_{ideal} + 1} \tag{3.7}$$

from [46], where $v_{ideal}$ is the normalized voltage given by:

$$v_{ideal} = \frac{qV_{SQ}}{AkT} \tag{3.8}$$

where $V_{SQ}$ is the SQ limit open-circuit voltage for the specific band-gap and A = 1 representing an ideal diode. For a CdTe device with band gap of 1.4 eV, $FF_{ideal}$ = 89.3%. $\alpha$ is

separated into individual factors such that:

$$\alpha = \delta_G \delta_R \delta_{diode} \tag{3.9}$$

where each $\delta$, $0 < \delta < 1$, represents the fractional loss due to the diode parameters determined with the method from the previous section. The loss factors for series resistance and shunt conductance are given by:

$$\delta_G \approx 1 - (\frac{v_{oc} + 0.7}{v_{oc}})(\frac{FF_{ideal} V_{oc} G}{J_{sc}}) \tag{3.10}$$

$$\delta_R \approx 1 - \frac{R J_{sc}}{V_{oc}} \tag{3.11}$$

where:

$$v_{oc} = \frac{qV_{oc}}{AkT} \tag{3.12}$$

The diode contribution to FF loss is determined by taking the ratio of $FF_{ideal}$ and the FF resulting when the measured $V_{oc}$ and determined A-factor are placed into Eqn. 3.7 such that:

$$\delta_{diode} \approx \frac{FF_{V_{oc},A}}{FF_{ideal}} \tag{3.13}$$

This diode contribution to FF loss can be separated into two parts, the non-ideal $V_{oc}$ and a diode quality factor greater than 1 such that:

$$\delta_{diode} = \delta_{V_{oc}} \delta_A \tag{3.14}$$

where $\delta_{V_{oc}}$ represents the fractional loss of fill-factor due to the voltage of the cell falling below the SQ limit value. The $V_{oc}$ term is found by taking the ratio of the calculated FF with an ideal A-factor, but the measured $V_{oc}$ parameter ($FF_{V_{oc},A=1}$) such that:

$$\delta_{V_{oc}} = \frac{FF_{V_{oc},A=1}}{FF_{ideal}} \tag{3.15}$$

This allows the contribution from the lowered voltage to be taken into account while decoupling the diode quality factor's impact. The A factor impact is found after the $V_{oc}$

impact by taking the ratio of both the $V_{oc}$ and A factor are into account compared to just the $V_{oc}$ giving:

$$\delta_A = \frac{FF_{V_{oc},A}}{FF_{V_{oc},A=1}} \tag{3.16}$$

Together these δ's represent the fractional fill-factor loss contributions compared to the ideal. Once they are calculated, they are used to determine the share of FF loss attributed to a specific parameter by taking the ratio of parameter loss to the sum of losses, as illustrated for the diode quality factor here:

$$Loss_A = \frac{(FF_{ideal} - FF_{measured})(1-\delta_A)}{(1-\delta_A) + (1-\delta_V) + (1-\delta_G) + (1-\delta_R)} \tag{3.17}$$

The loss term of interest is weighted against the total loss from all contributors, then scaled to the difference between the measured FF and the $FF_{ideal}$ to determine what percentage of FF was lost due to each parameter.

With this analysis a quantitative impact of loss mechanisms is obtained, leading to more direct information on how parameters are negatively impacting device performance. Since this analysis compares to $FF_{ideal}$ it can also be used to further compare device performance to the SQ limit.

## 3.4 Fill-Factor Loss Comparison

### 3.4.1 Record Single-Junction Devices

To best understand the path forward towards higher efficiencies, researchers must have a good understanding of where their records fall short of the SQ limit. The analysis in the previous section was applied to the top-performing devices discussed in section 3.1.1 to gain a better understanding of not only how far the FF is from the SQ limit, but also what is causing the loss in FF. The results of the diode analysis and their contribution to fill-factor loss are shown numerically in Table 3.2 and visually in Fig. 3.8. Figure 3.8 illustrates which

research cells are near their SQ limit, which are further away, and what is causing these differences.

| Technology | FF Total Loss % | G [mS/cm$^2$] (***FF Loss*** %) | $R_s$ [$\Omega$/cm$^2$] (***FF Loss*** %) | A factor (***FF Loss*** %) | $V_{oc}$ [V] (***FF Loss*** %) |
|---|---|---|---|---|---|
| GaAs | 2.5 | 0.11 ***(0.3)*** | 0.43 ***(0.9)*** | 1.17 ***(1.2)*** | 1.130 ***(0.1)*** |
| Si | 0.3 | 0.01 ***(0)*** | 0.1 ***(0)*** | 1.01 ***(0)*** | 0.749 ***(0.3)*** |
| Perovskite | 8.0 | 0.15 ***(0.6)*** | 1.29 ***(2.6)*** | 1.59 ***(4.4)*** | 1.194 ***(0.4)*** |
| CIGS | 6.5 | 0.1 ***(0.2)*** | 0.27 ***(1.1)*** | 1.42 ***(4.1)*** | 0.767 ***(1.1)*** |
| CdTe | 8.1 | 0.08 ***(0.2)*** | 0.16 ***(0.5)*** | 1.64 ***(5.6)*** | 0.904 ***(1.8)*** |

**Table 3.2:** Secondary diode parameters calculated as described above. The contribution to FF loss is shown in parentheses.

Silicon had a near perfect *FF*, with its only significant loss contribution coming from the fact that its $V_{oc}$ fell short of the maximum. GaAs also utilized almost all of its *FF* potential with very small losses attributed to its slightly non-ideal diode quality factor and a small amount of series resistance. For thin-film perovskites, CIGS, and CdTe, the majority of *FF* loss was attributed to larger diode quality factors. These devices are all poly-crystalline technologies, in contrast to single-crystal GaAs and Si, which have the lower diode quality factors. A high diode quality factor is often attributed to non-radiative recombination in the depletion region of the device [46]. The higher diode quality factors in the polycrystalline devices likely indicate that grain boundaries play a major roll in non-radiative recombination which in turn reduces their fill-factors.

The reduced $V_{oc}$ also played a notable role in the FF loss for the CdTe device, at 1.8% of the FF loss, which had the lowest normalized $V_{oc}$ at only 81%. This, combined with a

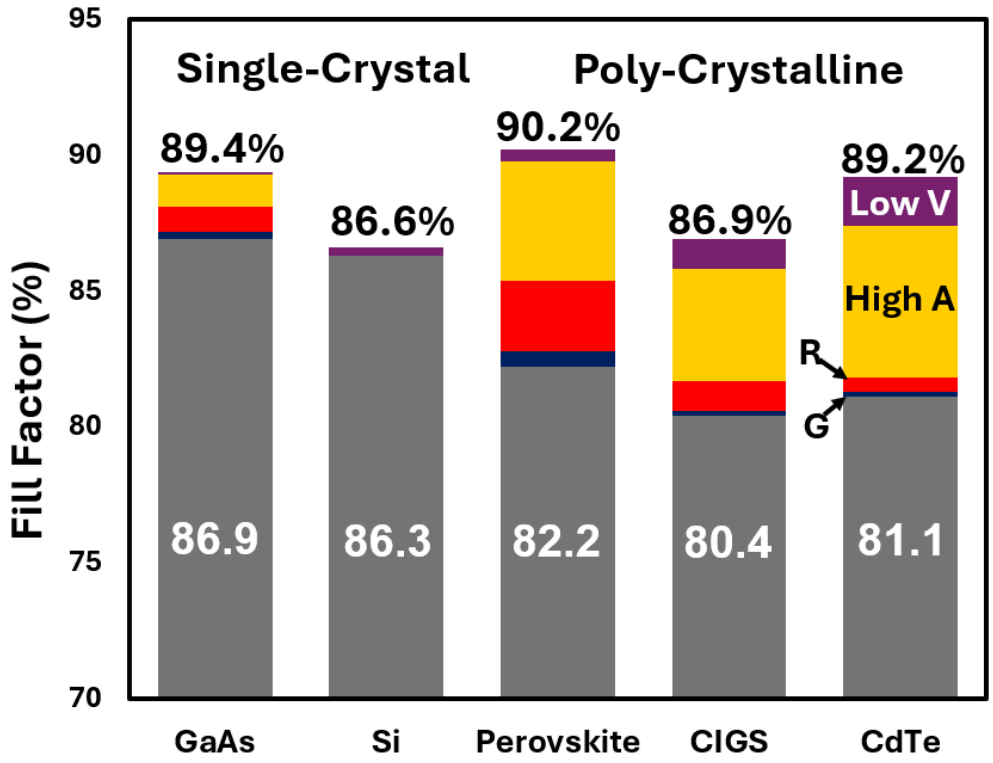


**Figure 3.8:** Visual comparison of ideal FF values (given on top of the bars) to measured values (given in grey part of the bars). The total FF loss is separated into contributions from the individual diode parameters.

poor diode quality factor, were the primary causes of CdTe having the largest loss in FF. Reduced $V_{oc}$ impacted the CIGS device the next most, with 1.1% loss contribution, and played a more minor role in the other three record devices losses with all below 0.5%. The loss due to series resistance played a roll in all devices except for Si. The record perovskite had by far the highest series resistance at 1.3 $\Omega/cm^2$ causing a 2.6% loss in fill-factor while GaAs and CIGS, which were the next most impacted, had losses of only 0.9% and 1.1% respectively. The shunt conductance $G$ played only a minor roll in reducing the $FF$ for all devices shown here.

Separating the FF losses into individual loss factors helps determine where even the best cells have room for improvement. This analysis can also be applied to devices within the same technology to compare how different processing choices affect these different parameters and the FF.

### 3.4.2 CdTe Devices

#### Different Research Laboratories

The CdTe community is spread across different universities, national laboratories, and companies around the world. These laboratories use various device structures and techniques to obtain high performing devices. By performing diode analysis on these J-V curves information can be gained as to have exactly the different layers, or processes, are affecting device performance. In this work top performing devices, with efficiencies at or above 20%, from First Solar [50], Loughborough University (LU) in concert with First Solar [51], the University of Toledo (UT) [52], and Colorado State University (CSU) [53] are analyzed, using published results, to determine how their different device structures impact diode parameters and the fill factor. The device structures are outlined in Table 3.3. By investigating these devices, the community can see what is causing the primary losses in device performance among the best devices in the field and determine what fabrication techniques and material layers create high performing devices.

| Affiliation | AR Coating | Window | $n^+$ Buffer | Absorber | Doping | Back Buffer | Metal Contact |
|---|---|---|---|---|---|---|---|
| FSLR Record $V_{oc}$ | Yes | $SnO_2 : F$ | Unpublished | CdSeTe/CdTe | As | ZnTe | Unpublished |
| FSLR PCE Record | Yes | $SnO_2 : F$ | Unpublished | CdSeTe/CdTe | P | ZnTe | Unpublished |
| LU/FSLR | Yes | $SnO_2 : F$ | ZnO | CdSeTe/CdTe | As | ZnTe | Unpublished |
| UT | Yes | $SnO_2 : F$ | None | Cd(S,Se,Te)/CdSeTe/CdTe | Cu | CuSCN | Au |
| CSU | Yes | $SnO_2 : F$ | MgZnO | CdSeTe/CdTe | Cu | Te | C/Ni Polymer |

**Table 3.3:** The device structure for top devices from top CdTe research facilities. Each device is separated into different layers or processes used in the fabrication process.

All of the top-performing devices in Table 3.3 had an anti-reflective coating on the glass substrate to increase current generation by transmitting more light to the absorber, and the top devices all used a fluorine-doped tin oxide as a conductive front layer as shown in Table

3.3. Generally, the absorber was a graded CdSeTe/CdTe bi-layer, with the exception of the University of Toledo's champion device which included sulfur. The main differences between the devices were the $n^+$ buffer layer at the front, the doping method, and the hole-selective back layer. Absorbers, in table 3.3, manufactured at First Solar were doped with arsenic, while devices at UT and CSU were doped with copper. Another difference between labs is which $n^+$ buffer layer was used, with CSU and Loughborough using MgZnO and ZnO respectively while the University of Toledo deposited the absorber directly onto the $SnO_2$ layer. The hole transport layer was ZnTe at First Solar, a thin Te layer at CSU, and a CuSCN layer at UT. These devices all produced good results, with efficiencies at or above 20%, but the differences in structure lead to variations in the diode parameters extracted as shown in Table 3.4, with FF loss calculations shown in Fig. 3.9.

| Affiliation | $V_{oc}$[V] | $J_{sc}$[mA/cm$^2$] | FF [%] | PCE [%] | G [mS/cm$^2$] | R [$\Omega$/cm$^2$] | A factor | $E_g$(eV) |
|---|---|---|---|---|---|---|---|---|
| FSLR Record $V_{oc}$ | 0.917 | 30.9 | 78.3 | 22.2 | 0.04 | 0.4 | 1.85 | 1.39 |
| FSLR PCE Record | 0.904 | 31.8 | 81.1 | 23.3 | 0.08 | 0.16 | 1.64 | 1.39 |
| LU/FSLR | 0.876 | 30.4 | 80.5 | 21.4 | 0.11 | 0.25 | 1.6 | 1.41 |
| UT | 0.862 | 29.2 | 79.4 | 20 | 0.9 | 0.2 | 1.6 | 1.41 |
| CSU | 0.875 | 28.7 | 80.4 | 20.1 | 0.04 | 0.57 | 1.6 | 1.41 |

**Table 3.4:** Performance parameters and secondary diode parameters for top-performing cells from different research laboratories.

The largest FF loss in all these CdTe devices came from the diode quality factor, followed by the contribution from $V_{oc}$. The large diode quality factors, all above 1.6, caused all these devices to lose at least 5% FF, with the largest $V_{oc}$ device losing over 7%. The A-factor causing the majority of FF loss in all devices indicates that improving it will yield the largest benefits going forward. The $V_{oc}$ in all these CdTe devices was well below the SQ limit, which caused the voltage reduction to be the next largest cause of FF reduction in

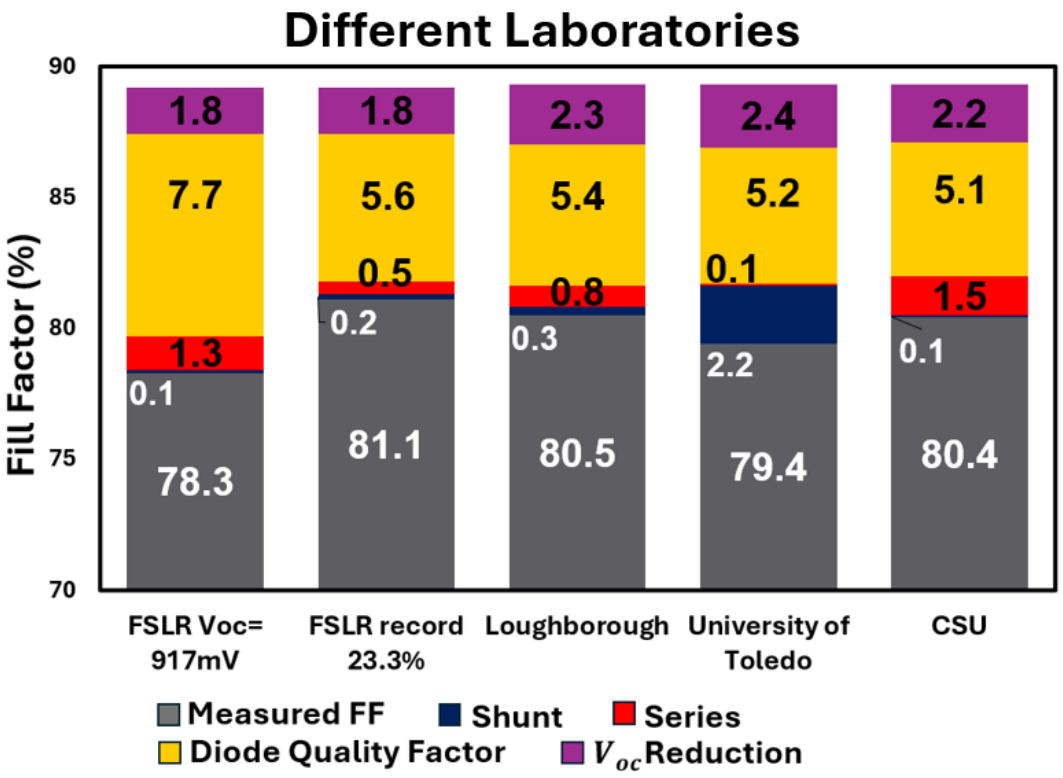


**Figure 3.9:** Detailed fill-factor loss analysis for top devices from different CdTe laboratories.

all devices analyzed. Both the diode quality factor and the $V_{oc}$ are known to be related to unfavorable recombination within the device, suggesting that by improving carrier lifetimes and reducing recombination pathways there should be a significant improvement in both $V_{oc}$ and FF. The diode quality factor is related specifically to non-radiative recombination in the depletion region of the device [54], indicating that reducing recombination in the bulk of the device should improve the FF of devices.

While First Solar depositions utilized arsenic doping and a ZnTe back contact, the fill-factor losses were similar to those from Colorado State University who used copper-doping and a Te back buffer layer. Loughborough University and Colorado State University had similar diode parameters, resulting in both having a fill-factor over 80%. Both used a window layer containing ZnO, while CSU incorporated Mg to make MgZnO. Both utilized a back buffer layer containing Te. These differences in device structure ultimately lead to similar fill factor losses. The most notable difference between the device FF losses is that the University

of Toledo had a higher loss due to shunt conductance. The major differences in the UT device structure were that instead of a standard window layer they incorporated sulfide into the front of the absorber. In this case, this major difference corresponded with a large shunting in the device.

By comparing record devices between labs, a better understanding of where CdTe falls short of theoretical limits becomes more clear. Different devices analyzed had different structures and fabrication methods, but still had similar losses attributed to the diode quality factor and $V_{oc}$ reduction. Going forward, high performing devices should be analyzed to see where losses come from. This should give a good idea on where CdTe has the most room for improvement, allowing the community to direct research to issues that will yield the most improvement.

### 3.4.3 Thin vs Thick Absorbers

One area of current CdTe research is reducing the thickness of the absorber layer. This has benefits for reducing the material needed, which is a concern for rare materials such as tellurium. It also has benefits for reducing the manufacturing time, which in turn helps improve profits. Using thinner absorbers also helps researchers understand the back-contact better, which is described in detailed in the next chapter. At CSU there is a recent project, lead by Dr. Katherine Zaunbrecher, that achieved a PCE of 18.1% with just a 1.5 μm absorber. This is compared to a standard thickness device fabricated around the same time, by Pradeep Murugan, that reached 19% PCE as shown in Table. 3.5. These devices had nominally the same device structure other than the thickness of the absorber. The J-V curves were analyzed by Jennifer Drayton to extract the secondary diode parameters as shown in Table. 3.6.

This data can also be used to compare devices' FF losses to each other, which was done and is shown in Fig. 3.10. The analysis shows nearly the same loss contributions for all parameters except for the $V_{oc}$ reduction. The $V_{oc}$ for the thin device was ∼60 mV lower than the thicker device. This lead to almost a full percent more FF loss and accounted for

| Absorber | Fill-Factor [%] | PCE [%] | $J_{sc}$[mA/cm$^2$] | $V_{oc}$[V] | R [$\Omega$/cm$^2$] | G [mS/cm$^2$] | A factor |
|---|---|---|---|---|---|---|---|
| 1.5 μm | 78.5 | 18.1 | 28.7 | 0.804 | 0.8 | 0.25 | 1.45 |
| 3.3 μm | 79.3 | 19 | 27.6 | 0.868 | 1 | 0.35 | 1.54 |

**Table 3.5:** Performance parameters and secondary diode parameters for the best thin and thick devices fabricated at CSU around the same time.

the difference in FF between the two devices. Voltage is known to be an issue in thinner devices because more carriers recombine at the back interface. This analysis supports this, showing that the devices are electronically similar except for the impact of the lower voltage extracted.

| Absorber | FF Total Loss [%] | Shunt Loss [%] | Series Loss [%] | A Loss [%] | $V_{oc}$Loss[%] |
|---|---|---|---|---|---|
| Thin | 10.8 | 0.6 | 2.6 | 4.5 | 3.1 |
| Thick | 10 | 0.8 | 2.6 | 4.4 | 2.2 |

**Table 3.6:** Calculated fill-factor loss due to each parameter. Used to compare thick and thin fill-factor performance.

More generally, performing this analysis on similar devices with one major difference is a good way to identify how that one difference is affecting the device. In this case the thin absorber was not only lowering the $V_{oc}$ as expected, but the lower voltage directly impacted the FF as well. It draws attention to the need for a better back-contact for CdTe devices, especially if the community continues to try and thin absorbers.

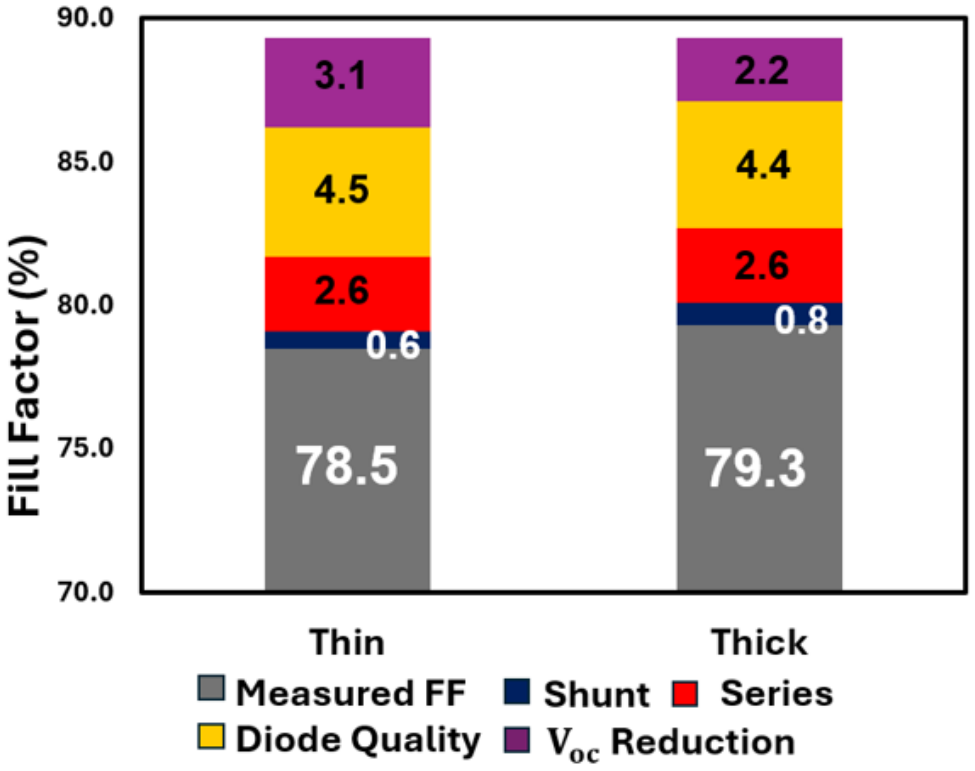


**Figure 3.10:** Detailed fill-factor loss analysis comparing thick and thin absorber devices fabricated at CSU.

### 3.4.4 Records Over Time

Comparing devices over time is another good way to better understand how changes in device structure impact performance. Figure 3.11 shows record devices from First Solar's California Research Center over the course of a few years. The device with the highest voltage (917 mV) had the lowest fill-factor due primarily to a weeker diode quality factor. That same batch of cells produced the previous world record with 22.3% PCE [50]. The record cell though had a lower voltage, but better diode quality factor, which is a major reason why there was an improvement in FF.

The next batch of cells with increased PCE had fill-factors at 80%, a noticeable improvement from the previous record cell. This improvement was mainly due to a decrease in series resistance, which led to ∼1% improvement in the FF. Whatever was changed in the newer cells, which is not all public information, specifically improved the series resistance which in

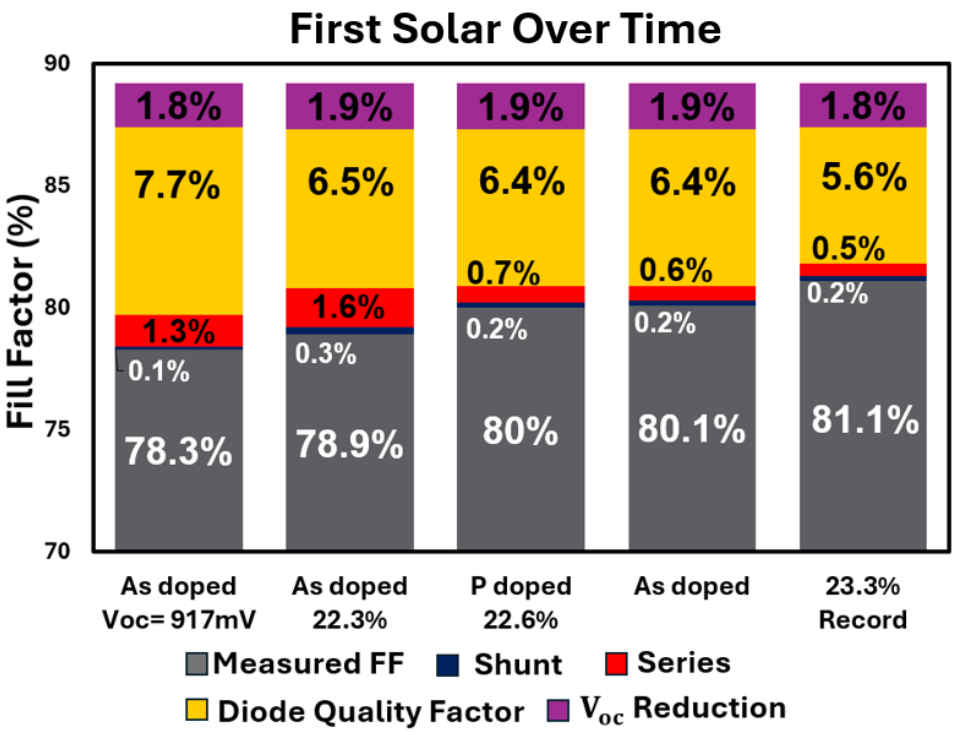


**Figure 3.11:** Visual comparison of ideal FF values (given on top of the bars) to measured values (given in grey part of the bars). The total FF loss is separated into contributions from the individual diode parameters.

turn increased the device performance. The current record CdTe cell is shown in Fig. 3.11 as the 23.3% record. In this case nearly all the improvement in FF came from improved diode quality factor, suggesting that whatever changes were made to reach this device specifically improved the absorber quality.

Tracking top devices over time demonstrates the value of performing this loss analysis. When more details are known about the changes being made to devices, information can be gained as to how processes are fundamentally impacting the device performance and where focus should be put to see the largest increase in FF.

## 3.5 Multi-Junction Devices

So far only analysis on single-junction devices has been discussed, but SQ limit comparison can also be done for multi-junction tandem devices as well. Multi-junction devices

utilize multiple absorber layers in order to improve the PCE of the device. This improvement comes mainly from an increased voltage due to reduced thermalization losses when using multiple absorbers. Tandem devices are set up such that the higher energy photons are absorbed by a high band-gap absorber and the photons that are below the band-gap energy will be absorbed by a later absorber. This allows for a reduction in the thermalization losses, which results in an increased voltage extraction. In this work only tandems with only two absorbers are discussed, but including additional absorbers is possible to achieve higher efficiencies.

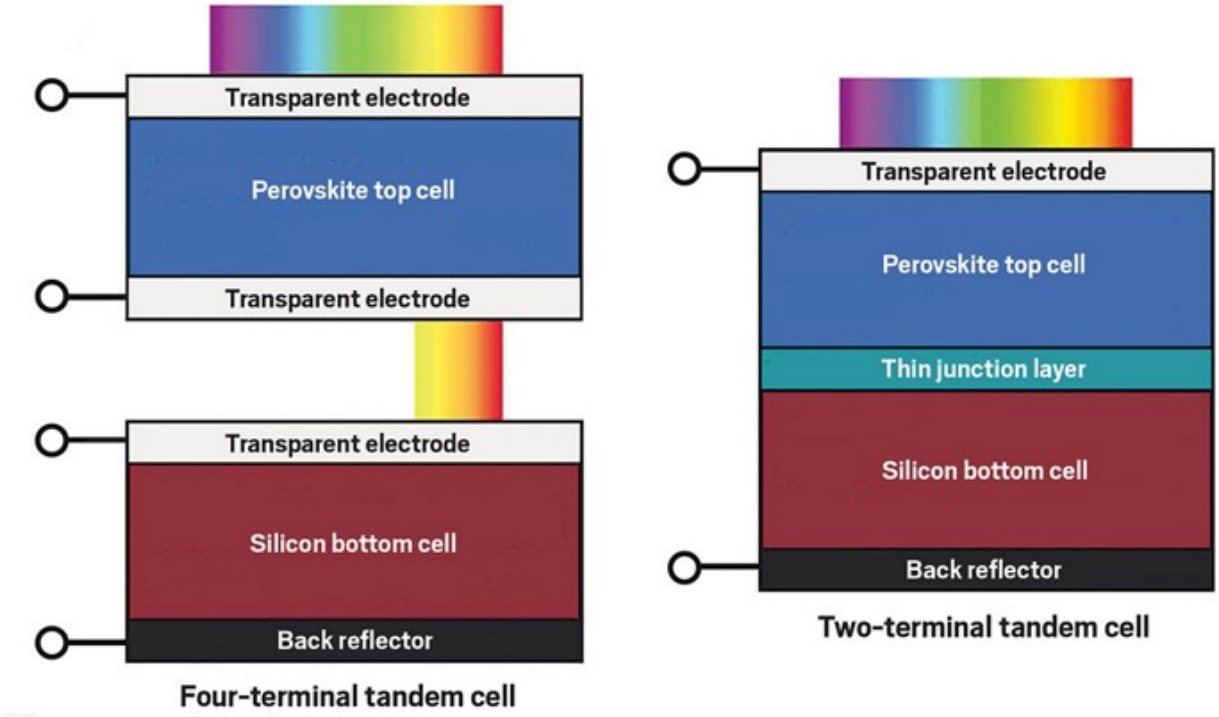


**Figure 3.12:** Example of a two-terminal and four-terminal tandem structure. These examples use perovskite top cells and silicon bottom cells. Image from [55].

Tandem devices are more complex and difficult to fabricate than single junction devices, which is why they are not yet prevalent in the commercial market. Typically the higher PCE they produce is valuable for space applications where the cost of the panel itself is small compared to the launch cost into space. There are two types of two-junction tandem

devices, two-terminal and four-terminal, with example structures shown in Fig. 3.12. In two-terminal devices, current is extracted with contacts at the front of the cell and after both absorbers. This leads to a current-limiting effect where the current throughout the device is limited by the lower of the two absorbers. Designing tandems so that they are current match is a vital part of two-terminal device construction. Four-terminal devices do not have this current limiting problem, because power is extracted after each absorber individually. The lower energy photons still reach the second absorber, but the device does not need to incorporate current matching to reach high efficiencies. Regardless of the junction choice, the implementation of two absorbers impacts the theoretical limit of devices.

Shockley and Queisser calculated the theoretical limit for single junction devices, but when implementing the calculation to multiple absorbers, it is called the detailed balance limit (DB limit). The overall principle of the calculation is the same as discussed at the beginning of this chapter, but adjustments accounting for the thermalization differences must be made. For this work the detailed balance limit was calculated by Dr. Marko Jošt at the University of Ljubljana.

### 3.5.1 Record Perovskite Multi-Junctions

Comparison of multi-junction technologies is not as straightforward as with single-junction cells, but they have also made significant progress, especially two-terminal ones with thin-film perovskite cells. Table 3.7 summarizes the J-V parameters and efficiencies reported for perovskite top cells on crystalline Si [56], thin-film CIGS [57], and a lower-gap thin-film perovskite with a band gap of 1.2 eV [58]. The top cell had a band gap of 1.68 eV on the 1.12 eV bottom cells with Si and CIGS, while the perovskite only tandem had a top cell with a 1.79 eV band gap. Four-terminal tandem cells with perovskites have also shown respectable efficiencies [59, 60], but are not included in the comparisons here. Perovskite specific tandems were chosen due to the tunability of perovskite band-gaps. This makes tandem devices with perovskite top cells a very attractive choice for researchers.

The theoretical parameter limits for specific two-terminal cells depend on the band gaps of both absorber materials and can be calculated [61, 62] from these band gap values. Ideal efficiencies for the three cells in Refs. [56, 57, 58] are in the ∼43-45% range, but are subject to at least two caveats. One is the thickness of the top cell, and the other is whether radiative coupling is included. The decisions here were to assume that ideally all photons with energies below the top-cell gap would be transmitted to the bottom cell and to defer inclusion of radiative coupling until experimental values for these cells get closer to their ideal.

| Tandem Configuration | $V_{oc}$ [V] | $J_{sc}$[mA/cm$^2$] | FF [%] | PCE [%] |
|---|---|---|---|---|
| Perovskite/ Si | 1.95 | 20.9 | 80.5 | 32.8 |
| Perovskite/ Perovskite | 2.11 | 16.5 | 81.9 | 28.5 |
| Perovskite/ CIGS | 1.77 | 18.8 | 71.2 | 24.2 |

**Table 3.7:** Main performance parameters for the tandem devices investigated.

Comparisons of parameters to ideal values for the three cells evaluated are shown in Fig. 3.13, and their full J-V curves are overlaid in Fig. 3.14 (a), then normalized to their approximate ideal currents and voltages in Fig. 3.14 (b). In large part due to the highest bottom-cell $J_{sc}$ of the three, the tandem cell with crystalline Si had the highest current and the largest relative efficiency of about ∼73%. Among two-terminal, thin-film tandems, perovskite/perovskite devices achieved good normalized $FF$ and $V_{oc}$, but low current limited the overall PCE to ∼67% of the SQ limit.

The PCEs of these tandem research devices are still quite far from the detailed balance limit compared to their single-junction tandem counterparts. The perovskite/Si tandem

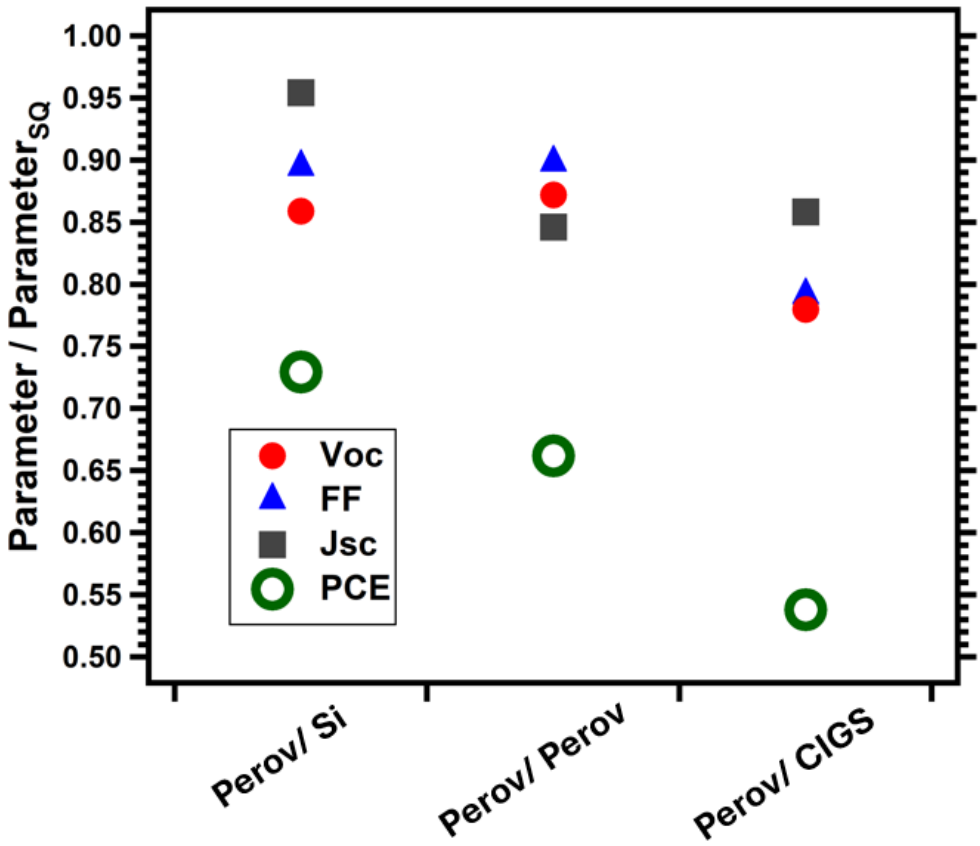


**Figure 3.13:** Comparing individual parameters to the detailed balance limit for tandem devices.

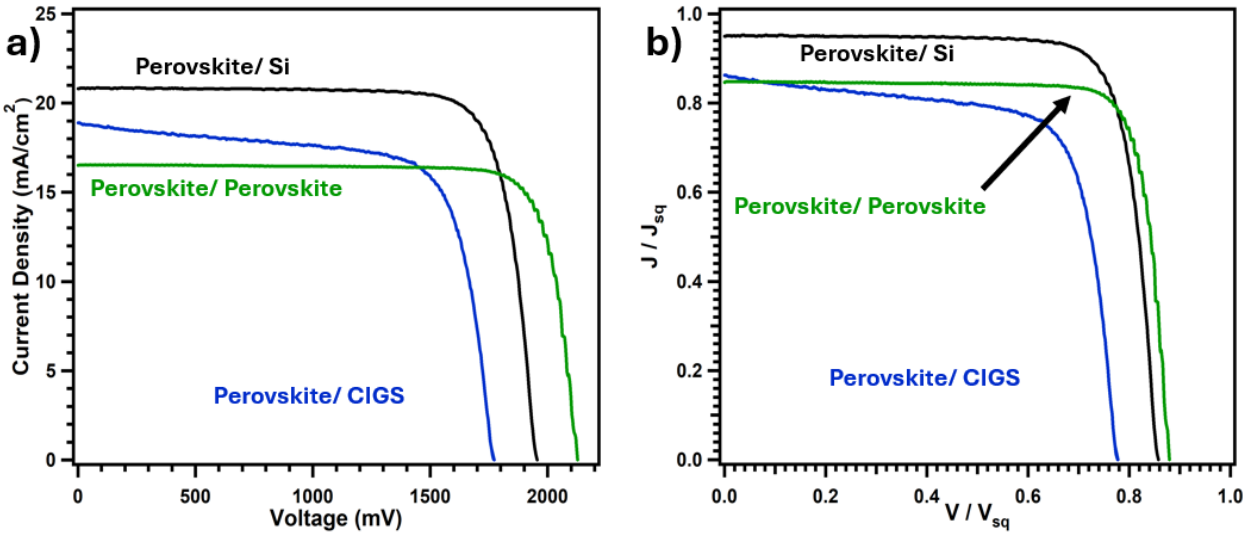


**Figure 3.14:** a) J-V curves for multi-junction cells investigated. b) J-V curves normalized to the SQ limit for multi-junction cells.

reached 73% of its maximum efficiency while the perovskite and Si single-junction cells each reached 83%. This is due at least in part to the additional complexities, such as recombination junctions, involved in constructing tandem devices. These additional complexities add loss pathways that are absent in single-junction devices.

Although the perovskite/Si and perovskite/CIGS devices had nearly the same band gaps for the top and bottom cells, the perovskite/CIGS devices reached a $V_{oc}$ and $FF$ of only ∼77% and ∼78% of their theoretical limit, respectively. This led the tandem combination to have the lowest normalized PCE at ∼54%. The normalized $J_{sc}$ for the perovskite/CIGS tandem was slightly higher than the perovskite/perovskite tandem at 87%. Each of these tandem devices produced a higher PCE than their single-junction counterparts, but comparison to the detailed balance limit shows there is room for significant improvement in these technologies.

Performing detailed diode analysis on multi-junction devices will require significant modification to the analysis procedure and additional measurements of those cells [63]. The fill-factor analysis in particular would need to be modified because it depends heavily on the SQ limits for a single band-gap. Separating the fill-factor losses in tandem cells is beyond the scope of this investigation, but doing so would shed additional light on issues facing the multi-junction technologies.

## 3.6 Loss-Analysis Summary

Comparing device performance to the theoretical limit is valuable to better understand how devices can improve. Analysis of record single-junction devices from different technologies revealed that most technologies extract nearly all the current available but still have room to improve voltage extraction. Detailed analysis comparing the fill-factor to the Shockley-Queisser limit showed that poly-crystalline devices have a larger diode quality factor than single-crystal ones that leads to reduced fill-factor compared to single crystal devices. This analysis was also done on different CdTe samples from different laboratories,

with different absorber thicknesses, and on records over time to extract information on how to improve CdTe devices going forward.

Two-terminal multi-junction tandem devices with perovskite bottom cells were also compared to the theoretical limit to learn where these devices have the most room for improvement. These devices have higher overall efficiencies, but the normalized PCEs are lower than those of single-junction devices. Detailed fill-factor loss analysis was not done on these tandem devices due to the additional complexities involved in tandem devices. Adaptation of the diode and fill-factor loss analysis is required to further investigate these multi-junction devices.

# Chapter 4

BACK-CONTACT BUFFER LAYERS

Creating good ohmic contact for a semiconductor device requires conductivity, favorable energy band alignment, and defect passivation. Achieving this for hole extraction at the back of CdTe devices has been a challenge for researchers. This chapter focuses on different material layers, tellurium dioxide ($TeO_2$) and cadmium zinc telluride (CdZnTe), to passivate defects and improve band alignment. $TeO_2$ was used to attempt to reduce dangling bonds at the back surface of CdTe, while CdZnTe was used to adjust the band alignment using an electron reflector method discussed in the next section. Doping, when these layers are incorporated, is discussed as it plays an important roll in the band alignment and creating good conductivity. The optimization of an absorber layer, and control device, used in back-contact experiments is presented. Experiments and measurements optimizing and investigating the different back-contact layers are presented before the results and suggested next steps are explained.

## 4.1 CdTe Back-Contact Challenges

When a semiconductor is brought into contact with a metal electrode the Fermi-levels of each are required to match up [9]. The Fermi-levels of the metal and semiconductor depends on the work function of the material, while the valance band position of the semiconductor depends on the ionization potential. In order to make ohmic contact, the valence band, which is transporting the holes, must not bend significantly downwards at the back of the device where it is contacted with a metal back electrode. CdTe has problems achieving this for two main reasons; the high ionization potential of CdTe ($\sim$5.8 eV) and the low doping efficiency seen in CdTe devices [28]. The former is a problem because no metal has a high enough work function to match CdTe's ionization potential. Low doping efficiency increases

the energy difference between the Fermi-level and the valence band. Both of these issues lead to downward band-bending at the back interface of CdTe devices creating a barrier to hole extraction with an example shown in Fig. 2.8.

In recent years, research has focused on improving doping in order to improve the voltage. Historically copper-doping treatments were used on CdTe absorbers, but had numerous problems. One problem is the diffusion of Cu atoms in CdTe over time causing degradation of performance, and with commercial modules being in use for upwards of 30 years this can have a large impact. The other main issue is that Cu has had low activation, $< 1\%$, meaning the number of dopant atoms creating carriers is a small faction of the dopant atoms introduced to the absorber. This leads to both low carrier concentration and a large number of impurity atoms creating defect states. Researchers now often utilize arsenic and phosphorous to increase the activation and improve the voltage of CdTe devices. By increasing doping, the Fermi-level moves closer to the valence ban, limiting the downward band-bending that harms performance. Doping is an active area of research yielding good results [64, 65], but is not the primary focus of improving the back-contact pursued in this work. That being said, the relation of doping to Fermi-levels and band-bending does play an important role in understanding back-contact dynamics and plays an important role in creating a proper contact with the materials discussed in this work as will be discussed at length.

Another issue at the back-contact is interface recombination. Whenever two materials are brought together to form an interface defect states will form. The change in lattice structure creates vacancies in the crystal lattice, leading to defect states causing non-radiative recombination. These interface defect states can impact the Fermi-level by increasing the number of carriers within the band-gap due to trapping, causing the Fermi-level to be further away from the valence band. This concept, sometimes refereed to as Fermi-level pinning, holds the Fermi-level at a specific energy within the band-gap and makes it difficult to favorably adjust this location with doping. Defect states at the interface also cause high levels of non-radiative recombination which harms device performance. Due to these concerns,

reducing recombination at the back interface of CdTe devices is important to improve the $V_{oc}$ of devices and will be explored in the work presented.

There are multiple concepts researchers use in an attempt to decrease recombination at the back surface. CdTe surface preparation is one method being investigated to improve the back interface. Making the CdTe Cd rich or Te rich at the surface impacts the recombination at the back surface [28]. Many methods for adjusting surface conditions have been investigated, and continue to be investigated, such as adjusting growth parameters and chemical etching to determine what CdTe surface is best for contacting [66, 67]. The two main methods investigated in this work are additive passivation and electron-reflection layers. The passivation method involves depositing a thin oxide layer to passivate any dangling bonds on the surface. If these defect states are passivated, they will not contribute to electron-hole recombination. The electron-reflector concept involves a back buffer layer with a higher conduction band such that electrons see an energy barrier at the back and are repelled. If the electrons are not present at the interface they are not able to recombine with holes, thus reducing the recombination rate at the back interface.

## 4.2 Thin-Absorber Optimization

In order to investigate back-contact properties, carriers must be present at the back interface. In recent years the bulk lifetimes of carriers have significantly improved, making it easier for them to reach that back-contact. To further increase the number of carriers at the back-contact a thinner absorber is helpful. CdTe devices require only $\sim$ 1-μm thick absorbers to absorb 98% of the incoming light, but absorbers are typically made $\sim$ 3-μm thick because of the potential problems with the back surface. By using thinner absorbers, more light will be absorbed closer to the back interface, and carriers are more likely to reach the back surface increasing its impact on device performance. Thus, before experimenting with back-contact layers, it is prudent to create a good baseline device that utilizes a thinner absorber than is standard. The deposition systems' operation can fluctuate over time, so making the same

control device every experiment provides insight into how good the depositions are the day of the experiment.

At CSU the standard absorbers are 3-4-μm thick and utilize an optimized bulk-passivating $CdCl_2$ treatment and a CuCl-doping treatment. In order to fabricate a thin absorber with a good PCE, these treatments must be adjusted. These thin absorbers devices were deposited on TEC10 glass substrates with 100 nm of MgZnO deposited on it as an n-type window layer. The absorbers are a CdSeTe/CdTe graded bilayer absorber with a fixed 0.5 μm of CdSeTe deposited first. Absorbers used 1 and 1.5 μm of CdTe, deposited on top of the CdSeTe, before the $CdCl_2$ and CuCl treatments that were done as described in chapter 2). A thin layer of ∼40 nm of elemental Te was deposited after the CuCl treatment before the back electrode was deposited. A general device structure is shown in Fig. 4.1. Dr. Jennifer Drayton was an immense help running the fabrication systems and discussing results during these optimization experiments.

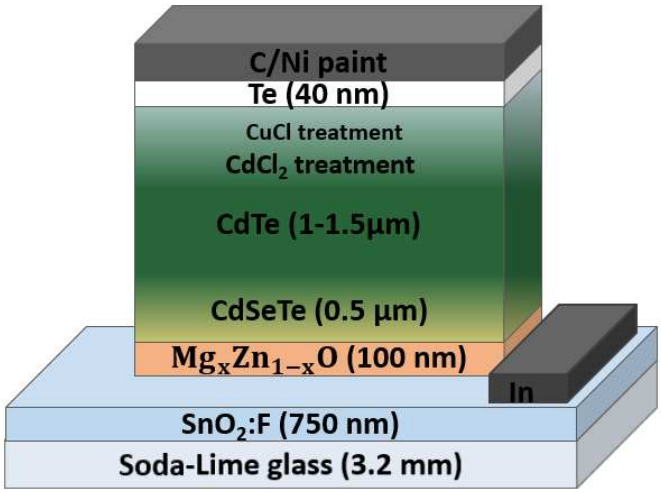


**Figure 4.1:** Generic device structure for experiments optimizing a thin absorber.

### 4.2.1 Cadmium Chloride Passivation Optimization

The $CdCl_2$ treatment is done after the absorber deposition to increase grain size and passivate grain boundaries in the CdTe absorber [22]. There are numerous parameters to

take into account during this treatment such as source temperatures as well as background gas pressure and composition. This optimization focused on the dose and anneal times. The dose time refers to the amount of time where the substrate is positioned over the $CdCl_2$ source that is sublimating the $CdCl_2$ onto the substrate. The anneal time is done in a separate source, without $CdCl_2$, and is the time the plate is held at an elevated temperature to diffuse the previously deposited $CdCl_2$ through the grain boundaries. The treatments shown in this work were done with approximately 40 mTorr of nitrogen as the background gas, with 400°C anneal temperatures and approximately 450°C dose temperature.

Similar optimization was done in the past by Dr. Alexandra Bothwell, and her results influenced the starting points for these optimization experiments [36]. The $CdCl_2$ dose time was varied from 250 to 350 seconds in steps of 50 seconds to get a large relative range of dose times. The anneal times were also varied, in the same experiment, between 210 and 260 seconds. Optimizing multiple parameters at once allows for greater confidence that a true maximum is reached rather than a local one. Twenty-five devices are fabricated on a single substrate plate, and the highest average performing substrate was chosen going forward. All substrates had comparable performances that ranged from 12 to 16%. The device with a 350-s of dose time and 210-s anneal time produced the best and most consistent devices in this experiment, and other similar experiments. The devices with these treatment times, which reached a $V_{oc}$ of 840 mV and a PCE of just over 16%, were used for future thin absorber experiments.

### 4.2.2 Copper Chloride Passivation Optimization

After the $CdCl_2$ treatment was optimized, the CuCl doping treatment was investigated. The temperatures always used in the CuCl doping treatment, $\sim$ 190°C dose and 200°C anneal, are sufficiently low as to not cause $CdCl_2$ diffusion [68]. Thus changing the CuCl treatment does not affect the optimized $CdCl_2$ treatment discussed in the previous section. The range parameters were being adjusted was again influenced by Alex Bothwell's previous

optimization which showed a much shorter dose and anneal time, ∼5-s dose and ∼200-s anneal, is needed for thin absorbers compared to the standard CSU devices.

Experiments with longer than 35-s dose time on thin absorbers showed significant non-uniformity. To finalize the CuCl optimization, an experiment keeping the dose time at or under 35-s was performed. The results determined that the 35-s dose time had the best performance and the mean device outperformed others in every parameter. The $V_{oc}$ uniformity was not as consistent as desired, but the consistency in other parameters made the 35-s dose time the clear choice moving forward.

### 4.2.3 Absorbers used for Back-Contact Experiments

Initially 1.5-μm absorbers were used for some back-contact experiments, but it was later decided that they yielded results that were too inconsistent. Any variation in absorber thickness across the plate means little when the absorber is ∼3 μm thick, but can have a large impact when working with 1.5-μm absorbers. CSU 1.5-μm absorbers were used for some of the back-contact research shown in the next section, but to avoid the issues with the system and promote consistency across experiments, the First Solar company was requested to provide additional absorbers for further experiments.

The First Solar absorbers used were deposited on glass that also had an MgZnO n-type window layer at the front. A thin layer of CdSe was deposited on this window layer before CdTe, then the Se was annealed in such a way that created a graded CdSeTe/CdTe absorber that was approximately 3-μm thick. This absorber was then given an unspecified $CdCl_2$ treatment along with an arsenic-doping treatment. These absorbers, called FS200 absorbers, were then shipped from a fabrication facility in Perrysburg, Ohio to CSU for back-contact depositions.

The absorbers used in this work switched from CSU to First Solar absorbers to achieve more consistency and confidence in results. With the consistent First Solar absorbers, any change in performance can confidently be attributed to the experimental parameters being

tested rather than absorber variations. In the following sections the absorber used, CSU or First Solar, will be specified to avoid confusion.

## 4.3 Tellurium Oxide

One way to reduce recombination at the back of devices is to passivate the dangling bonds creating the defect states. The incorporation of oxides at the front of CdTe devices has reduced parasitic absorption, recombination, and increased the overall device performance [69]. Work elsewhere with silicon devices has shown the use of metal oxides as a hole selective transport layer for dopant free devices [70]. This sparked interest in the CdTe community to use metal oxides at the back contact to help with the doping and recombination issues CdTe struggles with.[28]. Materials such as aluminum oxide, molybdenum oxide, and more have shown promise in these areas [71, 72, 73].

Previous work at CSU, by Dr. Adam Danielson and Dr. Carey Reich, demonstrated favorable passivating affects from a naturally forming layer of tellurium dioxide ($TeO_2$) [74]. The formation of this native $TeO_2$ layer, and corresponding device improvement, has also been observed by other research groups [75, 76]. This layer forms when CdTe is exposed to air or oxygen for varying periods of time and has shown an increase of external radiative efficiency (ERE) which is a measurement of recombination in films. In parallel, former CSU student Dr. Ramesh Pandey began purposefully depositing $TeO_2$ to examine the possible passivating affects [30]. As he transitioned out of the laboratory, I took over this work and the results are presented below. The $TeO_2$ layer presented in this work was deposited by RF sputtering using a power density applied to the target of 0.75 $W^2/cm^2$ with a background pressure of 18 mTorr of argon gas.

### 4.3.1 $CdCl_2$ Treatment of CSU Absorbers

The first fabrication parameter investigated was the $CdCl_2$ treatment used on the $TeO_2$ devices. Ramesh showed previously that a modified $CdCl_2$ treatment was required when

using $TeO_2$. This was then investigated further to test if a second passivation treatment is required after the $TeO_2$ deposition, the J-V curves for this experiment is shown in Fig. 4.2. The results showed that when a $CdCl_2$ treatment is done only before the $TeO_2$ layer, no current was extracted. Oxides are known to be highly resistive, and $TeO_2$ has a high band-gap of ~3.4 eV, making it difficult for current to pass through a thick layer. For this reason the tellurium oxide layer was kept at or below 10 nm in thickness. This result also showed the importance of performing a passivation treatment after the $TeO_2$ layer is deposited in order to get any significant PCE out of the device.

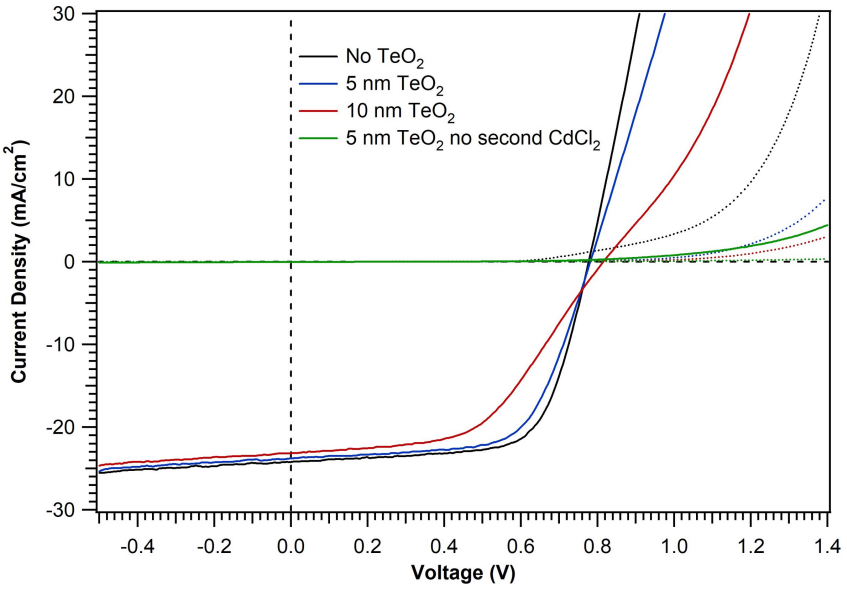


**Figure 4.2:** J-V curves of $TeO_2$ devices with different $CdCl_2$ treatments.

Knowing that a passivation treatment is required after the $TeO_2$ raised the question of whether only a single $CdCl_2$ treatment after the $TeO_2$ layer would be sufficient to passivate both the absorber and the interface. Devices with only a single $CdCl_2$ treatment, however, performed far worse than those with a double passivation treatment. Average efficiencies went from 8.5% and 7.6%, for 5 nm and 10 nm respectively, to 17.1% and 16% when passivation was done before and after the $TeO_2$ layer as shown in Fig. 4.3. A major improvement in performance uniformity was also noticed when including two $CdCl_2$ treatments. These improvements were present in all J-V parameters measured.

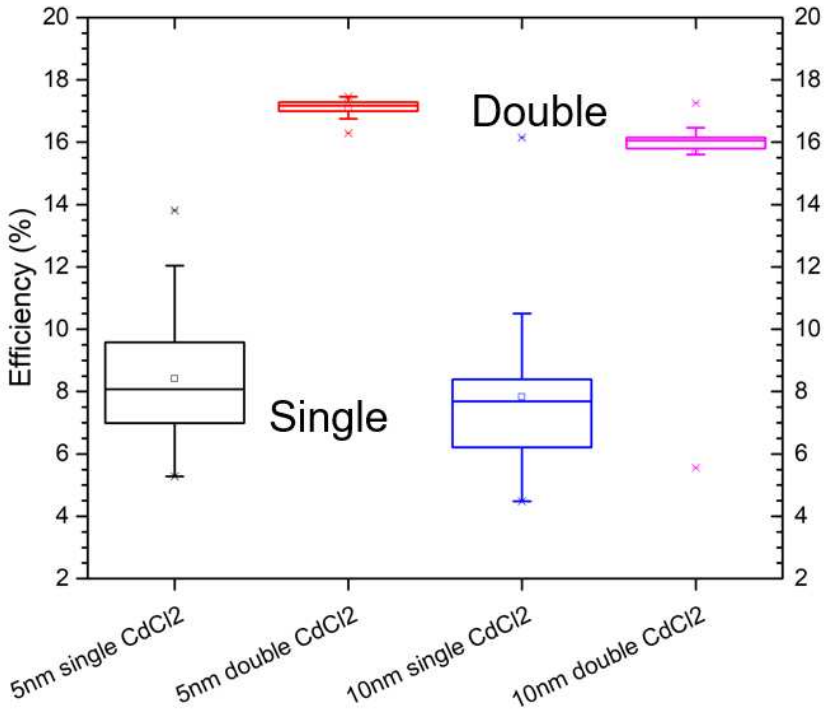


**Figure 4.3:** Efficiency box plots of $TeO_2$ devices with different $CdCl_2$ treatments.

Admittance measurements were used to create carrier-density plots shown in Fig. 4.4. Devices with two $CdCl_2$ treatments, which were made by Dr. Pandey, had an order of magnitude increase, from 1E14 to 1E15 carriers per cubic centimeter, in carrier density compared to single treatment devices which were fabricated jointly by Dr. Pandey and I. The zero bias point for the double $CdCl_2$ devices is at the bottom of the curve, while it is on the right branch of the single treated devices. This indicates the absorbers become fully depleted at smaller voltage bias when only a single $CdCl_2$ treatment is used. The change in width of the U-shape in Fig. 4.4 also indicates the p-n junction occurs closer to the front interface for devices, which is preferable, with two passivation treatments.

These results showed the importance of passivation before the $TeO_2$ layer to ensure bulk passivation, and treatment after the $TeO_2$ for interface passivation. A single $CdCl_2$ passivation treatment done after the $TeO_2$ layer was not adequate to passivate both the interface and the bulk absorber.

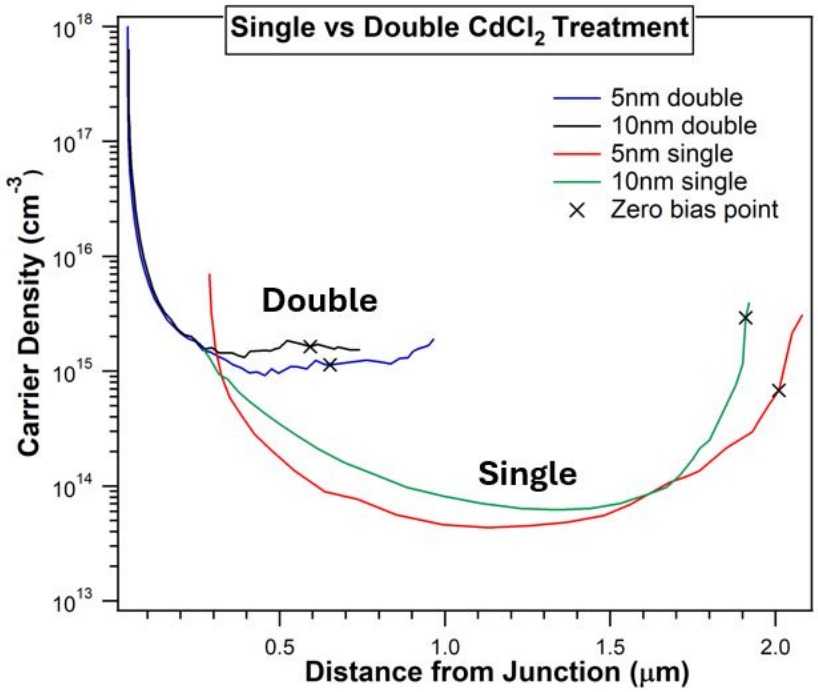


**Figure 4.4:** Carrier-density plot showing the difference between one and two $CdCl_2$ treatments. Zero voltage-bias point indicated.

### Photoluminescence

The purpose of both the passivation treatment and the $TeO_2$ layer is to reduce recombination in these films. As discussed in chapter 2), photoluminescence provides insight into the recombination of devices, and Fig. 4.5 shows the progression of PL signal for two devices between deposition steps. The front-side measurements show a slight increase in PL signal after the deposition of $TeO_2$ and a large increase after the second passivation step. The slight increase after the $TeO_2$ does not stand out as significant evidence of passivation, but the second $CdCl_2$ treatment clearly shows an increase in PL indicating reduced recombination. This is exemplified in Fig. 4.5 (b) where there is little to no difference during the $TeO_2$ step, but a very significant increase after the second $CdCl_2$ treatment.

These photoluminescence measurements support the earlier evidence that when depositing $TeO_x$ on CSU absorbers a second $CdCl_2$ treatment is required to get the best performance out of the device.

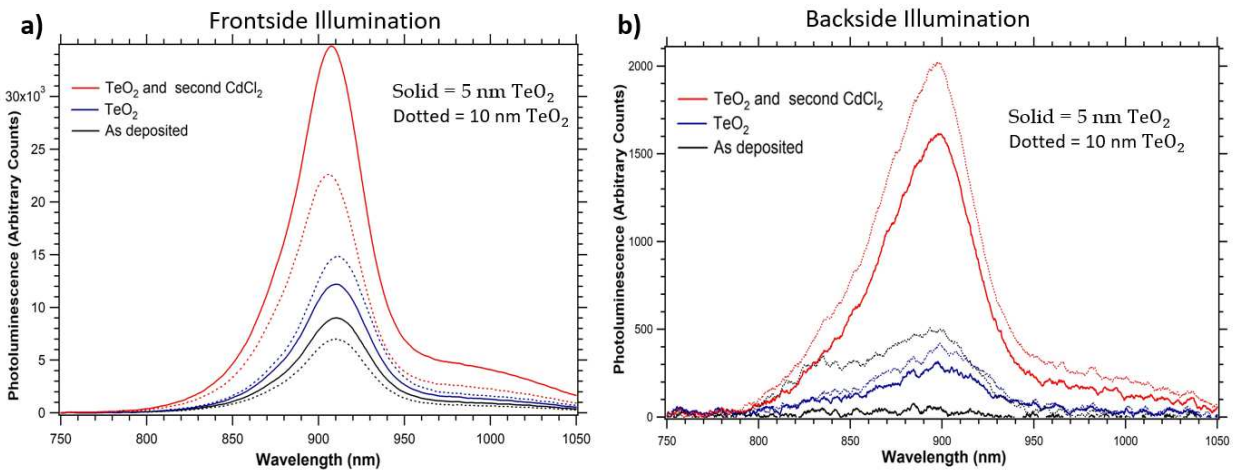


**Figure 4.5:** Photoluminesce on the same device at each step of the $TeO_2$ process. Solid and dotted lines represent separate devices. a) Frontside illumination b) Backside illumination.

### 4.3.2 Doping of CSU $TeO_2$ Devices

One of the major reasons for using $TeO_2$ was the success Si devices had with metal oxides as a dopant-free back contact. CSU CdTe devices are typically copper-doped in order to increase carrier concentration and improve the voltage. As mentioned above, there are many issues involved with Cu doping, so the $TeO_2$ devices here were initially fabricated without any intentional Cu doping. One reason for a Cu-free device structure not mentioned above is the impact Cu has on the carrier lifetime with an example shown in Fig. 4.6 using time-resolved photoluminescence (TRPL). The devices without Cu doping, including the $TeO_2$ devices, had significantly longer lifetimes compared to the Cu device. This exemplifies the negative impact of Cu on carrier lifetime, which is related to the $V_{oc}$ of devices [77].

Undoped and doped devices were made with different thicknesses of $TeO_2$ to compare both the impact thickness has on performance, and if thickness matters for the impact of copper doping. The J-V parameters were measured and the results of the undoped devices are shown in Fig. 4.7. On average, the efficiencies for devices without copper doping outperformed devices with copper doping. Devices with $TeO_2$ demonstrated significant improvement when there is no copper doping. For a 5-nm $TeO_2$ layer the average efficiencies went from 14.8% to 17.1% while the average $V_{oc}$ went from 779 mV to 808 mV when copper

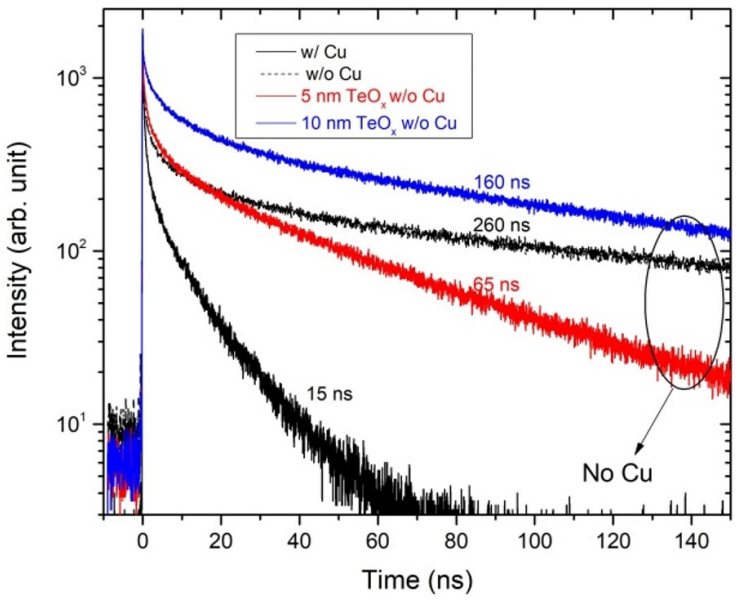


**Figure 4.6:** Time-resolved photoluminescence measurements of Cu doping and $TeO_x$ devices. Plot taken from [30].

was excluded. The same favorable trend for $TeO_2$ devices without copper was shown for the 10-nm devices. $TeO_2$ devices without copper not only have better overall performance than doped devices, but the uniformity across the twenty-five-device plate was significantly better.

Based on the results from these devices, which were fabricated by Dr.Pandey, it is clear the 5-nm devices outperformed the thicker 10-nm devices in every parameter, with the best 5-nm device reaching 17.5% efficiency with a $V_{oc}$ of 829 mV. While the $J_{sc}$ between the 5-nm and 10-nm devices seemed unaffected, the better efficiency with 5-nm can be attributed to higher fill-factor and $V_{oc}$. When the thickness of $TeO_2$ was increased to 20-nm, the device performance was further reduced.

Temperature-dependent current-voltage (J-V-T) measurements, taken by me and shown in Fig. 4.8, were done to study the back barrier of $TeO_2$ devices. As the temperature is decreased the device with copper-doping exhibited a rollover effect, indicative of the formation of a back-contact barrier that inhibits current flow in forward bias. The device without the intentional copper-doping did not demonstrate this rollover effect. This suggests $TeO_2$ does

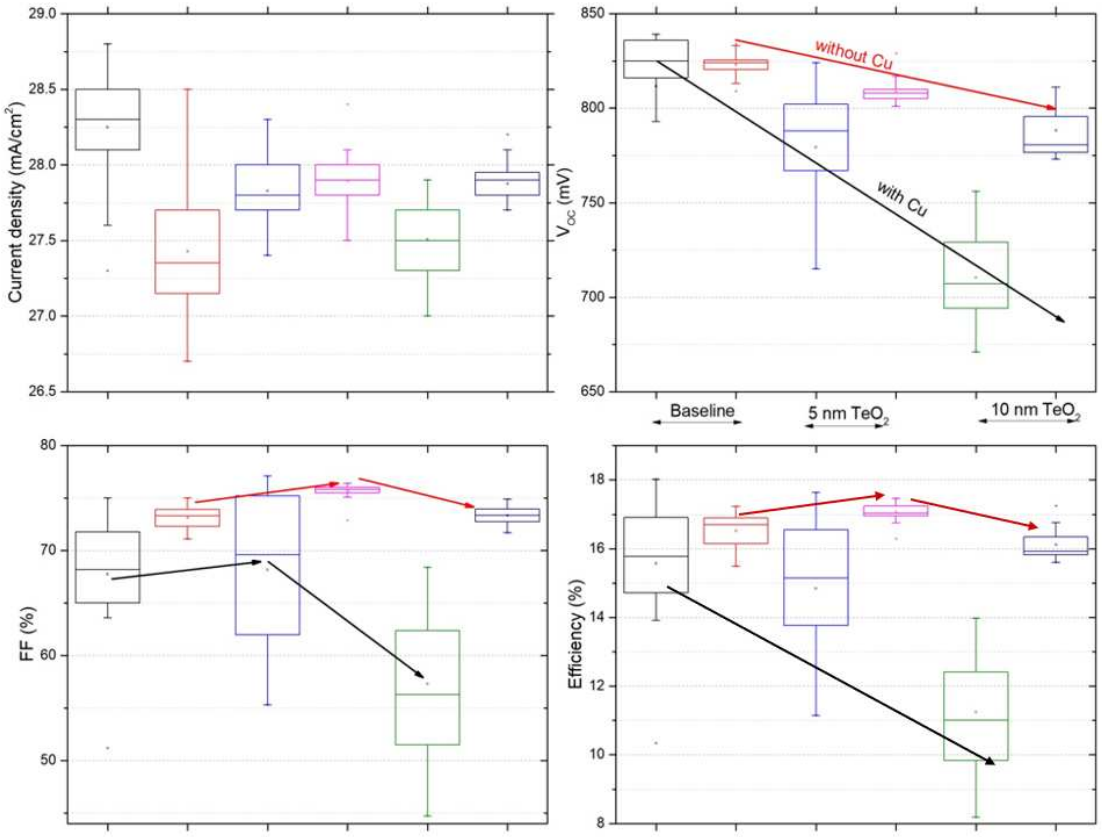


**Figure 4.7:** Box plots comparing parameter performance for $TeO_2$ devices with and without Cu doping.

not create a large hole barrier by itself, but the intentional copper doping in conjunction with the $TeO_2$ lead to current limitation in forward bias. This is unexpected because Cu is typically used to improve the back barrier but in this case an interaction with the $TeO_2$ causes an increase in hole barrier energy. In a plot not shown, a J-V-T measurement was taken on an arsenic doped $TeO_2$ device and did not show any rollover effect down to 233 K. This indicates the formation of an energy barrier is not due to other dopants, but specifically due to a Cu interaction with the $TeO_2$. There was, however, a decrease in the fill-factor with the undoped $TeO_2$ as well, likely due to reduced carrier density in the front buffer layer.

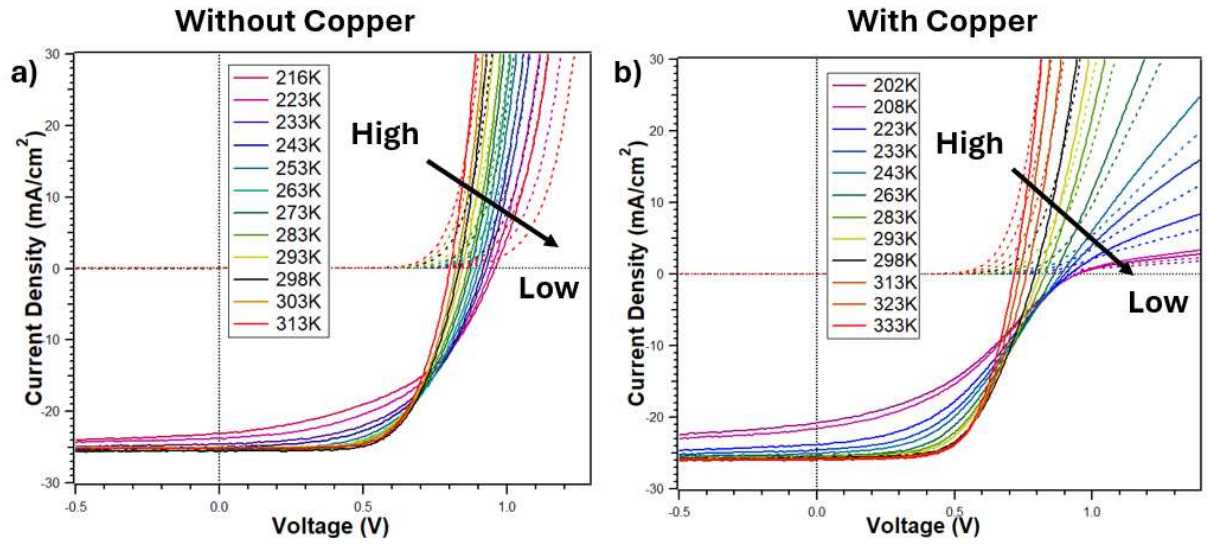


**Figure 4.8:** Temperature dependent current-voltage plots comparing $TeO_x$ devices a) Without copper a CuCl treatment b) With a CuCl treatment.

### 4.3.3 Photoluminescence on First Solar Absorbers With $TeO_x$

#### Wet $CdCl_2$ Deposition

The first devices made with FS200 absorbers were done with a non-standard wet $CdCl_2$ treatment at CSU. None of these devices performed well, with the best PCE being 6.8%. The device that received a $TeO_2$ deposition, but not second $CdCl_2$ passivation treatment, performed the worst by far, supporting the conclusion that the second passivation treatment is crucial when including a $TeO_2$ layer.

Photoluminescence measurements on these devices were taken to determine the effect of the $TeO_2$ and wet $CdCl_2$ treatment on recombination, with the results shown in Fig. 4.9. The PL signal did not change significantly after the $TeO_2$ depositions, as had been seen in CSU absorbers, but the wet $CdCl_2$ treatment both dramatically lowered the PL signal and moved the peak to a lower wavelength. The conclusion is that the wet $CdCl_2$ treatment was not optimized and thus produced poor results. Another explanation relates to the dopants already active in the FS200 absorber. During CSU absorber experiments the absorber was not doped when the second $CdCl_2$ treatment was done, whereas the First Solar absorbers

already have arsenic. The high temperatures of the second $CdCl_2$ passivation treatment could cause the arsenic, which is optimally placed by First Solar, to diffuse causing issues with increased defect states and dopant location. The Se profile may be affected by the high temperatures as well, causing the change in PL signal peak wavelength.

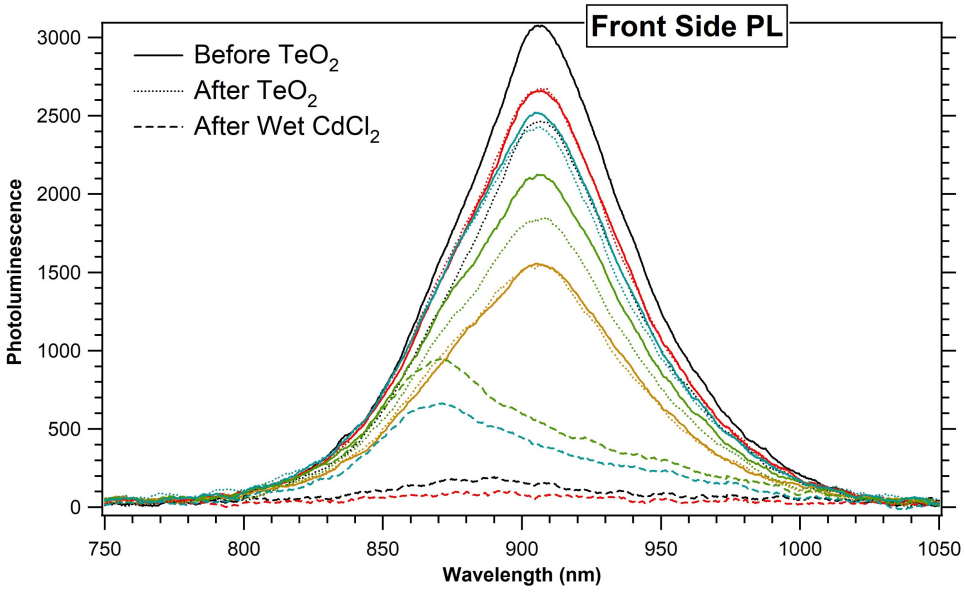


**Figure 4.9:** Photoluminescence signals for devices before and after a $TeO_2$ deposition and a wet $CdCl_2$ treatment.

### Close-Space Sublimation Deposition of $CdCl_2$ on First Solar Absorbers

To account for the high temperatures during a passivation treatment this experiment was repeated with the standard $CdCl_2$ by close-space sublimation (CSS) for a much shorter time. This should limit the negative effects of the second $CdCl_2$ treatment while allowing for the investigation of the $TeO_2$ layer's impact on recombination.

The absorbers used for these experiments were again FS200. The device with $TeO_2$ and a second $CdCl_2$ treatment and the standard Te layer did not perform as well (10.3%) as the device with just the standard Te (12.1%). To better understand what caused this performance difference PL measurements were taken.

At the point of this experiment, the PL system had been upgraded, allowing for investigation of subband-gap features from defect states within the band gap as well as the band

to band recombination. The PL plots, shown in Fig. 4.10, showed a notable increase in signal when the $TeO_2$ was deposited, however most of this increase came from subband-gap features which are generally unfavorable to device performance. Likely this increase in PL signal corresponds to newly formed defect states at the interface as a result of the energetic sputtering deposition of the $TeO_2$. During sputtering depositions, atoms smash into the substrate and can cause defect formation. To avoid this in the future, a greater distance between the target and the substrate is suggested.

The affect of a second $CdCl_2$ was also seen in the blue dashed signals shown in Fig. 4.10. The PL band-gap signal decreased and the sub-band defect features became relatively more pronounced, though more separated form the primary peak, when a second $CdCl_2$ treatment is performed. Even though the second passivation treatment is required to extract current, the second passivation treatment clearly had a negative effect on the recombination within the device. This is again likely due to the high temperatures of the treatment causing diffusion of arsenic and chlorine already present in the FS200 absorber, similar to the effect during the wet $CdCl_2$ treatment.

Another notable feature of Fig. 4.10 is how the subband-gap features dissipated when the elemental Te is deposited on the back. It is possible the Te layer passivated the $TeO_2$ interface in such a way to reduce these defect states, but is unlikely. More likely the Te layer, which highly p-type, impacted the electric field in this location such that the defect states are less important. Determining the exact cause of this sub-band-gap feature decrease requires further investigation.

### 4.3.4 Next Steps for $TeO_2$

Tellurium oxide has shown promise for use in dopant free devices by creating high performance devices without the need to copper-doping. A second passivation treatment is required to passivate the $TeO_2$ layer, but this impacts any doping and passivation already present in the absorber. The process of sputtering $TeO_2$ negatively impacts photoluminescence intensity, which is attributed to surface damage from the energetic deposition process.

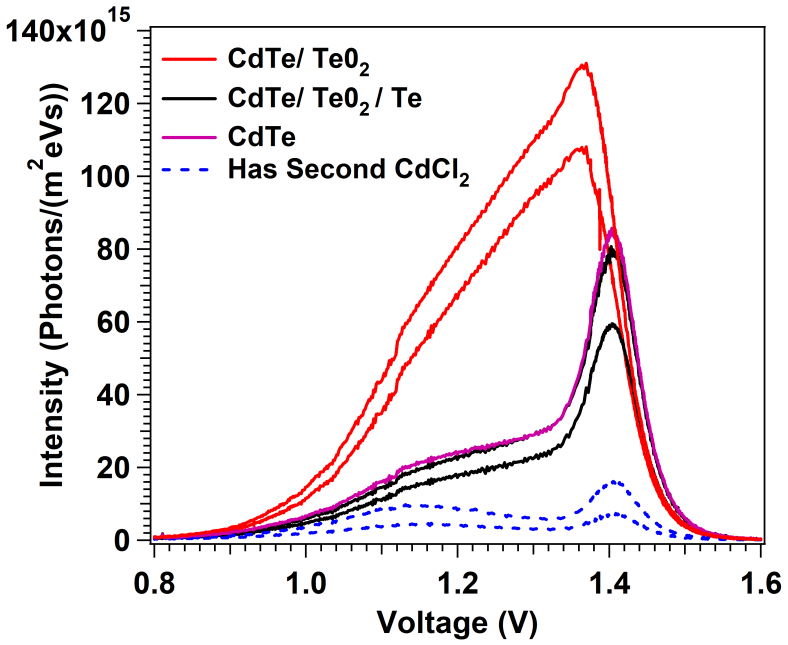


**Figure 4.10:** Photoluminescence signals for devices before and after a $TeO_2$ deposition and a thermally evaporated Te layer. This shows a full spectrum signal due to system upgrades done by Daniel Shaw.

To further explore $TeO_2$ as a passivation layer a less disruptive growth method should be explored to avoid any defect formation at the back interface. The effect of the native $TeO_2$ layer that forms when exposed to oxygen should be accounted for when performing experiments on purposefully deposited $TeO_2$. Better tracking of the time between the absorber and $TeO_2$ depositions is one way to achieve this.

## 4.4 Cadmium Zinc Telluride

Passivating bonds at the interface is one method of reducing recombination at the back surface. Another concept is using an electron reflector, which is when a material of higher band-gap, in this case cadmium zinc telluride (CdZnTe or CZT), is deposited after the absorber to reflect electrons away form the interface [78]. Since the CdZnTe layer has a higher conduction band than the CdTe absorber, the excited electrons will see this as an energy barrier causing the electrons to repel away from the back surface. Without electrons and

holes at the same location they are not able to recombine, thus reducing the recombination at the back interface.

One material quality to keep in mind when creating an electron reflector is the lattice-constant mismatch. The lattice structure needs to remain the same, in this case zincblend, to get the best performance, but the lattice constant plays a large role in the amount of defect states at the interface. CdTe has a lattice constant of 6.48 nm, while ZnTe's is 6.1 nm as shown in Fig. 4.11, along with several other possibilities. This is a relatively good match, but not as good as with magnesium telluride (MgTe) which has a lattice constant of 6.43 nm. In an effort to reduce the lattice mismatch between layers at the back interface alloys such as cadmium zinc telluride can be used. To minimize the lattice mismatch the alloy cadmium magnesium telluride (CdMgTe) was previously researched by Dr. Alexandra Bothwell, but resulted in limited success [36]. One reason for the limited success could be the unfavorable valence band alignment of CdTe and MgTe.

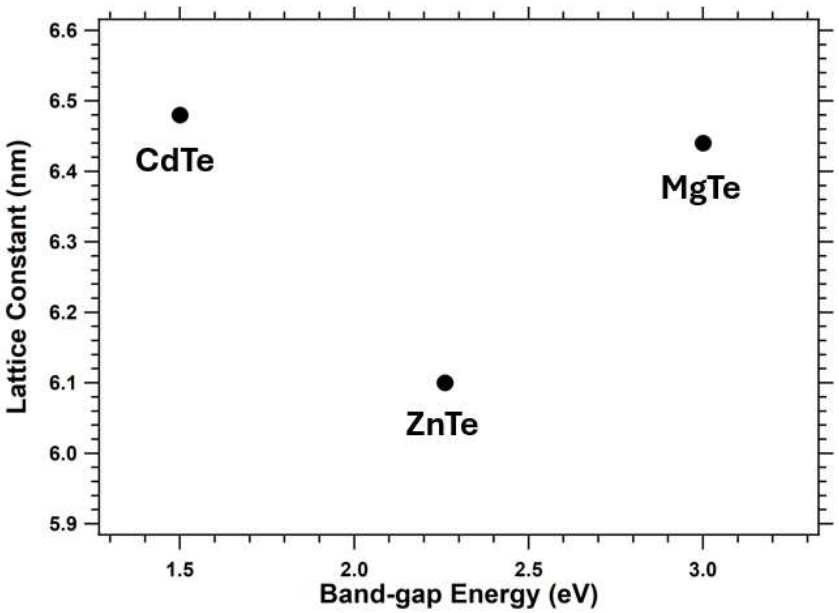


**Figure 4.11:** Lattice constants and band-gaps of common materials used in solar cells. Taken from [77].

The back-surface field present at the interface is important to reflect electrons, while still allowing the holes to be extracted. The conduction-band offset (CBO) determines the effect

on the electron carriers, while the valence-band offset (VBO) impacts the hole carriers. In order to have a good electron reflector, there must be a favorable CBO to reflect electrons, without creating a large mismatch in the VBO. Simulations using the SCAPS-1D program were run to test this, and the results are shown in Fig. 4.12. It shows the importance of maintaining a good VBO when creating an electron reflector (ER) layer. When the valence band of the ER layer matches the CdTe, the highest voltage and PCE is achieved by the black curve in Fig. 4.12. When the VBO is positive, that is the valence band of the ER layer is above the CdTe valence band, the impact is minimal, slightly reducing the $V_{oc}$. Alternatively, when the offset is negative it severely impacts the performance of the device particularly in the voltage and FF. From this modeling, it is clear that a zero VBO gave the best outcome, and a positive VBO is preferable to a negative VBO when making an electron reflector. ZnTe has a favorable VBO to CdTe, making it a prime choice for electron reflector research [79, 80].

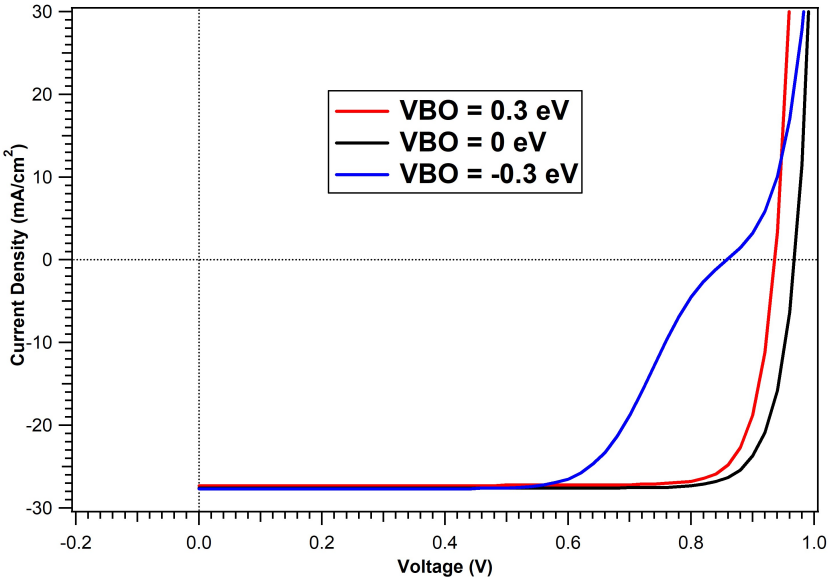


**Figure 4.12:** SCAPS-simulated J-V curves showing the impact of the VBO. The $V_{oc}$ of the curves are Blue = 858 mV, Black = 968 mV, and Red: 936 mV

When actually fabricating an electron reflector, the VBO will depend on the Fermi-level positioning of the CdTe and the ER layer because it must match when the layers are brought into contact. The closer the Fermi-level to the valence band of the ER layer, the

more favorable the VBO will be and the better contact with a metal electrode is likely. As discussed before, doping plays a major roll in determining the position of the Fermi-level with respect to the valence band, and thus proper doping is crucial to fabricating a good electron reflector. Doping, as well as other material properties in ZnTe, has been explored [81, 82, 83] previously with mixed results. ZnTe is also used in the current First Solar panels being sent to market, demonstrating the commercial capabilities of the material. By alloying ZnTe and CdTe to get CdZnTe the favorable band alignment should remain and the lattice mismatch should be reduced compared to a CdTe/ZnTe interface. CdZnTe has also been shown to be more highly doped than CdTe, helping with the band bending at the back-contact [84].

The valence band match, high doping, and reduced lattice mismatch combine to make CdZnTe an attractive choice for electron-reflector research. CdZnTe has been investigated previously at CSU, but mostly as a candidate for a top absorber in tandem applications [85, 86]. The main challenge in this work was passivating the CdZnTe without sublimating the Zn out of the device. A similar problem occurred with magnesium in [36]. The processing temperatures required to passivate the grain boundaries cause zinc loss in the device, leaving it as standard CdTe. To avoid, as much as possible, resistivity problems due to this, the CdZnTe layers are kept thin in the devices used in this work.

In this work a comparison of CdZnTe deposition methods is made and comparisons to baseline devices are used to analyze results. The devices made are characterized with various opto-electronic measurements to investigate the property of devices made. The discussion of remaining limitations are discussed along with possible solutions to overcome limitations.

### 4.4.1 CdZnTe Device Structure and Optimization on CSU Absorbers

The CdZnTe layers in this work were deposited by RF sputtering with a power density of 0.75W/cm$^2$ and 18 mTorr of argon background gas. Devices were initially deposited with close-space sublimation, but non-uniformity led sputtering to be the top choice. As mentioned in previous sections, a thin absorber was used for this electron reflector work.

### Copper Doping Optimization

As before, doping improves the conductivity of a material and brings its Fermi-level closer to the valence band, which are both important to creating a good back-contact. High temperatures cause Cu to diffuse rapidly through the absorber, so to avoid potential issues with copper reaching the front of the device, the CuCl treatment is done after the CZT deposition. By doing it in this order, a single CuCl treatment was used to dope both the CZT and the CdTe.

An extensive experiment was conducted to optimize both the dose and anneal times for CZT. The thickness of the CZT layer was also varied to determine the optimal thickness for different doping treatments. The results of the doping and thickness optimization are shown in Fig. 4.13. Devices with 100 nm of CZT had higher variation across the substrate especially at lower dose and anneal times. The 50 nm CZT devices had better uniformity across the substrate except for the lowest dose and anneal time. It is also noteworthy that the devices with 50 nm of CZT outperformed the control by over 3% total PCE. This showed the positive impact CZT can have at a back-contact layer. This experiment showed the need for long doping treatments when CZT is used, which is in agreement with previous experiments not shown were the control CuCl treatment, 35-s dose and 200-s anneal, was done on a CZT device. In that case, the CZT device performed far worse (3% PCE) than the control device without CZT (10.7% PCE) indicating the CdZnTe layer needs significant doping to extract carriers.This is likely due to the lack of passivation in the CZT layer as well as slow Cu diffusion though the layer. Without the passivation the CZT layer is resistive and requires higher concentrations of Cu to improve conductivity.

### Substrate Temperature During CdZnTe Deposition

The substrate temperature during thin-film depositions has a significant impact on growth parameters and quality. The sputter system used for CZT depositions had a heater built

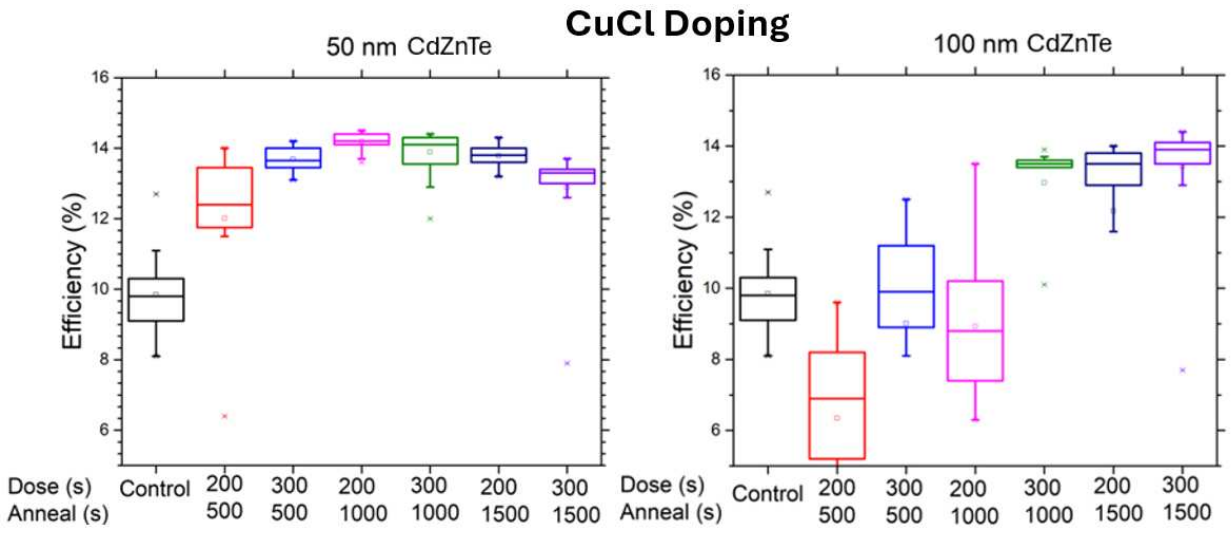


**Figure 4.13:** Efficiency box-plots comparing different CdZnTe thicknesses and doping treatment times.

in, with a metal sheet to ensure uniform thermal distribution, to allow control of the glass substrate during deposition.

As shown in Fig. 4.14, the optimized thin control devices again had lower performance than the devices with CZT. The control device had comparable $V_{oc}$ to the CZT devices, but the FF and $J_{sc}$ were below the others. The device with a 150°C substrate temperature performed the best on average primarily due to increased FF. As discussed in the last chapter, FF loss is often caused by a non-ideal diode quality factor, which can be attributed to unfavorable recombination. The increase in FF for this substrate temperature indicates it is forming the best electronic interface and reducing recombination. While the CZT devices outperforming the control devices, on average, is a good sign, the $V_{oc}$ being mostly unaffected is worrying for the electron reflector concept. The goal of the electron reflector layer is to increase the $V_{oc}$ of devices by reducing recombination at the back surface. Increased FF is a good sign, but not the desired affect.

Photoluminescence measurements were taken on these devices, with the resulting signals shown in Fig. 4.15. There was nearly an order of magnitude increase in PL signal after the deposition of CZT above room temperature. CdZnTe deposited at room temperature had

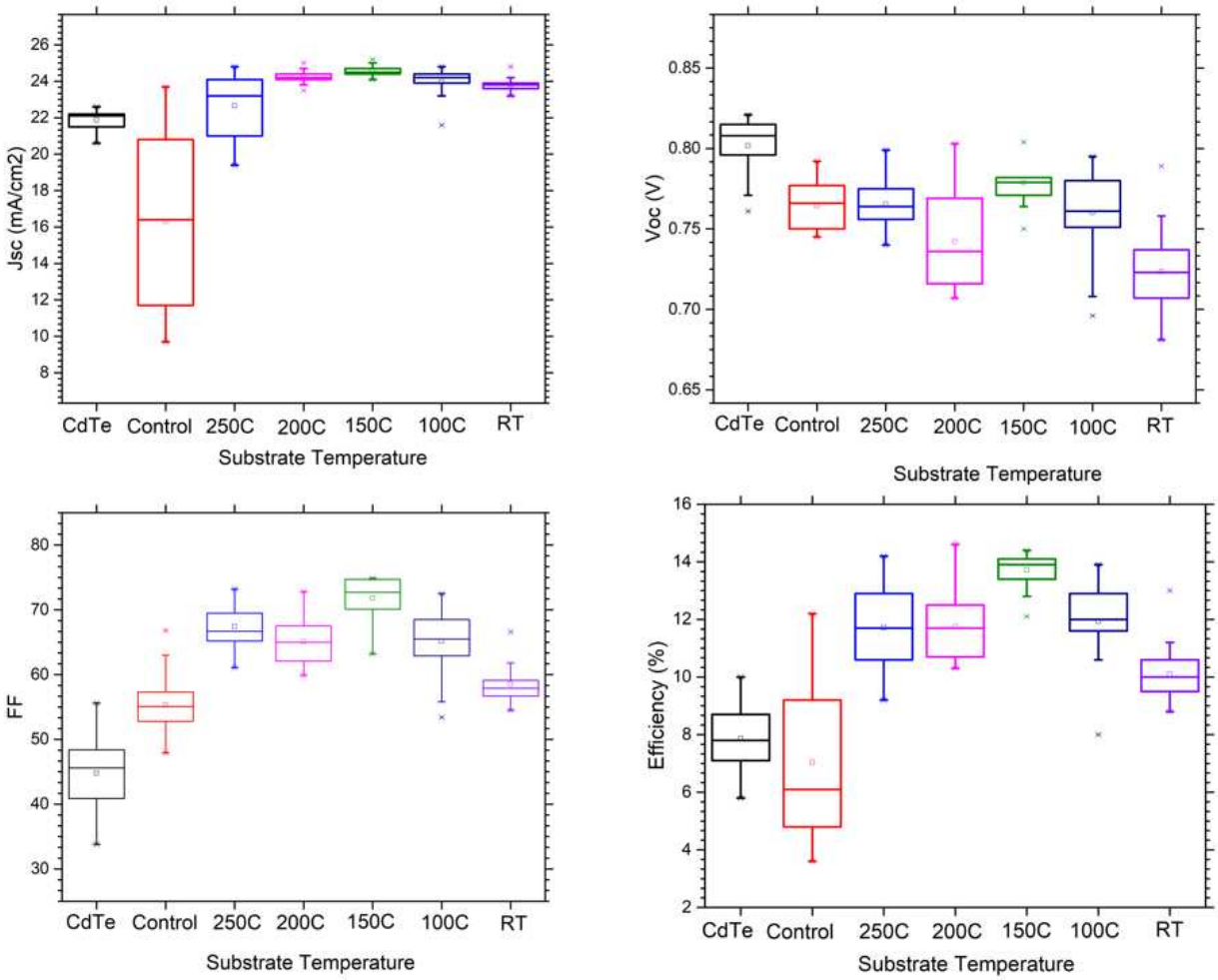


**Figure 4.14:** Current-voltage parameter box-plots for different substrate temperatures during the CdZnTe deposition. The CdTe referenced is a CdTe only device plate without any CdSeTe included.

an increase in PL signal, but not as dramatically as devices with depositions at elevated temperatures. The increase in PL signal did not follow the same trend as the average performance of the J-V curves, with 200°C seeing the largest increase in PL. This is likely due to the PL measurements having been performed on the best device from each plate where the 200°C plate had the highest performing single device, thus the PL signal for the 200°C device was the highest. This increase in PL for CZT plates at higher temperatures indicates reduced unfavorable recombination in the device.

Time-resolved photoluminescence measurements were taken by Daniel Shaw to determine any change in carrier lifetime when CZT is used. The quick initial decay in the baseline device

without CZT represents high recombination rates when carriers are first excited, this was then followed by minimal decaying which can be attributed to shallow defect states [87, 88] and electric-field separation of electrons and holes. The difference in decay rates between the room temperature deposition and the 150°C deposition was relatively small, and indicates lower lifetimes in the 150°C device, even though these were better performing cells.

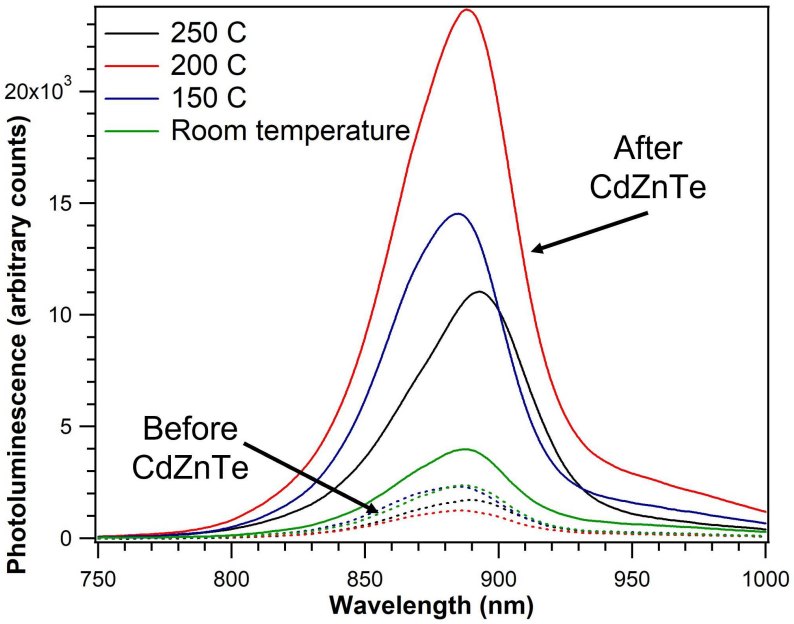


**Figure 4.15:** Photoluminescence measurement on devices with CdZnTe deposited at different substrate temperatures.

### 4.4.2 CdZnTe Film Characterization

To better understand the difference between CZT quality for different substrate temperatures, scanning electron microscopy (SEM) and X-ray diffraction (XRD) were done on CZT samples by Priya Suryavanshi. These samples were deposited on TEC10 glass and were 175-nm and 250-nm thick for the 150°C and room temperature samples respectively. There did not seem to be any notable difference in grain size between the two deposition temperatures, as shown in Fig. 4.17 a) and b). The grain sizes for both were relatively small, on the order of 100-nm, compared to CdTe device grain sizes with a First Solar example

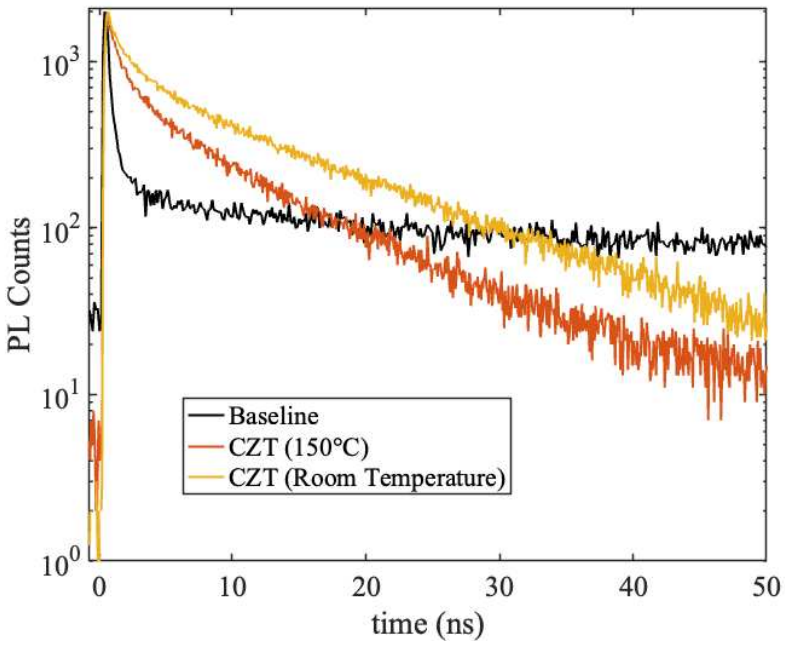


**Figure 4.16:** Time-resolved photoluminescence comparing room temperature and 150°C substrate temperatures during the CdZnTe deposition.

shown in Fig. 4.17 c) on the order of a few microns. The small grain sizes are likely due to the CZT not being $CdCl_2$ treated, which is known to increase the size of CdTe grains. The lack of difference between the temperature deposition grain sizes indicates the grain size is not the cause of the performance difference between the two.

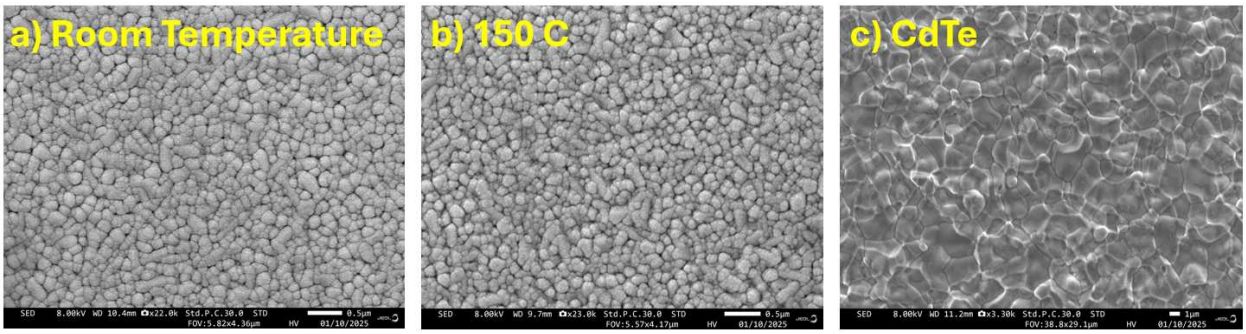


**Figure 4.17:** SEM images of CdZnTe deposited at a) room temperature and b) 150°C. c) First Solar deposited CdTe.

X-ray diffraction measurements were also done on these samples to investigate the crystallization of the CdZnTe layers. Measurements on the CdTe sample showed distinct peaks

representing crystal orientations, but the peaks were not present for the CdZnTe sample. This indicates that the grain sizes were so small, in the CdZnTe film, that the film was more amorphous than crystalline. This was the case for both substrate temperature materials. In order to create better grain formation higher deposition temperatures are likely required, due to the inability to $CdCl_2$ treat the material, but this can lead to diffusion problems of materials in the device. Incorporating higher temperatures into the CZT deposition will likely yield larger grains but come at the cost of disturbing prior optimized depositions and risk zinc diffusion.

An amorphous film generally leads to high resistances that limit carrier collection. These results indicate the need for a method that improves the crystal size in CdZnTe film. One method for this could be finding a way to passivate the material, similar to a $CdCl_2$ treatment, as is currently being researched at the University of Delaware. It is possible depositions on a CdTe surface will lead to better grain formation in the CdZnTe as there is already a crystal structure to follow instead of the amorphous structure of the TEC10 glass. Measurements of such depositions should be done to investigate this possibility.

### 4.4.3 CdZnTe on First Solar Absorbers

First Solar absorber devices were made with different combinations of back-contacts used in the CSU process. Figure 4.18 shows the resulting J-V curve performance for these devices. Due to the arsenic doping already present in the absorbers, no CuCl treatment was given to devices that only received Te and a back electrode. These devices showed much more rollover than devices that received CZT and a CuCl treatment. This indicated that the Te and back electrode did not form a good ohmic contact with the First Solar absorber, which led to an energy barrier at the back-contact. The device with CZT but no doping performed worse than all other devices, again illustrating the importance of doping in the back buffer layer. The blue curve in Fig. 4.18 represents the device that received the CuCl treatment that was optimized for the thin absorbers, 1000-s, while the red curve had half that anneal time during the CuCl treatment. The device with 500-s anneal time outperformed the "optimized" CuCl

treatment, but a device with only 250-s anneal time, not shown, performed worse. This implies that excessive annealing is bad for the First Solar absorber, but not enough leads to the CZT not creating a good back-contact.

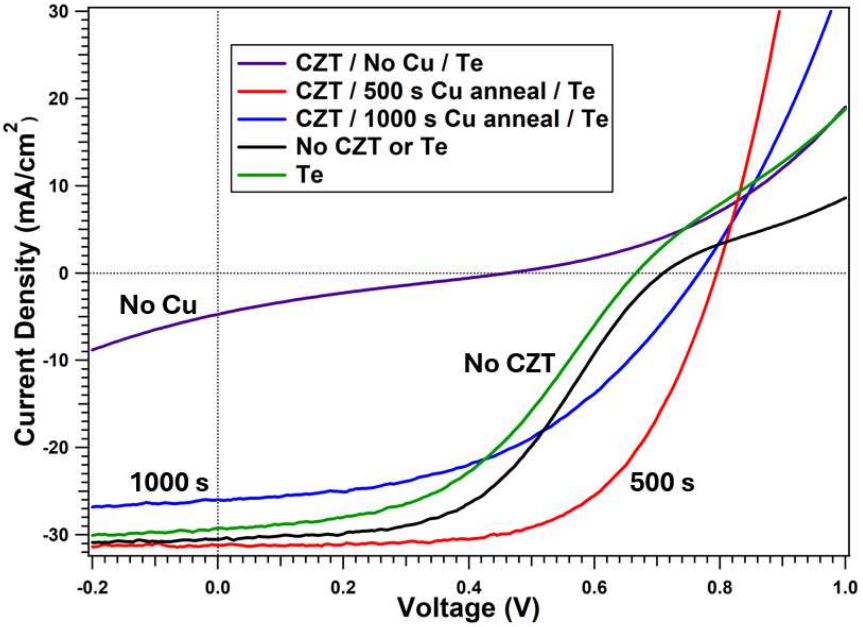


**Figure 4.18:** Current-voltage curves of CdZnTe devices deposited on First Solar absorbers.

The CuCl treatment is not likely to have reached the front of the absorber because the same treatment was given to thinner absorbers without that issue. The temperatures used in the CuCl treatment are too low to cause diffusion of the $CdCl_2$ passivating material. The likely culprit of the worse performance is diffusion of arsenic during the CuCl treatment. The arsenic doping in these absorbers has been optimized by First Solar, so when thermal annealing was done to diffuse the Cu into the CZT it is likely the arsenic diffused as well. This diffusion can lead to an increase of defect states and a decrease in carrier concentration. Capacitance measurements were done, results shown in Fig. 4.19, on this material to probe the affect on carrier concentration.

Devices that received a CuCl treatment actually decreased the carrier concentration, by an order of magnitude, for the longer anneal times, compared to the as-received First Solar absorbers. The CZT deposition was not the cause of this decrease because the device

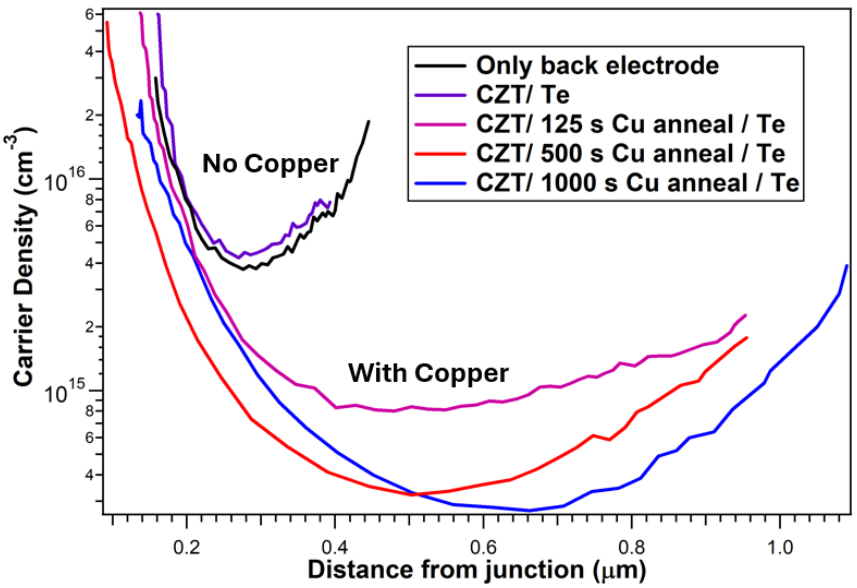


**Figure 4.19:** Carrier density curves of CdZnTe devices deposited on First Solar absorbers.

with CZT and Te had the same concentration as the device that just had a back electrode deposited on the First Solar absorber. The shortest anneal time affected the carrier concentration, but did not decrease it as much as the longer anneal times. This supports the idea that the CuCl treatment causes arsenic diffusion, harming device performance. In order to avoid this, either undoped absorbers are required, or a non-disruptive doping method needs to be found. One possibility is nitrogen doping during the CZT deposition by flowing nitrogen gas over the plasma. This was briefly attempted during this work, on thin absorber devices, and no doping activation was seen and the devices did not perform well.

Another possible solution is a cadmium arsenide ($Cd_3As_2$) anneal that has shown success doping CdTe at CSU [89]. A preliminary arsenic doping experiment was performed, where the temperature of the deposition process were changed. As the temperature of the bottom source increased the performance of the device increased, which indicated the doping had a positive effect. The overall performance of these devices was low, which indicates that higher temperatures are needed to determine if this doping method will produce good devices. The lowest temperature arsenic treatment had a J-V curve similar to that of undoped CZT devices shown previously, which suggested that the CZT layer was barely being doped. Capacitance

measurements were taken to see if the different $Cd_3As_2$ doping treatments affected the carrier concentration, but no notable differences in carrier concentration were found.

Full spectrum photoluminescence measurements showed a decrease in signal after the arsenic doping step. There was no notable difference in PL between the different doping temperatures. After the elemental Te was thermally evaporated a significant decrease in the subband-gap features was seen, similar to the Te effect seen on the $TeO_2$ samples in Fig. 4.10. This again brings attention to the effect the Te layer has on the PL signal and the need to determine the exact cause of this effect.

### 4.4.4 Temperature-Dependent Current-Voltage on CdZnTe

Temperature-dependent current-voltage measurements were done on devices with CdZnTe deposited, with results shown in Fig. 4.20. These measurements, done on devices using both CSU and First Solar absorbers, showed no roll-over effect at low temperatures down to 233K, but did show the formation of a kink in the curve at lower temperatures. A kink is said to form when the J-V curve starts to flatten out in forward bias, but rights itself as it resumes a steep increase in forward bias giving a S-shape to the curve whereas roll-over occurs when the curve flattens out and does not right itself. The kink set in slightly faster with reduced temperature in the CSU cell compared to the First Solar. Kink formation generally indicates and issue at the front contact, or in the absorber. The kink formation, rather than roll-over, indicated the back-contact was not the main cause of barrier formation in the devices. The inclusion of CdZnTe did not introduce roll-over at low temperatures for either absorber, indicating this layer does not introduce an energy barrier for hole extraction.

## 4.5 Summary and Next Steps

In this chapter the issues facing the back-contact of CdTe solar cells were discussed. The deep valence band of CdTe makes it difficult to form ohmic contact with a back electrode.

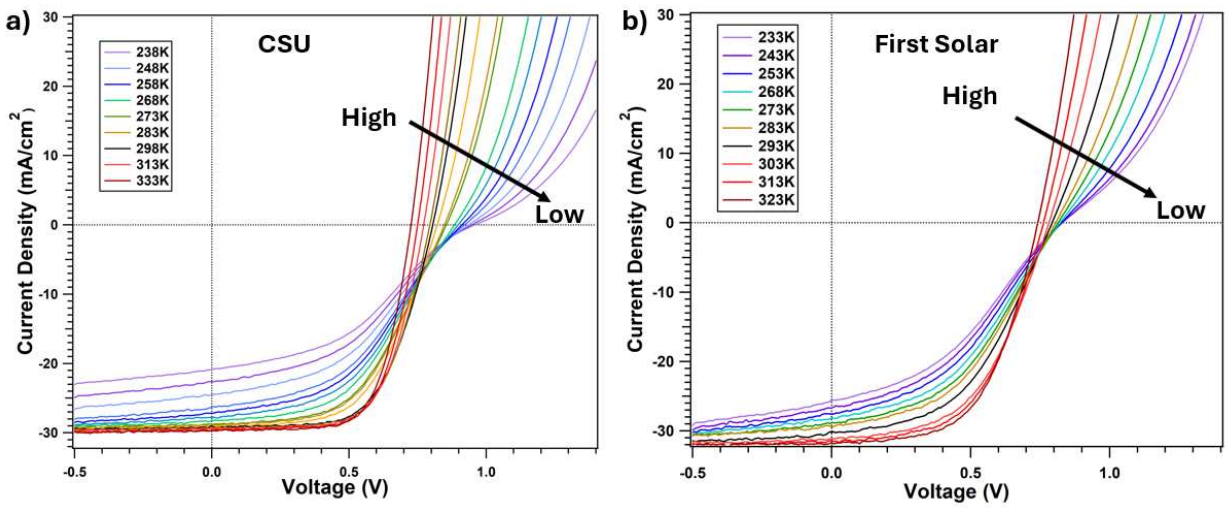


**Figure 4.20:** Temperature-dependent current-voltage curves for CdZnTe devices using absorbers from (a) CSU (b) First Solar.

Dangling bonds at the CdTe surface also present a problem, causing non-radiative recombination at the back interface. In order to better research these problems a thin absorber was optimized to allow carrier generation to occur closer to the back-contact, leading to more carriers being present at the interface. Once issues with the thin absorber occurred, more consistent absorbers from the company First Solar were used to learn about the back interface.

The use of added $TeO_2$ as a thin passivating layer was discussed. In order to get good performance from a device with $TeO_2$, a second passivation treatment is required. If some passivation treatment is not done following the $TeO_2$ layer, then little or no PCE will occur. If the treatment is done only after the $TeO_2$ layer then the device performance and substrate uniformity will be worse than when two passivation treatments are used. The use of copper-doping in devices with $TeO_2$ led to barrier formation at the back-contact resulting in reduced performance and substrate uniformity. When depositing $TeO_2$ on an arsenic doped absorber from First Solar the photoluminescence showed an increase in continuous defect states, likely due to surface damage from the energetic sputtering deposition. When elemental tellurium is thermally evaporated onto the tellurium oxide layer these defect states are mitigated as seen in photoluminescence. This suggests that an electric field forms at the interface and

causes the defect states to be less impactful. The effect that elemental tellurium has on the photoluminescence deserves further study in future works. Due to the negative impact the $TeO_2$ deposition process had on photoluminescence it is important to explore less energetic deposition methods such as rapid oxidation going forward.

Cadmium zinc telluride was tested as an electron-reflecting layer and showed some initial success. CdZnTe PCE was routinely above the control device and photoluminescence showed a large increase after the CdZnTe deposition. Film characterization showed small grain formation which can lead to large resistances if the layer is not properly doped. Ensuring the CdZnTe layer is conductive is essential to creating a good contact. Utilizing CdZnTe on First Solar absorbers proved more difficult than expected due to the high temperatures required to dope the CdZnTe layer. These processes negatively affected the already optimized CdTe layer leading to limited success. Other doping methods were investigated with some promise and should be probed more extensively in future works.

Maintaining a consistent absorber quality is crucial for back-contact work going forward. Better monitoring and tracking of the deposition processes and parameters will help maintain consistent absorbers for back-contact work. One example for this is the impact of native $TeO_2$ formation. Tracking the time between absorber and back-contact deposition is method to gain a better understanding of how native $TeO_2$ effects the interface with the back-contact layer.

Photoluminescence measurements should be more heavily utilized in future back-contact work. The impact of and elemental tellurium layer is clearly seen in photoluminescence measurements, demonstrating the usefulness of the measurement. The aim of back-contact research is to reduce recombination and promote hole extraction so using photoluminescence is essential moving forward.

# Chapter 5

CONCLUSIONS

Cadmium telluride solar cells have made significant advances in recent years, increasing the record device to 23.1% efficiency. These advances can be attributed to the incorporation of oxide buffer layers at the front contact, the improvement of the absorber by including a graded CdSeTe alloy layer, and improving doping methods at the back. Even with these advances, CdTe has only achieved 71% of its maximum possible efficiency under standard test conditions, with a plurality of the losses coming from the $V_{oc}$ only reaching 81% of its maximum. Understanding the losses in photovoltaic devices, and their causes, is essential to improving performance.

In this work, device efficiencies for both single and multi-junction devices, were compared to the theoretical limit, the Shockley-Queisser (SQ) limit, to better compare performance. The limit for different current-voltage parameters depends on the band-gap of the absorber material, so to better compare devices from different technologies these parameters were normalized to their SQ limit. These record single-junction cells showed minimal difference in the normalized $J_{sc}$ values with most technologies utilizing close to 95% of their respective limit. The $V_{oc}$ of gallium arsenide is closest to ideal performance utilizing 99% of its limit, while CdTe is notably lower at 81% the SQ limit. The normalized fill-factor showed that all record devices utilize over 90% of their theoretical maximum.

Even though multi-junction tandem devices with at least one thin-film cell have a higher power conversion efficiency compared to single-junction cells, the normalized efficiency is lower, with the best tandem investigated being the perovskite/Si device that reached 73% normalized efficiency. The perovskite and Si single-junction devices both have a normalized efficiency over 80%, showing that even though total efficiencies are higher, multi-junction devices with thin-film cells still have significant room for improvement.

The fill-factor losses were further analyzed by calculating individual parasitic parameters. The losses in fill-factor were quantified by separating the total fill-factor loss into contributions from different parasitic parameters, the shunt conductance, series resistance, diode quality factor, and the voltage deficit. This quantification revealed a major difference between the single-crystal (silicon and gallium arsenide) and poly-crystalline(CdTe, CIGS and perovskites) technologies. The single crystal devices have near perfect fill-factor, while the poly-crystalline devices have a notably lower fill-factor attributed, for the most part, to a higher diode quality factor. This demonstrates that unfavorable recombination along grain boundaries has a negative impact not only on $V_{oc}$ but also on fill-factor. Performing detailed diode and fill-factor analysis on multi-junction devices requires significant modification to the analysis procedure used in this work, and is not included in this thesis.

Similar analysis done on CdTe devices from different leading laboratories showed that the diode quality factor is the main contributor to fill-factor loss throughout the CdTe community. Comparing the fill-factor loss of record CdTe devices from First Solar over time showed which diode parameters were improved. This demonstrates the importance detailed loss analysis has to better understand how the community is improving cells and what areas of research should lead to the most improvement going forward.

This work also focused on improving CdTe performance by introducing back buffer layers to the device structure. Tellurium dioxide was used as a passivating back layer to improve $V_{oc}$ by reducing interface recombination. It was shown to be an effective back layer without the need for intentional copper doping, reaching an undoped efficiency of 17.5%. Temperature-dependent current-voltage measurements showed the presence of an energy barrier to hole extraction when copper-doping was included in the device structure. A second $CdCl_2$ passivation treatment after the tellurium dioxide layer was found to be necessary, and showed an order of magnitude increase in carrier concentration when the second passivation treatment was performed. Photoluminescence measurements showed that the impact of the second $CdCl_2$ process conditions, particularly the temperature, must be taken into account when fabricating devices with tellurium dioxide. Full spectrum photoluminescence measurements

showed the impact sputtering depositions can have on increased sub band-gap defect states at the interface, which is opposite of the $TeO_2$ purpose. High temperatures during these processes cause dopants in the absorber to diffuse and impact non-radiative recombination.

Cadmium zinc telluride was used as an electron-reflection layer to reduce the recombination at the back surface. CdZnTe was incorporated into the device structure by RF sputtering and an increase in device performance was seen when the substrate was held at 150°C during the CdZnTe deposition. Photoluminescence measurements indicated reduced unfavorable recombination after the CdZnTe was deposited. SEM and XRD measurements showed small grain formation and a lack of crystallinity in the CdZnTe layer, likely due to the lack of passivation. This exemplified the need for proper doping of the CdZnTe to improve conductivity and extract carriers.

Copper doping experiments showed that an extended treatment was required to diffuse through the CdZnTe layer and dope both the CdTe and CdZnTe. Devices with CdZnTe showed results, outperforming the control device without CdZnTe by over 3% PCE, but the target $V_{oc}$ parameter did not see improvement. Doping treatments with both copper and arsenic performed on CdZnTe layers deposited on First Solar absorbers, that had been previously doped by the company, showed a decrease in performance and a decrease in carrier concentration. This again demonstrates the negative impact that processes, particularly at high temperatures, can have on an absorber that already contains dopants.

Photoluminescence measurements on $TeO_2$ devices, shown in Fig. 4.10, show a notable decrease in sub band-gap features after the thermal evaporation of elemental Te. This is likely due to the added Te layer, which has high carrier concentration at ∼1E18, impacting the electric field at the back surface and causing the defect states to be less impactful. This effect deserves further study in future works to better understand the fundamental effects leading to the decrease in unfavorable recombination.

Future work on back-contact layers requires a focus on improving the doping in the buffer layers without disturbing the absorber. Non-additive methods of surface passivation, such as chemical depositions or rapid oxidation methods, should be explored to reduce the

impacts of energetic deposition techniques, and investigation of the photoluminescence of devices utilizing back-contact layers is essential to understanding the difference in fabrication strategies.

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