THESIS

DESIGN OF INTEGRATED ON-CHIP IMPEDANCE SENSORS

Submitted by

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ABSTRACT

DESIGN OF INTEGRATED ON-CHIP IMPEDANCE SENSORS

In this thesis two integrated sensor systems for measuring the impedance of a device under test (DUT) are presented. Both sensors have potential applications in label-free affinity biosensors for biological and bio-medical analysis. The first sensor is a purely capacitive sensor that operates on the theory of capacitive division. Test capacitance is placed within a capacitive divider and produces an output voltage proportional to its value. This voltage is then converted to a time-domain signal for easy readout. The prototype capacitive sensor shows a resolution of 5 fF on a base of 500 fF, which corresponds to a 1 % resolution. The second sensor, a general purpose impedance sensor calculates the ratio between a DUT and reference impedance when stimulated by a sinusoidal signal. Computation of DUT magnitude and phase is accomplished in silicon via mixed-signal division and a phase module. An automatic gain controller (AGC) allows the sensor to measure impedance from 30 Ω to 2.5 MΩ with no more than 10 % error and a resolution of at least .44 %.

Prototypes of both sensing topologies were implemented in a .18 µm CMOS process and their operation in silicon was verified. The prototype capacitive sensor required a circuit area of .014 mm^2 and successfully demonstrated a resolution of 5 fF in silicon. A prototype impedance sensor without the phase module or AGC was implemented with a circuit area of .17 mm^2. Functional verification of the peak capture systems and mixed-signal divider was accomplished. The complete implementation of the impedance sensor, with phase module and AGC, requires an estimated .28 mm^2 of circuit area.

ACKNOWLEDGEMENTS

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This thesis is typset in LaTeX using a document class designed by Leif Anderson.

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Introduction

1.1. Impedance

Impedance is the total opposition to the flow of alternating current through a device, circuit or material at a given frequency [1]. Impedance (Z) extends the concept of resistance to AC circuits to account for frequency dependent properties of reactive elements and is measured in units of Ohms (Ω). Impedance is represented as a complex ratio between voltage and current, therefore can be represented either as rectangular coordinates on the complex plane or as a magnitude and phase in polar format.

When represented in rectangular coordinates impedance takes the form of $Z = R + jX$ where the real part, R, is the resistive component and the imaginary part, X, is the reactive component of the impedance. When represented in polar form, $Z = |Z|\angle\theta$, the magnitude, $|Z|$, describes the ratio of voltage amplitude to current amplitude and the phase, θ, describes the phase shift between the voltage and current when subject to sinusoidal inputs. Conversion between rectangular and polar coordinates can be achieved via the following equations.

$$|Z| = \sqrt{R^2 + X^2} \qquad \theta = \tan^{-1}(\frac{X}{R}) \tag{1.1}$$

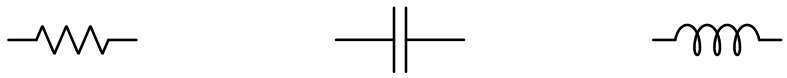
$$R = |Z|\cos(\theta) \qquad X = |Z|\sin(\theta)$$

The reciprocal of impedance, admittance (Y), measured in units of Siemens (S) can also be used to describe the AC properties of a circuit, device or material. In rectangular coordinates admittance is represented as $Y = G + jB$ where the G is the conductance and B is the susceptance.

Admittance is often used for parallel circuits where the expression for impedance is significantly more complex.

1.1.1. Passive Devices

The three fundamental passive circuit components are the resistor, capacitor and inductor. The schematic symbols for each are show in Figure 1.1. Each can be described in terms of its



(A) Resistor (B) Capacitor (C) Inductor

FIGURE 1.1. Passive Device Schematic Symbols

ideal impedance, how its impedance changes with respect to frequency, and how it alters the phase of a signal.

An ideal resistor has a purely real impedance given by $Z_R = R$, no frequency dependence and no phase shift. An ideal capacitor has a purely reactive (imaginary) impedance given by $Z_C(j\omega) = \frac{1}{j\omega C}$, which approaches infinity at DC and zero at high frequencies. The capacitor introduces a phase shift causing the current through the capacitor to lead the voltage by 90°. An ideal inductor also has a purely reactive impedance given by $Z_L(j\omega) = j\omega L$, which approaches zero at DC and infinity at high frequencies. Like a capacitor, an inductor introduces a 90 phase shift between voltage and current, except that the voltage in an inductor leads the current.

Ideal devices only exist in the realm of simulation and mathematics. Real devices have additional impedance characteristics due to the presence of unavoidable parasitic devices. A parasitic device is a undesirable resistance, capacitance, or inductance that appears due to nonideal materials and manufacturing. Real resistors, especially those of the wirewound type, have inductive properties. Real capacitors have a large parallel resistance due to imperfect dielectrics which results in leakage currents. Real inductors have a series resistance due to the resistivity of the

conductor, and a parallel capacitance between the windings. Fortunately these parasitics can often be ignored except for in the most detailed analysis or at high frequencies where the components may begin to resonate.

1.2. Resistive, Capacitive & Impedance Sensor

An impedance sensor is a device designed to measure and characterize an unknown impedance between two terminals. Resistive and capacitive sensors are simplified derivatives of impedance sensors used for measuring specific types of impedance. The simplest general purpose impedance sensor must be capable of measuring both the magnitude and phase of the test impedance at a frequency. Both magnitude and phase information is required to determine if the unknown impedance is capacitive, inductive, or resistive in nature. A typical, more complex, impedance sensor should measure the magnitude and phase of the test impedance over a range of frequencies. Advanced features for an impedance sensor may include adjustable bias and excitation values, automatic frequency sweeps, resistive and reactive value calculation, Q value calculation, and admittance calculation.

Impedance sensors can be used in laboratory environments for the characterization of passive and active devices [1], interconnects [2], circuit traces and filters. Impedance sensors and their derivatives also find use in environmental sensing in conjunction with specific transducers e.g. strain gauges [3], pressure sensors [4] and resistance thermometers for temperature. Capacitive sensing also finds application in Microelectromechanical (MEMS) devices, particularly in accelerometers and gyroscopes [5]. Impedance sensors have also been gaining ground in their application toward the biological and biomedical fields as electrochemical biosensors [6].

1.3. Electrochemical Biosensors

A biosensor is a device that detects the presence or concentration of an analyte, a substance or chemical of interest. Biosensors can be designed that exploit physical, electrical or optical properties of the analyte to perform detection. An electrochemical biosensor, as its name implies, exploits the electrical properties of the analytes to perform detection and characterization [7]. Although many biosensor eventually rely on electrical signals for processing and readout, electrochemical biosensor are considered unique as they directly convert the analyte concentration to an electrical signal. Electrochemcial biosensors show great promise in the miniaturization of these devices for their use in implantable sensing or point-of-care applications.

An electrochemical biosensor can be categorized by its detection mechanism: amperometric, potentiometric, and impedance. Amperometric sensors detect and measure currents produced by electron acquisition or release in solution due to reduction-oxidation reactions at the electrode surface. Potentiometric sensors operate by measuring the voltage between two electrode that arises due to the collection of charge on the electrodes. Amperometric sensors are widely used in amperometry and cyclic voltammetry experiments to detect the presence and concentration of analytes in solution. A key weakness of amperometric sensors is its dependence on the redox reaction. Analytes which do not reduce or oxidize, or do so at unreasonable potentials cannot be detected with amperometric sensors. An impedance biosensor can be used to detect and measure analytes that are otherwise not electrochemically active, by sensing a change in impedance at the electrode surface, or within the solution.

1.3.1. Affinity Impedance Biosensors

A key advantage of impedance biosensors is their ability to provide label-free detection. Many biosensors rely on the use of labeling to perform detection. In such sensors a label is attached

to the analyte by some means and the label itself is detected. The concentration of the label is then assumed to be related to the concentration of the analyte. Labeling increases time and cost associated with preparing a sample for analysis, additionally labeling prevents the sensor from being used in real-time applications. [8]

Instead impedance sensors can be used to perform label-free sensing. Label-free sensing is accomplished by modifying the sensor electrodes with a probe that the analyte has an affinity toward. Binding between the analyte and probe on the electrode surface causes a measurable change in impedance. Figure 1.2 depicts this concept. Possible applications of label-free sensing include DNA and protein detection for population genotyping [9] and cancer predisposition [10], small molecule sensors, cellular detection and lipid bilayer sensors [8].

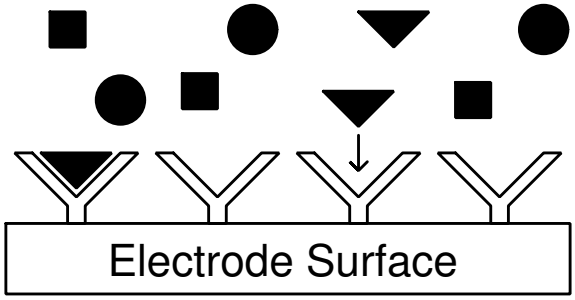
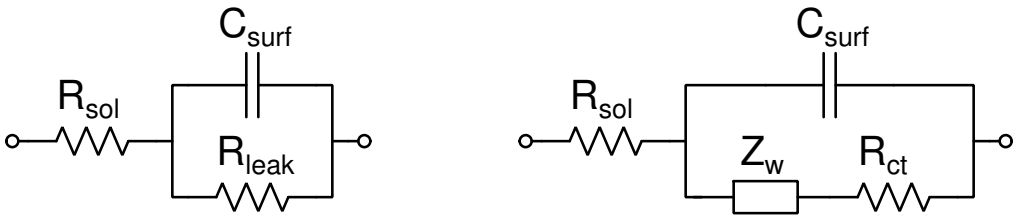


FIGURE 1.2. Analyte Binding at the Electrode Surface

Affinity impedance biosensor detect the analyte in a two step procedure. First, the affinity step, binding of targets to probes on the electrode interface. Second, the readout step, a change in electrode impedance is measured. An important parameter is the selectivity of the sensor, that is its ability to respond only to the analyte. An impedance sensor on its own cannot distinguish binding of the analyte from binding of other molecules, thus the selectivity of the entire sensor is set by the selectivity of the probe. [8]

An impedance biosensor is classified as either a faradaic or non-faradaic sensor depending on the charge transfer characteristics. A faradaic sensor has a physical transfer of charge across the

electrode interface. A non-faradaic sensor has no physical charge transfer across the interface, but is subject to transient currents due to capacitive charging. Capacitive sensors are inherently non-faradaic sensors. [8]



(A) Non-faradaic (B) Faradaic

FIGURE 1.3. Electrode Interface Circuit Models

Circuit models of faradiac and non-faradaic electrode interfaces are shown in Figure 1.3. C_{surf} is a combination of the double layer capacitance and any modification to the electrode surface. R_{sol} arises from the limited conductance of the solution. In non-faradaic sensors, R_{leak} comes from the leakage of the surface dielectric. In faradaic sensors, R_{ct} comes from the redox reaction of species in solution and Z_w, the Walburg impedance, is from the diffusion of species to the electrode surface. C_{surf} is typically the main indicator of detection is non-faradaic sensors. For faradaic sensors, R_{ct} is the most common indicator of binding. [8]

Chapter 2
Impedance Measurement Methods

2.1. Fundamental Concept

The basis of any impedance measurement is applying a known excitation signal to the Device Under Test (DUT) and measuring the corresponding output signal. An example of this is shown in Figure 2.1. Traditionally an sine wave excitation is used to account for reactive elements within the DUT, although a DC signal can be used if the device is resistive in nature and the only property of interest. For voltage excitation, the resultant magnitude and phase of the current through the DUT is measured and the unknown impedance can be solved for via Ohm's Law: $Z = \frac{V}{I}$.

The magnitude of the excitation signal is usually kept small, < 10 mV, to prevent non-linearity from appearing in the measurement. Although methods utilizing non-linearity as the property of interest have been reported for biosensing applications [11]. Additionally a DC bias signal can be applied to the excitation signal to analyze the effects of bias on the DUT. The use of bias is common in semiconductor characterization.

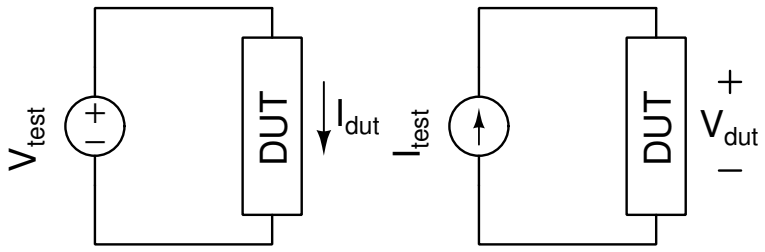


FIGURE 2.1. Excitation Sources and Corresponding Output Signals.

2.2. Measurement Methods

The Agilent Impedance Measurement Handbook lists the following as common methods of performing impedance measurements [1]. Each has specific advantages and disadvantages that make them more suitable for specific applications.

- Bridge method
- Resonant method
- I-V Method & RF I-V method
- Network analysis method
- Auto-balancing bridge method

The bridge and resonant methods require manual tuning which makes them infeasible for integrated applications. The RF I-V and network analysis methods are intended for high frequency applications ($>$ 100 kHz) which is unnecessary for the intended applications of this sensor. Finally the I-V methods requires either the use of a low value resistor in series with the DUT or a low loss transformer. Both of which are difficult to fabricate in silicon.

The auto-balancing bridge, shown in Figure 2.2, on the other hand is an great candidate for integration. Comprised of only an op-amp and a feedback impedance the auto-balancing bridge has reasonable accuracy for LF measurements ($<$ 100 kHz) [1] and can be easily fabricated in silicon. Current through the DUT and feedback impedance is "balanced" by means of the op-amp. The op-amp provides a virtual ground which eliminates the impact of many parasitics in the DUT connection. The virtual ground also ensure that only the excitation voltage is presented across the DUT. The DUT impedance is given by the following equation:

$$Z_{DUT} = -\frac{V_{excite}}{V_{out}} Z_f \tag{2.1}$$

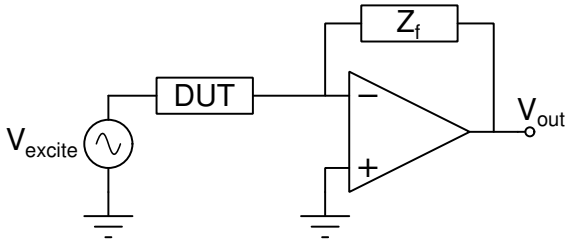


FIGURE 2.2. Auto-balancing Bridge Method

The auto-balancing bridge is simple and effective but accuracy of the measurement is dependent on known values of V_{excite} and Z_f. In silicon, the value of Z_f may not be well known, and can vary greatly across process corners. V_{excite} could also potentially vary if generated on-chip.

To overcome these limitations, a system utilizing two auto-balancing bridges was proposed in [11]. This dual-bridge technique, shown in Figure 2.3, measures impedance by comparing the DUT bridge output to the output of a reference bridge. The reference bridge exists to measure the excitation voltage in a manner that is consistent with the DUT measurement.

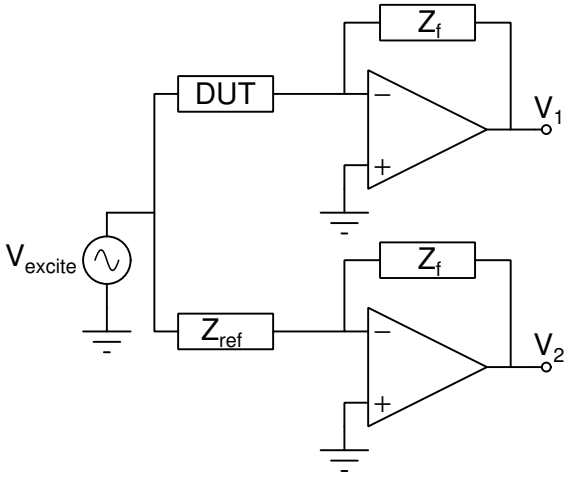


FIGURE 2.3. Dual Auto-balancing Bridge Approach

Applying the auto-balancing bridge equation to each bridge and solving for V_{excite} gives

$$V_{excite} = -\frac{Z_{DUT}}{Z_f} V_1 \qquad (2.2)$$
$$V_{excite} = -\frac{Z_{ref}}{Z_f} V_2$$

which when equated and solved for Z_{DUT} gives

$$Z_{DUT} = \eta \frac{V_2}{V_1} Z_{ref} \qquad (2.3)$$

where η is the coefficient of matching between the two feedback impedances, where $\eta = 1$ being a perfect match.

Using The dual-bridge method the exact value of the feedback impedance is irrelevant, only the degree of matching between the two stages matters. With careful layout a high degree of element matching in silicon is possible. Additionally the measurement is no longer dependent on the value of V_{excite}. However the dual-bridge method still does rely on the accuracy of Z_{ref}, which can made external or compensated for by calibrating the system after fabrication.

The above methods are simply tools for converting an impedance into a signal that is easier to handle and process. To acquire magnitude and phase information for the DUT additional processing is typically performed. For most of the measurement methods, the phase of the DUT impedance is obtained from the phase difference between the input and output signals, assuming no additional shift is introduced by the measurement system itself.

Chapter 3
Existing Impedance Sensors

Capacitive and impedance sensing are not new fields of study. Numerous laboratory instruments exist for the analysis of impedance in electronic and biological applications. There been significant work in the field of integrated sensors for numerous application and significant commercial deployment of capacitive sensing for MEMS applications. A review of some integrated sensing approaches for biological applications is presented in this section. All the systems discussed here are intended for label-free detection and characterization.

3.1. Integrated Capacitive DNA Sensor Array

In 2006, a team of Italian researchers designed and fabricated a label-free DNA microarray based on capacitive measurement of interdigitated gold electrodes. The same team published at least two additional works detailing the experimental characterization of the microarray capacitors for label-free DNA sensing [12], and the design and fabrication of a partially integrated sensor array with external read-out circuits [13]. The sensor consisted of an 8 x 16 array of interdigitated electrodes and integrated capacitive measurement system.

Sensor measurement was achieved by performing a capacitive to frequency conversion and each sensor was measured in parallel. Conversion to frequency was accomplished by a current source and a comparator. The current source either charged or discharged the sensor capacitor depending on the current state of the comparator. The comparator determined when the voltage across the capacitor reached a user defined reference value and reversed the direction of the current source.

This structure, shown in Figure 3.1, creates an oscillator whose frequency is dependent on the time constant of the sensor circuit. As the sensor capacitance changes, the time constant changes and the frequency of oscillation is changed. Frequency values were then converted to a digital word by counting the number of edges within a fixed time interval. Each sensor could be individually addressed and the frequency value read out to a computer via a serial interface.

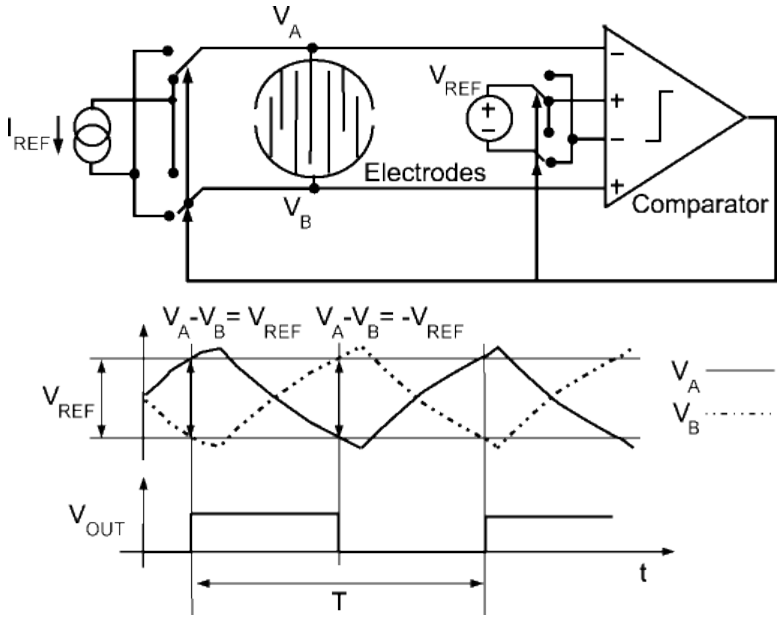


FIGURE 3.1. Capacitance to Frequency Conversion [14]

The system was fabricated in a .5 µm, three metal process with a 5 V supply. Sensor sites were constructed from interdigitated gold electrodes that were deposited after standard CMOS fabrication. The electrodes were fabricated with a line width and spacing of 1.2 µm. The circular sensor sites had a diameter of 200 µm and a pitch of 250 µm. Die dimensions were 6.4 mm x 4.5 mm and no power numbers were reported. The chip was mounted on a PCB which contained voltage reference circuits for the measurement system and an interface to a National Instruments data acquisition card. A LabView VI handled sensor addressing, frequency reading and capacitance calculation.

The sensor was tested with accurate external capacitors (1 % error) in the range of 330 pF to 10 nF to verify its linearity. Sensor linearity was shown to be good except for test circuits involving high leakage currents ($R_{leak} < 700$ kΩ) and smaller charge/discharge currents (< 1 µA). When tested for DNA detection the system demonstrated an ability to distinguish between specific and a-specific binding. Specific binding resulted in a change of 3.5 nF $\pm$ .5 nF to the sensor capacitance. A-specific binding only resulted in a .25 nF $\pm$ .5 nF compared to the non-bound functionalized electrodes. The base capacitor values were not reported. [14]

A key limitation of this sensing system was its ability to only perform characterization of capacitive or non-faradaic sensors. Reported data indicated that the sensor linearity degraded if a conductive (< 700 kΩ) path between the electrodes existed prohibiting its application to faradaic sensors. The system also required external biasing, data acquisition and computation to achieve the final results. Although integration of some or all of these features would be feasible.

3.2. Stanford Integrated Impedance Sensor Array

Published in 2010, this dissertation from Stanford detailed a comprehensive impedance biosensor array system. Two systems were presented in the work, a prototype PCB system and an integrated CMOS system. A key component of the research was the application of DUT non-linearity as a detection variable. Both systems utilized a 6 x 6 microelectrode array fabricated on a quartz substrate. The electrodes were 300 µm x 300 µm with a pitch of 600 µm. A custom socket was developed and manufactured for interconnecting the electrode array to the PCB and CMOS measurement systems. Excitation was achieved by a external Ag/AgCl electrode placed in solution above the array.

The PCB measurement system was composed of an excitation amplifier, a measurement channel, a reference channel and an analog multiplexer. The measurement and reference channels consist of a transimpedance amplifier (TIA), signal amplifier and anti-aliasing filters. The measurement channel connects to the electrode array via the analog multiplexer. The reference channel measured the excitation voltage via a reference impedance.

This system is the origin of the dual-bridge measurement technique discussed in Chapter 2, although it is not refereed to as such in the work. Generation of the excitation signals, multiplexer control, signal acquisition and computation is achieve by a LabView virtual instrument and a National Instruments data acquisition card. Figure 3.2 shows the schematic diagram of the PCB measurement system.

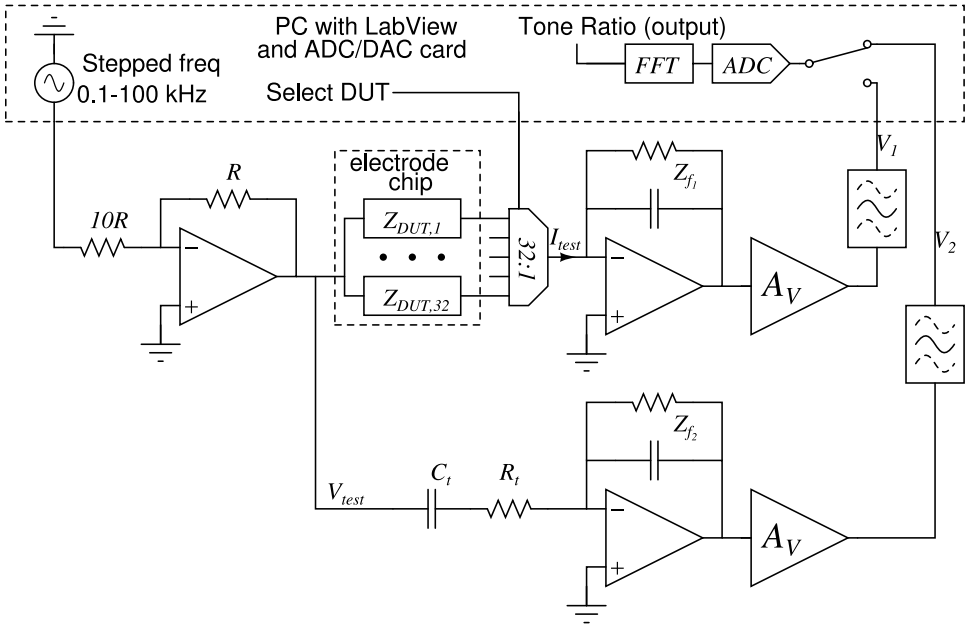


FIGURE 3.2. PCB Measurement System [11]

Impedance measurement of an electrode was accomplished by computation of the FFT for the measurement and reference channel. The FFT magnitude and phase values were then used to compute the complex ratio between the reference and measurement channels. This process was repeated at multiple frequency points defined by the user in the LabView VI to create an

impedance spectra. Up to 32 electrodes could be automatically be measured through the use of the digital outputs of the data acquisition card and the analog multiplexer. The collected data was calibrated against known DUT values and fitted to expected circuit models for analysis. The PCB achieved a reproducible precision of approximately .1 %.

The CMOS implementation of the sensor system consisted of a transimpedance amplifier (TIA) and tone cancellation circuit for each of the 36 electrodes. The external electrode array was still utilized although it was the author's opinion that consolidating the two would straightforward. Multiplexing, excitation, acquisition and computation were still accomplished by the LabView VI.

A tone cancellation circuit was built for each electrode to cancel a large tone at the input of the TIA that would saturate the output. The large tone originated from a two-tone non-linearity test method. The tone cancellation operated by injecting current into the TIA in opposite phase of the large tone. The nulling current was generated from quadrature waveforms through resistor-string DACs controlled by a digital feedback system.

The CMOS system was implemented in a .18 µm process operated at an analog supply of 3.3 V and a digital supply of 1.8 V. Each pixel required an area of 380 µm x 370 µm and consumed 1.9 mW of power. The total die area was not reported but was limited by the CMOS fab to no more than 3 mm x 3 mm. The system demonstrated a reproducible precision of .2 % for a capacitive DUT.

Both system implementations operate as a non-faradaic sensor with the electrode-solution interface modeled as shown in Figure 3.3. Table 3.1 summarizes the expected impedance values determined experimentally via the PCB measurement system. Both system used an excitation magnitude in the range of 1-10 mV with frequencies ranging from 100 Hz to 100 kHz. [11]

The system excelled as a general purpose impedance sensor and implemented a unique detection mechanism based on electrode non-linearity. The system was significantly dependent on

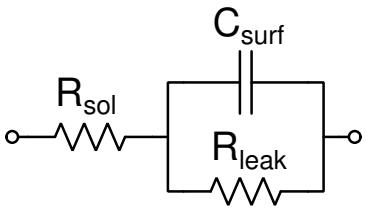


FIGURE 3.3. Non-faradaic Sensor Model

TABLE 3.1. Expected Impedance Values [11]

Parameter	Min. Z_{DUT}	Typ. Z_{DUT}	Max. Z_{DUT}
C_{surf}	30 nF	15 nF	7.5 nF
R_{sol}	700 Ω	1 kΩ	1.5 kΩ
R_{leak}	25 MΩ	50 MΩ	1 GΩ

external equipment for excitation generation, control signals, data acquisition and data computation. Depending on the desired application of the system these dependencies could significantly limit the architecture's utility. As described the sensor architecture is also a poor candidate for integration as the Fast Fourier Transform requires significant computation.

3.3. Integrated Impedance Spectroscopy Biosensors

Published in 2012, this dissertation details the requirements and design of a CMOS integrated circuit specifically for electronic impedance spectroscopy. The system performed frequency response analysis (FRA) which, unlike FFT-based methods, excites the solution with a single frequency at a time. The sensor system contained a 10 x 10 array of electrodes with a large shared electrode in solution to provide the excitation signal. Sensor electrodes were approximately 40 μm

x 40 μm with a pitch of 50 μm between the electrodes. Post processing was utilized to fabricate gold electrodes in passivization openings on the chip surface.

The system measured the electrode-solution interface admittance through a direct conversion or coherent detection method. The electrode current is converted and amplified by a low-noise TIA and then mixed with quadrature signals, I & Q, of same frequency as the excitation signal. After filtering, V_I & V_Q (DC signals) are used to estimate the admittance magnitude and phase. The I and Q signals were generated from an external clock through on-chip circuits. The excitation signal is also drawn from the I signal which ensured all three signals remain phase-locked. A schematic of the system is shown in Figure 3.4.

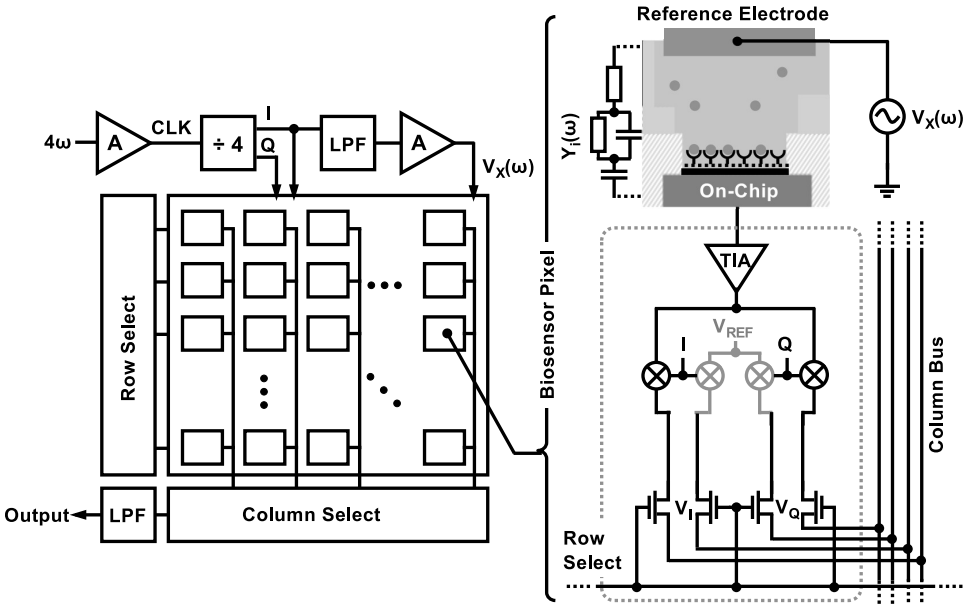


FIGURE 3.4. Sensor Array Architecture [15]

Supporting electronics for each electrode were approximately 100 μm x 100 μm. Electrode measurement occurred in parallel but sensor readout was accomplished individually through row and column decoders. An external multiplexer, preamplifier and data acquisition card was used to measure the values of V_I & V_Q. The system had a supported frequency range of 10 Hz to 50 MHz.

The system was implemented in a .35 µm, four metal process, with a supply of 3.3 V. Total die dimensions were 2 mm x 2 mm with the array consuming only 1 mm x 1 mm of the die. Total power was reported as 84.8 mW at 100 kHz operation. A dynamic range of 97 dB was reported with a minimum admittance of 10 nS (100 MΩ) and a maximum admittance of 1 mS (1 kΩ). [15]

The system exhibited an impressive amount of dynamic range, and bandwidth over which measurements could be performed. This performance was achieved with reasonable power consumption of approximately 850 µW per sensor site. Although the system did utilize significant external support for signal generation, acquisition and processing the frequency response analysis (FRA) approach shows considerable promise for integration compared to FFT-based methods.

3.4. Other Works

A number of other works have been published on the design of impedance sensors and their biological applications. Two works described a direct conversion FRA approach with integrated multiplying ADCs to perform mixing without dedicated mixers [16, 17]. A work from 2009 described an array that measured cell impedance by utilizing the test impedance as part of a feedback loop [18]. In 2008, a sensor array was described that detected DNA polymerization through charge sensing [19]. A work from 2006 described a 5 x 10 programmable microarray capable of impedance spectroscopy, voltammetry and potentiometry analysis [20].

Chapter 4
Proposed Sensors

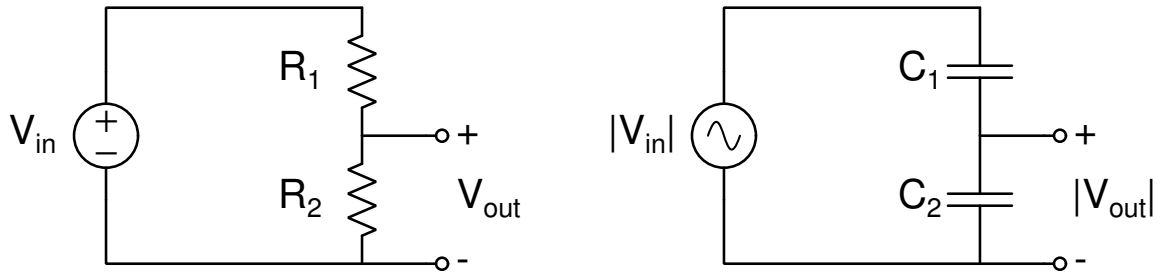
4.1. Capactive Sensor

4.1.1. Theory

The proposed capacitive sensor topology operates around a simple voltage divider. The classic resistor voltage divider, shown in Figure 4.1a, divides the input voltage by a ratio determined by R_1 and R_2. The expression for the output voltage is given in equation 4.1.

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in} \tag{4.1}$$

Equation 4.1 shows the output voltage is proportional to R_2 and is inversely proportional to the value of R_1. Therefore an increase of R_2, or a decrease of R_1 will result in a larger output voltage.



(A) Resistive (B) Capacitive

FIGURE 4.1. Voltage Dividers

The voltage divider concept can be extended to any impedance when an AC input voltage is used. Figure 4.1b show a capacitive divider which operates similarly to its resistive counterpart. The input magnitude is divided by a ratio determined by the value of C_1 and C_2. The output

expression is given in equation 4.2.

$$|V_{out}| = \frac{C_1}{C_1 + C_2}|V_{in}| \tag{4.2}$$

Derivation of equation 4.2 is shown below.

Given the following:

$$C_{total} = \frac{C_1 C_2}{C_1 + C_2}$$
$$i_{src} = C_{total}\frac{dv_{in}}{dt} \tag{4.3}$$

We can determine the voltage across C_2, assuming zero initial conditions.

$$v_{out} = v_{C_2} = \frac{1}{C_2}\int i_{src}dt$$
$$v_{out} = \frac{1}{C_2}\int C_{total}\frac{dv_{in}}{dt}dt \tag{4.4}$$
$$v_{out} = \frac{C_{total}}{C_2}\int dv_{in} \rightarrow v_{out} = \frac{C_1}{C_1 + C_2}v_{in}$$

For the capacitive divider the output magnitude is proportional to C_1 and inversely proportional to C_2, the reverse of the resistive divider. This is due to the inverse relationship between a capacitor's value and its impedance. Knowing the relationship between C_1, C_2 and $|V_{out}|$ the capacitive divider can be extended into a simple capacitive sensor. Given the situation depicted in Figure 4.2, where C_1 has become variable to some extent, a change in C_1 can be detected as a change in the magnitude of V_{out}.

The sensor concept can be further simplified by replacing the sinusoidal voltage source with a sawtooth waveform. An AC signal is still present so the divider operates as previously described, but with the added benefit of resetting every period. On-chip generation of a sawtooth is also trivial compared to sinusoidal signals. Utilizing a sawtooth waveform allows for a simple conversion

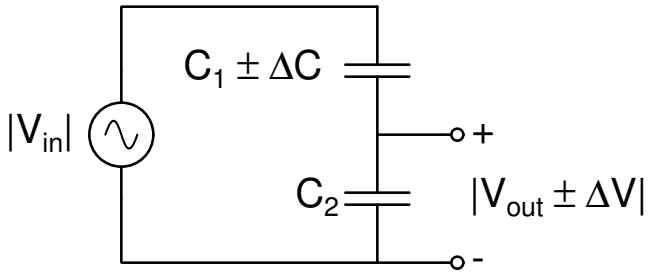


FIGURE 4.2. Capacitive Divider as a Sensor

from voltage to time with the inclusion of a comparator. As the capacitive divider affects the final output voltage within a time period, it is therefore altering the time the output signal is above or below a specific threshold. As the value of C_1 changes, and the duration the comparator remains triggered changes.

4.1.2. Prototype Sensor

A barebones integrated proof of concept is shown in Figure 4.3. In this design the op-amp operates as a buffer to drive the capacitive divider, which is composed of C_1 and C_2. $C_{3\text{-}5}$ are small valued capacitors that can be switched in to the divider individually to test the resolution of the system. The comparator converts the output voltage to a digital pulse, as described above.

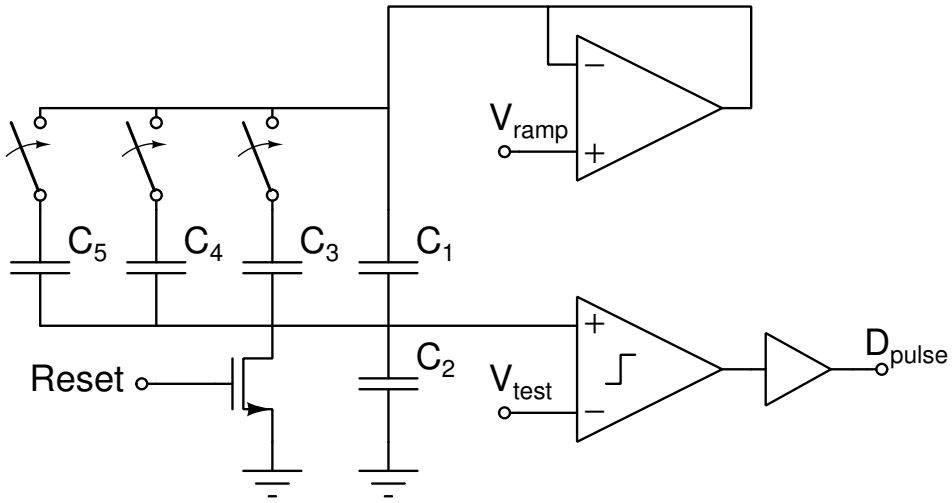


FIGURE 4.3. Prototype Capacitive Sensor

In actual sensing applications, C_1 and the switched capacitors are replaced with the capacitive DUT being measured. C_2 is a known reference capacitance whose value should be similar to the base value of C_1. The test voltage, V_{test}, can be adjusted to determine the base pulse width for testing. A reset signal exists to zero any residual charge that may exist on C_2.

The relationship between the test capacitance and the pulse duration is given by equation 4.5.

$$T_{pulse} = T_{per}\left(1 - \frac{V_{test}}{|V_{ramp}|}\frac{(C_1 + C_2)}{C_1}\right) \quad \text{if} \quad V_{test} < \frac{C_1}{C_1 + C_2}|V_{ramp}| \tag{4.5}$$

Taking the derivative of T_{pulse} with respect to C_1 with give us the expected sensitivity as given in equation 4.6.

$$\frac{\partial T_{pulse}}{\partial C_1} = \frac{V_{test}T_{per}}{|V_{ramp}|}\frac{C_2}{{C_1}^2} \tag{4.6}$$

The resolution of the capacitive sensor is ultimately limited by the time resolution of the system measuring the pulse duration. Integrated digital counters would be limited by the system clock, while external equipment is limited by its minimum time base. From equation 4.6 the sensitivity of the sensor can be increased by adjusting the either decreasing C_1, increasing C_2, increasing the test period, or reducing $|V_{ramp}|$. For simplicity, $|V_{ramp}|$is typically fixed at the supply voltage of the system. In sensing applications the base value of C_1 is most likely fixed. By increasing the size of C_2 the sensitivity of the system is potentially increased. Although the value of C_2 can not be increased indefinitely, as it increases the output voltage of the divider drops, and eventually the comparator will not be tripped therefore no pulse will be generated. The sensitivity can also be increased by using a higher V_{test}, although care must be taken to ensure it does not exceed the final output voltage of the divider or else no pulse is generated. The last tuning parameter, T_{per}, can also be increased to improve sensitivity. The length of the test can be extended as long as

the measurement system is capable of handling the pulse width, and the capacitor leakage does not affect the results.

4.1.3. Op-amp & Comparator

The op-amp used to drive the capacitive divider should have input common-mode range and output swing to properly replicate the desired sawtooth waveform. The prototype utilizes a rail-to-rail cross-coupled op-amp presented in [21], to replicate a sawtooth with magnitude equal to V_{DD}. Additionally the op-amp needs enough drive strength to source and sink the necessary current to prevent slewing with any desired value of base capacitance.

A rail-to-rail comparator would enable the sensor to accept any V_{test} voltage although this is not necessary. Other comparator parameters are relatively unimportant, as long as the delay is much smaller than the test period. A simple pMOS differential pair with a common source output stage was used as the comparator for the prototype sensor. With this comparator test voltages should be kept below $V_{DD} - V_{sat}$. The schematic, sizing and performance of the comparator and op-amp are discussed in detail in Chapter 5.

4.1.4. Additional Work

The capacitive divider concept was expanded upon in another work utilizing a pair of dividers [22]. The described sensor compared the output voltage of a reference divider to a test divider via a switched capacitor difference amplifier to determine the change in capacitance between the dividers. The described system adjusted for offset between the two dividers, and within the signal chain, via gain calibration in the difference amplifier. A process insensitive resolution of 10 fF was achieved..

4.2. General Purpose Impedance Sensor

The capacitive sensor prototype presented previously is limited to impedance sensing application where only a capacitive DUT is expected and of interest. A more general purpose impedance sensor is presented bellow which can be used in impedance sensing applications where a complex DUT impedance is expected.

4.2.1. System Topology

The proposed impedance sensor utilizes a dual-bride front-end to measure the impedance. Recall from equation 2.3, a division of two signals is necessary to compute the DUT impedance. The magnitude and phase of the DUT impedance can obtained independently according to the equations in 4.7. The impedance magnitude and phase are calculated on-chip, unlike the system presented in [11] which required an external data processor.

$$|Z_{DUT}| = \frac{|V_2|}{|V_1|}|Z_{ref}| \tag{4.7}$$

$$\underline{/Z_{DUT}} = \underline{/V_2} - \underline{/V_1} \quad \text{if} \quad \underline{/Z_{ref}} = 0$$

The impedance sensor is organized into 3 sections: the front-end, peak capture, and mixed-signal divider. A schematic of the measurement system is shown in Figure 4.4. The measurement front-end is composed of two auto-balancing bridges operated in a dual-bridge configuration and an automatic gain controller (AGC). The ratio between the DUT and reference magnitude is calculated by the peak capture system and mixed-signal divider. DUT phase is calculated in the phase module by comparing the relative time difference between zero crossings of the front-end outputs. An analysis of the system's detection resolution is discussed below. Design considerations pertaining to the front-end and AGC are discussed in subsection 4.2.3. Operation and limits of the

peak capture are discussed in subsection 4.2.4. The mixed-signal divider concept and topology is discussed in subsection 4.2.5. Details of the phase module are presented in subsection 4.2.6.

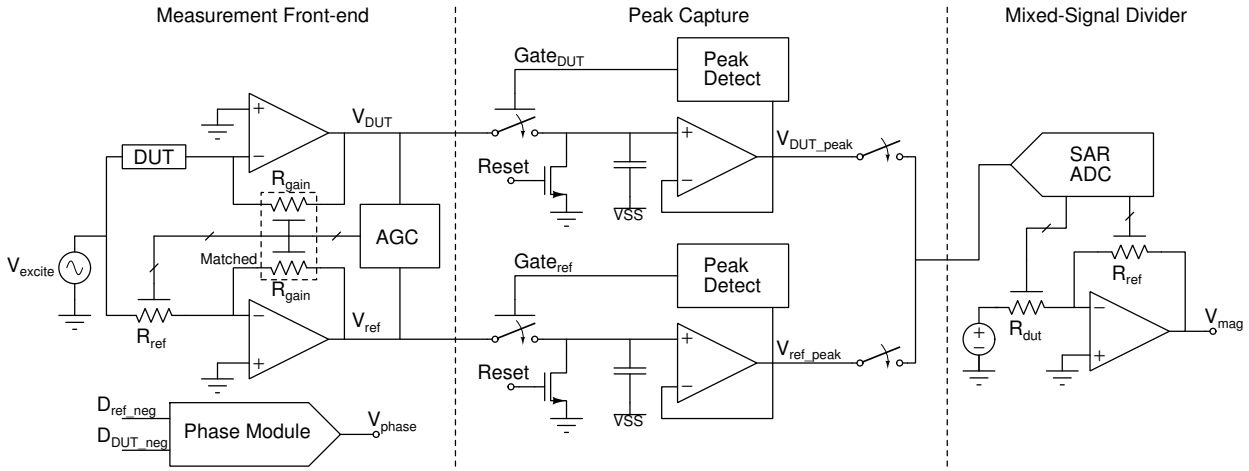


FIGURE 4.4. Impedance Sensor Schematic

4.2.2. Detection Resolution

The detection resolution of the system is defined as the minimum relative change in impedance that the system can detect. The system's limit of detection is determined by the front-end's output voltage and the resolution of the ADC within the mixed-signal divider. The LSB of the ADC determines the minimum detectable voltage change at the output of the front-end, therefore the minimum relative change that can be detected is given by equation 4.8.

$$\text{Resolution (\%)} = \frac{LSB}{|V_{out}|} \times 100 \tag{4.8}$$

Figure 4.5 shows the calculated minimum detectable resolution vs. front-end output magnitude for an 10-bit, 12-bit, & 14-bit ADC, assuming a 900 mV full-scale voltage.

From the figure, a higher resolution ADC always improves detection resolution, although diminishing returns occur around 14 bits and above. For a full-scale voltage of 900 mV, a 14-bit ADC has an LSB of approximately 55 μV, which places stringent requirements for op-amp noise

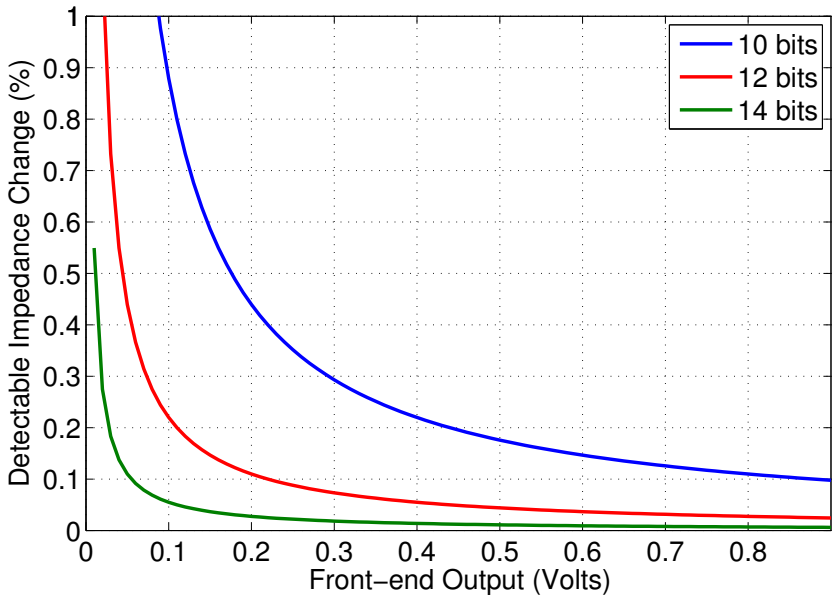


FIGURE 4.5. Detection Resolution vs. Output Voltage & ADC Resolution

and offset. A resolution of 12 bits was chosen for the the final design, which provides a detection resolution of .44 % for outputs greater than 50 mV. Keeping the output voltage above this limit can be accomplished by proper design of the AGC.

4.2.3. Front-end & Automatic Gain Control

The complete front-end is shown in Figure 4.6. It is composed of two auto-balancing bridges arranged in a dual-bridge configuration and an automatic gain controller. Each auto-balancing bridge is composed of a single op-amp and a digital feedback resistance. The AGC consists of digital control logic, 4 comparators and 3 digital resistors.

The measurement front-end is responsible for converting the current through the DUT and reference impedance into a voltage for processing by the back-end of the impedance sensor. Overall system accuracy and performance parameters are highly dependent on the performance of the front-end circuits. Op-amp bandwidth and swing create boundaries that the sensor must be

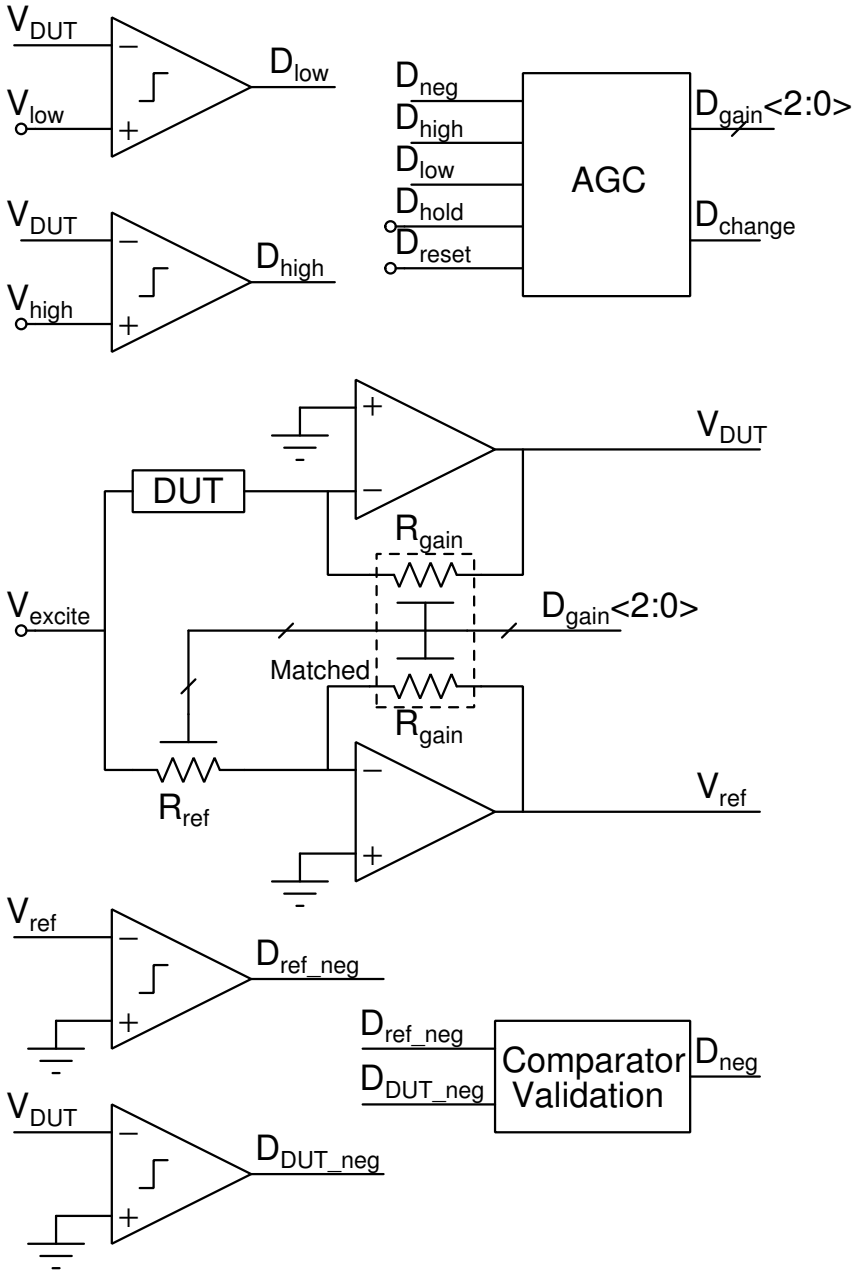


FIGURE 4.6. Measurement Front-end Schematic

operated within for target performance. Op-amp offset and resistor mismatch negatively impact the accuracy of the system.

To maintain a target resolution for the entire system, the front-end output magnitude must remain above a predetermined threshold. The threshold value can be determined from the desired system resolution and ADC resolution as shown in the previous section. The front-end also has an

upper limit for acceptable output magnitudes determined by the maximum swing of the op-amps in the signal chain. Outputs above this value will begin to clip and alter measurement readings.

Given these output constraints the DUT detection range is limited by the selected values for the reference and gain resistors. E.g. a gain and reference resistance of 85 kΩ and 2 kΩ, respectively, will limit the measurable impedance magnitude from 1 kΩ to 17 kΩ with a resolution of at least .44 %, assuming a 12-bit ADC and an output window of 50 mV to 850 mV.

The automatic gain controller is responsible for ensuring that both auto-balancing bridges operate within this output window and has the added benefit of expanding the measurable range of impedances. The automatic gain controller switches alternate values of R_{ref} and R_{gain} into the front-end circuits to greatly increase the measurement ranges while maintaining system precision. With the automatic gain controller the detectable impedance range can span orders of magnitude.

An automatic gain controller cannot infinitely extend the range of the system. The absolute lower bound of detectable impedances is set by the drive current of front-end op-amps, and the feasibility of creating accurate small reference resistors in silicon. The upper bound is limited by the feasibility of large resistors in silicon, and leakage current in the switching circuits. The upper bound could be further increased while maintaining reasonable resistors values by utilizing a larger excitation voltage, although this may lead to non-linearity in the DUT.

The implemented AGC relies on 4 comparators to determine information about the front-end outputs. One determines if the output has exceeded the lower bound. Another if it exceeds the upper bound. The last two remaining comparators and a logic system detect when it is valid to test the waveform. The signals, V_{high} & V_{low}, determine the upper and lower bounds the AGC tests against. The control logic outputs a 3-bit thermometer code that is used to control 3 digital resistors, R_{ref} and the R_{gain} pair. The AGC control logic has two external inputs to force a reset of the AGC or to instructed the AGC to hold its state regardless of the comparator outputs. The

control logic also outputs a reset signal when the gain state is changed which ensures the peak capture system properly captures the output peaks.

4.2.4. Peak Capture

An essential part of measuring the DUT impedance is acquiring the magnitude of the front-end outputs. The magnitude of each front-end channel is captured with a passive sample & hold circuit that is gated by a peak detector. The schematic of the peak capture system is shown in Figure 4.7.

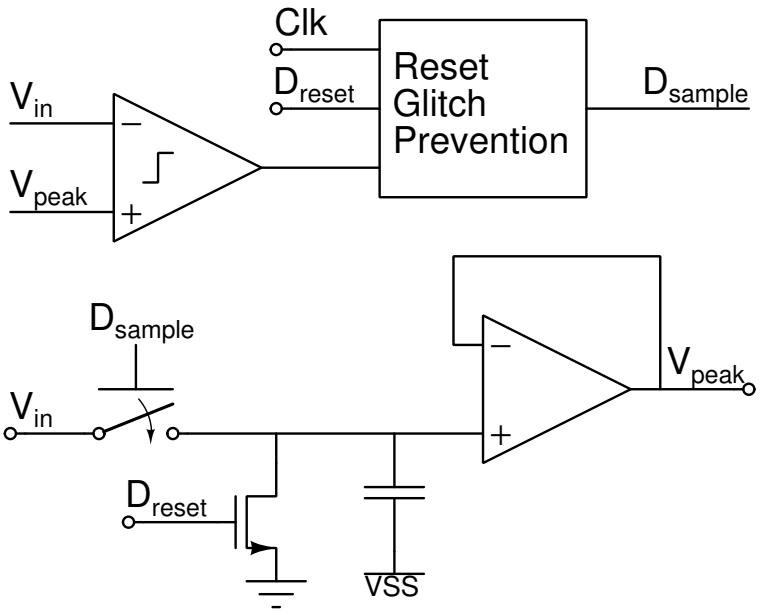


FIGURE 4.7. Peak Capture Schematic

Peak detection is accomplished through a high gain, low offset comparator. Each comparator monitors the output and input of its associated S&H circuit. When a input signal larger than the current output is detected the gate signal goes high to allow the S&H to capture the input signal. This is repeated until the peak value of the input signal is captured. At this time the gate signal falls and no more sampling occurs.

The sampling capacitors can be discharged to a zero value by the user via a reset signal, if necessary. The reset signal is also triggered when the AGC adjusts the gain to ensure the proper peak values are recaptured. Comparator output is fed into glitch prevention logic which prevents accidental sampling of transient glitches during reset.

4.2.5. Mixed-Signal Divider

A challenging aspect of the dual-bridge approach is the requirement for two analog voltages to be divided. The system described in [11] relied on the use of an external data processor to perform this operation. An integrated solution requires a method of performing division in silicon.

Methods exist for performing division in both the analog and digital domains. Straightforward digital division logic can be readily synthesized with the help of Verilog or VHDL, but requires 2N-bits to represent the quotient of 2 N-bit numbers. A resolution of 12 bits would produce an output word of 24 bits, an unacceptable amount of I/O for the application.

Division in the analog domain can be performed by exploiting the non-linearities of MOSFETs [23], clever application of analog multipliers [24], exploiting the logarithmic properties of diodes [25], or by linear MOSFETs & current manipulation [26, 27].

For example, exploiting the properties of logarithms can transform the division operation into subtraction operation as shown:

$$\frac{A}{B} = \text{antilog}(\log(\frac{A}{B})) = \text{antilog}(\log(A) - \log(B)) \tag{4.9}$$

Input signals are fed through logarithmic amplifiers, subtracted by some means and an anti-log operation is performed to achieve the quotient. This technique, and the other mentioned analog dividers, can be easily fabricated in silicon. However many of the designs have stringent input

requirements, poor linearity or process dependent gain. A desirable division scheme for the system would have a large input range, and a process insensitive gain, preferably of 1.

The implemented mixed-signal divider operates around a basic inverting amplifier, as shown in Figure 4.8. The output of the inverting amplifier is given by equation 4.10.

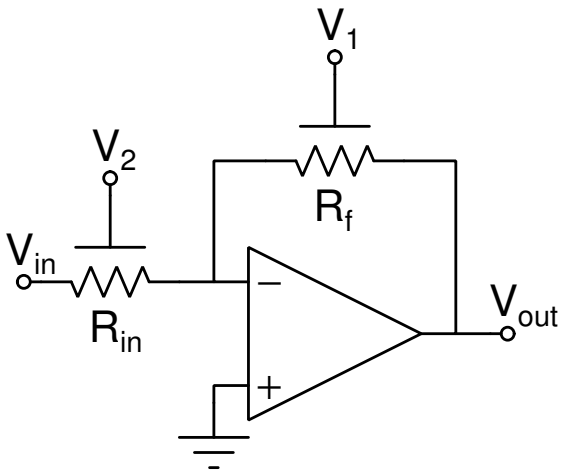


FIGURE 4.8. Inverting Amplifier as a Divider

$$V_{out} = -\frac{R_f}{R_{in}} V_{in} \tag{4.10}$$

Given some form of voltage sensitive resistance

$$\begin{aligned} R_f &\propto kV_1 \\ R_{in} &\propto lV_2 \end{aligned} \tag{4.11}$$

division of two voltages can be accomplished.

$$V_{out} = \frac{R_f}{R_{in}} V_{in} \rightarrow V_{out} = \frac{V_1}{V_2} V_{in} \text{ if } k = l \tag{4.12}$$

A major hurdle in implementing the divider in such a manner is creating a voltage controlled resistance. Two possible approaches are to use a MOSFET operating in the linear region or a switched capacitor as a simulated resistor.

A MOSFET operating in the linear region obeys the following first order model.

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{OV}V_{DS} - \frac{V_{DS}^2}{2}) \tag{4.13}$$

By assuming $V_{DS} \ll 1$ the resistance of the MOSFET as a function of V_{GS} is given by

$$\begin{aligned} I_D &= k_n^{'} \frac{W}{L}(V_{OV}V_{DS}) \quad \text{if} \quad V_{DS} \ll 1 \\ R_{linear} &= \frac{V_{DS}}{I_D} = \frac{1}{k_n^{'}\frac{W}{L}V_{OV}} \end{aligned} \tag{4.14}$$

This method has a number of limitations, first the controlling voltage and divider input and output must be limited to ranges that guarantee the MOSFET is within its linear operating region. Second, the linearity of the resistor only holds for small values of V_{DS}, and third the value of the resistance is highly dependent on process parameters.

A capacitor switched at a fixed clock rate is capable of simulating a resistance with a value given by

$$R_{eq} = \frac{T_{period}}{C} \tag{4.15}$$

In combination with a voltage controlled oscillator is would be feasible to implement a voltage controlled resistance. Given a desired resistance range of R to $2^{12}\times$R, a VCO would need to be tunable across orders of magnitude. Designing such a VCO might be possible, but doing so with a linear response would be incredibly difficult. Additional concerns like leakage, charge injection and switch non-linearity would result in further error.

To avoid the limitations of the two methods described above, digitally controlled variable resistors, refered to as digital resistors, were implemented. An ADC converts the control voltages into digital words which are then presented to the digital resistors. A single ADC is used for the conversion of both control voltages to eliminate the effects of mismatch between two ADCs. Every conversion cycle the ADC alternates between the two input voltages and stores the result into the correct output register. A schematic of the complete mixed-signal divider is shown in Figure 4.9.

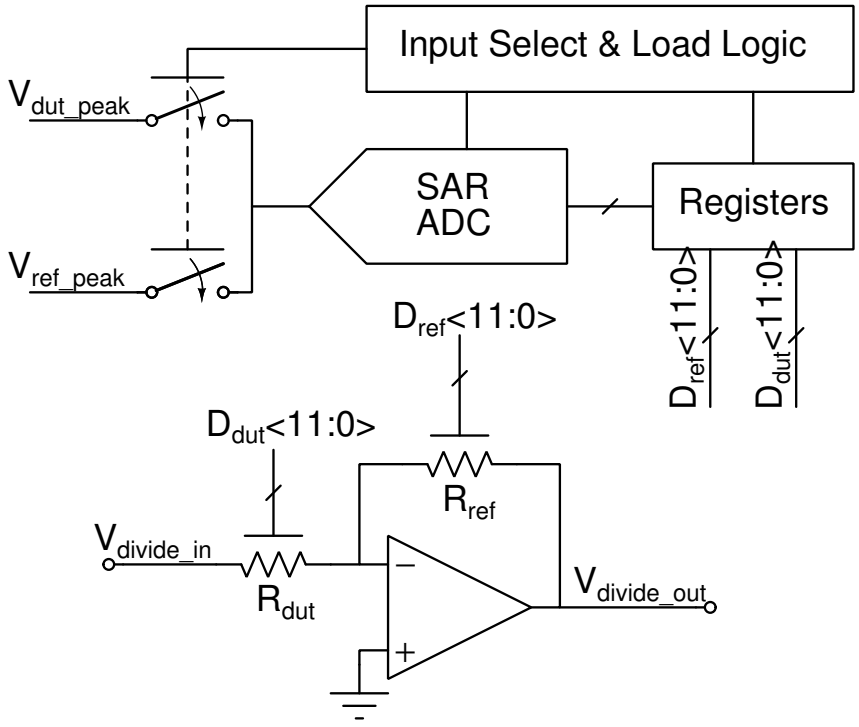


FIGURE 4.9. Mixed-Signal Divider Schematic

Each digital resistor is created from a series of switched binary weighted resistors. The value of each digital resistor is given by $R = (N + 1)R_{base}$ where N is the decimal value of the digital control code. Substituting the expression for the digital resistors into the expression for

the inverting amplifier equation gives the following

$$V_{out} = \frac{(N+1)R_{base}}{(M+1)R_{base}} V_{in} = \frac{(N+1)}{(M+1)} V_{in} \tag{4.16}$$

The addition of the unswitched resistor in each digital resistor prevents the possibility of the a 0 in the numerator or denominator, which could produce an undefined result. An error is introduced by the additional resistance but it is below 1% for expected usage. Details of the digital resistor design and divder performance are discussed in Chapter 5.

4.2.6. Phase Module

The phase of the DUT impedance is acquired by comparing the relative phase of the two front-end outputs. Using two comparators from the AGC, the phase module monitors the zero crossing of both bridge outputs. When either output crosses zero, a 12-bit counter begin. The counter is clocked so a desired resolution can be achieved, typically above the system clock. The counter operates until the other signal's (the terminating signal's) zero crossing is detected. The counter value at this point now represents the time shift between the two outputs and the relative phase can be calculated as:

$$\theta^\circ = \frac{N_{counter} \times T_{clk}}{T_{per}} \times 360^\circ \tag{4.17}$$

If additional zero crossings in initiating signal are detected before the terminating signal occurs the counter value is reset, and the previous crossing is assumed to be a false start. To indicate whether the phase is leading or lagging a flag is set by the phase module to indicate which waveform peak was detected first. The 12-bit output is loaded into another register clocked at the system rate and then fed into a 12-bit DAC for output. This system allows a 12-bit resolution

while only utilizing 2 pins and no serial interface. A schematic of the phase module is shown in Figure 4.10

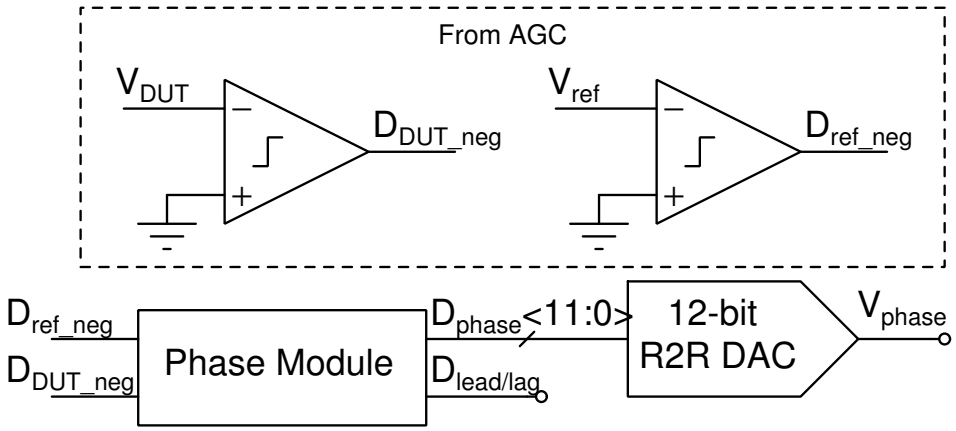


FIGURE 4.10. Phase Module Schematic

Chapter 5
Simulation Results

Simulations of the proposed sensor systems were performed with Cadence Spectre and AMS simulators in a Texas Instrument .180 µm 1.8 V CMOS process. Simulations were performed at room temperature in the nominal corner unless otherwise specified.

5.1. Capacitive Sensor

The prototype sensor proposed in Chapter 4 and shown, again, in Figure 5.1 with labels for each component was simulated to determine its expected performance. Table 5.1 summarizes the chosen design parameters, and component values, for implementing the prototype sensor. Switches $S_{1\text{-}3}$ are implemented as CMOS switches with both FETs having the dimensions reported in the table.

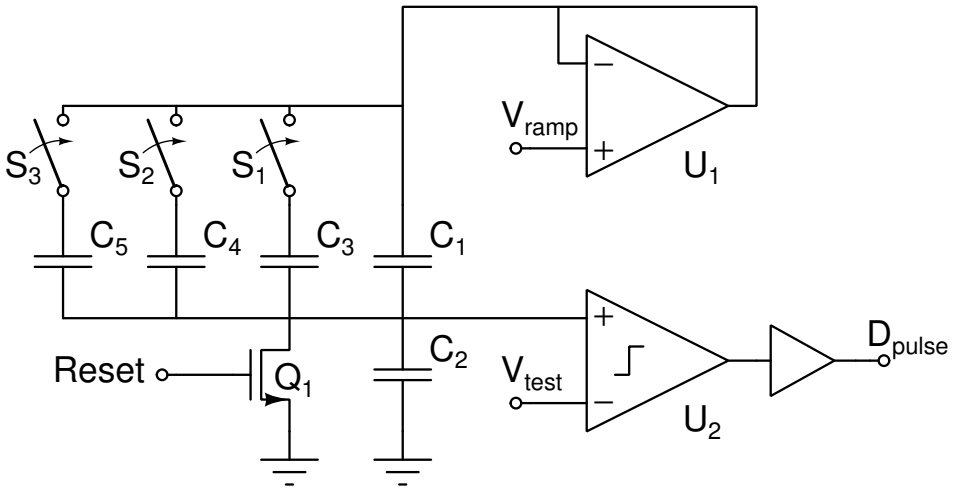


FIGURE 5.1. Labeled Capacitive Sensor Schematic

The chosen parameters produce a theoretical base pulse width of 458 µs and a sensitivity of 361 ns/fF, implying that a 1 MHz counter should be capable of detecting a 5 fF change in

TABLE 5.1. Capacitive Sensor Parameters

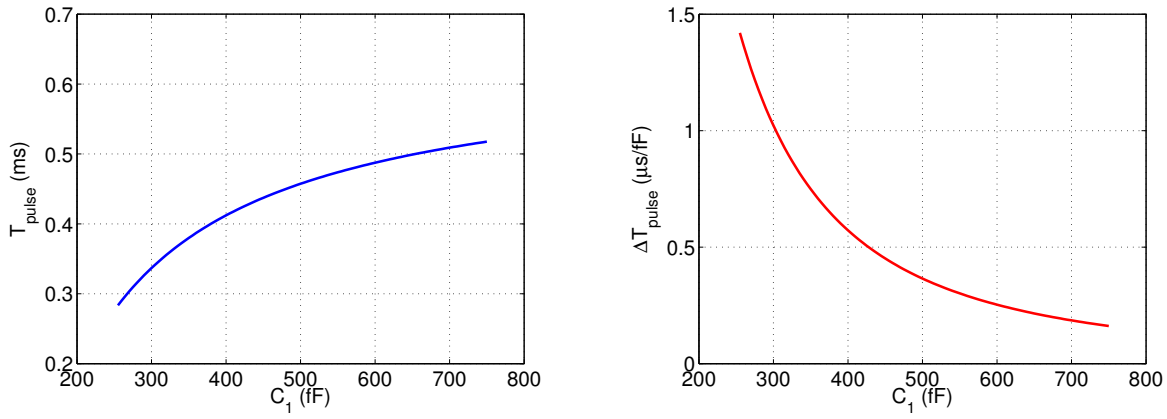
Parameter	Value
T_{per}	1 ms
V_{test}	650 mV
$\lvert V_{ramp} \rvert$	1.8 V
C_1	500 fF
C_2	250 fF
C_3	5 fF
C_4	10 fF
C_5	15 fF
Q_1	.22/.18 µm
$S_{1\text{-}3}$	2/.18 µm

capacitance. $C_{3\text{-}5}$ were chosen such that the capacitance delta could be set to any value between 5 fF and 30 fF, in 5 fF steps. The ideal sensor response and sensitivity vs. C_1 are shown in Figure 5.2a & 5.2b, respectively. Simulated sensor performance is presented after the op-amp design is discussed.

5.1.1. Op-amp & Comparator

The prototype sensor utilizes two op-amps to operate. The first, U_1, a cross-coupled rail-to-rail op-amp, is used to drive the capacitive divider. A schematic of the op-amp is shown in Figure 5.3. The op-amp uses dual input pairs and a push-pull output stage to allow op-amp to

operate from rail-to-rail in unity gain mode. The cross-coupled architecture provides a very high impedance load to the differential pairs and is capable of maintaining a proper bias voltage for the output stage over a wide range of bias currents. Table 5.2a list the device sizes that were chosen for the op-amp and Table 5.2b summarizes key performance parameters of the op-amp. In the prototype sensor described above, with a $|V_{ramp}|$ of 1.8 V, the op-amp successfully drives the capacitive divider with an error of no more than 5 mV.



(A) Response (B) Sensitivity

FIGURE 5.2. Calculated Sensor Response & Sensitivity

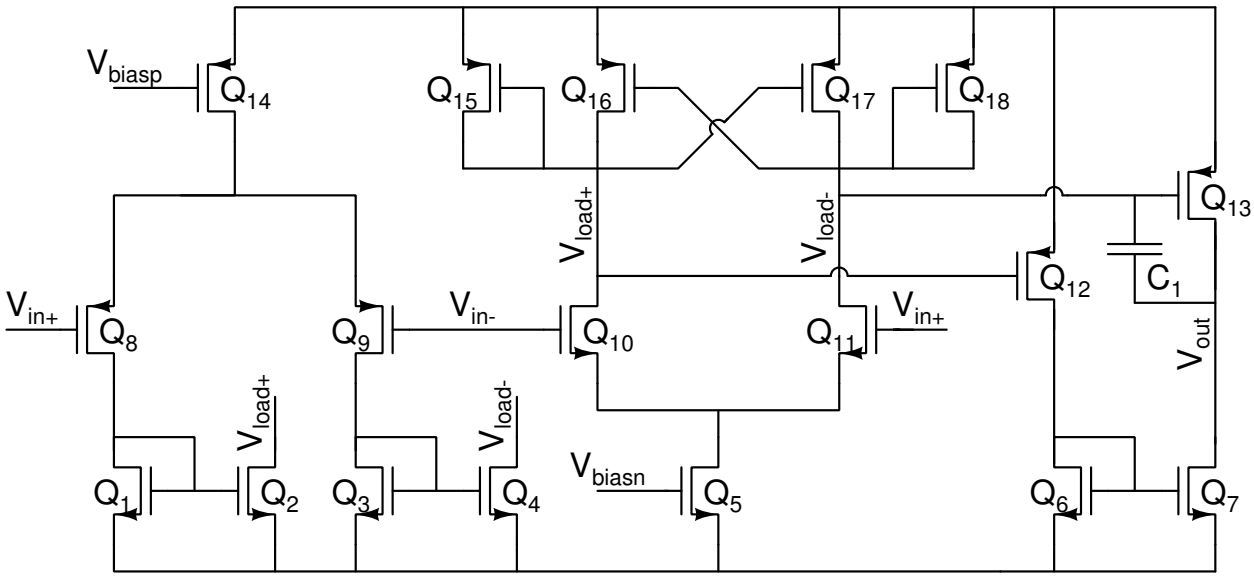


FIGURE 5.3. Capacitive Sensor Op-amp Schematic

TABLE 5.2. Capacitive Sensor Op-amp Sizing & Performance

(A) Device Sizes

Device	Value
$Q_{1\text{-}4,15\text{-}18}$	2.2/1.8 µm
Q_5	.22/.18 µm
$Q_{6,7,12,13}$	.8/.18 µm
$Q_{8\text{-}11}$	4/1 µm
Q_{14}	.28/.18 µm
C_1	750 fF

(B) Performance Specs

Parameter	Value
A_v	71 dB
Unity Swing	0 - 1.8 V $\pm$1.75 mV
Unity BW	8.58 MHz
Offset	7.4 mV (3-σ)
Area	20 µm x 40 µm
Max Power	14 µW

The second op-amp, U_2, is used as a comparator to generate a pulse from the output of the capacitive divider. The schematic for the comparator is shown in Figure 5.4. A pMOS input pair is utilized which allows for test voltage values below V_{DD} - V_{sat}. Table 5.3a lists the device sizes for the comparator and Table 5.3b summarizes some specification of the comparator.

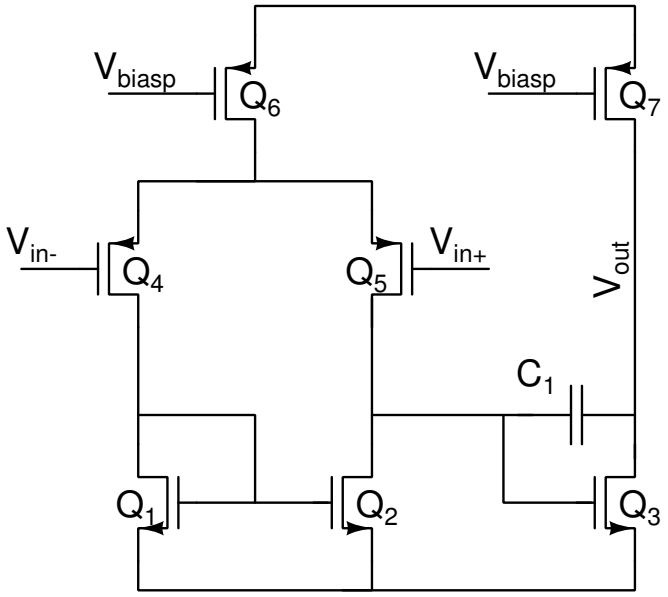


FIGURE 5.4. Capacitive Sensor Comparator Schematic

TABLE 5.3. Capacitive Sensor Comparator Sizing & Performance

(A) Device Sizes

Device	Value
$Q_{1,2}$	30/25 µm
Q_3	10/1 µm
$Q_{4,5}$	80/2 µm
Q_6	.65/.18 µm
Q_7	4.9/.9 µm
C_1	1 pF

(B) Performance Specs

Parameter	Value
A_v	94 dB
$BW_{-3\ dB}$	260 Hz
BW_{unity}	5.4 MHz
Offset	1.1 mV (3-σ)
Area	60 µm x 65 µm
DC Power	21.6 µW

5.1.2. Prototype Sensor Simulation

Transient simulations of the prototype sensor were performed with Cadence Spectre. The baseline sensor response, with no additional capacitance switched in, is shown in Figure 5.5. This

simulation determines the base pulse width that is compared against when the test capacitance is increased. The base pulse width according to the simulation is only 134 µs, approximately a third less than the calculated value. Most of this significant error can be attributed to the additional unaccounted for capacitance attached to the divider. The additional capacitance arises from the input capacitance of the comparator, the parasitic capacitance of the CMOS switches, parasitic substrate capacitance, and the input capacitance of additional signal buffers attached for internal node inspection.

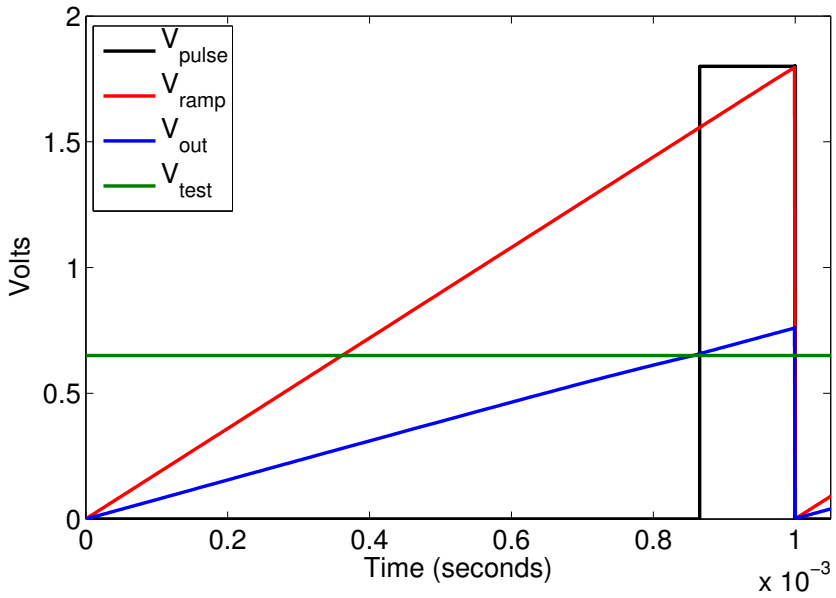


FIGURE 5.5. Base Capacitance Simulation Output

The output magnitude of the divider, 760 mV, is approximately 60 % of the expected value, 1.2 V. This indicates that the effective value of C_2 is being increased by the spare capacitance. Using equation 4.5 the effective value of C_2 is calculated to be approximately 700 fF, which means there is 450 fF of additional capacitance on the divider. The sensitivity of the divider with the new value of C_2 is calculated to be 1.01 µs/fF. Table 5.4 shows the simulated pulse widths for every testable capacitance. From the data is can be determined that the prototype response

is non-uniform. This may be a result of the imperfect nature of CMOS switches, and their non-linear parasitic capacitance. Regardless, even if the sensor response were to remain non-uniform in actual sensing applications the divider topology could still useful. Applications exist where the actual value of the capacitor is unimportant and only sensing that change occurred is necessary, as discussed in [14].

TABLE 5.4. Capacitive Sensor Simulated Pulse Widths

ΔC_1	T_{pulse}	ΔT_{pulse}	Calculated ΔC_1
+0 fF	134.2 µs	0 µs	+0 fF
+5 fF	140.5 µs	6.2 µs	+6.3 fF
+10 fF	145.9 µs	5.4 µs	+11.9 fF
+15 fF	150.7 µs	4.7 µs	+16.9 fF
+20 fF	156.6 µs	5.9 µs	+23.2 fF
+25 fF	161.8 µs	5.1 µs	+28.9 fF
+30 fF	167.6 µs	5.7 µs	+35.4 fF

If this sensing topology were applied to an array, or any application where the results between multiple sensor's are compared, mismatch between the different sensors would degrade the limit of detection if calibration was not performed. A Monte Carlo analysis was performed to estimate the limit of detection that could be achieved between sensors without additional calibration. Base capacitance, +5 fF, +10 fF and +15 fF were tested with 50 points per step. The mismatch of C_1, $C_{3\text{-}5}$ and the CMOS switches was not included in the analysis under the assumption that these components would not exist in actual sensing applications. The results for each step were

fit with a Gaussian distribution and plotted together in Figure 5.6. The results from the Monte Carlo analysis indicate that the sensor topology could successfully resolve a difference of 10 fF between a collection of non-calibrated sensors.

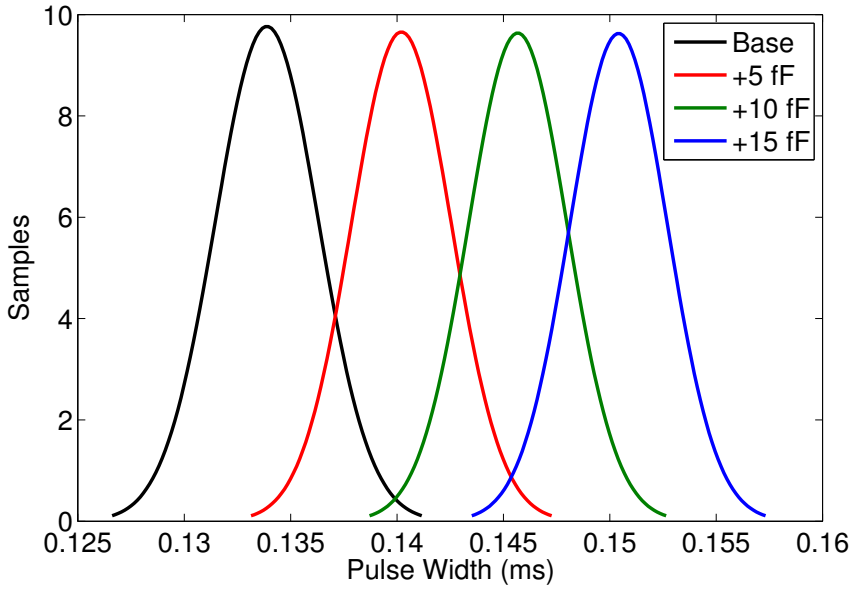


FIGURE 5.6. Monte Carlo Analysis Of Capacitive Sensor

Calibration of a sensor array is straight forward if the base capacitance of each sensor is assumed to be uniform. First, a base pulse width for each sensor site is acquired and stored. Second, after experimentation, the delta pulse width for each site is calculated from its respective base pulse width. Finally, the capacitance change can be estimated from equation 4.5 or 4.6 and the results between the array sites can be compared.

5.2. General Purpose Impedance Sensor

Transient mixed-signal simulations of the impedance sensor and its subsystems were performed to characterize their accuracy, resolution and functionality. Subsystems were tested and simulated independently to best characterize their performance, and possible limitations in the entire sensor.

The complete sensor was then simulated to determine its accuracy and resolution. The design utilizes a split rail of $\pm.9$ V, with all circuits referenced to a common-mode of 0 Volts. Voltage magnitudes reported are negative relative to common-mode due to the chosen op-amp topology. The sensor operates on a standard clock of 200 kHz.

5.2.1. Op-amp & Comparator

The full system utilizes 5 single-ended op-amps and 7 high gain comparators. There is at least one op-amp or comparator in each sensor subsystem. The performance of these circuit have a strong effect on the speed, accuracy and resolution of the system as a whole. A large source of inaccuracy within the system is due to the front-end op-amps as any error introduced propagates through the entire system.

Each bridge can be considered a single pole closed loop system with a fixed gain-bandwidth product. As the closed loop gain of the bridge increases the usable bandwidth decreases a proportional amount. When the reference and DUT impedance are not the same, the closed loop gain between the bridges differs and the bandwidth between the bridges differs as well. When bandwidth of either bridge begins to roll off before the other an error is introduced in the measurement. Op-amp bandwidth (and gain) determines the gain-bandwidth product of the bridges and thus determines the maximum test frequency that can be used with a given amount of error. Figure 5.7 demonstrates the effects of test frequency on the measurement error when the DUT is smaller and larger than the reference impedance. The dashed line represented the chosen maximum test frequency of 2.5 kHz, which limits error to less than 1 % in both cases.

Op-amp offset can introduce significant error through the measurement system. Offset in the front-end manifests itself as a variation in the output magnitude. Offset in the peak capture system impairs its ability to accurate determine the waveform peak. The ADC is also affected by

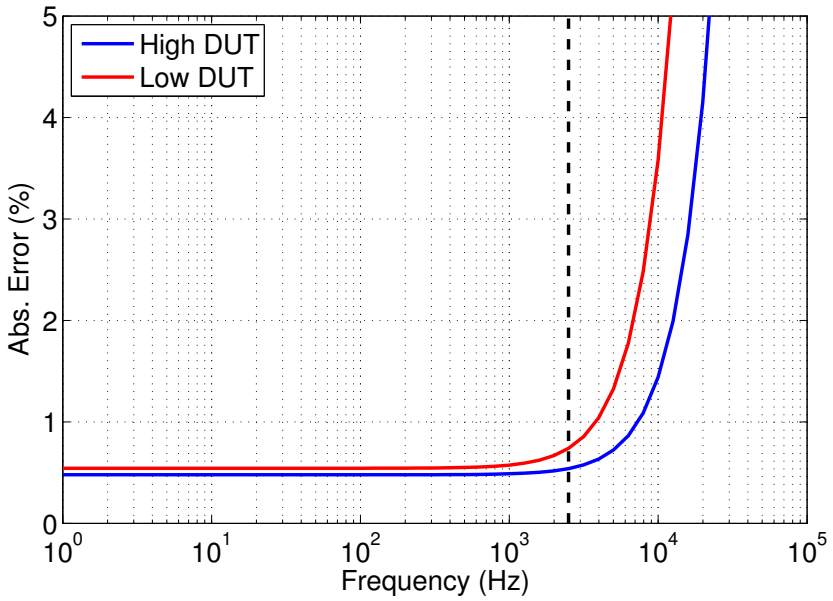


FIGURE 5.7. Impedance Measurement Error vs. Test Frequency

offset in its comparator. Therefore the op-amp and comparator were designed with minimal offset. Comparator sensitivity plays a significant role in the accuracy of the peak capture system, and ADC within the mixed-signal divider. A properly designed comparator should be able to resolve the LSB of the ADC.

Fortunately the above mentioned parameters do not affect the precision of the system, only the accuracy. Op-amp noise can affect the precision of the system. To maintain the best possible precision the total noise generated in the front-end should be kept below the LSB of the ADC, 220 μV. Many components of the system operate at or near DC, thus flicker noise is prominent than thermal noise.

The op-amp is a low offset variant of the op-amp used as a comparator in the capacitive sensor. It is composed of a PMOS input pair and common-source output stage. For low offset and flicker noise the input pair and load employ large device geometries. A schematic of the op-amp is shown in Figure 5.8. Table 5.5a and 5.5b list the device sizes and key specifications, respectively, for the op-amp.

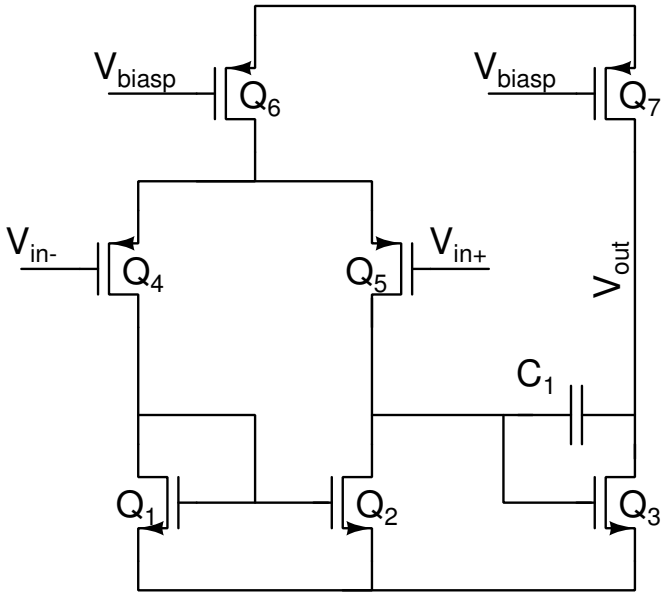


FIGURE 5.8. Impedance Sensor Low Offset Op-amp Schematic

The comparators used in the system are a modification of the rail-to-rail cross-coupled op-amp presented in [21]. The op-amp was modified with significantly enlarged input pairs, mirrors, and loads for reduced offset. An additional output stage was added and compensation capacitor removed for quicker response time. The comparator schematic can be seen in Figure 5.9. Device sizing and critical performance specifications are shown in Table 5.6a and 5.6b, respectively.

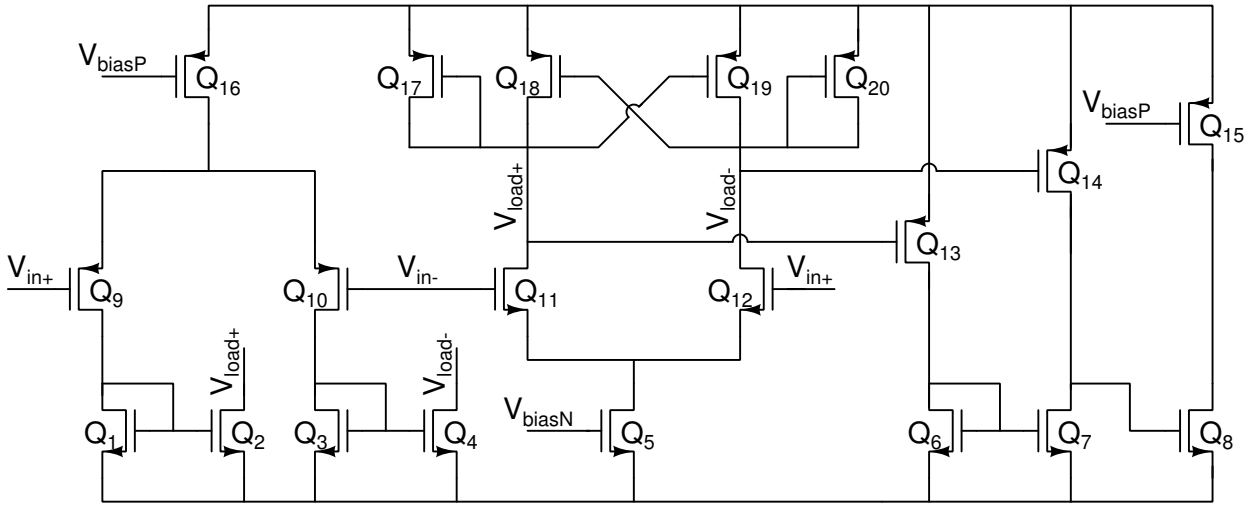


FIGURE 5.9. Impedance Sensor Low Offset Comparator Schematic

TABLE 5.5. Impedance Sensor Low Offset Op-amp Sizing & Performance

(A) Device Sizes

Device	Value
$Q_{1,2}$	30/25 µm
Q_3	20/1 µm
$Q_{4,5}$	100/5 µm
Q_6	.65/.18 µm
Q_7	9.16/.9 µm
C_1	2 pF

(B) Performance Specs

Parameter	Value
A_v	94 dB
$BW_{-3\ dB}$	109 Hz
BW_{unity}	2.81 MHz
PM	45.2°
Offset	696 µV (3-σ)
Input Noise (1 Hz - 2.8 MHz)	24.6 nV^2
DC Power	34.7 µW
Area	70 µm x 70 µm

TABLE 5.6. Impedance Sensor Low Offset Comparator Sizing & Performance

(A) Device Sizes

Device	Value
$Q_{1\text{-}4}$	25/10 µm
Q_5	7.2/.72 µm
$Q_{6\text{-}8,13,14}$	.8/.18 µm
$Q_{9\text{-}12}$	60/5 µm
Q_{15}	.375/.35 µm
Q_{16}	6/.72 µm
$Q_{17\text{-}20}$	22/2.5 µm

(B) Performance Specs

Parameter	Value
A_v	115 dB
$BW_{\text{-3 dB}}$	126 kHz
BW_{unity}	761 MHz
Offset	1.17 µV (3-σ)
DC Power	74.4 µW
Area	40 µm x 125 µm

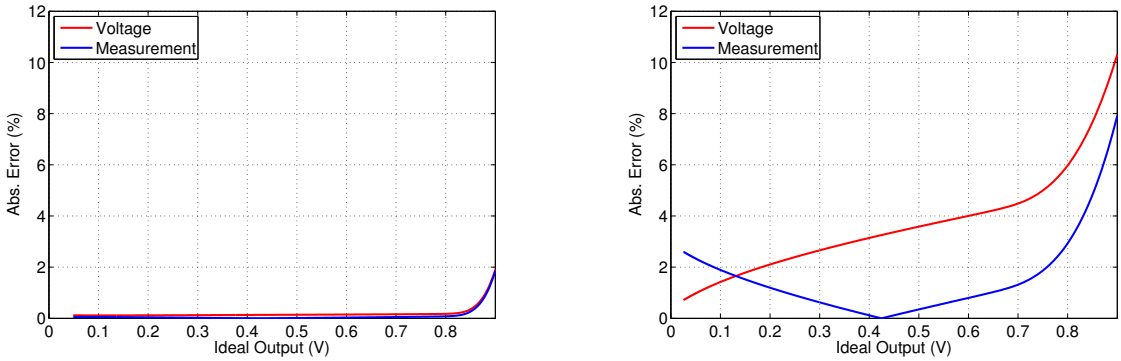
5.2.2. Front-End & Automatic Gain Control

As discussed previously the front-end performance has significant impact on the performance of the entire system. The effects of op-amp bandwidth on the accuracy of the front-end has already been discussed. Three other important factors are the output swing, output impedance (or drive strength) and offset. The maximum output voltage of the op-amp, or swing, sets the lower bound of impedance that may be accurately measured with a fixed feedback resistance. As the DUT impedance decreases the output voltage rises until it is clipped by the swing of the op-amp, at this point the measurement error of the front-end rises dramatically.

An additional measurement error is introduced when the op-amp can not "drive" the feedback or load impedance with enough current. This occurs when the feedback or load impedance is small enough that it degrades the output impedance of the amplifier. A degraded output impedance reduces the open loop gain of the op-amp and the output drifts away from the expected output.

Figure 5.10a & 5.10b show the voltage and measurement errors due to limited output swing and limited drive strength, respectively. A maximum output of 850 mV was selected to keep error below 5 % for either case. A lower bound of 50 mV was set by the peak capture system, which is discussed in the following section. Ensuring the front-end does not output a voltage above or below this window is accomplished via the automatic gain controller.

The AGC design provides 4 levels of gain which increases the range of the sensor from 30 Ω to 2.5 MΩ with an absolute error of no more than $\pm$5 %. Figure 5.11 shows the calculated front-end output voltage for the supported test impedance range. The dotted lines represent the DUT limits for each gain code. The selected values of R_{ref} & R_{gain} cause a small amount of overlap between the gain codes, which prevents undesirable oscillation between two gain settings. The values of R_{ref} was chosen so that it falls within the middle of the operating range, approximately 425 mV.



(A) Swing Limited (B) Drive Limited

FIGURE 5.10. Impedance Measurement Error vs. Output Voltage

Table 5.7 summarizes the design values for R_{ref} & R_{gain} for each gain code. The Verilog code for implementing the AGC can be seen in Appendix A.

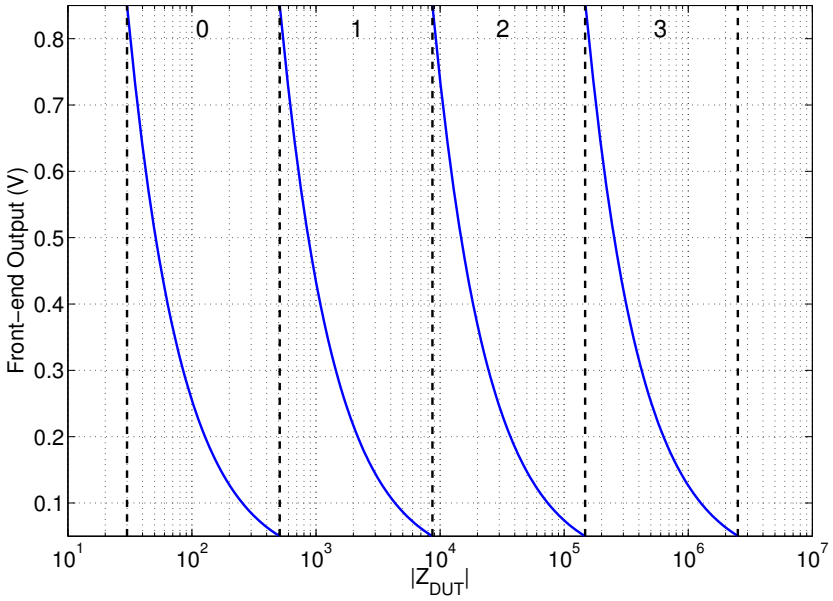


FIGURE 5.11. Expected Front-end Output vs. DUT Impedance

The variable gain and reference resistors are implemented as digital resistors controlled by a thermometer code. CMOS switches are used to bypass progressively high valued resistors. The schematic of these resistors can be shown in Figure 5.12. By utilizing a thermometer coded gain value and the bypass-style structure the overall size of the resistors can be reduced. Each

TABLE 5.7. AGC Design Values

Gain	R_{gain}	R_{ref}	DUT_{low}	DUT_{high}
0	2.55 kΩ	60 Ω	30 Ω	510 Ω
1	43.35 kΩ	1.02 kΩ	510 Ω	8.67 kΩ
2	737.8 kΩ	17.36 kΩ	8.67 kΩ	147.56 kΩ
3	12.54 MΩ	295.12 kΩ	147.56 kΩ	2.51 MΩ

successive physical resistor's value is actually the desired value minus the value of the previous resistor. Thus R_4 has a physical value of 11.8 MΩ with a effective value of 12.54 MΩ. Compared to the latter-style resistors used in the mixed-signal divider, the bypass-style has improved low resistance performance at the cost of more absolute error at high resistances due to the leakage currents through the MOSFETs switches. The switches were sized such that the relative error of each value was kept below .5 %.

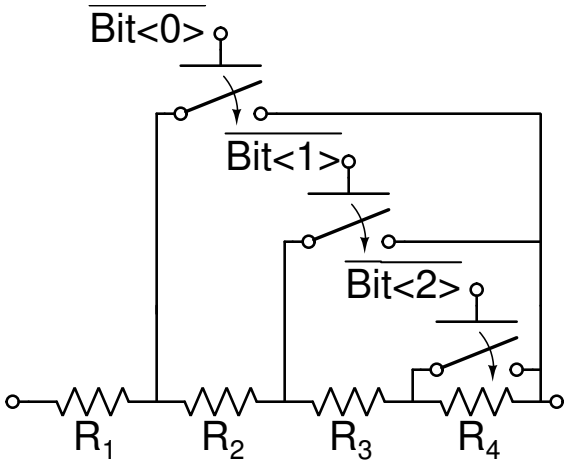


FIGURE 5.12. Bypass-style Digital Resistors for AGC

Simulations demonstrating the operation of the AGC were performed. Figure 5.13 & 5.14 show two simulations were the AGC steps up and steps down the gain to adjust for a changing

DUT impedance. Both simulations were performed with resistive DUTs at a test frequency of 2.5 kHz. The first shows the AGC response when the DUT increased from 2 kΩ to 35 kΩ. The second test shows the response when the DUT is decreased from 35 kΩ to 2 kΩ.

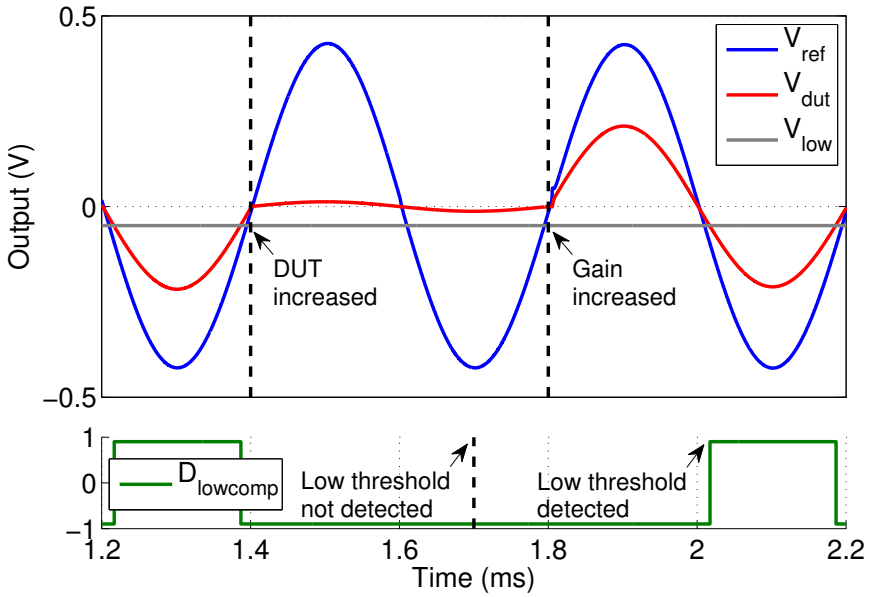


FIGURE 5.13. Impedance AGC Step Up

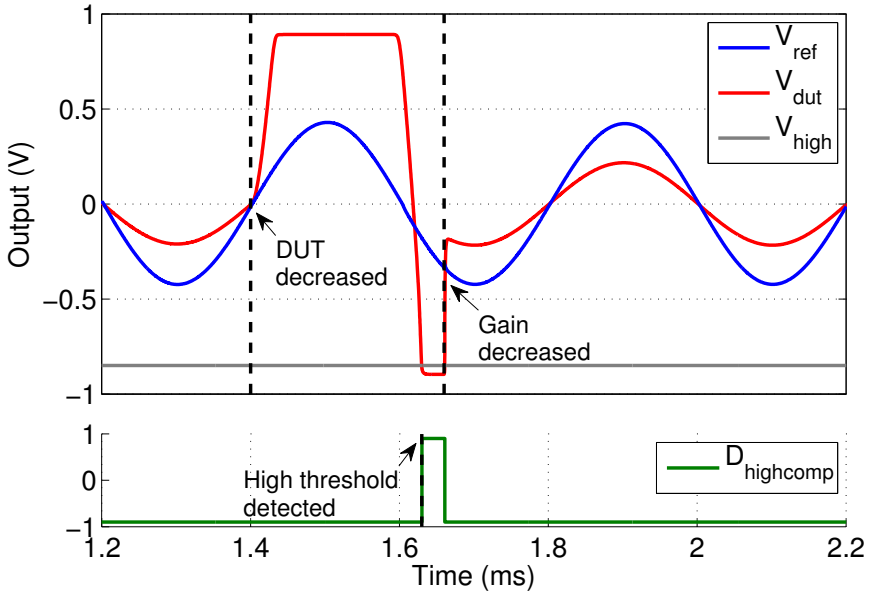


FIGURE 5.14. Impedance AGC Step Down

5.2.3. Peak Capture

The performance of the peak capture system places important limits on the overall system architecture. The accuracy at which magnitude measurements can be made is highly dependent on how accurately the peak capture system operates. The S&H circuits use 2 pF sampling capacitors and 1/.18 µm CMOS switches. The simulated output of a single peak capture circuit, after a reset event, is shown in Figure 5.15.

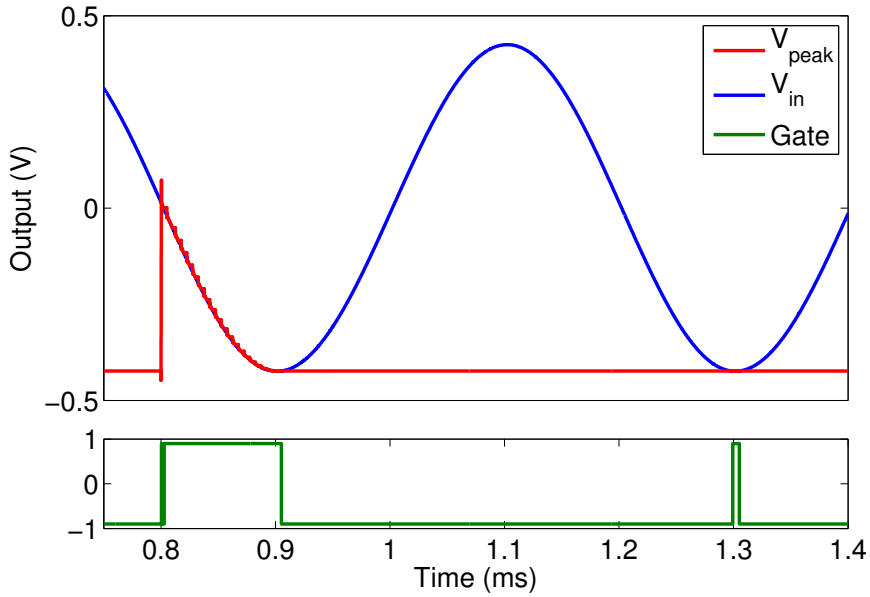


FIGURE 5.15. Peak Capture Simulation

Like the front-end, op-amp output swing sets the upper bound of acceptable inputs to the peak capture system. The system's ability properly detect signal peaks sets a lower limit on acceptable input levels as well. As the input magnitude drops the difference between the input and output values at the waveform peak decreases which increases the capture error. These two factors limit the acceptable range of input values to the peak capture system, and therefore set the transition points for the AGC. Figure 5.16 shows the capture error vs. input magnitude for the peak capture system.

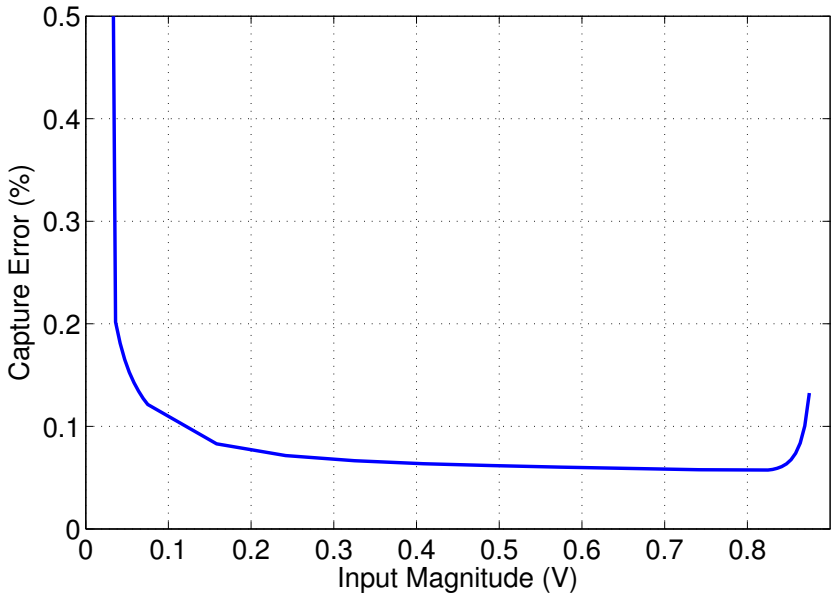


FIGURE 5.16. Peak Capture Error vs. Input Magnitude

A lower limit of 50 mV was selected which limits capture error to .25 %. The AGC maintains the front-end output above this limit and below the maximum limit determined previously.

The peak capture system also limits the frequencies that can be used in measurement. Op-amp settling time and comparator resolution time limit the maximum clock rate that the peak capture system can be operate at. To obey Nyquist criteria the input frequency cannot exceed half the system clock frequency, although significant capture error may occur far before the Nyquist frequency. As test frequency increases, the peak width decreases relative to the clock width and the possibility that a clock event will occur during the waveform peak decreases. If no clock event occurs current the waveform peak the proper peak value can not be sampled.

5.2.4. Mixed-Signal Divider

The mixed-signal divider calculates the ratio between the two front-end outputs to calculate the ratio between the DUT and reference impedance. The two significant circuits within the mixed-signal divider are the ADC and digital resistors.

The ADC is a Successive Approximation Register built around a 12-bit R2R sub-DAC. A schematic of the ADC is shown in Figure 5.17. The ADC does not have its own sample & hold circuit but instead piggybacks on the peak capture S&H circuits. This eliminates additional errors from chaining two S&H circuits. A load signal is output from the ADC when a conversion is complete to assist in the multiplexing function.

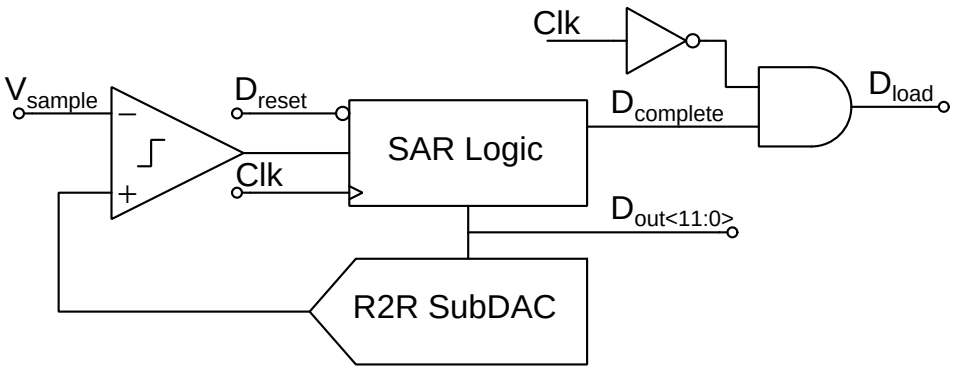


FIGURE 5.17. SAR ADC Schematic

The sub-DAC, and therefore the ADC, has a full scale voltage of -900 mV and, at first glance, operates in an inverse manner. The output of the DAC decreases as the digital input increases. e.g. An input of all 0's produces an output of 0 V, while an input of all 1's produces an ouput of -900 mV. However if one were to take the absolute value of the output the DAC it would operate as any other. The DAC operates in such a manner to match the rest of the system which operates on negatively swinging signals. The schematic for the DAC is shown in Figure 5.18. Key performance and design parameters are given in Table 5.8.

The ADC has an input range of 0 to -900 mV and operates of the system clock of 200 kHz. The SAR has a conversion latency of 13 cycles for an sampling rate of 15.384 kHz. The effective rate is reduced by a factor of 2 to 7.692 kHz due to the input multiplexing. Although slow, this sampling rate is more than sufficient as the input to the ADC is effectively a DC signal. For its

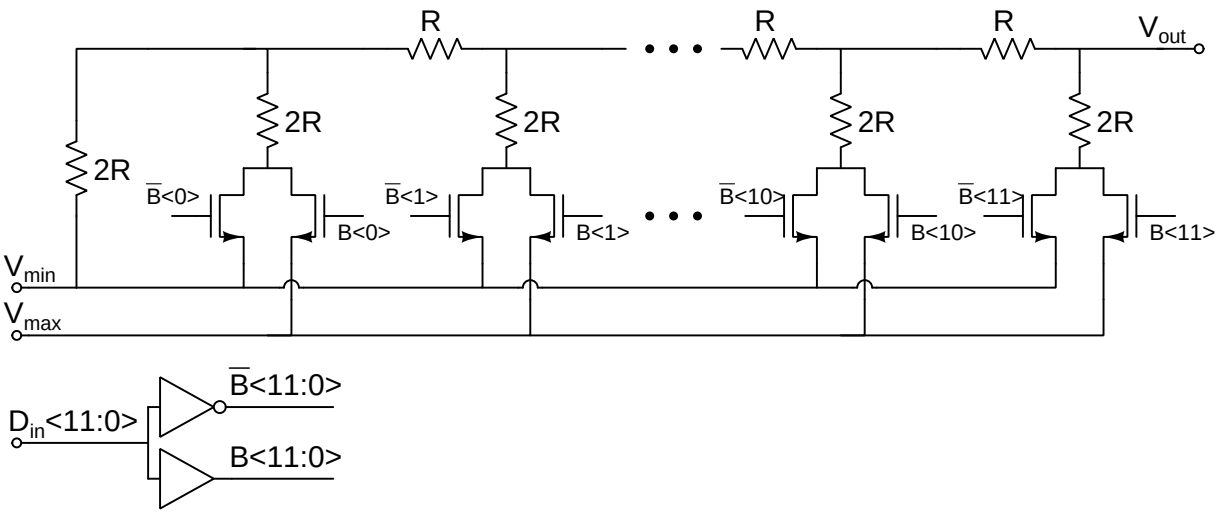


FIGURE 5.18. R2R DAC Schematic

TABLE 5.8. DAC Parameters

Paramter	Value
FET Size	60/.18 µm
R	50 kΩ
V_{min}	0 V
V_{max}	-.9 V
DNL_{max}	.11 LSB
INL_{max}	.54 LSB

expected input range of 50 mV to 850 mV the ADC has a SINAD of 69.32 dB for an ENOB of 11.23 bits. The output spectrum for a 1.022 kHz input can be see in Figure 5.19.

The digital resistors are created from a series of switched binary weighted resistors. The value of each digital resistor is given by $R = (N + 1)R_{base}$ where N is the decimal value of the digital control code. A schematic of a digital resistor is shown in Figure 5.20. The base resistor size

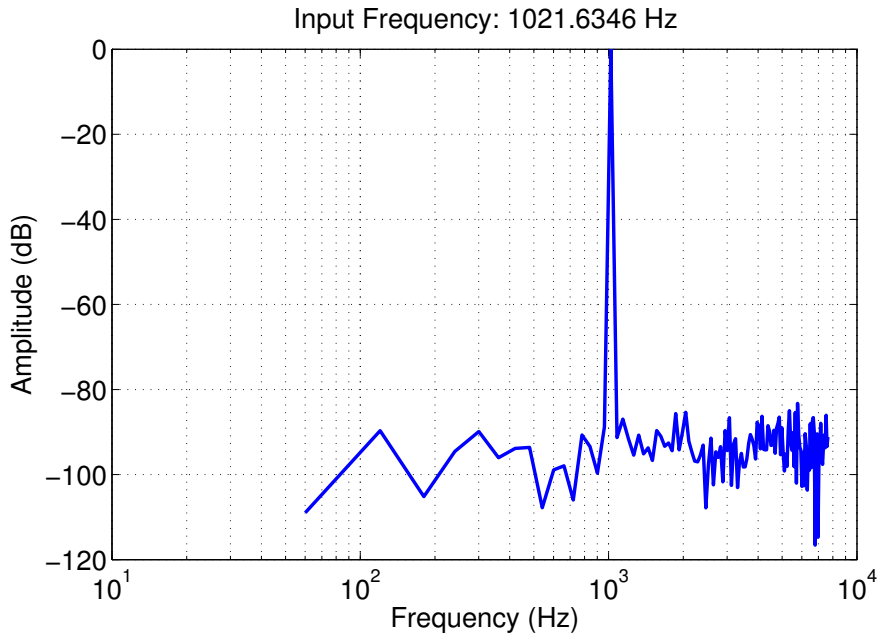


FIGURE 5.19. 12-bit SAR ADC 256-point FFT (50 mV to 850 mV)

was selected to be 2.5 kΩ and switches were implemented as CMOS switches with dimensions of 12/.18 µm. The max DNL of the digital resistors was calculated from simulation to be .24 LSB.

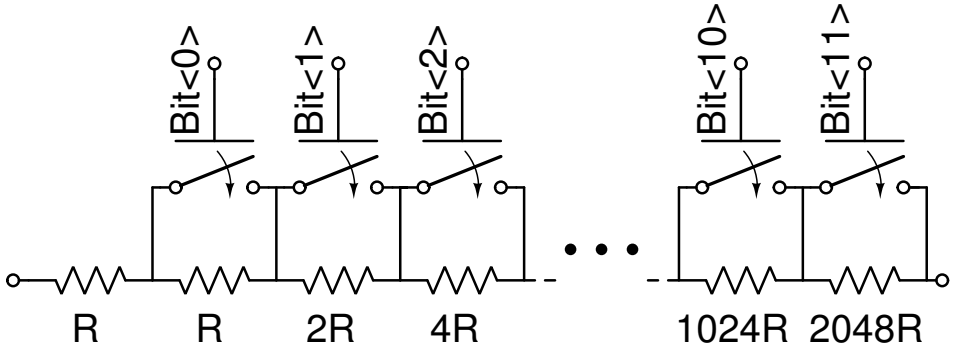


FIGURE 5.20. 12-bit Digital Resistor

Simulations of the mixed-signal divider were performed to characterize its error. As simulated the dividend was held at a constant voltage of 425 mV, while the divisor was stepped from 50 mV to 850 mV in 12.5 mV steps. This mimics the expected operation of the divider within the entire sensor system. The quotient was taken from the output of the divider and compared to the ideal value. Figure 5.21 shows the percentage error of the divider output vs. the input magnitude.

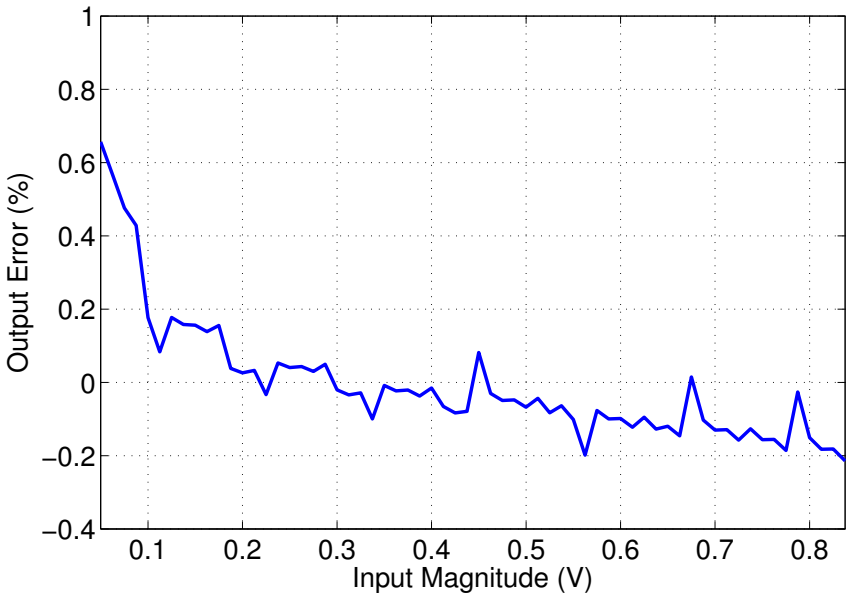


FIGURE 5.21. Mixed-Signal Divider Error vs. Input Magnitude

5.2.5. Phase Module

As designed the phase module utilizes the previously discussed 12-bit R2R DAC and a counter clock of 10 MHz. With a clock period of 100 ns and a test period of 400 µs (2.5 kHz), a phase resolution of .09° is achieved. The Verilog code for implementing the phase module is located in Appendix B. The resolution of the phase module decreases as the test frequency increases unless the counter clock is correspondingly increased. As designed the phase counter has a width of 12 bits which gives it a maximum value of 4096. If the counter reaches the maximum value the output is reset and the counter stops operating. This creates one major limitation for phase measurement, given a fixed counter clock, there exists a lower bound of frequencies that can be successfully tested. The maximum test period is given by equation 5.1, assuming a maximum shift of $90°$. As designed the phase module cannot properly measure test periods above 1,638.4 µs (test frequencies below 610 Hz).

(5.1) $$T_{per} \leq 4 \times 4096 \times T_{clk}$$

Phase is calculated from the DAC output according to the equations in 5.2.

$$N_{counter} = 4096 \times \frac{|V_{phase}|}{.9}$$
$$\theta^{\circ} = \frac{N_{counter} \times T_{clk}}{T_{per}} \times 360^{\circ} \tag{5.2}$$

Figure 5.22 shows the key phase module signals for a series RC combination of 6 kΩ and 10 nF at a test frequency of 2.5 kHz. A phase shift of approximately 48.6° is expected. An output of 117.84 mV was measured which corresponds to a calculated phase shift of 48.2°, an error of less than 1 %.

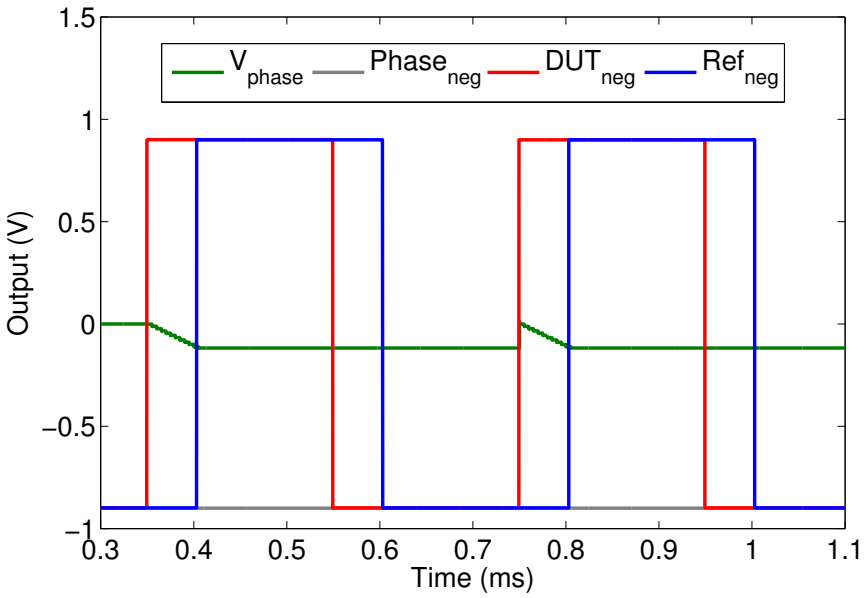


FIGURE 5.22. Phase Module Signals

5.2.6. Full System

The full impedance sensor was simulated to verify its operation and performance. The system parameters were chosen so that it has a detection resolution of at least .44 %, with an accuracy error no more than 10 %. A simulation at 2.5 kHz, with a resistive DUT of 58 kΩ was performed to demonstrate sensor. The system outputs are shown in Figure 5.23. Divider input voltage was

set at 100 mV, and an output of -332 mV was measured after simulation. This gives a ratio of 3.32 between the DUT and reference impedance. The front-end was operating at a gain code of 2 for a reference impedance of 17.36 kΩ, thus the DUT impedance was measured to be 57.6 kΩ. Average power during the 1.6 ms simulation was calculated to be approximately 780 µW.

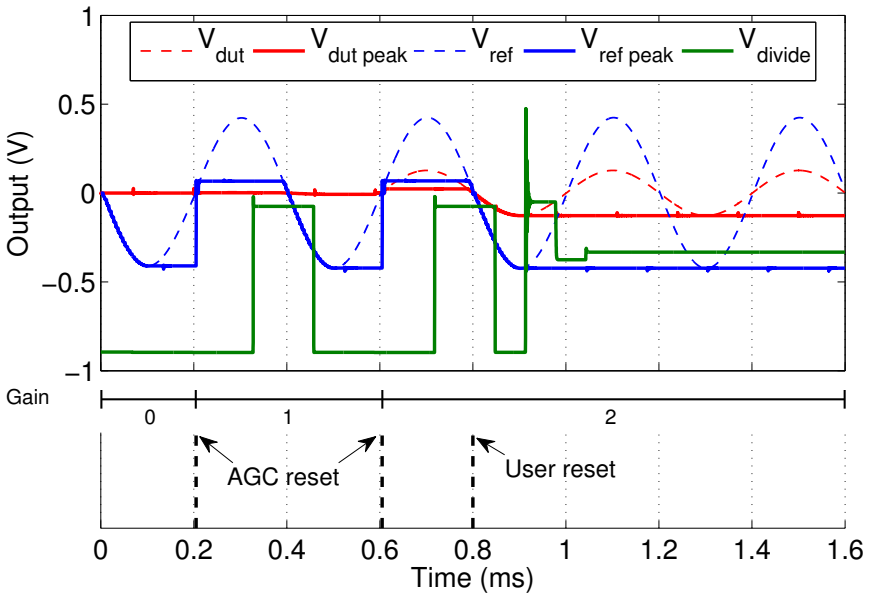


FIGURE 5.23. Impedance Sensor Simulation

Simulations to test the system accuracy and resolution were performed. the Figure 5.24 shows the measured impedance error for the defined input impedance range, at the output of the divider and as calculated from the input to the divider.

System precision was verified by simulating a DUT impedance in 2 Ω increments around a 1.02 kΩ base impedance, demonstrating a resolution better than .44 %. The pre-divider and post-divider results are shown in Figure 5.25.

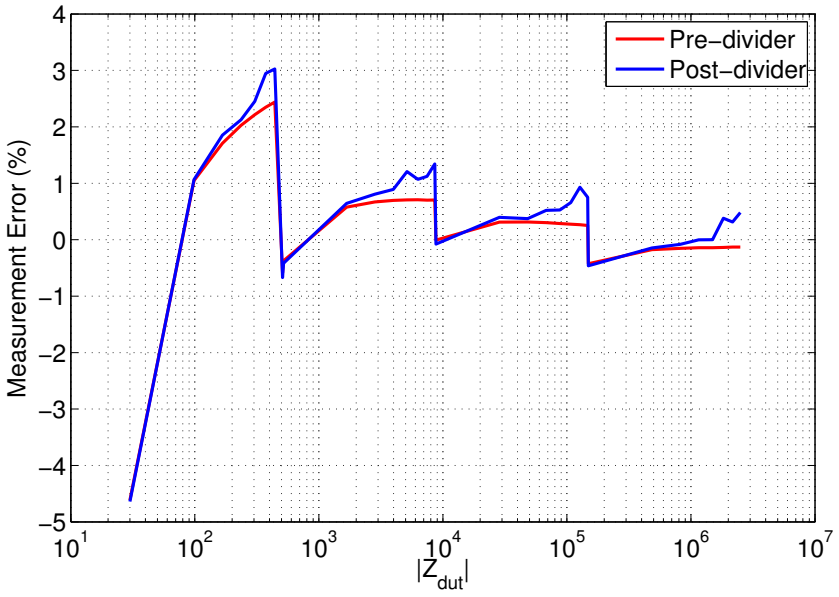


FIGURE 5.24. System Accuracy vs. Input Impedance

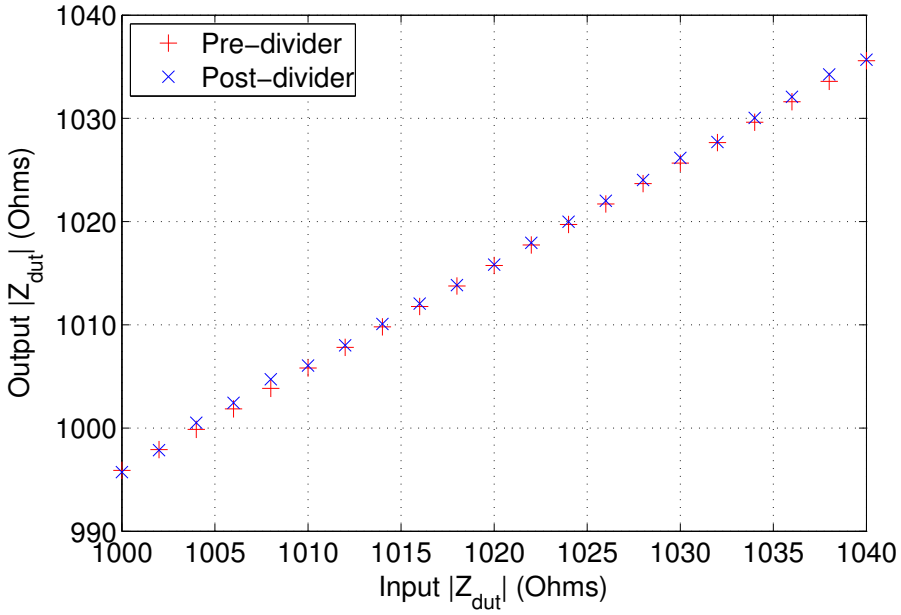


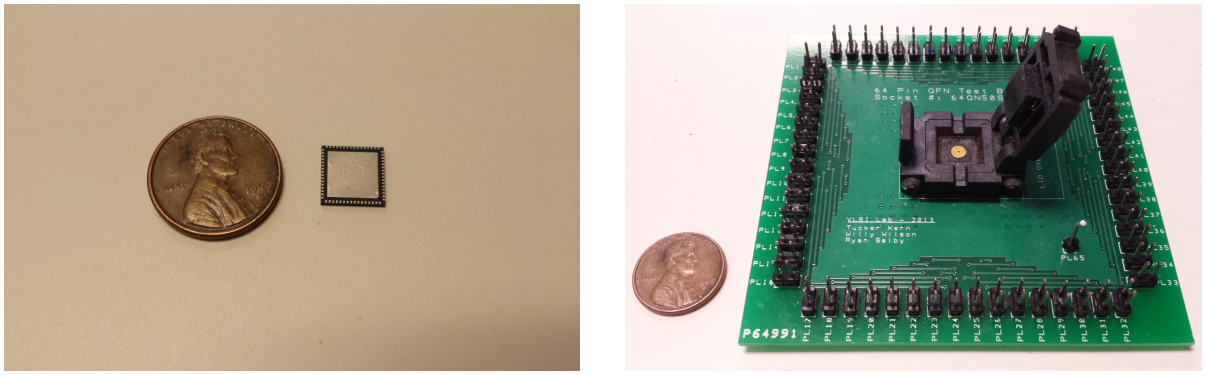
FIGURE 5.25. System Resolution

Chapter 6
Silicon Implementation & Verification

Pertinant information about the silicon implementation of the proposed sensor systems is discussed in this chapter. Experimental verification of the sensors is silicon was also performed.

Both sensor systems were implemented in a Texas Instrument .180 µm 1.8 V CMOS process. The process provided thin film resistors which exhibit good linearity and mismatch characteristics compared to poly and diffusion resistors. Various capacitor technologies were also available, including metal comb and double-poly capacitors, both which have good linearity and low leakage.

The circuits were fabricated on a shared die with other unrelated test circuits and packaged in a 64-pin QFN package. The circuits were tested using a Plastronics QFN Clamshell socket on a custom PCB breakout board. Pictures of the package and test board are shown in Figure 6.1.



(A) 64-pin QFN Package (Dead-bug) (B) Socket installed on breakout board

FIGURE 6.1. Package & Socket Photos

6.1. Capactive Sensor

6.1.1. Implementation

Implementation of the capacitive sensor is relatively straightforward. No significant matching requirements exists beyond typical common-centroid matching methods applied within the op-amps.

The divider capacitors, C_1 & C_2, were implemented as double-poly capacitors, while the smaller switched capacitors, $C_{3\text{-}5}$, were implemented at metal comb capacitors. Layout of the test capacitors was done in a manner that reduced additional parasitics from appearing due to nearby traces. A labeled picture of the layout is shown in Figure 6.2. Two additional op-amps exist in the layout for buffering internal nodes for inspection, these were not labeled. The total circuit area is approximately 180 µm x 80 µm.

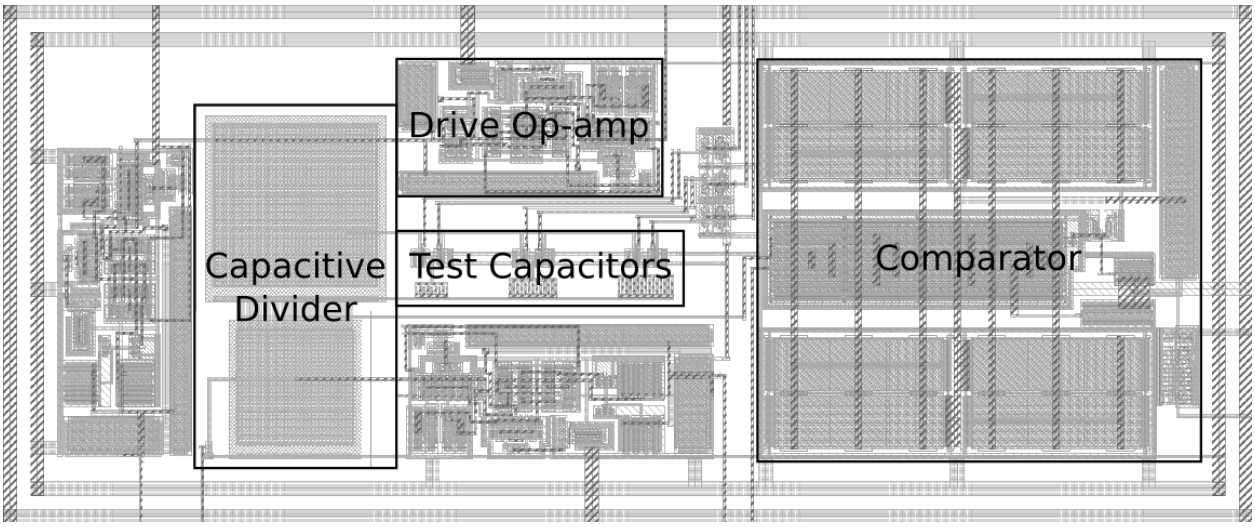


FIGURE 6.2. Layout of Prototype Capacitive Sensor

6.1.2. Silicon Verification

Verification of the sensor prototype was achieved using standard laboratory equipment. A 200 MHz digital oscilloscope was used to measure the pulse width from the comparator. A scope

capture of the baseline response is shown in Figure 6.3, where green is V_{ramp}, blue is V_{test}, purple is D_{pulse}, and yellow is the buffered divider output. V_{test} was reduced from the simulation value of 650 mV to 560 mV so that the base pulse width in silicon similar to the simulation value. The need to reduce V_{test} most likely is a result of the divider output staying at 0 V for part of the test period.

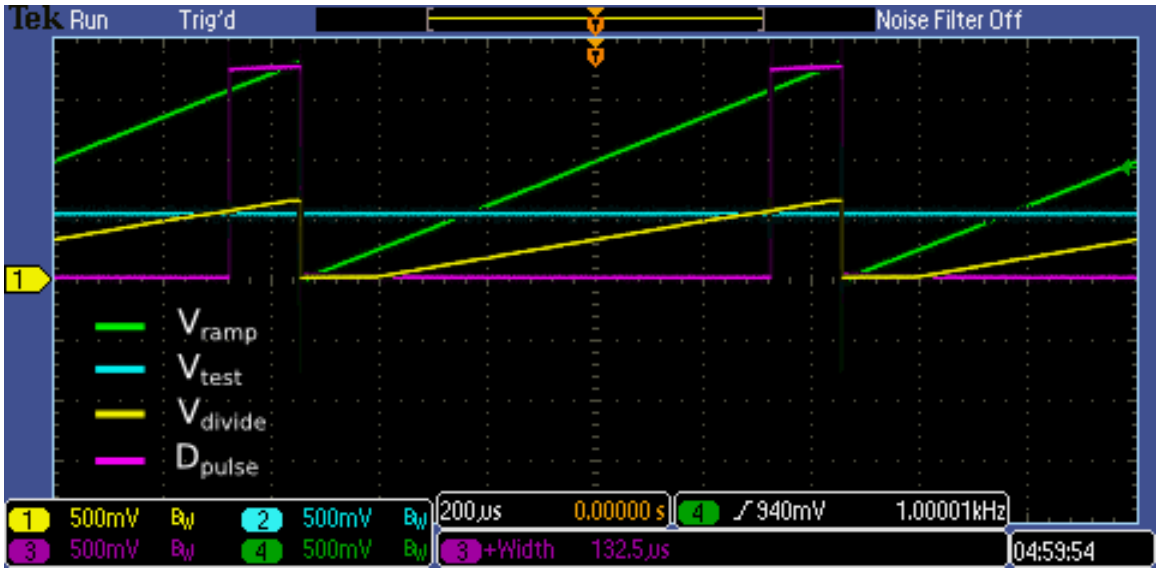


FIGURE 6.3. Capacitive Sensor Response - Baseline Silicon

Each capacitive step was tested to compare the actual and simulated sensor response. Figure 6.4 shows another scope capture of the sensor with the +5fF step enabled. The rest of the test states are given in Table 6.1 along with comparisons to the simulated values. A variation of approximately .3 µs was observed in the pulse width values. Like the simulated sensor, the actual prototype has a non-uniform response. Characterization of the sensor response between multiple chips was not performed.

FIGURE 6.4. Capacitive Sensor Response - +5fF Silicon

TABLE 6.1. Capacitive Sensor Pulse Widths - Silicon

ΔC_1	Measured T_{pulse}	Simulated T_{pulse}	Measured ΔT_{pulse}	Simulated ΔT_{pulse}
+0 fF	132.5 µs	134.2 µs	0 µs	0 µs
+5 fF	137.0 µs	140.5 µs	4.5 µs	6.2 µs
+10 fF	141.7 µs	145.9 µs	4.7 µs	5.4 µs
+15 fF	147.4 µs	150.7 µs	5.7 µs	4.7 µs
+20 fF	151.7 µs	156.6 µs	4.3 µs	5.9 µs
+25 fF	156.6 µs	161.8 µs	4.9 µs	5.1 µs
+30 fF	160.1 µs	167.6 µs	3.5 µs	5.7 µs

6.2. Impedance Sensor

6.2.1. Matching Considerations

Compared to the capacitive sensor the impedance sensor has significant matching considerations that must be addressed. As the sensor topology is more susceptible to device and component

mismatch care must be taken in its design. As parts of sensor depends on absolute voltage values, any variation in these values due to offset or mismatch degrade the accuracy of the measurement. This mismatch could be compensated for with calibration coefficients, although this is not ideal. The main system components in the sensor that are highly susceptible to mismatch are the front-end gain resistors, the mixed-signal digital resistors, and the R2R DACs within the ADC and phase module.

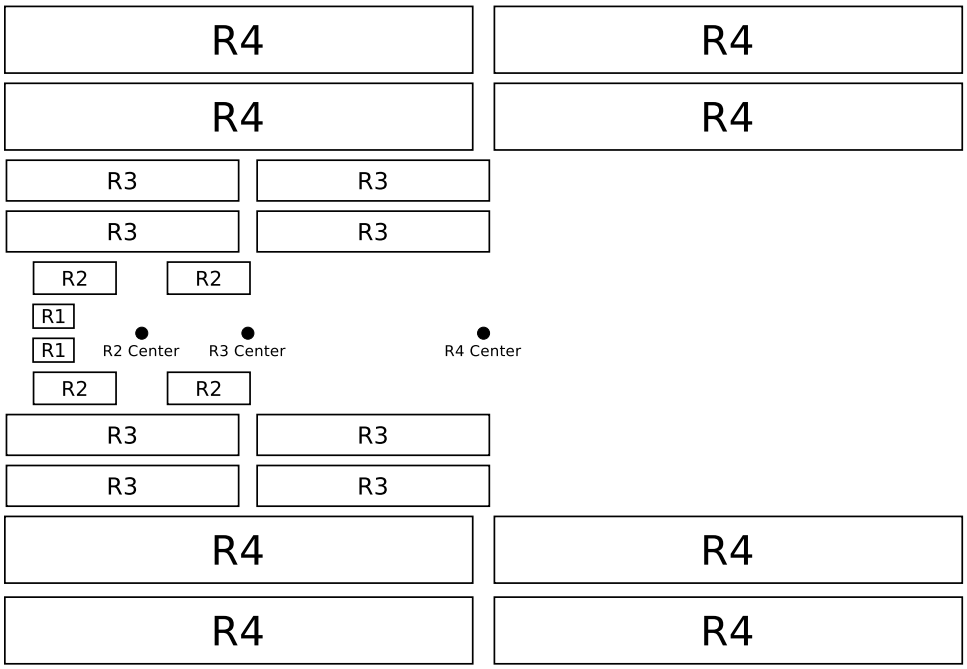


FIGURE 6.5. Gain Resistor Matching Pattern

Recall from Chapter 2 that the dual bridge measurement approach assumes the two signal path are identical, any variation between the two results in a measurement error. Specifically, as shown in equation 2.3, the matching of the feedback resistances is extremely important. To facilitate matching the two gain resistors were implemented within a single block, and large resistances were segmented to allow for common-centroid placement. The smallest resistance in each resistor, R1, was not matched in a common-centroid fashion because the device was too small to split. Each resistance was matched to its corresponding twin, but no matching within a single digital resistor

was performed and this would have no effect on system accuracy. A diagram of the matching arrangement is given in Figure 6.5. Scale in the diagram was altered for readability. The large space on the right-hand side housed the switches and routing for the resistors. The centers of each common-centroid arrangement are marked with a dot and labeled.

Matching of the resistors within the R2R DAC is also important to ensure accurate operation of both the mixed-signal divider and phase module. Resistor matching on the DAC composed mainly of interleaving the R and 2R resistors as shown in Figure 6.6. This provides a reasonable match within each bit of the DAC but does not provide any circuit wide matching.

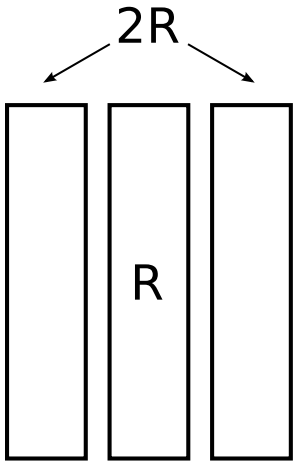


FIGURE 6.6. R2R Interleaving

Interleaving the bit resistors in such a manner made implementing a chain trivial. In an attempt to reduce the severity of process gradients on the DAC the most significant bits were folded back and interleaved between the least significant bits in the bit string. To clarify, a regular bit string would be represented as follows:

$$B_0 B_1 B_2 B_3 \cdots B_{10} B_{11}$$

while the folded bit string would have the following pattern:

$$B_0 B_{11} B_1 B_{10} \cdots B_5 B_6$$

For a reduced dependence on calibration a true matching scheme in the DAC would be beneficial.

As the mixed-signal divider operates on the concept of a ratio between two resistances the digital resistors would benefit greatly from significant matching. A matching scheme similar to the one used in the digital gain resistors would be a good candidate for an attempt at matching. Regrettably at time of writing no matching between the divider resistors was performed.

6.2.2. Implementation

At the time of writing two version of the impedance sensor exist. A prototype with reduced functionality was implemented and fabricated. The prototype sensor is composed of the front-end without an AGC, the peak capture systems, and the mixed-signal divider. Preliminary silicon results are available for this prototype which allows some components of the sensor to be verified. All resistors were implemented as thin film resistors for their superior performance. Sampling capacitors in the peak capture systems were double-poly for their linearity. Standard matching techniques were utilized to minimize offset in the comparators and op-amps. A picture of the prototype layout is shown in Figure 6.7, with major components labeled. The prototype circuit area is approximately 540 µm x 320 µm. A die photo of the implemented impedance sensor in silicon is shown in Figure 6.8.

Implementation of the full system will require the addition of 4 comparators, the AGC control logic and digital resistors, the phase module logic, DAC and output buffer. The approximate dimensions or area of each component is given in Table 6.2. The estimated area needed to implemented the additional circuit components, assuming a 50 % margin for routing, is .11 mm^2.

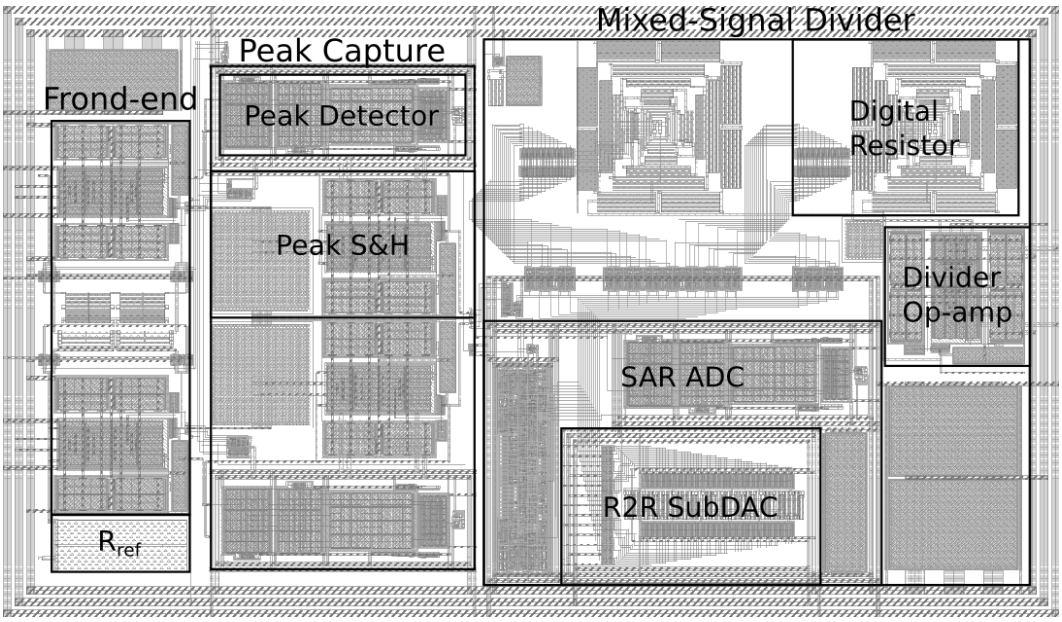


FIGURE 6.7. Layout of Prototype Impedance Sensor

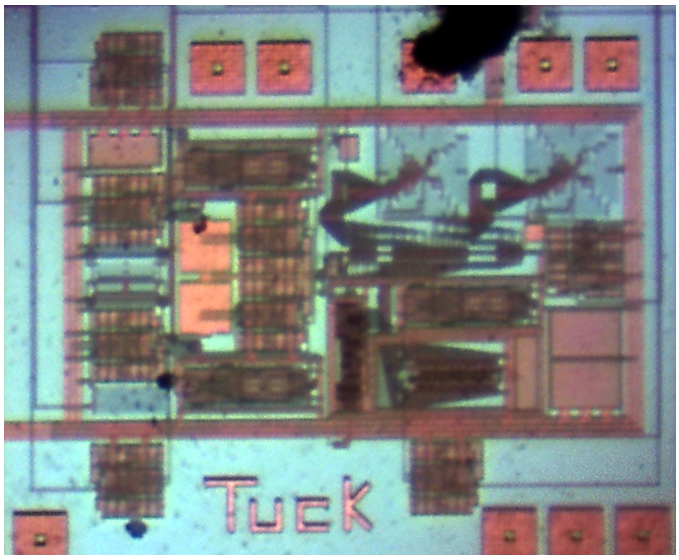
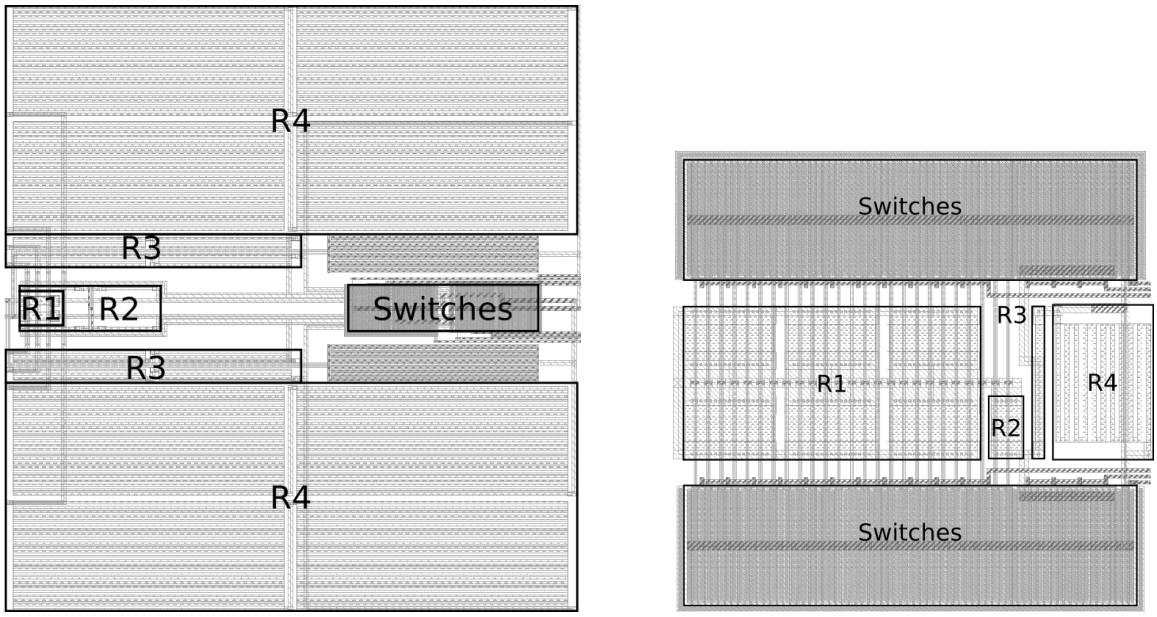


FIGURE 6.8. Impedance Sensor Die Photo

This corresponds to a 65 % increase in circuit area over the prototype for an estimated total circuit area of .28 mm^2, or approximately 690 µm x 410 µm if the aspect ratio of the prototype circuit is maintained. Figure 6.9a and 6.9b show the digital gain and reference resistor layouts, respectively. The other layout are all visible within the prototype layout in Figure 6.7.

TABLE 6.2. Dimensions of Additional Circuit Components for Impedance Sensor

Component	Dimension/Area
AGC Logic	(est.) 1,523 μm^2
Phase Module Logic	(est.) 2,145 μm^2
Comparator (each)	140 µm x 55 µm
DAC	135 µm x 80 µm
Buffer	70 µm x 70 µm
R_{gain} (joint)	140 µm x 130 µm
R_{ref}	50 µm x 50 µm



(A) Gain Resistors (B) Reference Resistor

FIGURE 6.9. Digital Resistor Layouts

6.2.3. Silicon Verification

Verification of the prototype impedance sensor was accomplished with standard laboratory equipment. The prototype sensor had two manually select-able gain resistances, 100 kΩ & 700

kΩ, and a reference resistance of 10 kΩ. On the low gain setting, a reference output of 100 mV is expected, and a testable impedance range of 1.2 kΩ to 20 kΩ is achieved assuming the 50 mV to 850 mV output window. On high, the reference bridge output of 700 mV is expected and an DUT range of 8.2 kΩ to 140 kΩ is supported.

The prototype allowed for the ADC to be shut down by holding its reset signal low indefinitely. Initial experiments on the front-end and peak capture systems were performed with the ADC shut off in an attempt to reduce noise in the measurements. Later it was determined that enabling the ADC corrupted an output of the peak capture system and therefore one of its own inputs. Regardless limited verification of the operation of the front-end, peak capture and mixed-signal divider was possible.

As stated the ADC was shut down to perform initial verification of the front-end and peak capture systems. Outputs of the peak capture system were buffered and made available externally so that the circuits could be verified semi-independently from the rest of the sensor. The high gain setting was used and input impedance of 10 kΩ, 15 kΩ, 30 kΩ & 40 kΩ were tested. Additionally an RC combination of 40 kΩ and 2.2 nF was tested in a parallel and series format to visualize the phase shift at the output of the peak capture.

A screen capture in Figure 6.10 shows the operation of both peak capture circuits. The screen cap in Figure 6.11 shows the measured peaks for a 15 kΩ DUT right before a reset is performed, the slewing is from the output buffer and not the actual circuit. The measured peaks, and calculated DUT value for all the tested impedance are summarized in Table 6.3.

From the data a few things can be determined. Foremost the measured reference peak is 70 mV off from the expected value, although it appears the cause of this change is similarly affecting the DUT bridge thus accuracy isn't severely degraded. There appears to be a mild positive correlation between the DUT impedance and measured reference output. This may be

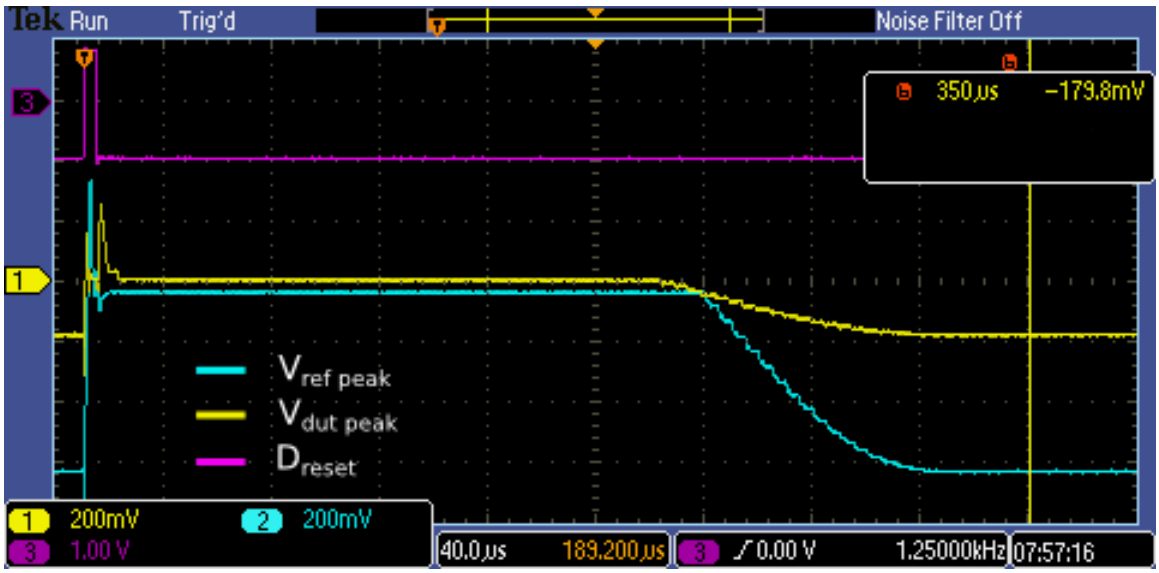


FIGURE 6.10. Peak Capture Outputs - Silicon

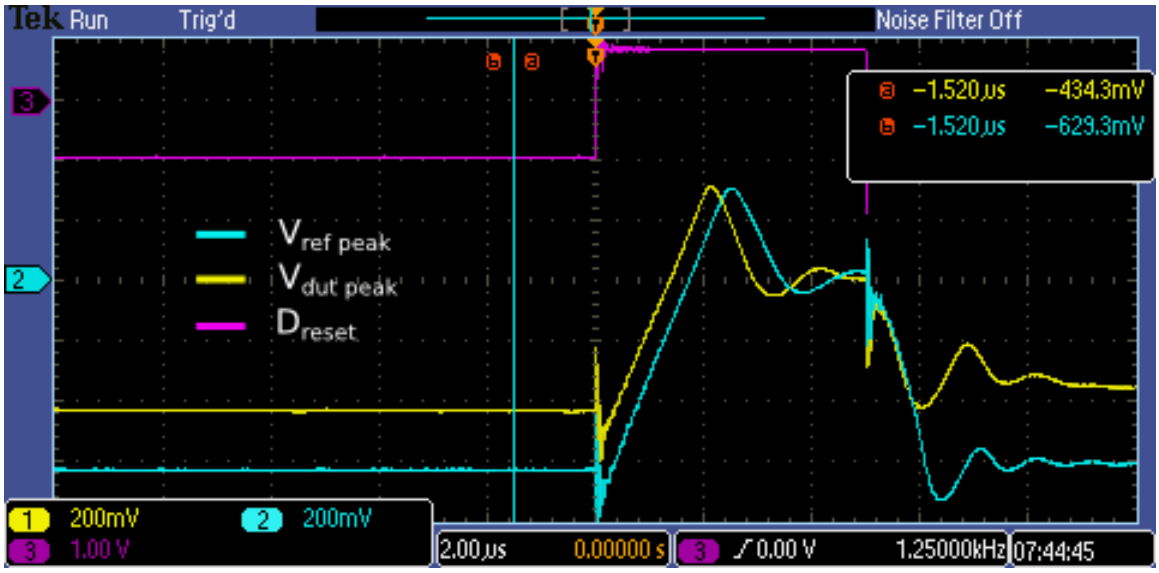


FIGURE 6.11. 15 kΩ DUT Peak Capture Values - Silicon

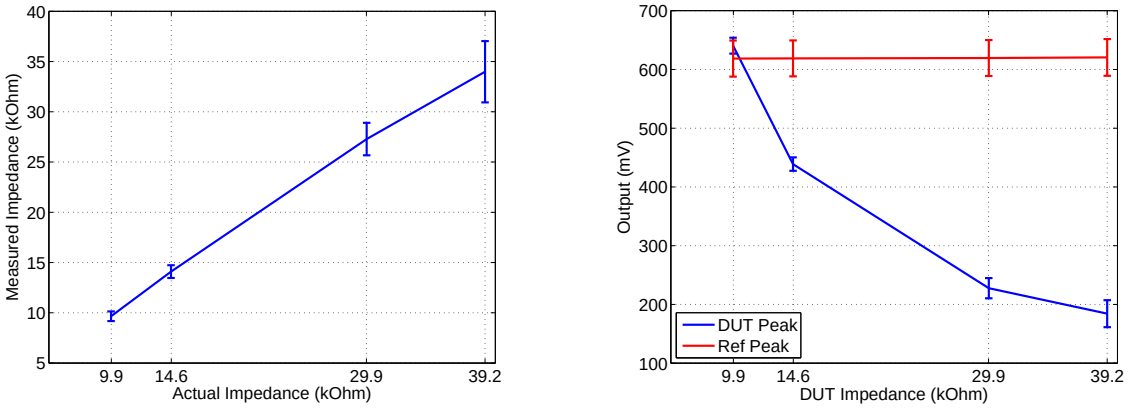
the result of coupling within the circuit, or an interaction at the source of the excitation signal which is shared between the two bridges. For the tested impedance values the peak capture system is within the target goal of no more than 10 % error, although the error grew significantly at large impedance.

Multiple chips were sampled to determine the chip to chip variation in the sensor. Figure 6.12a shows the mean calculated DUT values with error for the 4 DUTs accross 10 randomly selected

TABLE 6.3. Measured DUT Peaks & Calculated DUT Values

DUT	$V_{ref\ peak}$	$V_{dut\ peak}$	Calculated Ratio	Calculated DUT	Error
9.88 kΩ	627 mV	635 mV	0.98	9.8 kΩ	0.8 %
14.58 kΩ	629 mV	434 mV	1.45	14.5 kΩ	0.5 %
29.92 kΩ	631 mV	217 mV	2.91	29.1 kΩ	2.8 %
39.20 kΩ	633 mV	175 mV	3.62	36.2 kΩ	8.3 %

chips. The measured peak values from the same 10 chips are plotted in Figure 6.12b. From the figures two key things can be determined, the measured variation increases greatly as the DUT impedance increases and there is significant variation in the measured reference peak. The increasing variation at higher impedance is most likely due to poor performance of the peak capture system, either due to offset or noise, both which have a greater realtive effect when the front-end output is smaller. The variation among the reference peak most likely indicates that the on-chip reference impedance is of relatively poor tolerance, an external reference resistor, or laser-trimmed resistor could rememdy this.



(A) Measured DUT (10 samples) (B) Peak Values (10 samples)

FIGURE 6.12. Impedance Sensor Chip to Chip Variation

The prototype sensor did not implement the phase module, but the concept behind it can be easily verified by comparing the outputs of the peak capture system when a reactive DUT is tested. The peak capture outputs to a 40 kΩ resistor are shown in Figure 6.13, note how both peak capture outputs reach their maximum value approximately at the same time. A 2.2 nF capacitor was then inserted in parallel with the resistor. The outputs of this RC combination are shown in Figure 6.14, note how the yellow DUT output reaches its peak values significantly before the blue reference output, indicating a leading current through the DUT.

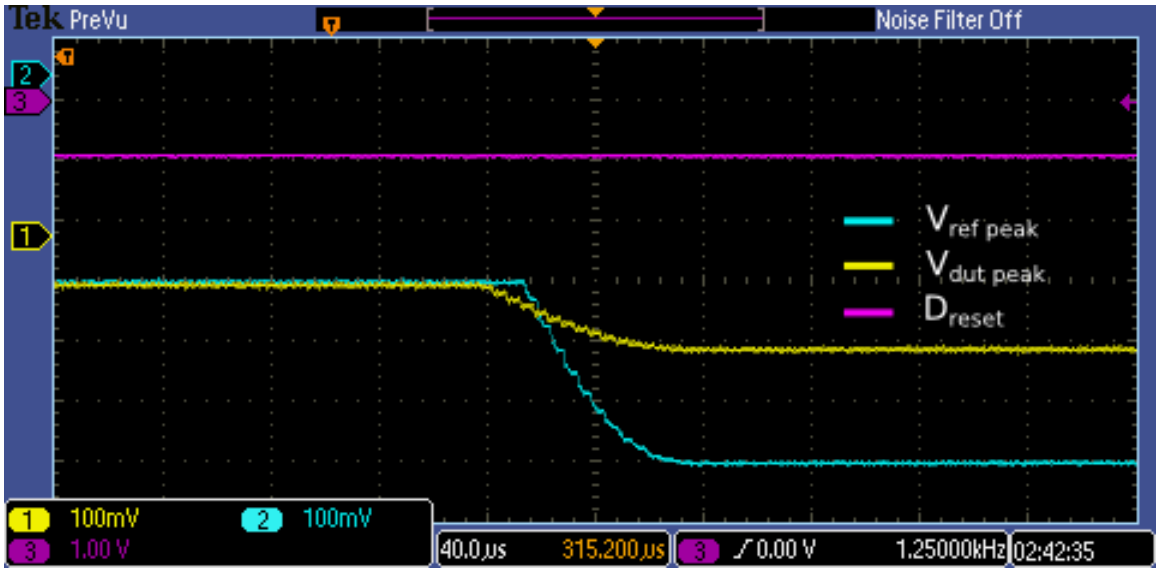


FIGURE 6.13. Resistive DUT Peak Outputs - Silicon

For unknown reasons, enabling the ADC corrupts one of the peak capture circuits. Fortunately despite the corruption the affected output can still be varied to some degree and verification of the mixed-signal divider is still possible. An analysis of possible reasons why the ADC corrupts the peak capture circuit is discussed in Chapter 7. Once enabled the ADC's sub-DAC output is available for viewing via an additional signal buffer. This allowed verification that the SAR logic, DAC and input multiplexing are all properly functioning. The DAC output (green) can be seen in Figure 6.15 alternately tracking the two inputs. The purple signal is the ADC's conversion complete signal.

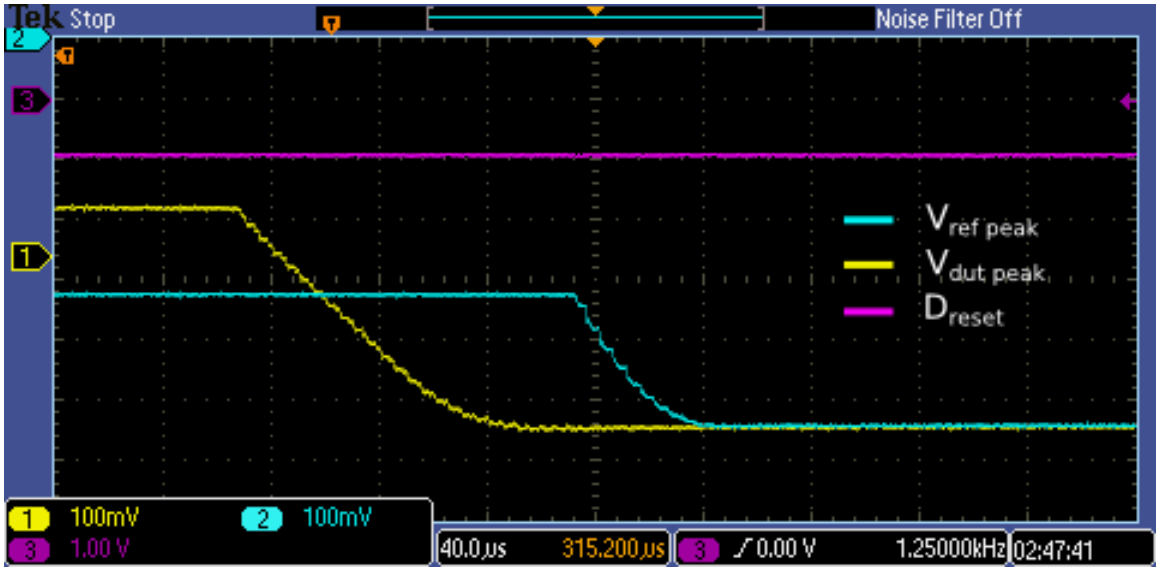


FIGURE 6.14. RC DUT Peak Outputs - Silicon

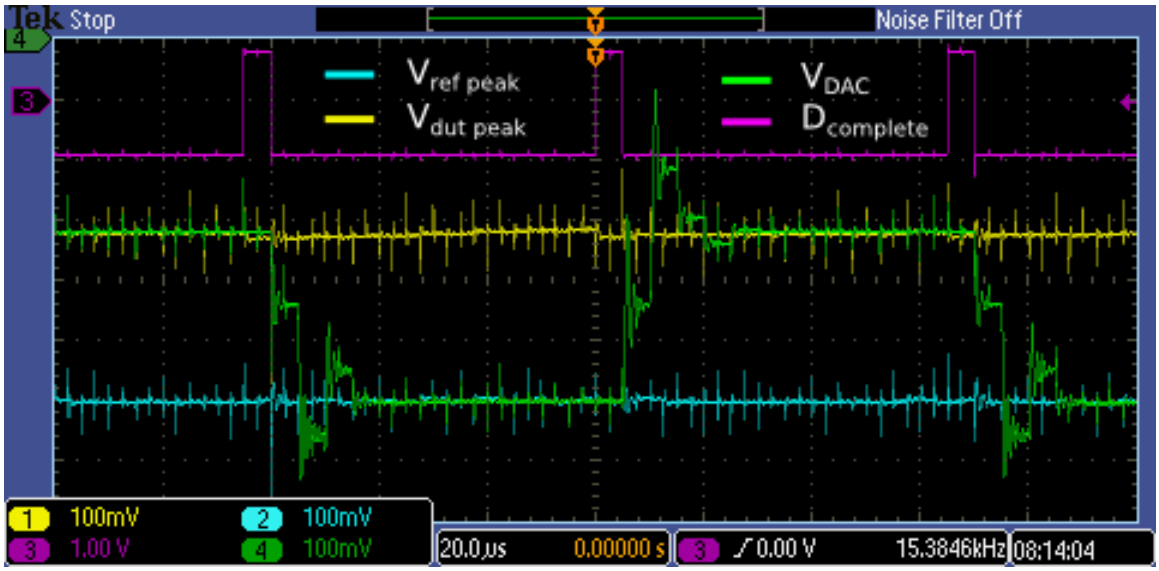


FIGURE 6.15. ADC SubDAC Operating - Silicon

Verifying operation of the mixed-signal divider was accomplished by testing two different DUTs. The first, outputs shown in Figure 6.16, a resistive DUT of 15 kΩ and the second, outputs shown in Figure 6.17, a series combination of a 15 kΩ resistor and 2.2 nF capacitor. Output of the mixed-signal divider is green, the DUT peak is yellow and reference peak is in blue. The corruption of the DUT peak capture circuit can be witnessed in Figure 6.16. The two outputs

are nearly identical but the DUT is 1.5 times the value of the reference impedance of 10 kΩ. A summary of the values measured is given in Table 6.4.

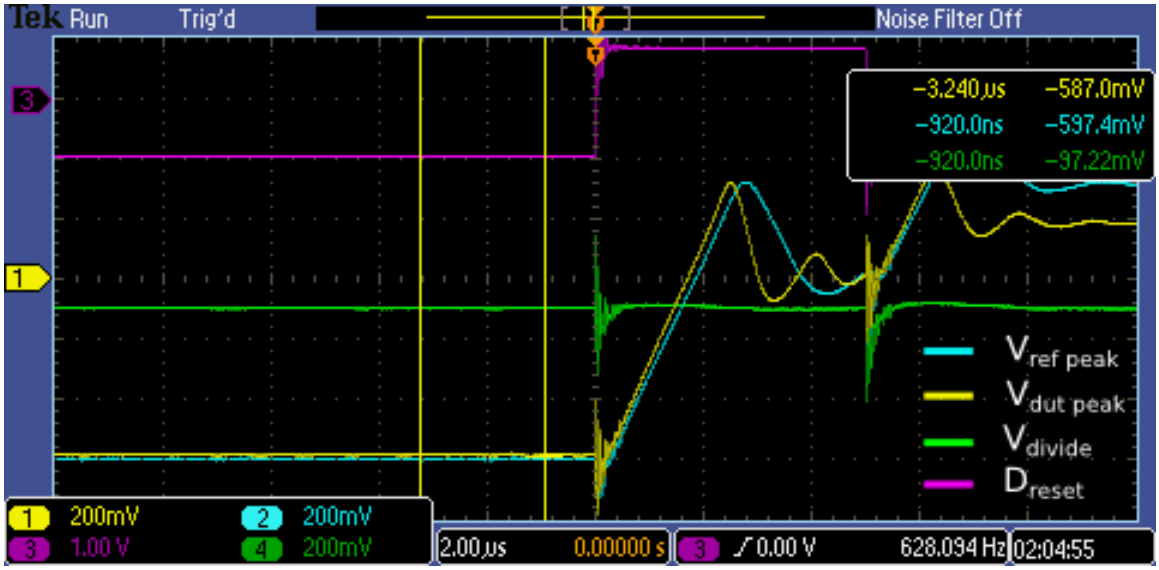


FIGURE 6.16. Divider Output 15 kΩ DUT - Silicon

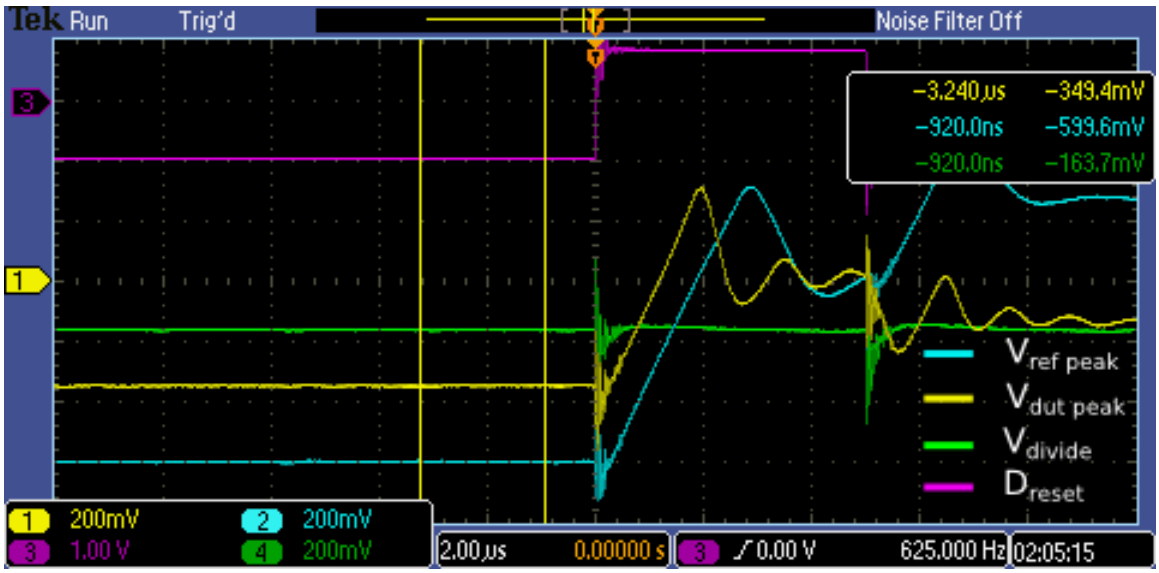


FIGURE 6.17. Divider Output RC DUT - Silicon

TABLE 6.4. Measured & Calculated Divider Values

DUT	$V_{ref\ peak}$	$V_{dut\ peak}$	Calculated Ratio	Measured Ratio	Error
15 kΩ	597 mV	587 mV	1.02	0.97	5.0 %
15 kΩ & 2.2 nF	600 mV	349 mV	1.72	1.64	4.9 %

Chapter 7
Discussion & Future Improvements

7.1. Capacitive Sensor

The proposed capacitive sensing topology, and its implemented prototype, were demonstrated to be a success although a clear disadvantage to the sensing topology is its non-linear response. A quadratic relationship between the test capacitance and the sensor sensitivity exists, as given in equation 4.6. A linear response is typically desirable for any sensing application. At best the sensor response can be estimated as linear for small displacements around a base capacitance. Another limitation of the topology is the necessity for C_2 to be similarly valued to the test capacitance. If the test capacitance is not known, or could vary orders of magnitude then a fixed C_2 can not be used and would most likely be implemented off chip.

The implemented prototype exhibited an unexpected response on the output of the divider. After each test period ended, the divider output node remains at zero for a portion of the new test period. This effect, shown in Figure 7.1, was not seen in simulations. The divider output is most likely not sitting at zero, but instead swinging below the rail which the signal buffer can not reproduce.

The cause of the negative divider output is not fully understood. Conservation of charge must be obeyed within the divider and can be used to show that the divider output should equal 0 V when the input voltage to the divider is 0 V. Any parasitics that appear on the divider also obey this law and should not cause the negative output voltage. According to charge conservation, for the negative output voltage to appear charge either has to be added to the test capacitance, removed from C_2 or the value of either capacitor must be changing. Although non-linear capacitors within

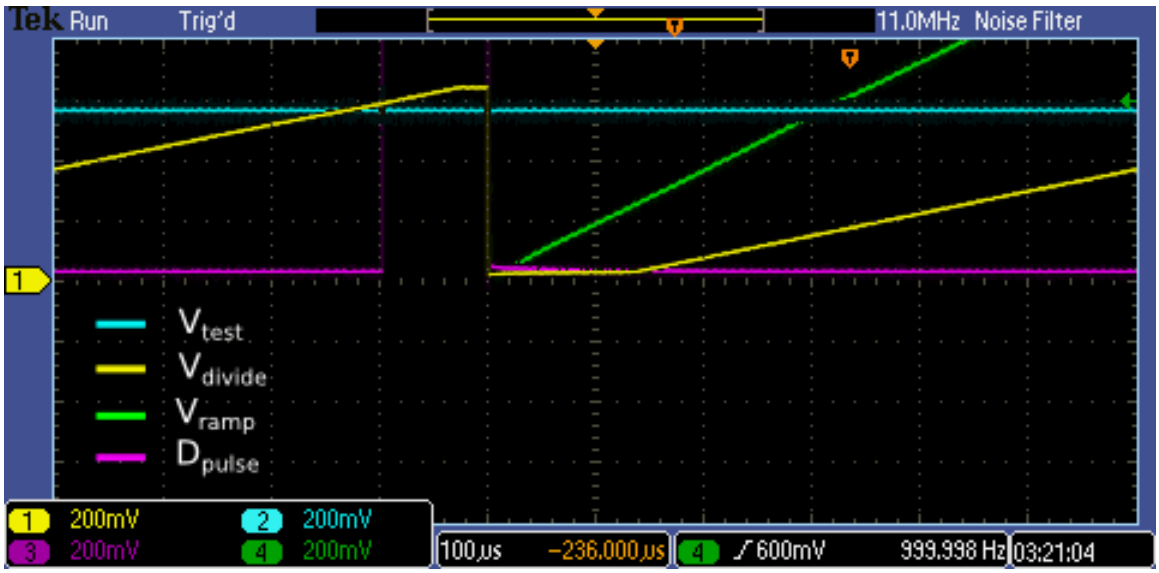


FIGURE 7.1. Negative Output in Silicon Capacitive Sensor

the FET switches could potentially be causing the divider capacitance to fluctuate the more likely cause is due to a loss of charge on C_2.

The loss of charge on C_2 could be a result of self-leakage within the capacitor or leakage from another device connected to the divider output. A simulation was performed with a much larger test period in order to exaggerate the effect of both leakage sources. Over an extended test period the self-leakage of the capacitors becomes more substantial and the current through the divider is reduced so that external leakage sources become more significant as well. The simulation was successful in demonstrating the unexpected behavior as seen in Figure 7.2.

It was determined that at such low speeds the leakage through the reset FET was significant enough to alter the output of the divider and cause the negative swing. This experiment implies that either leakage through the reset FET is significantly larger than modeled, the capacitor self-leakage is poorly modeled, or a large unknown source of leakage exists on the implemented sensor.

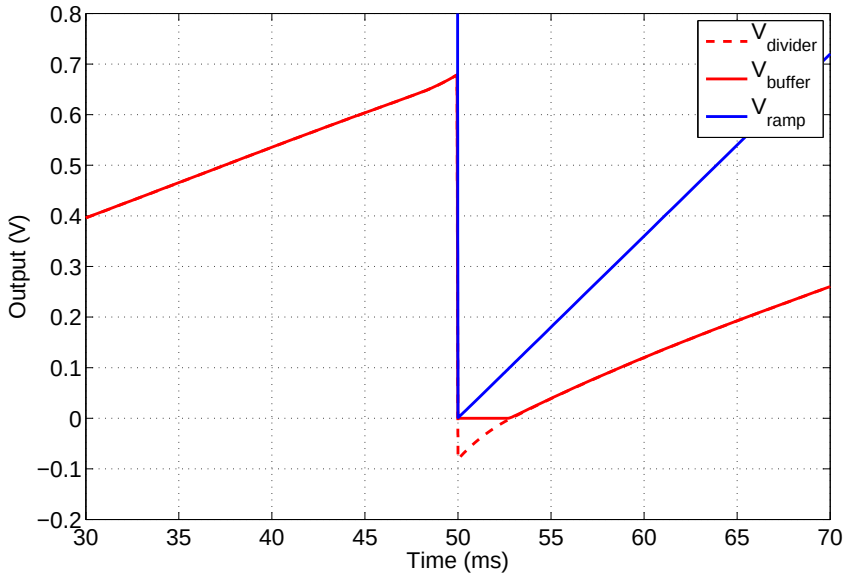


FIGURE 7.2. Negative Output Recreated in Simulation of Capacitive Sensor

7.2. Impedance Sensor

Although each subsystem in the implemented prototype impedance sensor was shown to be functional, and the entire system was shown to operate it can not be said the sensor was truly functional. The root of this problem stems from the corruption of a peak capture circuit when the ADC within the mixed-signal divider is activated. An analysis of the possible causes and their solutions is discussed.

The implemented prototype has a limited number of buffered internal nodes available for monitoring which makes troubleshooting difficult. The sampling nodes are available for viewing, but the input and gate signals are not. It was determined that only the DUT peak capture is corrupted when the ADC is activated, the reference system is not affected. The layout of the prototype sensor is shown in Figure 7.3 with subcircuits and nets possibly related to the corruption issue labeled. The ADC reset signal, in red, is driven by a Power-on Reset circuit which can be overridden manually. The remaining signal-color mappings are: blue - clock, green - S&H inputs, yellow - S&H outputs.

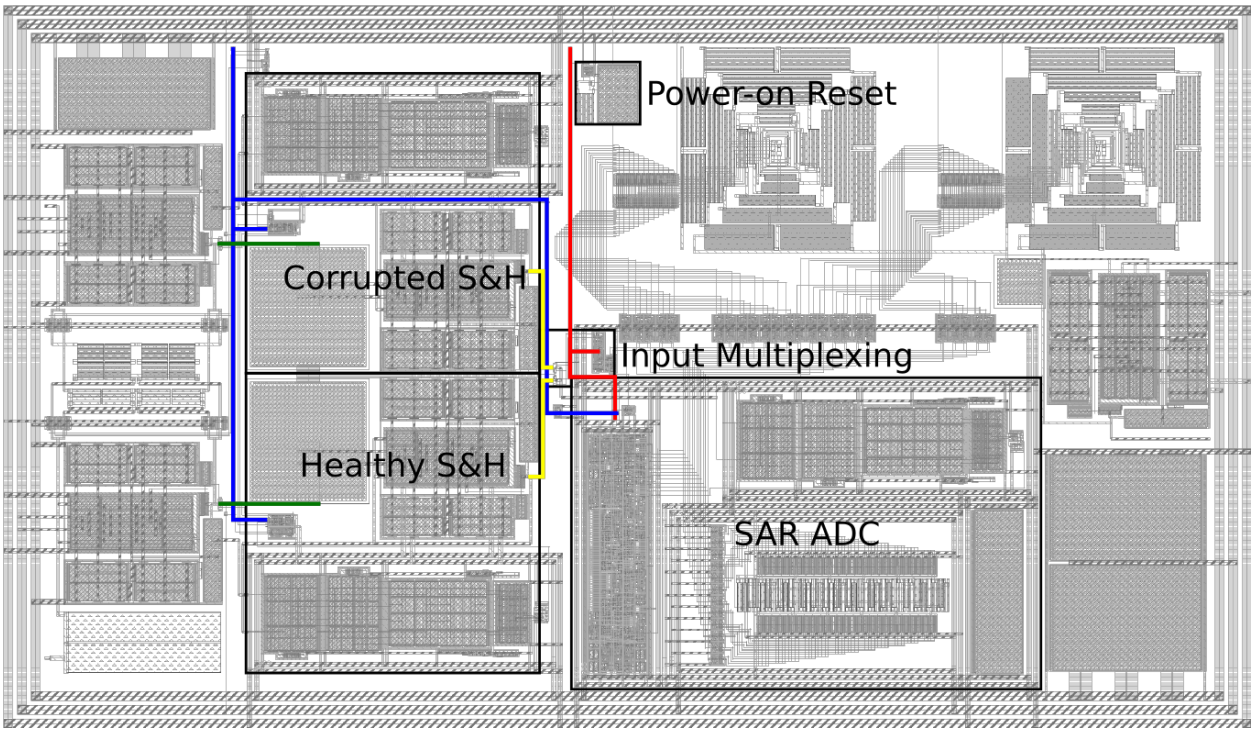


FIGURE 7.3. Prototype Impedance Sensor Layout with Possible Corruption Sources Labeled

Possible causes for the corruption are clock crosstalk, malfunctioning sample buffer, substrate noise from SAR, supply noise from SAR, and a front-end failure. Clock crosstalk, and a malfunctioning buffer can be easily be eliminated as probable causes of the corruption. The system clock runs regardless of the ADC reset signal thus the corruption would be apparent with or without the ADC running. Corruption of the sampling node is witness directly via an external signal buffer for off-chip inspection, thus a malfunction of the S&H signal buffer can be eliminated. Substrate noise from the SAR logic can also be eliminated from the list of probable causes as the healthy S&H circuit is actually closer to this logic. One would expected the nearby circuit to malfunction and not the more distant circuit. An oscillation in the front-end due to supply noise from the ADC could cause an invalid input to the peak capture circuit. This is most likely not the cause as the reference front-end would also be susceptible and the problem should not persist across every chip. The final, and most likely, cause of corruption is due to supply noise from the ADC

affecting the sampling of the DUT front-end. The ADC and DUT peak capture circuits share the same clock phase while, because the two peak capture systems operate on opposite clock phases, the reference peak capture would be unaffected. This would explain why the corruption only occurs on the DUT peak capture and not the reference circuit. Fixing this issue is as simple as moving the DUT peak capture to the alternate clock phase. There was not significant reasoning for operating the two peak capture systems on alternate clock phases.

7.2.1. Future Improvements

There are numerous possible improvements that could be made to the impedance sensor presented depending on the target usage and implementation priorities. An absolutely necessary improvement to the system is proper matching of the resistors within the mixed-signal divider and the R2R DAC. The core operation of both these circuits relies on accurate ratios between two resistors, thus proper matching should be a must. At the time of implementation there were more pressing time constraints and the accuracy loss was considered worthwhile in exchange for actually having the circuit implemented.

Improving the performance specification of the sensor is another route of improvement. Sensor resolution can be readily increased by adopting a higher resolution ADC and/or a more stringent front-end output window. Higher clock rates and test frequencies could be readily reached by increasing the op-amp and comparator bandwidth and thus power. Front-end error from the op-amps could be improved by offset correction, increased open-loop gain, and higher drive strength. The overall system could also benefit from a calibration scheme to compensate for variation in the reference impedance.

Improvements that would further the integration of the sensor system could be considered. Currently the system relies heavily on a number of signal from off-chip. On-chip sine wave generation and buffering would be necessary to eliminate external signal generators. While process invariant voltage references for deriving AGC test voltages and divider input could eliminate additional external sources. On-chip signal generation is not a terribly challenging process but achieving proper excitation would large buffers to supply the necessary currents into the DUT. Furthermore the effects of excitation non-linearity would need to be analyzed to determine the constraints on signal quality. Accurate voltage references are need to ensure the AGC transitions properly, significant variation in the test voltage could result in a failure of the AGC to select a proper gain code. While the value of the divider input is not important, knowing it exactly is important. Thus if an internally generated voltage is used for the divider input it should be available off-chip for measurement or extremely process insensitive.

Chapter 8
Conclusion

Presented in this thesis were two sensor systems for measuring the impedance of a device under test (DUT). Both sensor system could potentially be used as label-free affinity biosensor for biological applications. The first was a purely capacitive sensor that operated on the concept of a capacitive divider. The divider produces an output voltage that is dependent on a ratio between the test and a reference capacitance. This output voltage was then converted to a time-domain signal through the use of a comparator. The second, a general purpose impedance sensor, performed impedance measurement by calculating the ratio between the DUT and a reference impedance when excited by a sine wave signal. Measurement of the DUT and reference impedance was accomplished by two auto-balancing bridges operated in a dual-bridge configuration. Impedance magnitude is calculated through the use of a peak capture system and mixed-signal divider. While a phase module also computes the phase of the DUT. The system implemented an AGC for a wide range of testable DUTs.

Prototypes of each sensor were implemented in .18 µm CMOS and their operation was verified. The capacitive sensor achieved a detection resolution of at least 5 fF for a single sensor, and a simulated non-calibrated limit of detection of 10 fF between multiple sensors. The impedance sensing prototype demonstrated the functionality of the peak capture systems and mixed signal-divider. A mistake in implementation was present which prevented proper testing of its limit of detection or accuracy but the probable cause was determine for future elimination.

A planned complete implementation of the impedance sensor achieves a simulated resolution of at least .44 % with an accuracy error no more than 10 % over a range of DUT magnitudes from 30 Ω to 2.5 MΩ. The full system has a phase resolution of .09° at a test frequency of

2.5 khz. The complete sensor has an estimated circuit area of .28 mm^2 and an average power consumption of approximately 800 μW.

References

[1] Agilent Tech. *Agilent Impedance Measurement Handbook, 4th ed*. Agilent Tech., 2013.

[2] Daeil Kwon, Michael H Azarian, and Michael Pecht. Identification of interconnect failure mechanisms using rf impedance analysis. In *Signal Propagation on Interconnects, 2009. SPI'09. IEEE Workshop on*, pages 1–4. IEEE, 2009.

[3] Chunshien Li, P.J. Hesketh, and G. J. Maclay. Thin gold film strain gauges. *Journal of Vacuum Science Technology A: Vacuum, Surfaces, and Films*, 12(3):813–819, May 1994.

[4] A. Zribi, Luana E. Iorio, and D.J. Lewis. Oil-free stress impedance pressure sensor for harsh environment. In *Sensors, 2005 IEEE*, pages 3 pp.–, Oct 2005.

[5] A. Beliveau, G.T. Spencer, K.A. Thomas, and S.L. Roberson. Evaluation of mems capacitive accelerometers. *Design Test of Computers, IEEE*, 16(4):48–56, Oct 1999.

[6] F Lisdat and D Schäfer. The use of electrochemical impedance spectroscopy for biosensing. *Analytical and bioanalytical chemistry*, 391(5):1555–1567, 2008.

[7] Joseph Wang. Electrochemical detection for microscale analytical systems: a review. *Talanta*, 56(2):223–231, 2002.

[8] Jonathan S Daniels and Nader Pourmand. Label-free impedance biosensors: Opportunities and challenges. *Electroanalysis*, 19(12):1239–1257, 2007.

[9] Stéphane Moutereau, Rémy Narwa, Catherine Matheron, Natalie Vongmany, Emmanuelle Simon, and Michel Goossens. An improved electronic microarray-based diagnostic assay for identification of mefv mutations. *Human mutation*, 23(6):621–628, 2004.

[10] Penny K Riggs, Joe M Angel, Erika L Abel, and John DiGiovanni. Differential gene expression in epidermis of mice sensitive and resistant to phorbol ester skin tumor promotion. *Molecular carcinogenesis*, 44(2):122–136, 2005.

[11] Jonathan S Daniels. *An Integrated Impedance Biosensor Array*. PhD thesis, Stanford University, 2010.

[12] C. Guiducci, C. Stagni, A. Fischetti, U. Mastromatteo, L. Benini, and B. Ricco. Microelectrodes on a silicon chip for label-free capacitive dna sensing. *Sensors Journal, IEEE*, 6(5):1084–1093, Oct 2006.

[13] C. Stagni, C. Guiducci, L. Benini, B. Ricco, S. Carrara, C. Paulus, M. Schienle, and R. Thewes. A fully electronic label-free dna sensor chip. *Sensors Journal, IEEE*, 7(4):577–585, April 2007.

[14] C. Stagni, C. Guiducci, L. Benini, B. Ricco, S. Carrara, B. Samori, C. Paulus, M. Schienle, M. Augustyniak, and R. Thewes. Cmos dna sensor array with integrated a/d conversion based on label-free capacitance measurement. *Solid-State Circuits, IEEE Journal of*, 41(12):2956–2964, Dec 2006.

[15] Arun Manickam. *Integrated Impedance Spectroscopy Biosensors*. PhD thesis, The University Of Texas At Austin, 2012.

[16] Chao Yang, S.R. Jadhav, R.M. Worden, and Andrew J. Mason. Compact low-power impedance-to-digital converter for sensor array microsystems. *Solid-State Circuits, IEEE Journal of*, 44(10):2844–2855, Oct 2009.

[17] Hamed Mazhab Jafari and R. Genov. Cmos impedance spectrum analyzer with dual-slope multiplying adc. In *Biomedical Circuits and Systems Conference (BioCAS), 2011 IEEE*, pages 361–364, Nov 2011.

[18] Alberto Yufera and A. Rueda. A cmos bio-impedance measurement system. In *Design and Diagnostics of Electronic Circuits Systems, 2009. DDECS '09. 12th International Symposium on*, pages 252–257, April 2009.

[19] E. Anderson, J. Daniels, H. YU, T. Lee, and N. Pourmand. A label-free cmos dna microarray based on charge sensing. In *Instrumentation and Measurement Technology Conference Proceedings, 2008. IMTC 2008. IEEE*, pages 1631–1636, May 2008.

[20] A. Hassibi and T.H. Lee. A programmable 0.18-µm cmos electrochemical sensor microarray for biomolecular detection. *Sensors Journal, IEEE*, 6(6):1380–1388, Dec 2006.

[21] T. Kern and T. Chen. A low-power, offset-corrected potentiostat for chemical imaging applications. In *Circuits and Systems (LASCAS), 2013 IEEE Fourth Latin American Symposium on*, pages 1–4, Feb 2013.

[22] R. Quintana, A. Sequra, K. Tucker, and T. Chen. Design of a capacitance sensor in 0.18um cmos technology for biomedical application. In *Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on*, pages 396–399, Aug 2013.

[23] Gang Li and B. Maundy. A novel four quadrant cmos analog multiplier/divider. In *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, volume 1, pages I–1108–11 Vol.1, May 2004.

[24] I. Padilla-Cantoya. Compact low-voltage cmos analog divider using a four-quadrant multiplier and biasing control circuit. In *Circuits and Systems (MWSCAS), 2012 IEEE 55th International Midwest Symposium on*, pages 502–505, Aug 2012.

[25] U. Torteanchai, M. Kumngern, and K. Dejhan. A cmos log-antilog current multiplier/divider circuit using ddcc. In *TENCON 2011 - 2011 IEEE Region 10 Conference*, pages 634–637, Nov 2011.

[26] M. Ismail, R. Brannen, S. Takagi, R. Khan, O. Aaserud, N. Fujii, and N. Khachab. A configurable cmos multiplier/divider for analog vlsi. In *Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on*, pages 1085–1088 vol.2, May 1993.

[27] J. Parnklang, C. Arammongkonwichai, and P. Kongtanasunthorn. Four-quadrant cmos analog divider. In *Circuits and Systems, 1998. IEEE APCCAS 1998. The 1998 IEEE Asia-Pacific Conference on*, pages 271–274, Nov 1998.

Appendix A
Verilog Code for AGC

```
module Impedance_AGC_Controller (Clk, Reset, Hold, Low_Comparator,
    Negative_Comparator, High_Comparator, Gain, Gain_Therm,
   GainChange);

// Input types
input Clk, Reset, Low_Comparator, Negative_Comparator,
   High_Comparator, Hold;
wire Clk, Reset, Low_Comparator, Negative_Comparator,
   High_Comparator, Hold;

// Output types
output [1:0] Gain;
reg [1:0] Gain;

output [2:0] Gain_Therm;
wire [2:0] Gain_Therm;

output GainChange;
reg GainChange;

assign Gain_Therm = (Gain == 0) ? 3'b000 :
        (Gain == 1) ? 3'b001 :
        (Gain == 2) ? 3'b011 :
        3'b111;

// Internals
reg HighTest;
reg [2:0] HighCount;
reg LowTest;
reg LowFound;

always @ (posedge Clk or negedge Reset) begin
        if (!Reset) begin
                Gain <= 0;
                HighTest <= 0;
                LowTest <= 0;
                HighCount <= 0;
```

```
        LowFound <=0;
        GainChange <= 0;
end else if (!Hold) begin
        if (Gain != 3) begin
                if (Negative_Comparator && !LowTest) begin
                        LowTest <= 1;
                        LowFound <= 0;
                end else if (LowTest && Low_Comparator)
                   begin
                        LowFound <= 1;
                end else if (!Negative_Comparator &&
                   LowTest) begin
                        if (!LowFound) begin
                                Gain <= Gain + 1;
                                GainChange <= 1;
                        end
                        LowTest <= 0;
                        LowFound <= 0;
                end
        end
        if (Gain != 0) begin
                if (High_Comparator && !HighTest) begin
                        HighTest <= 1;
                        HighCount <= 1;
                end else if (HighTest && High_Comparator)
                   begin
                        HighCount <= HighCount + 1;
                end else if (HighTest && !High_Comparator)
                    begin
                        HighCount <= HighCount -1;
                end
        end

        if (HighCount == 4) begin
                Gain <= Gain - 1;
                HighTest <= 0;
                GainChange <= 1;
        end else if (HighCount == 0) begin
                HighTest <= 0;
        end
end
if (GainChange) begin
        GainChange <= 0;
```

```
            end
end

endmodule
```

Appendix B

Verilog Code for Phase Module

```
module Impedance_Phase_Module (Clk, Reset, Signal1, Signal2, Phase
    , Negative, Sig1_Prev, Sig2_Prev);

// Input types
input Clk, Reset, Signal1, Signal2;
wire Clk, Reset, Signal1, Signal2;

// Output types
output [11:0] Phase;
reg [11:0] Phase;

output Negative, Sig1_Prev, Sig2_Prev;

// Internals
reg Sig1_Prev, Sig2_Prev, Counting, Negative;

always @ (posedge Clk or negedge Reset) begin
        if (!Reset) begin
                Phase <= 0;
                Counting <= 0;
                Negative <= 0;
                Sig1_Prev <= 1;
                Sig2_Prev <= 1;
        end else begin
                if (Signal1 && !Sig1_Prev) begin
                        if (!Counting) begin
                                Counting <= 1;
                                Phase <= 0;
                                Negative <= 0;
                        end else if (Negative && Counting)  begin
                                Counting <= 0;
                        end else if (Counting && !Negative) begin
                                Phase <= 0;
                        end
                end
                if (Signal2 && !Sig2_Prev) begin
                        if (!Counting) begin
```

```
                        Counting <= 1;
                        Phase <= 0;
                        Negative <= 1;
                    end else if (!Negative && Counting) begin
                        Counting <= 0;
                    end else if (Counting && Negative) begin
                        Phase <= 0;
                    end
                end
                if (Counting) begin
                    Phase <= Phase + 1;
                end
                if (Phase > 4096) begin
                    Phase <= 0;
                    Counting <= 0;
                    Negative <= 0;
                end
                Sig1_Prev <= Signal1;
                Sig2_Prev <= Signal2;
        end
end

endmodule
```