

THESIS

AN EFFICIENT MULTI CHANNEL,  $0.2 \text{ nJ/BIT}$  TRANSMITTER WITH TUNING FOR  
PROCESS VARIATION FOR BIOMEDICAL TELEMETRY IN THE MEDRADIO BAND OF  
401-457 MHz

Submitted by

Abhiram Reddy Gundla

Department of Electrical and Computer Engineering

In partial fulfillment of the requirements

For the Degree of Master of Science

Colorado State University

Fort Collins, Colorado

Spring 2016

Master's Committee:

Advisor: Tom Chen

George Collins

Chuck Henry

Copyright by Abhiram Reddy Gundla 2016

All Rights Reserved

## ABSTRACT

### AN EFFICIENT MULTI CHANNEL, 0.2 nJ/BIT TRANSMITTER WITH TUNING FOR PROCESS VARIATION FOR BIOMEDICAL TELEMETRY IN THE MEDRADIO BAND OF 401-457 MHz

With the increasing applications of bio-integrated telemetric systems, there is a growing demand for wireless transceivers in these systems to interface with the outside world. The use of wireless transceivers is desirable because they allow complete untethering of medical devices from patients. Applications of the medical devices that have transceivers may include, but not limited to, neuro-prosthetics for stimulation, sensing vital signs, wireless monitoring of neuro chemicals in the brain, wireless endoscopy, and remote medical diagnosis and therapy. The implantable medical devices to introduce impulses to the central nervous system to treat the diseases efficiently and/or to provide relief to pain are usually in the medical implantable communication services band of 401-406 MHz. The spectrum of 401-457 MHz band is called medical device radio communications service (MedRadio) band, was allocated by FCC on secondary basis.

There exists various transmitter designs for the MedRadio band aimed at high energy efficiency (i.e low energy per bit transmitted), as low as 0.16 nJ/bit. A few designs are targeted to work at high dc power transmission efficiency, as high as 22%. But, the existing designs fail to be truly MedRadio-standard compliant with short-comings either in terms of not using all the channels in the MedRadio band, low transmitter efficiency, or low output power emitted. The search for better designs of transmitters that can utilize all the channels with high transmission efficiency and high emitted output power continues.

This thesis proposes an efficient multichannel transmitter circuit design in the MedRadio band at 401-457 MHz. The transmitter circuit consists of a multichannel phase locked loop(PLL) with rail to rail quadrature output voltage controlled oscillator (VCO), a low power digital synchronous programmable integer N-divider, bang bang Phase frequency detector (PFD), charge pump and a 3<sup>rd</sup> order loop filter, a passive mixer and a power amplifier (PA). The VCO of the transmitter is designed to account for process variation. The proposed transmitter uses quadrature phase shift keying (QPSK) modulation scheme to transmit data. The power consumption of the transmitter is 460  $\mu$ W at the power supply voltage of 1.2 V, and consumes only 0.2 nJ of energy for every bit transmitted in the MedRadio band. The output power emitted by the power amplifier of the transmitter is -10.8 dBm. The transmitter is able to hop through all the 10 channels of 300 kHz bandwidth of each from 402 to 405 MHz, all the 4 channels of 6 MHz bandwidth of each from 413 to 457 MHz. The overall global efficiency of the transmitter is 13.9%. The proposed transmitter meets all the FCC requirements for the MedRadio band. This proposed work is implemented in a 180 nm CMOS process.

The proposed transmitter working in the MedRadio band consumes only 0.2 nJ/bit compared to 0.65 nJ/bit of the only other MedRadio-band compliant design. The transmitter energy consumption is low at 460  $\mu$ W and efficiency is high at 13.9% when compared to mW energy consumption and single-digit efficiency achieved by existing designs.

## ACKNOWLEDGEMENTS

I would like to thank Dr. Tom Chen for the confidence in me and advising my thesis. I learned all the concepts of Digital and Analog Integrated Circuit (IC) Design from him. I would also like to thank Dr. George Collins and Dr. Chuck Henry for serving on my committee. I would like to thank Dr. Hugh Grinolds for teaching RFIC design. I would like to thank Electrical and Computer Engineering Department at Colorado State University-Fort Collins for providing me with this opportunity.

I would like to thank Tucker Kern, William Wilson and Kristy Scholfield, previous master graduate students of the VLSI System Architecture Laboratory for helping me in navigating through different cadence related issues. This thesis is typeset in Latex using a class created by Leif Anderson.

A special thanks to my parents, sister and friends for providing me constant support through out my life. This would not have been possible without all of you.

This thesis is typeset in  $\text{\LaTeX}$  using a document class designed by Leif Anderson.

## TABLE OF CONTENTS

Abstract .....	ii
Acknowledgements .....	iv
List of Tables .....	vii
List of Figures .....	ix
Chapter 1. Introduction .....	1
1.1. Bioelectronics and Biosensors .....	1
1.2. Medical Device Radio Communications Service Band.....	3
1.3. Contributions of This Thesis .....	4
Chapter 2. Existing Transmitter Designs.....	7
2.1. Transmitters without Phase Locked Loops .....	7
2.2. Transmitters with Phase Locked Loops.....	8
Chapter 3. Transmitter Design.....	11
3.1. Phase Locked Loop .....	12
3.2. Synchronous Pulse Swallow Divider .....	20
3.3. Voltage Controlled Oscillator.....	34
3.4. Modulation Scheme and Passive Mixer .....	40
3.5. Power Amplifier.....	42
Chapter 4. Silicon Implementation and Simulation Results .....	48
4.1. Silicon Implementation.....	48
4.2. Simulation Results .....	58

Chapter 5. Prototype of Wearable Devices .....	67
5.1. Wearable Device .....	67
Chapter 6. Conclusions and Discussions .....	73
Bibliography .....	81
Appendix A. Phase Locked Loop Parameters .....	87
Appendix B. Matching Network Design .....	90
Appendix C. Verilog code for components of Phase Locked Loop .....	92
C.1. Phase Frequency Detector and Charge Pump .....	92
C.2. Divider .....	94
Appendix D. PSS and Pnoise Analysis of the VCO .....	96
Appendix E. Wireless Interface of the Device and Connection to Internet .....	100
E.1. MSP430G2553 .....	100
E.2. Connecting to Internet via Wi-Fi through CC3200 .....	102

## LIST OF TABLES

1.1	Allowed FCC Bands .....	5
3.1	Loop filter values .....	19
3.2	States of 5/6 divider of DMP with MC=1 .....	22
3.3	States of 5/6 divider of DMP with MC=0 .....	23
3.4	Characteristic equation of D flip-flop .....	25
3.5	Characteristic equation of T flip-flop .....	25
3.6	Binary values of P and S for different output Frequencies with Fref=150 kHz .....	29
3.7	Division ratio D for different output Frequencies with Fref=100 kHz .....	30
3.8	Divider Design Comparison .....	33
3.9	Bond wire and Bond pad parasitics .....	43
3.10	Comparison of parameters for different Vdd .....	47
3.11	Summary of the PLL .....	47
4.1	Standard Cell Library gates and sizes .....	49
4.2	Power breakdown of the different components of the transmitter working in the MICS band of 401-406 MHz .....	65
4.3	Power breakdown of the different components of the transmitter working in MMNs band of 413-457 MHz .....	66
6.1	PLL Design Comparison .....	74
6.2	Comparison of Transmitter Design including PLLs in the MICS band .....	76
6.3	Comparison of Transmitter Design without PLLs in the MICS band .....	77

6.4	Comparison of Transmitter Design in the MedRadio band.....	79
A.1	Parameters of the PLL.....	87
B.1	Matching Network Variables.....	90

## LIST OF FIGURES

1.1	Top-level schematic .....	6
3.1	Transmitter block diagram .....	11
3.2	Architecture of PLL .....	12
3.3	Phase frequency Dectector .....	13
3.4	State Diagram of PFD .....	14
3.5	Phase frequency Detector output when $F_{\text{ref}}$ lagging $F_{\text{fb}}$ .....	14
3.6	Phase frequency Detector output when $F_{\text{ref}}$ leading $F_{\text{fb}}$ .....	15
3.7	Schematic of the Charge Pump .....	16
3.8	Charge pump output when $F_{\text{ref}}$ leads $F_{\text{fb}}$ .....	17
3.9	Charge pump output when $F_{\text{ref}}$ lags $F_{\text{fb}}$ .....	17
3.10	A 3 <sup>rd</sup> order loop filter .....	19
3.11	Loop filter output waveform .....	20
3.12	Block diagram of Pulse Swallow counter .....	21
3.13	Circuit Schematic of the DMP divider .....	22
3.14	DMP 20/21 output with MC=0 .....	23
3.15	DMP 20/21 output with MC=1 .....	24
3.16	Circuit Schematic of the TSPC D flip-flop .....	24
3.17	Circuit Schematic of the Program Counter .....	26
3.18	Circuit Schematic of the TFF using D flip-flop .....	26
3.19	Output of the program counter .....	27

3.20	Circuit Schematic of the Swallow Counter .....	28
3.21	Output of the swallow counter .....	28
3.22	Input Frequency to the divider .....	31
3.23	Output Frequency of the divider .....	31
3.24	Waveform with different Division Ratio of 1388 and 1372 .....	32
3.25	Waveform with different Division Ratio of 4068 and 4052 .....	32
3.26	Block diagram of the Oscillator .....	34
3.27	Circuit Schematic of the Voltage Controlled Oscillator .....	35
3.28	Monte-Carlo simulation for the frequency deviation of the VCO .....	37
3.29	Transient analysis of the VCO at different corners and temperature .....	37
3.30	Gain of the VCO ( $K_{vco}$ ) .....	38
3.31	Periodic Steady State output of the VCO .....	39
3.32	Noise profile of the VCO .....	40
3.33	Circuit Schematic of the Passive Mixer .....	41
3.34	Variation of rise and fall times with W/L .....	42
3.35	Schematic of the class-D Power Amplifier with antenna .....	43
3.36	Schematic of the $\pi$ RLC matching network .....	44
3.37	Power Consumption of PA as a function of PA transistor size with different Vdd .	45
3.38	Output Power of PA as a function of PA transistor size with different Vdd .....	45
3.39	Efficiency of PA as a function of PA transistor size with different Vdd .....	46
4.1	Layout of the Phase frequency Detector .....	48

4.2	Layout of the TSPC D flip-flop .....	50
4.3	Layout of the Dual Modulus Prescaler .....	50
4.4	Layout of the Program Counter .....	51
4.5	Layout of the Swallow Counter .....	52
4.6	Layout of the Pulse Swallow Counter .....	53
4.7	Layout of the VCO .....	54
4.8	Layout of the Capacitive bank .....	54
4.9	Layout of the Buffers, the Mixer and the Power Amplifier .....	55
4.10	Layout of the loop filter .....	56
4.11	Layout of the Charge Pump .....	56
4.12	Layout of the Transmitter .....	57
4.13	Spectrum of output of the PLL for schematic netlist .....	59
4.14	Spectrum of output of the PLL for extracted layout netlist .....	59
4.15	Control voltage ( $V_{ctrl}$ ) settling at various temperatures for same D .....	60
4.16	Spectrum of the frequency synthesizer after change in temperature for same D ...	61
4.17	Control voltage ( $V_{ctrl}$ ) settling at different D for a step size of two .....	61
4.18	Control voltage ( $V_{ctrl}$ ) settling at different D for a step size greater than one .....	62
4.19	Output waveform at the antenna .....	63
4.20	Spectrum of output at the antenna .....	64
4.21	Spectrum of output at the antenna for the channel 451-457 MHz of the MMNs band .....	66
5.1	Airpack with MSP430G2553 .....	67

5.2	MSP430 launchpad board form Texas Instruments .....	68
5.3	Spectrum of A110LR09C captured from the RSA6100A. ....	69
5.4	CC3200 board form Texas Instruments with Anaren booster pack.....	69
5.5	The web page display for the capacitive biosensor .....	70
5.6	The mobile web page display for the capacitive biosensor.....	71
5.7	Saving data on to a computer with time stamp.....	72
B.1	Matching network .....	91
D.1	Setup for PSS Analysis .....	96
D.2	Setup for Pnoise Analysis .....	97
D.3	Settings for VCO simulation .....	97
D.4	Settings for VCO simulation .....	98
D.5	PSS simulation output window.....	98
D.6	Pnoise simulation output window .....	99

## CHAPTER 1

# INTRODUCTION

Research in bioelectronics and biosensors is taking precedence nowadays. The reasons can be attributed to the rapid growing age of the large demographic population in the world, to provide point of care to the patients and to make the diagnosis and treatment with ease and much faster. The importance of bioelectronics and biosensors is ever growing with the emerging technologies and new discoveries. Hence the medical device radio communications service band, the medical network, and the medical devices are constantly evolving to meet the demands and make use of new technologies and discoveries.

This thesis discusses one such effort to meet the demands of wireless data transfer of implantable medical devices with design of an efficient and a low power transmitter in the MedRadio band of 401-457 MHz and a prototype for body wearable device connected to internet using off the shelf boards and ICs.

### 1.1. BIOELECTRONICS AND BIOSENSORS

Bioelectronics is a field of science that applies electronic hardware to the biology, medicine, and health. One of the goals of bioelectronics is to be able to implant a wireless device inside the human body with as minimum invasive process as possible. One such effort is described in [1] using electronics to interact with nerve cells. A nerve is macroscopic cord like structure of the body, comprising a collection of nerve fibers that convey impulses between a part of the central nervous system and some other body region. A peripheral nerve is a collection of nerve fibers that are between brain and the spinal cord. Research is going on to interface devices with the nerves [2]. The bio-sensors are used to detect impulse pattern of nerves and convert them to processable electrical signals. Once we are able to know the impulse pattern

of the different organs using the implantable devices connected to the organs or nerves. We can distinguish and categorize the disease cells using signature impulses patterns of various cells.

Now researching is going on in the field of impedance spectroscopy [3, 4] to determine the impedance signature of the healthy cells and infected cells. This also helps us in determining the extent of damage done to cells in the body.

These new discoveries in the field of science will enable us to detect the symptoms of diseases at an early stage. Doctors can then make an informed decision, since this gives them an accurate information of the diagnosis. This empowers the doctors to treat the diseases with a rapid pace, when compared to the existing methods.

The treatment may include external medicine or to send commands to wireless implantable device implanted on the peripheral nerve to repair and/or correct the defect impulse pattern of the organ using fibers of the nerve. This gives the patient relief immediately and more effectively. The Bio-sensors will need Bio-electronics to transmit and receive information to and from the outside world more efficiently.

The application of these wireless implantable devices also called implantable medical devices (IMD) may include neuro-prosthetics for stimulation [5], to use this stimulation as a part of therapy to reduce pain or to regain the sense of the tissues damaged. Sensing vital signs [6, 7], wireless monitoring of neuro chemicals in the brain [8], and gases in the intestine [9].

Medical capsules are another class of devices in bioelectronics. These are used for remote medical diagnosis and therapy [10]. Medical capsules are used to scan the intestine parts which are not otherwise easily reachable. With a camera embedded in these capsules, images for the inner parts of the intestine can be taken and transmitted for external monitoring.

These medical capsules are also used to introduce targeted drugs into the human body for effective treatment of diseases [11]. Detection of early onset of malignant tumor and stop the further growth of these using external commands.

Wearable medical devices are another class of devices in bioelectronics. These devices are worn on the body and can be used in various applications. These devices can be used as interface between IMDs and base stations. Body-worn devices can be used to monitor the vital signs of patients in trauma care. The wearable medical devices also require transceivers for communication and data transfer.

The power budget of the IMDs, and the capsules is low. This is to prevent the device from over heating, hence save the nerves or tissues from being damaged. The small power budget also helps keep the device small in case of IMDs, by using small battery cells. Implantable medical devices can also be powered by the energy scavenging and/or harvesting using the surrounding electromagnetic waves like in [12, 13]. This limitation on the power budget inspired many low power designs.

## 1.2. MEDICAL DEVICE RADIO COMMUNICATIONS SERVICE BAND

In 1999, Federal communications commission (FCC) created Medical Implant Communications Service (MICS) band with the 3 MHz spectrum in the 402-405 MHz range [14] to meet the requirements of the Implantable medical devices. The allowed bandwidth in the MICS band is 300 kHz, without any restriction on the center frequency. In 2009, Federal communication commission (FCC) created Medical Device Radio communications Service (MedRadio) band with 5 MHz spectrum in the 401-406 MHz range. The adjacent bands are 401-402 MHz and 405-406 MHz added to the previously existing 3 MHz MICS band from 402-405 MHz. This is to meet the demands of the medical devices both human implantable

and body worn. In 2011, the FCC released an order to allow up to 24 MHz of additional spectrum in the MedRadio Service for implanted devices that help restore sensation, mobility, and other functions to limbs and organs. The technical term for these devices is Medical Micro-Power Networks (MMNs).

The reasons for choosing 401-457 MHz band for MedRadio is propagation characteristics, availability, and compatibility with other users in this band. The 400 MHz frequency is optimum frequency for the waves to propagate through human body with minimum losses, although size of antenna for 400 MHz is large with a few  $\text{cm}^2$  area.

401-457 MHz band is allocated to the medical devices on the secondary basis. The primary priority is given to the Federal Government meteorological operations in the band. There are regulations on the power emitted by the devices and the bandwidth utilized in the allocated spectrum. The regulations of FCC limits the maximum strength of the output signal emitted by the transmitter to  $-16$  dBm, which translates to the  $V_{\text{peak}}$  of signal to 50 mV for an antenna impedance of  $50 \Omega$ . The spurious signal in the adjacent channels within the 401-457 MHz band should be 20 dB below the main channel signal strength. The range of frequencies and the allowed bandwidths in the MedRadio communication service band as per FCC regulations is shown in Table 1.1.

### 1.3. CONTRIBUTIONS OF THIS THESIS

This thesis is part of ongoing research on bioelectronics and biosensors at Colorado State University- Fort Collins. Figure 1.1 [15] show the top level schematic of the research at CSU. The previous research in [16, 17] concentrated on the design of interface circuits for the biosensor applications. A temperature sensor for biomedical applications was presented in [15]. The experimental data from interface circuits is proposed in thesis [18]. An

TABLE 1.1. Allowed FCC Bands

<b>Frequency</b>	<b>Bandwidth</b>
401-401.85 MHz	100 kHz
401.85-401.2 MHz	150 kHz
402-405 MHz	300 kHz
405-406 MHz	100 kHz
413-419 MHz	6 MHz
426-432 MHz	6 MHz
438-444 MHz	6 MHz
451-457 MHz	6 MHz

impedance sensor was proposed in [19], which allowed conversion of the impedance to digital data. This allows us to detect any abnormalities in the cells. This thesis attempts to complete the wireless interface part by designing a transmitter in the MedRadio band of 401-457 MHz to transfer the processed digital data from the different interface circuits and demonstrate the capability of wearable devices to be able to connect to the Internet.

This thesis presents a high efficiency and an ultra low power transmitter design for MedRadio band, a discrete wireless module for the hand held and body worn devices. The proposed transmitter consists of a frequency synthesizer which can utilize all the bandwidths allowed by the FCC in the MedRadio band of 401-457 MHz. Power consumption of the proposed design is 460  $\mu$ W, with an efficiency of 13.9% for the MMNs band. This is significantly higher than most of the published designs with phase locked loops. The energy consumed per bit transmitted is at 0.2nJ/bit.

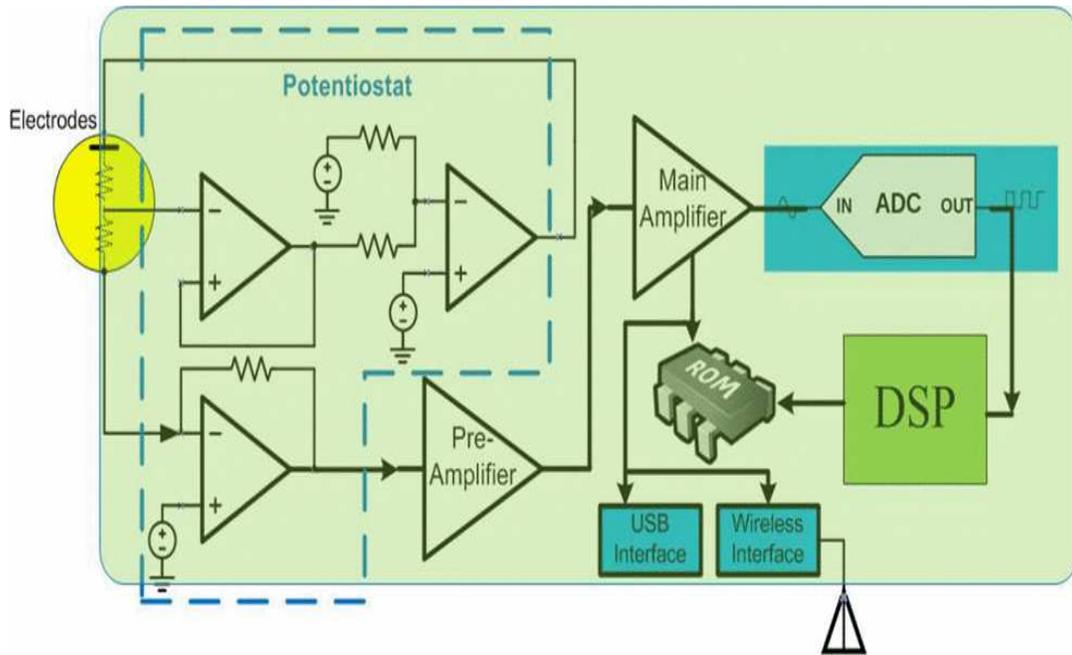


FIGURE 1.1. Top-level schematic

This thesis is organized as follows: Chapter 2 discusses the existing work in low power transmitters for IMDs mainly in the MICS band. Chapter 3 presents the details of the components and working of the transmitter. Chapter 4 shows the CMOS silicon implementation and simulation results of the proposed transmitter design in a 180nm process. Chapter 5 discusses with the prototype of the Internet connect-able hand held and body worn devices and Chapter 6 concludes the thesis with analysis of results and scope for further improvements.

## CHAPTER 2

### EXISTING TRANSMITTER DESIGNS

This chapter reviews the existing research on the transmitter designs, concentrating on the Medical Device Radio communications Service Band of 401-457 MHz. Section 2.1 discusses the transmitters designed using Injection Locked Loop Transmitters. Section 2.2 deals with the transmitters implemented using Phase Locked Loop.

#### 2.1. TRANSMITTERS WITHOUT PHASE LOCKED LOOPS

The designs in [20–22] reported low power and high efficiency transmitters. They use injection locked loop to present an optimum solution at a particular frequency in MedRadio band. These designs are able to produce 400.5 MHz and 400.68 MHz with a crystal oscillator of frequency 44.5 MHz.

The MedRadio band for the IMDs is allocated on the secondary basis. So these designs cannot cover all the allotted frequency bands in the MedRadio band users may have to wait more time to be turned on to transmit the data effectively without interference from the other high priority signals in the 401-406 MHz. This wait time is avoidable with efficient use of spectrum in the MedRadio band. Moreover to generate all the frequency bands in range of 401-406 MHz, these designs may have to use different crystal oscillators on-chip. This will not only increase the area but also increase the power consumption of the transmitter.

Ma, et. al. [23] proposed a low power design by biasing transistors near their threshold voltages to achieve power consumption in the order of hundreds of  $\mu\text{W}$ . The design also uses a lower power supply (0.6 V) for the transmitter and a higher voltage supply (0.7 V) for the receiver to reduce power consumption. However, such designs using multiple power

supplies significantly increase design complexity. This design like the previous injection locked designs [20–22] can only produce a few frequencies in the band of 402-405 MHz

These designs are not MedRadio band complaint, i.e. not able to cover all the channels in the MedRadio band. Thus the use of injection locked loop transmitters inhibits the effective use of the frequency spectrum in the MedRadio band of 401-457 MHz. Most of the injection locked loop transmitters are built to operate with low power, hence high efficiency of power transmission and low energy per the bit transmitted.

## 2.2. TRANSMITTERS WITH PHASE LOCKED LOOPS

On the other hand there are many transmitter architectures that use the classical Phase Locked Loop (PLL) in the frequency synthesizer. These transmitters can use the spectrum allocated in the MedRadio band as described in [24–26]. But, the power consumption of the proposed designs in [24, 25] is high in the order of mW because of their use of high power consumption for oscillator to generate a high frequency output and then obtain the MICS band frequencies. The high power consumption in these designs lowers the transmitters efficiency drastically.

Similarly, the design in [26] uses a power supply of 1.8 V with the power consumption of 4.9 mW for the transmitter. The data rate in the MICS band is at 50 kbps. The high power consumption can be attributed to the use of relatively high supply voltage of 1.8 V and the use of LC Voltage Controlled Oscillator (VCO). The overall transmission efficiency is low and the energy per bit is high for this design. This design cannot cover MMNs band.

The published designs in [27–29] suffer from low overall global efficiency. The low global efficiency is due to the use of high power supply between 1.8 V and 3.3 V in these designs.

The power consumption in [27] is 10 mW. The reasons for high power consumption are due to the fact that its a whole transceiver and the running frequency of the VCO of the PLL in frequency synthesizer is four times the required frequency.

The transmitter designs proposed in [28, 29] utilizes the Medradio band of 340-457 MHz for the Medical Micro-Power Networks (MMNs). But, there is no way to utilize all the channels in the range of 401-406 MHz since fixed input reference frequencies are used in designs in [28, 29]. This limits the effective utilization of the MedRadio band by these proposed designs for IMDs. The energy per bit transmitted is 0.65nJ/bit in these designs. More over same technique as in [24, 25] is used to generate the frequencies of the VCO, that to generate high frequency of 800 MHz to derive 400 MHz frequency, this technique places the power consumption of these transmitters in the order of mWs.

The Digital Controlled Oscillator (DCO) as proposed in [30] uses direct modulation of the DCO to transmit data, thus eliminating power amplifier. This design is able to cover all the ten channels of 300 kHz bandwidth in the MICS Band. But, this design uses off chip calibration of the capacitance bank to correct the frequency error of the DCO. The power consumption of the periodic calibration is not accounted towards the power of the transmitter, which will increase the power consumption of transmitter beyond the reported 350  $\mu$ W.

The proposed design in [31] uses an input reference frequency of 300 kHz. A total of 10 channels each of 300 kHz can be used in 402-405 MHz band. But this design can utilize only 9 channels out of the 10 usable channels.

The MICS band frequency synthesizer design in [32] uses an input reference frequency of 300 kHz and can utilize only 9 channels instead of 10 channels in 402-405 MHz band.

Moreover the area of frequency synthesizer used by the proposed design is high, due to use of LC tank type voltage controller oscillator (VCO).

The designs in [31, 32] are only aimed at MICS band and cannot cover the MMNs band. Moreover these designs present only the frequency synthesizers, not the transmitters.

This thesis addresses the demand of wireless transceivers with a transmitter design in MedRadio band with an ultra low power consumption of  $460\ \mu\text{W}$  at a supply voltage of  $1.2\ \text{V}$ , utilize the MedRadio band spectrum effectively, and achieve a high overall global efficiency while keeping up with the energy per bit. The proposed transmitter is operated at a reduce supply voltage of  $1.2\ \text{V}$  instead of the nominal  $1.8\ \text{V}$  in the  $180\ \text{nm}$  CMOS process to increase the global efficiency. This proposed transmitter utilize the spectrum by hopping through all the channels with different bandwidths allowed in the  $401\text{-}457\ \text{MHz}$  band, with the help of the programmable integer N-divider of the phase locked loop (PLL).

## TRANSMITTER DESIGN

This chapter explains the working components of the transmitter in detail in the following sections. The block diagram of the proposed transmitter for the IMD is shown in Figure 3.1. A transmitter contains a Phase Locked Loop (PLL), a passive mixer, and a power amplifier (PA).

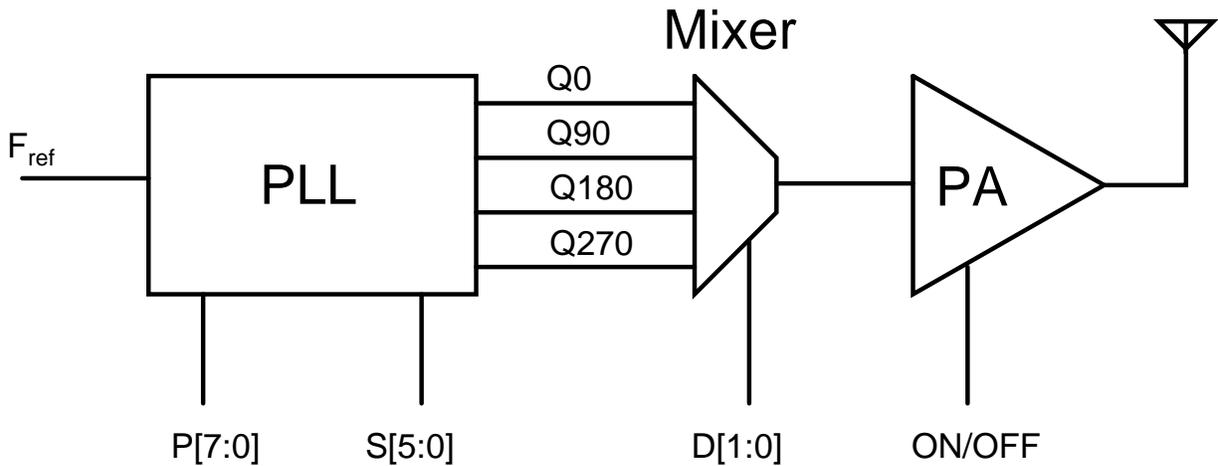


FIGURE 3.1. Transmitter block diagram

The PLL is responsible for two tasks, it provides the frequency synthesis function to allow the transmitter to hop among the defined bands within the MedRadio band, it provides a tuning capability to tackle the effect of process and temperature variations. The PLL provides a quadrature output signal for the mixer for better management of spectrum resources within the MedRadio band with lower bit rate. The use of passive mixer in the design contributes to lower overall power consumption. A class-D power amplifier was used

to improve power efficiency and design simplicity. The following subsections describe each major component in the transmitter in more detail.

### 3.1. PHASE LOCKED LOOP

The conventional architecture of frequency synthesizers using the PLL is shown in Figure 3.2. A PLL contains a phase frequency detector, a charge pump, a loop filter, a programmable divider that can operate up to 1 GHz, a voltage controlled oscillator that can cover all the frequency bands in the range 355-550 MHz followed by the buffers.

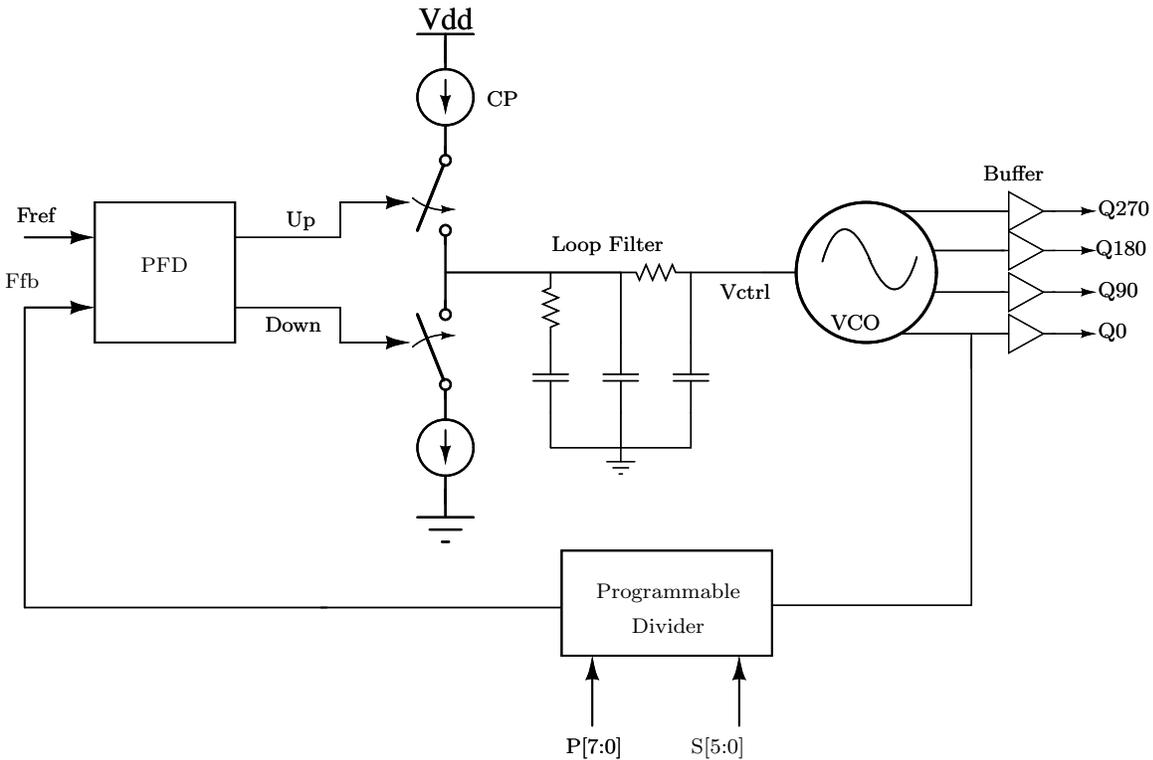


FIGURE 3.2. Architecture of PLL

The working principle of the frequency synthesizer is the input reference frequency ( $F_{ref}$ ) is multiplied by the by the division ratio ( $D$ ) of the programmable divider. The output frequency is divided by the programmable divider and is compared with the  $F_{ref}$  using the

phase frequency detector (PFD). The PFD controls the duration of current charged and discharged of the charge pump according to the phase difference between  $F_{\text{ref}}$  and  $F_{\text{fb}}$ . The output of charge pump drives the loop filter which in turn control the varactor of the VCO. The phase is compared until the phase difference is nil and then the final settled output frequency of the VCO is  $D \times F_{\text{ref}}$ .

3.1.1. PHASE FREQUENCY DETECTOR. The phase frequency detector (PFD) used in the proposed frequency synthesizer is shown in Figure 3.3. PFD consists of two D flip-flops, one is fed with input reference frequency ( $F_{\text{ref}}$ ) and the other flipflop is fed with feedback frequency ( $F_{\text{fb}}$ ) which is an output of the programmable divider.

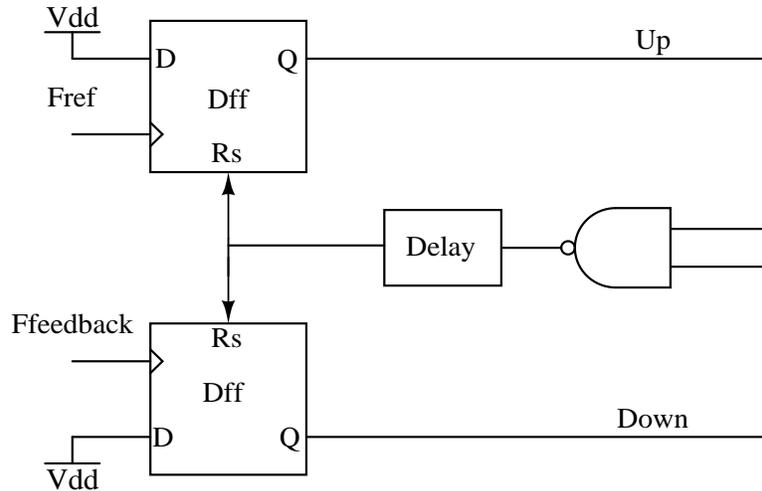


FIGURE 3.3. Phase frequency Dectector

The state transition diagram of the phase frequency detector is shown in Figure 3.4. The outputs of the D flip-flops generate “Up” signal when  $F_{\text{ref}}$  leads  $F_{\text{fb}}$  and “Down” signal when  $F_{\text{ref}}$  lags  $F_{\text{fb}}$ . These “Up” and “Down” signals are used to clear the flipflop and to control the charge pump. The delay element is added to generate the pulses of minimum width required to turn on or off the charge pump, when phase difference is small to detect.

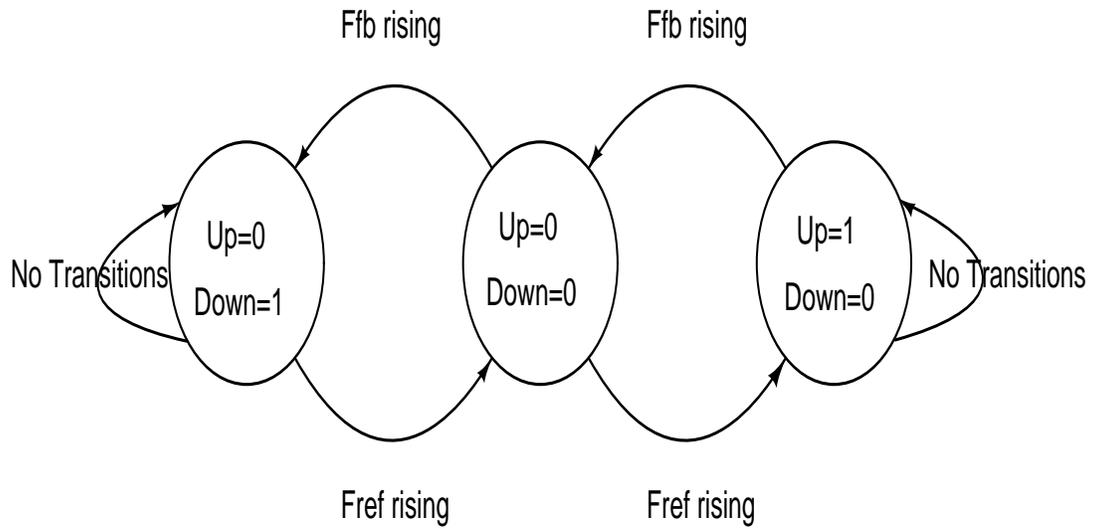


FIGURE 3.4. State Diagram of PFD

The outputs of the Phase Frequency Detector is when  $F_{\text{ref}}$  lagging  $F_{\text{fb}}$  and  $F_{\text{ref}}$  leading  $F_{\text{fb}}$  are shown in Figure 3.5 and Figure 3.6.

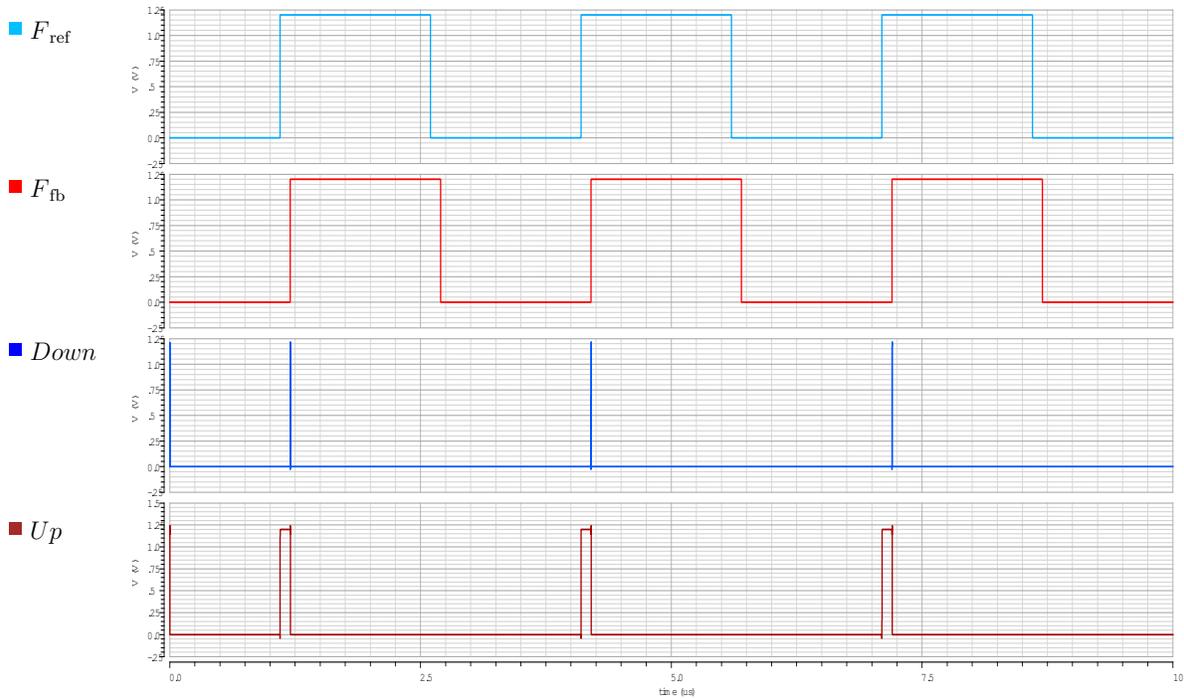


FIGURE 3.5. Phase frequency Detector output when  $F_{\text{ref}}$  lagging  $F_{\text{fb}}$

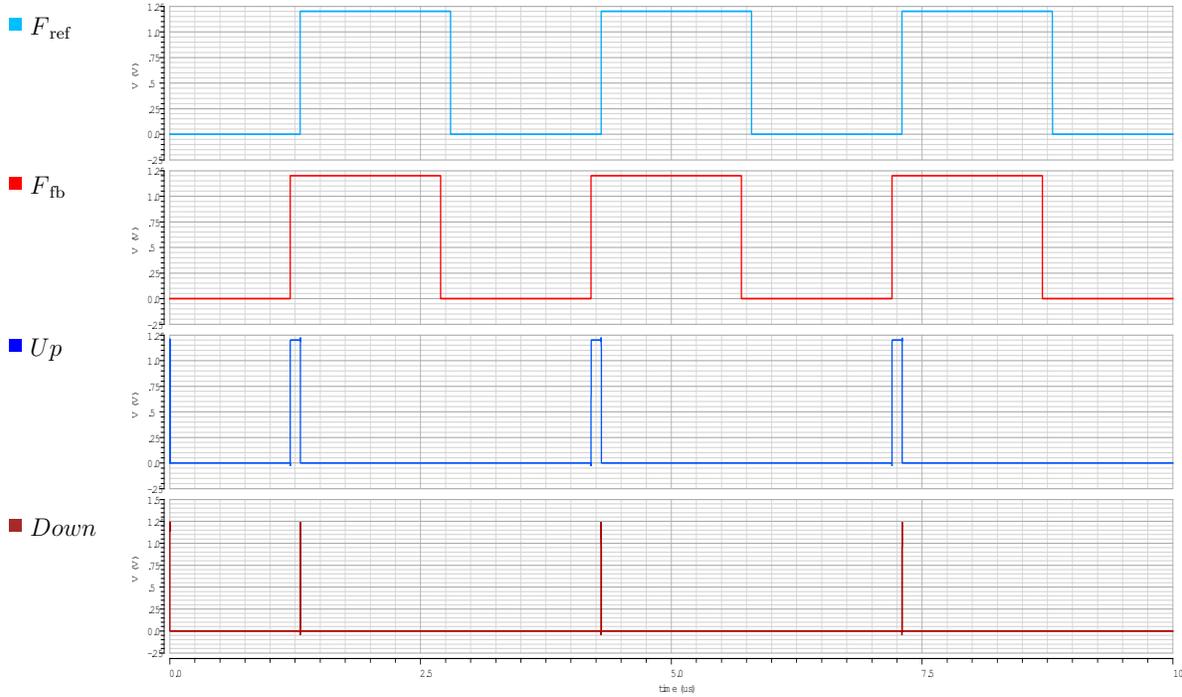


FIGURE 3.6. Phase frequency Detector output when  $F_{\text{ref}}$  leading  $F_{\text{fb}}$

3.1.2. CHARGE PUMP. The charge pump used in this frequency synthesizer is shown in Figure 3.7. A Cascode structure is implemented for the current mirror to improve power supply rejection ratio (PSRR), thereby reducing the spurious emissions of the PLL. This also improves the output impedance of the current mirror and hence allows the current mirror to draw or sink the current that’s required.

The “Up” signal controls the PMOS side of the current mirror, “Down” signal controls the NMOS side of the current mirror. The switching transistors MP9, and MN12 are placed away from output signal ( $V_{\text{ctrl}}$ ) to prevent the clock feed-through of the “Up” or “Down” signals on to the output,  $V_{\text{ctrl}}$ . The output current of the charge pump for this PLL is chosen to be  $15\ \mu\text{A}$  to limit the power consumption of the PLL, while achieving sufficient loop gain and bandwidth for the frequency synthesizer.

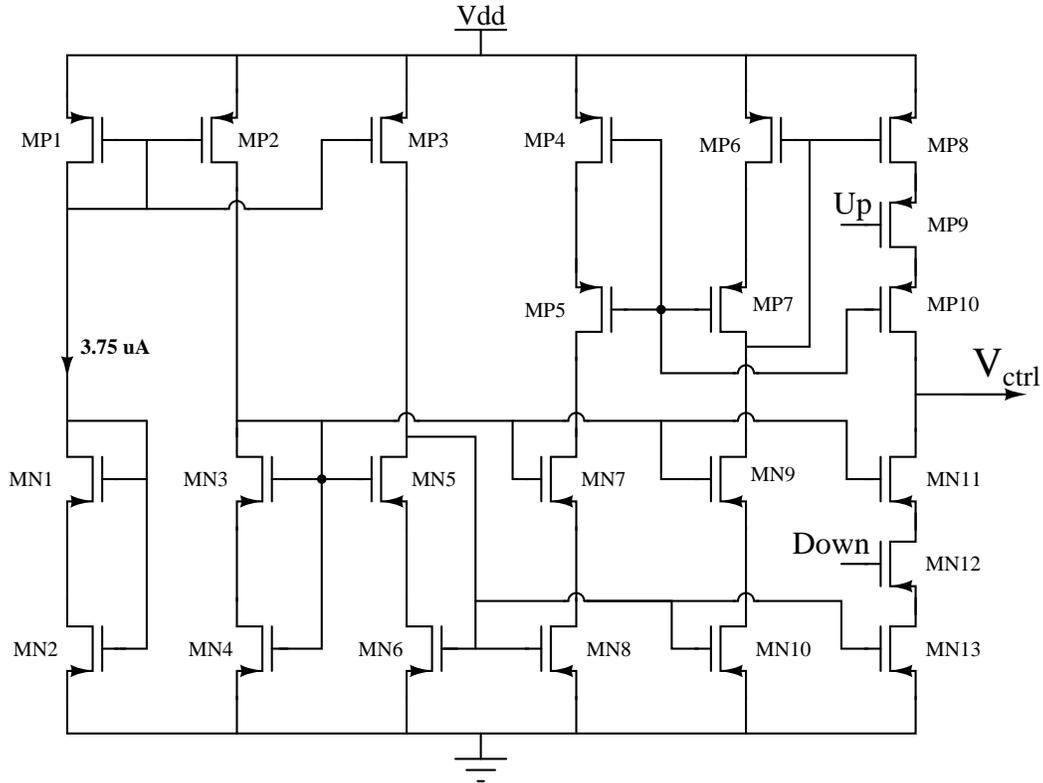


FIGURE 3.7. Schematic of the Charge Pump

The first five stages of the charge pump consume a total current of  $18.75 \mu\text{A}$  with each stage being  $3.75 \mu\text{A}$ . The current in the final stage is  $15 \mu\text{A}$ . The total power consumption of the charge pump is  $40 \mu\text{W}$ .

The output of the charge pump is shown in Figure 3.8 when the  $F_{\text{ref}}$  leads  $F_{\text{fb}}$ . Here, the “Up” signal is high; the “Down” signal is low. This will turn on the PMOS side, turn off the NMOS side of the output branch. Hence, the loop capacitor is charged as the waveform  $V_{\text{cp}}$  for every “Up” high signal generated in this case. The  $V_{\text{ctrl}}$  is the output of the loop filter. Figure 3.9 shows the output of the charge pump when  $F_{\text{ref}}$  lags  $F_{\text{fb}}$ . This is when the “Up” signal is low and the “Down” signal is high. The loop capacitor is discharged from the initial value for every “Down” high signal generated, as the waveform  $V_{\text{cp}}$ .

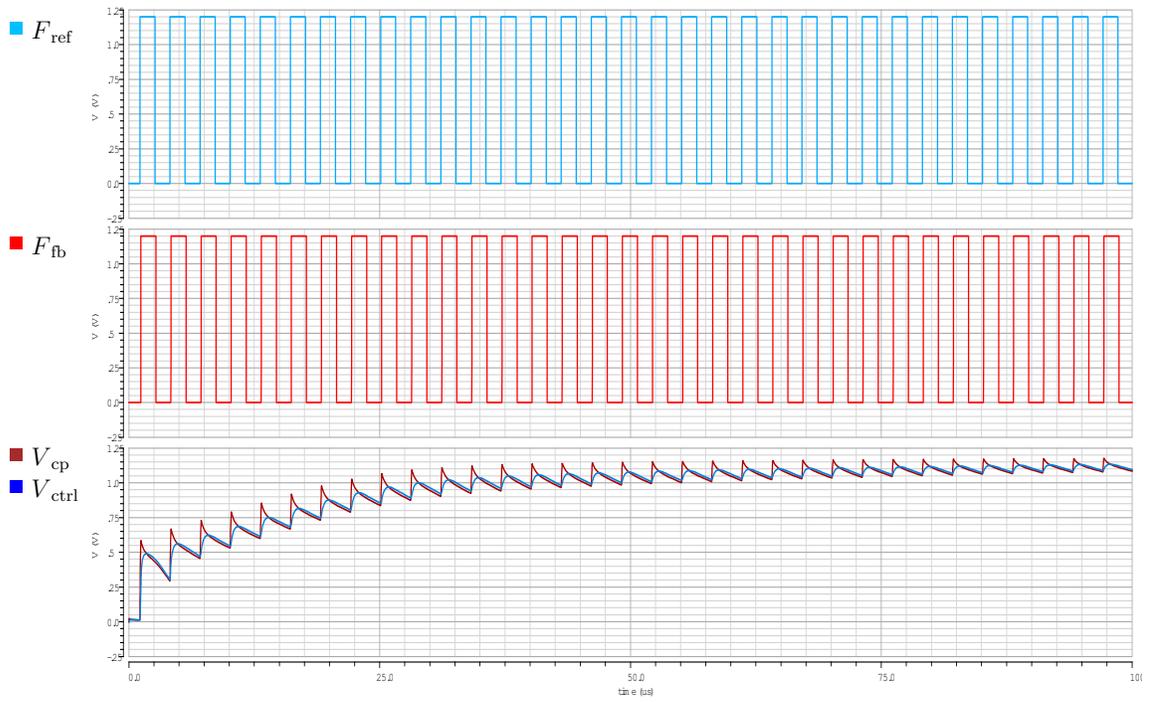


FIGURE 3.8. Charge pump output when  $F_{\text{ref}}$  leads  $F_{\text{fb}}$

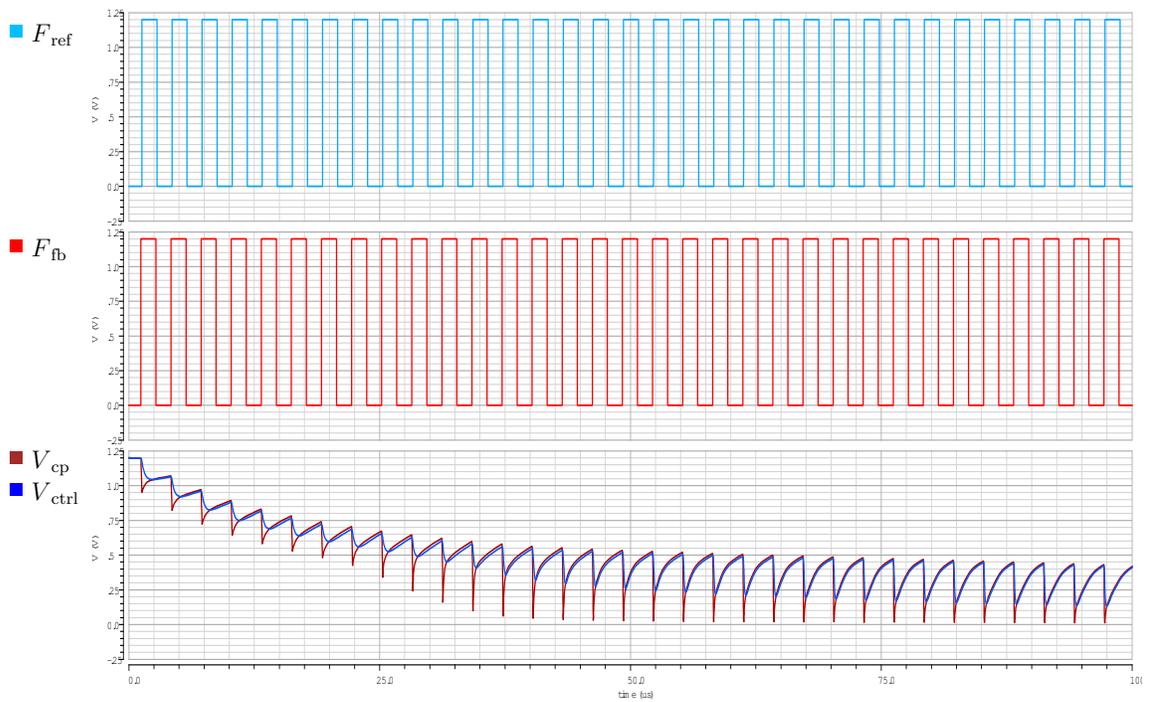


FIGURE 3.9. Charge pump output when  $F_{\text{ref}}$  lags  $F_{\text{fb}}$

3.1.3. LOOP FILTER. The loop filter is a low pass filter in the PLL. It filters the control voltage after the Charge Pump (CP) to limit the spurious emissions of the PLL in terms of sideband harmonics, multiples of input reference frequency for a given output frequency. The loop filter can be either active or passive. Active loop filters are used in PLL to drive the varactor of the VCO more accurately to prevent spurious frequencies in the out of band frequencies. Active filters are generally used where the gain of the Voltage Controlled Oscillator (VCO) is high and the control voltage has to be maintained with minimum drift. Active loop filter often have a unity gain buffer, so the power consumption of the PLL increases. The gain of the VCO used in the proposed design is moderate, hence the use of a passive filter in the proposed frequency synthesizer is justified.

The third order passive loop filter used for the proposed frequency synthesizer as shown in Figure 3.10. The design of the 3<sup>rd</sup> order loop filter follows the similar procedure discussed in [33]. The impedance transfer function of the loop filter can be approximated to the equation (1)

$$(1) \quad Z(s) = \frac{(s.T_2 + 1)}{s.C_1.(s.T_1 + 1).(s.T_3 + 1)} \cdot \frac{T_1}{T_2}$$

where  $T_2 = R_2C_2$ ,

$T_1 = R_2C_2C_1 / (C_1 + C_2 + C_3)$ , and

$T_3 = R_3C_3$ .

The open loop gain of the 4<sup>th</sup> order PLL with 3<sup>rd</sup> order loop filter is as expressed in equation (2)

$$(2) \quad G(S).H(S) = \frac{K_\phi.K_{vco}.(s.T_2 + 1)}{s^2.C_1.N.(s.T_1 + 1).(s.T_3 + 1)} \cdot \frac{T_1}{T_2}$$

Optimizing the open loop gain equation for phase margin ( $\phi$ ) gives us the time constants as a function of phase margin ( $\phi$ ), and loop bandwidth( $F_c$ ). Solving for components of loop filter resulted in design parameters shown Table 3.1. The equations are derived in detail in Appendix A. The loop bandwidth of the frequency synthesizer determines the size of the components of the loop filter and the settling time of the PLL.

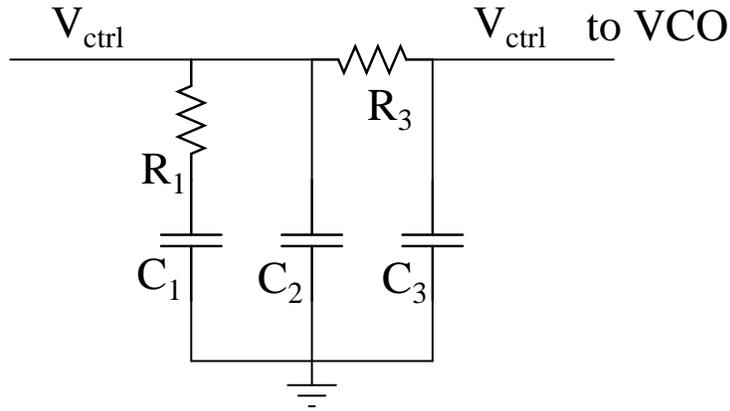


FIGURE 3.10. A 3<sup>rd</sup> order loop filter

TABLE 3.1. Loop filter values

Parameter	Value
C1	68.0 pF
C2	6.8 pF
C3	2.5 pF
R1	670.0 k $\Omega$
R3	470.0 k $\Omega$

Figure 3.11 shows waveforms at the output of the charge pump ( $V_{cp}$ ) and at the output of the loop filter ( $V_{ctrl}$ ), which controls the varactors of the voltage controlled oscillator

(VCO) of the PLL. The waveforms shown are from the simulation of the proposed frequency synthesizer. The output of the charge pump ( $V_{cp}$ ) has glitches which are evident from Figure 3.11. The 3<sup>rd</sup> order loop filter in the frequency synthesizer reduces these glitches.

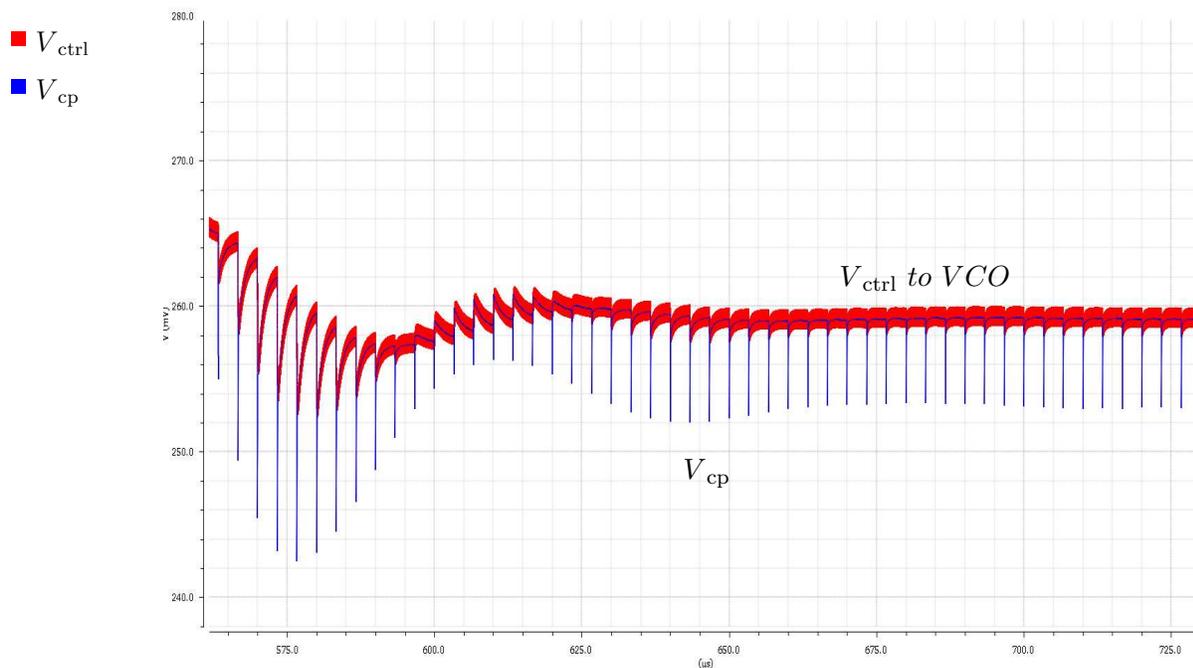


FIGURE 3.11. Loop filter output waveform

### 3.2. SYNCHRONOUS PULSE SWALLOW DIVIDER

Figure 3.12 shows the block diagram of the divider originally proposed in [34]. This is a low power synchronous pulse swallow counter. The counter has a 20/21 Dual modulus prescaler, a 8 bit wide program counter and a 6 bit wide swallow counter.

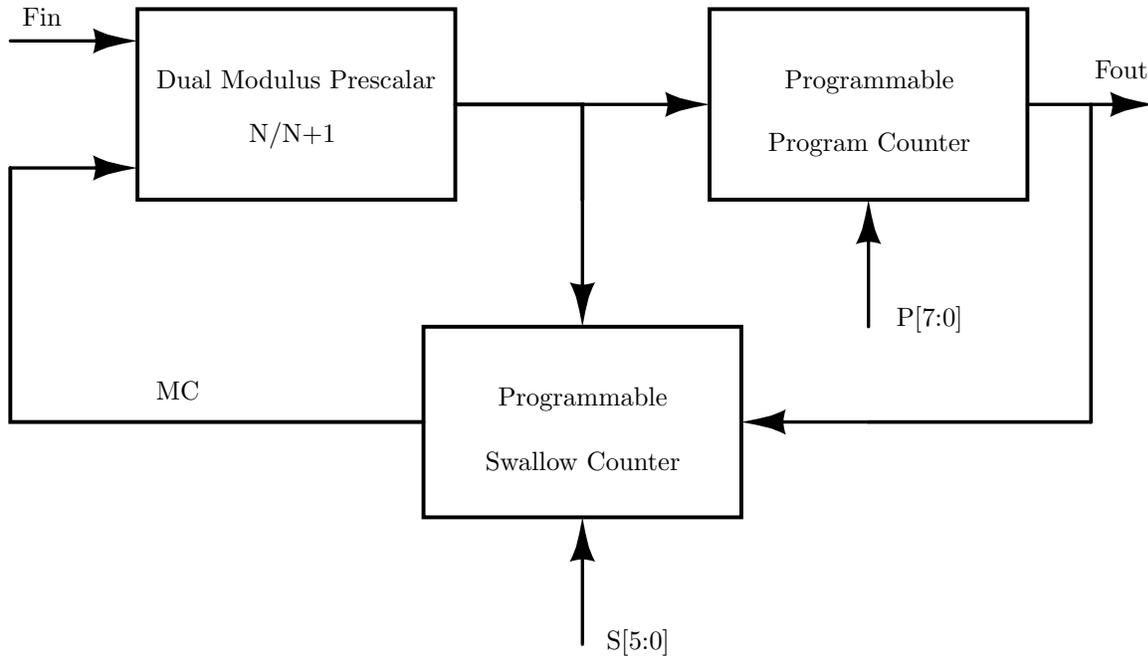


FIGURE 3.12. Block diagram of Pulse Swallow counter

3.2.1. DUAL MODULUS PRESCALAR. Dual modulus prescalar is a 20/21 divider and is shown in Figure 3.13. The division ratio is set to be 21 and 20 when modulus control signal from the swallow counter (SC) is 1 and 0 respectively. It contains a divide 5/6 circuit followed by two divide-by-2 asynchronous circuits. The Dff1, Dff2, Dff3 form 5/6 modulus divider. The different transition states of the 5/6 divider for both values of MC are shown in Table 3.2 and 3.3.

When MC=0 first 3 flip flops count five clock cycles, divide by 4 circuit count a total of 20 cycles. When MC=1, after counting 20 clock cycles A=1, B=1 making the circuit count one more extra cycle before its reset and start counting 20 or 21 cycles depending on the value of MC.

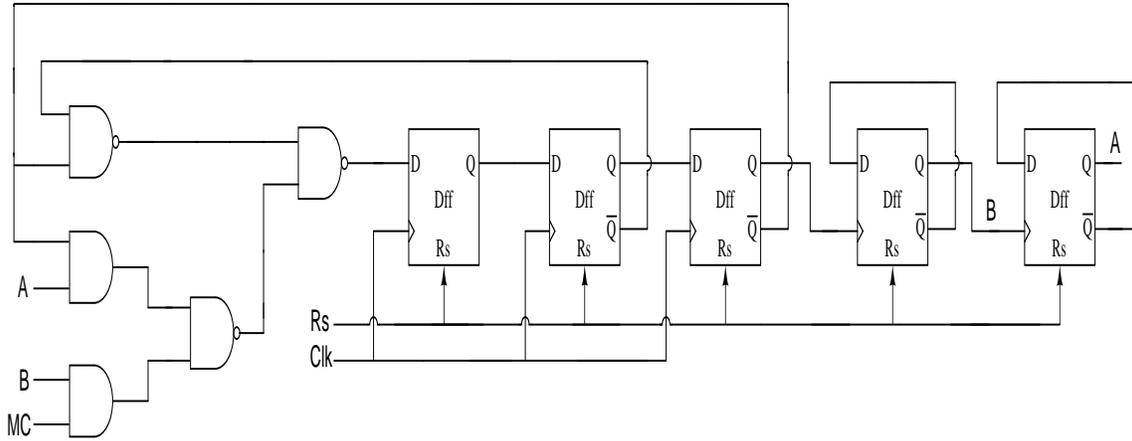


FIGURE 3.13. Circuit Schematic of the DMP divider

TABLE 3.2. States of 5/6 divider of DMP with MC=1

Present State	Next State
111	011
011	001
001	000
000	100
100	110
110	111

Figure 3.14 and 3.15 shows the output of the Dual Modulus Prescaler under different conditions of Modulus Control (MC) signal. When MC=0 we can see that the 20/21 DMP counts 20 cycles of the input, hence the division by 20. When MC=1 we can see that the 20/21 DMP counts 21 cycles of the input as explained previously, hence the division by 21.

Most of the power consumption of the DMP is due to DFF1, DFF2 and DFF3. Since these 3 DFFs run on the same clock which run at the speed of the VCO output i.e. 406 MHz for the MICS band application.

TABLE 3.3. States of 5/6 divider of DMP with MC=0

Present State	Next State
011	001
001	000
000	100
100	110
110	011

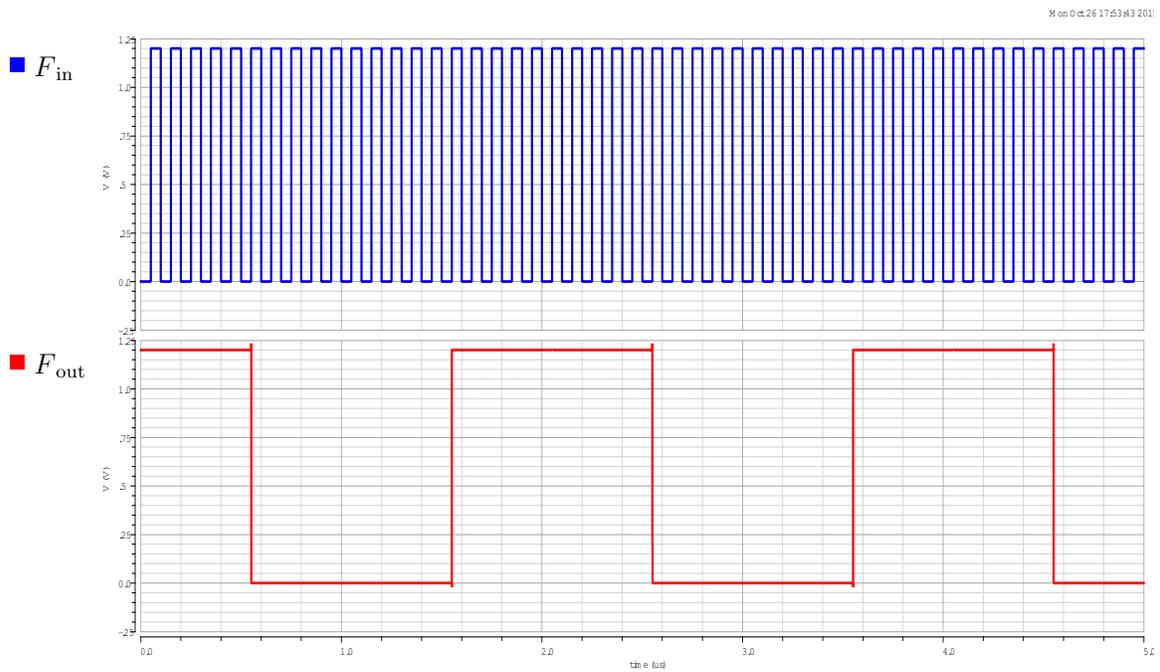


FIGURE 3.14. DMP 20/21 output with MC=0

A simple True Single Phase Clock D flip-flop (TSPC-DFF) shown in Figure 3.16 is used for the divider. The delay of the divider determines how quick the divided output is present at the Phase Frequency Detection (PFD) circuit. The longer the delay, the time to change the  $V_{ctrl}$  of the loop filter increases. Hence, the output of VCO is at different frequency for a longer period, effecting the spectrum of the transmitter. The TSPC-DFF is a good

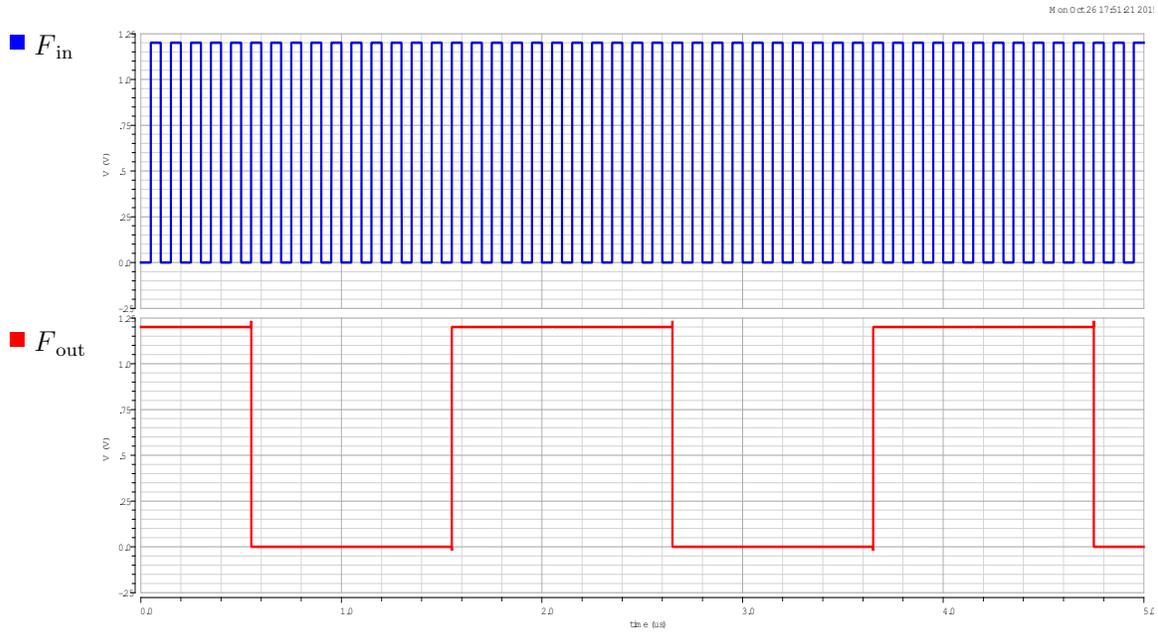


FIGURE 3.15. DMP 20/21 output with MC=1

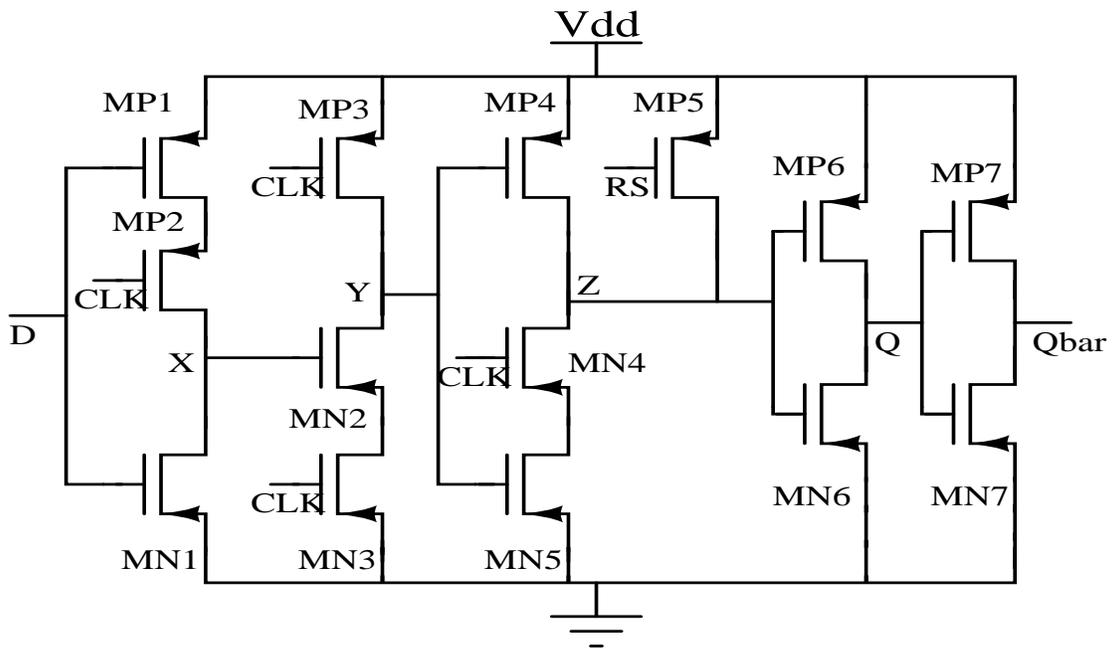


FIGURE 3.16. Circuit Schematic of the TSPC D flip-flop

design choice for divider design because of lower delays. The divider in the proposed pulse swallow programmable divider is designed to be synchronous to avoid accumulated jitter and the delays involved in the asynchronous design. The synchronous divider consume higher power when compared to asynchronous dividers, due to operation of the DFFs at high frequencies in the synchronous divider. The power savings is not affected drastically by using the synchronous divider in the proposed design.

A positive edge TSPC-DFF is chosen for this design. When Clk is low MP2, MP3 is on and MN3, MN4 is off. At node X output is D', node Y is pre-charged to 1. When Clk is high MP2, MP3 is off and MN3, MN4 is on. Then node Y is D, node Z is D'. So the value of D at the positive edge of the Clk is sampled and stored till the next rising clock edge.

TABLE 3.4. Characteristic equation of D flip-flop

Present State	Next State
Q	D

3.2.2. PROGRAM COUNTER. The 8-bit programmable program counter is shown in Figure 3.17. The other input to the XOR gate is D[0:7], the code for programming the program counter. The output is sampled by 2 DFFs to make it align with the clock timing.

The T flip-flop used in the programmable program counter is designed using a TSPC D flip-flop and an XOR gate is shown in Figure 3.18. The characteristic equation of the T flip-flop is shown below.

TABLE 3.5. Characteristic equation of T flip-flop

Present State	Next State
Q	$T \oplus Q$



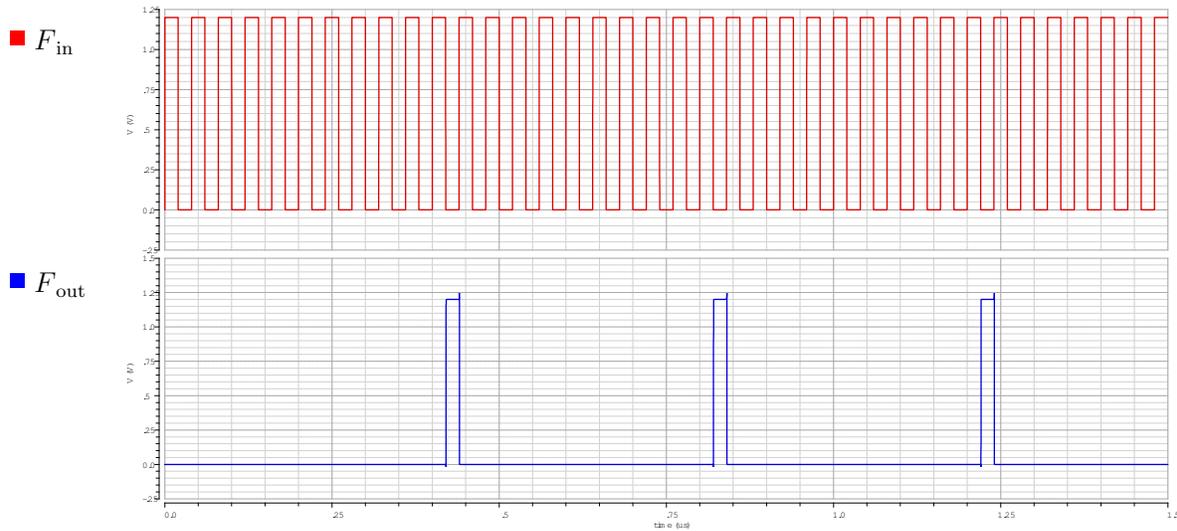


FIGURE 3.19. Output of the program counter

The output of the program counter is shown in Figure 3.19. The input frequency is 25 MHz, the division ratio (P [7:0]) of the program counter is set to 00001010 (decimal 10). The output pulses are at a separation of 400  $\mu$ s. Hence, the division ratio 10 has been performed using the programmable program counter.

3.2.3. SWALLOW COUNTER. Programmable swallow counter is shown in Figure 3.20. The output of the swallow counter is shown in Figure 3.21. The input frequency is 25 MHz. The frequency of main reset to the swallow counter is 2.5 MHz. The division ratio (S [5:0]) of the swallow counter is set to 000100 (decimal 4). Hence, at the onset of every reset pulse the swallow counter is high for 4 clock cycles and low until the swallow counter is activated by the next reset pulse.

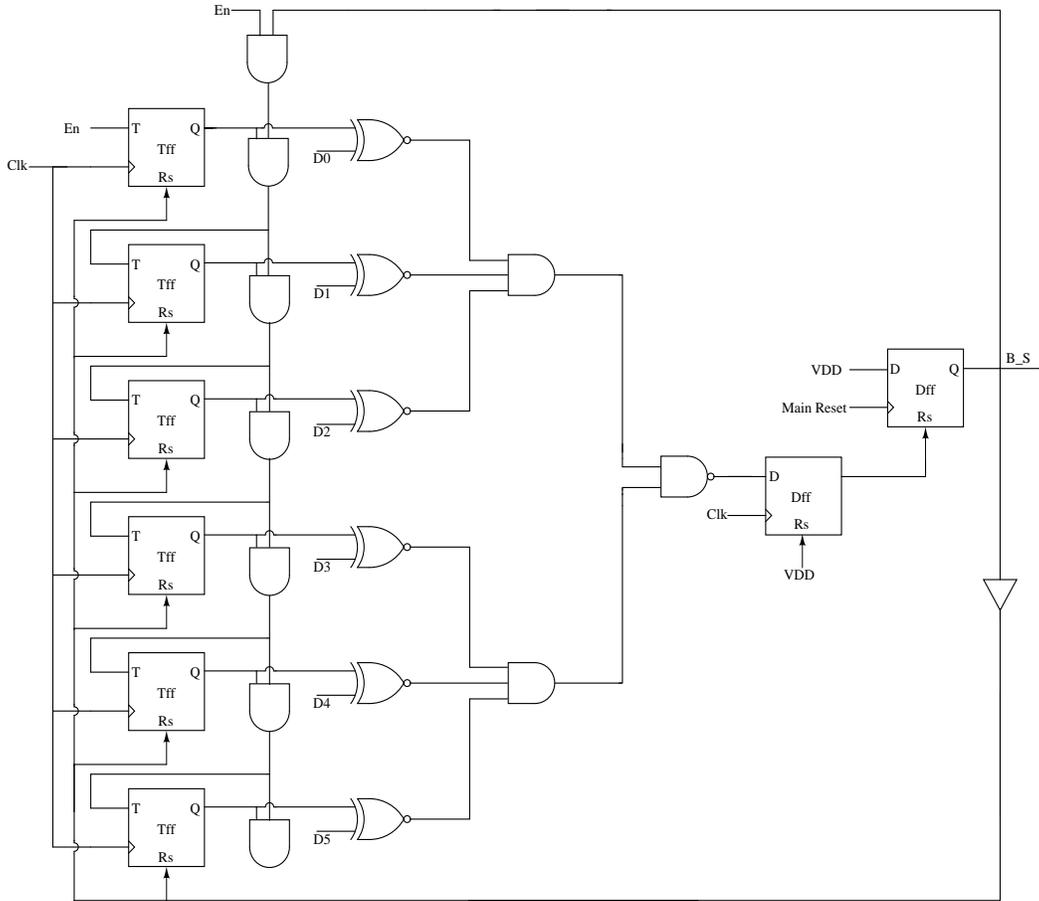


FIGURE 3.20. Circuit Schematic of the Swallow Counter

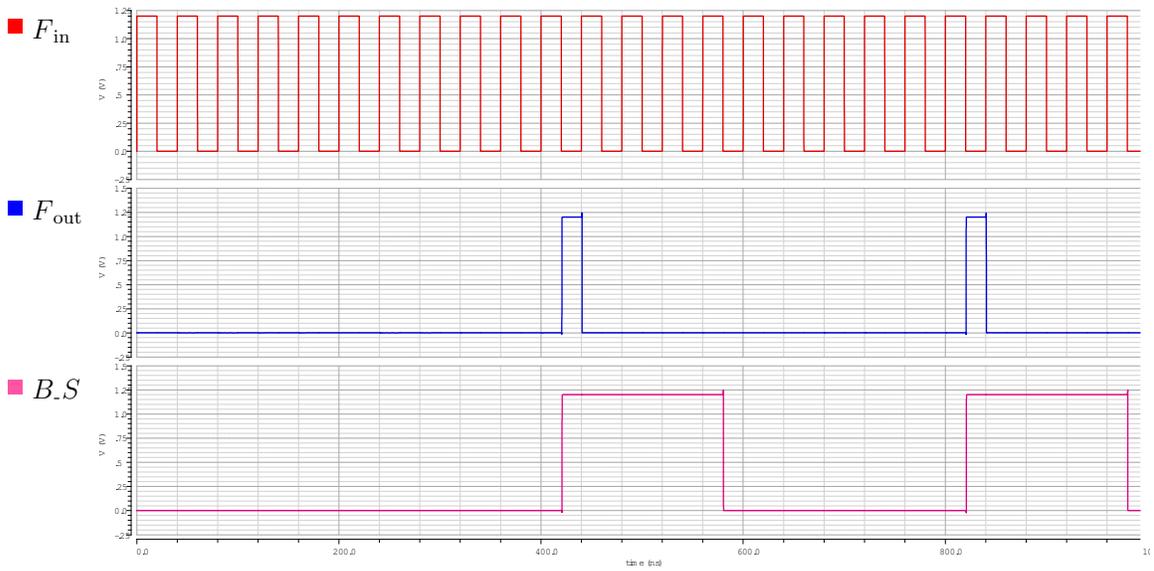


FIGURE 3.21. Output of the swallow counter

The digital input P of the program counter and S of the swallow counter is programmed to attain required frequency in 401-457MHz band. The overall integer division ratio D is given by  $N \cdot P + S$ . The required division ratio D for different input reference frequencies is shown in Tables 3.7 and 3.6, for the output frequencies to be in the range of 401-457MHz.

TABLE 3.6. Binary values of P and S for different output Frequencies with Fref=150 kHz

<b>D</b>	<b>P</b> (N=20)	<b>S</b> (N=20)	<b>Fout</b> (MHz)
2681	1000 0110	000001	402.15
2683	1000 0110	000010	402.45
2685	1000 0110	000101	402.75
2687	1000 0110	000111	403.05
2689	1000 0110	001001	403.35
2691	1000 0110	001011	403.65
2693	1000 0110	001101	403.95
2695	1000 0110	001111	404.25
2697	1000 0110	010001	404.55
2699	1000 0110	010011	404.85
2773	1000 1010	001101	415.95
2860	1000 1110	010100	429.00
2940	1001 0010	010100	441.00
3027	1001 0111	000111	454.05

TABLE 3.7. Division ratio D for different output Frequencies with Fref=100 kHz

<b>D</b>	<b>Fout</b> (MHz)	<b>D</b>	<b>Fout</b> (MHz)
4011	401.1	4051	405.1
4012	401.2	4052	405.2
4013	401.3	4053	405.3
4014	401.4	4054	405.4
4015	401.5	4055	405.5
4016	401.6	4056	405.6
4017	401.7	4057	405.7
4018	401.8	4058	405.8
4019	401.9	4059	405.9

The values of P and S are shown in Table 3.6. Since a 20/21 dual modulus scalar divider is used in the pulse swallow counter, the value of N is fixed at 20. To achieve a division ratio of D equal to 2681 for an input reference frequency of 150 kHz with N equal to 20, the value of P is 134 and the value of S is 1 for the output to be at 402.15 MHz. Hence 8 bit wide P[7:0] is 10000110, 6 bit wide S[5:0] is 000001.

Figure 3.22 shows the input frequency of 406 MHz to the pulse swallow divider. Figure 3.23 is the output for division ratios of 1388 and 1372. Figure 3.24 shows the division ratio of pulse swallow divider for 1388 and 1372 for the dual modulus prescaler N (20), the program counter P (68), and the swallow count division ratio changing from S (28) to S (12). Similarly, Figure 3.25 shows the division ratios of 4068 and 4052 for N (20), P (202) and the swallow count division ratio changing from S (28) to S (12). The division ratio waveform is derived by dividing the input frequency by the output frequency.

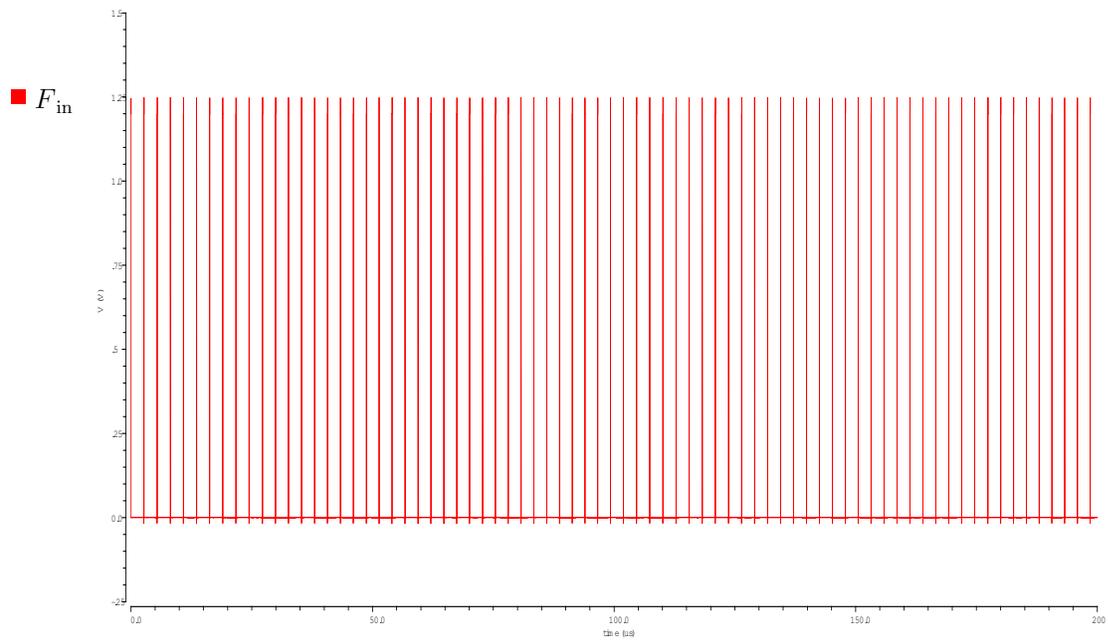


FIGURE 3.22. Input Frequency to the divider

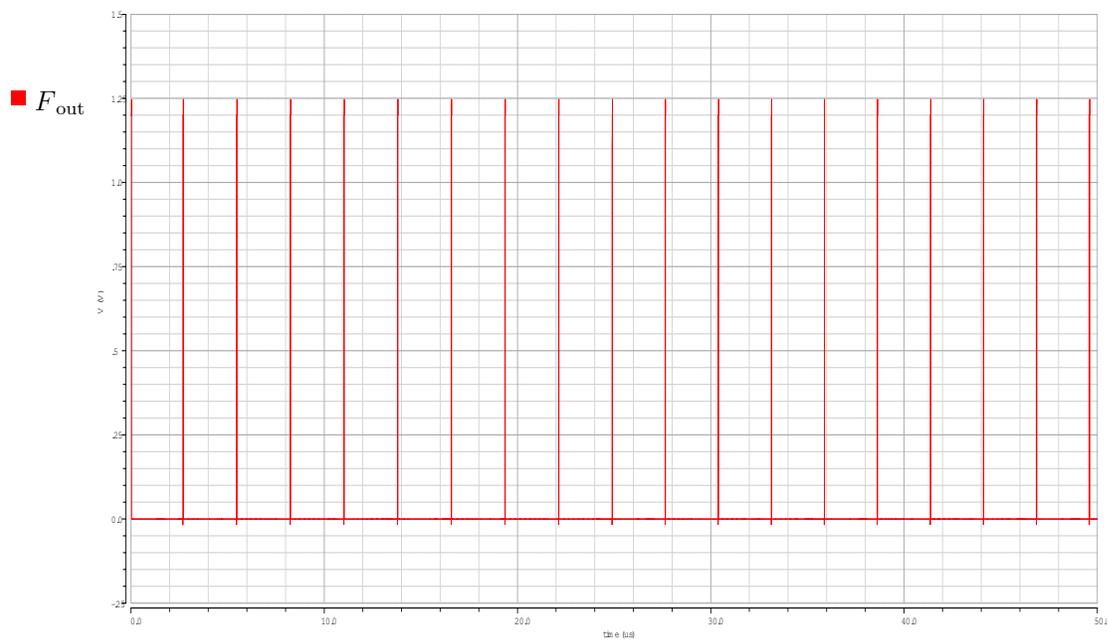


FIGURE 3.23. Output Frequency of the divider

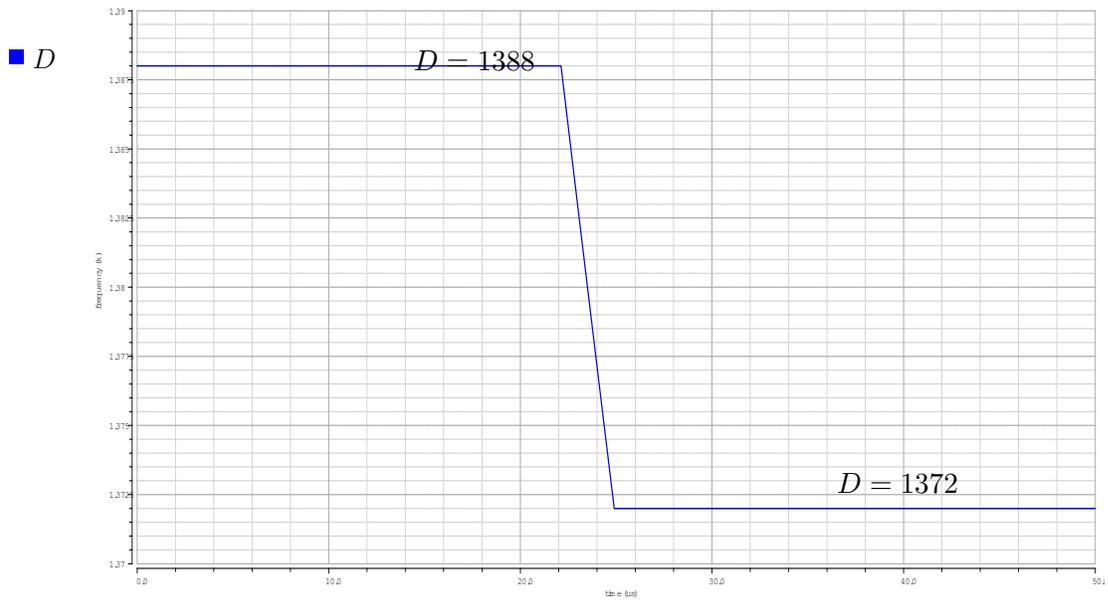


FIGURE 3.24. Waveform with different Division Ratio of 1388 and 1372

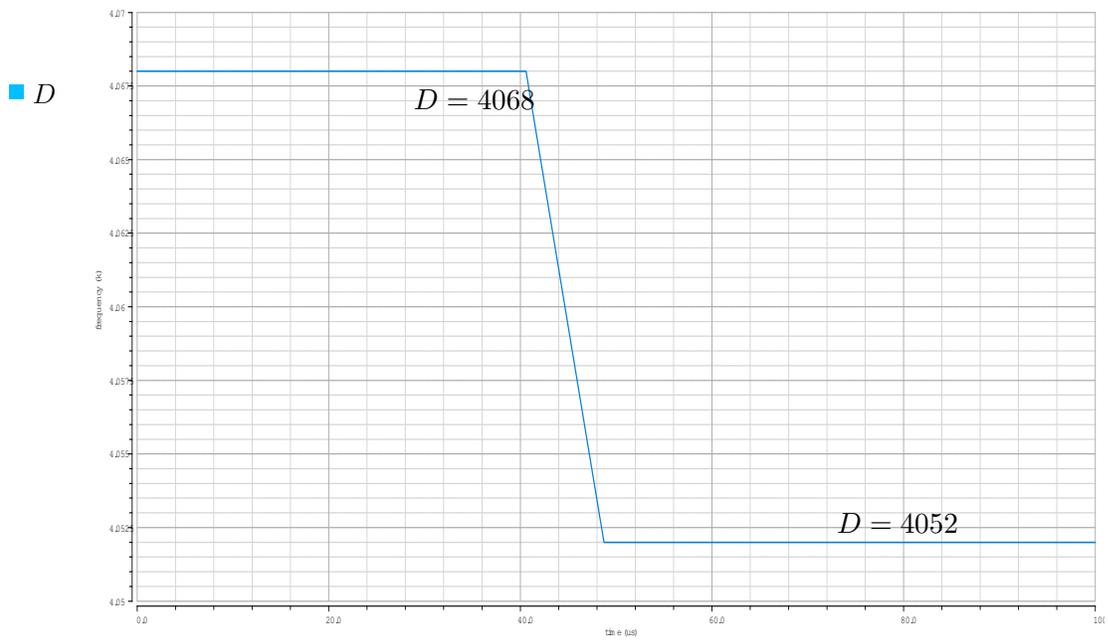


FIGURE 3.25. Waveform with different Division Ratio of 4068 and 4052

The Figure-of-merit (FOM) for the proposed divider design is defined as the ratio of power consumed and the highest operational frequency. The FOM of the proposed divider is at  $0.074 \mu\text{W}/\text{MHz}$  which is significantly better than the results reported in [35–40]. The comparison is illustrated in Table 3.8.

TABLE 3.8. Divider Design Comparison

<b>Reference</b>	<b>Process CMOS</b> (nm)	<b>Power supply</b> (V)	<b>Power</b> ( $\mu\text{W}$ )	<b>Operation Frequency</b> (MHz)	<b>FOM<sub>pwr</sub></b> ( $\mu\text{W}/\text{MHz}$ )
This work	180	1.2	30	406	0.074
[35]	130	0.7	210	200-1000	0.247
[36]	180	1.8	540	440	1.230
[37]	180	1.5	3200	1700	1.880
[38]	180	1.5	3230	3500	0.0923
[39]	180	1.8	2600	2400-2500	1.080
[40]	180	1.8	3.01	500-3500	0.860

### 3.3. VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator (VCO) is the heart of the PLL. It determines the spectrum purity of the whole transmitter. Most of the power consumed by PLL can be attributed to VCO. VCO's can be built using LC tank or ring oscillators (RO). Phase noise of LC tank VCOs is typically low compared to that of RO based VCOs and the spectrum of output is better in terms of spurious signals attenuation in the case of LC tank oscillator.

The disadvantages of the LC type VCO is its large area on die and potentially high power consumption. It has been shown that the RO VCO will consume 450 times the current of the LC VCO in order to achieve the same phase noise performance, even when quality factor (Q) of the LC tank is as low as 3 [41, 42]. The output of LC tank oscillator is small signal sine wave sitting on top of the VDD. VCO with LC tank oscillator require extra circuitry to bias the output of the VCO to get maximum efficiency out of the power amplifier. RO based VCO provides a rail-to-rail output sine waveform. However phase noise requirements for the PLL in the MedRadio band is less stringent, so RO is a better trade-off for the VCO from the area and power perspective.

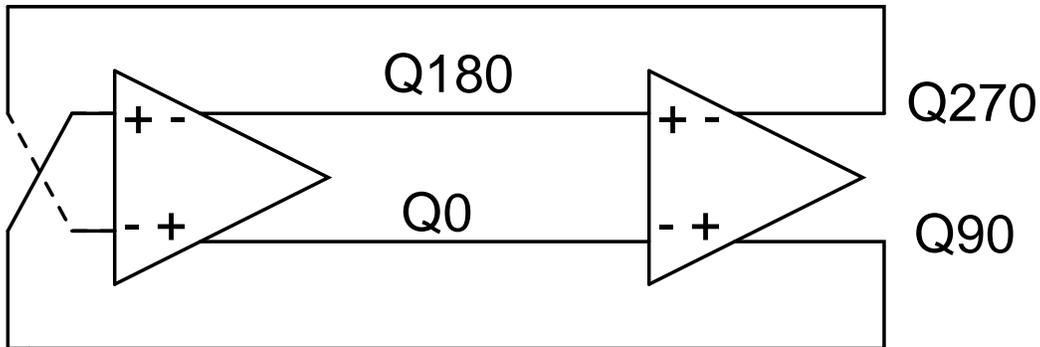


FIGURE 3.26. Block diagram of the Oscillator

Similar to the design reported in [31, 43], two ring oscillators are connected back to back with inverted output to form the required VCO for the proposed frequency synthesizer with quadrature output as shown in Figure 3.26.

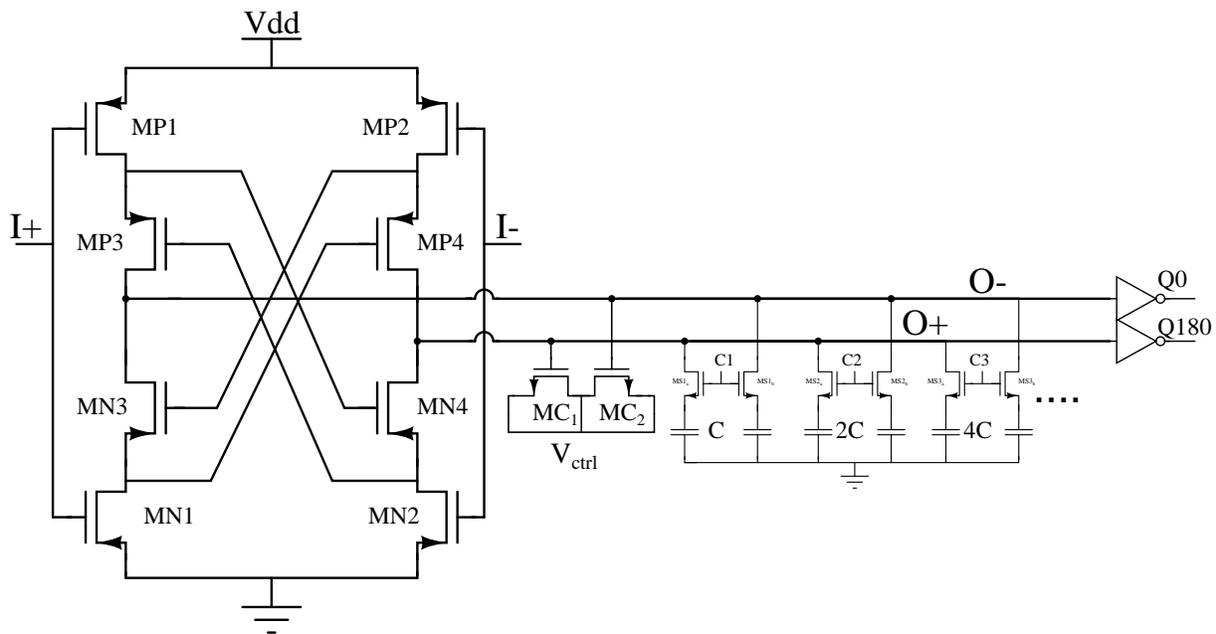


FIGURE 3.27. Circuit Schematic of the Voltage Controlled Oscillator

The ring oscillator circuit is shown in Figure 3.27. The control voltage  $V_{ctrl}$  is used to vary the capacitance of the varactors  $MC_1$  and  $MC_2$ . The varying capacitance of the varactor is used to dither the frequency of the VCO for the change in the division ratio  $D$  of the pulse swallow counter to cover the different channels of the MedRadio band of 401-457 MHz. Six external signals  $C_1$  to  $C_6$  are used to control the digital switches for coarse calibration of the VCO to cover the entire MedRadio band of 401-457 MHz.

The PLL output frequency can vary in the steps of the reference frequency by varying the integer division ratio of the synchronous integer- $N$  divider with different combinations of the digital signals  $P[7:0]$  and  $S[5:0]$ . The input reference frequencies can be 100 kHz, 150 kHz, and 300 kHz. The division ratio accordingly can be selected between 4060 to 1335 to achieve

all the output frequencies within the MedRadio band of 401-457 MHz with all the input reference frequencies.

Since the VCO is optimized to consume low power, the area of the transistors is bound to be less with minimum length of 180 nm. The VCO frequency will vary under process voltage temperature (PVT) variations. The effect of process variations will be dominant due to small sizes of the transistors as discussed, hence the compensation capacitor bank to tune the VCO is needed.

The deviation of frequency of the proposed VCO is shown in Figure 3.28, using the Monte-Carlo simulations with 80 data points. The standard deviation ( $\sigma$ ) of the frequency of the VCO is 42.2 MHz. The capacitance bank connected to the output is used to account for the process and temperature variations of the PLL. Through calibration, the capacitive bank is intended to adjust the output frequency to fall within the intended MedRadio band. The capacitance bank allows the VCO to cover frequencies up to  $+\sigma$  and  $-\sigma$ , above and below the MedRadio band frequencies respectively. This will significantly improve the yield of the proposed transmitter. Six external signals C1 to C6 are used to control the digital switches for coarse calibration of the VCO frequency. The control voltage  $V_{ctrl}$  is used for the fine calibration of the VCO frequency for a fixed output capacitance from the capacitive bank.

Figure 3.29 shows the output waveform of the VCO at different temperature and corners. It can be seen that the frequency of the VCO varies at different temperature and corners, which is similar to the Monte-Carlo simulation but the transient waveforms are shown. Hence, the compensation capacitor bank is required to tune the VCO frequency to the desired frequency range of 401-457 MHz.

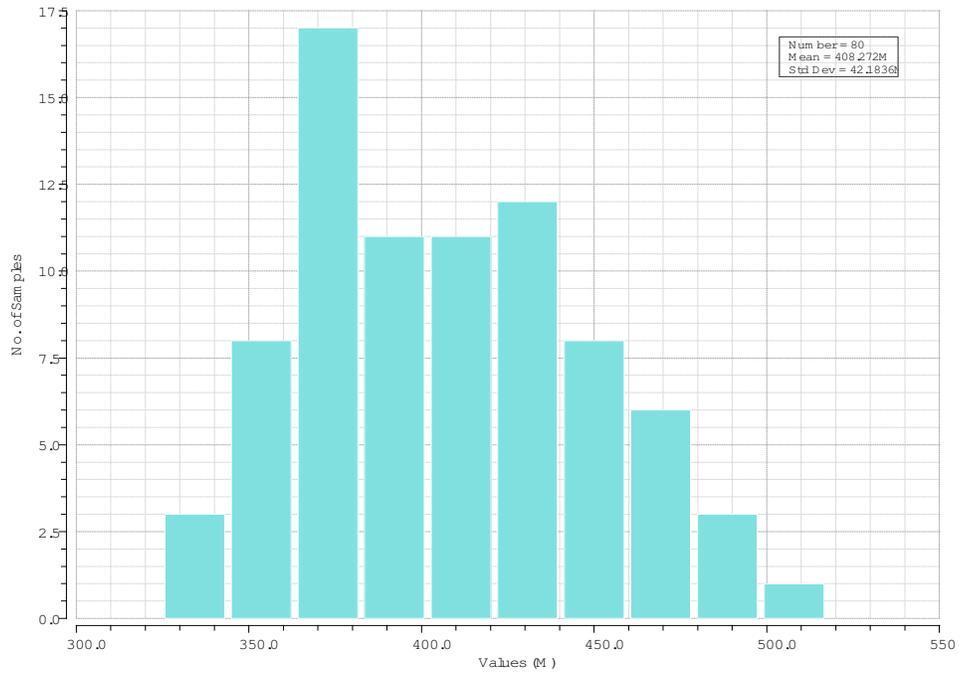


FIGURE 3.28. Monte-Carlo simulation for the frequency deviation of the VCO

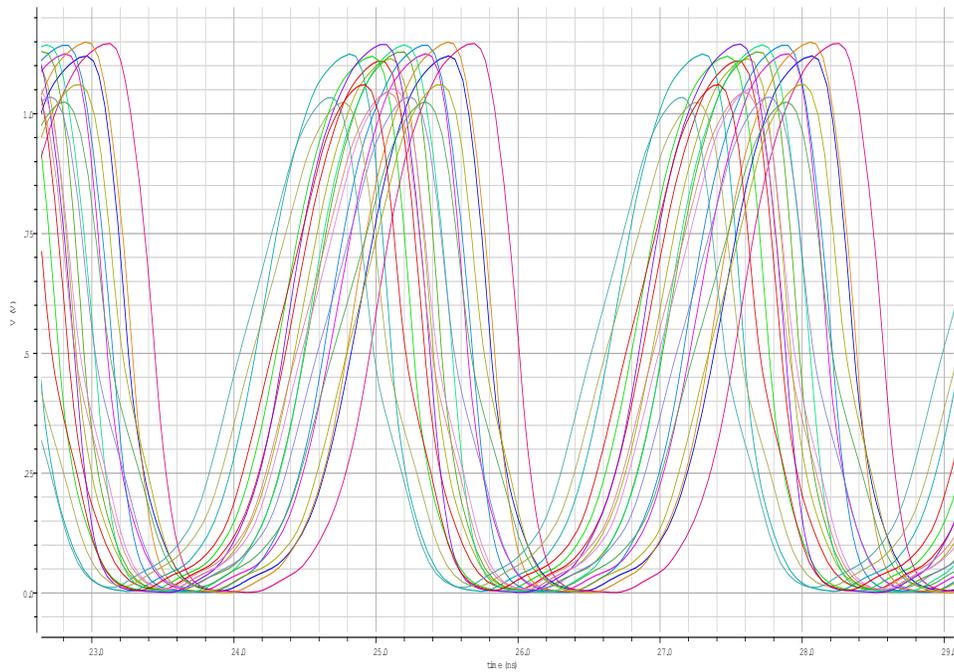


FIGURE 3.29. Transient analysis of the VCO at different corners and temperature

The gain of the VCO is 24 MHz/V as shown in Figure 3.30. The gain is chosen low to avoid spurs on the output of the VCO. The higher the gain of VCO, higher the effect of the noise on the  $V_{ctrl}$  to the output of the VCO in the form of frequency drift. The lower the gain of VCO, the lower the range of output frequencies that a VCO can cover during the sweep of  $V_{ctrl}$  from 0 to VDD. Therefore, a large capacitance bank is required. In order to cover all the frequencies in the band of 401-457 MHz, the VCO is designed to work at high frequencies and a capacitance bank is used to tune the frequency of the VCO to fall within the required MedRadio band with the load.

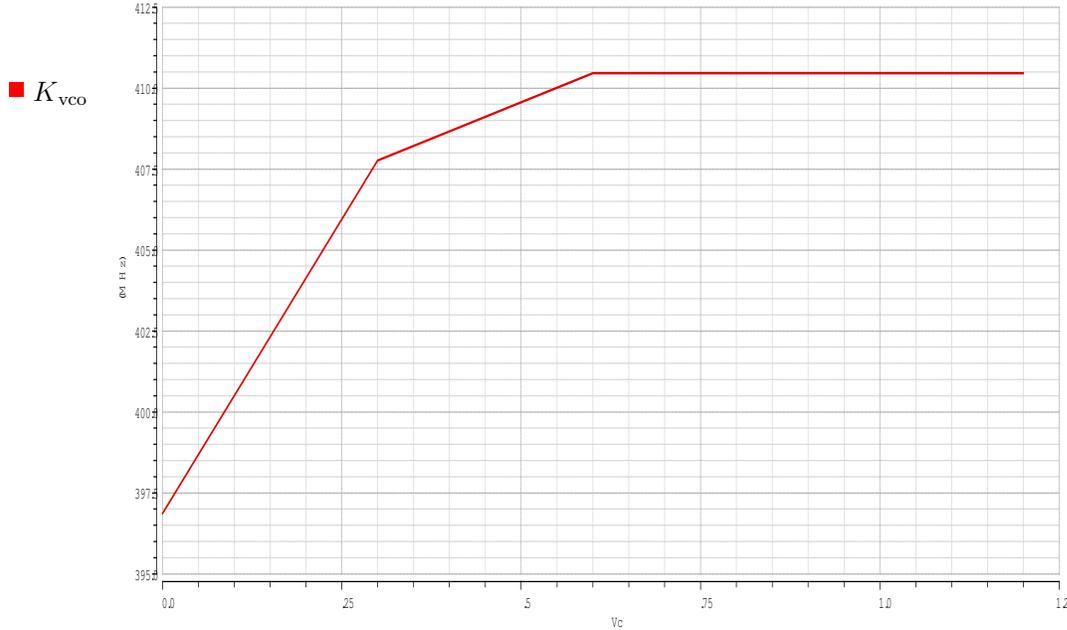


FIGURE 3.30. Gain of the VCO ( $K_{vco}$ )

The VCO is designed to work at the required frequency of 401 MHz (mainly to cover MICS band) at the slow-slow corner and at 40°C. In this corner the load capacitor bank is turned off. When the VCO is simulated at fast-fast corner and at 20°C the output frequency is high nearly 850 MHz. Although it is desirable to cover all the possible frequencies due to PVT variations, the highest frequency VCO can cover is 550 MHz at typical-typical at 27°C

to keep the power consumption low and capacitor bank small. The capacitor bank has to be turned on to maximum load to make the output frequency fall in the required range of 401-457 MHz. The reason behind choosing temperature range of 20-40°C, is the fact that the human body usually operates in the temperature range of 30-40°C.

Figure 3.31 shows the results of the oscillator (VCO) using periodic steady state (PSS) analysis simulation as described in Appendix D. The PSS show the settling of the VCO at a frequency in 401-406 MHz for MICS band working, with higher order harmonics suppression greater than 20 dB. Phase Noise of the VCO is as shown in 3.32 from the PSS analysis, followed by pnoise analysis simulation in the cadence software. The simulated phase noise of the extracted VCO is at  $-95 \text{ dBc /Hz @ 1 MHz}$  relative to the center frequency.

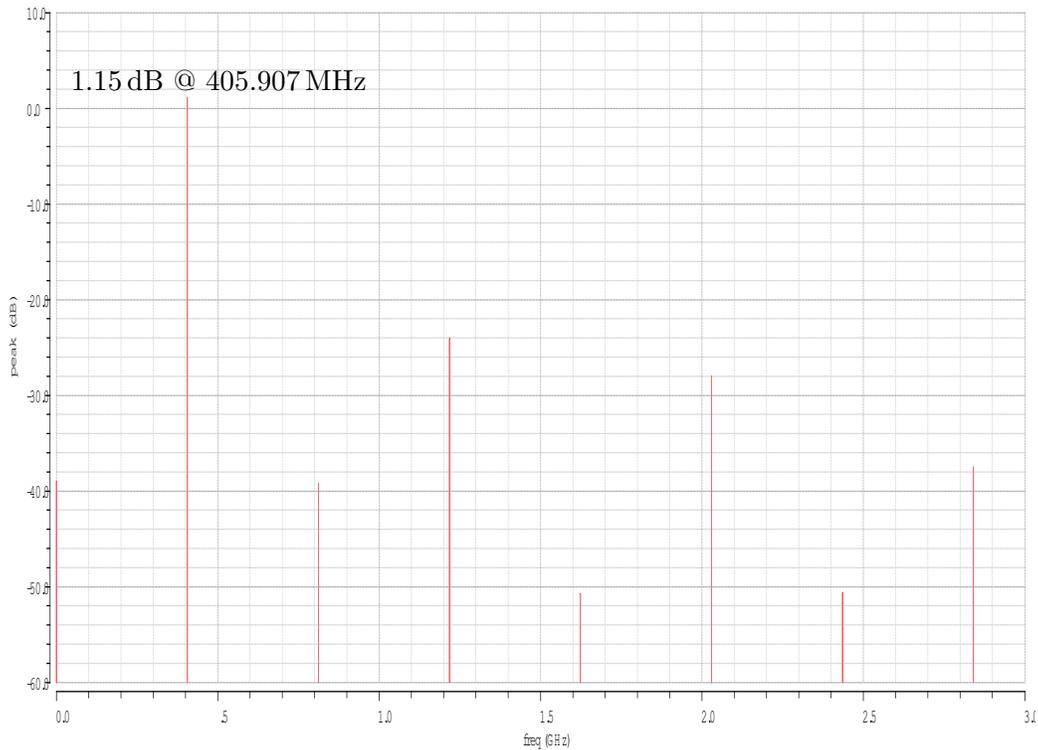


FIGURE 3.31. Periodic Steady State output of the VCO

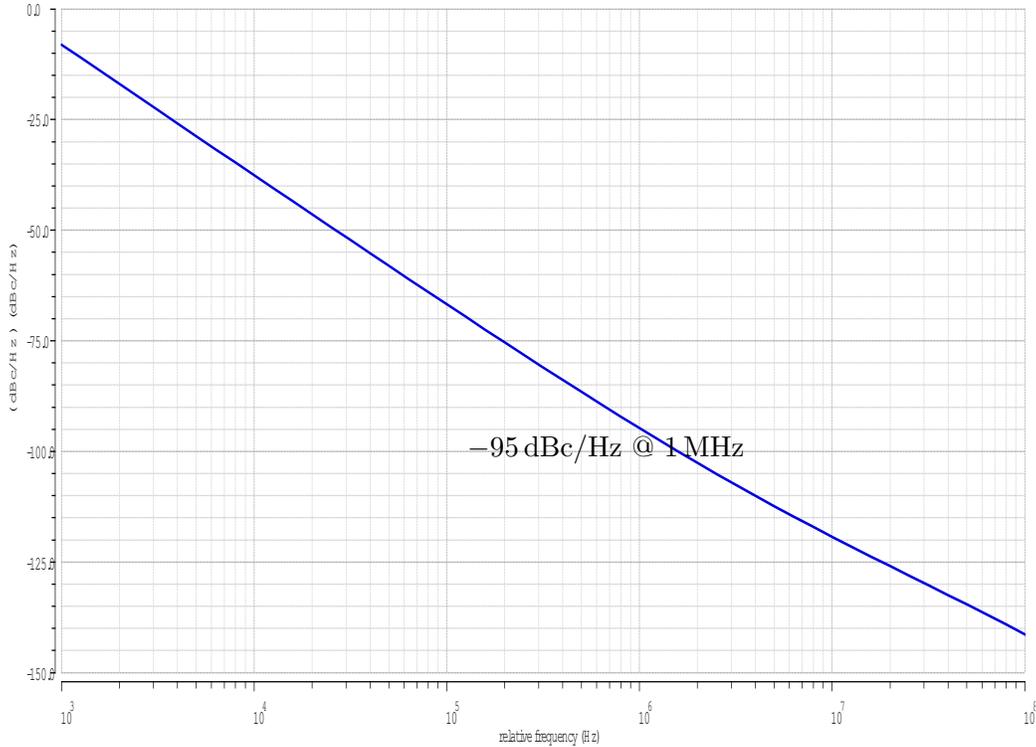


FIGURE 3.32. Noise profile of the VCO

### 3.4. MODULATION SCHEME AND PASSIVE MIXER

The passive mixer used in this transmitter design is shown in Figure 3.33 for the modulation of the data signal. A 4:1 multiplexer serves as the mixer for the proposed transmitter design. A simple complementary transmission pass gate is used as the switching element in the mixer. The quadrature output of the PLL is the input to the four terminals of the mixer. The encoded data signal is used as the select lines for the mixer. The output of the mixer is fed to the power amplifier (PA).

A quadrature phase shift keying (QPSK) modulation scheme is achieved with this mixer. The QPSK enables us to transmit data with less bit error rate (BER) for the same output

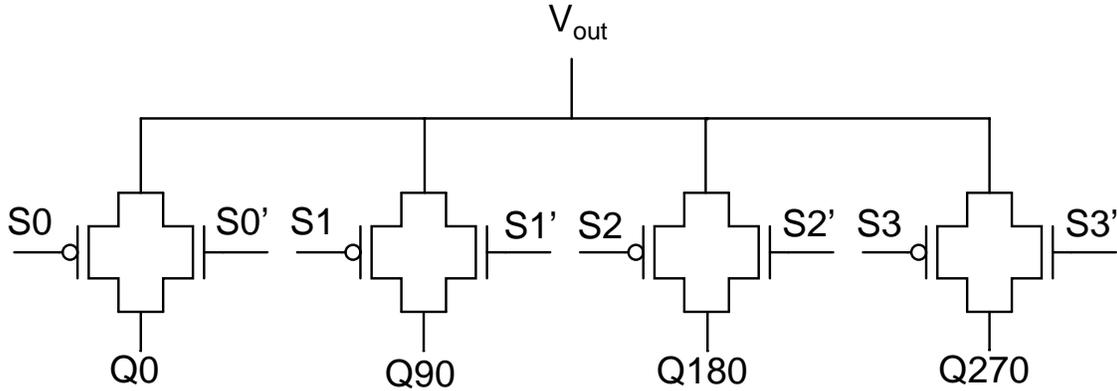


FIGURE 3.33. Circuit Schematic of the Passive Mixer

power as described in [29]. The zero active power consumption of the passive mixer allows the total power consumption of the proposed transmitter stay low.

Careful sizing of transistors in the passive mixer was carried out to balance size, distortion and performance. Figure 3.34 shows the rise and fall times of the schematic of mixer for the length  $L$  of 180 nm. The low  $W/L$  presents a distorted waveform at the input of the power amplifier (PA). The high  $W/L$  presents high capacitive load to the fixed VCO buffer causing the rise and fall time at the mixer input to deteriorate. The mixer size is optimized to achieve a fast transient waveform at the input of the PA, for a chosen output buffer of the VCO. Optimized rise and fall times also prevents the power amplifier short circuit current from being excessively high.

The capacitance between gate and source ( $C_{gs}$ ) is higher for MOS-FET device with large gate width. The higher the  $C_{gs}$ , the larger is the feed-through signals to the mixer output terminal (drain). Hence, the optimized value of  $W/L$  in Figure 3.34 minimizes the feed-through of the data signals to the output and maintain the spurious frequency harmonics below the allowed levels in MedRadio band for a given data rate.

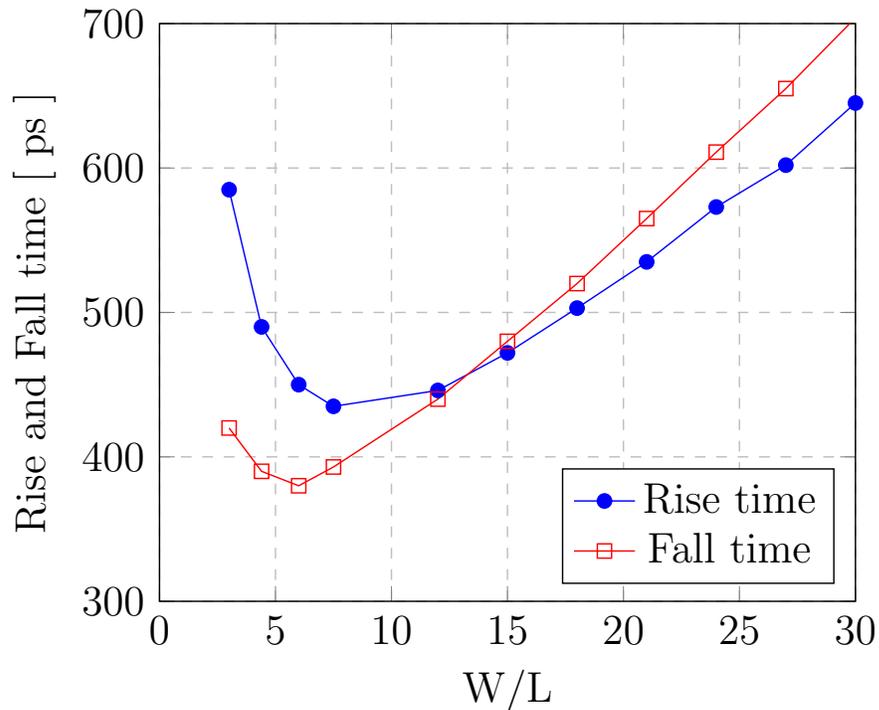


FIGURE 3.34. Variation of rise and fall times with W/L

### 3.5. POWER AMPLIFIER

The class-D power amplifier (PA) used for the proposed transmitter is shown in Figure 3.35. The class-D PA was chosen for its power efficiency and simplicity. The PA has a series capacitance  $C_2$  to block DC current to the output.

A standard commercial  $\pi$  aluminum (AL) bonding wire model is used for the resonant network assuming 8 mm long bonding wires. The parasitic components of the resulting  $\pi$  network that mimics the output pad is shown in Table 3.9. The parasitic resistance  $R_1$  and parasitic capacitance  $C_1$  of the bonding wire to the ground are very small compared to the load resistance and capacitance. They are ignored in the calculation of component values in the final RLC matching network.

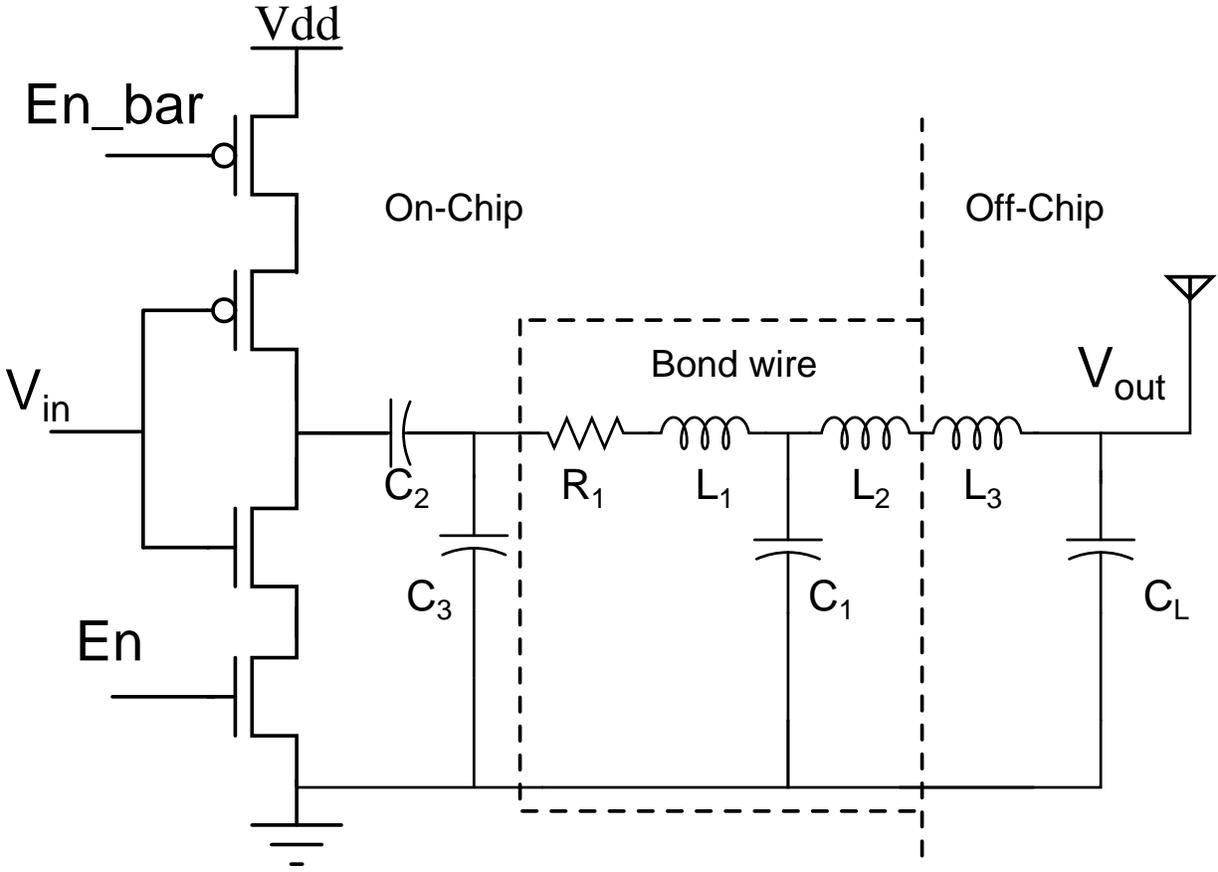


FIGURE 3.35. Schematic of the class-D Power Amplifier with antenna

TABLE 3.9. Bond wire and Bond pad parasitics

Parameter	Value
$R_1$	300 m $\Omega$
$L_1$	8 nH
$L_2$	1 nH
$C_1$	400 fF

The approximated  $\pi$  RLC is as shown in Figure 3.36. The resonant impedance matching network consists of  $C_3$ ,  $L_1$ ,  $L_2$ ,  $L_3$  and  $C_L$  to match the output impedance of the PA  $R_{in}$  to the antenna impedance  $R_{out}$  of 50 $\Omega$ . The capacitance  $C_3$  is designed such a way that

the parasitic capacitance of the bond-pad is absorbed into  $C_3$ ,  $L_3$  and  $C_L$  come from the PCB assembly board along with antenna. The resonant network's components  $L_3$  and  $C_L$  are off-chip to keep the die size small.

Both  $L_3$  and  $C_L$  can be tuned around 23 nH and 28.6 pF, respectively, to match the antenna impedance of  $50 \Omega$ . A switch is provided to turn off PA when the PLL is still in calibration state to avoid emission of the spurious frequencies.

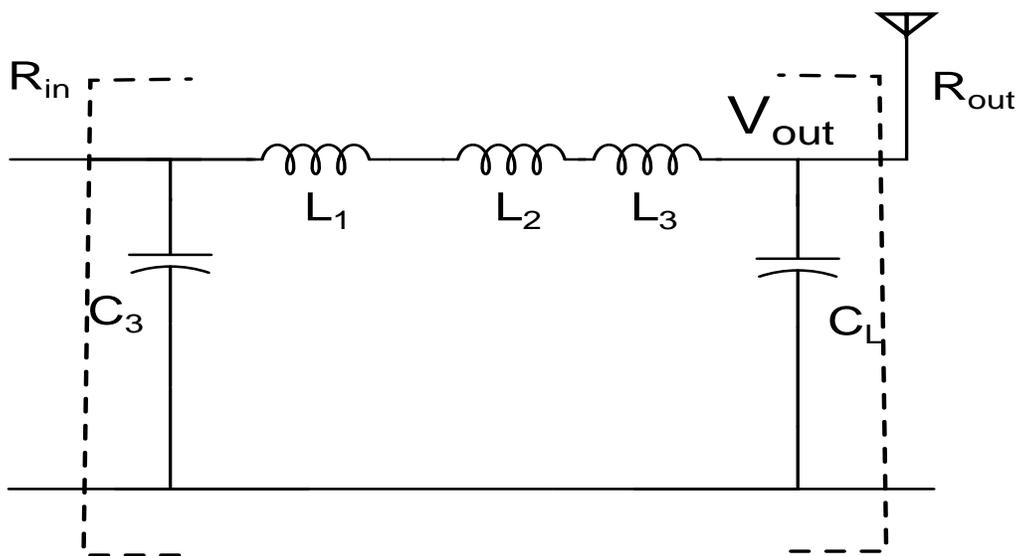


FIGURE 3.36. Schematic of the  $\pi$  RLC matching network

Figure 3.37 shows the power consumed by the PA for different Vdd with the variation of W/L of the PA. Figure 3.38 shows the power at the output of matching network, i.e. at the antenna. Various parameters of the power amplifier driving the output pad, the bond wire, the matching network and the antenna with impedance of  $50 \Omega$  for different supply voltages are illustrated in Table 3.10.

The power supply voltage Vdd of 1.2 V will result in same transmitter efficiency when compared to Vdd of 1.4 V, as in Figure 3.39 for an approximate effective width of  $3.5 \mu\text{m}$ . The power supply voltage of 1.2 V will reduce the total average power consumption of not

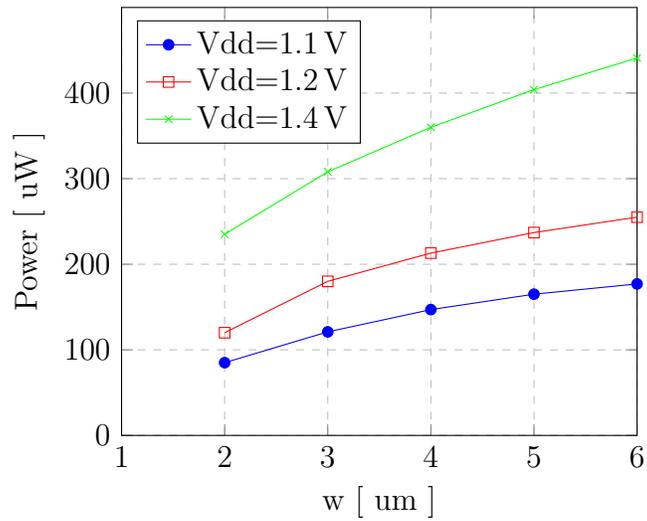


FIGURE 3.37. Power Consumption of PA as a function of PA transistor size with different Vdd

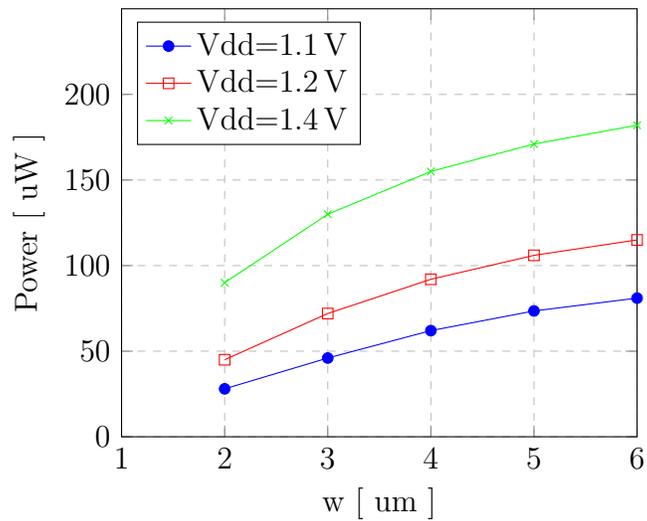


FIGURE 3.38. Output Power of PA as a function of PA transistor size with different Vdd

only the PA but also the frequency synthesizer. Hence, efficiency of the proposed transmitter increases and the reduced power consumption will also improve the energy consumed per bit of the transmitter.

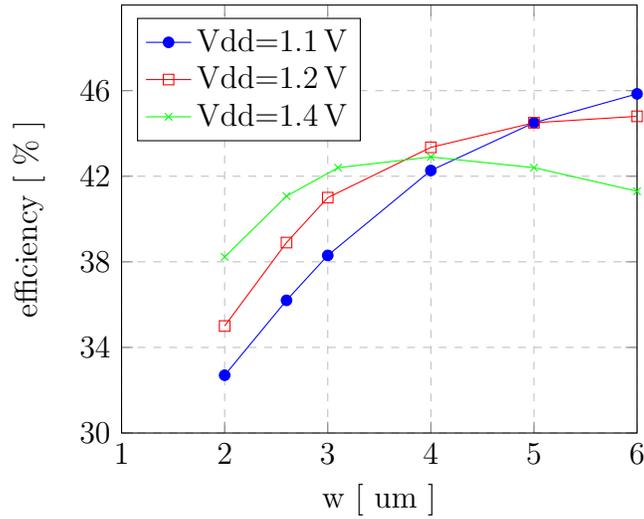


FIGURE 3.39. Efficiency of PA as a function of PA transistor size with different Vdd

The required output power will limit the minimum supply voltage even though power consumption is lower at low voltage is less, the overall efficiency of the transmitter takes a hit for the proposed design.

One of the disadvantage from higher supply voltage in the case of implantable medical devices is the high power output at the antenna as we observe from Table 3.10. The implantable devices are operated with constraints on the power consumed, due to the limited power sources in the implantable devices. The maximum power that can be emitted as per the FCC regulation is -16dBm. With a supply voltage of 1.2 V the output power is -11dBm. With the assumption of losses due to antenna as 5dB, power supply of 1.2 V will give output power of -16dBm. Even if a higher power supply is used the excess power at the antenna cannot and should not be emitted out of the transmitter. Hence, the power supply voltage of 1.2 V is a good choice for optimum efficiency of the transmitter and for low energy per bit transmitted for the proposed transmitter in the MICS and MMNs bands.

TABLE 3.10. Comparison of parameters for different Vdd

Vdd (V)	Power Consumed ( $\mu$ W)	V <sub>p-p</sub> (mV)	Power at antenna ( $\mu$ W)	Power at antenna (dBm)	PA efficiency %
1.1	140	155	60	-12.2	39
1.2	200	182	83	-10.8	41
1.4	340	240	144	-8.4	42

The electrical parameters of the frequency synthesizer used in the transmitter design were obtained by the calculations and extensive SPICE-level simulations. Table 3.11 lists some key electrical parameters.

TABLE 3.11. Summary of the PLL

Parameter	Value
C1	68.0 pF
C2	6.8 pF
C3	2.5 pF
R1	670.0 k $\Omega$
R3	470.0 k $\Omega$
I <sub>CP</sub>	15 $\mu$ A
K <sub>VCO</sub>	24 MHz/V
Loop Bandwidth	11.25 kHz
Phase margin of PLL	52°
Phase noise of VCO	-95 dBc /Hz @ 1 MHz
Settling time	20 $\mu$ s
Spurious frequency attenuation	-27 dB @ 150 kHz

## CHAPTER 4

# SILICON IMPLEMENTATION AND SIMULATION RESULTS

### 4.1. SILICON IMPLEMENTATION

The layout of the proposed transmitter is implemented in a 180nm CMOS process. Figure 4.1 shows the layout of the phase frequency detector of the frequency synthesizer surrounded by p and n guard rings to better isolate the digital parts from the analog parts from noise coupling perspective. The noise coupling and the parasitics in the case of PFD will effect the locking of the PLL.

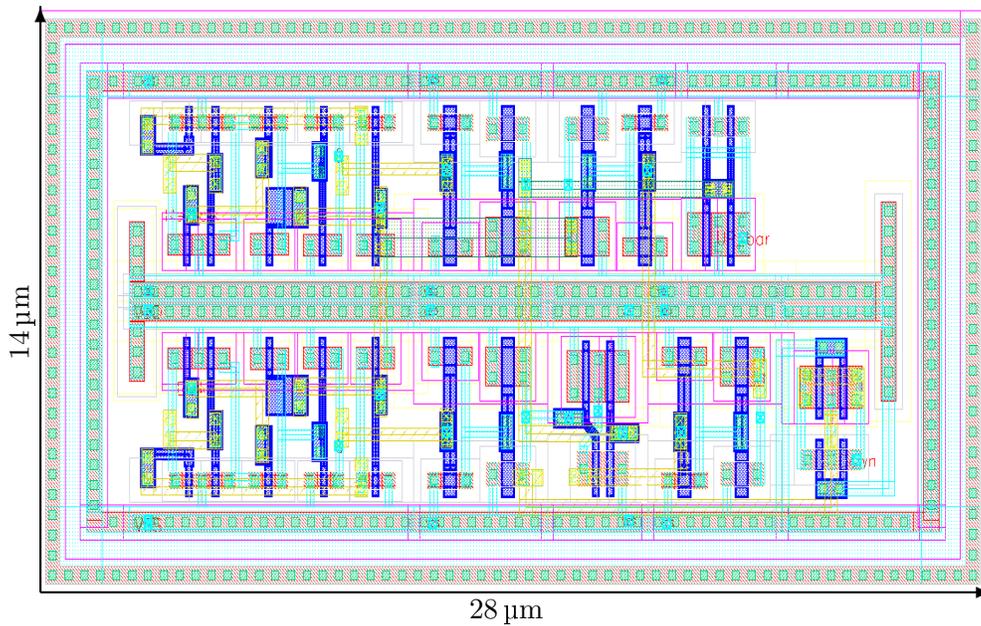


FIGURE 4.1. Layout of the Phase frequency Detector

All the digital parts of the design are implemented using a standard cell library and synthesized manually. Table 4.1 lists the cells in the standard cell library and their sizes. All the standard cell library gates are optimized with appropriate choice of pitch of the gates. The height of TSPC-DFF shown in Figure 4.2, is kept equal to that of the standard pitch of the digital gates. Single contacts are used in places for the design of TSPC-DFF at the cost of reliability to reduce the parasitic capacitance and improve the speed. The speed improvement will reduce the jitter due to the divider, hence that of the PLL.

TABLE 4.1. Standard Cell Library gates and sizes

<b>Digital Gate</b>	<b>Size</b>
INV 1x	2 $\mu\text{m}$ x 5.4 $\mu\text{m}$
INV 2x	3 $\mu\text{m}$ x 5.4 $\mu\text{m}$
NAND2	3 $\mu\text{m}$ x 5.4 $\mu\text{m}$
AND2	4 $\mu\text{m}$ x 5.4 $\mu\text{m}$
AND3	5 $\mu\text{m}$ x 5.4 $\mu\text{m}$
XOR2	6.5 $\mu\text{m}$ x 5.4 $\mu\text{m}$
DFF	9 $\mu\text{m}$ x 5.4 $\mu\text{m}$

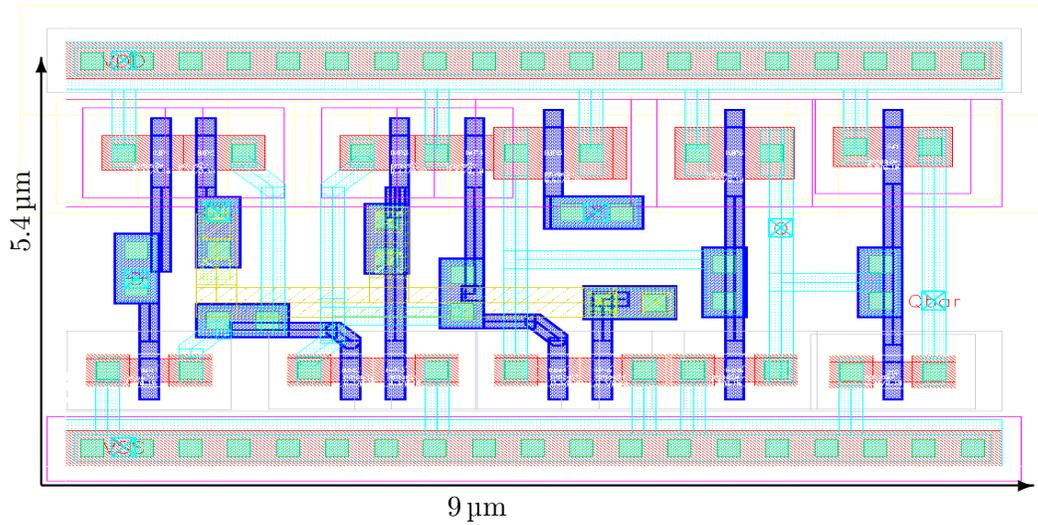


FIGURE 4.2. Layout of the TSPC D flip-flop

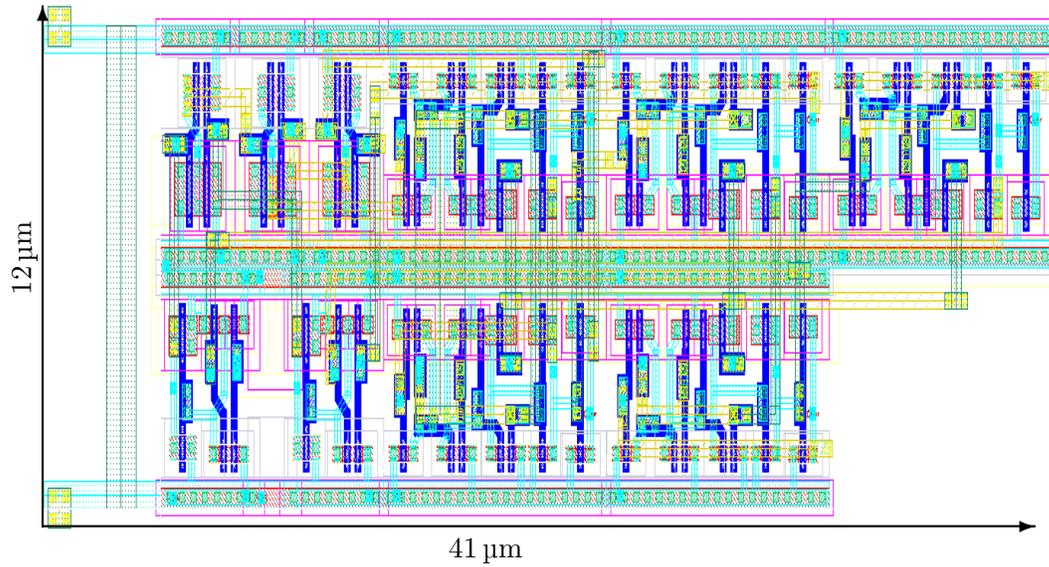


FIGURE 4.3. Layout of the Dual Modulus Prescaler

The individual layout of Dual Modulus Prescaler is shown in Figure 4.3. It is designed to fit into the swallow counter, hence making the divider layout as square as possible.

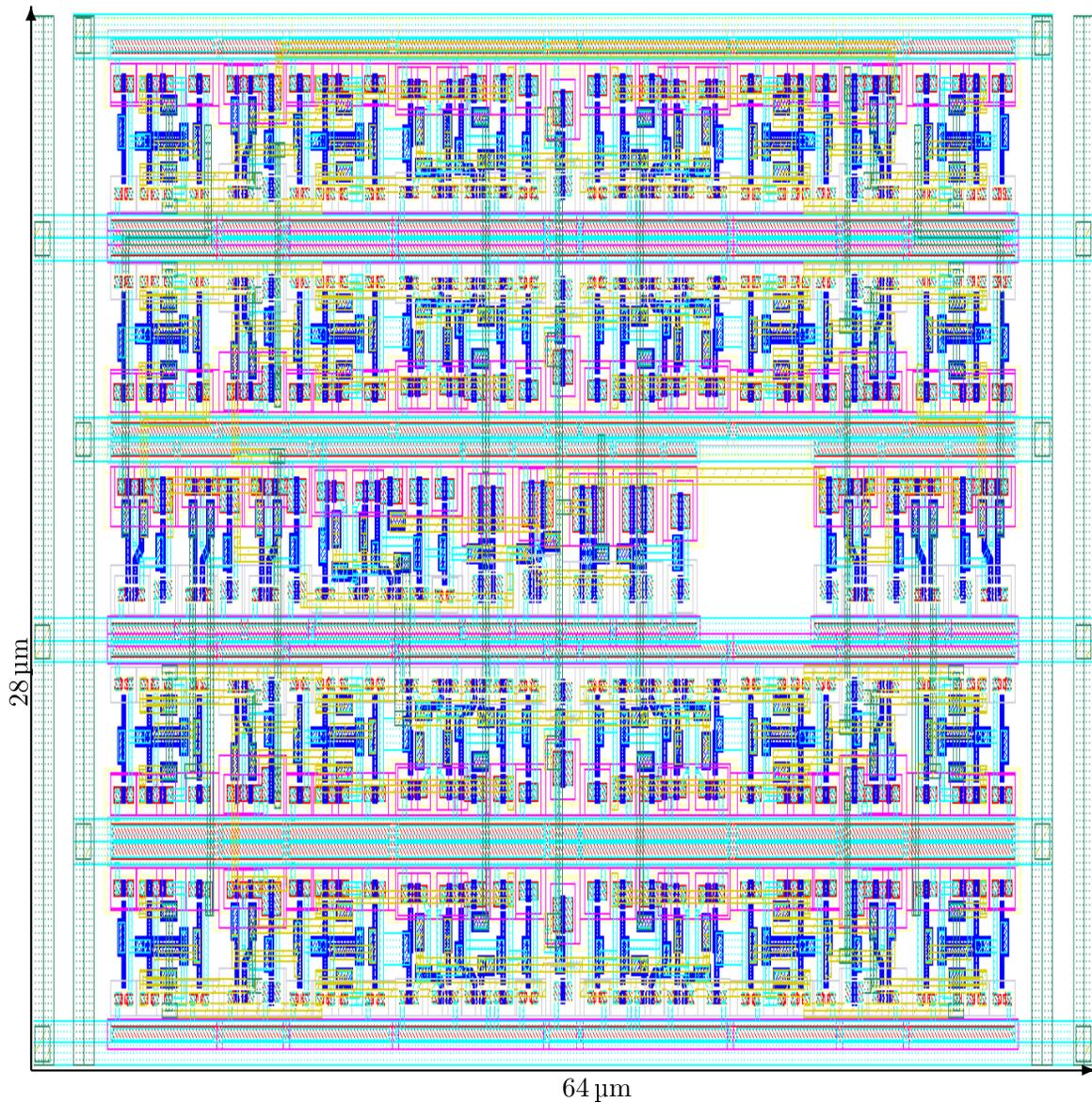


FIGURE 4.4. Layout of the Program Counter

Layout of the programmable counter and the programmable swallow counter are shown in Figures 4.4, and 4.5 respectively. These counters are designed manually as individual blocks to be square, to utilize the core area of the overall layout in more efficient manner. The empty space at top-right corner in Figure 4.5 is reserved for the dual modulus prescaler as shown in Figure 4.3.

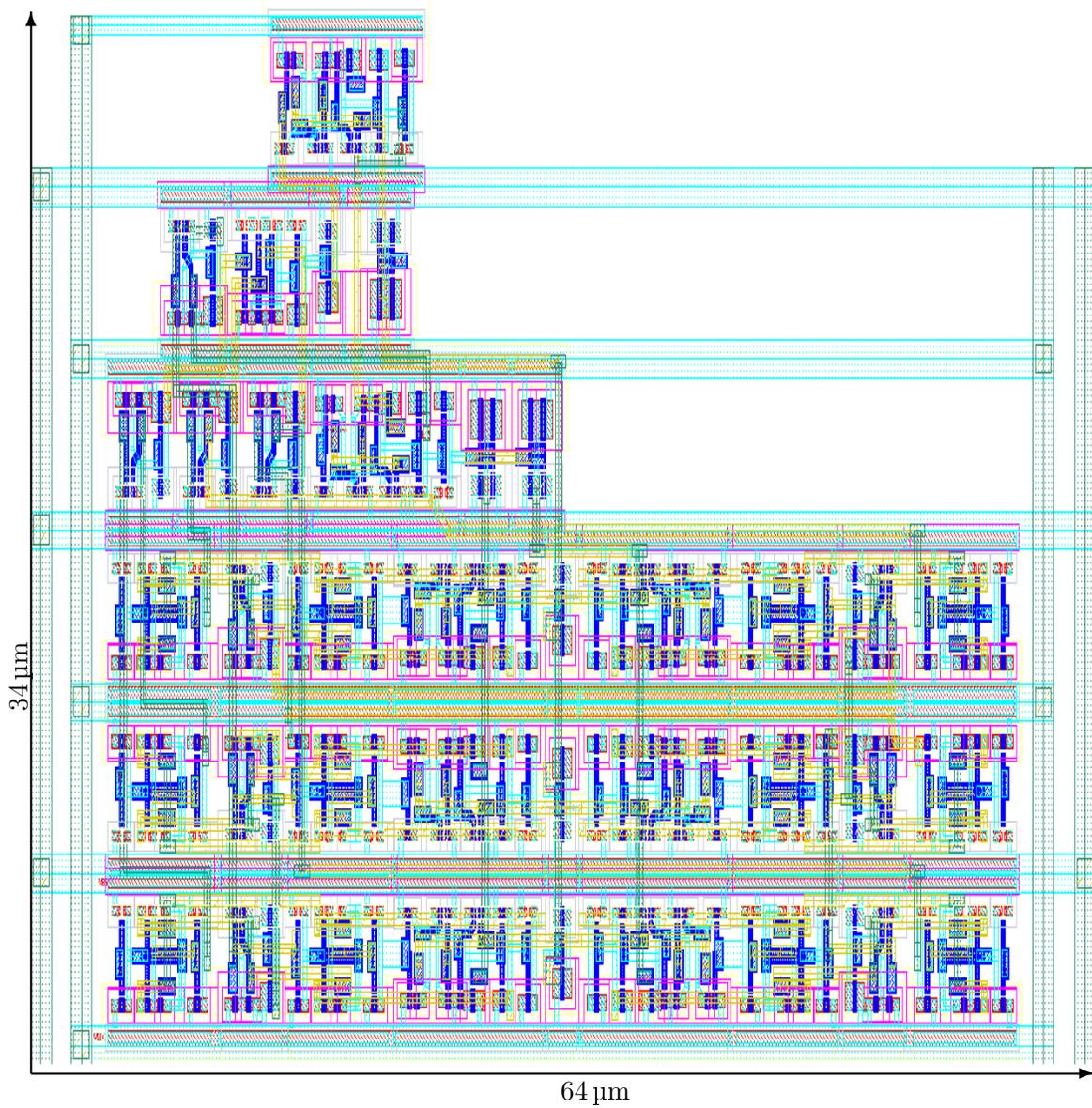


FIGURE 4.5. Layout of the Swallow Counter

Layout of the programmable synchronous pulse swallow counter is shown in Figure 4.6. The layout is designed to fit in the whole transmitter architecture. This counter is surrounded by p and n guard rings. It is routed with a  $1\ \mu\text{m}$  wide alternating positive and negative power supply lines, in addition to the enclosed power rails.

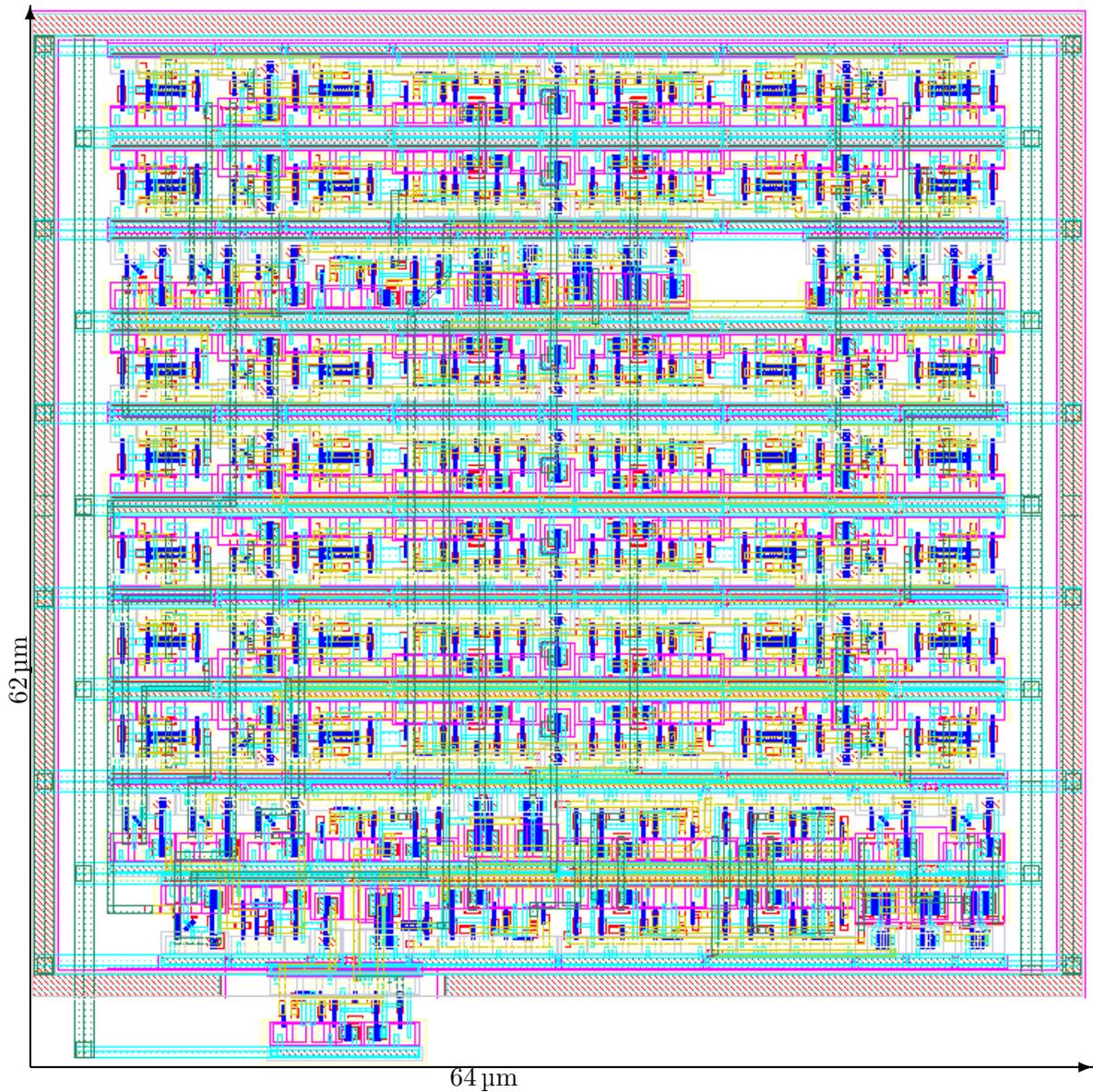


FIGURE 4.6. Layout of the Pulse Swallow Counter

Figures 4.7 and 4.8 show the layout of the VCO and the capacitor bank. Steps followed in the layout process are single contact to reduce the self loading of the VCO with extra metal, the layout is as compact as possible with minimum distance between the layers, and the routing of the VCO and the capacitor bank is minimized to optimize the signal spectrum purity at a given power consumption. The varactors are included in the VCO layout to reduce further routing parasitics of the outputs of the VCO. Dummy FETs are added to all

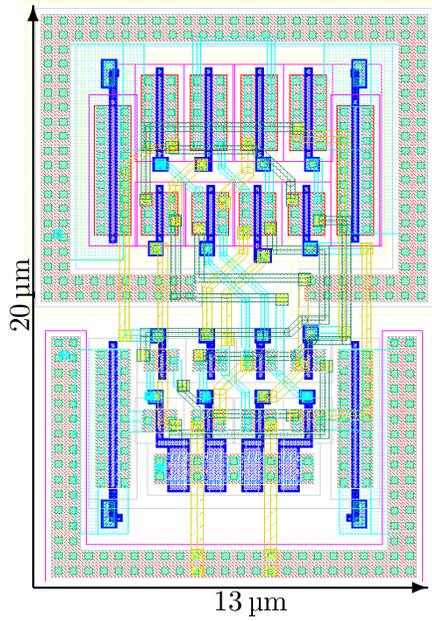


FIGURE 4.7. Layout of the VCO

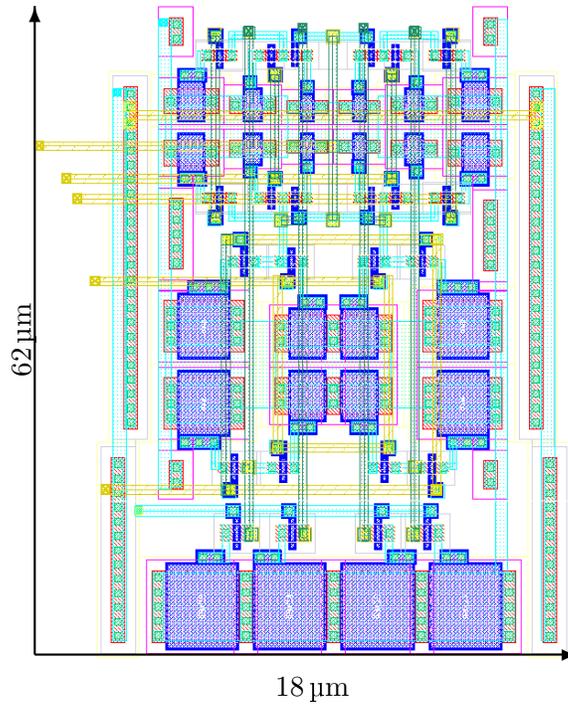


FIGURE 4.8. Layout of the Capacitive bank

the components of the VCO to improve the yield of the targeted frequencies of the VCO. The efficient floor planning of the VCO and capacitor bank significantly reduced the power consumption of the VCO, hence the low power consumption of the transmitter.

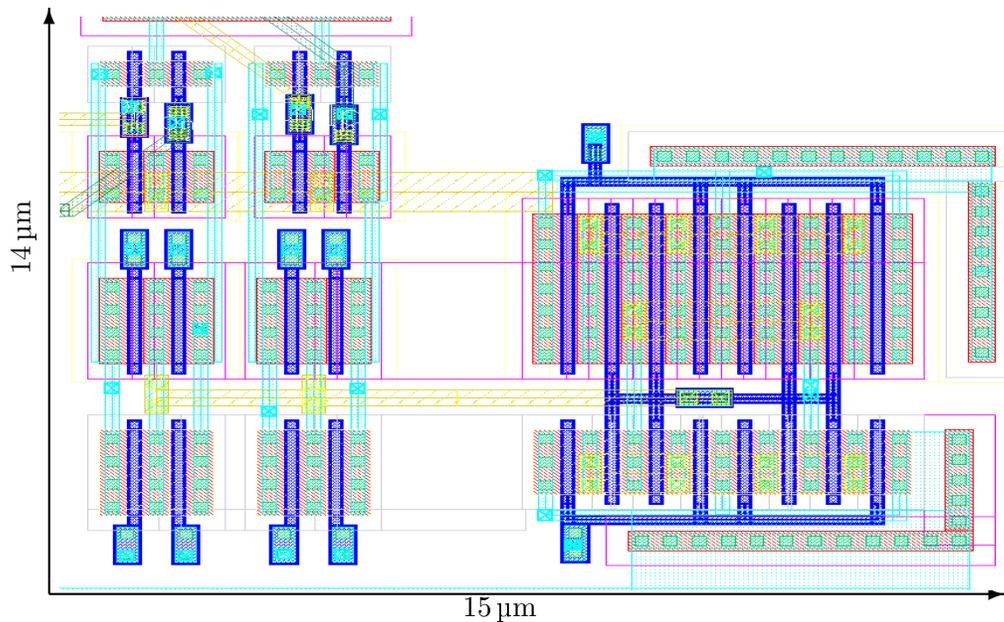


FIGURE 4.9. Layout of the Buffers, the Mixer and the Power Amplifier

Another aspect of optimization is the layout for the mixer. The mixer is placed as closely as possible to the outputs of buffers from the frequency synthesizer, the power amplifier is close to the mixer, to prevent any parasitic and stray capacitance effecting the output spectrum. Optimization prevents the output spectrum spreading over to the adjacent bands, therefore higher data rate can be achieved.

Figure 4.9 shows the layout of the PA, the mixer, and the buffers driving the mixer. Sources are abutted together wherever possible as in the source of buffers, passive mixer. The source and drain in the power amplifier are abutted together. The transistors are surrounded by the respective guard rings.

The layout of the loop filter, and the charge pump of the frequency synthesizer are shown in Figures 4.10, and 4.1. Capacitor and resistors are laid out in common centroid fashion for the loop filter. The Charge pump is enclosed in double guard rings.

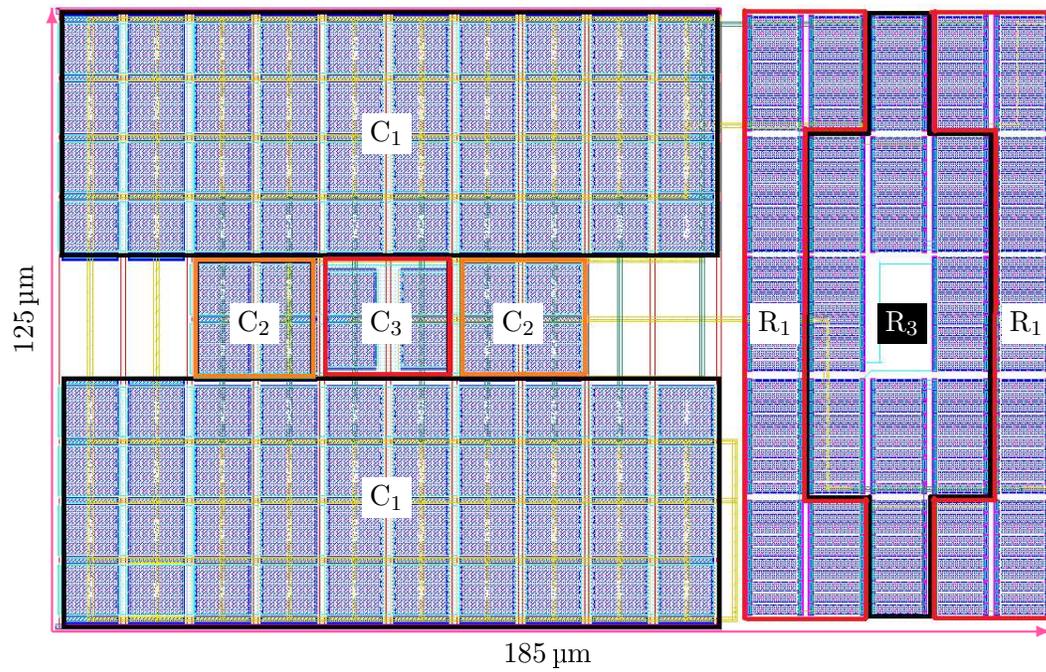


FIGURE 4.10. Layout of the loop filter

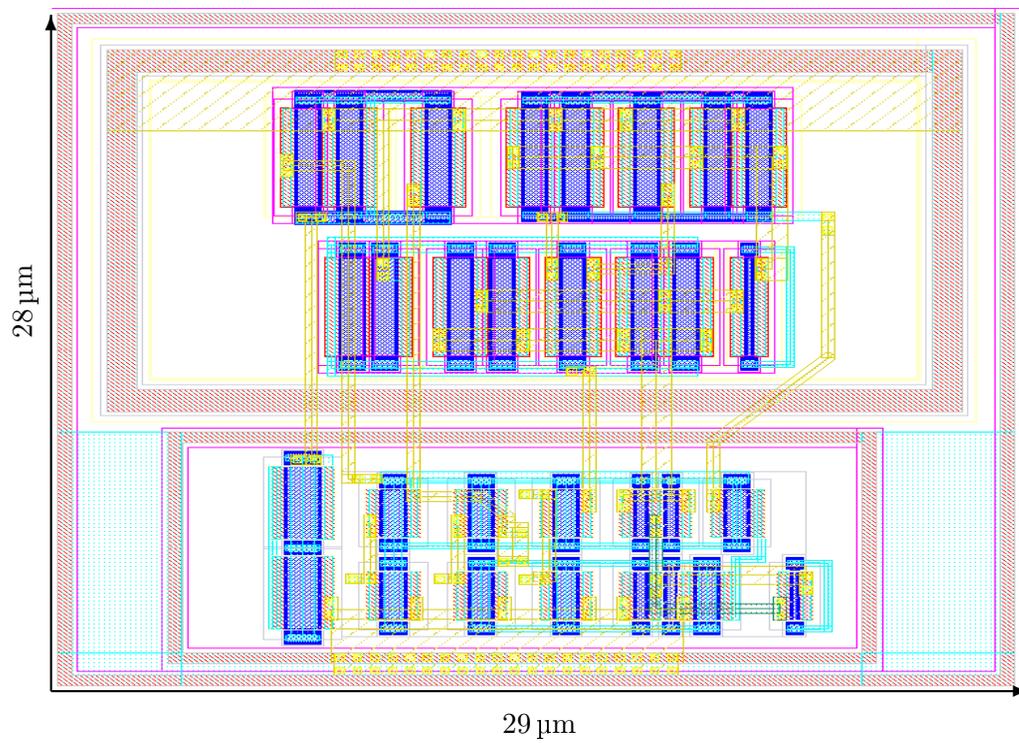


FIGURE 4.11. Layout of the Charge Pump

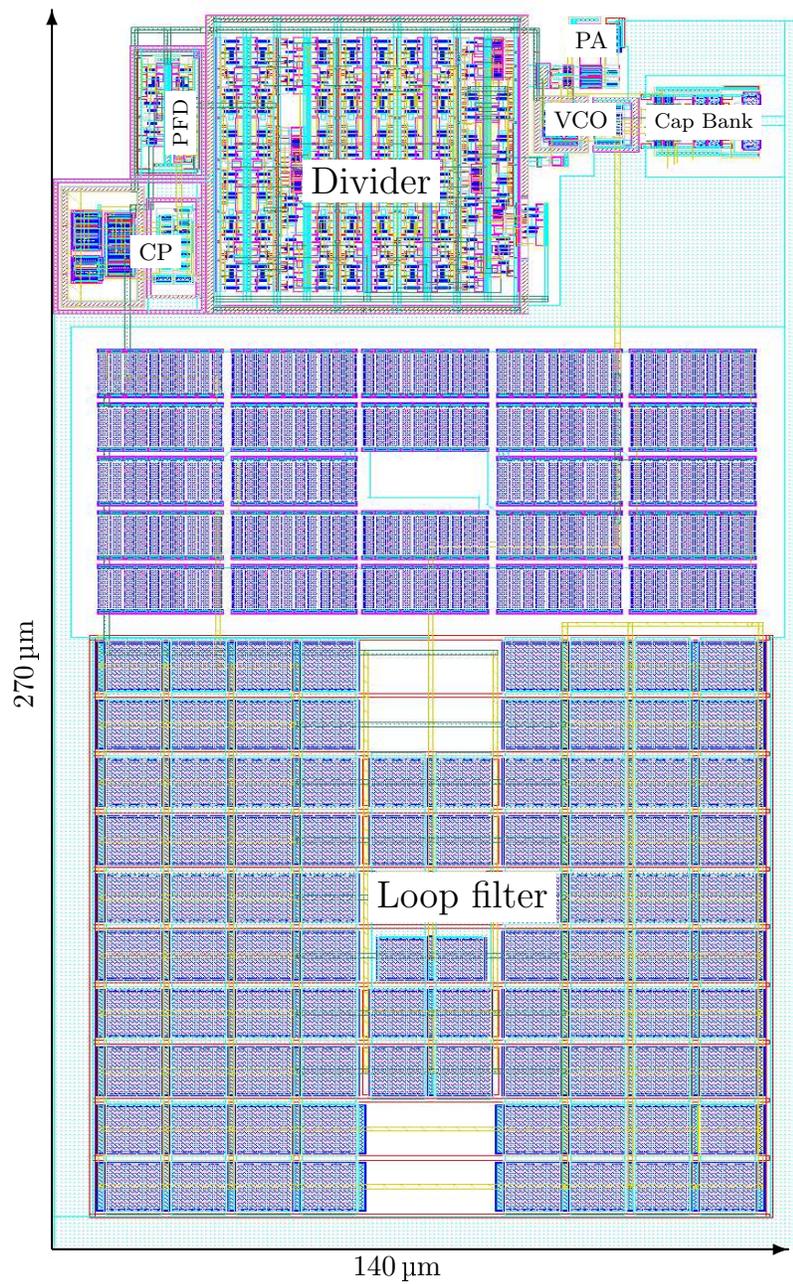


FIGURE 4.12. Layout of the Transmitter

The layout of the transmitter is shown in Figure 4.12 with locations of different components in the transmitter clearly marked. The VCO, the capacitor bank of the VCO, the mixer

and the PA are planned on the layout floor-plan to be as closely as possible to reduce routing parasitics. The PA is near the output pad on the layout. This is to minimize the routing resistance to the output. The silicon area occupied by the transmitter is  $270\ \mu\text{m} \times 140\ \mu\text{m}$ .

## 4.2. SIMULATION RESULTS

The overall goal of verifying the proposed transmitter design is to

- (1) Measure it's ability to adapt to environment.
- (2) Transmitter's output settling time when channels are changed from one to another.
- (3) Transmitter's output spectrum in terms of output signal strength relative to all the unwanted components in the output for different channels and data rates.
- (4) The overall transmitter performance from the simulations.

All the simulation results are based on extracted layout netlist unless it is stated otherwise. Figure 4.13 shows the output of the frequency synthesizer of the proposed transmitter for an input reference frequency of 300 kHz for the schematic netlist. The adjacent band's signal strength is 45.3 dB below when compared to the main band strength. Figure 4.14 shows the output of the frequency synthesizer of the proposed transmitter for the extracted netlist, for an input reference frequency of 300 kHz. The adjacent band's signal strength is 27 dB below when compared to the main band strength. The higher adjacent band signal strength is due to the parasitics in the extracted layout at the same power consumption. The 27 dB adjacent band suppression is well above the required suppression of the adjacent bands of 20 dB specified by the MedRadio band.

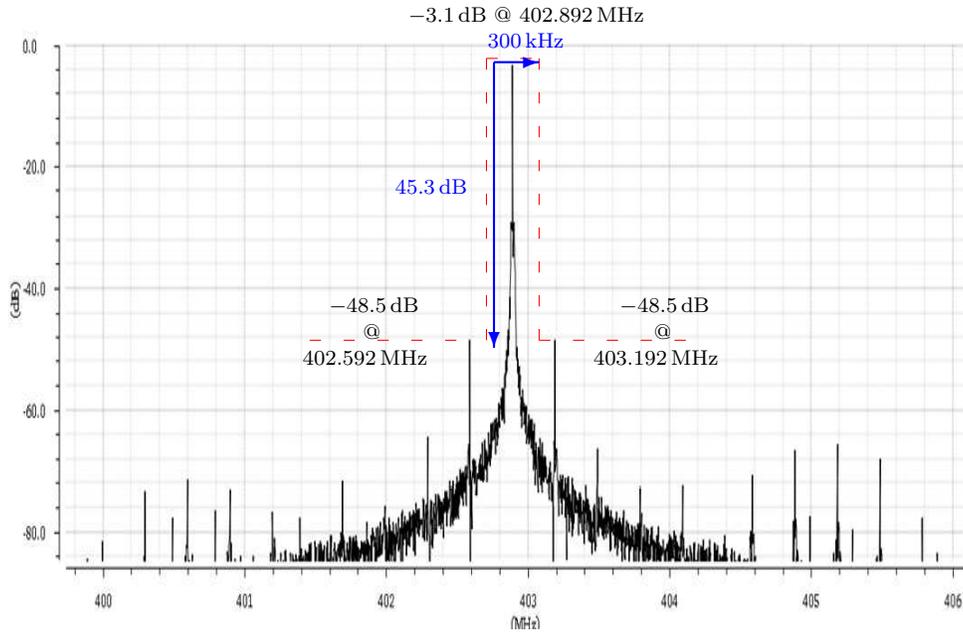


FIGURE 4.13. Spectrum of output of the PLL for schematic netlist

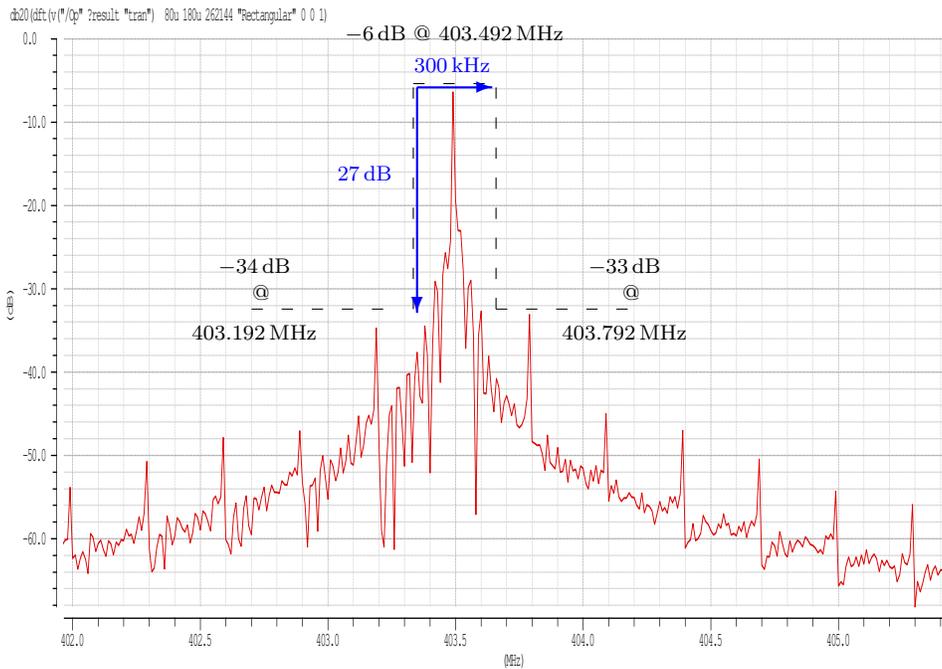


FIGURE 4.14. Spectrum of output of the PLL for extracted layout netlist

Figure 4.15 shows the settling of the control analog voltage ( $V_{ctrl}$ ) of the frequency synthesizer from transient analysis of the extracted layout at different temperature starting from 27°C followed by 40°C at 120  $\mu$ s and 20°C at 300  $\mu$ s. The control voltage settles at different voltage level to compensate the varying temperatures to maintain the output frequency constant. The settling time for the high temperature jump is usually high when compared to small increments in temperature. Figure 4.15 shows the case of exaggerated jump in temperature of 13°C from 27°C to 40°C, covering the range of 20°C to 40°C. Usually electronics used in the implantable devices are tested for the range of 20°C to 40°C. Moreover the human body temperature does not change so abruptly.

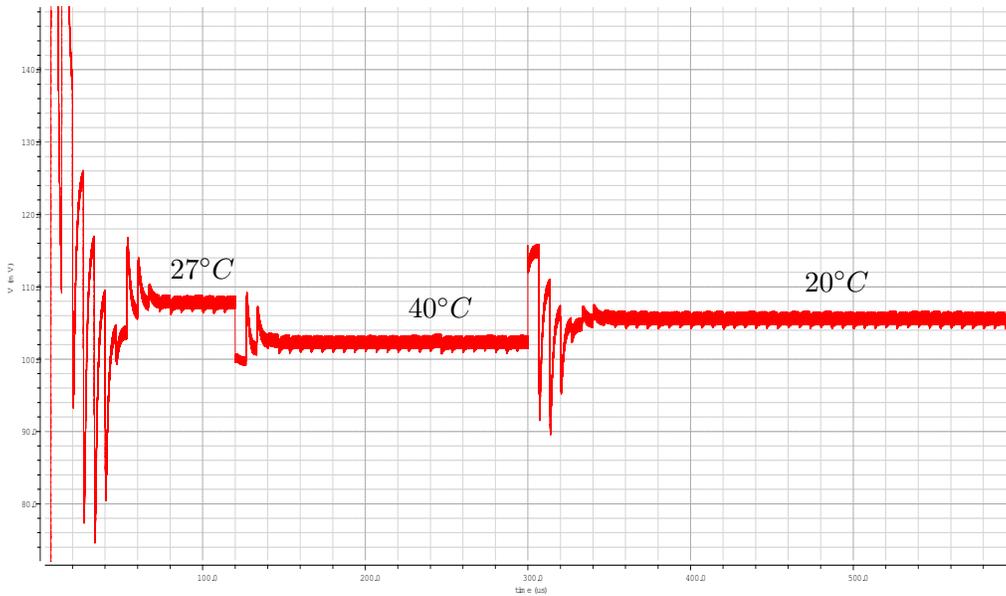


FIGURE 4.15. Control voltage ( $V_{ctrl}$ ) settling at various temperatures for same D

Figure 4.16 shows the spectrum of the frequency synthesizer with the above setup of varying temperature. The spectrum shows the PLL still maintains 20 dB suppression in the adjacent bands. But, the power level in the adjacent bands is increased due to the PLL settling for the temperature change. When large time intervals after settling of the PLL are considered then the spectrum performance will increase.

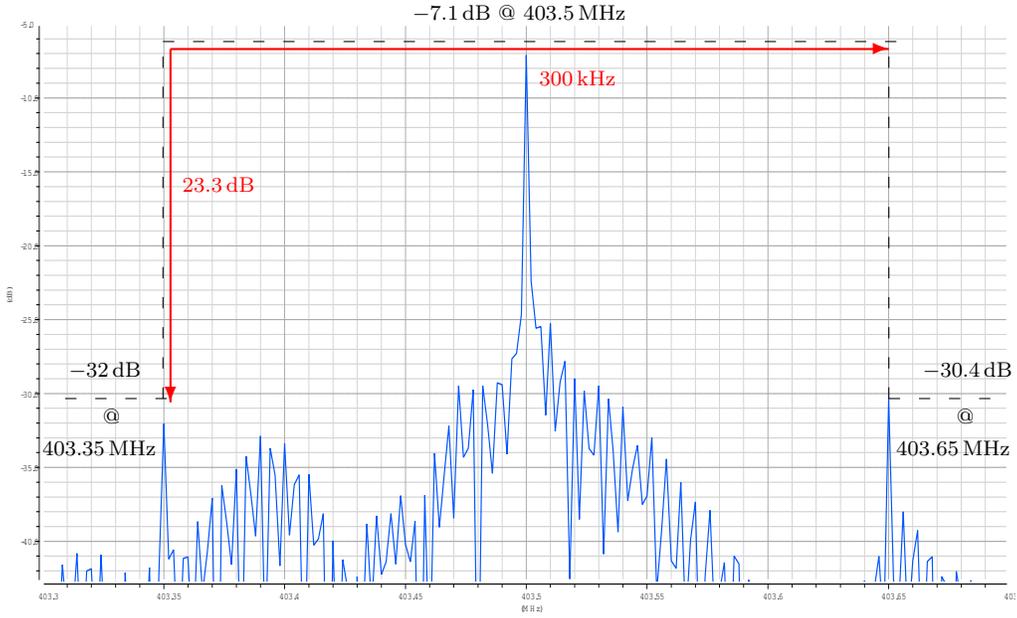


FIGURE 4.16. Spectrum of the frequency synthesizer after change in temperature for same D

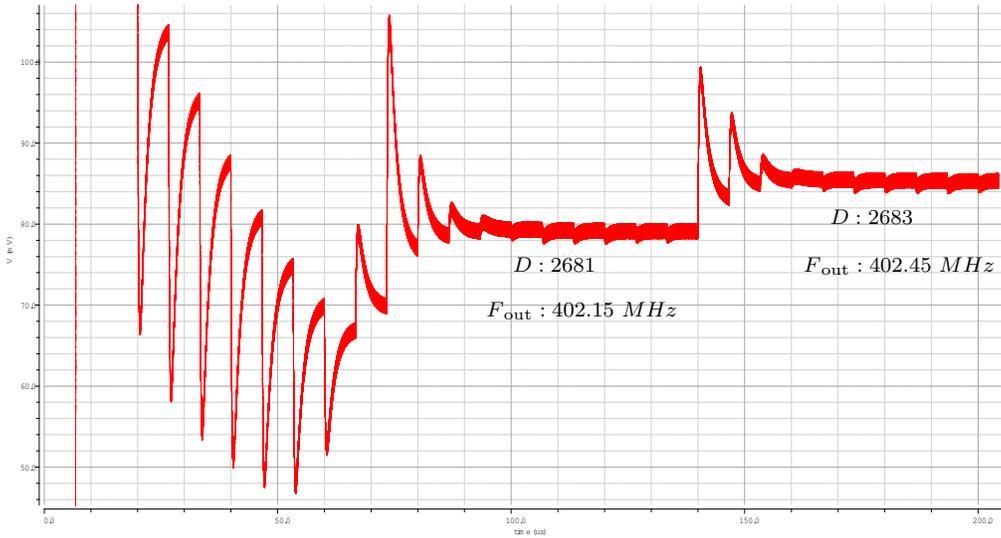


FIGURE 4.17. Control voltage ( $V_{ctrl}$ ) settling at different D for a step size of two

Figure 4.17 shows the settling of the control analog voltage ( $V_{ctrl}$ ) from transient analysis of the PLL for two different neighboring channels with division ratio of D being 2681 and 2683, for an input reference frequency of 150 kHz. Initially the control analog voltage ( $V_{ctrl}$ ) is settled around 79 mV, the PLL is locked at a frequency of 402.15 MHz (Channel 1 of the

MICS band) for D of 2681. Then D is increased by two to 2683. The  $V_{ctrl}$  is increased to 85 mV to increase the output frequency to 402.45 MHz (Channel 2 of the MICS band). This is to illustrate that the frequency synthesizer of the proposed transmitter can settle within 20  $\mu$ s time period for the change in the channel to the adjacent channel.

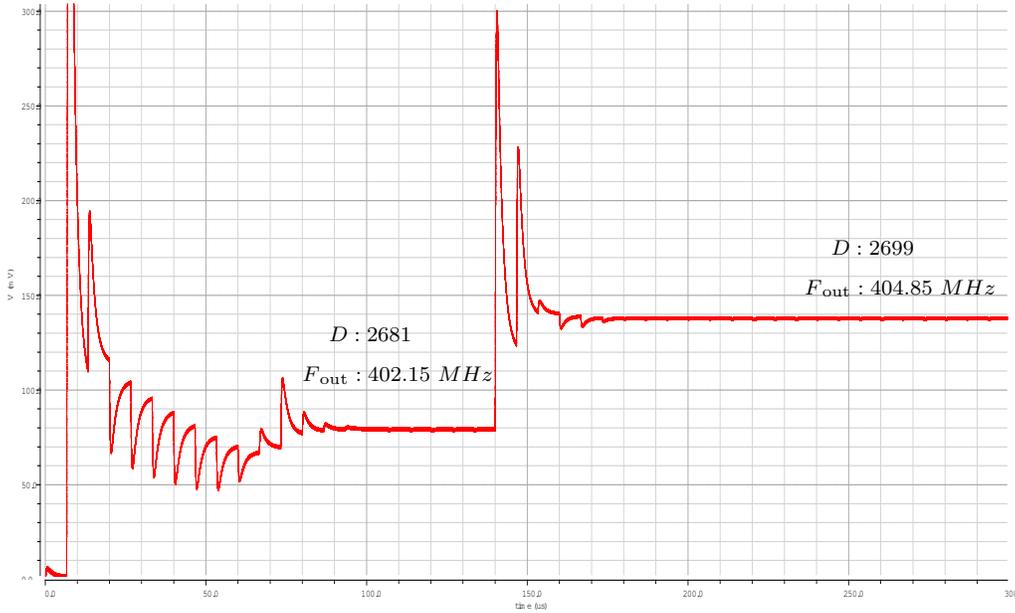


FIGURE 4.18. Control voltage ( $V_{ctrl}$ ) settling at different D for a step size greater than one

Figure 4.18 shows the simulation of a large step change in the division ratio of the frequency synthesizer. Initially the PLL is locked at a frequency of 402.15 MHz (Channel 1 of the MICS band) for D of 2681. Then D is increased by eighteen to 2699. The  $V_{ctrl}$  is increased to increase the output frequency to 404.85 MHz (Channel 10 of the MICS band). The proposed transmitter will settle within 40  $\mu$ s time period for the maximum change in the channel from channel 1 to channel 10. The control voltage before settling is high and will cause spurious emissions into the MICS adjacent bands, so care has to be taken to gradually increase the division ratio in the steps of two (2) to make the output of the frequency synthesizer settle within the MICS band with less spurious emissions.

The output waveform at the antenna from the transient analysis of the extracted layout netlist of the transmitter is shown in Figure 4.19. The output sine wave is around 184 mV peak to peak at the antenna with output impedance being  $50\ \Omega$ .

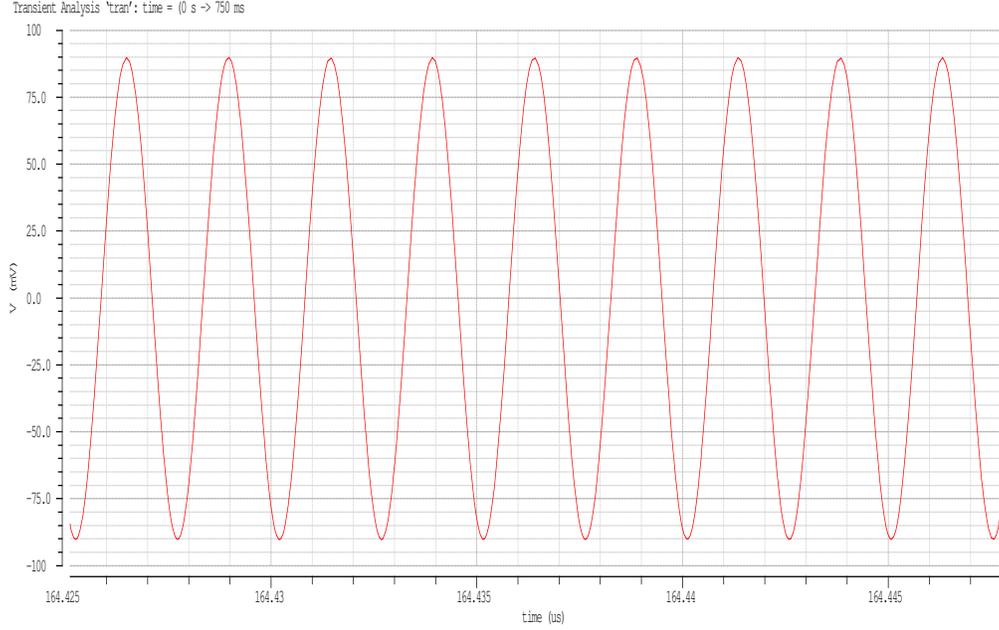


FIGURE 4.19. Output waveform at the antenna

$$(3) \quad \text{Outputpower}(p) = \frac{V^2}{2 * R}$$

$$(4) \quad \text{Outputpower}(dBm) = 20 * \log\left(\frac{p}{0.001}\right)$$

The output power given equation 1 is  $82\ \mu\text{W}$ . Hence the output power in dBm given by equation 2 is  $-10.8\ \text{dBm}$ . The output power of  $-10.8\ \text{dBm}$  is greater than the allowed power in the MedRadio band of  $-16\ \text{dBm}$ . The higher output power is useful in compensating for the losses of the implantable antenna.

The frequency spectrum of the transmitted signal at the antenna with modulation data rate of 60 kbps is shown in Figure 4.20, for an input reference frequency of 150 kHz. The

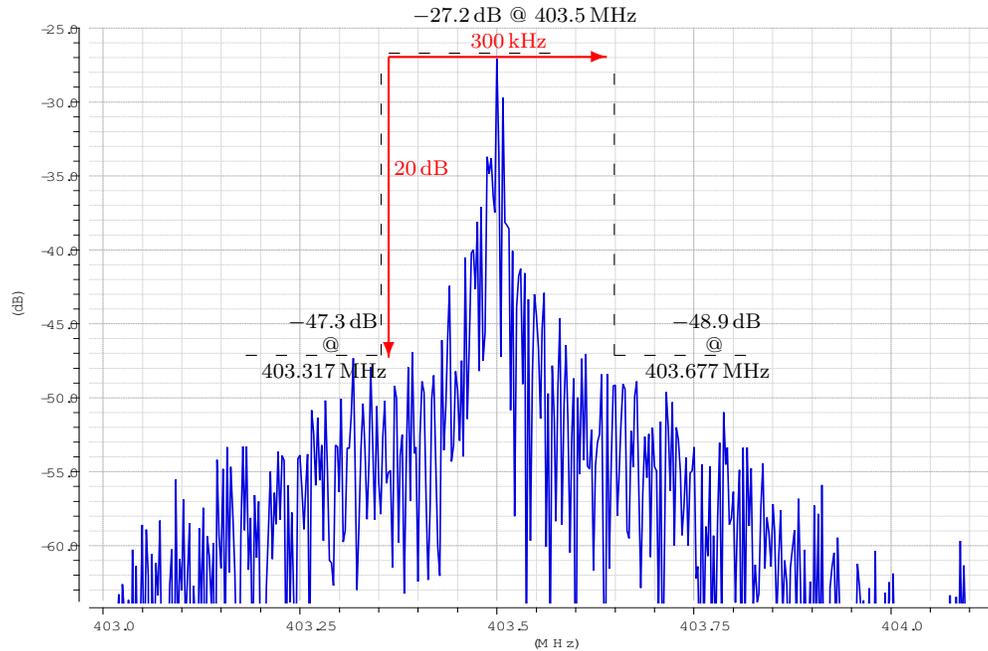


FIGURE 4.20. Spectrum of output at the antenna

output waveform at the antenna from the transient analysis of the extracted layout of the transmitter is at  $-10.8$  dBm. The adjacent channel signal strength is 20 dB below when compared to the output channel strength. The spectrum is spread across the 300 kHz channel, due to the modulation of data on to the carrier signal frequency. This transmitter can cover all the sub-band frequencies in 401-406 MHz MedRadio band.

Table 4.2 shows the final breakdown of the average DC power consumption of the various components of the transmitter, when working in the MICS band of 401-406 MHz at a power supply voltage of 1.2 V. These results are obtained after transient simulation on the extracted layout of the proposed transmitter.

TABLE 4.2. Power breakdown of the different components of the transmitter working in the MICS band of 401-406 MHz

<b>Component</b>	<b>Power (<math>\mu</math>W)</b>
PFD	5
Charge Pump	40
Divider	35
VCO	160
PLL	240
PA	185
<b>Total Power</b>	<b>425</b>

The frequency spectrum of the transmitted signal at the antenna with modulation data rate of 2.3 Mbps is shown in Figure 4.21. The input reference frequency is 150 kHz,  $D$  equal to 3026 and the output frequency of the PLL is 454.05 MHz. The output waveform at the antenna from the transient analysis of the extracted layout of the transmitter is at  $-10.8$  dBm. The adjacent channel signal strength is 20 dB below when compared to the output channel strength. The spectrum is spread across the 6 MHz channel, due to the modulation of data of 2.3 Mbps on to the carrier signal frequency of 454.05 MHz. This is to illustrate that the proposed transmitter can work in one of the four channels, 451-457 MHz channel of the MedRadio band of 413-457 MHz. This transmitter can cover all the four channels 413-419 MHz, 426-432 MHz, 438-444 MHz, and 451-457 MHz in the MedRadio band with appropriate division ratio ( $D$ ) .

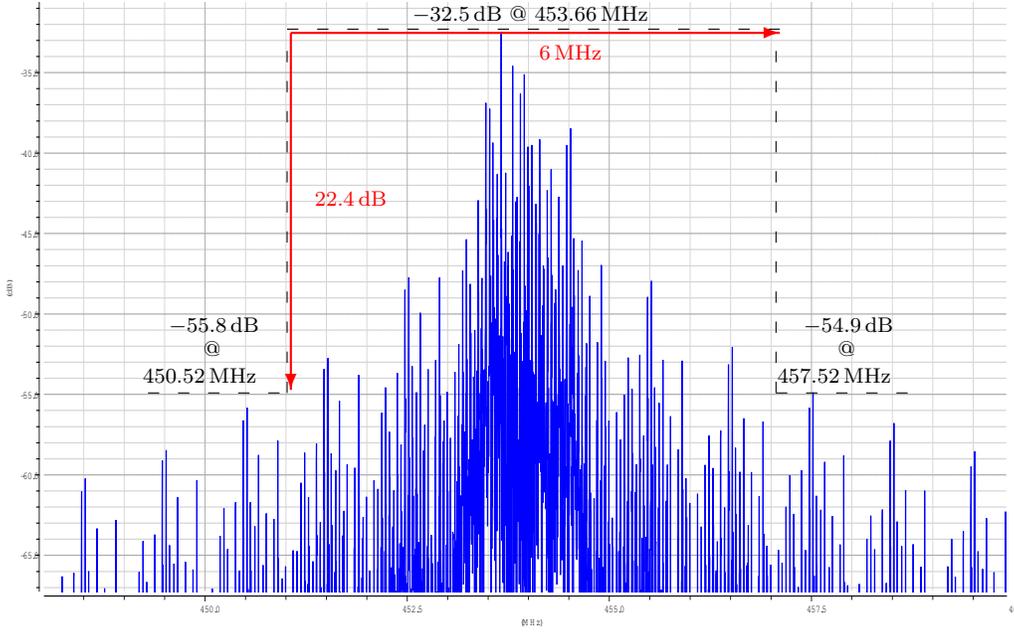


FIGURE 4.21. Spectrum of output at the antenna for the channel 451-457 MHz of the MMNs band

Table 4.3 shows the final breakdown of the average DC power consumption of the various components of the transmitter, when working in the channel of 451-457 MHz of the MMNs band at a power supply voltage of 1.2 V. These results are obtained after transient simulation on the extracted layout of the proposed transmitter. Hence the maximum power consumption of the transmitter is 460  $\mu$ W.

TABLE 4.3. Power breakdown of the different components of the transmitter working in MMNs band of 413-457 MHz

Component	Power ( $\mu$ W)
PLL	255
PA	205
<b>Total Power</b>	<b>460</b>

## CHAPTER 5

# PROTOTYPE OF WEARABLE DEVICES

This chapter will explore the details of implementation of the wearable device and retrieving data through Internet using off-the-shelf ICs, components and development boards.

### 5.1. WEARABLE DEVICE

The wearable devices are a form of Control Unit (CU) worn on the body of patient/person to monitor vital signs of the body or to relay the information received from the implanted device to the base station. Figure 5.1 shows the board used as CU in the present case.

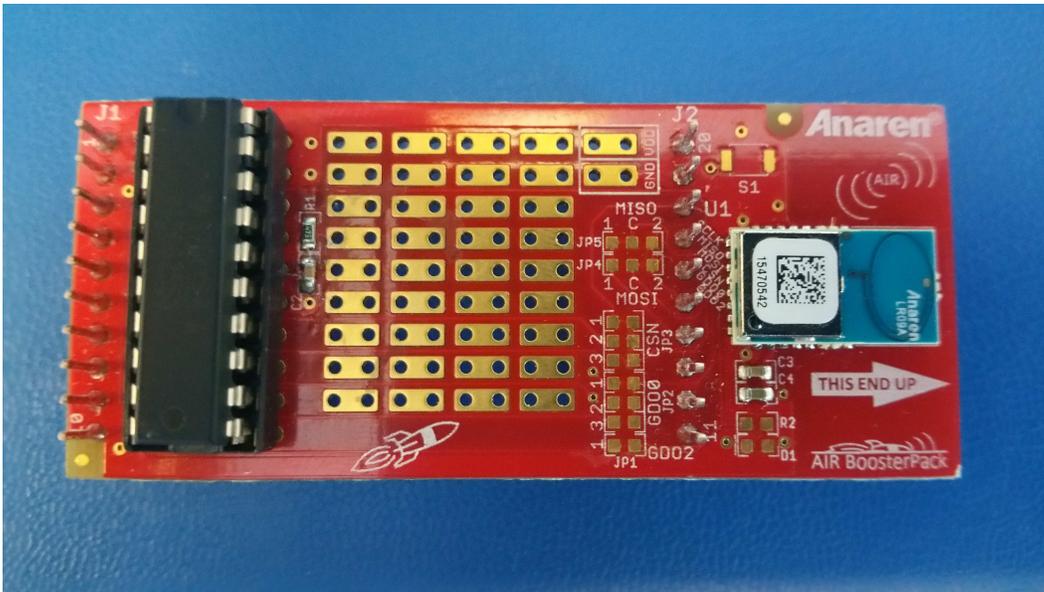


FIGURE 5.1. Airpack with MSP430G2553

The data from the implanted devices can be received with the help of wearable device shown in Figure 5.1. This is an attempt to show the working of wearable device, but in practical applications the device size should be reduced using a custom made PCB board with only required components. The CU in present design is an AIR booster pack from Anaren. It

consists of the RFIC A110LR09C from Anaren. The micro-controller used is MSP430G2553 from Texas Instruments, programmed using MSP430 launchpad which is shown in Figure 5.2. This wearable device works on 3.3 V power supply. The I2C protocol is used by the micro-controller to communicate with the RFIC A110LR09C. Anaren's RFIC A110LR09C uses the 900 MHz of Industrial Scientific and Medical (ISM) band for communication. The spectrum usage of this device is shown in Figure 5.3 captured using Real Time Spectrum Analyzer (RSA6100A) from Tektronix.

This wearable device is tested with a capacitive sensing hand held device prototype for wireless connectivity. Energia [44] is used as the integrated development environment for the device. Code for this device is included in Appendix E.1.

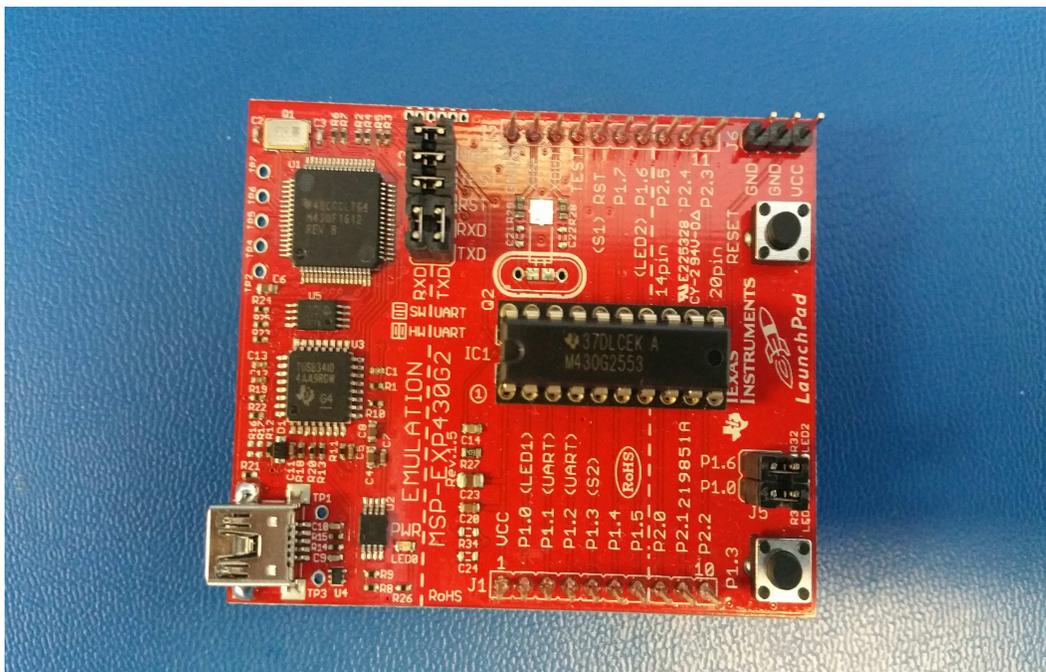


FIGURE 5.2. MSP430 launchpad board form Texas Instruments

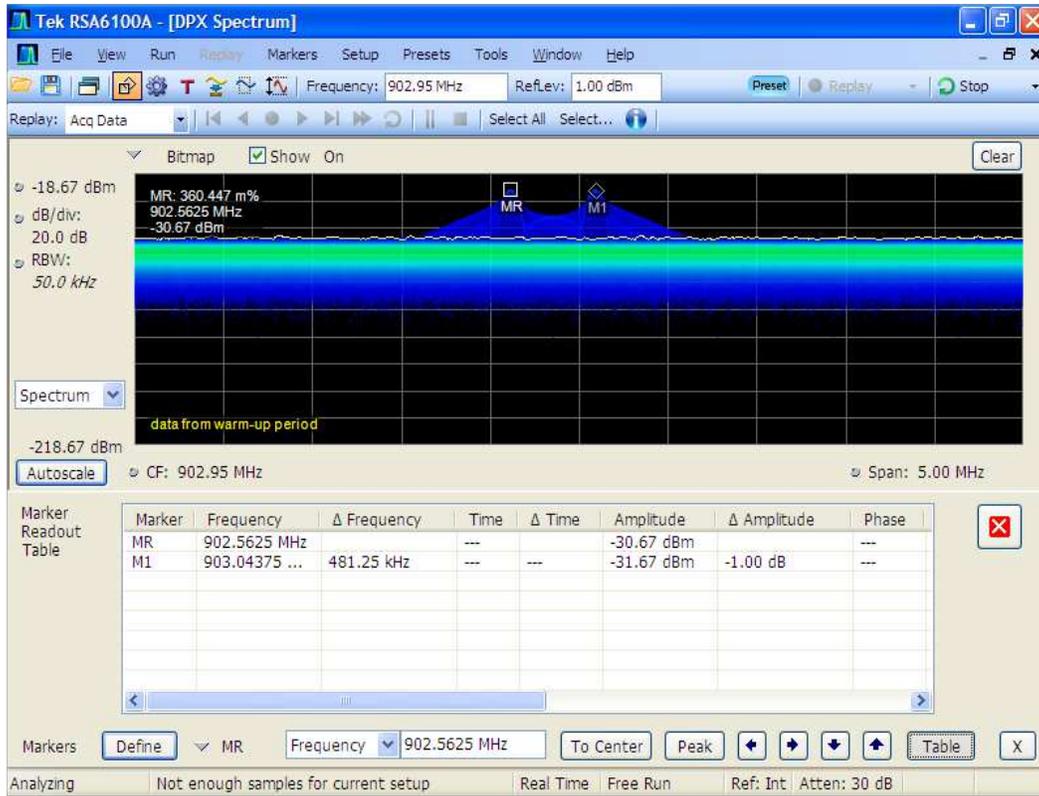


FIGURE 5.3. Spectrum of A110LR09C captured from the RSA6100A.

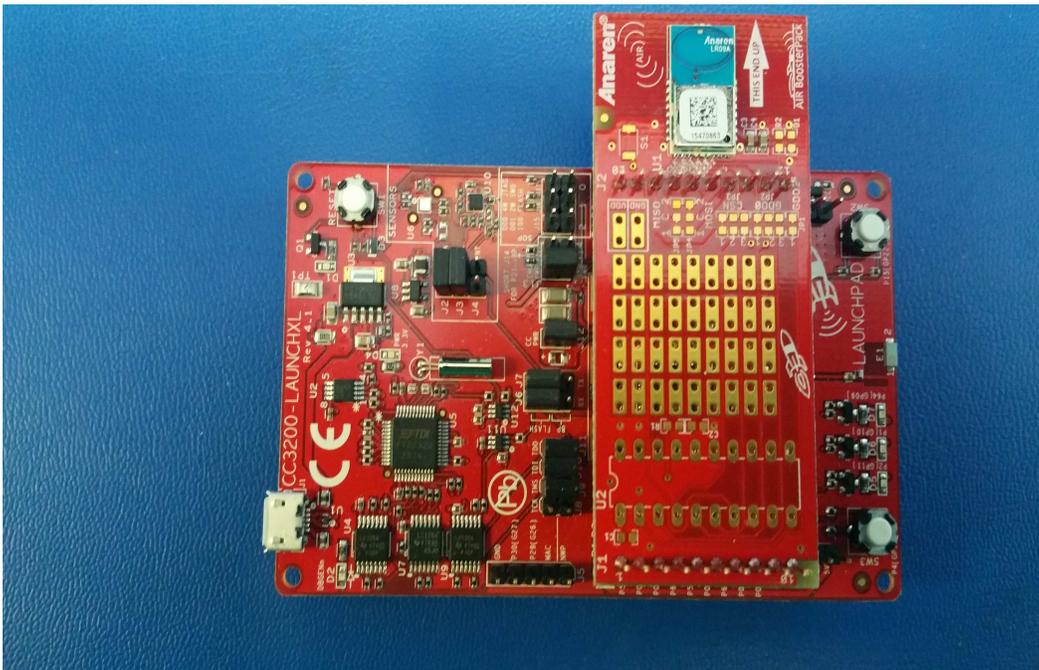


FIGURE 5.4. CC3200 board form Texas Instruments with Anaren booster pack

The base station here is a development board called Launch pad CC3200 from Texas Instruments with a Anaren Booster pack as shown in Figure 5.4. The data from the CU unit can be saved on the base station, and transmitted to Internet through the local Wi-Fi

The data transmitted from CU working in the 900MHz band is received with the help of Anaren booster pack installed on the top of CC3200 using the 900 MHz ISM band. The 2.4GHz transceiver in CC3200 is used to connect to the local Wi-Fi. The CC3200 Launch pad is then connected to the cloud based web-server.

The same Energia is used as the integrated development environment for the device. The code for this device is included in Appendix E.2. In this specific application “dweet” [45] is used as the cloud server. Freeboard io [46] shown in Figure 5.5 is used for displaying the transmitted data.

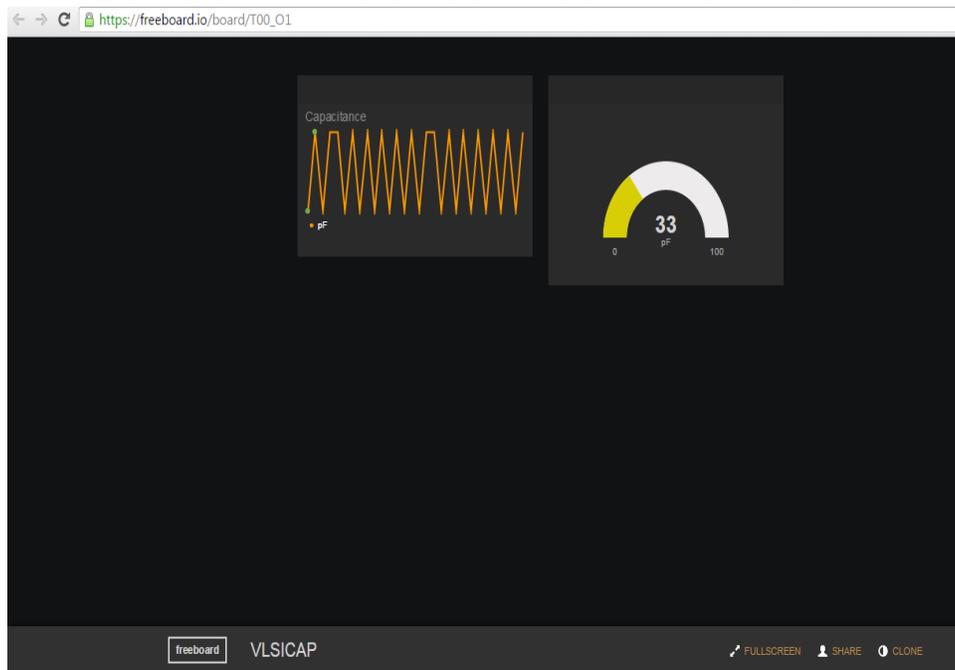


FIGURE 5.5. The web page display for the capacitive biosensor

The data received can be displayed on a web page with an URL specific to the application. The web page can be accessed from any device connected to the Internet. An example of the URL being accessed from a mobile phone is shown in Figure 5.6, which shows the capacitance reading from a wireless-enabled capacitive biosensor.

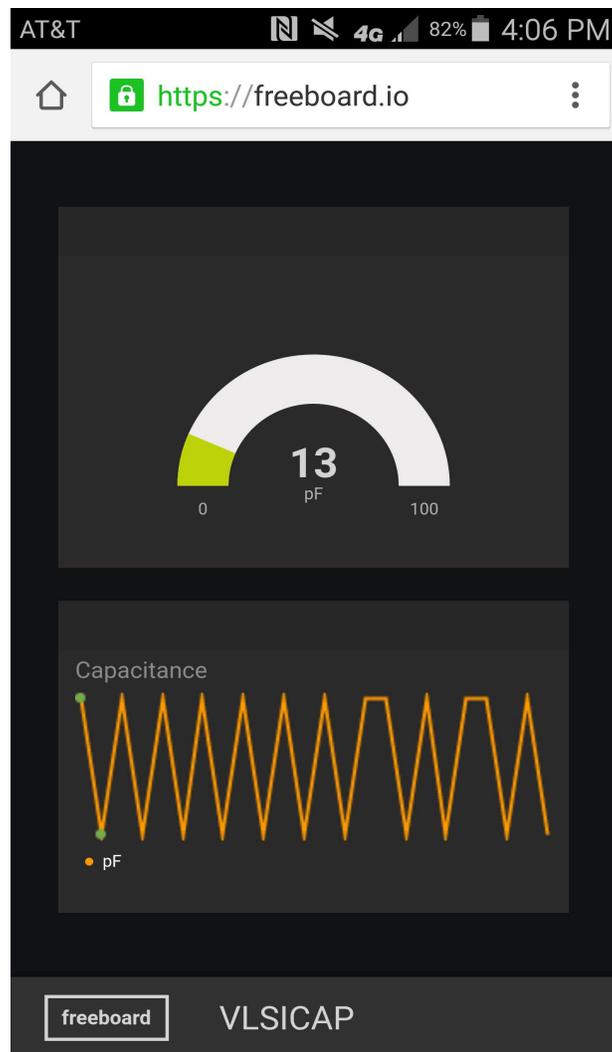


FIGURE 5.6. The mobile web page display for the capacitive biosensor

Apart from the displaying the data online. The real time data can be stored on the computer as shown in Figure 5.7 along with the time stamp. This data can be later used to access information. CoolTerm [47] is used for implementing this application.

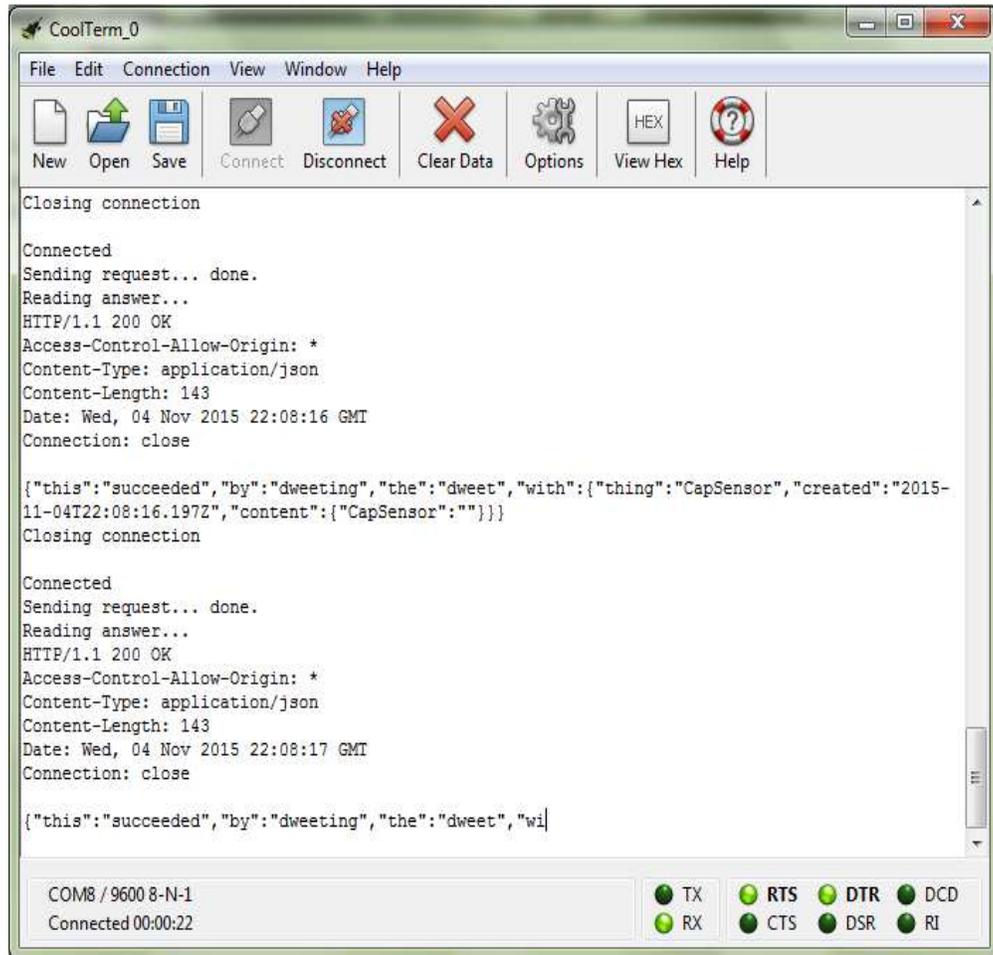


FIGURE 5.7. Saving data on to a computer with time stamp

## CHAPTER 6

### CONCLUSIONS AND DISCUSSIONS

This thesis presented an ultra low power transmitter consuming only around 460  $\mu$ W at power supply of 1.2 V in a 180 nm CMOS process. The proposed transmitter has a process and temperature independent frequency synthesizer that can utilize all the bandwidths that are authorized by the FCC in the 401-457 MHz MedRadio band, while satisfying all the regulations of the MedRadio band. The silicon area occupied by the transmitter is 0.04 mm<sup>2</sup>.

One of the key contributions of the proposed transmitter design is the careful balance and design trade-off in the PLL design to achieve low power and high efficiency. For example in the proposed PLL the gain of the VCO ( $K_{VCO}$ ) is chosen small as 24 MHz/V, the charge pump current  $I_{CP}$  is at 15  $\mu$ A, and the loop filters values are optimum to occupy as small area as possible. These design decisions helped the PLL design to become one of the most power efficient and smallest designs compared to existing designs with PLL.

A power centric figure-of-merit ( $FOM_{pwr}$ ) is used for better comparison among existing designs of the phase locked loops (PLL). The  $FOM_{pwr}$  is defined as ratio of the total power consumed by the frequency synthesizer and the highest operational frequency generated by the frequency synthesizer.

$$(5) \quad FOM_{pwr} = \frac{Power}{F_{out}}$$

The  $FOM_{pwr}$  for the proposed frequency synthesizer of the transmitter design is better when compared with the existing designs of the frequency synthesizer, while occupying a smaller area.

TABLE 6.1. PLL Design Comparison

Reference	Process CMOS (nm)	Power supply (V)	Power ( $\mu$ W)	Area (mm <sup>2</sup> )	Settling time ( $\mu$ s)	Operation Frequency (MHz)	FOM <sub>pwr</sub> ( $\mu$ W/MHz)
This work	180	1.2	255	0.04	20	401-457	0.56
[31]	90	1.2	251	0.05	68	402-405	0.6
[32]	65	1.0	430	0.54	350	402-405	1.1
[48]	90	0.5	400	0.07	600	400	1.0
[42]	130	0.5	440	0.07	90	400-433	1.0
[24]	180	1.2	2640	0.70	16	440	6.0
[25]	180	1.2	2280	0.70	16	435	5.2
[26]	180	1.8	2400	0.20	NA	402-405	5.9
[49]	130	0.5	1250	0.04	5	550	2.2

The proposed design also achieved an excellent settling time given the design choices made to have a narrower loop bandwidth to accommodate  $F_{\text{ref}}$  of 100 kHz. The settling time for different bands is less than 20  $\mu$ s. This design choice enables us to use high division ratio of 4010-4060, still stay in the MedRadio band of 401-406 MHz and utilizes 100 kHz bandwidths as allowed by FCC in 401-402 MHz and 405-406 MHz.

The comparison of the data rate, output power, transmitter efficiency, and power consumption of the proposed design with the existing published designs is shown in Tables 6.2, and 6.3. An energy centric figure-of-merit (energy/bit) is used for better comparison among the designs of the transmitter. The energy/bit is defined as ratio of the DC power consumed and the highest modulation data rate achieved by the transmitter.

$$(6) \quad FOM_{E/\text{bit}} = \frac{\text{Power}}{\text{Data rate}}$$

The transmission efficiency ( $\eta$ ) of the transmitter is defined as the ratio of the output power transmitted to the total DC power consumed by the transmitter.

$$(7) \quad \eta = \frac{P_{\text{out}}}{DC \text{ Power}}$$

The energy per bit for the proposed design is significantly better when compared with the existing transmitter designs including PLL in [24–29], shown in Table 6.2, while occupying a smaller area, is consuming less power, and output more power. The existing designs in Table 6.2 were designed to be MICS-standard compliant in some settings, while working in other standards like body channel communication (BCC) [26], medical micro-power networks (MMNs) [24, 25, 28, 29], which are not MICS-standard compliant. For a fair comparison, only MICS-band compliant performance data for those designs are chosen and included in Table 6.2. The most optimistic data rate of 300 kbps is given to the existing designs for comparison. This is because the maximum specified bandwidth of a channel in MICS band communications by FCC is 300 kHz and this limits the data rate in the each channel to a value less than 300 kbps.

Another category of low power transmitter designs employs techniques to omit PLLs in the designs in [20–23, 30, 50]. By eliminating PLLs, the overall transmitter power consumption can be significantly lower. However, designs belonging to this category tend to trade off certain aspects of MICS-standard compliance with power consumption.

TABLE 6.2. Comparison of Transmitter Design including PLLs in the MICS band

Reference		This work	[24, 25]	[26]	[27]	[28, 29]
<b>Process CMOS</b>	nm	180	180	180	180	180
<b>Power supply</b>	V	1.2	1.2	1.8	2-3	1.0
<b>Operation frequency</b>	MHz	401-457	350-440	400-2400	402-405	402-405
<b>Transmitter architecture</b>		Mixer based	Mixer based	Mixer based	Mixer based	FIR-PM
<b>Modulation scheme</b>		QPSK	O-QPSK	BFSK	G/FSK	HS-QPSK
<b>With PLL</b>		Yes	Yes	Yes	Yes	Yes
<b>Maximum Data rate</b>	Mbps	0.06	0.30	0.3	0.30	0.3
<b>Output power</b>	dBm	-11.4	-15	-12	NA	-8
<b>DC power</b>	$\mu$ W	425	3500	8900	10000	2600
<b>Transmitter efficiency</b>	%	19.3	0.9	0.63	NA	6.0
<b>Energy/bit</b>	nJ/bit	7.08	11.67	29.67	33.34	8.67

Designs in [20, 21] achieved a higher overall transmission efficiency of 22% vs. 19.3% achieved by the proposed design. These designs output low power, and low transmission propagation distance.

The designs in [20–23] have low energy per bit due to low power consumption. However, these designs using the direct injection method instead of PLL does not allow for frequency

TABLE 6.3. Comparison of Transmitter Design without PLLs in the MICS band

Reference		This work	[20, 21]	[23]	[22]	[50]	[30]
<b>Process CMOS</b>	nm	180	130	90	130	180	90
<b>Power supply</b>	V	1.2	1.0	0.6	0.5	0.7	0.7
<b>Operation frequency</b>	MHz	401-457	402-405	402-405	402-405	402-405	391-415
<b>Transmitter architecture</b>		Mixer based	Edge Combining	Edge Combining	Edge Combining	Direct VCO	Direct VCO
<b>Modulation scheme</b>		QPSK	BFSK	OOK	BFSK	FSK	MSK
<b>With PLL</b>		Yes	No	No	No	No	No
<b>Maximum Data rate</b>	Mbps	0.06	0.20	1.00	0.10	0.25	0.12
<b>Output power</b>	dBm	0.06	0.20	1.00	0.10	0.25	0.12
<b>DC power</b>	$\mu$ W	425	90	160	400	400	350
<b>Transmitter efficiency</b>	%	19.3	22	12.5	6.3	6.25	NA
<b>Energy/bit</b>	nJ/bit	7.08	0.45	0.16	4.00	1.60	2.90

band hopping within the MICS and MMNs bands. Therefore, they are not completely MICS-standard compliant.

Designs in [30, 50] allows frequency hopping among the MICS band of 402-405 MHz. However, due to eliminating on-chip PLL, they have chosen to incorporate mechanisms of manual periodic frequency calibration involving base stations, thus, shifting the power consumption from the transmitters to the base stations to achieve lower power consumption.

Furthermore, the use of relatively low supply voltage of 0.7 V and the free running DCOs in these designs will have difficulties in achieving carrier frequency stability as defined by FCC. The silicon area of the proposed transmitter is less at 0.04 mm<sup>2</sup> in comparison with [30, 50] at 0.5 mm<sup>2</sup> and 1 mm<sup>2</sup>, respectively. Moreover, the output signal power of these designs is low when compared to the proposed transmitter design. When the transmission distance is taken into account for better comparison the proposed design will perform better, because of the high output power of the proposed transmitter design.

An attempt was made to compare the proposed transmitter design to the designs in [20–23, 30, 50], which are not compliant with the MICS standard in Table 6.3. It must be noted that the comparison in Table 6.3 is not a fair comparison due to the fact that the proposed transmitter design with on-chip PLL is fully MICS-standard compliant. Table 6.3 is compiled to provide readers with different perspectives on possible power trade-offs that were taken by existing designs that resulted from significant deviations from the MICS standard. It is, however, not intended for straight power and performance comparison. Table 6.2 is mainly intended for that purpose.

The energy/bit for the proposed design is significantly better when compared with the existing transmitter designs consisting of the PLL like [24, 25, 27–29, 20, 21] for the MICS band complaint data rate, while occupying a smaller area.

The low energy/bit in [23] is due to absence of the PLL. Moreover, the output signal power of this design is low due to use of relatively low supply voltage of 0.7 V. When the transmission distance is taken into account for better comparison the proposed design will perform better, because of the high output power and QPSK modulation scheme of the proposed transmitter design as compared to On-Off Keying (OOK) modulation in [23].

TABLE 6.4. Comparison of Transmitter Design in the MedRadio band

Reference		This work	[20, 21]	[23]	[24, 25]	[28, 29]	[27]
<b>Process CMOS</b>	nm	180	130	90	180	180	180
<b>Power supply</b>	V	1.2	1.0	0.6	1.2	1	2-3
<b>Operation frequency</b>	MHz	413-457 401-406	402-405	402-405	355-440	413-457 402-405	402-405
<b>Transmitter architecture</b>		Mixer based	Edge Combining	Edge Combining	Mixer Based	FIR PM	Mixer based
<b>Modulation scheme</b>		QPSK	BFSK	OOK	O-QPSK	HS-QPSK	G/FSK
<b>With PLL</b>		Yes	No	No	Yes	Yes	Yes
<b>Maximum Data rate</b>	Mbps	2.3	0.20	1.00	6	4	0.08
<b>Output power</b>	dBm	-10.8	-17	-17	-15	-8	NA
<b>DC power</b>	$\mu$ W	460	90	160	3500	2600	10000
<b>Transmitter efficiency</b>	%	13.9	22	12.5	0.9	6.0	NA
<b>Energy/bit</b>	nJ/bit	0.20	0.45	0.16	0.60	0.65	18.00

Table 6.4 show the transmitters proposed in various designs in the MedRadio band. Although most of the designs in Table 6.4 are not MMNs-band compliant i.e not able to cover all the four channels in the 413-457 MHz band, but are included to give the readers an idea of the existing designs and the trade offs involved while designing the MedRadio

transmitter. The presented design is not only MMNs-band complaint but can also cover MICS-band of 401-406 MHz.

The only designs truly can be compared with the proposed design are the designs in [28, 29]. Since, these designs cover all the channels in the MedRadio band as in the proposed design. The proposed transmitter design performs better in terms of energy per bit transmitted and the overall transmitter efficiency.

Due to the careful trade offs between performance and power consumption, we are able to achieve a transmitter design with the highest overall transmission efficiency compared to the other existing designs while maintaining performance sufficient for low data rate of biomedical applications in the MedRadio band. The proposed transmitter has struck a balance between total power consumed, global efficiency, energy per bit and at the same time utilize all the bandwidths allocated in the MedRadio band efficiently.

Further improvements of the proposed transmitter may include incorporation of automatic on-chip calibration to tune the output frequency of the VCO to be in the MedRadio band by varying the load capacitance and to turn off power amplifier (PA) during the calibration stage. A complete transceiver design on chip which would require a receiver design to receive data and detect the strength of signals to determine a “not activity channel to transmit data. Integration of the front-end sensor and data processing functions on chip to build a complete bio-integrated system is highly desirable.

Another improvement can be building a wearable device (Control Unit) that has the capability of both 400 MHz ISM band, and 2.4 GHz ISM band, thereby developing the capability of wearable device to connect to the Internet via 2.4 GHz ISM band. This will eliminate the need of the base station (Launch pad CC3200) altogether.

## BIBLIOGRAPHY

- [1] Setpointmedical, “Neuromodulation for inflammation.” <http://www.setpointmedical.com/index.php/technology/neuromodulation-for-inflammation>, 2012.
- [2] GSK, “Bioelectronics: skip the fiction, this is science.” <http://us.gsk.com/en-us/our-stories/how-we-do-randd/bioelectronics-skip-the-fiction-this-is-science/>, 2015.
- [3] A. Ali, N. Pal, and P. Levine, “Cmos impedance spectroscopy sensor array with synchronous voltage-to-frequency converters,” in *Circuits and Systems (MWSCAS), 2015 IEEE 58th International Midwest Symposium on*, pp. 1–4, Aug 2015.
- [4] N. Lewis, C. Lahuec, S. Renaud, E. McAdams, P. Bogonez-Franco, C. Lethias, S. Kellouche, F. Carreiras, A. Pinna, A. Histace, M. Boissiere, E. Pauthe, I. Lagroye, F. Soulier, S. Bernard, S. Binczak, B. Granado, P. Garda, M. Terosiet, A. Goguin, and O. Romain, “Relevance of impedance spectroscopy for the monitoring of implant-induced fibrosis: A preliminary study,” in *Biomedical Circuits and Systems Conference (BioCAS), 2015 IEEE*, pp. 1–4, Oct 2015.
- [5] J. L. R. Eric, C. Leuthardt and W. Z. Ray, “Neuroprosthetics.” <http://www.the-scientist.com/?articles.view/articleNo/41324/title/Neuroprosthetics/>, 2014.
- [6] A. Peer, “Implanted biosensors track vital signs.” <http://thefutureofthings.com/5617-implanted-biosensors-track-vital-signs/>, 2015.
- [7] T. Yilmaz, R. Foster, and Y. Hao, “Detecting vital signs with wearable wireless sensors,” *Sensors*, vol. 10, no. 12, p. 10837, 2010.
- [8] F. Agnesi, S. J. Tye, J. M. Bledsoe, C. J. Griessenauer, C. J. Kimble, G. C. Sieck, K. E. Bennet, P. A. Garris, C. D. Blaha, and K. H. Lee, “Wireless instantaneous neurotransmitter concentration systembased amperometric detection of dopamine, adenosine,

- and glutamate for intraoperative neurochemical monitoring,” *Journal of Neurosurgery*, vol. 111, no. 4, pp. 701–711, 2009. PMID: 19425899.
- [9] K. Kalantar-zadeh, C. K. Yao, K. J. Berean, N. Ha, J. Z. Ou, S. A. Ward, N. Pillai, J. Hill, J. J. Cottrell, F. R. Dunshea, C. McSweeney, J. G. Muir, and P. R. Gibson, “Intestinal gas capsules: A proof-of-concept demonstration,” *Gastroenterology*, vol. 150, no. 1, pp. 37 – 39, 2016.
- [10] A. S. for Gastrointestinal Endoscopy, “Understanding capsule endoscopy.” <http://www.asge.org/patients/patients.aspx?id=390>, 2015.
- [11] S. Woods and T. Constandinou, “Wireless capsule endoscope for targeted drug delivery: Mechanics and design considerations,” *Biomedical Engineering, IEEE Transactions on*, vol. 60, pp. 945–953, April 2013.
- [12] C. Merz, G. Kupris, and M. Niedernhuber, “A low power design for radio frequency energy harvesting applications,” pp. 74–78, Sept 2014.
- [13] S. Faghihi and M. Moallem, “Analysis and design of a low power electronics circuit for energy harvesting applications,” pp. 183–188, May 2012.
- [14] FCC, “medical device radiocommunications service-medradio.” <https://www.fcc.gov/encyclopedia/medical-device-radiocommunications-service-medradio>, 1999.
- [15] H. Chi and T. Chen, “A cmos temperature sensor with -0.34 c to 0.27 c inaccuracy from -30 c to 80 c,” in *VLSI (ISVLSI), 2014 IEEE Computer Society Annual Symposium on*, pp. 261–266, July 2014.
- [16] R. Shelby, “Low-power switched-capacitor amplifier and sigma-delta modulator design for integrated biosensor applications,” Master’s thesis, Colorado State University, May 2013.

- [17] W. Wilson, “Low-noise, low-power transimpedance amplifier for integrated electrochemical biosensor applications,” Master’s thesis, Colorado State University, May 2014.
- [18] K. Scholfield, “Low power biosensor and deciamtor design,” Master’s thesis, Colorado State University, May 2013.
- [19] T. Kern, “Design of intergerated on-chip impedance sensors,” Master’s thesis, Colorado State University, May 2014.
- [20] J. Pandey and B. Otis, “A 90 uw mics/ism band transmitter with 22% global efficiency,” in *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*, pp. 285–288, May 2010.
- [21] J. Pandey and B. Otis, “A sub-100 uw mics/ism band transmitter based on injection-locking and frequency multiplication,” *Solid-State Circuits, IEEE Journal of*, vol. 46, pp. 1049–1058, May 2011.
- [22] S. Rai, J. Holleman, J. Pandey, F. Zhang, and B. Otis, “A 500 uw neural tag with 2 uvrms afe and frequency-multiplying mics/ism fsk transmitter,” in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 212–213,213a, Feb 2009.
- [23] C. Ma, C. Hu, J. Cheng, L. Xia, and P. Chiang, “A near-threshold, 0.16 nj/b ook-transmitter with 0.18 nj/b noise-cancelling super-regenerative receiver for the medical implant communications service,” *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 7, pp. 841–850, Dec 2013.
- [24] Y.-H. Liu, C.-L. Li, and T.-H. Lin, “A 200-pj/b mux-based rf transmitter for implantable multichannel neural recording,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, pp. 2533–2541, Oct 2009.

- [25] Y.-H. Liu and T.-H. Lin, “A 3.5-mw 15-mbps o-qpsk transmitter for real-time wireless medical imaging applications,” in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp. 599–602, Sept 2008.
- [26] N. Cho, J. Bae, and H.-J. Yoo, “A 10.8 mw body channel communication/mics dual-band transceiver for a unified body sensor network controller,” *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 3459–3468, Dec 2009.
- [27] P. Bradley, “An ultra low power, high performance medical implant communication system (mics) transceiver for implantable devices,” in *Biomedical Circuits and Systems Conference, 2006. BioCAS 2006. IEEE*, pp. 158–161, Nov 2006.
- [28] Y.-H. Liu and T.-H. Lin, “An energy-efficient 1.5-mbps wireless fsk transmitter with a sigma delta - modulated phase rotator,” in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, pp. 488–491, Sept 2007.
- [29] Y.-H. Liu, L.-G. Chen, C.-Y. Lin, and T.-H. Lin, “A 650-pj/bit medradio transmitter with an fir-embedded phase modulator for medical micro-power networks (mmns),” *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 60, pp. 3279–3288, Dec 2013.
- [30] J. Bohorquez, A. Chandrakasan, and J. Dawson, “A 350 uw cmos msk transmitter and 400 uw ook super-regenerative receiver for medical implant communications,” *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 1248–1259, April 2009.
- [31] S. Cui, V. Acharya, and B. Banerjee, “An ultra-low power integer-n frequency synthesizer for mics transceivers,” *Microelectronics Journal*, vol. 42, no. 8, pp. 1018 – 1023, 2011.

- [32] J. Yang and E. Skafidas, “A low power mics band phase-locked loop for high resolution retinal prosthesis,” *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 7, pp. 513–525, Aug 2013.
- [33] D. Banerjee, “Pll performance simulation and design handbook (4<sup>th</sup> ed.),” 2006.
- [34] B. Razavi, *RF Microelectronics*. Upper Saddle River NJ: Prentice Hall, 2<sup>nd</sup> ed., 2011.
- [35] T. khan, “Subthreshold frequency synthesis for implantable medical devices,” Master’s thesis, Ryerson University, May 2010.
- [36] L. Zhang, B. Chi, Z. Wang, H. Chen, and E. Wu, “A low power 440-mhz pulse-swallow-divider combination synchronization-asynchronism-hybrid frequency divider,” in *Circuits and Systems, 2006. MWSCAS ’06. 49th IEEE International Midwest Symposium on*, vol. 2, pp. 566–568, Aug 2006.
- [37] H. Zhang, H. gang Yang, J. Zhang, and F. Liu, “High-speed programmable counter design for pll based on a delay partition technique,” in *Radio-Frequency Integration Technology, 2009. RFIT 2009. IEEE International Symposium on*, pp. 100–103, Jan 2009.
- [38] K.-Y. Kim, Y.-J. Min, S.-W. Kim, and J. Park, “Low-power programmable divider with a shared counter for frequency synthesiser,” *Circuits, Devices Systems, IET*, vol. 5, pp. 170–176, May 2011.
- [39] K.-C. Kuo and F.-J. Wu, “A 2.4-ghz/5-ghz low power pulse swallow counter in 0.18um cmos technology,” in *Circuits and Systems, 2006. APCCAS 2006. IEEE Asia Pacific Conference on*, pp. 214–217, Dec 2006.
- [40] X. Lei, Z. Wang, K. Wang, and X. Wang, “A high speed low power pulse swallow frequency divider for drm/dab frequency synthesizer,” in *Wireless Communications Signal Processing, 2009. WCSP 2009. International Conference on*, pp. 1–4, Nov 2009.

- [41] A. Abidi, “Phase noise and jitter in cmos ring oscillators,” *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 1803–1816, Aug 2006.
- [42] W.-H. Chen, W.-F. Loke, and B. Jung, “A 0.5-v, 440uw frequency synthesizer for implantable medical devices,” *Solid-State Circuits, IEEE Journal of*, vol. 47, pp. 1896–1907, Aug 2012.
- [43] N. Van Helleputte and G. Gielen, “An ultra-low-power quadrature pll in 130nm cmos for impulse radio receivers,” in *Biomedical Circuits and Systems Conference, 2007. BIOCAS 2007. IEEE*, pp. 63–66, Nov 2007.
- [44] R. Wessels, “Prototyping software to make things easy.” <https://energia.nu/>, 2015.
- [45] BugsLabInc, “Share your thing like it ain’t no thang.” <https://dweet.io/>, 2015.
- [46] BugsLabInc, “Visualize the internet of things.” <https://freeboard.io/>, 2015.
- [47] R. Meier, “Roger meier’s freeware.” <http://freeware.the-meiers.org/>, 2015.
- [48] K.-H. Cheng, Y.-C. Tsai, Y.-L. Lo, and J.-S. Huang, “A 0.5-v 0.4 - 2.24-ghz inductorless phase-locked loop in a system-on-chip,” *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, pp. 849–859, May 2011.
- [49] T.-S. Chao, Y.-L. Lo, W.-B. Yang, and K.-H. Cheng, “Designing ultra-low voltage pll using a bulk-driven technique,” in *ESSCIRC, 2009. ESSCIRC '09. Proceedings of*, pp. 388–391, Sept 2009.
- [50] J. Bae, N. Cho, and H.-J. Yoo, “A 490uw fully mics compatible fsk transceiver for implantable devices,” in *VLSI Circuits, 2009 Symposium on*, pp. 36–37, June 2009.
- [51] K. Kurdent, “Verilog ams.” <http://www.desingers-guide.com>, 2010.
- [52] CadenceInc, “Virtuoso spectre circuit simulator rf analysis user guide.” <http://www.Cadence.com>, 2007.

APPENDIX A

PHASE LOCKED LOOP PARAMETERS

TABLE A.1. Parameters of the PLL

Parameter	Variable
Gain of Charge Pump	$K_\phi$
Gain of VCO	$K_{VCO}$
Loop Bandwidth	$F_c$
Phase Margin of PLL	$\phi$
Input Reference Frequency	$F_{ref}$
Output Frequency	$F_{out}$
Divider Ratio	$N$
Loop Filter Poles	$T_1, T_3$
Loop Filter Zero	$T_2$
Ratio of Pole $T_3$ to Pole $T_1$	$T_{31}$
Natural Frequency	$\omega_n$
Damping Factor	$\zeta$

(8) 
$$\omega_c = 2\pi.F_c$$

(9) 
$$N = \frac{F_{out}}{F_{ref}}$$

$$(10) \quad T_1 = \frac{\sec(\phi) - \tan(\phi)}{\omega_c \cdot (T_{31} + 1)}$$

$$(11) \quad T_3 = T_1 \cdot T_{31}$$

$$(12) \quad T_2 = \frac{1}{\omega_c^2 \cdot (T_1 + T_3)}$$

$$(13) \quad C_t = \frac{K_\phi \cdot K_{\text{vco}} \cdot \sqrt{1 + (\omega_c \cdot T_2)^2}}{\omega_c^2 \cdot N \cdot \sqrt{[1 + (\omega_c \cdot T_1)^2] \cdot [1 + (\omega_c \cdot T_3)^2]}}$$

$$(14) \quad C_1 = \frac{T_1}{T_2} \cdot C_t$$

$$(15) \quad C_3 = \frac{C_1}{2}$$

$$(16) \quad C_2 = C_t - C_1 - C_3$$

$$(17) \quad R_2 = \frac{T_2}{C_2}$$

$$(18) \quad R_3 = \frac{T_3}{C_3}$$

$$(19) \quad \omega_n = \sqrt{\frac{K_\phi \cdot K_{vco}}{N \cdot C_t}}$$

$$(20) \quad \zeta = \frac{R_2 \cdot C_2}{2} \cdot \omega_n$$

$$(21) \quad LockTime = \frac{-\ln\left[\frac{tol}{f_2 - f_1} \cdot \sqrt{1 - \zeta^2}\right]}{\zeta \cdot \omega_n}$$

APPENDIX B

MATCHING NETWORK DESIGN

TABLE B.1. Matching Network Variables

<b>Parameter</b>	<b>Variable</b>
Bandwidth	$BW$
Center Frequency	$F_c$
Quality Factor	$Q$
Input Resistance	$R_{in}$
Load Resistance	$R_{ld}$
Intermediate Resistance	$R_i$
Quality Factor Right	$Q_R$
Quality Factor Left	$Q_L$
Capacitance Right	$C_R$
Capacitance Left	$C_L$

$$(22) \quad Q = \frac{F_c}{2.\pi.BW}$$

$$(23) \quad R_i = \left( \frac{\sqrt{R_{in}} + \sqrt{R_{ld}}}{Q} \right)^2$$

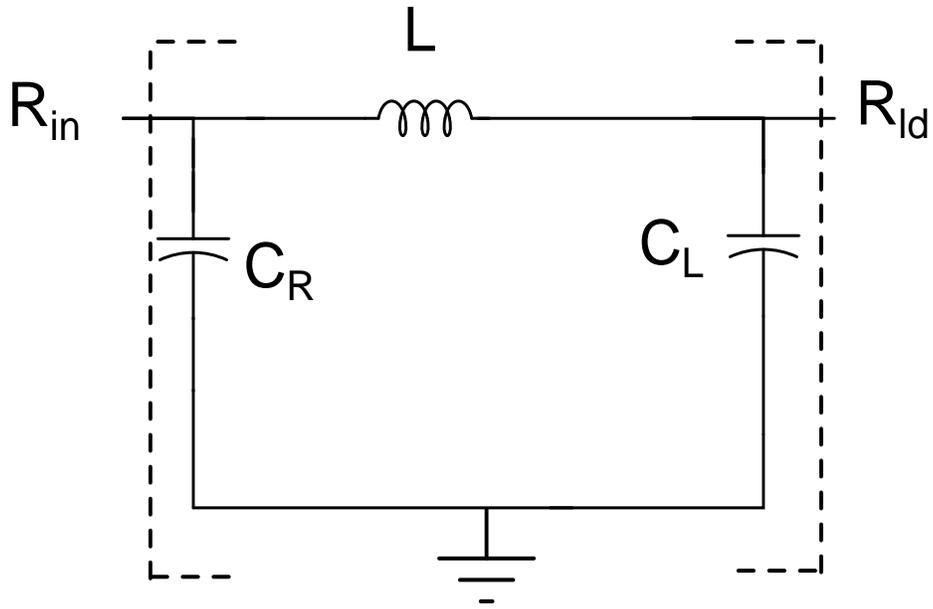


FIGURE B.1. Matching network

$$(24) \quad Q_R = \sqrt{\frac{R_{ld}}{R_i}}$$

$$(25) \quad Q_L = \sqrt{\frac{R_{in}}{R_i}}$$

$$(26) \quad C_L = \frac{Q_L}{2 \cdot \pi \cdot F_c \cdot R_{in}}$$

$$(27) \quad C_R = \frac{Q_R}{2 * \pi \cdot F_c \cdot R_{ld}}$$

$$(28) \quad L = \frac{Q \cdot R_i}{2 \cdot \pi \cdot F_c}$$

## APPENDIX C

### VERILOG CODE FOR COMPONENTS OF PHASE LOCKED LOOP

The blocks of the PLL were modeled in Verilog-ams for the top level fast simulation of the PLL using Analog-Mixed Signal (AMS) Simulator of the Cadence. The PFD and charge pump were modeled as in [51], shown in C.1. The code for divider is shown in C.2.

#### C.1. PHASE FREQUENCY DETECTOR AND CHARGE PUMP

```
'include "constants.vams"
'include "disciplines.vams"

module pfd_cp2(out, ref, fb);
output out;
electrical out;
input ref;
electrical ref;
input fb;
electrical fb;
parameter real iout=15u;
parameter real vh=1.8;
parameter real vl=0;
parameter real vth=(vh+vl)/2;
parameter integer dir=1 from [-1:1] exclude 0;
parameter real tt=1n from (0:inf);
parameter real td=0 from [0:inf);
```

```

integer state;

analog begin
@(cross(V(ref)-vth, dir))
    if (state > -1) state=state-1;
@(cross(V(fb)-vth, dir))
    if (state <1) state=state+1;
    I(out)<+ transition(iout*state, td ,tt);

if (V(out)> vh)
    I(out)<+ (V(out)-vh)/100;
else if (V(out)< vl)
    I(out)<+ (V(out)-vl)/100;

I(out)<+ V(out)/1T;

end

endmodule

```

## C.2. DIVIDER

```
% verilog HDL for functional simulation of Divider block
% N can be replaced by appropriate required division ratio.
module Divider_N (Clkin,Rst,Clkout);
input Clkin,Rst;
output reg Clkout;
integer counter;
initial
    begin
        counter=N;
    end
always@(posedge Clkin)
begin
    if(!Rst)
        begin
            counter=N;
            Clkout=0;
        end
    else
        if(counter==0)
            begin
                counter=N;
            end
        else
```

```
    if(counter<(N/2))
        begin
            counter=counter-1;
            Clkout=1;
        end
    else
        begin
            counter=counter-1;
            Clkout=0;
        end
    end
endmodule
```

## APPENDIX D

# PSS AND PNOISE ANALYSIS OF THE VCO

Various parameters like the signal strength, the phase noise, and the gain ( $K_{vco}$ ) of the VCO can be simulated using PSS and Pnoise analysis of the VCO [52]. The PSS and Pnoise setup for an independent VCO is shown in Figures D.1 and D.1, proper differential nets has to be chosen. Care has to taken as shown in Figures D.3 and D.4 to setup initial conditions for the oscillations to occur, and to save all the required nodes for the proper functioning of the simulator.

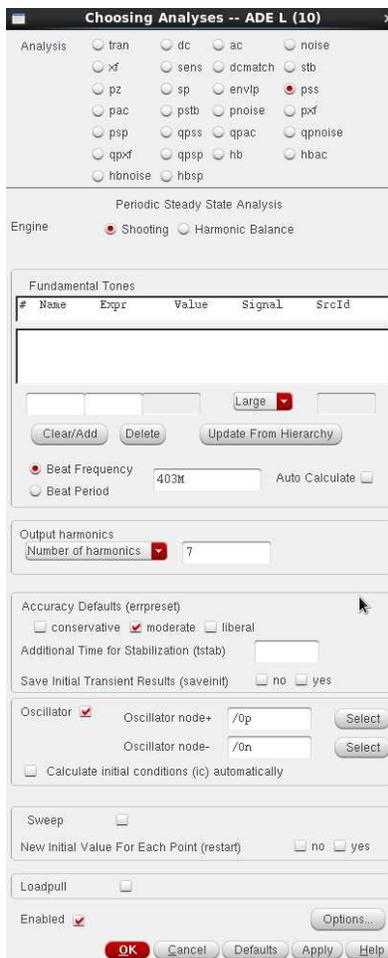


FIGURE D.1. Setup for PSS Analysis

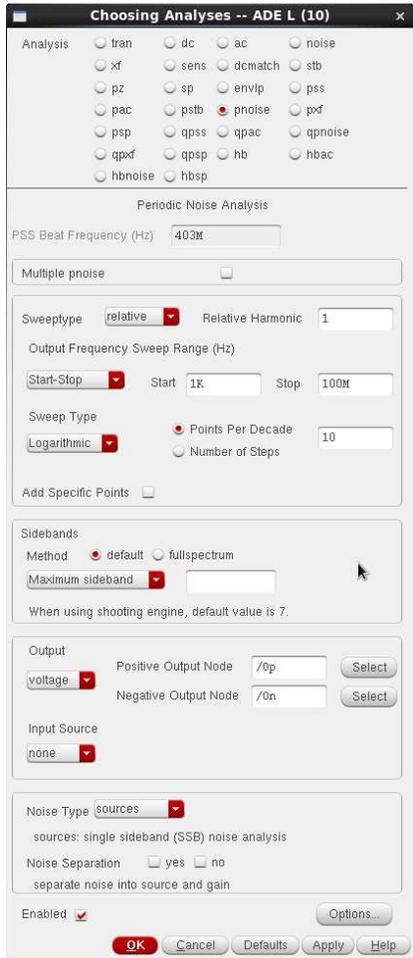


FIGURE D.2. Setup for Pnoise Analysis

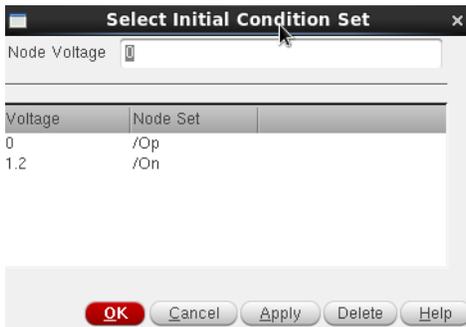


FIGURE D.3. Settings for VCO simulation

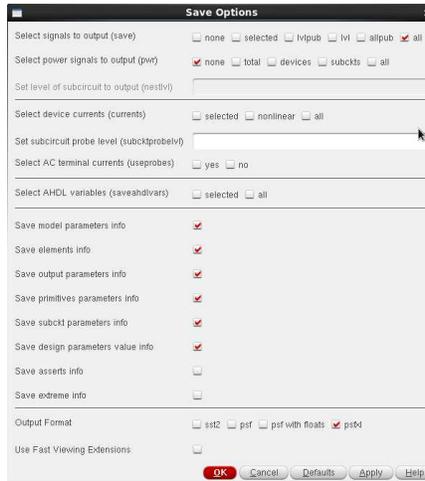


FIGURE D.4. Settings for VCO simulation

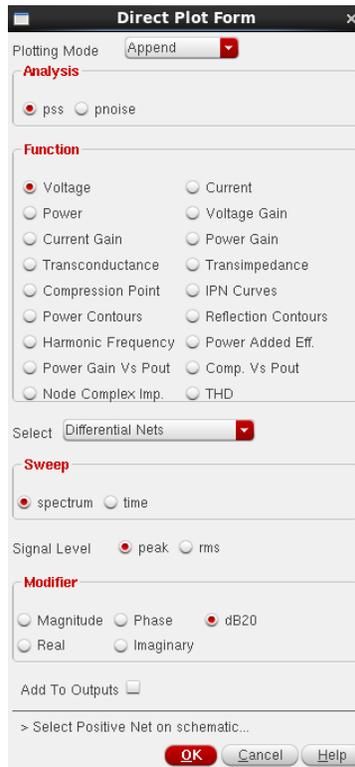


FIGURE D.5. PSS simulation output window

The window shown in Figure D.5 is obtained from Results → Direct plot → Main Form.

The outputs from the required PSS or Pnoise analysis can be chosen as shown in Figures D.5 and D.6.

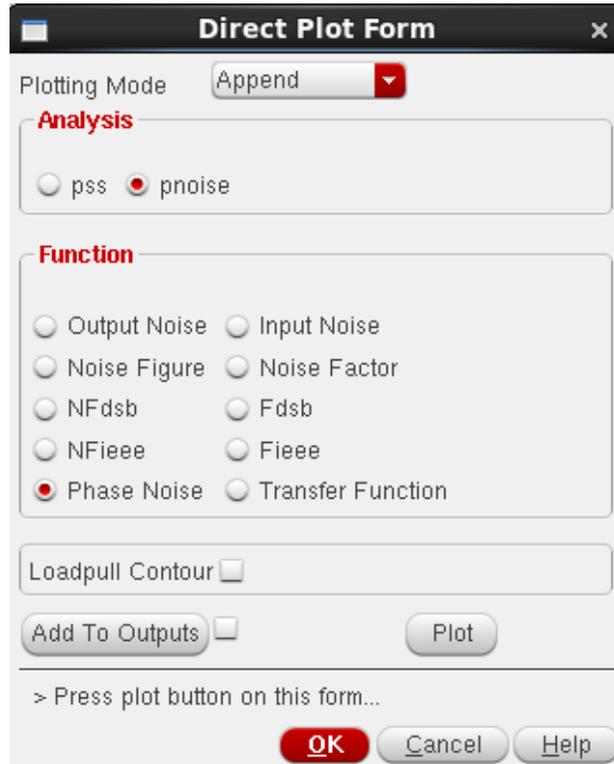


FIGURE D.6. Pnoise simulation output window

## APPENDIX E

# WIRELESS INTERFACE OF THE DEVICE AND CONNECTION

## TO INTERNET

### E.1. MSP430G2553

```
#include <SPI.h>

#include <AIR430BoostFCC.h>

#include <Wire.h>

// -----

/* Defines, enumerations, and structure definitions */

/* sPacket - packet format. */

struct sPacket

{ uint8_t message[59];    // Local node message [MAX. 59 bytes] };

// -----

/* Global data */

// Data to write to radio TX FIFO (60 bytes MAX.)

struct sPacket txPacket;

// variable for for loop

int i,j;

// variable to read incoming data

char inChar;

// variable to store incoming data

String dataString;

// -----
```

```

// Main

void setup(){

// The radio library uses the SPI library internally, this call initializes
// SPI/CSn and GDOO lines.

// Also setup initial address, channel, and TX power.

  Radio.begin(0x01, CHANNEL_1, POWER_MAX);

  memset(txPacket.message, 0, sizeof(txPacket.message));

// Setup serial for debug printing.

  Serial.begin(9600); }

void loop()

{  delay(960);

  if(Serial.read()=='$')

  {  for(i=0; i<8; i++)

    {  delay(20);

      inChar = (char)Serial.read();

      dataString += inChar;

      Serial.write(inChar); }  }

  String json = json + " ";

      json = json+ dataString;

  int payloadLength = json.length()+1;

  json.toCharArray((char*)txPacket.message, payloadLength);

  Radio.transmit

      (ADDRESS_BROADCAST, (unsigned char*)&txPacket,sizeof(txPacket));

  dataString="";          }

```

## E.2. CONNECTING TO INTERNET VIA WI-FI THROUGH CC3200

```
// Libraries

#include <SPI.h>

#include <WiFi.h>

#include <WiFiClient.h>

#include <AIR430BoostFCC.h>

// WiFi Client

WiFiClient client;

#define ADDRESS_LOCAL    0x01

/* sPacket - packet format. */

struct sPacket

{

    uint8_t from;// Local node address that message originated from

    uint8_t message[59];// Local node message [MAX. 59 bytes]

};

// Your network name also called SSID

char ssid[] = "your network name";

// your network password

char password[] = "your network password";

// your network key Index number (needed only for WEP)

int keyIndex = 0;

// Dweet parameters
```

```

char * server_name = "www.dweet.io";

#define thing_name "CapSensor"

// -----

/* Global data */

struct sPacket rxPacket;

// -----

void setup() {

    // Initialize serial communication

    Serial.begin(9600);

    // The radio library uses the SPI library internally,

    // this call initializes SPI/CSn and GDO0 lines.

    // Also setup initial address, channel, and TX power.

    Radio.begin(ADDRESS_LOCAL, CHANNEL_1, POWER_MAX);

    rxPacket.from = 0;

    memset(rxPacket.message, 0, sizeof(rxPacket.message));

    // attempt to connect to Wifi network:

    Serial.print("Attempting to connect to Network named: ");

    // print the network name (SSID);

    Serial.println(ssid);

    // Connect to WPA/WPA2 network.

    // Change this line if using open or WEP network:

    WiFi.begin(ssid, password);

    while ( WiFi.status() != WL_CONNECTED) {

        // print dots while we wait to connect

```

```

    Serial.print(".");
    delay(300);
}

    Serial.println("\nYou're connected to the network");
Serial.println("Waiting for an ip address");
    while (WiFi.localIP() == INADDR_NONE) {
        // print dots while we wait for an ip address
        Serial.print(".");
        delay(300);
    }
}

void loop() {
    delay(1000);

    // Turn on the receiver and listen for incoming data.

    // Timeout after 1 seconds.

    // The receiverOn() method returns the number of bytes copied to rxData.
    if (Radio.receiverOn
        ((unsigned char*)&rxPacket, sizeof(rxPacket), 1000) > 0) {
        digitalWrite(RED_LED, HIGH);
        Serial.print("FROM:");
        Serial.print(rxPacket.from);
        Serial.print(" MSG:");
        Serial.println((char*)rxPacket.message);
        digitalWrite(RED_LED, LOW);    }
}

```

```

// Send data to server

if (client.connect(server_name, 80)) {

    Serial.println("Connected");

    Serial.print(F("Sending request... "));

    client.print(F("GET /dweet/for/"));

    client.print(thing_name);

    client.print(F("?CapSensor="));

    client.print(F(rxPacket.message));

    client.println(F(" HTTP/1.1"));

    client.println(F("Host: dweet.io"));

    client.println(F("Connection: close"));

    client.println(F(""));

    Serial.println(F("done."));      }

// Read answer

Serial.println(F("Reading answer..."));

while (client.connected())      {

    while (client.available()) {

        char c = client.read();

        Serial.print(c);          } }

Serial.println(F(""));

// Close connection

client.stop();

Serial.println(F("Closing connection"));

Serial.println(F(""));      }

```