# An Electrothermal Model of Memory Switching in Vertical Polycrystalline Silicon Structures

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*Abstract*—**A previous publication described an experimental investigation of memory switching in vertical thin-film structures formed in polycrystalline silicon. An electrothermal model of switching in those structures is presented here. The theoretical preswitching temperature, resistivity, and current density distributions within the device were obtained from the solution of the transient two-dimensional heat equation. The results of the computer simulation, obtained for the case where conductivity is dependent on both temperature and electric field, show that current crowding occurs at the center of the device and that thermal runaway develops in a few tens of nanoseconds for voltages above a critical value. A simulated conductive irregularity forces the filament to nucleate away from the center and closer to or at the inhomogeneity. The excellent agreement between the experimental data and the simulation lends support to the idea that the fundamental switching mechanism is thermal in nature.**

## I. INTRODUCTION

MEMORY switching, a permanent transition to a lower resistance state, has been observed in an extremely large variety of materials [1]–[3], including polycrystalline silicon (polysilicon) [4]–[8] and amorphous silicon [9], [10]. It is well accepted that switching may occur due to Joule heating of the structure, resulting in the formation of a crystallized or recrystallized filament within the semiconducting material [11]. The filament is relatively more conductive and therefore the structure assumes a higher conductance state (sometimes referred to as the "ON" or the "programmed" state).

A detailed experimental study of memory switching in vertical $n^+$-i-$n^+$ structures formed in polysilicon thin films was reported earlier by us [6]. The initial state had a very high resistance, with transport being dominated by polysilicon grain boundary potential barriers. It was shown that an increase in conductance by a factor of approximately $10^5$ can be achieved with a suitable voltage pulse. A delay of several microseconds was observed at near-threshold voltages, which decreased to the order of nanoseconds with over-voltages of only a few volts. A moderately doped filamentary region, which formed as a result of "programming," exhibited single-crystal silicon transport phenomena.

There are several mechanisms, both electronic and thermal, that can induce memory switching in thin films. Such mechanisms have been used in attempts to explain threshold switching characteristics in chalcogenide glasses [12]–[15]. For a thermal mechanism, in materials that have a thermally activated conductivity ($\sigma$), i.e.,

$$\sigma = \sigma_0 \exp(-E_a/kT) \tag{1}$$

(where $E_a$ is the activation energy, $k$ is Boltzmann's constant, $T$ is the temperature, and $\sigma_0$ is the pre-exponential conductivity term) an unstable situation arises when the rate of energy input exceeds the capacity of the system to dissipate it. This occurs because of a positive feedback mechanism that in the region of instability allows the system to carry larger and larger currents with a constant applied voltage. Such a feedback loop is shown in Fig. 1. The essential link is the sensitivity of the conductivity to temperature, a negative temperature coefficient of resistance being required. The larger the value of the activation energy, the greater is the tendency toward instability.

A simple experiment, determining the thickness dependence of the threshold voltage, helps distinguish purely electronic mechanisms from purely thermal processes [16]–[18]. Switching due to bulk electronic properties of the film requires a critical electric field, leading to a linear increase of programming voltage with thickness. However, for a mechanism based on Joule heating the threshold voltage is proportional to the square root of the thickness. This can be easily derived in the following way: thermal instability is initiated at a critical threshold voltage $V_c$ when the rate of heat generation is equal to the rate of dissipation

$$I_c V_c = A V_c^2 \sigma / h = D \tag{2}$$

where $I_c$ is the threshold current, $A$ is the area and $h$ is the thickness of the film. Since the dissipation term $D$ varies only very slightly with the film thickness, it can be assumed to be independent of thickness. Therefore

$$V_c \propto (h)^{1/2}. \tag{3}$$

None of the investigations of silicon thin films in the past, however, have been supported with a detailed study of the switching mechanism(s). We present below a model

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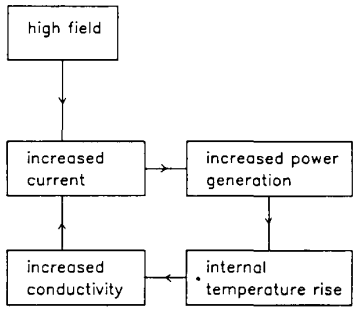



Fig. 1. Positive feedback loop leading to thermal runaway.

based on the process of thermal runaway that successfully predicts several features of memory switching in polysilicon films. The fundamental questions addressed in this article are: What determines the programming voltage? What is the cause for the delay observed during programming at voltages slightly over the threshold? Is the position of a filament predictable? In brief, what is the programming mechanism?

## II. Thickness Dependence of the Threshold Voltage

That the switching mechanism is thermal in nature in our polysilicon structures was originally suggested to us by two points of observed thickness dependence for the programming threshold voltage, as shown in Fig. 2. An average programming voltage for devices with an effective thickness (after subtracting the heavily doped regions [6]) of 4000 Å is approximately 18 V, as compared to 15 V for 2000-Å-thick films. The vertical bars in the figure indicate the total spread of programming voltages over which the averages were calculated and the horizontal bars, the potential error in thickness measurements. The approximate square root dependence of threshold voltage with the thickness is qualitatively in accordance with the thermal mechanism discussed above.

For an electronic mechanism, a linear fit to the experimental data is expected; perhaps the process really is electronic and the curvature in Fig. 2 is due to an extraneous series resistance. A linear fit using the absolute limits of the error bars, so as to minimize the voltage intercept, results in a minimum possible intercept of 5.5 V, as shown in the figure. It is most unlikely that there is a series resistance big enough to cause this; the initial state current–voltage characteristic of the devices is that of the polysilicon film itself [6]; thus, a thermal mechanism is suggested by Fig. 2.

Similar results were also obtained for structures formed in amorphous silicon and are presented in the Appendix. In addition, Dey [10] has investigated Ti-Si-Ti sandwich structures formed in amorphous silicon. An electrothermal switching model, similar to ours, was suggested for those devices by the author.

## III. Formulation of the Computer Model

To evaluate whether a given applied voltage will lead to an instability, one must calculate the temperature increase while accounting for the relevant modes of heat generation and dissipation. In our case, this was accomplished by solving the time-dependent thermal-conduction equation, with suitable boundary conditions.

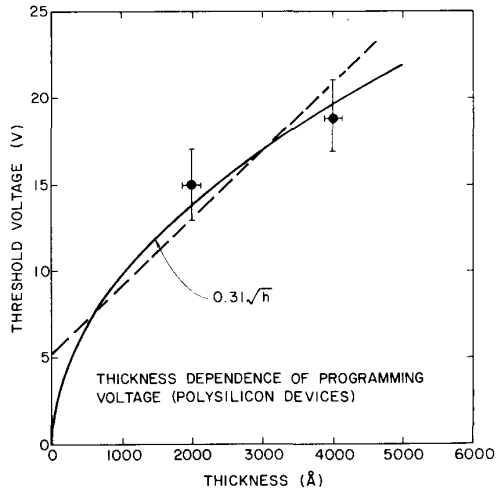



Fig. 2. Threshold voltage versus effective thickness (2000 and 4000 Å).

$$\partial/\partial x\left[K(x, y)\partial T/\partial x\right] + \partial/\partial y\left[K(x, y)\partial T/\partial y\right] + \sigma E^2 = d(x, y)\, C(x, y)\partial T/\partial t \quad (4)$$

where $T$ is the temperature, $K$ is the thermal conductivity, $d$ is the mass density, $C$ is the heat capacity, and $E$ is the applied electric field.

The geometry of the device used in the computer simulation is shown schematically in Fig. 3. There is one obvious difference in this structure when compared to the experimental devices as described in [6]—the tungsten layer, interposed between aluminum and polysilicon. This tungsten layer was included in the model because it was found to be a valuable addition to the fabrication process; it was obtained experimentally by selective tungsten chemical vapor deposition. It was found to be effective in tightening the distribution of programming characteristics in the experimental devices and it allowed a contact alloying step by preventing the shorting of the device that would otherwise occur upon alloying. Repeated controlled experiments have shown that the tungsten barrier layer has absolutely no effect on the devices' terminal characteristics. Neither does it fundamentally affect the memory switching mechanism.

The two-dimensional case was chosen to include heat flow both parallel and perpendicular to the direction of current. The boundaries of the figure (top surface of the aluminum layer, bottom surface of the substrate, and the left and right sides) were assumed to be at 300 K.

Such boundary conditions have been employed with good results in simulations done on chalcogenide glasses [19]–[21] and may be seen to be reasonable from the following considerations: 1) The experimental wafers were held tightly on a room temperature vacuum chuck. 2) The conduction of heat from the sides is limited by the rela-

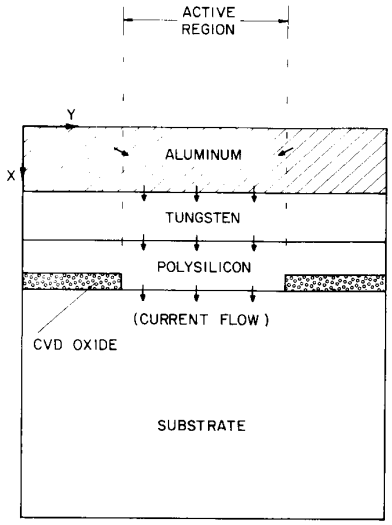



Fig. 3. Device geometry used in the computer model; assumed current flow is shown by the arrows.

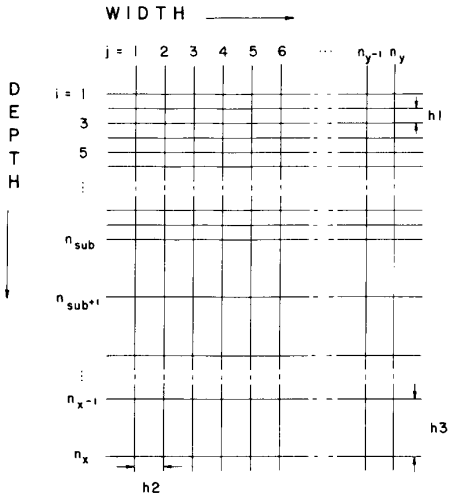



Fig. 4. Grid pattern used to discretize the device.

tively small surface area of the sides of the active region, and the fact that $SiO_2$ forms part of the material surrounding the active region. (The thermal conductivity, the heat capacity and the density values of the various layers are summarized in Table I (see [25]); the temperature dependences of these physical constants were neglected in the model.) 3) It will be shown that thermal runaway accelerates enormously at only a few tens of degrees higher than the ambient temperature. This means that only moderate temperature gradients are possible prior to switching; during thermal runaway, boundary conditions have little effect on peak temperatures internal to the devices.

The current was allowed to flow from the top contact to the substrate only in the active region of the device (as defined in Fig. 3). For a given applied voltage, the value of the current was determined by the resistance of the polysilicon film only; the resistances of the substrate, aluminum, and tungsten layers were considered to be negligible. All contact resistances were neglected in the simulation because they were found experimentally to be insignificant when compared to that of the polysilicon layer.

The dependence of conductivity on temperature and the composite device structure together make the solution of the problem very complicated. The boundary value problem does not have analytical solutions, and therefore a fully implicit numerical technique known as the Crank–Nicolson method [22] was used. The computational mesh is shown in Fig. 4. Two different vertical grid spacings $h_1$ (0.01 $\mu$m) and $h_3$ (20 $\mu$m) were used. This was necessary in order to maximize the efficiency of the program without sacrificing resolution in the active region. For mesh points at the boundaries of two or more layers in the device structure, average property values were used.

The solution was obtained numerically [22, p. 85]. The flow chart is shown in Fig. 5. The theoretical current–voltage characteristic was then obtained from the simulation results for each input voltage assumed.

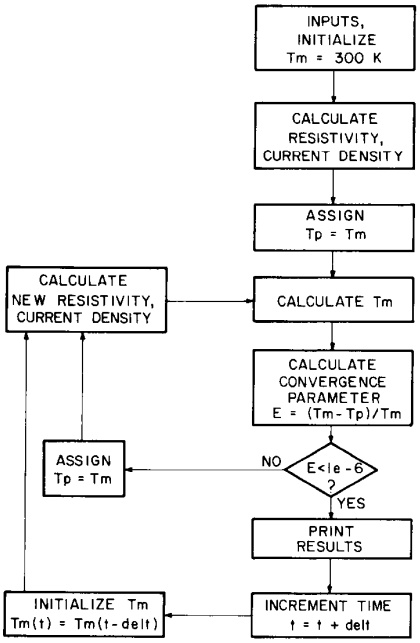



Fig. 5. Flow chart of the algorithm used to calculate the temperature, resistivity, and current density.

TABLE I
THERMAL PROPERTIES
(See [25].)

| | density ($g/cm^3$) | thermal conductivity (watts/cm-K) | heat capacity (J/g-K) |
|---|---|---|---|
| Aluminum | 2.63 | 2.37 | 0.896 |
| Tungsten | 19.4 | 1.63 | 0.134 |
| Polysilicon | 2.33 | 0.3 | 0.95 |
| Silicon (Substrate) | 2.33 | 1.5 | 0.95 |
| Silicon dioxide | 2.22 | 0.014 | 0.75 |

## IV. Simulation Results

The solutions of the heat equation and consequently the derived current–voltage characteristics were obtained for the following two conditions: 1) conductivity dependent on temperature only, and 2) conductivity dependent on both temperature and electric field. A model based on the former case is known as a "thermal model," while in the latter case it is referred to as an "electrothermal model" [21].

For polycrystalline silicon, it is generally accepted that the superlinear current–voltage behavior of resistors is due to an electronic process proposed by Korsch *et al.* [23], the thermionic emission of carriers over potential barriers at the grain boundaries. This leads to the "sinh" behavior in the current–voltage characteristics, with a strong field dependence of the conductivity, as observed experimentally [6]. Therefore, a purely thermal model of switching for polysilicon devices, with conductivity independent of the electric field, should be unrealistic. Nevertheless, we were not aware of an explicit check on heating effects as a possible origin of the superlinear behavior. The calculation is useful also for giving a perspective on the importance of heating effects.

### A. Field-Independent Conductivity

In this case, the conductivity was considered to be thermally activated as given by (1). The activation energy was assumed to be independent of applied field, and a zero-field value of 0.56 eV was used in the simulation (see [6, Fig. 4]).

To compare the theoretical and experimental results, representative experimental data for a 2 × 3 square micron area device (2000-Å effective polysilicon thickness) are plotted in Fig. 6. The experimental data points, which may be fitted quite well with a "sinh" characteristic, were taken from an actually continuous curve and plotted as shown for ease of illustration. The "turn-on" in the experimental current–voltage characteristic occurs at approximately 1 to 2 V, with the programming event at 15 V and 0.6 mA.

The theoretical curve for the simulated device exhibits almost perfectly ohmic behavior with only very slight heating at relatively high voltages. The maximum calculated temperature within the device at 50 V was 302 K, an increase of only two degrees above the assumed room temperature.

Thus, the contribution of heating to the observation of the "sinh" characteristic in the initial state is negligible and this simulation lends support to the accepted grain boundary potential barrier model. Furthermore, the purely thermal model does not predict memory switching at reasonable voltages in our devices.

### B. Field-Dependent Conductivity

The role of an electronic mechanism upon the superlinear preswitching current–voltage characteristics of our devices, therefore, is very important. Since a purpose of the model is to estimate the increase in temperature within the device, and to suggest the fundamental switching mechanism(s), an empirical relation for $\sigma(T, E)$ having a sound physical basis is needed.

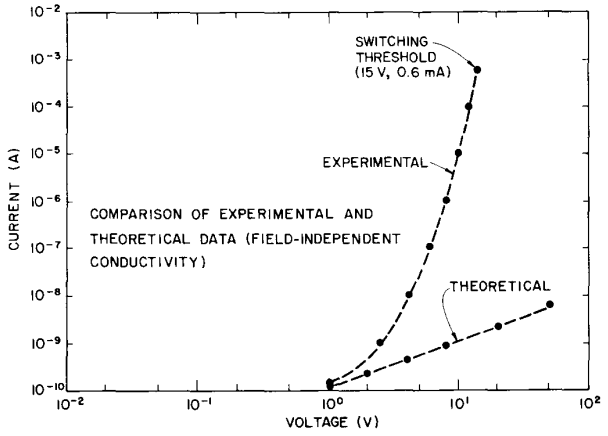



Fig. 6. Experimental and theoretical current–voltage characteristics of a 2 × 3 square micrometer device; field-*independent* conductivity assumed in model.

The empirical form of conductivity used in the simulation was

$$\sigma = \sigma_0 \exp(-E_a/kT) \exp(V_a/V_0) \tag{5}$$

where $V_a$ is the applied voltage and $V_0$ is a parameter depending on the conduction mechanism itself. This exponential variation with voltage is, to a very good approximation, that of the grain boundary potential barriers. The current density equation was

$$J = \sigma V_a/L \tag{6}$$

where $L$ is the thickness of the device. At low bias ($V_a \ll V_0$) the current varies approximately linearly with voltage; however, at high bias ($V_a \gg V_0$) it increases exponentially. The onset voltage of nonohmic behavior is determined by $V_0$. The value of this parameter depends upon the thickness of the film, and therefore also on the apparent number of grains ($N_g$) present.

In the grain boundary potential barrier model

$$V_0 = 2N_g kT/q \tag{7}$$

where $q$ is the electronic charge. The experimental current–voltage characteristic for the 2 × 3 $\mu m^2$ area device discussed above was curve-fitted using a value of 0.95 V for $V_0$ and the rest of the parameters being the same as before. The number of grains calculated using the above equation is 19.

Fig. 7 shows the theoretical data in open circles together with the same experimental data as in Fig. 6. The maximum temperature within the device at steady state is given for each theoretical point. The simulation indicates that there is no appreciable heating in the sample up to approximately 13 V. For voltages larger than ~ 13 V, the increase in temperature becomes significant and also very sensitive to the applied bias. A steady-state maximum temperature of 315 K is reached within the device for an applied voltage of 13.2 V. At a higher voltage (13.35 V,

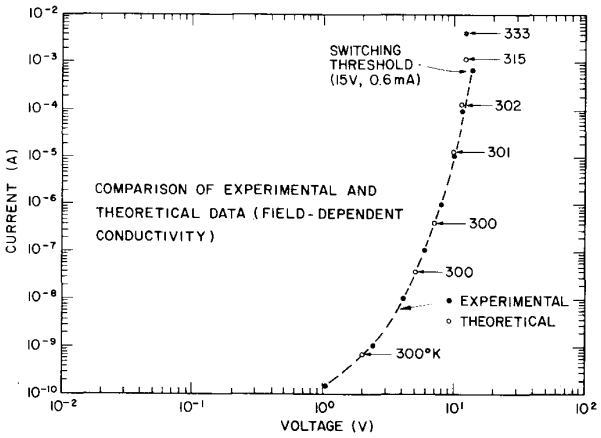



Fig. 7. Experimental and theoretical current-voltage characteristics of a 2 × 3 square micrometer device; field-*dependent* conductivity assumed in model.

corresponding to 333 K), a thermal instability occurs leading to temperature and current runaway with no steady-state solution. This datum point, shown in Fig. 7 as a star, is unlike all the others. The values for current and temperature after approximately 35 ns, rather than the steady-state value, were plotted. The theoretical switching threshold voltage therefore, lies between 13.2 and 13.35 V. This value is remarkably close to the threshold value observed experimentally (15 V).

It should be recognized that the theoretical threshold voltage will depend upon the boundary conditions used in the simulation. Our results were obtained, as explained above, under the assumption that the boundaries of the device are held at 300 K. This by itself should lead in principle to an overestimate of the threshold voltage. On the other hand, the model is only two-dimensional, rather than three-dimensional as are the real devices. This fact should compensate for the assumed boundary conditions to some extent, pushing the computer simulation in the direction of an underestimate of the programming voltage, which was actually the case.

The onset of the thermal instability occurs in the simulation with the maximum stable temperature only a few tens of degrees above room temperature. Similar behavior has been noted in electrothermal models for chalcogenide glasses. Simulations performed under boundary conditions similar to ours by Kroll and Cohen [19] show an increase of only 21.8 degrees above room temperature before the switching event. The threshold voltage in their case was around 11 V. The results obtained by Kaplan and Adler [21] show a maximum temperature of only 340 K before the negative resistance transition.

The process of thermal runaway is extremely fast, with calculated temperatures rising higher, in a fraction of a microsecond, than any conceivable recrystallization temperature of polycrystalline silicon, and the current being localized in the centre of the device. In real devices, however, the temperature cannot rise to such values because recrystallization will occur first, causing a permanent change in the structure (as seen experimentally in the formation of a single-crystalline silicon filament). This will cause the device conductance to increase by several orders of magnitude, and cause most of the current to channel through the localized region, thus cooling the surrounding area and stabilizing the process. Experimentally, the maximum current in the device during programming was limited by a series resistor in the circuit [6, Fig. 13].

The spatial and transient developments of the current filament within the device were obtained as temperature and current density profiles at incremental time steps. The results discussed below are for applied voltages of 13.2 and 13.35 V, the two highest points in Fig. 7. They represent the following conditions in regard to switching: 1) applied voltage less than the threshold voltage, and 2) applied voltage greater than the threshold voltage.

*1) Applied Voltage Less Than the Threshold Voltage:* The computed variations in temperature and current density with time, at 13.2 V, are presented in Figs. 8 through 10. The two-dimensional temperature distributions at 0.001, 0.01, and 0.1 $\mu$s are shown in Fig. 8. The apparent sharp drop in temperature in the substrate is not, in fact, sharp at all; this appearance is due to the sudden increase in grid spacing (the grid spacing increases from 0.01 to 20 $\mu$m).

Since the resistances of the aluminum, tungsten, and the substrate were assumed to be negligible, the heat generation occurs in the polycrystalline silicon layer only. Consequently, the temperature rise is mainly in this layer. At 1 ns, a maximum temperature of about 302 K occurs at the centre of the film (Fig. 8(a)), with the profile having a flat top. As time progresses (Fig. 8(b) and (c)) the temperature increases with the profile peaking at the center of the device but shifting closer to the substrate. A steady-state condition is reached before 0.1 $\mu$s, with the maximum temperature being 315 K, as indicated by no further change in temperature after this time. The "thermal time constant" of the device is dominated by the substrate, which has a relatively low thermal conductivity and an enormous mass as compared to the aluminum and tungsten layers.

The development of the temperature depth profile is shown with a plot of the temperature at the center of the device as a function of depth, in Fig. 9(a). The figure includes only a part of the profile in the substrate. The maximum temperature point shifts from the center of the polysilicon layer toward the substrate as steady state is attained. The variations in slope in going from one layer to the next are due to the differences in thermal conductivities.

The current crowding effect is illustrated in Fig. 10(a). The current density at 0, 0.001, 0.01, and 0.1 $\mu$s is plotted as a function of position along the width. Initially, the current is uniformly distributed over the device area. As time passes, the central region of the device heats more than the sides, causing the resistivity to be relatively lower there. For a fixed applied voltage, more current flows through this region, heating it even further. A steady state is reached when the rate of heat dissipation becomes equal to the rate at which heat is generated in the device. It is

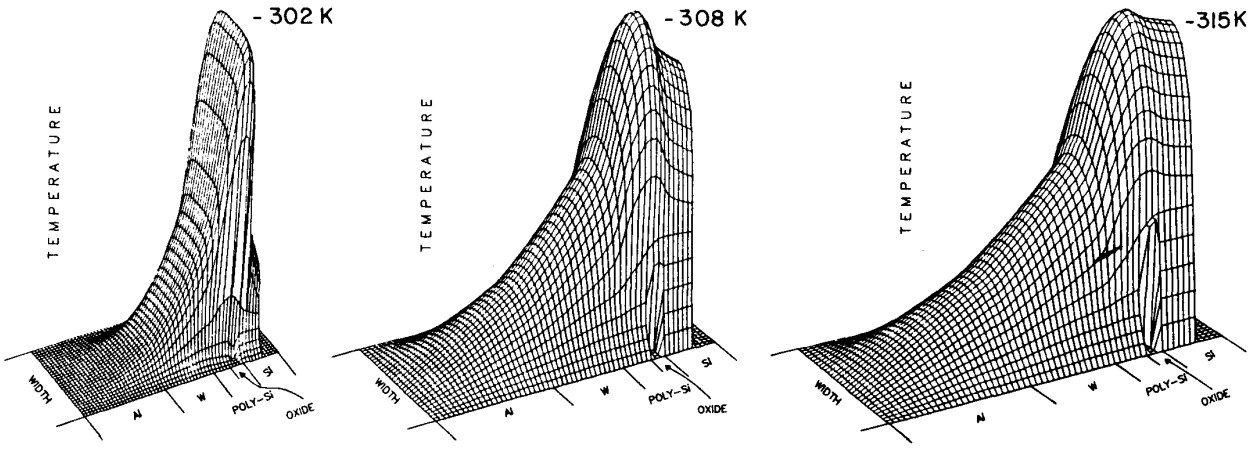



Fig. 8. Calculated two-dimensional temperature distributions (at 13.2 V) in a 2 × 3 square micrometer area device (a) after 0.001 μs (the maximum temperature is approximately 302 K), (b) after 0.01 μs (the maximum temperature is approximately 308 K), and (c) after 0.1 μs (the maximum temperature is approximately 315 K).

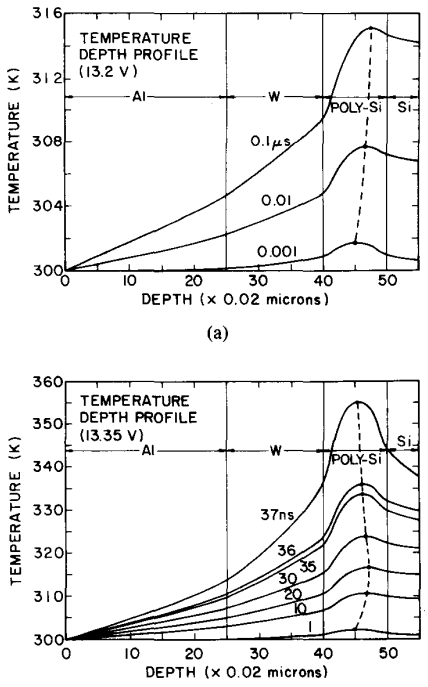



Fig. 9. Theoretical transient temperature depth profile of a 2 × 3 square micrometer area device (a) at 13.2 V and (b) at 13.35 V.

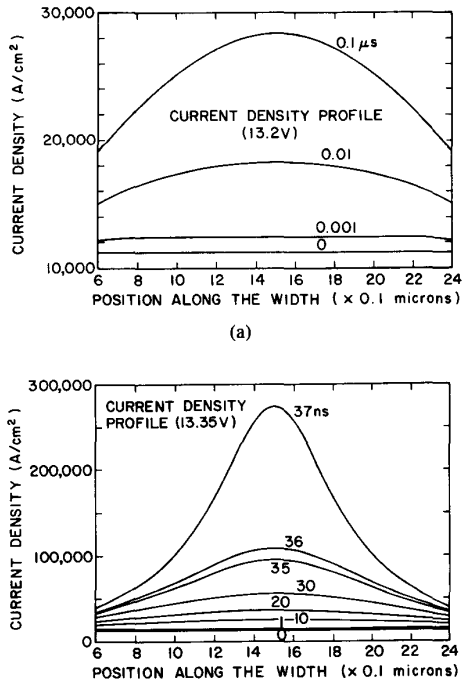



Fig. 10. Calculated current density versus position along the width of a 2 × 3 square micrometer area device for (a) 13.2 V and (b) 13.35 V.

at this point that the temperature stabilizes, resulting in no further increase in current. In this instance, the total current had doubled upon reaching essentially steady state at 0.1 μs.

*2) Applied Voltage Greater Than the Threshold Voltage:* The results presented in this section are for an applied voltage of 13.35 V. Thermal runaway occurs, with temperature continually increasing with time.

The two-dimensional temperature distribution after 37 ns is shown in Fig. 11. There is a sharp peak at the centre of the device with the highest temperature being about 355 K. A depth profile of the temperature at the center of the device as a function of time is plotted in Fig. 9(b). The maximum temperature in the film rises from 300 to about 336 K in 36 ns, at which point thermal runaway greatly accelerates. In the following 1 ns, the temperature increases to 355 K and accelerates even further. An interesting point to note is the shift in the peak temperature position within the polysilicon layer. The maximum in temperature shifts from the center of the film toward the polysilicon–substrate interface, and then back to the center of the film. This effect suggests that the substrate does

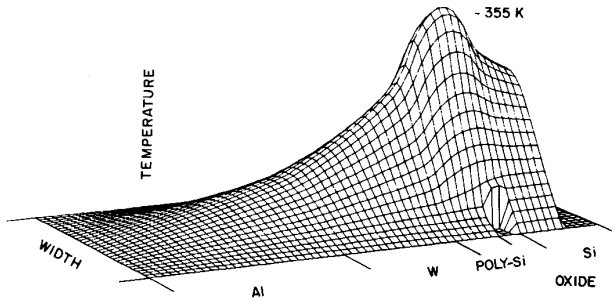



Fig. 11. Theoretical two-dimensional temperature distribution (at 13.35 V) in a 2 × 3 square micrometer area device after 37 ns.

not act as an effective heat sink after 36 ns, when the rate of heat generation in the film considerably exceeds the capacity of the system to dissipate it.

The crowding of current at the center of the device is shown in Fig. 10(b). The total current increases from 0.76 to 7.5 mA in 37 ns. The sharp peak in the current density profile at 37 ns suggests filamentary conduction with most of the current being localized in the central region of the device. It is this hot region that is likely to recrystallize. The formation of such a filamentary region in the center of an homogeneous silicon-on-sapphire film has also been predicted through numerical solutions of the heat equation by Pontius *et al.* [24].

The transient response of the device is shown in Fig. 12(a). The simulated device exhibits a relatively small increase in conductance until approximately 36 ns. This increase in conductance corresponds to the steady decrease of voltage across the device as seen experimentally during actual programming transients [6, Fig. 12(a)]. For better comparison, a voltage transient characteristic was simulated using the data of Fig. 12(a) and including an external series resistance as was done experimentally in [6]. With an initial conductance value of $5.69 \times 10^{-5}$ ℧ for the device and a series resistance of 980 Ω, a 14.09-V pulse is required to achieve 13.35 V across the device. If we allow the voltage across the device to change with time (note that this voltage was kept constant for the simulation) because its resistance varies, then

$$V_d(t) = V_p R_d(t)/(R_s + R_d(t)) \qquad (8)$$

where $R_s$ is the series resistance, $R_d(t)$ is the device resistance, $V_d(t)$ is the device voltage, and $V_p$ is the input voltage. The calculated voltage across the device along with the required input voltage are plotted in Fig. 12(b).

The general shape of the theoretical transient in Fig. 12(b) resembles the part of the transient up to the switching event as observed experimentally [6, Fig. 12(a)]. The voltage across the device decreases steadily with time until switching occurs. However, the theoretical delay associated with switching is only a few tens of nanoseconds. Several assumptions acting together caused the delay time to be underestimated by the simulation: 1) The value for the activation energy of the conductivity used in the simulation was the zero-field value of 0.56 eV, whereas in reality it decreases with applied voltage (see [6, Fig. 4]);

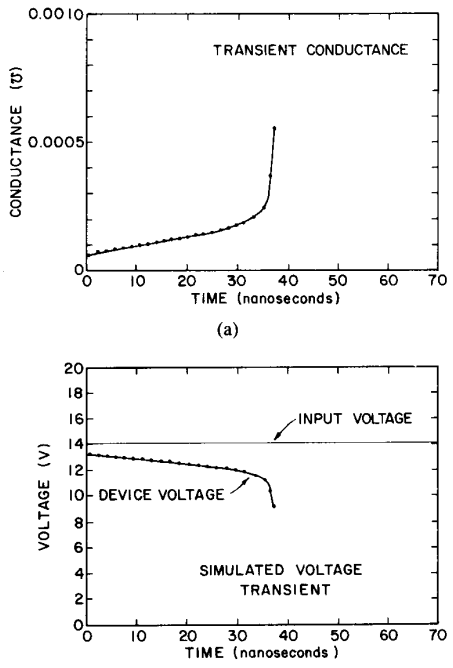



Fig. 12. (a) Conductance versus time for an applied voltage of 13.35 V; (b) simulated voltage transient for the 2 × 3 square micrometer device for the circuit described in the text; the input voltage is also shown.

and 2) the voltage across the device is held constant in the simulation, whereas it decreases slightly with time in the actual experiments.

The results of the simulation presented above for an homogeneous device predict the formation of a filament at the exact center of the structure. However, in the presence of inhomogeneities (arising due to the surface roughness), this may not be the case. The effect of a relatively conductive inhomogeneity upon the position of the filament was obtained from another simulation and is discussed next.

### C. Effects of a Relatively Conductive Inhomogeneity

A geometric irregularity was introduced in a 6 × 3 $\mu m^2$ area device by shortening a strip (to 70 percent of its original length) 1.8 $\mu$m away from the center. Therefore, a higher current density was achieved in this particular strip due to its lower resistance. However, the increase in total current due to the inhomogeneity itself as compared to an homogeneous device was relatively small. At 300 K and 13.4 V, the total current is 2.47 mA as compared to 2.41 mA in a similar structure without the inhomogeneity.

Fig. 13 shows the temperature and current density width profiles at an applied voltage of 13.4 V for such a structure as a function of time. As seen in Fig. 13(a), initially the current density at the inhomogeneity is just slightly higher than anywhere else. However, as time progresses, a sharp current filament forms at the inhomogeneity. The current increases from 2.47 to 13.7 mA in 65 ns, and subsequently increases at an even faster rate.

The corresponding temperature profile shown in Fig.

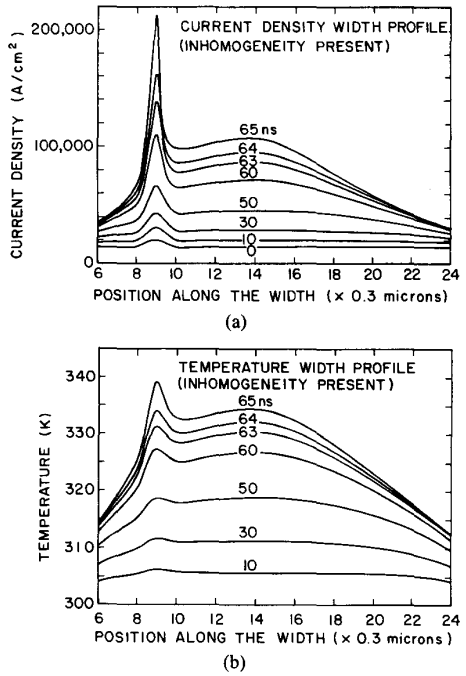



Fig. 13. Transient (a) current density and (b) temperature (at 13.4 V) versus position along the width of a 6 × 3 square micrometer area device having a geometrical inhomogeneity.

13(b) gives the temperature at the center depth of the film along the width of the device. The figure clearly shows that the temperature at the inhomogeneity progressively becomes higher and higher than the temperature at the center of the film. Thermal runaway accelerates after a delay of about 60 ns with the temperature at the inhomogeneity increasing at a faster rate than in other locations. Therefore, in this instance recrystallization is likely to occur at the inhomogeneity itself. This is in contrast to the homogeneous devices where the maximum temperature occurs in the exact center of the device.

The actual position of the peak temperature will depend upon the magnitude of the inhomogeneity. In a device having a severe inhomogeneity, resulting in a locally high current density as just illustrated, filamentation will occur at the inhomogeneity itself. For a moderate inhomogeneity, however, the current filament and the corresponding peak in temperature may occur somewhere between the position of the inhomogeneity and the center of the device [24].

In experimental polysilicon devices, we observed that the filaments mostly occur near the perimeter of the device and therefore are probably controlled by severe inhomogeneities. However, in amorphous silicon devices, which may be expected to be more nearly homogeneous on the microscopic scale, the filaments usually formed near to the center of the device as shown experimentally in the Appendix.

## V. Summary and Conclusions

A computer model based on an electrothermal mechanism is found to be sufficient in explaining experimental features of memory switching in polysilicon devices. The theoretical current–voltage characteristic, with a temperature- and field-dependent conductivity, exhibits thermal runaway at a critical voltage close to that observed experimentally. The simulated thermal runaway itself is extremely fast with spontaneous crowding of current at the center of a homogeneous device. A relatively conductive inhomogeneity causes the current filament to form away from the centre and closer to (or at) the inhomogeneity. Since it is observed that filaments occur near the perimeter in polysilicon structures, the position of the filaments is probably controlled by inhomogeneities in those devices.

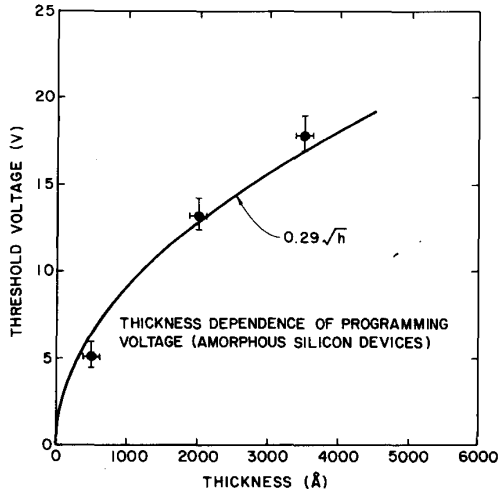
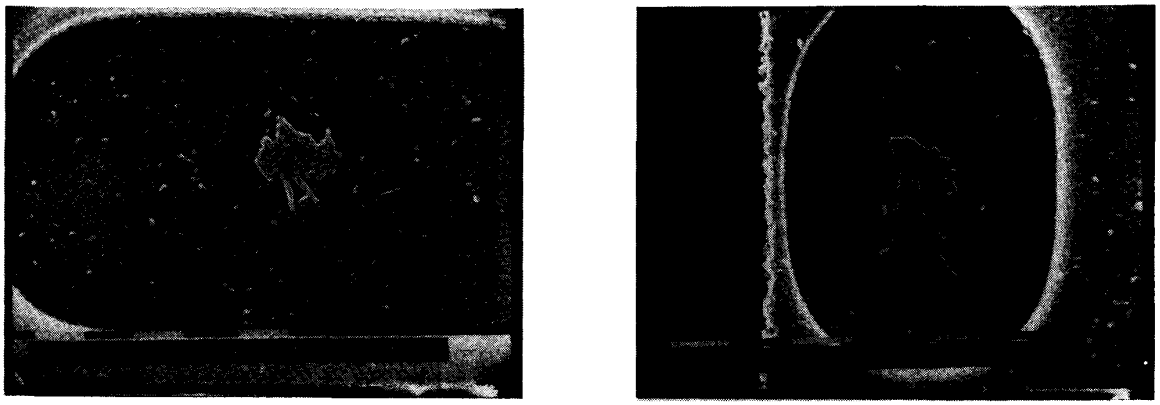



Fig. 14. Threshold voltage versus effective thickness (3500, 2000, and 500 Å) for amorphous silicon devices.

## Appendix
## Experimental Results for Memory Switching in Amorphous Silicon Devices

The results presented in this appendix are for device structures formed using amorphous silicon deposited at 570°C using the LPCVD technique. The structure of the device was the same as shown in [6, Fig. 1], except that the polycrystalline film was replaced with an amorphous film and that the upper implant was not activated because annealing would cause the film to crystallize.

Memory switching characteristics and the electronic properties of the programmed state in these devices resemble those of polysilicon devices. The threshold programming voltage again is approximately proportional to the square root of the thickness of the film, as illustrated in Fig. 14. The figure shows the threshold voltage versus effective thickness (after subtracting the fuse implant depth) of the amorphous silicon film. Since the implant was not activated via an anneal step, only 1000 Å were subtracted from the nominal thickness values. Each threshold voltage indicated in the figure is an average value of twenty devices with varying areas. The error bars are as defined for Fig. 2. Devices with effective amorphous silicon film thicknesses of 3500, 2000, and 500 Å program at approximately 18, 13, and 5 V, respectively; the thinner films require larger currents.



(a) (b)

Fig. 15. SEM micrographs of (a) 5 × 11 and (b) 5 × 3 square micrometer programmed devices after removing the metal and texturing the underlying amorphous silicon.

There is a dramatic difference in the physical appearance of the programming filaments of polycrystalline and amorphous silicon devices. Fig. 15 shows SEM micrographs of two amorphous silicon devices that were programmed and etched to expose the filaments. The filaments are much larger than those that form in polysilicon [6], and they tend to form closer to the center of the device.

We attribute these differences in filament appearance to two factors: they are larger in amorphous silicon because that material is more unstable, and they form nearer the device center because amorphous silicon is more nearly homogeneous in microstructure. As the computer simulation showed, the temperature within a device peaks in the exact center if there are no conductive inhomogeneities.

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