THESIS

FABRICATION AND CHARACTERIZATION OF HIGH-SPEED OXIDE-CONFINED VERTICAL CAVITY SURFACE EMITTING LASERS

Submitted by

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WE HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER OUR SUPERVISION BY AHMAD NASSER AL-OMARI ENTITLED FABRICATION AND CHARACTERIZATION OF HIGH-SPEED OXIDE-CONFINED VERTICAL CAVITY SURFACE EMITTING LASERS BE ACCEPTED AS FULFILLING IN PART REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE.

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ABSTRACT OF THESIS

FABRICATION AND CHARACTERIZATION OF HIGH-SPEED OXIDE-CONFINED VERTICAL CAVITY SURFACE EMITTING LASERS

The necessities for communication-network services such as database queries, remote education, telemedicine and videoconferencing have increased the need for high-speed communication systems with greater bandwidth. Faster single channel systems require faster VCSELs, and thus it is important to develop high-speed VCSELs, since they are suited for LAN application in a number of ways.

High-Speed Oxide-Confined Vertical-Cavity Surface Emitting Lasers were fabricated in this research. Standard and repeatable fabrication steps were developed. Important fabrication steps that enhance the oxide-confined VCSELs modulation frequency were adopted. Photosensitive and non-photosensitive polyimides were investigated. Metal-to-polyimide adhesion was improved. Adhesion strength was examined using scotch tape.

The measured threshold voltage and current of a fabricated VCSEL with 28μm diameter and 7μm oxide-confined aperture were as low as 1.5V and 0.4mA, respectively. The active area resistance at zero bias was found to be 98Ω. Optical modulation frequency of 17.0GHz for a VCSEL with 28μm diameter and 7μm oxide-confined aperture was observed. An equivalent circuit model for high-speed oxide-confined

VCSELs, which is important for designing high-speed interfacing circuits to VCSELs, was obtained.

Ion implanted VCSELs were investigated and simulated using the Trim and Pspice softwares. Ion implantation is expected to reduce the active area capacitance from 135fF to 83fF. As a consequence, the electrical –3dB frequency will increase to 32GHz, which represents about 30% improvement.

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CHAPTER 1

Introduction

1.1 Introduction

The world "LASER" is an acronym for Light Amplification by Stimulated Emission of Radiation. Some of the types of lasers are gas lasers, solid-state lasers, dye lasers and semiconductor lasers. In general, semiconductor lasers are efficient, compact, rugged and inexpensive compared to other types of lasers.

In 1917, Albert Einstein showed that the process of stimulated emission must exist [1], but it was not until 1960 that T. H. Maiman first achieved laser action at optical frequencies in ruby [2]. The basic principles and construction of a laser are fairly straightforward and it is quite surprising that the fabrication of the laser was so long delayed. The development of the laser since 1960 has been extremely rapid, and although applications for lasers had a very slow start during their first decade, new applications for laser radiation are being found almost every day. Lasers are used in many types of engineering, including metrology, scientific research, industrial processing, communication, holography, medicine and for military purposes [3,4].

Over the last decade, the semiconductor laser diode has emerged as a device that complements transistor technology to form the twin columns of modern information technology. Similar to the transistor's role in integrated circuits that process information, the laser is at the heart of fiber-optic networks that form the basis of the modern Internet. There are predominantly two forms of semiconductor lasers, edge emitting lasers (EEL) and vertical cavity surface emitting laser (VCSEL). A Vertical Cavity Surface emitting Laser is a semiconductor laser diode in which the two mirrors as well as the intervening gain region are grown epitaxially on a semiconductor substrate. Light generated at the

gain region bounces back vertically between the mirrors, and some leaks through the top surface mirror to form the emitted beam [11].

Before discussing the difference between the VCSEL and EEL, we want to summarize some work that had an important impact on the development of the VCSEL. Beginning in the early 1980s, several researchers, mainly at Bell Laboratories and The Optical Sciences Center of the University of Arizona, began looking into the use of lasers as a nonlinear optical phenomenon in micro cavities for potential applications in optical switching, signal processing and optical computing [7].

Two-dimensional (2-D) arrays of light modulators were used in some of the system architectures that have been inspected for optical computing. These architectures are known to allow the performance of specific mathematical operations such as the inversion of matrices in a simple and an efficient approach [7]. While researchers were searching for technologies that could be used in these applications, they began investigating simple Fabry–Perot resonators that include nonlinear optical media. David Miller and his group at Bell Laboratories studied resonators with GaAs–(Al,Ga)As multiple quantum wells as the nonlinear absorber [7]. The structures they investigated had a low threshold; because of this, they subsequently became the basis of the quantum-confined Stark-effect optical modulator. Dr. D. J. Goodwill and his group were able to fabricate modulators into large-size arrays and use them in switching applications [12]. These researchers implemented an optical hyper plane-based ATM switching fabric. They also designed the electronic interface and optical interconnects which are currently being fabricated using today's technology.

The performance of these devices as optical switches was improved by increasing the quality factor of the composite resonator structures by reducing the residual cavity losses and by increasing the reflectivity of the mirrors. Independent of any attempt to develop a laser, these improvements were essential for some of the main features of the practical VCSEL.

1.2 Vertical Cavity Surface Emitting Laser (VCSEL) vs. Edge Emitting Laser (EEL).

VCSEL, or Vertical Cavity Surface Emitting Laser, is a semiconductor micro laser diode that emits a cylindrical beam light vertically from the surface of a fabricated wafer. This special characteristic enables it to offer significant advantages over edge-emitting lasers (EEL). Figure 1.1 below illustrates some of the advantages of VCSELs over EELs. In the EEL, the beam comes out of the edge while in the VCSEL the beam comes out of the wafer surface, which makes it possible to carry out on wafer testing before the wafer is cut into individual laser dies that are then packaged. It is also noted that the EEL produces an astigmatic diverging beam of an elliptical cross-section, whereas the beam at the VCSEL has a much smaller divergence angle and circular beam cross-section, which results in simpler optics and better performance [5].

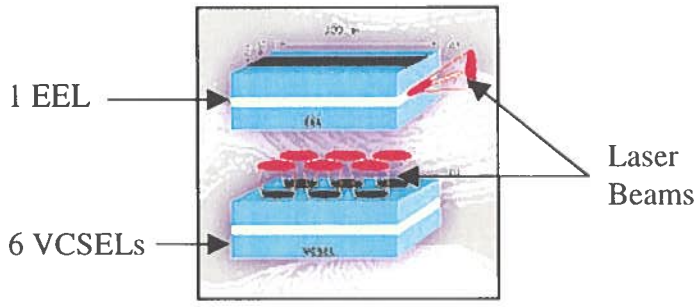


Figure 1.1 Vertical Cavity Surface Emitting Laser vs. Edge Emitting Laser [5]

In addition, VCSELs do not need corrective optics and over 50% of their light can be coupled into a fiber. VCSELs have lower current requirements than EELs, which makes them good for battery-driven applications and improves power budget efficiencies for low power applications. For high power applications, EELs are more efficient. VCSELs also have higher data rates (>10.0 GHz) than the simplest type of EELs, known as Fabry-Perot laser diodes (~2.0GHz). Other EELs, specifically distributed feedback (DFB) lasers, can operate at speeds of 20 GHz or higher, but are much more expensive than VCSELs. The large bandwidth of VCSELs makes them attractive for low cost, high-speed communications applications. Moreover, VCSELs can easily be fabricated into high-density 2-D arrays, while this is much more complicated using EELs. Easier fiber alignment and reduced packaging costs are additional advantages of the VCSEL [6].

1.3 Motivation

Communication has been one of the principal needs of people since ancient times. As a result, an interest in devising a communication system for sending messages from one distant place to another has increased. As time passes, several communications systems have emerged. The main inspiration behind each innovative system was either to improve transmission reliability, to increase data rate so that more information could be sent, or to increase the transmission distance between stations.

In the years that followed the invention of the telegraph by Samuel F. Morse in 1838, larger portions of the electromagnetic spectrum were utilized for transmitting information from one point to another.

There are two types of communications systems: electrical communication and optical communication. In electrical communication, the data are transferred by

superimposing information onto a sinusoidally varying electromagnetic wave, which is known as the carrier. As for optical communication, the information is in an optical format, which is carried by varying the intensity of the optical power through optical fiber.

Telecommunication networks based on optical fiber communication have become a major information transmission system all over the world. Local Area Networks (LAN) as a part of the telecommunication networks have become the norm for many workplaces and educational settings, as users move from an isolated desktop computing model to a more distributed computing model in which they gain access to shared and unlimited sources of information, and as the demand on communication-network services such as database queries, remote education, telemedicine and videoconferencing increase the need for high-speed communication systems with greater bandwidth.

There are three approaches to greater link bandwidth: parallel ribbons, wave division multiplexing and faster single channel systems. Faster single channel systems require faster VCSELs, and thus it is important to develop high-speed VCSELs. VCSELs are suited for LAN applications in a number of ways [8,9]. Because the optical beam is emitted perpendicular to the wafer surface, VCSEL arrays can be fabricated with photolithographic tolerances, making them ideal sources to mate with ribbon fiber interconnects. To date, most of the market has centered on either four elements operating up to 3.125GBd per channel or twelve elements operating up to 1.25GBd per channel. The operating reach of a parallel interconnect is more than 100 meters, and is limited by the skew in the optical fiber. In other systems, serial data communication is more advantageous, and VCSELs have been operated at speeds in excess of 10GBd by direct

modulation. Achievable link lengths are on the order of 75 meters over installed multimode optical fiber, with distances of 500 meters on 850nm optimized fiber such as Lucent's Lazer Speed™ [10].

The general purpose of this research is to fabricate 850nm High-Speed Vertical Cavity Surface Emitting Lasers, to understand their speed limitations, and to optimize them, which will result in reducing the number of elements used per channel in parallel data communication systems or increasing the overall speed of the system if the same number of elements is used.

1.4 Overview

The overall objective of the research presented in this thesis is to fabricate High-Speed Oxide-Confined Vertical Cavity Surface Emitting Lasers. To ahieve this objective, the parameters that affect VCSEL speed as well as the fabrication steps required to fabricate high-speed VCSELs were investigated. Included was the examination of the characteristics of two different types of polyimide. One critical characteristic, the adhesion strength between metals and polyimides, was investigated and improved. A standard procedure for obtaining the electrical model of the VCSEL out of the measured microwave reflection coefficient, S_{11} was also developed.

Chapter 2 details the background information about the physics and fabrication of VCSELs. It includes the present technical status of High-Speed VCSELs by highlighting the intrinsic and extrinsic parameters that affect VCSEL switching speed. It also reviews previously published work in fabrication and characterization of High-Speed VCSELs.

Chapter 3 discusses the detailed fabrication steps of High Speed VCSELs . It incorporates an overview of VCSEL fabrication steps, including the reasoning involving each step. It further includes a description of the actual fabrication steps and their setup, illustrated by images and schematic.

Chapter 4 presents the testing and characterization results of fabricated High-Speed VCSELs. It describes the measurements of electrical and optical characteristics of these VCSELs. Both the DC characterization and AC characterization setups are described and presented as a schematic diagram. Parameters such as threshold current and modulation bandwidth are presented and discussed for a range of device sizes.

Chapter 5 describes the electrical model for the VCSEL. A fitting procedure for obtaining the electrical model is described. Simulation results for Pspice software are shown. A comparison between the measured results given in Chapter 4 and the simulation results is presented.

Conclusions and suggestions for future work are given in Chapter 6. The detailed operational manual for devices used and fabrication processes are contained in Appendices A and Appendix B, respectively. Appendix C describes the typical CSU cleanroom photolithography processes. The HD-8000 polyimide data sheet and the HD-8000 polyimide inspection processes are described in Appendix D and Appendix E, respectively.

References:

[1] J. Wilson, J. F. B. Hawkes, " OPTOELECTRONICS An Introduction," 1983.

[2] T. H. Maiman, " Stimulated optical radiation in ruby masers," Nature ,London, 187, 1960, p. 493.

[3] M. Ross, " Laser Applications Vol. 1," Academic Press, New York, 1972.

[4] J. F. Ready, " Industrial Applications of Lasers," Academic Press, New York, 1978.

[5] http://www.nas.nasa.gov/.

[6] http://www.honeywell.com/.

[7] Elias Towe, Robert F. Leheny, and Andrew Yang, "A Historical Perspective of the Development of the Vertical-Cavity Surface-Emitting Laser" IEEE, Vol. 6, November/December 2000.

[8] J. A. Tatum, et al., "VCSELs Enable High Speed Data Communications," Lightwave, March, 2000.

[9] J. A. Tatum, "VCSEL Packaging for Transceiver Design," Fiber Optic Product News, 2000.

[10] Jim Tatum, "VCSELs in the information age," published in SPIE Optics in Information Systems Newsletter, April 2001.

[11] Paul L. Gourly, Kevin L. Lear, Richard P, " Advanced Technology Surface Emitting Lasers" IEEE SPECTRUM, Vol. 31, No. 8, August 1994.

[12] D. J. Goodwill, K. E. Davenport, and H. S. Hinton, "An ATM-based intelligent optical backplane using CMOS-SEED smart pixel and freespace optical interconnect modules," IEEE J. Select. Topics Quantum Electron., Vol. 2, pp. 85–96, 1996.

[13] Kent D. Choquette and Hong Q. Hou, "Vertical-cavity surface emitting lasers: Moving from research to manufacturing," Proc. IEEE 85, 1730 (1997).

[14] http://research.sun.com/.

CHAPTER 2

Background and Present Technical Status of High–Speed Vertical Cavity Surface Emitting Lasers

Modern high-speed short wavelength communication systems use the Vertical Cavity Surface Emitting Laser as their light source. Great progress has been achieved in the development of VCSELs for high-speed optical interconnects in high bit-rate data transmission systems [1]–[11].

2.1 VCSEL structure

In the 1970s, the Iga group at the Tokyo Institute of Technology, Tokyo, Japan, presented the first proposed idea for a Vertical Cavity Surface Emitting Laser. They achieve pulsed operation and continuous wave (CW) operation in 1984 and 1988 respectively [17]. State-of-the-art fabrication has developed throughout the years as more advances were achieved in the design and growth of mirrors, in addition to the progress accomplished in fabrication techniques for electrical and optical confinement. Various companies are presently manufacturing VCSELs.

Numerous means are used in VCSEL fabrication to achieve optical and current confinement. The four common ones are: proton implantation, oxidation, post etching and re-growth. Figure 2.1 below illustrates a cross-section for these four fabrication methods where most of the alterations focus on the method of defining the injected current path. All four structures will be discussed in more detail in the next section.

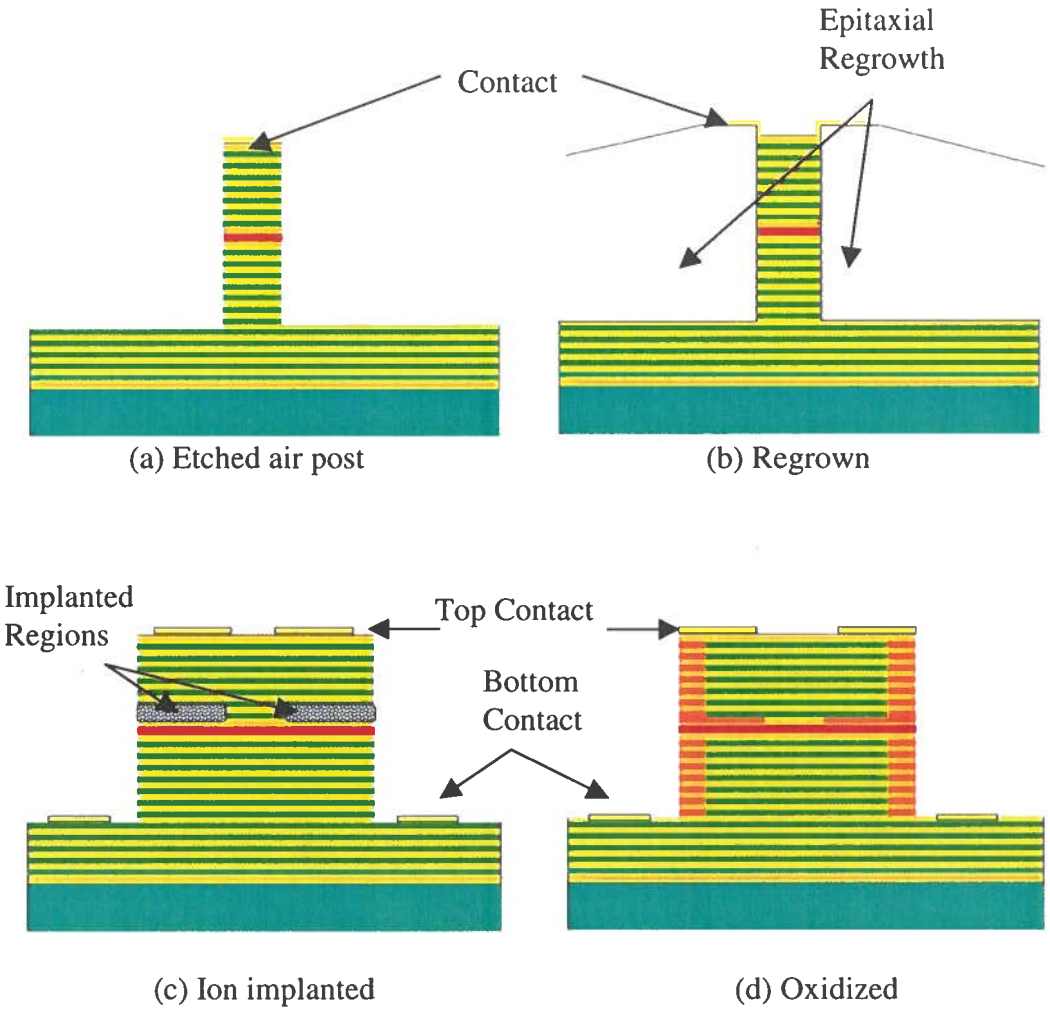


Figure 2.1 Various VCSEL structures (reproduced after [29])

2.2 Post etched, Regrown, Proton Implanted and Oxidized VCSEL structures

An air-post structure is a simple approach to defining the lateral extent of a VCSEL cavity. It is done by etching a pillar or post, as shown in Figure 2.1. The first illustration of a monolithic VCSEL was achieved with an etched air-post structure by the Jewell group at AT&T Bell Laboratories [18].

The disadvantage of the air-post VCSEL structure is carrier loss due to surface recombination at the sidewalls. Furthermore, there is a limit of how small the air post

diameter can be due to optical loss. Also, defects in the sidewalls will result in diffraction and scattering [19]. An additional concern is that these types of structure do not have an effective heat sink, which results in high thermal impedance. Moreover, in air-post VCSELs, the top contact overlaps at least part if not all of the active area, so the structure is not well suited to short wavelength VCSELs operating at wavelengths where the substrate is absorbing since top emission will be required.

The regrown structure is a method which gives index guiding in a planar geometry using a buried heterostructure, as shown in Figure 2.1. Etching the materials around the intended cavity isolates the active region. After that, the etched regions are filled with materials that have higher bandgap energies. Because of their wider bandgaps and lower refractive indices [17], the regrown regions are used to define the lateral margins of the active region and to play a part in electrical as well as optical confinement.

To date, three regrowth methods have been successfully demonstrated. These are: vacuum-integrated dry etching and molecular beam epitaxy (MBE) [30]; dry etching followed by chemical pretreatments before metalorganic vapor phase epitaxy (MOVPE) [31]; and etching followed by liquid phase epitaxy (LPE) utilizing melt-back cleaning [32].

To form implanted VCSELs, ion implantation is used to damage a certain part of the top mirror material and make it insulating, with the undamaged center acting as a conduit for the current. As a result, the current will flow from the top contact and channel through the undamaged region, which is the central region of the Distributed Brag Reflector (DBR), and into the underlying active region [13]. Figure 2.3 below represents a schematic cross-section of the ion implanted VCSEL.

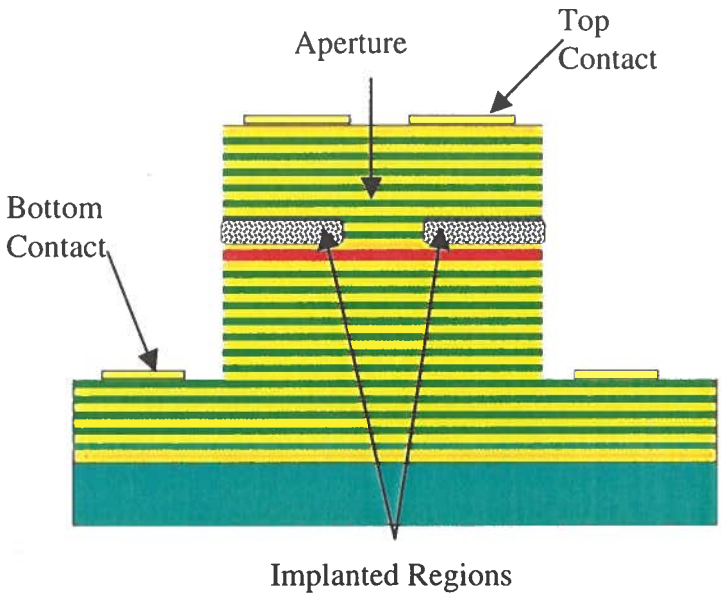


Figure 2.3 Schematic of an ion implanted VCSEL

Although the proton implantation structure is preferred by industry as a well-known, manufacturable process, which yields a desirable structure and better thermal dissipation [13], nonetheless this type of VCSEL structure has disadvantages. Using proton implantation structure, it is possible that the active layer will be will damaged by the implanted ions. Also, the lateral scattering of ion species (straggle) is indistinct, which limits the precision with which small apertures can be defined [17]. Another drawback of proton implantation is that it does not provide inherent index-guiding. Moreover, the implanted geometry does not provide inherent polarization discrimination or control [21]. Furthermore, the presence of some residual surface damage from the implanted protons increases the contact resistance over the implanted material. Simulation of the ion implantation process using the Stopping and Range of

Ions in Matter software (SRIM), which was written by James F. Ziegler, will be presented in Chapter 5 [33].

Oxide-Confined VCSELs involve the introduction of an oxide aperture close to the active region. This is achieved by growing layers with the highest Aluminum (Al) mole fraction adjacent to the active region. Etching the mesa will expose the edges of these layers, and then they will be oxidized at high temperatures in a water-steam environment using an oxidation furnace [14]. Details of the oxidation process will be discussed in Chapter 3. As a consequence, the layers with the highest Al mole fraction are converted from $Al_xGa_{1-x}As$ into Al-oxide, which is an insulator with a low refractive index (n~1.55) [13]. As illustrated in Figure 2.4 below, this insulating layer above the active region acts to confine the current to be injected into the preferred active area. Since this layer has a low refractive index, it also provides index-guiding.

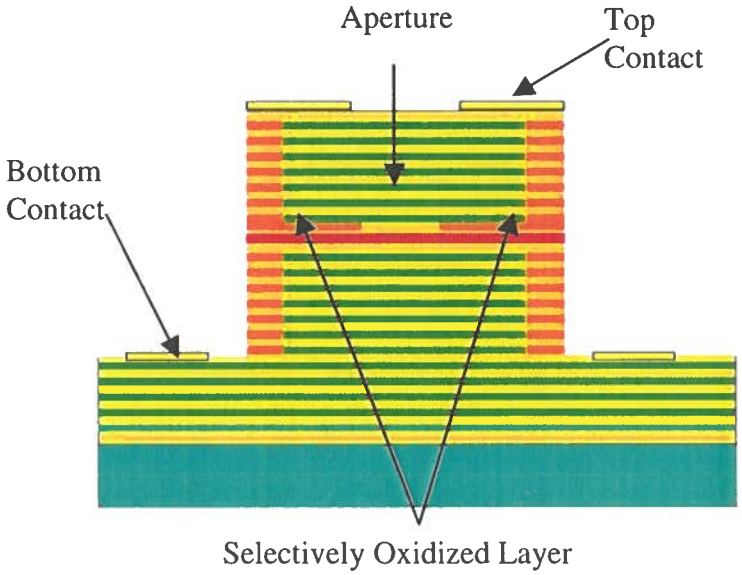
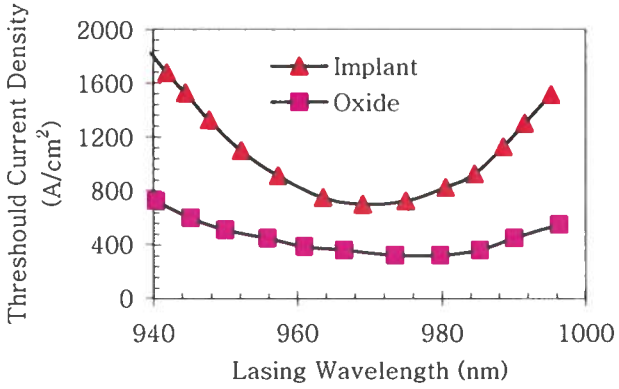
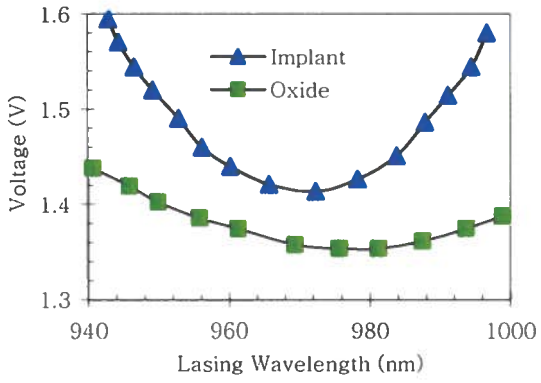


Figure 2.4 Schematic of an oxide-confined VCSEL

A comparison between the proton implanted and oxidized VCSEL structures (shown in Figures 2.3 and 2.4) indicates that the oxidized VCSEL provides excellent performance in terms of lower threshold current density and voltage, as illustrated in Figure 2.5 [17]. It is clear from the plots that the oxidized VCSEL structure has lower threshold current density (J_{th}) and lower threshold voltage (V_{th}) than that of the proton implanted VCSEL. Furthermore, while the best proton implanted VCSELs provide about 20% power conversion efficiencies, oxidized VCSELs with efficiencies up to 50% have been reported by Dr. K. L. Lear and his group [15].



(a)



(b)

Figure 2.5: (a) Threshold current vs Lasing wavelength, (b) Threshold voltage vs Lasing wavelength (reproduced after [29])

Most of the recent reports on the progress of VCSEL device operation have mainly been for oxide-confined VCSELs designs, which provide low threshold current and high power efficiency as a result of their good optical beam and current confinement. In these various designs, the aperture has a different refractive index than the oxide isolation layer and thus acts as an index guide, as well as providing the current confinement for current injection into the active region. This serves to create laser emission with greater modal coherence and low-lasing threshold [12].

2.3 Factors affecting VCSEL speed

As the bit rates of high-speed data transmission increase, the dynamic properties of the VCSELs are becoming more significant. Enhancing the VCSELs' speed to multi-gigabit ranges will extend its potential applications into future high-speed data transmission systems, parallel supercomputer interfaces, and multi-channel optical computing systems. For all these potential applications, it would be highly desirable to make the high speed VCSELs [16].

Three main aspects must be considered when discussing high speed VCSELs. These factors are the relaxation oscillation, optical nonlinearities, and parasitic circuit effects that include junction and pad capacitance, and DBR series resistance [16]. Using an electrically pumped VCSEL, a very high relaxation oscillation frequency was measured. When the injected current was maximized, a 71GHz relaxation oscillation was observed [22]. This is the highest ever-reported frequency for this type of measurement. Also, optical nonlinear gain limits the bandwidth of VCSELs. Low nonlinear gain allows a high resonance frequency up to the intrinsic bandwidth [16]. The third parameter is

circuit parasitics, which can limit VCSEL speed. Large parasitic circuit elements cause the bandwidth to saturate before achieving the maximum modulation frequency.

These parasitic circuit elements are mainly due to the resistance of the p- DBR or n-DBR mirrors, and also due to the extrinsic capacitance. If these parasitic components are quite high, they will set the modulation properties of the VCSEL. To fabricate high speed VCSELs, these parasitic values should be reduced. Figure 2.6 below illustrates a cross- section of high speed VCSEL with a superimposed equivalent circuit [23]. Parasitic elements, such as pad capacitance (C_p), mirror resistance (R_s) and oxide and junction capacitance (C_a), are shown.

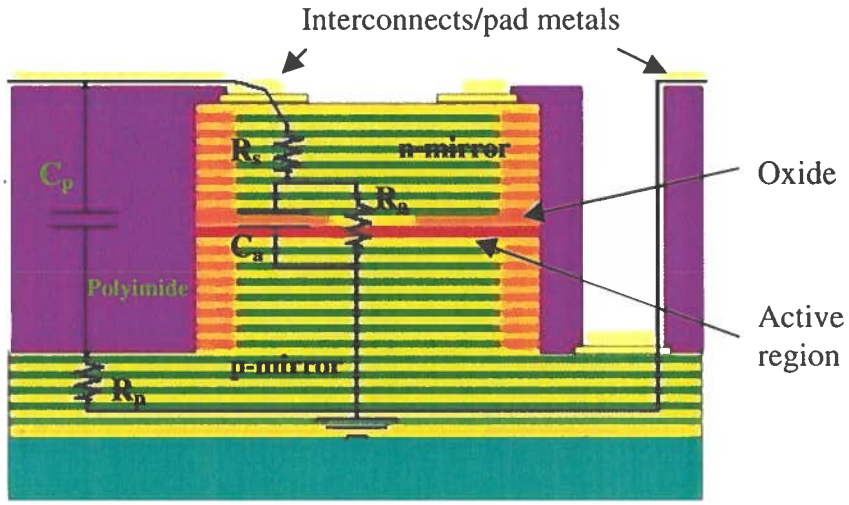


Figure 2.6 A cross section of high speed VCSEL with superimposed equivalent circuit (reproduced after [23])

2.4 Review of previous work in high-speed VCSEL fabrication

As mentioned in the previous section, since VCSEL speed is often determined by circuit parasitics, many research groups have tried different ways of reducing these parasitics.

Resistance can be reduced to some extent by using some means such as delta doping, which Dr. Kojima and his group did in 1993 [24], changing the VCSEL structure itself, as Dr. M. K. Hibbs's and Dr. R. A. Morgan's group did in 1994 [25,26], or by using the metalorganic vapor phase epitaxy (MOVPE) method, which was illustrated by Dr. K. L. Lear and his group in 1994 [27]. Using the delta doping in VCSEL mirrors, it was reported that the differential resistance was reduced almost by half and the peak output power was increased by 40%. MOVPE was used to implement a new mirror scheme. Mirrors with low vertical resistance can be achieved by grading mirror interface and decreasing alloy composition. As a result, low lateral resistance, high reflectivity and high thermal conductivity were obtained [27]. To date, much work has been done to achieve the low resistance.

On the other hand, parasitic capacitances in oxide-confined VCSELs are pad [16,23] and oxide capacitance [23]. To reduce pad capacitance, three parameters can be changed: pad area [16], dielectric material and the dielectric material thickness. Equation 2.1 illustrates the relationship between these three parameters. Clearly reducing the pad area, increasing the thickness of the dielectric material, or using a dielectric material that has a low dielectric constant will decrease the pad capacitance, and thus increase the 3dB frequency response of the VCSEL.

$$C_{pad} = \frac{\varepsilon_o \varepsilon_r A}{d} \qquad (2.1)$$

where:

ε_o: Permitivity of free space

ε_r: Dielectric constant

A: Pad area

d: Dielectric material thickness.

As reported in [16], the PSPICE program was used to simulate the VCSEL equivalent circuit using different pad areas. As a result, reducing the pad area by one fourth ($25x25\mu m^2$) of its normal area, which is ($50x50\mu m^2$) [28], improved the VCSEL dynamic response to more than 7.9 GHz (at 3 dB). Two VCSELs with pad areas ($20x20\mu m^2$) and ($50x50\mu m^2$) were also fabricated. Results show that the VCSEL with the smaller pad area ($20x20\mu m^2$) has a higher 3dB modulation frequency than that with ($50x50\mu m^2$) pad area. Figure 2.7 below illustrates the small signal modulation response characteristics for the VCSELs of the pad areas $20x20\mu m^2$ and $50x50\mu m^2$. Curves for different values of bias currents are shown.

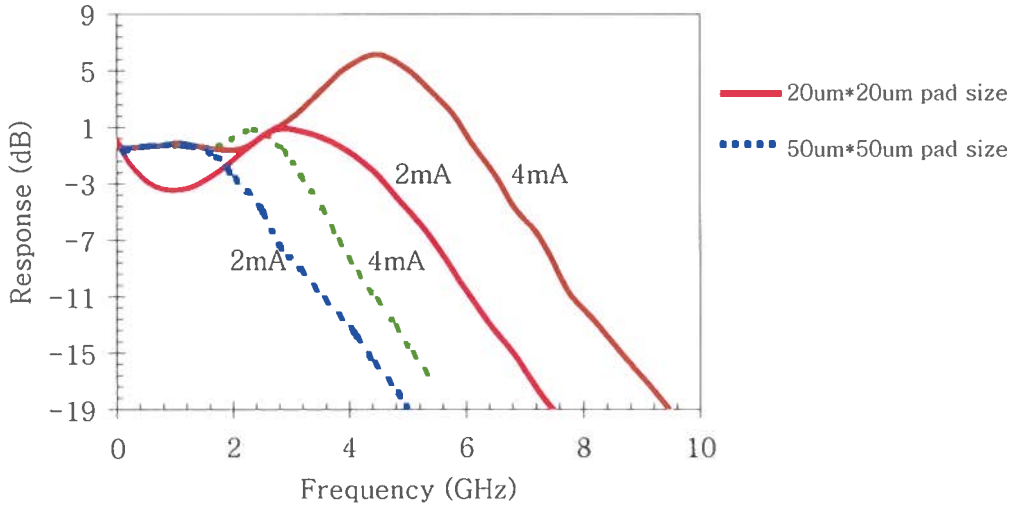


Figure 2.7 Small signal modulation response characteristics, measured at different values of bias currents above threshold (reproduced after [16])

Changing the dielectric material used to planarize the VCSEL, as well as increasing its thickness, will increase the modulation frequency. In other words, a low dielectric constant material, as well as keeping the thickness of this material at maximum, will result in lower pad capacitance.

Reducing the oxide capacitance will also result in increasing the modulation response of the VCSEL. Several values of the VCSELs' modulation frequencies were reported by different research groups, but the fastest-ever realized VCSEL of 850 nm was demonstrated by the Sandia National Laboratories group [23]. The modulation frequency for this device was reported to be in excess of 20GHz at room temperature. To achieve this, the group reduced the oxide capacitance by using an ion implantation process, as shown in Figure 2.8 below. The ion implantation process and ion implantation simulation software will be discussed in detail in Chapter 5.

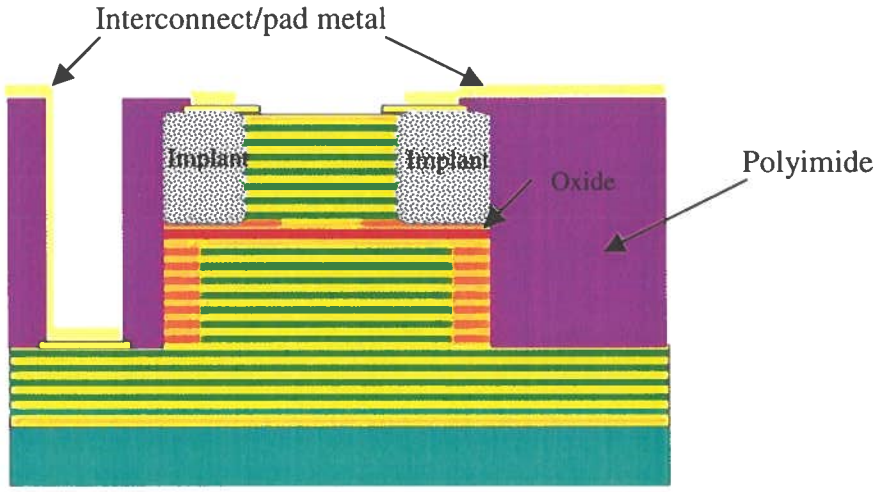


Figure 2.8 Implanted VCSEL cross- section (reproduced after [23])

As mentioned earlier, since the intrinsic VCSEL limit reaches as far as 70GHz, thermal issues inside the VCSEL limit the frequency response [23]. Consequently, in

principle reducing the VCSEL heat will increase its bandwidth. To prove this, in 1997 Dr. K. L. Lear and his group at Sandia National Laboratories decreased the testing-stage temperature down to –50°C, and as a result the current range prior to self-heating induced bandwidth saturation was extended. Dr. Lear and his group were able to achieve VCSEL modulating frequency up to 26GHz [23].

References:

[1] K. L. Lear, A. Mai, K. D. Choquette, S. P. Kilcoyne, R. P. Schneider, Jr, and K. M. Geib, "High-frequency modulation of oxide-confined vertical cavity surface emitting lasers," Electron. Lett., Vol. 32, p. 457, 1996.

[2] D. L. Huffaker, D. G. Deppe, K. Kumar, and T. J. Rogers, "Native-oxide defined ring contact for lowthreshold vertical-cavity lasers," Appl. Phys. Lett., Vol. 65, p. 97, 1994.

[3] D. Weidermann, R. King, C. Fung, R. Jager, R. Michalzik, P. Schnitzer, M. Kicherer, and K. J. Ebeling, "Design and analysis of single-mode oxidized VCSELs for high-speed optical interconnects," IEEE J. Select. Topics Quantum Electron., Vol. 5, pp. 503–511, May/June 1999.

[4] B. Weigl, M. Grabherr, C. Jung, R. Jager, G. R. Aeiner, R. Michalzek, D. Sowada, and K. J. Ebeling, "High-performance oxide-confined GaAs VCSELs," IEEE J. Select. Topics Quantum Electron., Vol. 4, pp. 409–415, Apr. 1997.

[5] K. D. Choquette, K. M. Geib, B. Roberds, H. Q. Hou, R. E. Twestea, and B. E. Hammons, "Short wavelength bottom-emitting vertical cavity lasers fabricated using wafer bonding," Electron. Lett., Vol. 34, p. 1404, 1998.

[6] K. D. Choquette, R. P. Schneider, K. L. Lear, and K. M. Geib, "Low threshold voltage vertical-cavity lasers fabricated by selective oxidation," Electron. Lett., Vol. 30, p. 2043, Nov. 1999.

[7] B. J. Thibeault, K. Bertilsson, E. R. Hegblom, E. Strzelecka, P. D. Floyd,A. Naone, and L. A. Coldren, "High-speed characteristics of low-optical loss oxide-apertured vertical-cavity lasers," IEEE Photon. Technol. Lett., Vol. 9, pp. 11–13, Jan. 1997.

[8] L. A. Coldren, H. Temkin, and C.W. Wilmsen, Introduction to VCSELs in Vertical Cavity Surface Emitting Lasers, Cambridge, U.K.: Cambridge Univ. Press, 1999.

[9] A. V. Krishnamoorthy, L. M. F. Chirovsky, W. S. Hobson, R. E. Leibenguth, S. P. Hui, G. J. Zydzik, K. W. Goosen, J. D. Wynn, B. T. Tseng, J. Lopata, J. A. Walker, J. E. Cunningham, and L. A. D'Asaro, "Vertical-cavity surface-emitting lasers flip-chip bonded to gigabit-per-second CMOS circuits," IEEE Photon. Technol. Lett., Vol.11, pp. 128–130, Jan. 1999.

[10] K. L. Lear, V. M. Hietala, H. Q. Hou, M. Ochai, U. J. Banas, B. E. Hammons, J. C. Zolper, and S. P. Kilcoyne, "Advances in Vertical Cavity Surface Emitting Lasers," Washington, DC: Opt. Soc. Amer., 1997, Vol. 15, p. 69.

[11] D. V. Kulsenkov, H. Temkin, and S. Swirhum, "Polarization instability and relative intensity noise in vertical-cavity surface-emitting lasers," Appl. Phys. Lett., Vol. 67, p. 2141, 1995.

[12] G. Dang , W. S. Hobson, L. M. F. Chirovsky, J. Lopata, M. Tayahi, S. N. G. Chu, F. Ren, and S. J. Pearton, "High-Speed Modulation of 850-nm Intracavity Contacted Shallow Implant-Apertured Vertical-Cavity Surface-Emitting Lasers," IEEE Photonics Technology letters, VOL. 13, NO. 9, SEPTEMBER 2001.

[13] A. Miller, M. Ebrahmzadeh, D. M. Finlayson, "Semiconductor Quantum Optoelectronics" Proceedings of the Fiftieth Scottish University Summer School in Physics, June 1998.

[14] K. M. Geib, K. D. Choquette, et al., "Fabrication issues of oxide-confined VCSELs," SPIE, Vol. 3003, 1997, pp. 69-74.

[15] K.L. Lear, K. D. Choquette, et al., " Selectively oxidized vertical cavity surface emitting lasers with 50% power conversion efficiency," Electron. Lett. Vol. 31, pp. 208-209 , 1995.

[16] Achyut Kumar Dutta, Hideo Kosaka, Kaori Kurihara, Yoshimasa Sugimoto, and Kenichi Kasahara, "High-Speed VCSEL of Modulation Bandwidth over 7.0 GHz and Its Application to 100 m PCF Datalink, " Journal of Lightwave Technology, Vol. 16, No. 5, MAY 1998.

[17] Weng W. Chow, Kent D. Choquette, Mary H. Crawford, Kevin L. Lear, and G. Ronald Hadley, "Design, Fabrication, and Performance of Infrared and Visible Vertical-Cavity Surface-Emitting Lasers, " IEEE Journal of Quantum Electronics, Vol. 33, No. 10, Oct. 1997.

[18] J. L. Jewell, A. Sherer, S. L. McCall, Y. H. Lee, S. Walker, J.P. Harbison, and L. T. Florez, "Low-threshold electrically pumped vertical-cavity surface-emitting microlasers," Electron. Lett., Vol. 25, pp. 1123–1124, 1989.

[19] Y. H. Lee, J. L. Jewell, B. Tell, K. F. Brown-Goebeler, A. Sherer, J. P. Harbison, and L. T. Florez, "Effects of etch depth and ion implantation on surface emitting microlasers," Electron. Lett., Vol. 26, pp. 225–227, 1990.

[20] G. Hasnain, K. Tai, L. Yang, Y. H. Wang, R. J. Fischer, J. D. Wynn, B.Weir, N. K. Dutta, and A. Y. Cho, "Performance of gain-guided surface emitting lasers with semiconductor distributed Bragg reflectors," IEEEJ. Quantum Electron., Vol. 27, pp. 1377–1385, 1991.

[21] D. Vakhshoori, J. D. Wynn, G. J. Aydzik, R. E. Leibenguth, M. T. Asom, K. Kojima, and R. A. Morgan, "Top-surface emitting lasers with 1.9 V threshold voltage and

the effect of spatial hole burning on their transverse mode operation and efficiencies," Appl. Phys. Lett., Vol. 62, pp. 1448–1450, 1993.

[22] D. Tauber, G. Wang, etc, "70 GHz Relaxation Oscillation in Vertical Cavity Surface Emitting Laser," IEEE Transactions on Electronic Devices., Vol. 39, N. 11,November 1992.

[23] Lear, K.L.; Hietala, V.M.; Hou, H.Q.; Banas, J.; Hammons, B.E.; Zolper, J.; Kilcoyne, "Small and large signal modulation of 850 nm oxide-confined verticai-cavity surface-emitting lasers," Lasers and Electro-Optics, 1997. CLEO '97. Summaries of Papers Presented at the Conference on , Volume: 11, pp.: 193 –194.

[24] Kojima, K.; Morgan, R.A.; Mullaly, T.; Guth, G.D.; Focht, M.W.; Leibenguth, R.E.; "Reduction of p-doped mirror electrical resistance of GaAs/AlGaAsvertical-cavity surface-emitting lasers by delta doping, " Electronics Letters , Volume: 29, Issue: 20, 30 Sept. 1993 pp.: 1771 –1772.

[25] R. A. Morgan, M. Hibbs-Brenner, J. Lehman, E. Kalweit, R. Walterson, T. Marta, and T. Akinwande, "Novel hybrid-DBR single mode controlled GaAs top-emitting VCSEL with record low voltage," in Proc. 7th Ann. Mtg. LEOS'94, 1994, Extended Abstract PD1.6.

[26] M. K. Hibbs-Brenner, R. A. Morgan, J. A. Lehman, R. A. Walterson, E. Kalweit, S. Bounnak, T. Marta, and T. Akinwande, "Record performance of planner, implanted GaAs/AlGaAs top-emitting vertical cavity surface emitting lasers (VCSEL's) grown by MOVPE," in Proc. 7^{th} Ann. Mtg. LEOS'94, 1994, Extended Abstract PD1.5.

[27] K. L. Lear, R. P. Schneider, Jr., K. D. Choquette, S. P. Kilcoyne, J. J. Figiel, and J. C. Zolper, "Vertical cavity surface emitting lasers with 21% efficiency by metalorganic

vapor phase epitaxy," in Proc. 14th Int. Semiconductor Laser Conf., 1994, Extended Abstract W1.5, pp.181–182.

[28] H. Kosaka and K. Kasahara, "VCSELs: Requirements and performance improvements for optical interconnects," in Proc. 7th Ann. Mtg. LEOS'94, 1994, Extended Abstract SL5.1, Vol. 1, pp. 259–260.

[29] A. Miller, M. Ebrahimzadeh, D. M. Finlayson, "Semiconductor Quantum Optoelectronics," 1999.

[30] M. Hong, D. Vakhshoori, L. H. Grober, J. P. Mannaerts, M. T. Asom, J. D. Wynn, F. A. Thiel, and R. S. Freund, "Buried heterostructure laser diodes fabricated by *in situ* processing," J. Vac. Sci. Technol. B, Vol. 12, pp. 1258–1261, 1994.

[31] C. J. Chang-Hasnain, Y. A. Wu, G. S. Li, G. Hasnain, K. D. Choquette, C. Caneau, and L. T. Florez, "Low threshold buried heterostructure vertical cavity surface emitting laser," Appl. Phys. Lett., Vol. 63, pp.1307–1309, 1993.

[32] S. Kinoshita and K. Iga, "Circular buried heterostructure (CBH) GaAlAs/GaAs surface emitting lasers," IEEE J. Quantum Electron., Vol. 23, pp. 882–888, 1987.

[33] http://www.srim.org/.

CHAPTER 3

Fabrication of High-Speed Vertical Cavity Surface Emitting Laser

3.1 Overview of oxide confined VCSEL fabrication process

Oxide confined vertical cavity surface emitting lasers are VCSELs with an oxide aperture formed by wet oxidation of $Al_xGa_{1-x}As$ to form Aluminum oxide Al_2O_3 where x is close to 1.

Fabricating VCSELs requires a number of processing steps carried out in the proper sequence. VCSELs designed for high-speed operation require additional processing steps designed to reduce parasitic capacitance that would otherwise limit their speed. This chapter discusses in detail the steps used in producing high speed VCSELs. Initially, in Section 3.2, the overall process will be summarized, and then subsequent sections will detail steps used for mesa etching, oxidation, contact formation, planarization, and finally interconnect metal deposition.

3.2 Overall process for oxide confined VCSEL fabrication

3.2.1 Epitaxial growth

Epitaxy is a process whereby the required types and compositions of semiconductor alloys are grown on top of each other in a certain order with a certain thickness on a compound semiconductor substrate [1]. In this case, the compound semiconductor substrate is GaAs. Epitaxial growth requires that the grown material and the substrate material have the same crystal structure. The lattice constants (space between 2 atoms) of the grown material and the substrate material should be as close as possible, and the difference between them, called the lattice mismatch, should be in the range of a few percent. There are three commonly used compound semiconductor growth techniques.

These are Metal Organic Chemical Vapor Epitaxy (MOCVD) [2], Liquid Phase Epitaxy (LPE), and Molecular Beam Epitaxy (MBE) [3].

The wafer with epitaxial material used for the devices fabricated as part of this thesis research were supplied by Mission Research Corporation, which purchased them from Emcore. Figure 3.1 represents the structure of the grown wafer that was used in this process. The compositions of the layers were chosen to emit at 850 nm [4]. As shown in Figure 3.1, the substrate is *p-type*. Consequently we will end with an *n*-side up VCSEL that offers a compatible electrical polarity with the npn bipolar-junction transistors used in driving circuits for VCSEL [5].

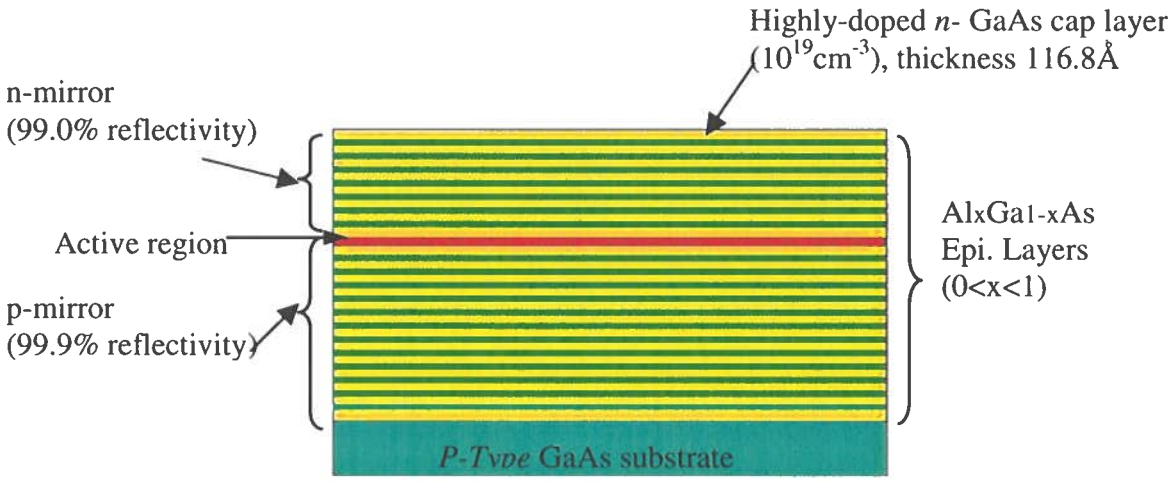


Figure 3.1 Epi. layers grown on a p-type GaAs substrate

The active region contains five GaAs (80Å)/$Al_{0.2}Ga_{0.8}As$ (80Å) quantum wells with indices of refraction of 3.64 and 3.42, respectively. Bragg reflectors can be made using $Al_xGa_{1-x}As$ superlattices. Layers of different composition x have different refractive indices. Several repetitions of a double layer of low and high Al content can lead to a constructive interference of incompletely reflected waves. For certain wavelengths that

depend on the refractive indices and thicknesses of the layers, a very high reflectivity can be achieved. Such structures are used as reflectors in our laser structures [6]. The n-mirrors have 20 periods of $Al_{0.92}Ga_{0.08}As$ (701.1Å)/$Al_{0.16}Ga_{0.84}$ As (605.4Å) n- DBRs with refraction indices of 3.03 and 3.51. The p-mirrors have 35 periods of $Al_{0.92}Ga_{0.08}As$ (701.1Å)/$Al_{0.16}Ga_{0.84}$ As (605.4Å) p- DBRs with corresponding refractive indices of 3.03 and 3.51. One layer that has the highest composition, x=0.98, ($Al_{0.98}Ga_{0.02}As$), is buried inside the n-DBRs with a thickness of 707.7Å and a 700Å barrier from the quantum wells. Some wafers may have two layers of $Al_xGa_{1-x}As$ with high aluminum composition grown above and below the quantum wells with a 700Å barrier. The cap layer is an n-GaAs layer with a 116.8Å thickness and a doping concentration of $(1-2)\times10^{19}\,cm^{-3}$. The reason why this top layer is highly-doped will be discussed later in this chapter. The doping of both n-DBRs and p-DBRs are in the range of $(1-2)\times10^{18}\,cm^{-3}$. After epitaxial growth the wafer is characterized by Polaron capacitance-voltage measurements to determine the doping level and by reflectivity measurements to determine layer thickness [5]. The wafer is now ready to proceed into the next step for VCSEL fabrication, which is mesa etching.

3.2.2 Mesa etching

Mesa etching for vertically stacked layers has to be done in such a way as to electrically isolate a working VCSEL to restrict undesirable leakage currents, make contact to underlying layers, and expose the $Al_xGa_{1-x}As$ layer with high Al composition for subsequent oxidation. It is important to expose the high Al composition layer to water vapor since our VCSELs are oxide-confined VCSELs, which means that water

vapor is necessary as an oxygen source to oxidize the high Al composition layer to form the required aperture [7]. Further explanation of wet oxidation will be discussed later in this chapter.

To etch a mesa, the sample has to go first through the Photolithography step. To carry out the Photolithography step, the sample has to be cleaned using certain chemicals in a specific sequence. Photolithography proceeds by exposing photoresist to an ultraviolet light passed through a photomask on top of the sample. The photomask consists of glass or quartz with the wanted pattern defined on them in a thin film material such as chromium. First the photoresist is applied and spun onto the sample. Then the photomask is aligned to any existing features on the sample, although no alignment is necessary for the first photolithography step used to define the mesas. After this the photoresist which is on top of the sample and the photomask are brought into contact, and finally the mercury lamp which is the source of the ultra violetlight is turned on for a certain time [3], as shown in Figure 3.2

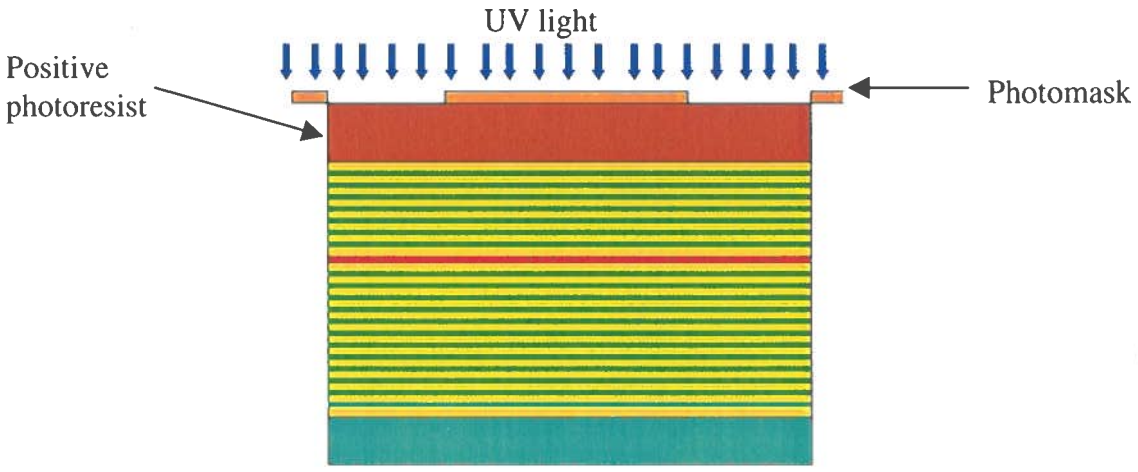
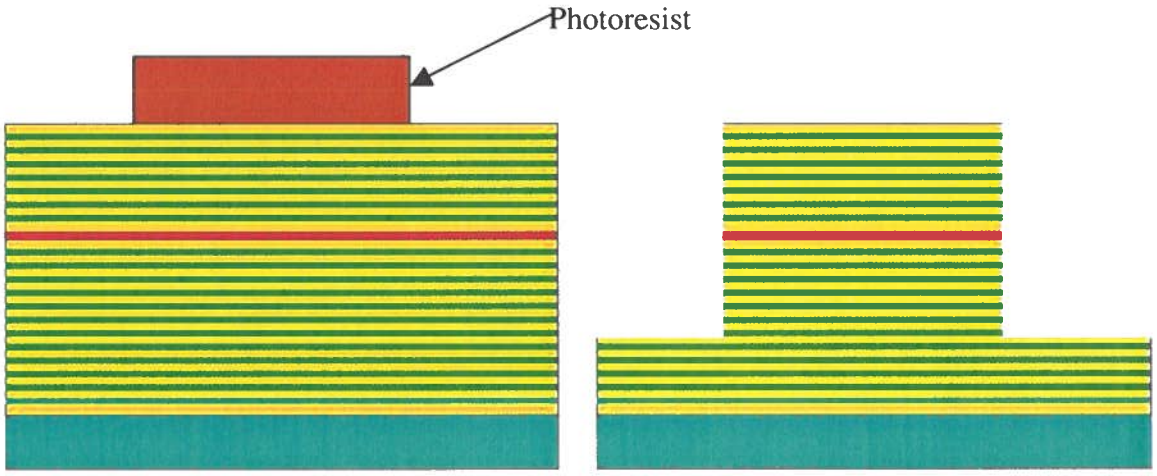


Figure 3.2 Sample during UV exposure

After this the photomask is removed and the sample is dipped into the developer for a certain period of time and then rinsed with DI water. A detailed discussion of the Photolithography process will be presented later in this chapter. After developing, the sample will appear as shown in Figure 3.3.a below. Since the photoresist has a positive tone, the exposed photoresist was removed while the unexposed photoresist remained [3].

The sample was etched using the chemical-assisted ion beam (CAIBE) [3], for which further information will be provided later in this chapter. After etching, the photoresist was stripped using a technique, which I will discuss later in more detail. The sample cross-section at this point is shown in Figure 3.3.b.



(a) (b)

Figure 3.3 (a) Photoresist mask after developing, (b) Mesa after etching and striping the photoresist

After stripping the photoresist, the sample is now ready to proceed to the next step, which is wet oxidation.

3.2.3 Wet oxidation

Due to its advantages in forming the current aperture and providing a lateral index guiding to the lasing mode [8], wet oxidation is used to fabricate high-speed VCSELs. The high Al composition layer, which we discussed in the epitaxial growth and the mesa etching sections, has a higher oxidation rate than the rest of the mirror stacks under the same conditions [7], [10]. Wet oxidation is carried out by exposing the sample to a high temperature (~450°C) steam environment [7]. The equipment, setup and schematic diagram of the oxidation furnace will be discussed later in detail in Section 3.3. Figure 3.3 shown below represents the mesa after oxidation. Note that the layer with the highest Al percent oxidized further than the other layers.

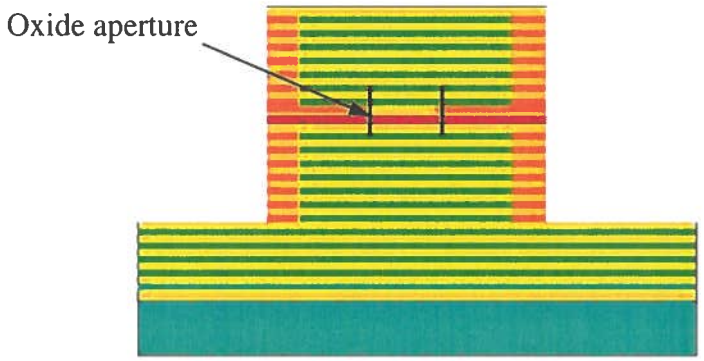
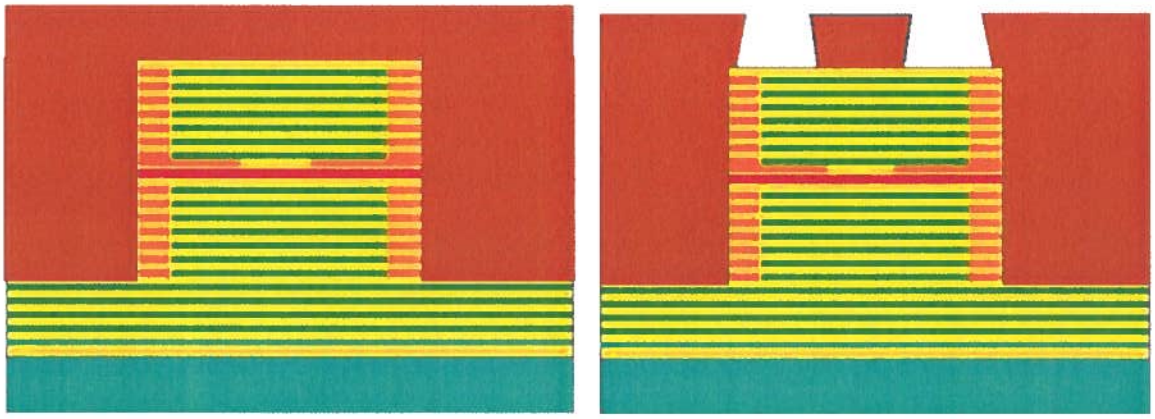


Figure 3.3 Mesa after oxidation. AlGaAs layers converted to Al-oxide are shown in orange

After the oxidation step, our mesa now has an oxide aperture with a certain diameter, depending on many variables in the oxidation process [7].

3.2.4 Ohmic contacts (top contacts/bottom contacts)

The term "ohmic contact" is used to describe a metal-semiconductor contact that follows Ohm's law. An ohmic contact should have a low contact resistance compared to the bulk resistance of the semiconductor [13]. Top contacts on the mesas are used to pass the current into or out of the VCSELs. Top contacts are applied by evaporating the required types of metals onto the sample after the sample passes through the photolithography process, as shown in Figure 3.5.



(a) (b)

Figure 3.5 (a) Mesa covered with photoresist, (b) Mesa after developing

As shown in Figure 3.5.b, it is important to get an overhanging photoresist profile by the edges since this will result in an easy, clean metal lift-off step. After checking the profile using the microscope, the sample is ready to proceed to the next step, which is loading the sample into the evaporator.

After loading the sample into the evaporator, the pressure needs to be pumped down to a low level. The required combination of metals can then be evaporated by melting each metal in sequence using an electron-beam. After unloading the sample its

entire surface will be covered with the evaporated metals and it will look like Figure 3.6.a shown below.

Lift-off is a simple, uncomplicated method for patterning metal films that are deposited. Lift-off processing can be done with acetone, whereby the photoresist will be stripped away, removing with it all the unwanted metals that lie on top of the photoresist surface, while the metals in the photoresist openings adhere directly to the substrate and remain [3] as shown in Figure 3.6. The sample is now ready to proceed to the bottom contact process.

For bottom contacts, the sample will go through the same process as for the top contact except that the types of metals that need to be evaporated as well as the photomask will be different. Figure 3.6.d shows the mesa with both top and bottom contacts.

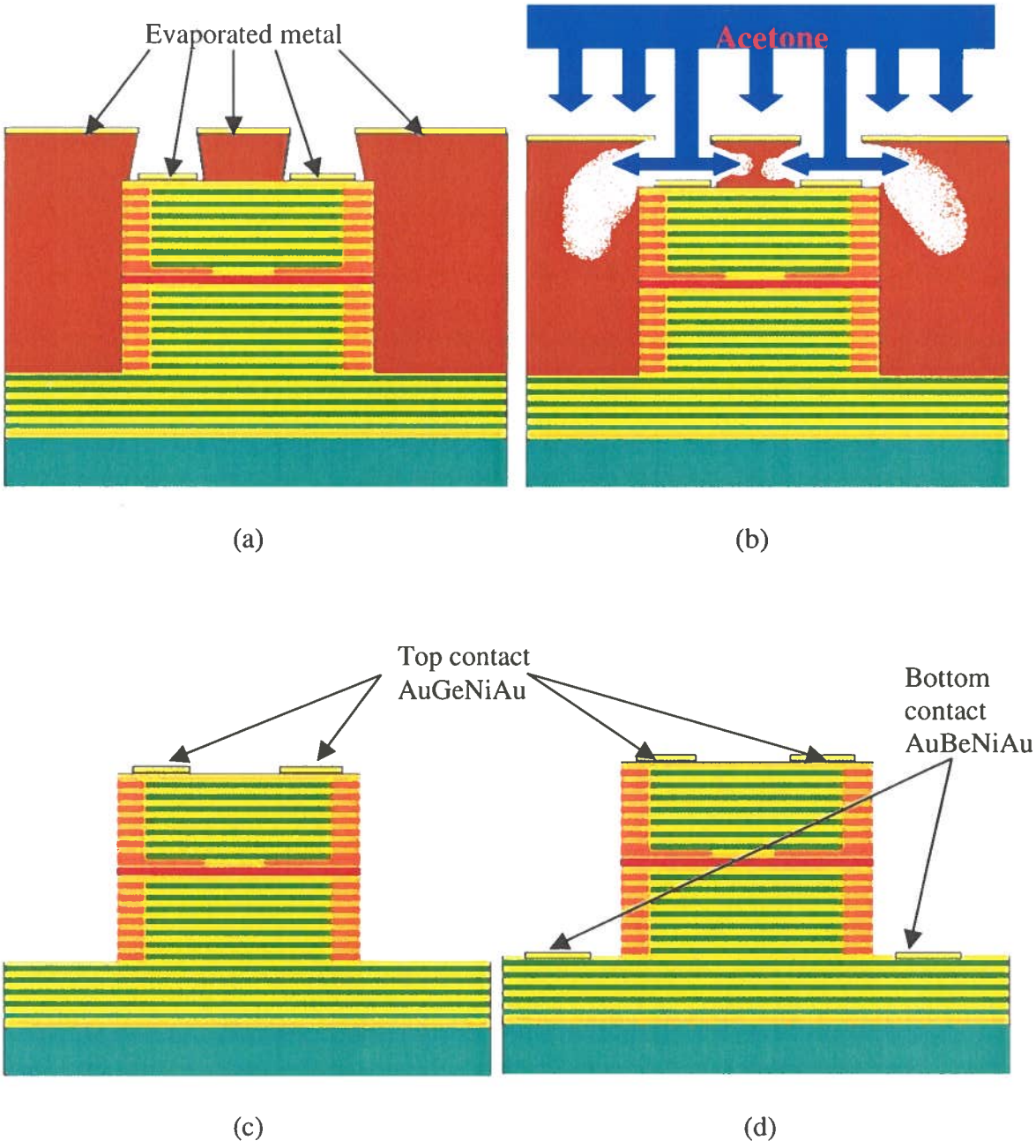


Figure 3.6 (a) Mesa after metal evaporation, (b) Mesa during lift-off process, (c) Mesa after lift-off, (d) Mesa with top and bottom contacts

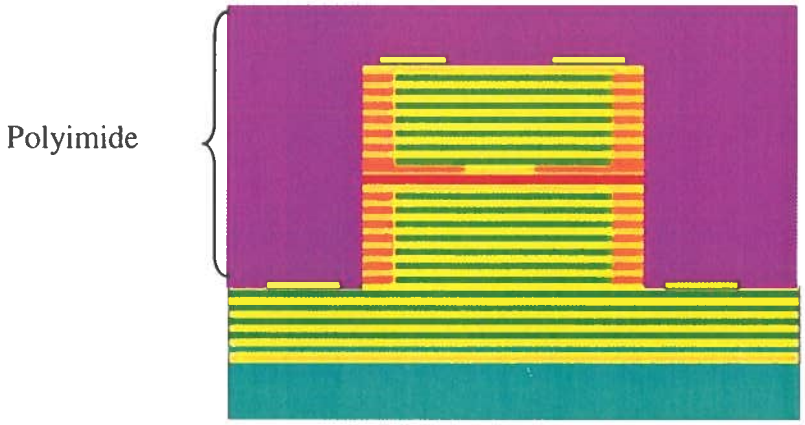
After contact-metal evaporation and lift-off, the sample will go through the high temperature-alloying step. The sample temperature is increased until the contact metals alloy onto the surface of the semiconductor. For the contacts on top of the mesa, the

metals are alloyed into the thin GaAs cap layer, shown in Figure 3.1. The sample is now ready for planarization using polyimide.

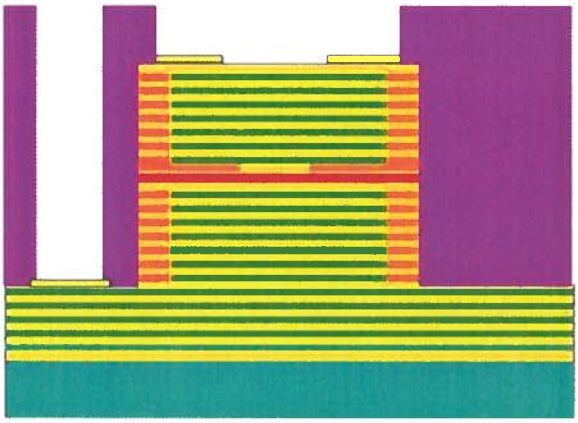
3.2.5 Planarization

The surface of the mesa must be planarized for several reasons. A smooth surface is needed for metal interconnects and metal bonding pads to be patterned and deposited. Planarization material also protects the sidewalls of the mesa from the external environment, and it creates an isolation layer between the n and p contacts. Planarization is accomplished using a photo-definable polyimide.

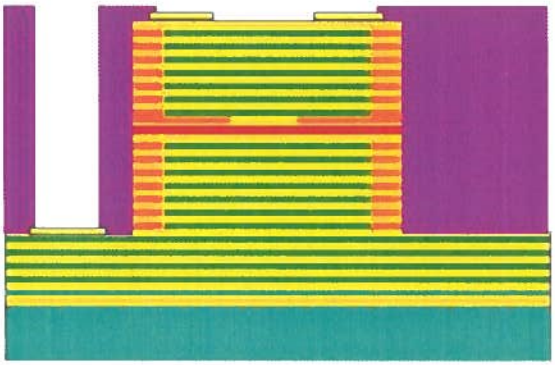
The polyimide is applied to the sample. It then has to go through a lithography process similar to the lithography process for the photoresist described earlier in this chapter. After developing, the polyimide has to be cured. A more detailed discussion of curing polyimide will be presented later in this chapter. Figure 3.7 shown on the next page illustrates the three main steps in mesa planarization.



(a) Polyimide all over the mesa



(b) Polyimide after developing



(c) Polyimide after curing

Figure 3.7 Different stages of mesa planarization

3.2.6 Metal interconnects/pad metal

In order to test the sample, we now need metal interconnects so that we can place the probe station tips on metal pads to electrically contact the VCSEL. The sample needs to go through the photolithography process to pattern the lift-off photoresist for the metal pads. After the required interconnect and pad metals are evaporated, the sample is unloaded from the evaporator and goes through the lift-off process mentioned earlier. Figure 3.8 below diagrams the sample after interconnect and pad metal lift-off. At this point, the VCSEL fabrication is complete and the sample is ready to be tested. However, preliminary testing can occur earlier in the middle of the process after the oxidation step, although electrically contacting the device is more difficult.

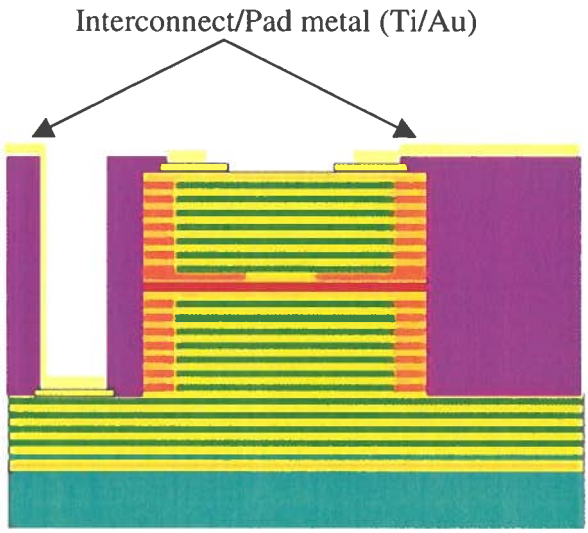


Figure 3.8 Sample after lift-off

3.2.7 Testing

A simple DC testing setup is shown in Figure 3.9. This setup is used to measure both the I-V curve and L-I curve of the VCSEL. Parameters such as the threshold current can be measured. Other useful measurements can be carried out by changing the probe position. Detailed information will be provided in Chapter 4.

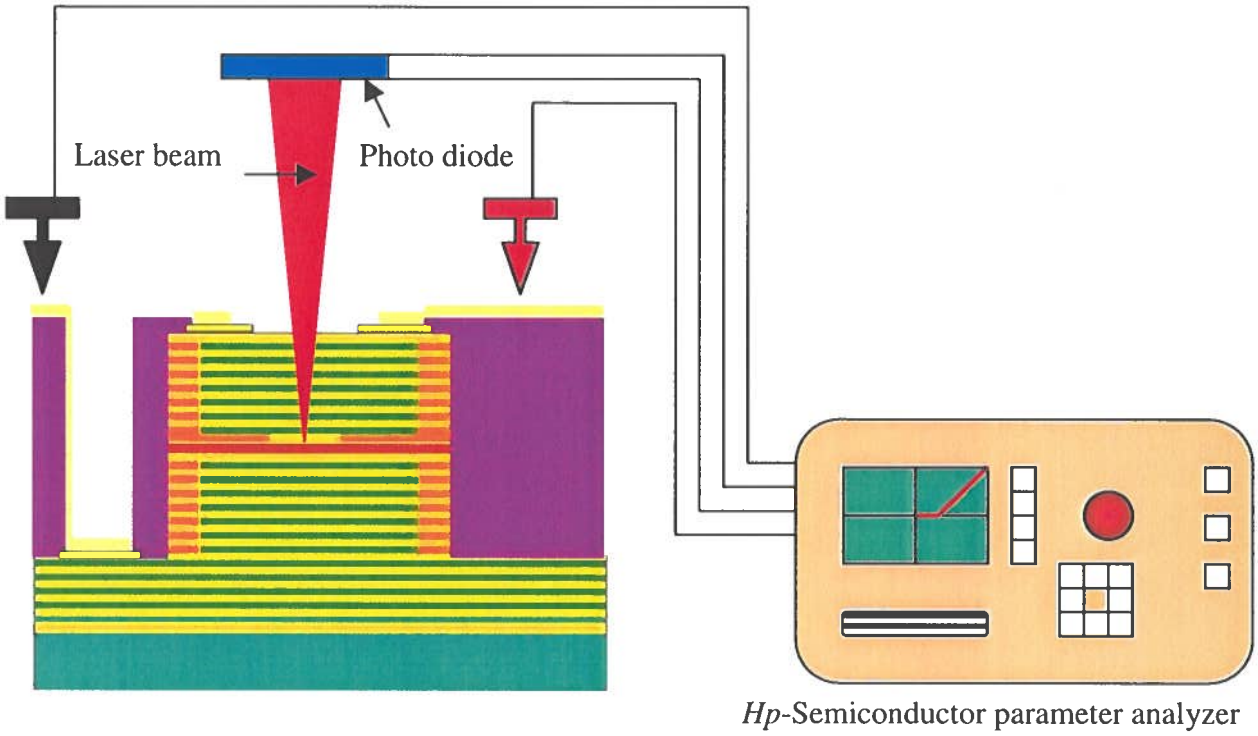


Figure 3.9 DC testing setup

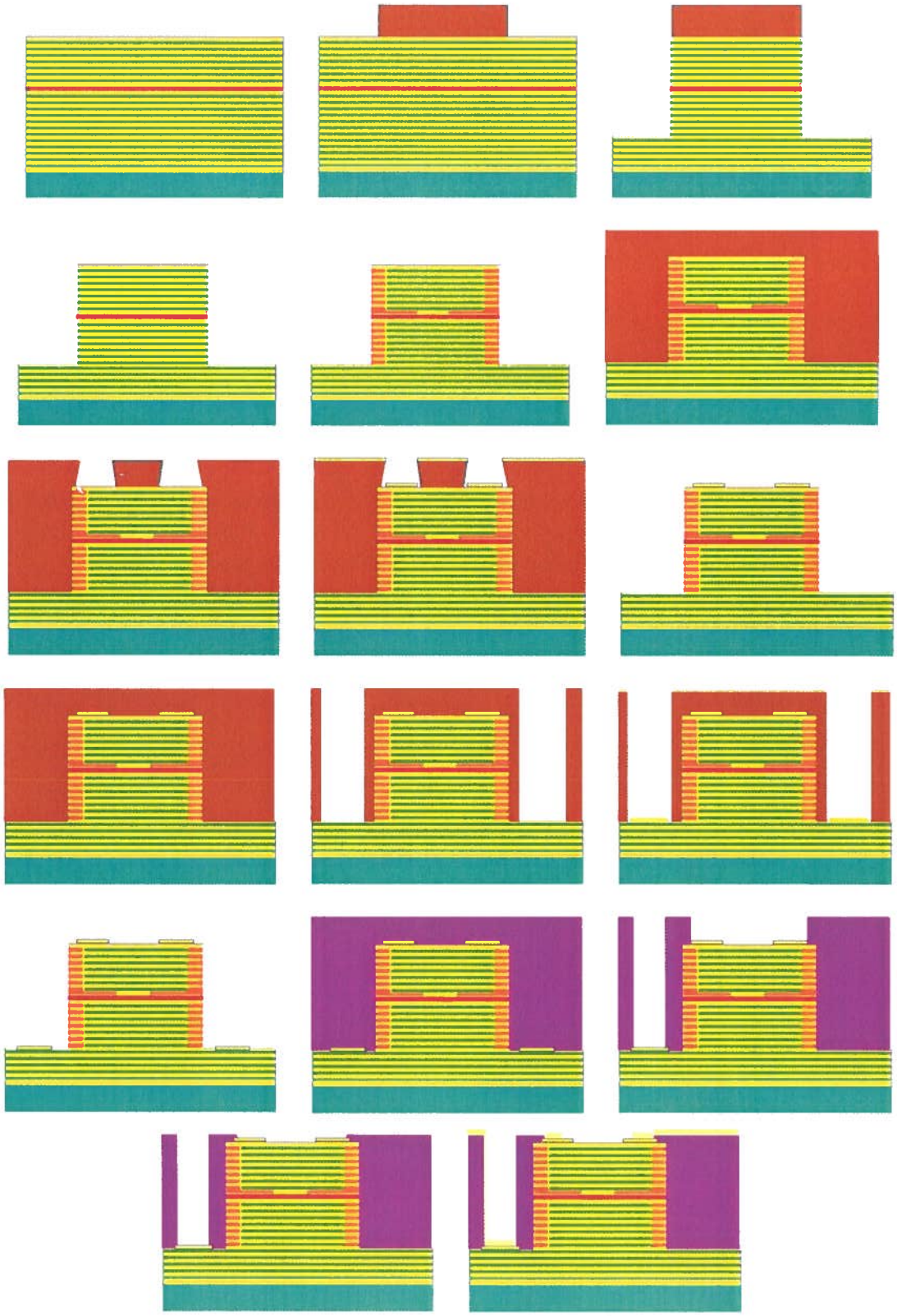


Figure 3.10 Image gallery for VCSEL fabrication steps (left to right)

3.3 VCSEL fabrication

3.3.1 Mesa etching

Wet etching, which refer to the use of liquid etchants to remove materials, was investigated for fabricating VCSEL mesas. The H_3PO_4:H_2O_2(30%): H_2O system with 20:2:2 volume ratios, respectively, was mixed and examined. Seven GaAs samples were patterned with the mesa photomask, and each of them was dipped into the etchant mixture for varying periods of time . All of the etching system components were stored at room temperature (20°C) and the mixture was left to stabilize for about five minutes. Figure 3.11 illustrates the etch depth for each of the samples. The linear fit corresponds to an etching rate of GaAs, which is ~1μm/min.

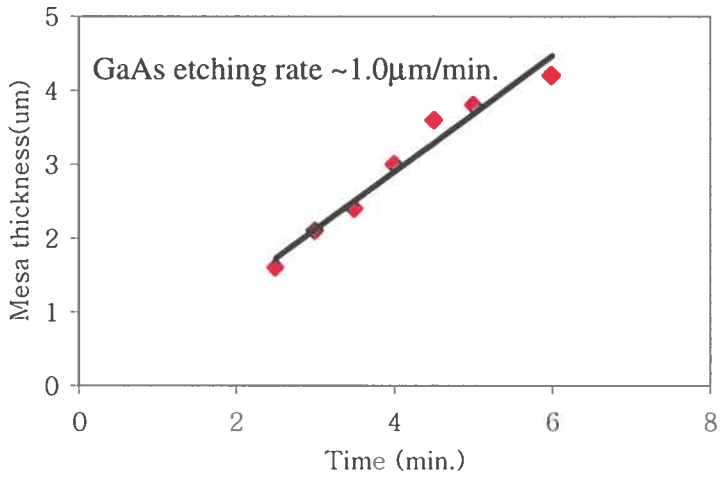


Figure 3.11 Mesa thickness vs. etching time

The SEM picture shown in Figure 3.12 on the next page illustrates the mesa sidewall profile. The sample was immersed in the etchant system for five minutes and then rinsed with DI water. It is clear from the image that this wet etchant results in an isotropic etching profile. Because of the associated undercutting of the photoresist mask,

we end up with a smaller semiconductor mesa top surface area than that of the original photoresist mask. This caused a problem in subsequent fabrication steps because the mask was designed assuming that the mesa top area would be the same as the photomask. To achieve this, a non-isotropic, vertical wall profile of the type obtained using dry reactive ion etching was used.

Ending with a smaller mesa surface area will result in the top contact metal falling onto the sidewalls of the mesa. If the metal contacts the sidewall below the p-n junction, it will produce a parallel schottky barrier diode with a turn-on voltage of about 0.7V. This schottky barrier will prevent the VCSEL from reaching its 1.45V threshold voltage, and consequently the VCSEL will never lase.

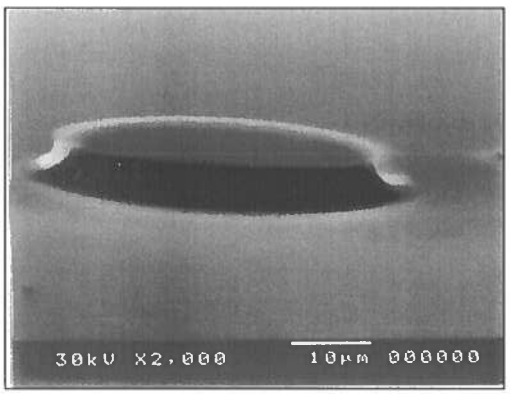


Figure 3.12 SEM image for wet etched mesa

Dry etching has several advantages over wet etching. It offers considerable directionality and etches more rapidly in the vertical direction than the horizontal direction. Some cases can result in a lateral etch rate close to zero, and hence undercutting of masked patterns can be significantly reduced. Moreover, dry etching is capable of patterning smaller geometric features (on the order of one micron) than wet

etching. Furthermore, contamination can be less and purity can be higher, since gas usage in dry etching is generally less than fluid use in wet etching. Also, dry etching provides steeper sidewalls that will result in a larger mesa surface area [3, 10].

Dry etching of the VCSEL mesa was investigated. Six samples of the real wafer were prepared by patterning the mesa photomask on them. The same photoresist preparation used for the wet etching investigation was used for dry etching, with the addition of one more step: hard-baking the photoresist after developing it for two minutes at 120°C to make the photoresist hard enough to withstand ion bombardment during dry etching.

A chemically-assisted ion beam (CAIBE) system was used for the dry etching. It is located at the CSU Foothills Campus in the Engineering Research Center (ERC) in Dr. Carmen Menoni's lab. For more detailed information about the etching system used, refer to [24]. 10 sccm of Argon gas and 2.5 sccm of Chlorine gas were used. The samples were etched by Dr. Dinesh Patel. Two samples were processed each day, and the other samples waited until the later day in order to ensure that the system cools down.

Consideration of the etch rates for the two samples etched on the same day illustrates the etch rate variation due to etch system heating. Figure 3.13 shown below illustrates two etch depth vs. etch time curves, one for the first sample that was loaded in the etching system that day and the other one for the sample that was loaded directly after the first sample. In other words, the system was hot when loading the second sample. During a three-day period, six different samples were examined. A new sample was used for each load. It is concluded from Figure 3.13 that the etching rate was not constant in each case but was more stable for the second sample than that for the first sample. We

therefore decided that for our real sample to run the system first with a dummy sample, and then load our real sample as a second sample to be etched during a given day.

The reason why the etching rate was not constant is that dry etching usually utilizes one or more halogens (especially F, Cl, or Br) or oxygen. These excited species can trap electrons from the plasma to form stable negative ions. Such a reaction reduces the conductivity of the plasma by replacing a highly mobile carrier (electron) with a heavier or less mobile ion. This situation can sometimes alter the behavior of the discharge, causes instabilities, and lead to nonuniform etching [25].

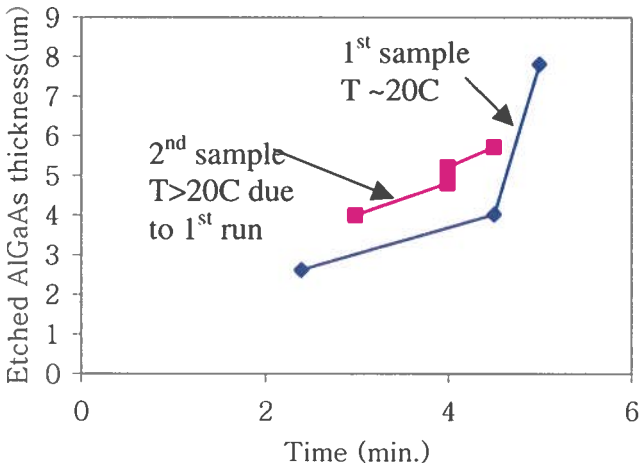


Figure 3.13 AlGaAs etching depth vs. time

Etching, like most process steps, is not applied uniformly across the sample being processed. Photomasks are used in most steps to pattern the photoresist in order to determine where the etching process will occur. Photolithography begins with cleaning operations that are performed before each major step during device processing. Solvents are used to remove any contaminants present on the wafer. The standard solvents used in my process are acetone, methanol, and de-ionized (DI) water applied in sequence by rinsing the surface of the sample with a stream from a squirt bottle.

After cleaning with solvents, the sample is blown-dry with nitrogen to remove any residual fluid from the sample surface. The sample is then baked at 95C to remove any moisture from the surface, since the photoresist properties depend on the amount of moisture in it. Liquid photoresist (Shipley 1818) is then applied by using a syringe loaded with photoresist and an attached filter. The photoresist is deposited in a puddle on the sample, which has been previously positioned on a spinner. Immediately after the photoresist is put on the sample, the sample is spun at approximately 6000 rpm for 30 seconds to evenly distribute the photoresist across the sample and to make the photoresist adhere to the sample after the spinning stops [3]. The thickness of the photoresist after spinning is a function of photoresist viscosity and spin speed, but usually ranges from about 1 μm to 10 μm. The thickness of the photoresist can be tested by scratching away part of the photoresist (optionally prepared on a dummy sample) and using a surface profilometer, e.g., Alpha Step model 100, to measure its thickness. Our measured photoresist thickness for Shipley 1818 spun at 6000 rpm was 2.0μm, as shown in Figure 3.15 below.

After photoresist application, the photoresist on the edges of the sample needs to be removed. Usually the photoresist is uniformly distributed across the sample except the edges, which will have a thicker layer of the spun photoresist, as shown in Figure 3.14. This build-up of resist at the edge of the sample is referred to as an "edge-bead". If the edge-bead is not removed, it will make a gap between the glass photomask and the photoresist surface in the middle of the sample during UV exposure. The gap between the photomask and photoresist will allow diffraction of UV light into parts of the photoresist that should not be exposed. As a result, the exposure resolution is reduced

and small features, such as small diameter mesas, will be lost in the developing step. Also, the edge bead will interfere with the movement of the photomask when it is in proximity to the photoresist, making it difficult to align the sample with the mask in the aligning step. The edge-bead can be removed either by using a cotton swab soaked with acetone or by using a blade.

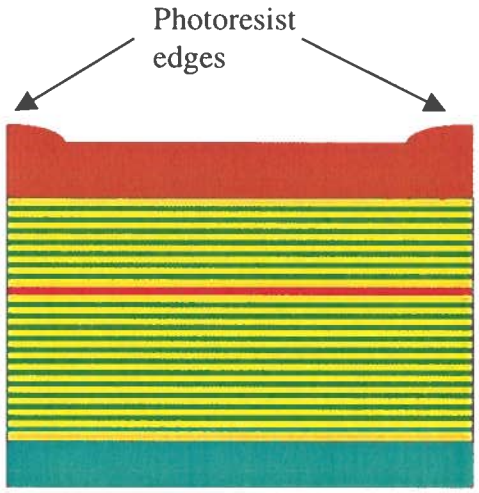
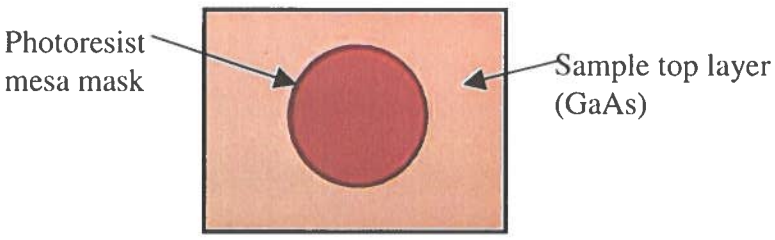


Figure 3.14 Sample with photoresist

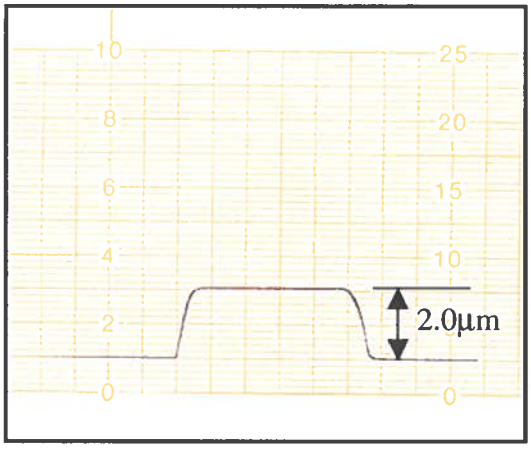
After edge-bead removal, the sample is placed on the mask aligner chuck, and the mesa mask is loaded and aligned with the sample. Once aligned, the sample and the mask are placed in contact. Finally, the mask aligner lamp is switched on for a duration determined by the exposure time, which is set as specified in the vendor data sheet. For more information about how to operate the Karl Suss mask aligner, refer to the standard clean room operation manual in Appendix A.

Next, the sample is developed for 50 seconds using AZ400K. The developing time is determined when all the exposed photoresist is developed away. The sample is then rinsed with DI water and blown-dry with nitrogen. Diagram 3.15 below shows a top

view of a mesa photoresist mask after developing, as well as the photoresist thickness measured using Alpha-Step 100.



(a)



(b)

Figure 3.15 (a) Top view of mesa photoresist mask, (b) Alpha step result (scale at 100kA=10μm)

Before proceeding to the etching step, the sample is baked at 120C for two mintues to make the photoresist mask hard enough to withstand the dry-etching process. Figure 3.16 below illustrates the top view of a mesa photoresist mask after baking.

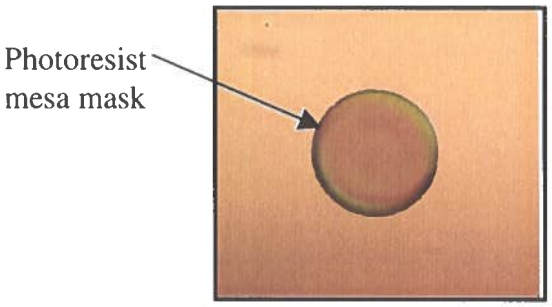


Figure 3.16 Baked mesa photoresist mask

Dr. Denish Patel used the load-locked, CAIBE dry-etching system located at the Engineering Research Campus (ERC). He carried out the sample etching by first loading a dummy GaAs sample without a AlGaAs epitaxial layer and running the system for five minutes. Afterwards he unloaded the dummy sample and immediately loaded the real sample. The etch time used for the real sample was about 3 minutes and 50 seconds. The sample was then unloaded directly. Figure 3.17 shows the mesa photoresist mask after dry-etching. Comparing the color of the photoresist mask in this image with the one in Figure 3.16 will lead to the conclusion that the photoresist mask is undergoing a chemical reaction with the gas species inside the etching chamber. To make sure that the surface of the resist has not just been roughened by ion bombardment and that this rough surface no longer reflects light as well as the smooth photoresist surface, a dummy sample was loaded into the etching system for only five seconds, which is a sufficiently short time not to cause the surface of the photoresist to be roughened. As a result, the same black color was observed.

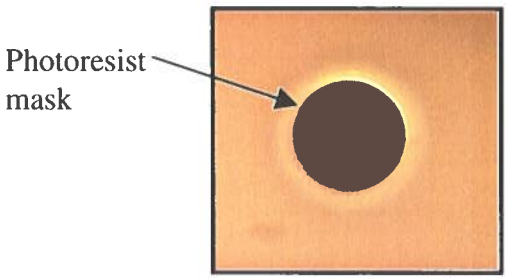


Figure 3.17 Plasma-treated mesa photoresist mask

The disadvantages of using the dry-etching are that the surface of the photoresist is roughened by ion bombardment, and as result it will be difficult to predict the mesa

height using the alpha step before striping the photoresist. Also, as soon as the etching begins, the photoresist mask will chemically react with the gases inside the chamber and this reaction will make it very difficult to strip away the photoresist afterward. Some research groups (Dr. Carmen Menoni's group) usually use plasma line asher to remove the plasma-treated photoresist, but the disadvantages of this are that it takes a relatively long time, up to one hour, at about 200W, and keeping the sample for that long of time inside the plasma line will expose the sample to a high temperature. Exposing the sample to high temperatures in the presence of oxygen for a long time (one hour) will grow a relatively thick oxide layer on the sample surface. If ohmic contact metals are to be evaporated next, then this thick layer of oxide will produce a high contact resistance, which will affect the device performance. Furthermore, if the sample already has ohmic contacts, then exposing it to high temperatures will cause some of the ohmic contact metals to diffuse deep into the sample, which may cause a short in the quantum wells in the case of a VCSEL. Other groups use a pretreated liquid solvent to strip away the plasma-treated photoresist. However, the disadvantage of this approach is that such a solvent reacts with some of the commercially-available substrates [12]. Therefore, before choosing this method one should make sure that this solvent would have no effect on anything other than the photoresist.

The technique I used to strip away the photoresist relied on the fact that exposing photoresist to ultraviolet light results in chemical changes to the photoactive components of the photoresist. This chemical reaction depends critically on the water content of the photoresist [3]. When the photoresist is exposed to UV light, the photoactive component degrades to form ketone. After this the ketone forms an indene. The indene carboxylic

acid is highly soluble in the basic developer. In the absence of water, the photoactive components form ester linkages with other molecules [11]. This cross-linking decreases the solubility of the resist. The advantages of using UV flood exposure in the presence of water in this method are that the method requires no special chemicals or plasma equipment, and hence is inexpensive. The solvent used is the same as that used in developing the photoresist, so additional chemicals are required. Also, the developer does not attack the substrate.

Based on the above argument, the sample was dipped in a hot DI water bath for about five minutes to force the photoresist to absorb some water. After that the sample was dried with nitrogen and exposed to UV light for six minutes using the mask aligner. As a result, the ketone formed indene carboxylic acid. The sample was then soaked in an ultra sonic bath of a basic developer, AZ400K. Figure 3.18 shows the mesa after stripping the photoresist mask, in addition to the mesa height, measured using the Alpha step.

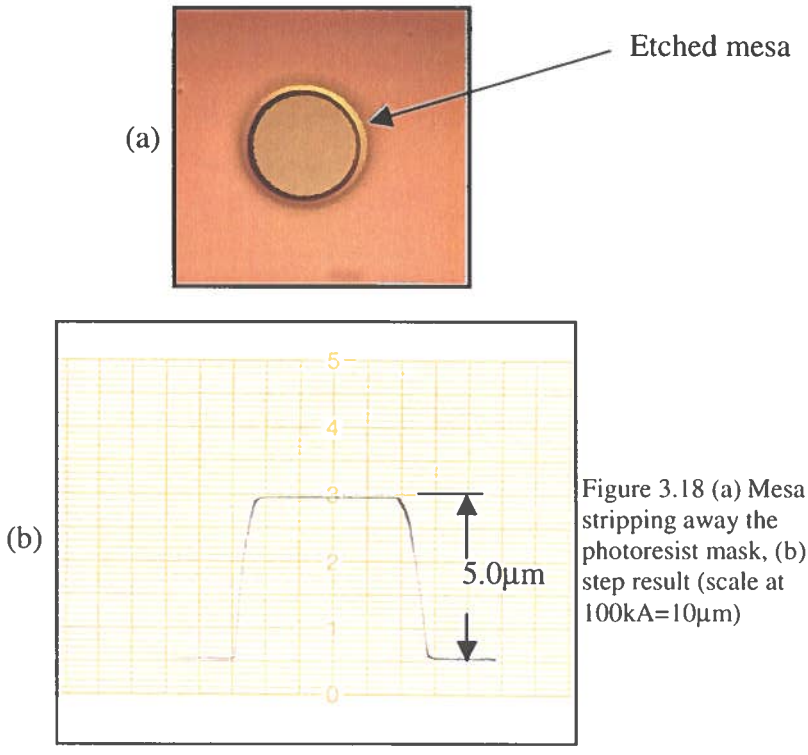


Figure 3.18 (a) Mesa after stripping away the photoresist mask, (b) Alpha step result (scale at 100kA=10μm)

The mesa is now ready to proceed to the next step, which is oxidation.

3.3.2 Wet oxidation

Oxidation is used to convert high aluminum content AlGaAs to aluminum oxide. It is carried out in a furnace using water vapor. The oxidation furnace is set up using a quartz tube inside a furnace with electrical heating elements. Water vapor is provided by heating water, and the resulting vapor is carried through the furnace tube using nitrogen gas. The amount of water vapor that can be transferred into the N_2 stream is proportional to the water temperature. To achieve maximum water vapor into the N_2 stream, the water temperature is kept below boiling temperature (75-85)°C. N_2 will bubble through the water to bring the vapor into the furnace. The inlet tubing has to be heated using heat tape at >(75-85)°C to prevent the condensation of vapor before entering the furnace [7]. The oxidation furnace apparatus is shown in Figure 3.19 below.

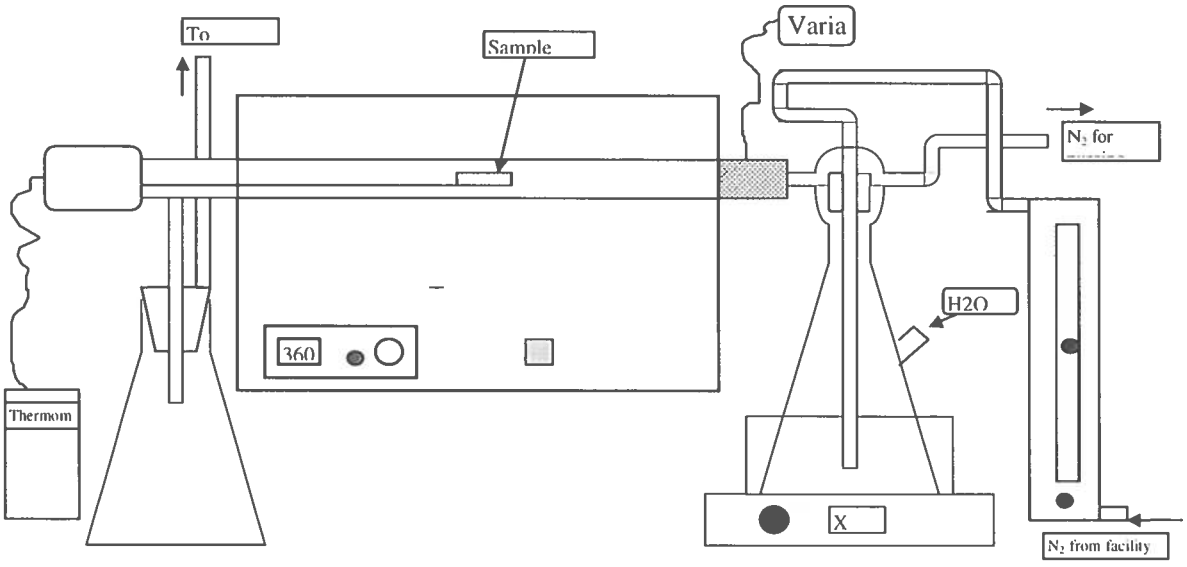


Figure 3.19 Oxidation furnace setup

First the furnace was operated without any sample so that we could obtain its temperature response in time. To operate the oxidation furnace, the exhaust at the left side of the furnace outlet is connected in order to collect the condensate from the oxidation process. After that, the flask and bath are filed with DI water. The water level in the flask and in the bath need to be is sufficient for the oxidation process (about 90% full). However the water level for the bath should be higher than the water level in the flask to ensure even heating of the water. The N_2 flow meter is then adjust to 560 sccm. Bubbles will then appear in the flask. If the pressure is too low or if the flow fluctuates too much, the pressure regulator is adjusted. The thermocouple thermometer for the sample, the VARIAC power control for the heat tape at the inlet of the furnace, and the furnace power switch are turned on. The red set-point button on the furnace is pressed to view the set-point; the furnace set-point should be at 360°C, which will result in a thermocouple temperature of about 420°C. The hot plateis then turned on, with a setting of around 8.5 for a temperature of (75-85)°C.

Figure 3.20 below illustrates the temperature of the oxidation furnace and the water temperature during the warm-up time for the settings mentioned above. It indicates that approximately 90 minutes are required for temperatures to stabilize.

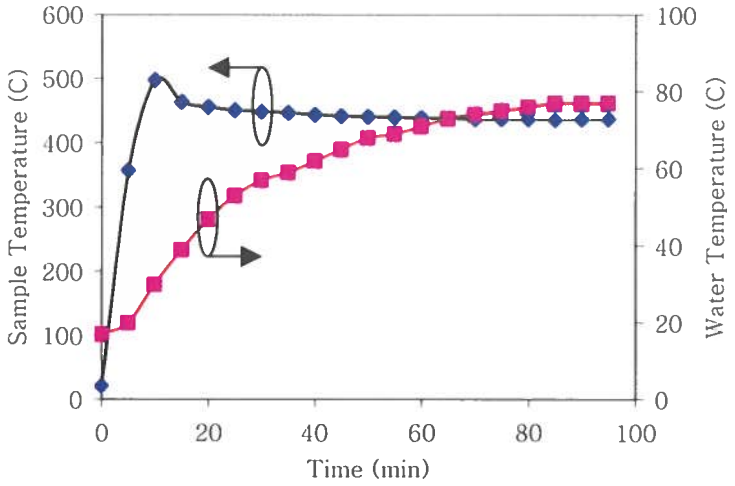


Figure 4.20 Oxidation furnace profile

To investigate the oxidation rate under the conditions stated above, a part of the real sample was loaded into the furnace after the system was left to stabilize for about 90 minutes. The test sample was oxidized for about 20 minutes and then the sample was unloaded. After that, the test sample was cleaved across one of the mesas and investigated using the scanning electron microscope (SEM). The image in Figure 3.21 below is a SEM photo for the cleaved mesa. Dark lines are the oxidized layers.

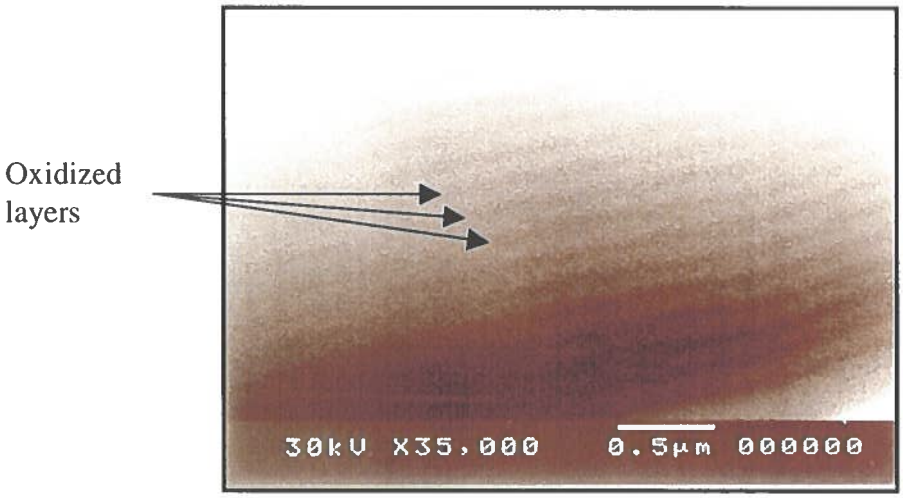


Figure 3.21 SEM photo for a mesa cross section

From the results above, the oxidation rate was about 0.3μm/minute for the low aluminum composition layers ($Al_{0.92}Ga_{0.08}As$) and about 1.0μm/minute for the high aluminum composition layer ($Al_{0.98}Ga_{0.02}As$). This means that the high aluminum composition layer ($Al_{0.98}Ga_{0.02}As$) oxidized ~4 times faster than the low aluminum composition layers ($Al_{0.92}Ga_{0.08}As$) [7].

Our real sample went through the same process and was oxidized for 20 minutes. Figure 3.22 below shows a top view of an oxidized mesa. The thin golden ring around the edge of the mesa results from the oxidation of several low-aluminum composition layers ($Al_{0.92}Ga_{0.08}As$). The color is the result of the reflection spectrum of the alternating oxide and $Al_{0.16}Ga_{0.84}As$ layers. The single oxide layer formed from the highest aluminum content, $Al_{0.98}Ga_{0.02}As$, layer is not visible in this optical photograph.

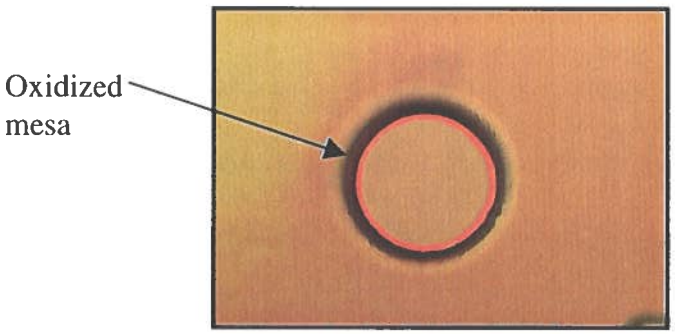


Figure 3.22 Top view of an oxidized mesa

Although the oxide aperture is not directly visible in the optical microscope, another way of estimating the aperture size is to use the golden ring shown in Figure 3.22. SEM data shows that its oxidization rate is one fourth of the high aluminum-composition layer ($Al_{0.98}Ga_{0.02}As$). Hence by measuring the width of the golden ring and multiplying it by 4, we can predict the oxide aperture size for this mesa. Figure 3.23 below illustrates this principle.

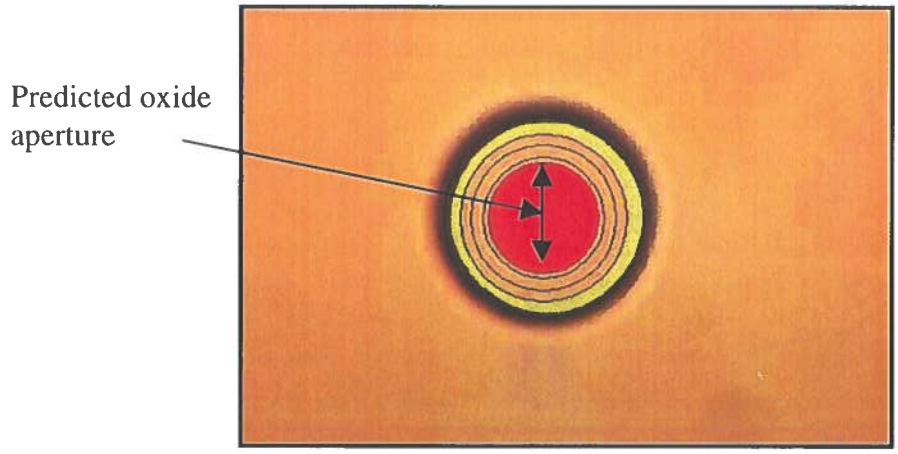


Figure 3.23 Predicted oxide aperture

3.3.3 Ohmic contacts

It is well-known that the ohmic contacts on the semiconductor device are used to pass the current into or out of the device [3]. A complete and comprehensive study of the basic theory of these ohmic contacts was recently reviewed by Rhoderick [14]. Ohmic contact resistance is defined as the contact resistance of a unit area for current flow perpendicular to the contact and is typically stated in units of $\Omega - cm^2$. Ideally, the contact resistance should be very small, in the range of $(10^{-5} - 10^{-6})\Omega - cm^2$, and the contact should have a linear I-V curve. Two different types of contacts present in the VCSEL structure are n-contacts and p-contacts. Whether one uses one or the other depends on whether the semiconductor surface is an n-type or a p-type.

Ohmic contacts are fabricated by evaporating different types of metals of certain thickness on the semiconductor surface. Before the contact can be used as an ohmic contact, the wafer (GaAs) must be heated until the metalization alloys into the layer underneath the contact. During this process, a component of the metal enters the GaAs

and highly dopes the surface. Nominal metal types for this doping function are Zn, Be, Cd and Mg for p-type GaAs and Ge, Se, Sn, and Si for n-type GaAs [15].

3.3.3.1 Top contact (n-contact)

The top contact was fabricated first. The top contact mask was patterned with a type of photoresist other than that used for etching the mesa, namely ma-N 490, which is a negative tone photoresist. We have a clear field mask for the top contacts. To pattern the contact metal, it is necessary to use either the conventional lift-off process with two positive photoresists or the simplified lift-off process with a single negative photoresist . The overhanging profile is critical for the lift-off process since it protects the part of the photoresist to be covered with the evaporated metals so that the acetone can attack the photoresist and remove the unwanted metals that lay on top of the photoresist, (refer to Section 3.2 for more details regarding the lift-off profile). If the contact is a dark field mask, it is necessary to use a positive-tone photoresist treated with chlorobenzene to make the profile suitable for the lift-off process. Soaking the photoresist in the organic solvent chlorobenzene removes residual solvents and low-molecule weight resins from the upper layers of the photoresist film. This slows down the developing actions for these layers and therefore yields an overhanging profile for lift-off [3]. The use of chlorobenzene to obtain an overhanging profile will be discussed later in this chapter. Figure 3.24 on the next page illustrates a comparison between the conventional Lift-Off and the simplified Lift-Off processes [12].

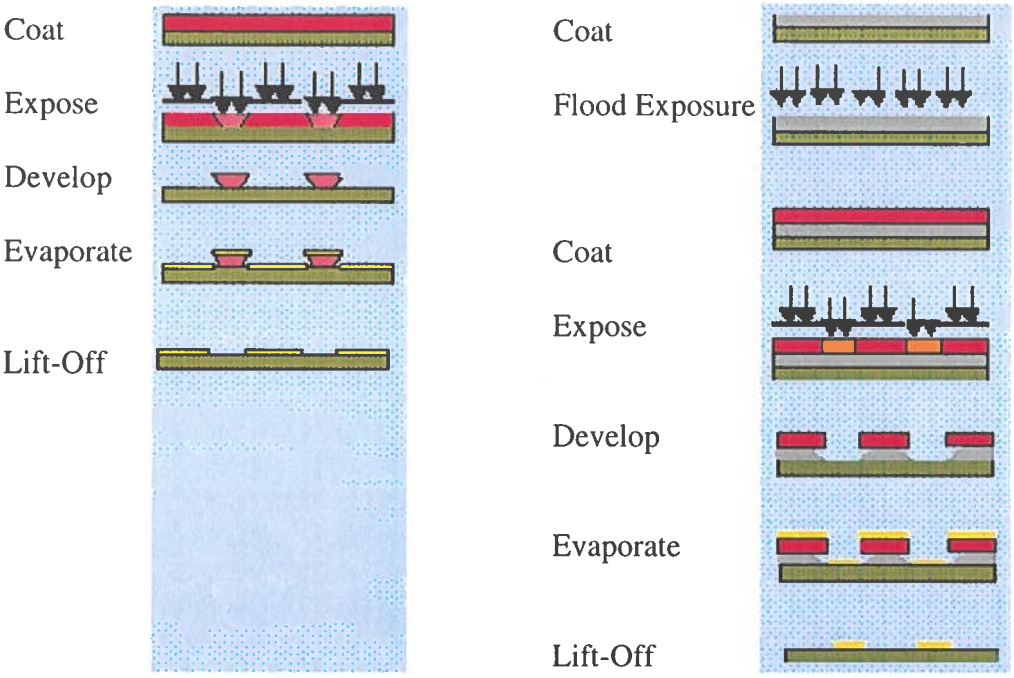
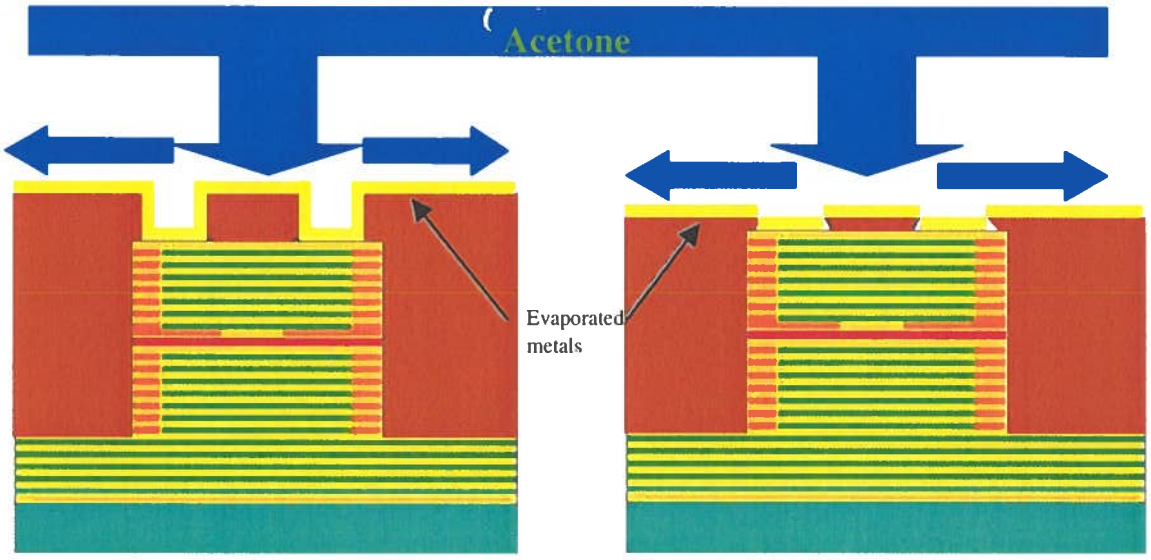


Figure 3.24 (a) Simplified Lift-Off processes, (b) Conventional Lift-Off [12]

Initially, AZ 5214-E negative tone photoresist was investigated for n-contact metal patterning, but the Lift-Off process failed using this photoresist. This was due to the fact that this photoresist has a maximum thickness of 1.6μm when spun at 3000 rpm while our mesa height was 5.0 μm. Consequently, with this thickness we failed to obtain an overhanging profile and sufficiently step coverage necessary for Lift-Off. Figure 3.25 below illustrates the need for sufficiently step coverage and an overhanging profile. In both cases, there was no place for the acetone to attach and strip the photoresist. In the case represented by Figure 3.35.a, where we have considerably step coverage and no overhanging profile, a mechanical "scrub" can be used, but it is not recommended since it may damage the surface of the sample. Ma-N 490 was therefore chosen because it is a negative tone photoresist that provides the right overhanging profile and is compatible

with the clear-field contact mask we used. The manufacturers of this photoresist also note that it may be used for either proximity or contact exposure, that it is fully compatible with conventional positive tone photoresist processing, and that it has high etching resistance, high structural resolution, and excellent adhesion on common surfaces. Also critical for our application is its thickness in the range of 5 to 14 μm, corresponding to spin speeds of 6000 to 1000 rpm. This high thickness was necessary since our mesa height is about 5 μm.



(a) (b)

Figure 3.25 (a) Non-overhanging profile, (b) Small step coverage

After choosing the suitable photoresist, the sample has go through the cleaning and photolithography processes. The sample was cleaned by first being soaked in a beaker filled with acetone. After that, the sample was taken out of the beaker with tweezers and rinsed with a methanol squirt bottle while there was still acetone on wafer, since the acetone or methanol should not be allowed to dry on the wafer surface. Next, the sample

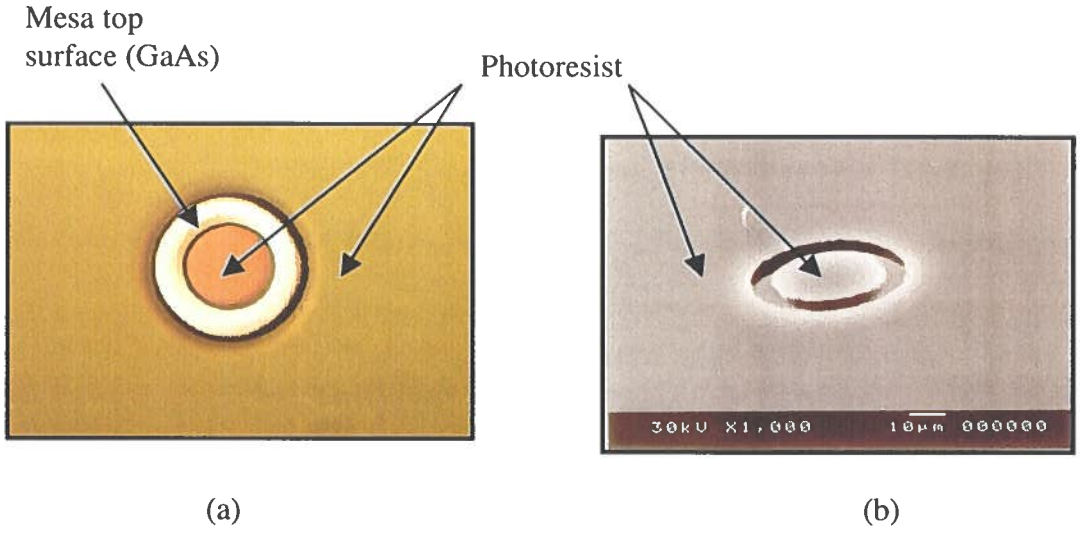
is rinsed in de-ionized (DI) water and blown-dry with nitrogen. Blow-drying is a quick and convenient method which is not as clean as spin-drying but is sufficiently clean for most research lab purposes. Drying a sample or wafer by "spinning dry" leaves very clean surfaces. Spin-dried samples are used for epitaxial growth or other processes in which the surface quality is very important. Next, the sample was baked at 120C for two minutes and left to cool down for about three minutes.

After cleaning the sample, the negative tone photoresist ma-N 490 was spun at 3000rpm for 30 seconds and baked for 10 minutes at 95°C to obtain a 7.5 μm photoresist thickness according to the data provided by the manufacturer [12]. Next, the photoresist edge-bead was removed using a sharp blade. Then using the mask aligner, the top contact photomask was aligned with the sample and the sample was UV-exposed the sample for about 90 sec. at 9.6mW/ cm^2. The 90 seconds. Exposure time was determined depending on the exposure dose decided by the manufacturer, which was 864 mJ/cm^2. The measured output power of our mask aligner using the optical power meter was 9.6mW/cm^2. The necessary exposure time was calculated as

$$time = \frac{864}{9.6} = 90\,\text{sec}.$$

The Ma-D 332S developer that was recommended by the photoresist vendor was investigated before proceeding with the real sample to determine the developing time, since it might vary. After that, the sample was dipped in the full strength ma-D 332S developer at room temperature for about 50 seconds [12]. Developing time was chosen depending on our own characterization for the developer at this particular photoresist thickness. Then the developed sample was examined in top view using the microscope camera to check whether the sample was fully-developed. Fully-developed means that

there is no photoresist left on the areas where the top contact metal will be deposited. Also, the scanning electron microscope was used to check the over hanging profile. Results of examining the developed sample are shown below. Figure 3.26 illustrates that the sample is fully-developed and that the overhanging profile for easier Lift-Off was achieved.



(a) (b)

Figure 3.26 (a) Photoresist mask for top contact, (b) SEM photoresist mask for top contact

If the small features that should be patterned developed away before the sample was fully-developed, then the exposure time has to be re-determined. But if the sample was fully-developed with all features present then the photoresist scum can be removed with the plasmaline asher. The plasmaline asher mainly removes very thin layers of dielectrics, but the concern in this step is that it may damage the overhanging profile we need for the Lift-off process. For more information about how to operate a plasmaline asher refer to the standard clean room operation manual in Appendix A

After the sample was inspected, it was soaked for 15 seconds in an HCl: H_2O solution with 1:1 ratio to remove the oxide layer formed on the GaAs surface [16]. After

that, the sample was blown-dry with nitrogen gas and mounted in the evaporator. It is important to remove the oxide layer before applying the ohmic contact metals since the presence of such an oxide layer will result in a high resistance ohmic contact, which will affect the VCSEL performance. Before closing the bell jar, the crystal which monitors the deposition rate was checked, in addition to the types of metals loaded in the evaporator, since the evaporator has to be loaded with only four different types of metals. The pressure inside the evaporator was pumped down to $\sim 2*10^{-6} Torr$.

While many metalizations have been examined for contacting n-type GaAs, none has been found to be better of quality than gold-germanium eutectics for reasonable doping ranges from 1×10^{16} to $5\times10^{17} cm^{-3}$ [3,17]. Gold-germanium ohmic contacts are usually applied with an overlay of another metal such as nickel. The nickel is introduced as a wetting agent and to prevent AuGe metal from "balling up". The germanium is used for doping the GaAs during alloying.

An Au-Ge-Ni-Au sequence of metals was chosen for the top n-type contact. The ratio of the lower Au and Ge layer thickness was chosen as 88% Au and 12% Ge percent by weight to make it a eutectic mixture. This percent are by weight corresponds to a ratio of layer thicknesses calculated using the volume densities of

$$\rho_{Au} = 19.311 g/cm^3, \rho_{Ge} = 5.35 g/cm^3$$

$$Vol_{Au} = 88/19.311 = 4.557 cm^3, Vol_{Ge} = 12/5.35 = 2.243 cm^3.$$

Since both metals will have the same area, this means that the fractional layer thicknesses are

$$\%Au_{thickness} = \left[\frac{4.557}{(4.557 + 2.243)}\right] * 100 = 67\%$$

$$\%Ge_{thickness} = \left[\frac{2.243}{(4.557 + 2.243)}\right] * 100 = 33\%.$$

The total AuGe thickness was chosen to be 1000Å since ohmic contact resistance will suffer if the contact thickness is less than 1000Å [3]. As a result, the Au thickness was 670Å, while the Ge thickness was 330Å. The nickel layer thickness that will be evaporated is approximately 280Å for each 1000Å of AuGe.

Au-Ge-Ni-Au was evaporated with thicknesses of (670:330:300:70) Å respectively. The reason why the last layer of 70 Å Au was added is to enhance the sheet resistance and make it easier to probe the device [3]. Although the last Au layer is very thin and will do little for the sheet resistance, it does keep the Ni from oxidizing. Another thick Au layer (~2000 Å) will be added when the metal pad is applied to reduce the sheet resistance. For more information about how to operate the beam evaporator, refer to the standard clean room operation manual in [Appendix A]. Figure 3.27 is a microscopic image of the mesa before the Lift-Off process.

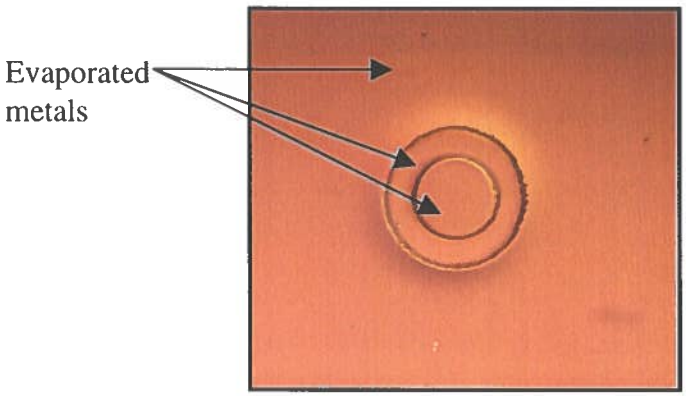


Figure 3.27 Mesa before Lift-Off process

Next, the lift-off process was performed. The sample was dipped into a beaker filled with acetone. Then the beaker was placed in the ultrasonic bath, which was filled with water. Ultrasound was applied to the sample in the acetone filled beaker for about five minutes. Ultrasonic waves caused the sample to vibrate, assisting the acetone in attacking the photoresist underneath the deposited metals. Figure 3.28 below illustrates the Lift-Off setup.

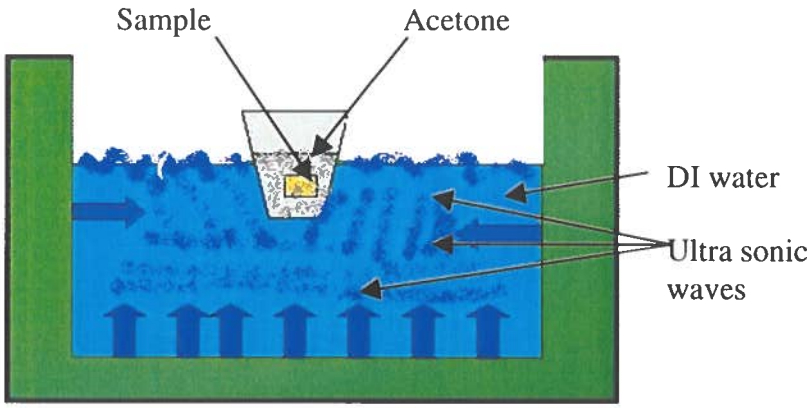


Figure 3.28 Lift-Off setup

After the lift-off process, the sample was washed with methanol, DI water and blown-dry. Figure 3.29 illustrates a top view of the mesa after Lift-Off with an Au-Ge-Ni-Au top contact prior to high temperature alloying.

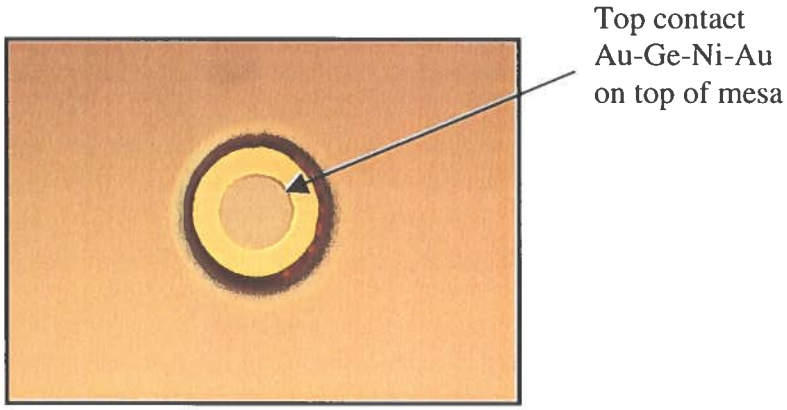


Figure 3.29 Top contact after Lift-Off

3.3.3.2 Bottom contact (p-contact)

The process for applying the bottom contact is very similar to that used for applying the top contact with few modifications. After cleaning the sample, photoresist ma-N 490 was spun at 3000rpm for 30seconds and baked for 10 minutes at 95°C to obtain a 7.5 μm photoresist thickness according to the data provided by the manufacturer [12]. Next, the photoresist edges were removed using a sharp blade. Then, using the mask aligner, the top contact photomask was aligned with the sample and the sample was UV exposed for about 200 seconds at 9.6mW/cm^2. The 200-second exposure time was determined according to the exposure dose determined by the manufacturer, which was 1900 mJ/ cm^2. The exposure time for the top contact is less than that of the bottom contact because in the first case the thickness of the photoresist to be developed is about 2.0μm, while in the bottom contact case the photoresist thickness that needs to be developed is about 7.0μm. The measured output power of our mask aligner, using the optical power meter, was 9.6mW/ cm^2.

$$time = \frac{1900}{9.6} \cong 200\text{sec}.$$

After this the sample was dipped into the ma-D 332S developer recommended by the vendor at room temperature for about 150 seconds. The developed sample was then examined using the microscopic camera for top view to check if the sample was fully-developed. Figure 3.30 shown below illustrates a top view of the mesa after developing. The light area represents the area where the bottom contact should be. After that, the sample was prepared for metal evaporation through the same steps used for the top contact.

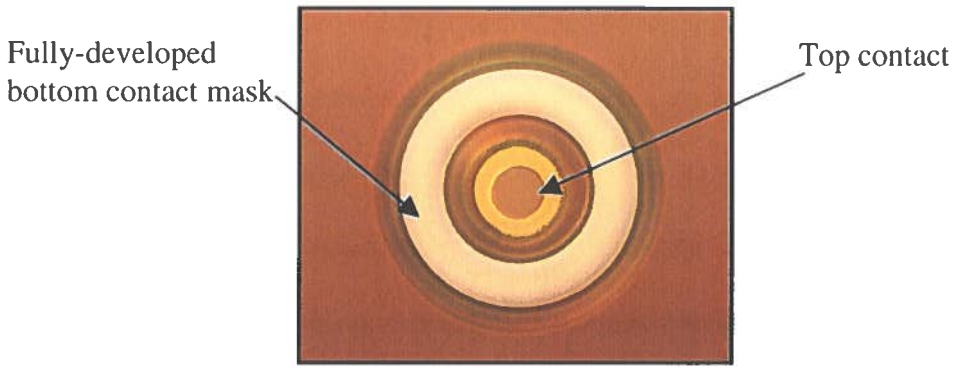


Figure 3.30 Mesa patterned with bottom contact mask

Different types of metalizations can be used for p-type contact including BeAu-Ti-Au, Ti-Pt-Au and ZnAu-Ti-Au. In out case Ti-Pt-Au metalization system cannot be used since the p-type layer that our contact will be deposited on is not highly-doped, consequently, Be or Zn must be used. Using Zn is not recommended since it will contaminate the evaporation system. BeAu-Ti-Au was chosen as our bottom-contact metalization. BeAu was applied as a pre-alloyed metal with (1% Be by weight) [3]. The concern in using a pre-alloyed BeAu is that the alloy composition of the metal mixture will not stay 1% Be as metal is evaporated from the crucible. The reason for this is that the heat of vaporization of Au is 334.4 $Kjmol^{-1}$ and for Be is 292.4 $Kjmol^{-1}$. Consequently the Be evaporation rate will be higher than the Au evaporation rate at the same pressure and electronic gun power [18]. Be was used to highly dope the surface layer.

BeAu-Ti-Au was evaporated with corresponding thicknesses of (500:300:700) Å. Figure 3.31 is a microscopic image of the mesa after p-contact metal evaporation but before the Lift-Off process. The inner photoresist circle protects the mesa underneath it and the top contact.

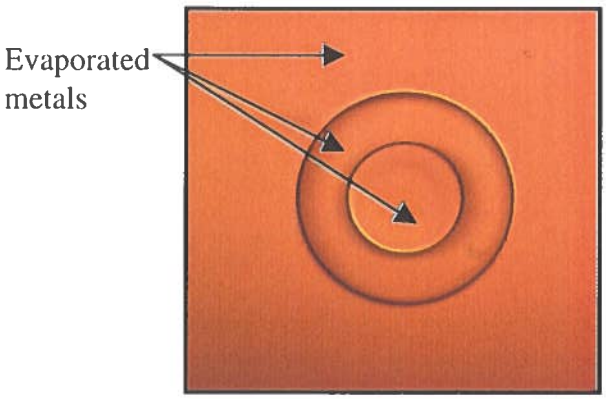


Figure 3.31 Mesa before Lift-Off process

Next, the sample went through the Lift-Off process using the same recipe used for top contact lift-off. Figure 3.32 below illustrates a top view of the mesa with both top and bottom contacts.

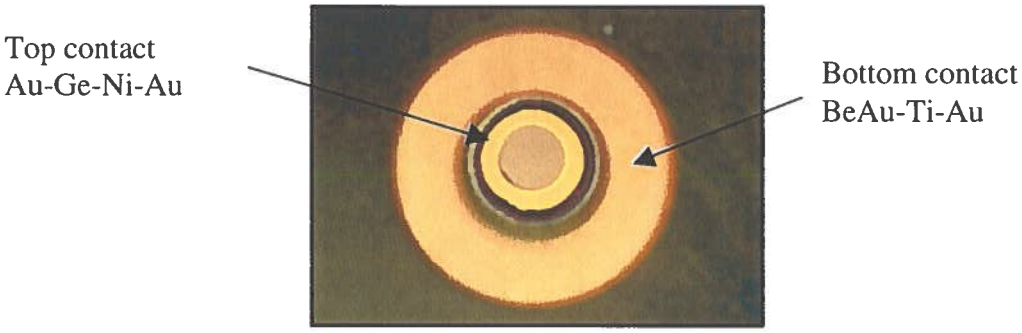


Figure 3.32 Mesa with top and bottom contacts

Before using these deposited metals as ohmic contacts, the sample contacts must be alloyed, which requires heating up the wafer to (400-480) °C in a nitrogen gas atmosphere for (30-60) seconds [3, 10]. During the heating and cooling, the sample components of the metal will diffuse into the semiconductor layer underneath it and highly dope it.

The sample was alloyed at 420 °C for 30seconds. [16]. The sample was then examined using a microscope. As shown in Figure 3.33 below, the alloyed contacts have a unique appearance, changed from what is observed in Figure 3.32. The metal appears splotchy, having dark and light spots. Such an appearance is necessary for lowest resistance contacts [3].

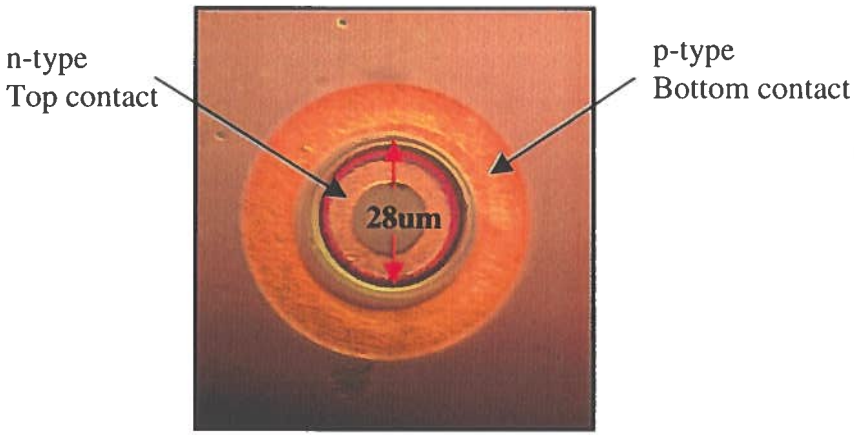


Figure 3.33 Mesa with alloyed top and bottom contacts

3.3.4 Planarization

Polyimides are typically applied in semiconductor micro-fabrication for use as stress buffers, for surface planarization, or as dielectric isolation layers [19]. Many factors should be considered in the combination of polymers and metals. The dielectric constant is an important factor in choosing the polymer since a low dielectric constant will result in a smaller RC time constant and consequently faster devices. Also, the polymer should have low moisture absorption so that it has stable properties. In addition, low curing temperature is important if the sample is sensitive to high temperatures. Good adhesion properties to metals such as gold are important factors that also need to be considered [19, 20].

3.3.4.1 Overview

Polyimide is used to planarize the VCSEL before depositing metal interconnects and bonding pads. Two types of polyimide have been used in our VCSEL fabrication: a non-photosensitive polyimide, which is not sensitive to UV light, and a photosensitive polyimide, which is sensitive to UV light. The standard photolithographic process for patterning non-photosensitive polyimides requires the use of a photoresist to serve as an etch mask for etching the polyimide. This introduces additional steps for applying, drying, patterning, developing and stripping the photoresist. Photosensitive polyimides make the fabrication process easier by reducing the number of steps required to pattern polyimide coatings [21]. The first one, which uses the non-photosensitive polyimide, failed in our application. More explanation and Scanning Electron Microscope (SEM) photos will be presented later to explain why it failed. Figure 3.34 below represents a comparison between the steps of the process for the two types of polyimides.

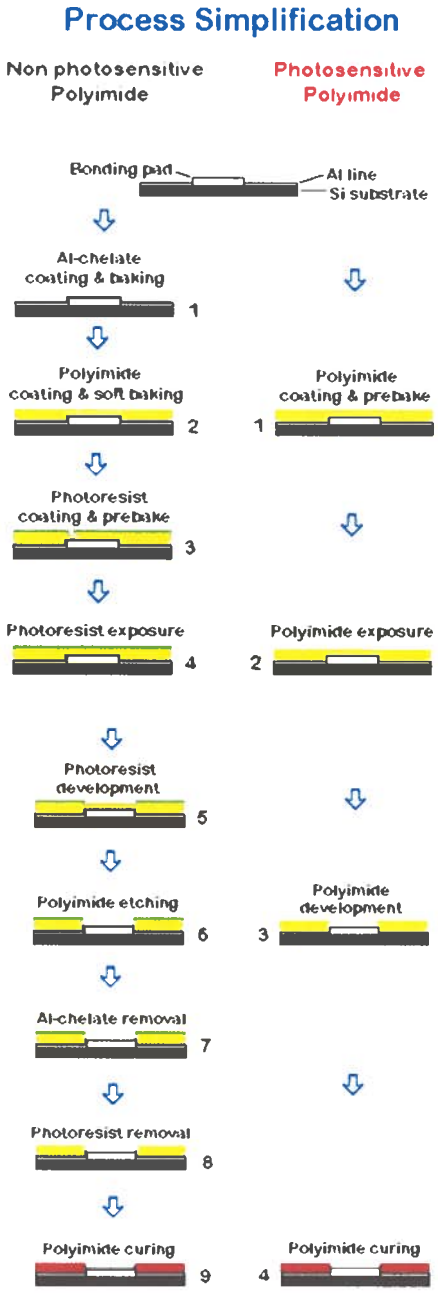


Figure 3.34 Process comparison between photosensitive and non-photosensitive polyimides [21]

3.3.4.2 Non-photosensitive polyimides

The non-sensitive polyimide that was investigated, Pyralin PI 2555, had been previously used by other students in the CSU cleanroom [21]. Before applying this type of polyimide, the surface of the sample has to covered with VM-651 adhesion promoter. VM-651 adhesion promoter is an organosilane which is used to improve the adhesive properties of all types of Pyralin polyimide coatings to the substrate surface [21].

To prepare a VM-651 adhesion promoter solution, a specific procedure has to be followed. First, a small container of pure VM-651 was removed from the freezer and allowed to warm up to room temperature (a bottle of adhesion promoter or polyimide should not be opened until it has warmed to room temperature to avoid contamination caused by water condensation). The following solution was then mixed in a specimen container: 95 ml Methanol, 5.0 ml DI H_2O, and 1.0 ml VM-651. This solution needs to stand a *minimum* of 12 hours before using. Once mixed, the adhesion promoter solution has a shelf-life time of five days. Using it after that will result in poor adhesion [21]. However, an alternative method for quickly preparing the VM-651 adhesion promoter solution without waiting for 12 hours was used, containing: 1000 ml of DI water and 5.0 ml of VM-651. This may be used immediately but its shelf life is only 24 hours [21].

The small container of PI 2555 was removed from the freezer and left to warm up to room temperature. Again, to avoid contamination it was not opened until it was warm. The sample was then cleaned according to the standard cleaning procedure mentioned earlier. After that, the sample was pre-baked for two minutes on the 95°C hot plate to make certain that there was no moisture on its surface. Next, the sample was mounted on the photoresist spinner. Subsequently, the promoter was applied by forming a puddle on

the sample using a syringe with an attached 0.2 μm filter. The puddle was allowed to stay on the wafer for about 20 seconds, and then the VM-651 solution was spun for 30 seconds at 5000 rpm. After that, the sample was ready for Pyralin PI 2555 polyimide coating [21].

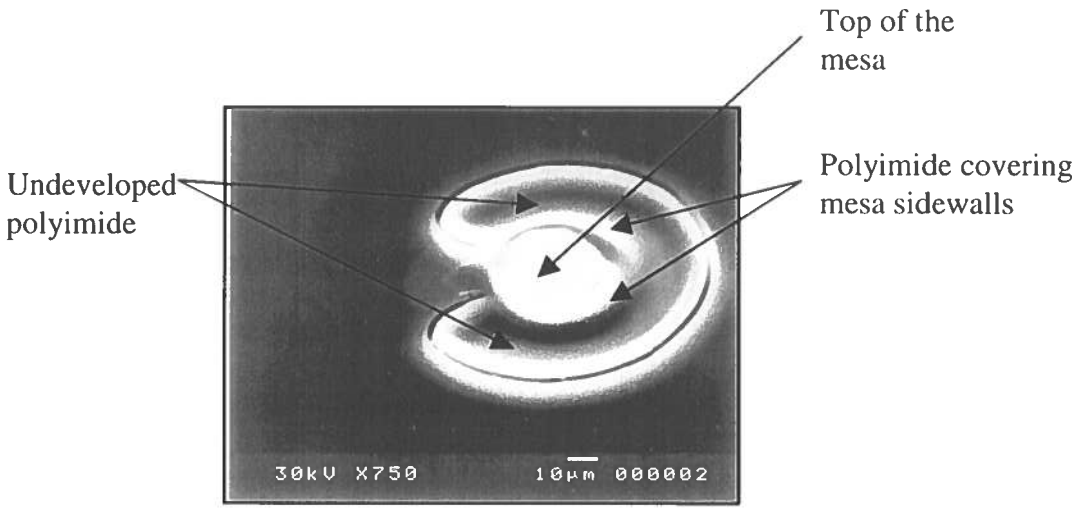
The sample was transferred to the polyimide spinner. Using a pipette, PI 2555 was dropped so that it completely covered the sample; it was left stand for 30 seconds to flow over and fill in the sample topology. After that, it was spun for 30 seconds at 5000 rpm as recommended in the manufacturer data sheet. Next, the sample was baked for ten minutes on the 120°C hot plate [21]. The sample was then left to cool down in dry air (skipping this step may result in severe cracking of the polyimide film).

The sample was moved back to the photoresist spinner and Shipley 1818 photoresist was applied and spun for 30 seconds at 6000 rpm. Next, the sample was baked for two minutes on the 95°C hot plate before being placed in the Karl Suss mask aligner for alignment with the photomask and UV exposed at 15 mW/cm^2 for eleven seconds. After exposure, the sample was developed in AZ 400K: DI H_2O (1:4) for around 45 seconds [Appendix C].

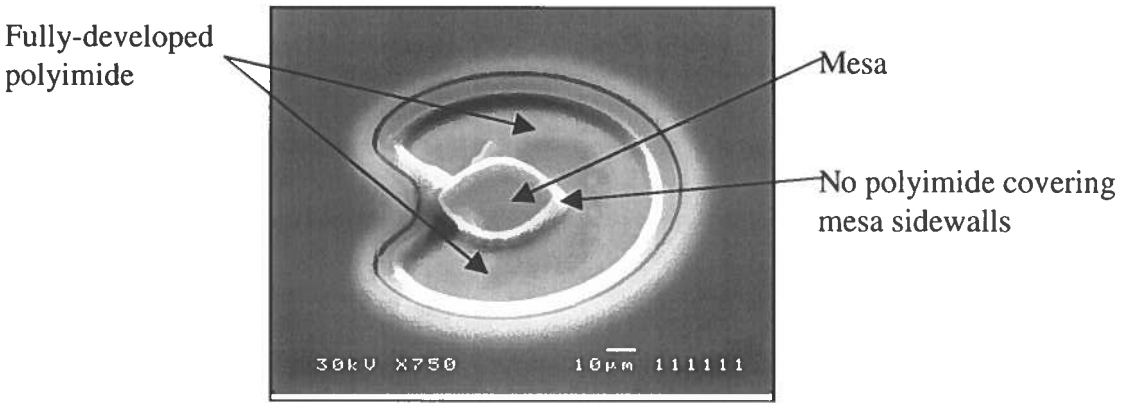
The photoresist pattern serves as a mask that defines the areas where the polyimide will be etched. The developer attacks both the UV exposed photoresist and the underlying polyimide, while the unexposed photoresist will not be developed and will protect the polyimide underneath it. Consequently, the etching of the underlying polyimide occurs based strictly on how long the sample is developed, regardless of whether or not it has received UV radiation. Subsequently, the sample was inspected using the microscope to make certain that the photoresist and polyimide had patterned

properly. The photoresist must be stripped prior to curing because the high curing temperature reflows and bakes the photoresist, which will damage the polyimide profile and make it hard to remove the photoresist. Finally, the sample was rinsed *quickly* with acetone, methanol and DI H_2O to strip away the photoresist. The acetone also attacks the uncured PI 2555, but not as rapidly as the photoresist, so the use of acetone should be minimized while insuring removal of the photoresist.

More than six samples of Pyralin PI 2555 polyimide were tried, but all of them failed. It was found that sufficient developing time to clear the full thickness of the polyimide was accompanied by unacceptable lateral etching that removed the polyimide layer that lies on the sidewalls of the mesa. Figure 3.35 below shows SEM images for two samples. Image (a) shows the polyimide profile that resulted from 180 seconds of developing. This development time was not adequate to fully remove the polyimide in the intended arc-shaped via for the bottom p-contact around the mesa, although it did preserve the polyimide covering the sidewalls of the mesa. Image (b) illustrates the polyimide profile after a longer development time of 195 seconds. This longer development time was sufficient to clear the arc-shaped polyimide via, but it also resulted in removal of the polyimide on the mesa sidewalls. Of particular concern is the fact that the polyimide isthmus or neck shown to the left of the mesa in the figure has been partially consumed. This will allow the metal interconnect that would be placed on that polyimide neck to potentially contact the mesa sidewall and short-out the laser junction.



(a)



(b)

Figure 3.35 SEM photos for mesa (a) Under-etched polyimide, (b) Over-etched polyimide

In summary, the Pyralin PI 2555 polyimide had the following disadvantages: It requires an adhesion promoter, which increases the complexity of processing and cost of chemicals . Next, it requires a relatively high curing temperature, 250 °C for a long duration of 180 minutes, according to its data sheet [21]. Based on the results mentioned, no curing was attempted. Also its cured film thickness ranges from 1.7 µm to 3.5 µm

[21], while the preferred cured film thickness is about 5 μm. Further, the PI 2555 polyimide has a bad etching profile, as concluded from our own experiments, illustrated in Figure 3.35. As a result, we began to search for a photosensitive type of polyimide.

3.3.4.3 Photosensitive polyimide

A negative tone PI-2700 photosensitive polyimide series was available, but it was not used since the photomask we have is a clear field mask.

A HD-8000 positive tone photosensitive polyimide was chosen. The key advantages of HD-8000 polyimides are: HD-8000 is a positive tone polyimide which is compatible with our photomask; it contains a built-in adhesion promoter; it can be directly exposed without needing an additional photoresist layer for patterning, it is developed with positive photoresist developer; as it is cured in only 90 minutes and provides a cured film thickness in the range of (5-12) μm; and it offers high resolution, good room temperature viscosity stability, and a low dielectric constant (~3.4 at 1 kHz) after curing [Data sheet: Appendix D].

Before incorporating the HD-8000 polyimide directly in VCSEL fabrication, its profile on a dummy GaAs sample was investigated. Four samples were processed to study the repeatability of this type of polyimide. The four samples were all processed on different days. The processing steps that were performed will be discussed later in this chapter. Figure 3.36 below illustrates a top view of the patterned HD-8000 polyimide and a cross-section drawing. The annular polyimide ring on top of each mesa shown below is about 1μm wide with a 9μm depth from the p-contact opening and 3μm from the top of the mesa side.

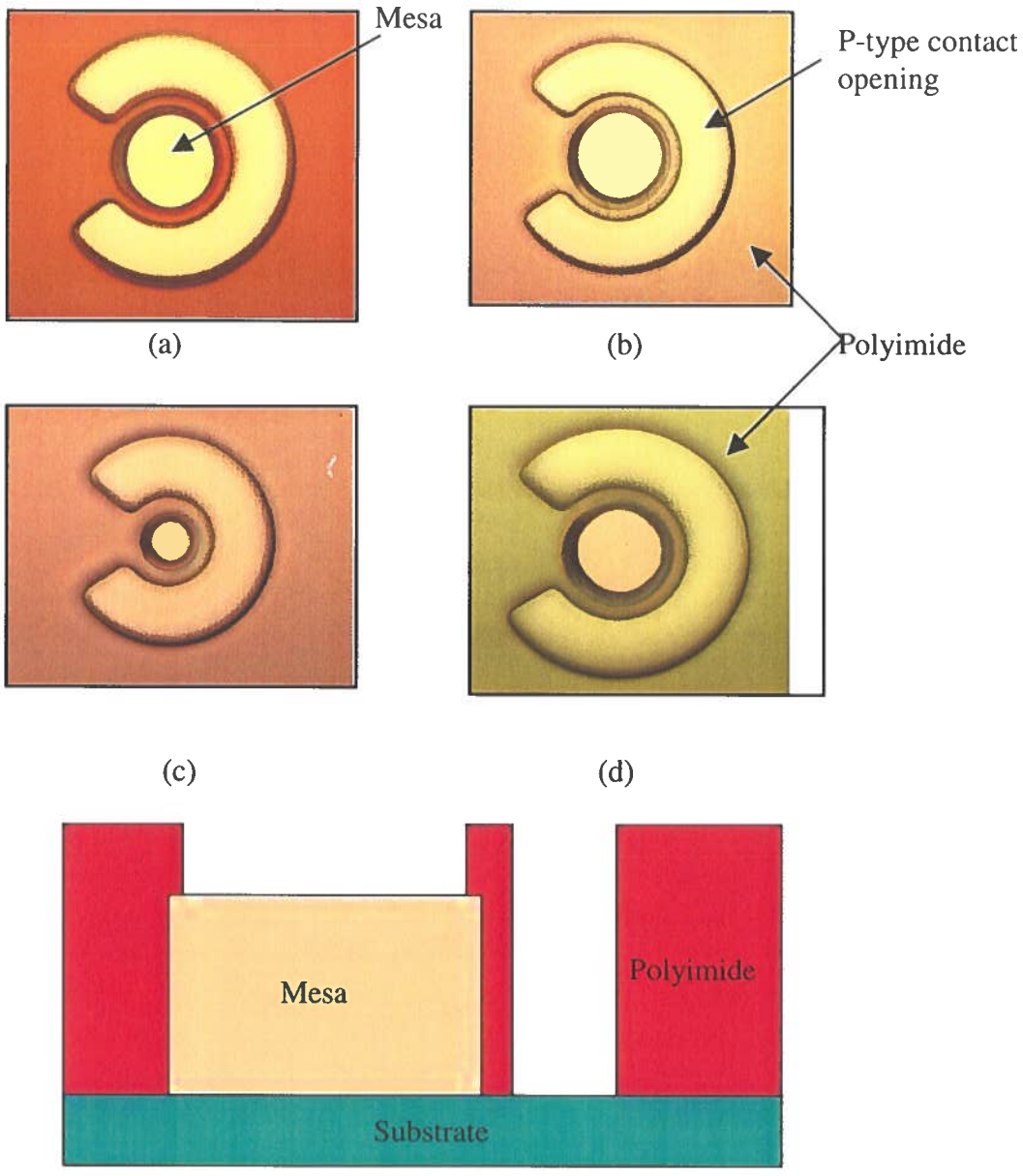


Figure 3.36 Top view of the polyimide photomask patterned using polyimide HD-8000

It is clear from Figure 3.36 that this type of polyimide is repeatable, since up to three samples were processed and we get the same developing profile. Moreover, a very

good resolution can be observed by looking at image (c), which represents the smallest mesa of this mask set.

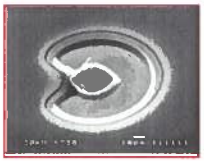
		HD-8000 [Appendix D]		PI 2555 [21]
Number of processing steps	☺	***4***	X	9
Photoresist film	☺	***Not needed***	X	Needed
Adhesion prompter	☺	***Built in***	X	Need to be added
Total curing time (min.)	☺	***90***	X	180
Cured film thickness (μm)	☺	***5-12***	X	1.7-3.5
Dielectric constant	☺	***3.4***	☺	***3.3***
Etching profile	☺	***Very good*** 	X	Bad 

Table 3.1 Comparison between HD-8000 and PI 2555 polyimides

The real VCSEL sample was processed as follows: First the sample was cleaned. Next the standard photolithography process was carried out but with some changes in the spinning speed and baking temperature according to the manufacturer's data sheet [Appendix D]. After exposure, the sample was baked for 100 seconds at 115 °C. The sample was left to cool down to ambient temperature for about 30 minutes prior to proceeding with the developing step (If the sample is not allowed to cool prior to developing the cured polyimide will have severe cracks). The reasoning behind this is that by decreasing the polyimide surface temperature to 20°C by dipping the sample in the developer while the temperature of the polyimide underneath the surface is about 120°C. As a result the surface of the polyimide shrinks while the polyimide underneath is

hot, which cracks the polyimide. Figure 3.37 shows a polyimide that was developed while the sample was still hot.

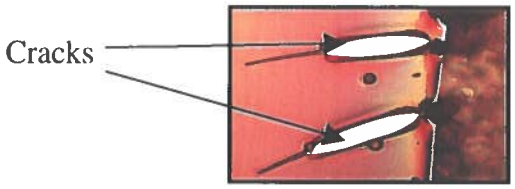


Figure 3.37 Polyimide with cracks

The sample was then developed using the AZ400K developer diluted with DI water (1:4). The developing step was carried out with the sample at the microscope stage by the use of a UV-blocking filter, enabling us to monitor the sample while it was developing so that we knew exactly when to take it out of the developer. Correct development is important since over-developing will result in losing the polyimide wall surrounding the mesa. After developing, the sample was rinsed by squirting it with DI water while it was spun at 1000 rpm for ten seconds. Immediately after the rinse, while the sample was still on the spinner, it was spin-dried at 3500rpm for ten seconds to make sure that the developed polyimide was cleaned [Data sheet: Appendix D].

The sample was then inspected using both the microscopic camera and the Alpha-Step surface profilometer. Figure 3.38 illustrates a top view of the mesa with polyimide and a plot of the sample surface profile. The α-Step full scale is 100kA=10μm.

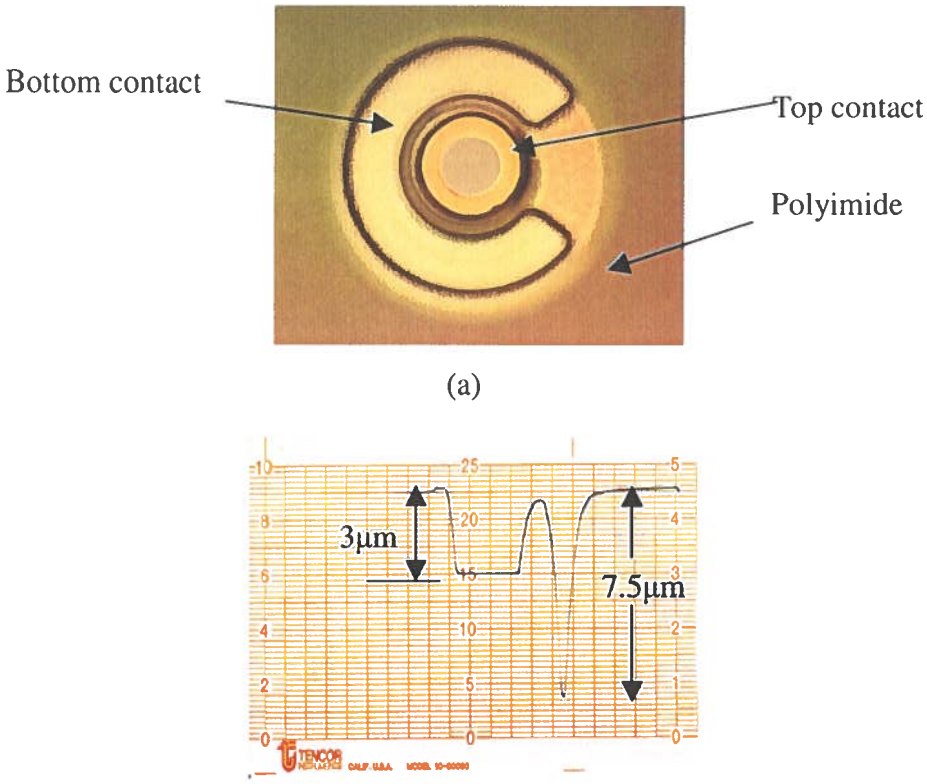


Figure 3.38 (a) Developed Polyimide, (b) Polyimide surface profile α-Step (scale at 100kA=10μm)

After developing, the sample has to pass through the curing process in which the sample temperature is raised to a certain value for a specific time. The objectives of the curing process are to remove the residual solvents, to remove all cross-links, and to complete the imidization, and the adhesion processes. Since all four events occur together at a given temperature, the cure schedule is a very important step that impacts the cured film quality and associated mechanical properties. Many variables need to be considered in curing polyimide films, such as the curing furnace, atmosphere, loading temperature,

ramp rate, soaks (holding temperatures), final cure temperature and ramp down [21]. Curing should be carried out in a nitrogen atmosphere. Figure 3.39 below shows a schematic illustration of the curing furnace that was used. For a detailed operational procedure for this curing furnace, refer to [Appendix A].

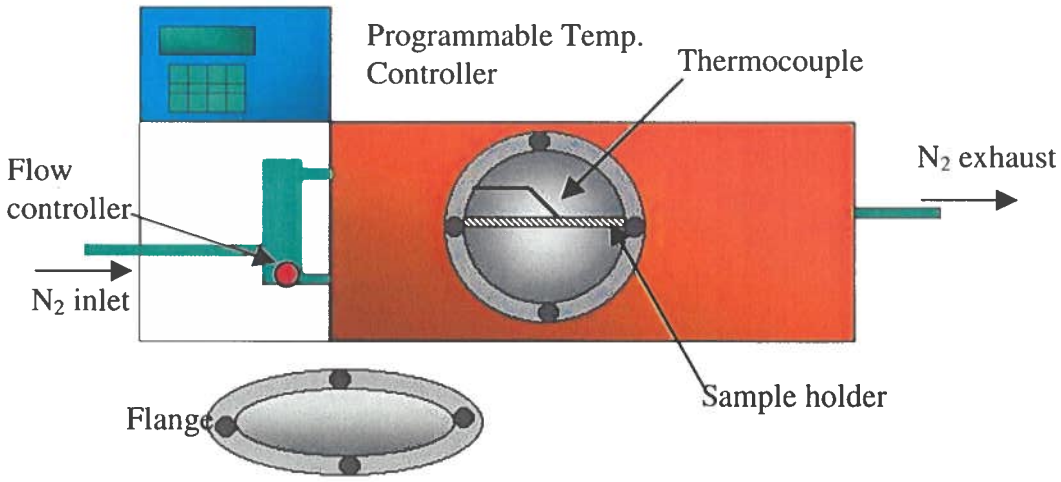


Figure 3.39 Curing Furnace setup

Before introducing the final curing schedule that was used to cure the real sample, details of some failures will be discussed. Before our real VCSEL sample was loaded into the curing oven, dummy GaAs samples coated with HD-8000 polyimide were tested. The curing schedule used was as recommended by the manufacturer [Appendix D]. The process began by loading the sample into the oven at <150°C and then gradually ramping from the loading temperature to 350°C over a 60-minute period. Next the temperature was held at 350°C for 30 minutes. Finally, the sample could be removed immediately or allowed to cool down. The polyimide furnace's programmable temperature controller was programmed according to this curing schedule.

A first sample (S1) was loaded, cured according to the schedule, unloaded and inspected under the microscope. Figure 3.40 below clearly illustrates that the curing process on this sample failed for some reason. Most of the polyimide was gone and only thin lines stay on the sample surface.

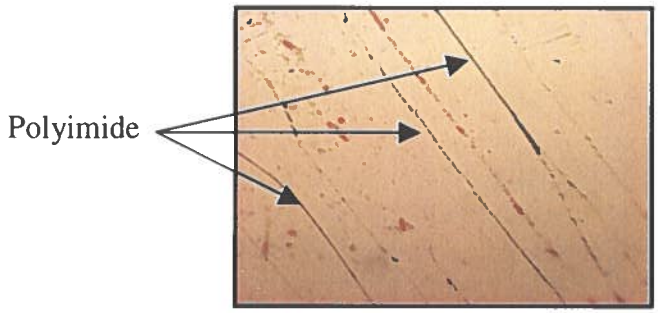


Figure 3.40 Thin lines of polyimide on the sample surface

Since nearly all of the polyimide film was missing, the failure of the first sample appeared to be an adhesion problem. This motivated preparing a second sample (S2) with the use of the adhesion prompter VM-651 as an interface layer between the sample surface and the polyimide layer [Appendix E]. Following the finishing of the curing cycle, the sample (S2) was unloaded an examined under the microscope. Figure 3.41 below clearly illustrates that the addition of the adhesion promoter, VM-651, gives better results, but still a high percentage of the polyimide was gone.

Figure 3.41 Cured polyimide on the sample surface

Different samples with different curing schedules were tried but they all failed. For images and detailed steps for these samples, refer to [Appendix E].

As a result, the curing furnace profile was examined. Another thermocouple was installed inside the curing furnace so that the two measurements for the temperature inside the furnace could be compared. The system was then allowed to pass through a whole cycle, i.e., the curing schedule recommended by the vendor of the HD-8000 polyimide [21]. A comparison between the temperatures measured by the built-in thermocouple and the additional installed one revealed that the built-in thermocouple gave temperature readings that were substantially lower than the actual temperature. For example, when the built-in thermocouple read 350°C, the actual temperature according to the additional thermocouple was about 475°C. The plot in Figure 3.42 on the next page shows the relationship between the temperature controller settings and the actual temperature inside the furnace.

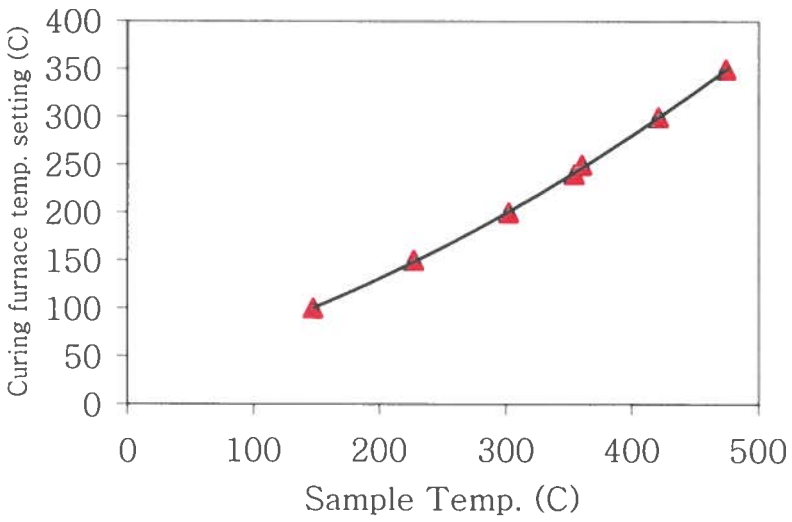


Figure 3.42 Temperature controller settings vs. sample temp. (The actual temperature inside the furnace)

Using the curve above to cure our sample at 350°C, we set the temperature controller to 240°C. The real VCSEL sample was loaded with the curing schedule adjusted as follows: the sample was loaded into furnace at 20°C, and the temperature was ramped from 20°C to 350°C over a 60-minute period *(furnace setting ~240°C)*. After that, the temperature was held at 350°C for 30 minutes *(furnace setting ~240°C)*. Finally, the sample was unloaded immediately or allowed to cool down.

To make sure that the polyimide film was sufficiently cured, a simple test was carried out on the edge of the real sample. The probe station tip was used to press and make a scratch on the cured polyimide surface. Depending on the scratch profile a decision was made. If the surface was squishy, the polyimide was not sufficiently cured. Figure 3.43 below shows the shape of a cured polyimide film at the correct temperature and time, and a top view of the mesa after curing the polyimide.

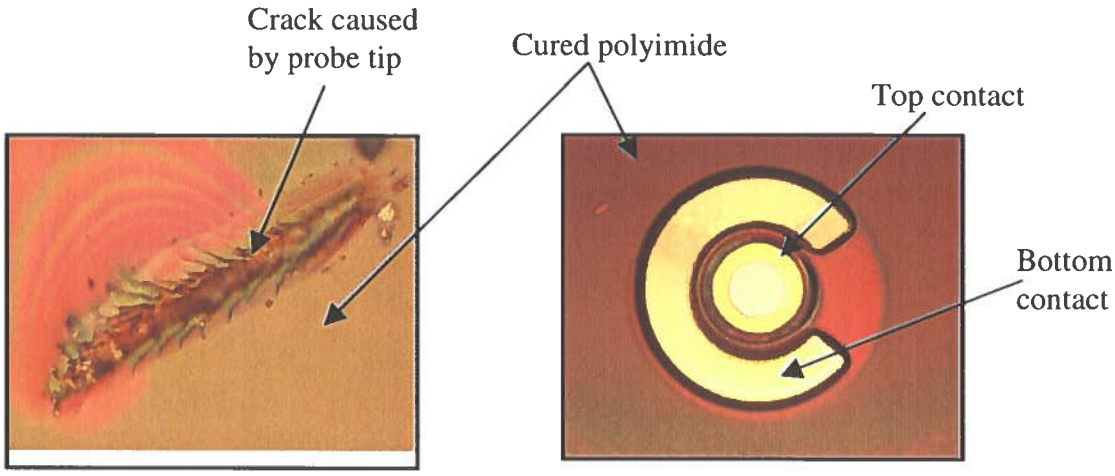


Figure 3.43 (a) Crack caused by probe tip, (b) Top view of the mesa after curing the polyimide

3.3.5 Metal interconnection

Metal interconnects and bonds are probing pads which allow for electrical connection to the VCSEL. For example, probe station tips can be placed on probe pads so that current can pass through the VCSEL. Depositing pad and interconnect metal is the last part of fabrication and proceeds with the following steps: After cleaning the sample, positive tone AZ4400 photoresist was used instead of the ma-N490 used for contacts since the photomask we have for the interconnects is compatible with positive tone photoresists, while the ma-N 490 photoresist in a negative-tone one. A 4.0μm step coverage can be easily obtained as recommended by the vendor. AZ4400 was applied and exposed to UV using the interconnect photomask. Next, to make the profile suitable for the lift-off process, the sample was soaked in the chlorobenzene for four minutes. Soaking the photoresist in the organic solvent chlorobenzene removes residual solvents and low molecular weight resin from the upper layers of the photoresist film. The removal of these photoresist constituents slows down developing actions for these layers so that the top layer of the resist develops less rapidly than the underlying photoresist. The reduced development of the top layer yields an overhanging profile for lift-off [3]. It was noted that the use of the chlorbenzene does not affect the required exposure or development times. Next, the sample was developed and loaded into the evaporator. For the detailed recipe, refer to [Appendix C]. Figure 3.44 below represents the sample after developing.

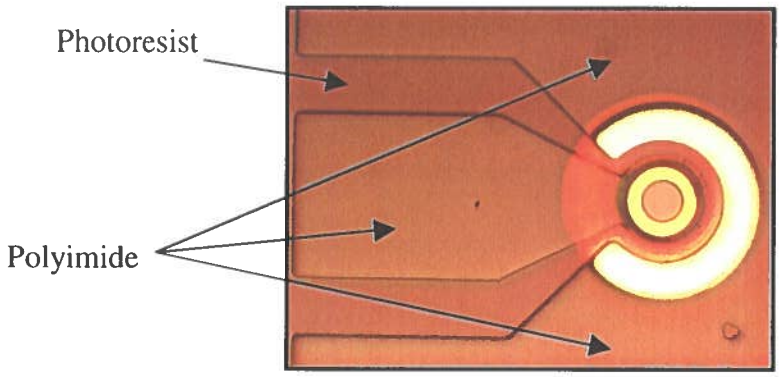


Figure 3.44 Sample after developing

Ti-Au was evaporated with thicknesses of (200:3000) Å, respectively. The lift-off process was then carried out using the same setup mentioned earlier in this chapter. Figure 3.45 below shows the VCSEL after Lift-Off process. VCSEL now is ready for testing.

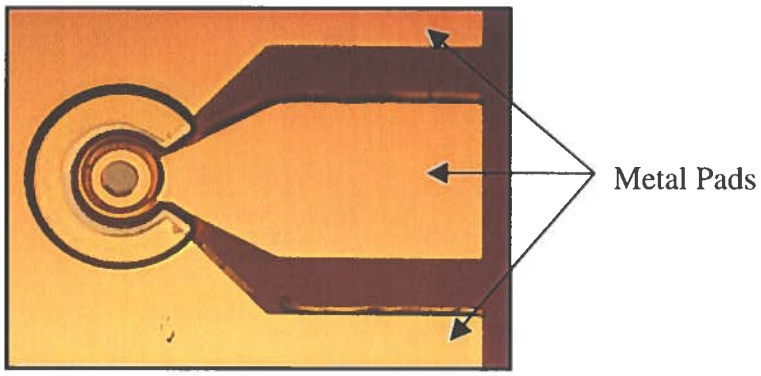
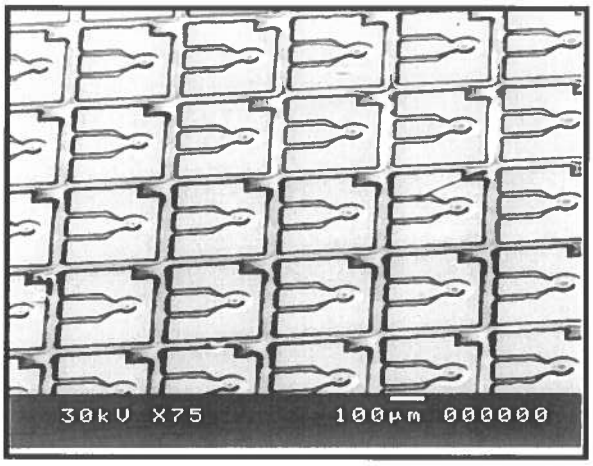
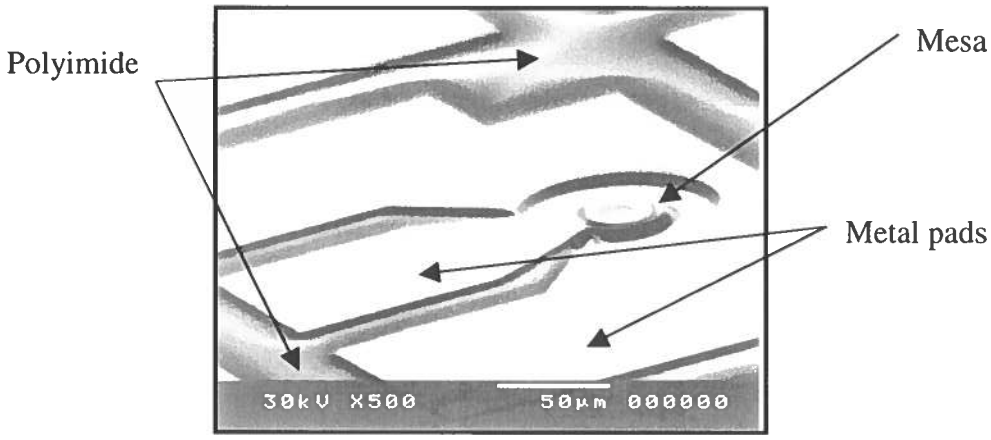


Figure 3.45 VCSEL after interconnect Lift-Off



(a)



(b)

Figure 3.46 Shows SEM photos for the real sample

3.4 Mask Set Analysis.

The mask set has to be used in a certain order. Five different masks, provided by Dr. David Wodered from Cornell University, were used in this research. Figure 3.47 below represents one unit cell from each mask. Each mask contains several sizes of its unit cells. A different color was used so that all the masks could be distinguished when combined together, as detailed later in this chapter.

The sequence for using the mask set shown in Figure 3.47 is as follows: The first mask to be used is the mesa mask, next the top contact mask, then the bottom contact mask, then the polyimide mask, and finally the interconnect mask. Figure 3.48 below illustrates the combination of the five masks used.

Each mask has its own alignment marks, which mainly look like a plus sign (+). After the use of each mask, a unique alignment mark is printed on the sample so that the next mask alignment mark must be aligned with the one previously obtained from the preceding mask. Figure 3.49 illustrates the combination of all the alignment marks for all the masks superimposed on each other. The arrays of triangles, which appear in Figure 3.49, are used to investigate metal-to-semiconductor sheet resistance [3]. Each VCSEL is also labeled with a number that represents the oxide aperture size after oxidation. For example, the number 2 that appears on Figure 3.48.b, means that after oxidation the oxide aperture of this particular VCSEL must be 2.0μm.

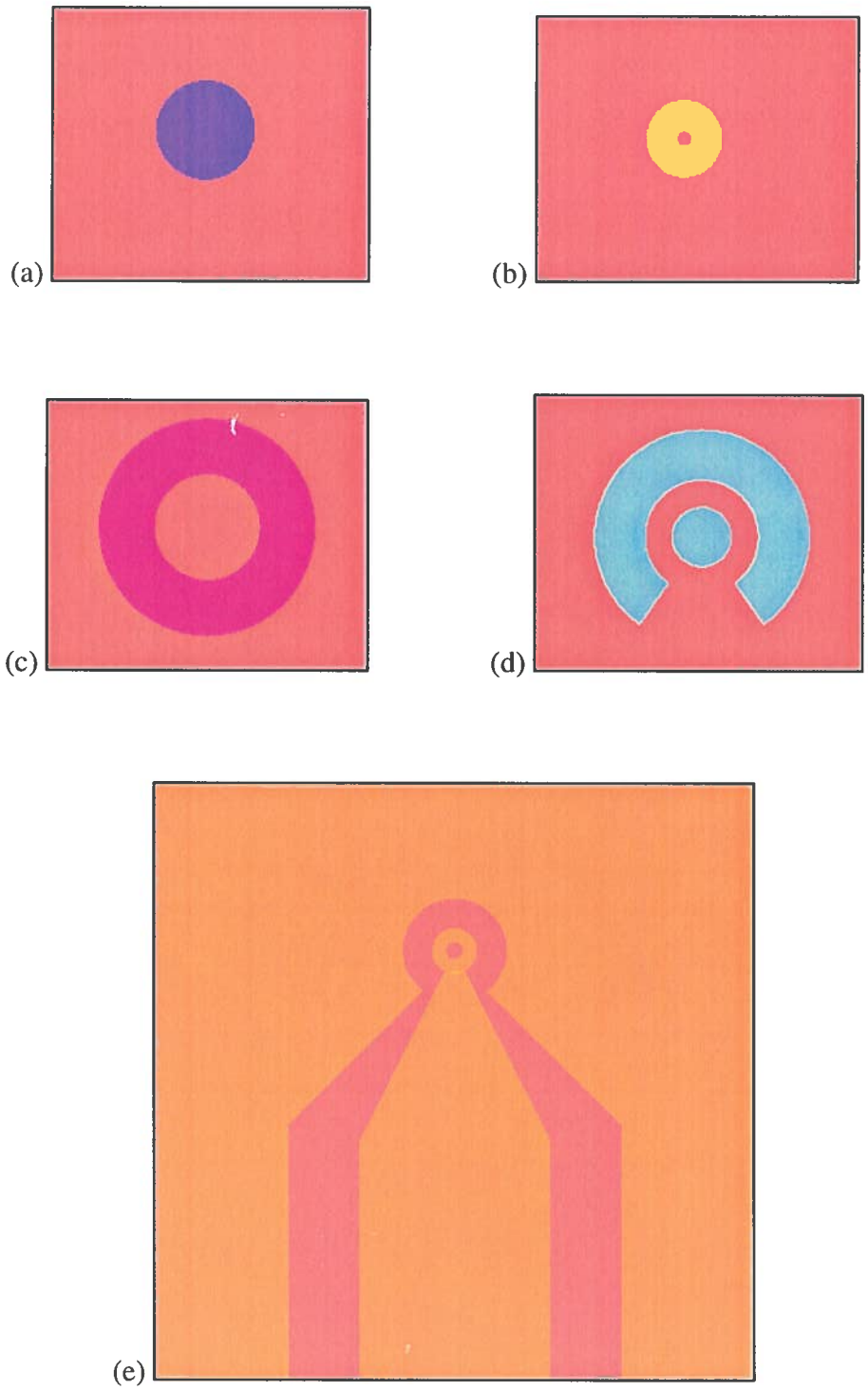
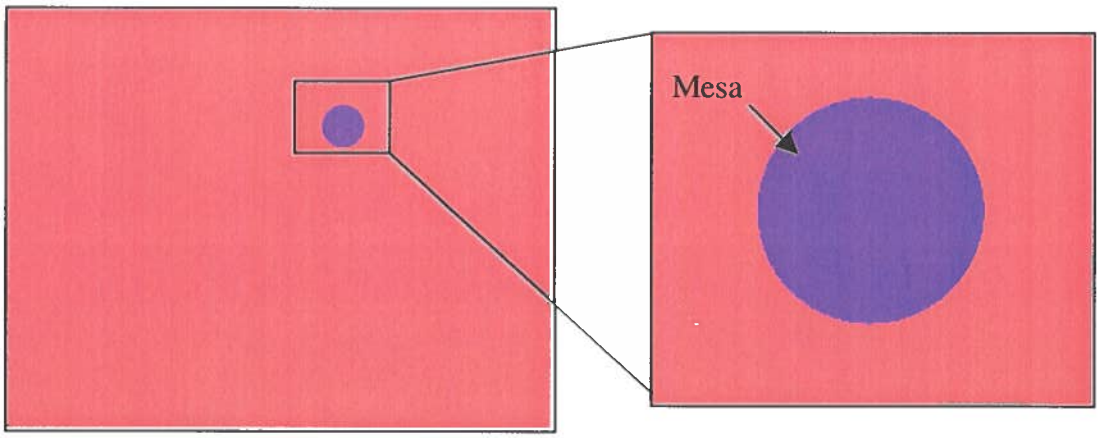
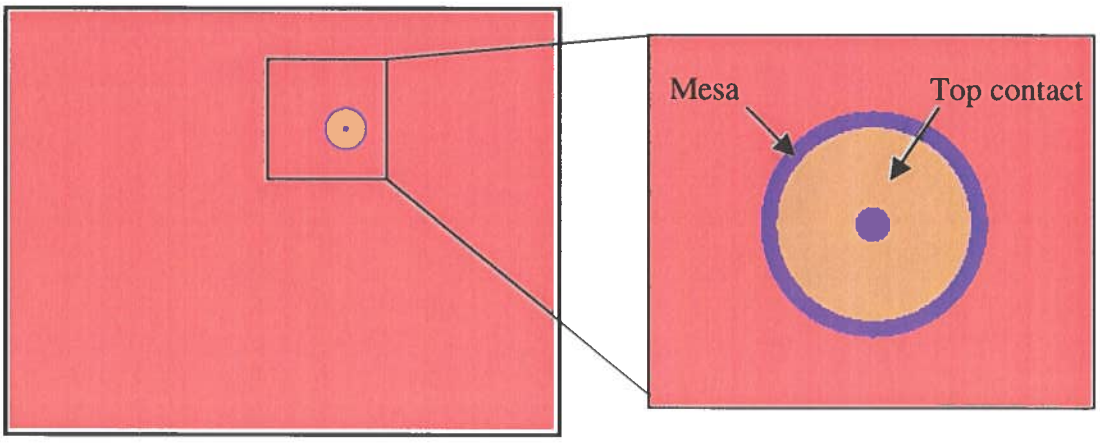


Figure 3.47 Photomasks for a VCSEL with 28μm diameter (a) Mesa, (b)Top contact, (c) Bottom contact, (d) Polyimide and (e) Metal interconnect

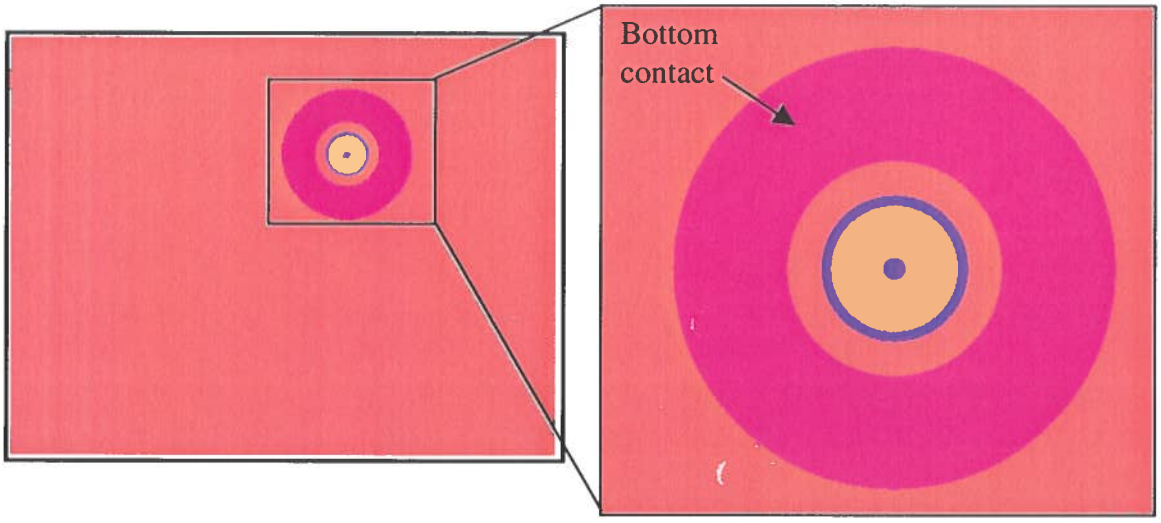


(1)

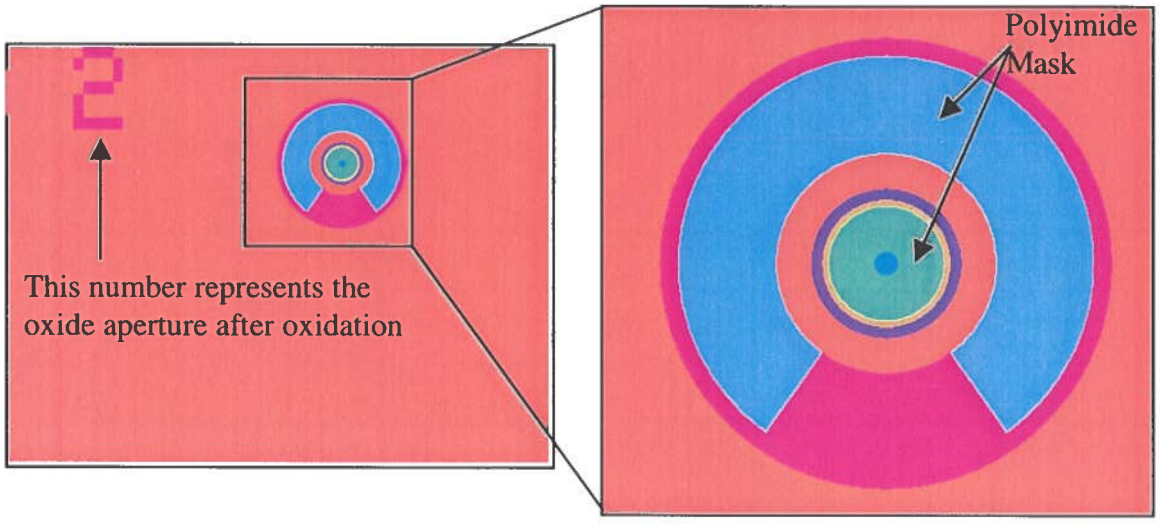


(2)

Figure 3.48.a (1) Mesa mask, (2) Top contact mask with mesa mask



(1)



(2)

Figure 3.48.b (1) Bottom contact, top contact and mesa masks, (2) Bottom contact, top contact, mesa and polyimide masks

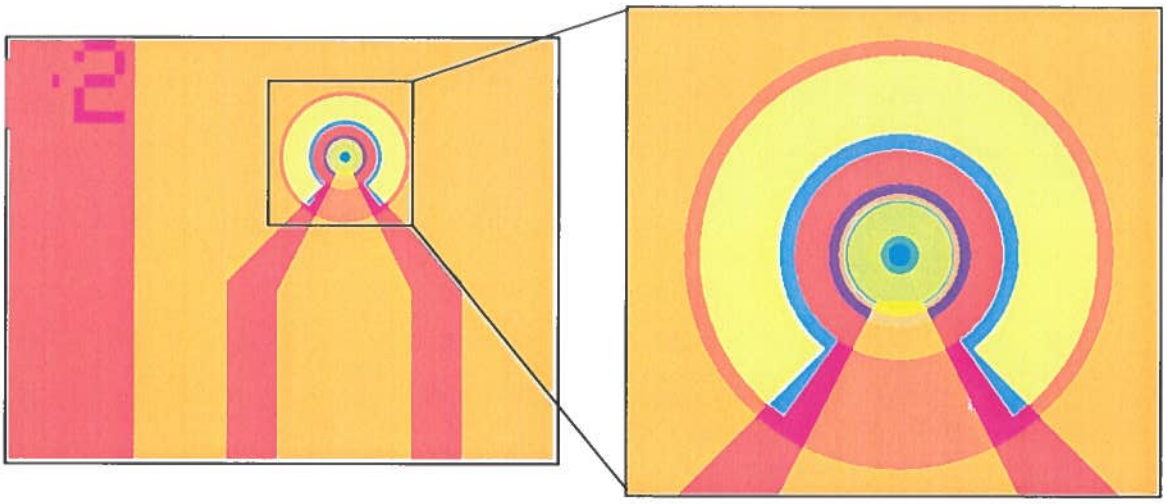


Figure 3.48.c Interconnect mask superimposed on all the masks

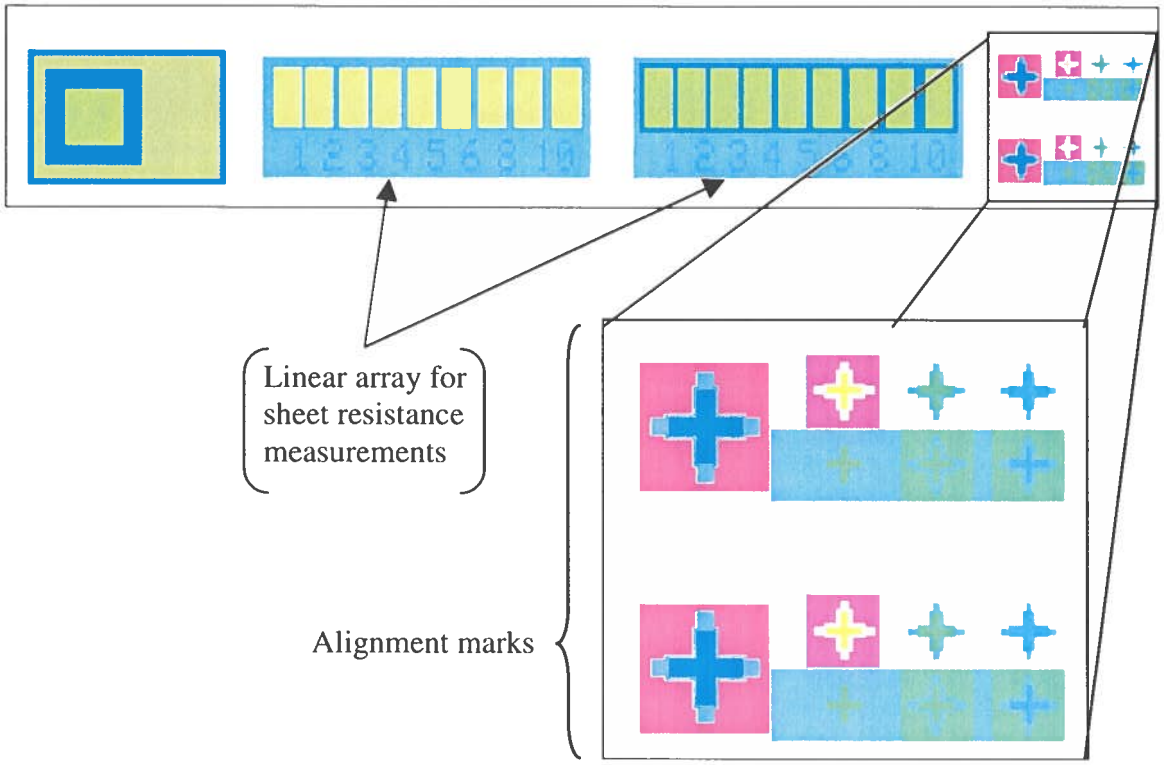


Figure 3.49 Linear array and alignment marks

3.5 Metal contact adhesion to HD-8000 polyimide

In general, polymers and metals do not adhere to each other very well. Many studies have been carried out to improve the adhesion quality between polymer and gold. Factors that affect the adhesion properties of metal and polymer are [23]: Surface morphology, diffusivity of metal atoms into the polymer layer, orientation of polymer chains and interaction sites of metal atoms and polymer group.

By looking at the binding energy Travaly's studies [23] show that there is no chemical interaction between gold and polyimide. To improve the adhesion between the polymer and gold, several groups have suggested using titanium, chromium, titanium, oxide or a combination of titanium and chromium as a glue layer between gold and polymer [19,23].

A GaAs sample (S9) was prepared to investigate the adhesion strength between Ti-Au and HD-8000 polyimide. The sample was processed as follows: First the sample was cleaned. Next, the HD-8000 polyimide was applied all over the sample and spun [Appendix D]. The sample was then baked at 115°C for about 100 seconds. Next, the sample was loaded into the polyimide curing furnace at 20°C, Then the temperature was ramped from 20°C to 350°C over a 60 minutes period *(Furnace setting ~240°C)*. After that, it was held at 350°C for 30 minutes *(Furnace setting ~240°C)*. Next, the sample was allowed to cool down. After the polyimide was cured, Ti-Au was evaporated with thicknesses of (200:3000) A, respectively, using beam evaporator.

The adhesion strength was tested using the scotch tape test. The scotch tape was placed on the surface of the sample and then pulled up. By investigating the surface of the GaAs as well as the scotch tape, it was concluded that both the Au and Ti stick to the

tape. As a result, the adhesion between the Ti and polyimide is weaker than that between the Ti and Au. Figure 3.50 is a top view of (S9). The brown area was covered with Ti-Au.

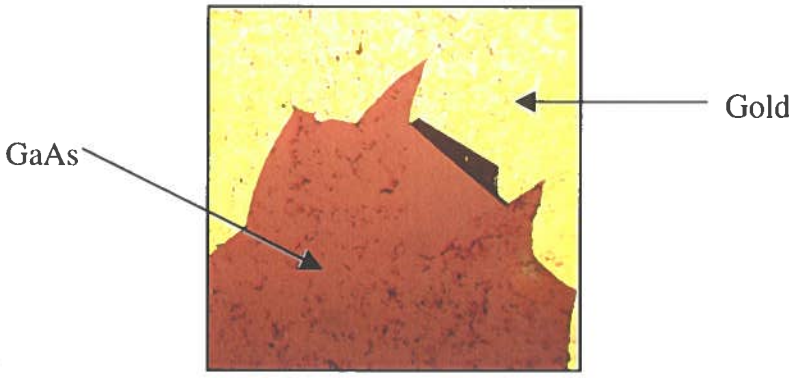


Figure 3.50 Gold on top of cured polyimide

A second approach was used to improve adhesion was to evaporate the Ti-Au metals on the polyimide before curing. Accordingly another sample was prepared (S10) [Appendix E]. However, this sample failed because it had a very poor surface profile, as shown in Figure 3.51 below. Such a profile was the result of polyimide contraction during curing, causing the metal layer to buckle up and the bubbles created by solvents being driven out of the polyimide under the metal layer.

Figure 3.51 Gold on top of cured polyimide

Next, four samples were prepared (S12, 13, 14, 15) as discussed in detail in [Appendix E]. After the metals were deposited, the samples were baked at 120°C for (1, 3, 6, 10) minutes, respectively using the hot plate (see [Appendix E] for details). Then the scotch tape test was carried out to test the adhesion strength. Figure 3.52 below represents images for the five samples after testing with scotch tape. It is clearly shown that the sample area covered with Ti-Au increases with increase of baking time that occurs after evaporation.

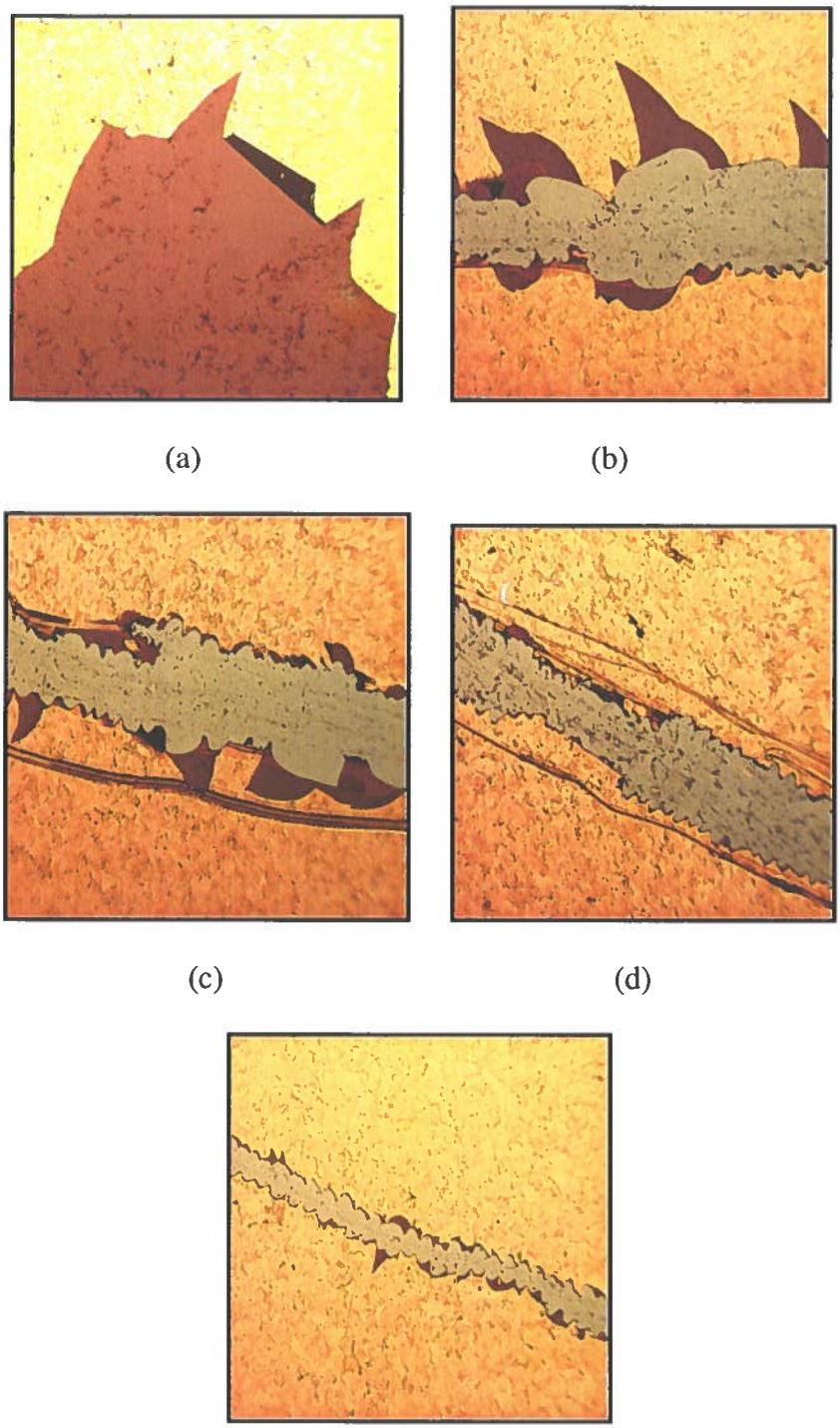


Figure 3.52 Images for all five samples after testing with scotch tape. It is clearly shown that the area covered with Ti-Au (dark area) increases with increasing the baking time that occurs after evaporation.

References:

[1] D. W. Pashley, "The Basics of Epitaxy" *in Growth and Characterisation of Semiconductors*, (Editors: R. A. Stradling and P. C. Klipstein; Publishers: Adam Hilger, New York), 1990, pp. 1–16.

[2] J. O. Williams, "Metal Organic Chemical Vapour Deposition (MOCVD) for the Preparation of Semicondutor Materials and Devices" *in Growth and Characterisation of Semiconductors*, (Editors: R. A. Stradling and P. C. Klipstein; Publishers: Adam Hilger, New York), 1990, pp. 17–33

[3] Ralph Williams, "Modern GaAs Processing Methods,"1990.

[4] Gred Keiser, "Optical Fiber Communications," Third Edition, 2000.

[5] H. Q. Hou, K. D. Choquette, et. al., "Highly uniform and reproducable visible to near-infrared vertical-cavity surface-emitting lasers grown by MOVPE", SPIE, Vol. 3003, 1997, pp. 34-45.

[6] http://www.mtheiss.com/index.htm.

[7] K. M. Geib, K. D. Choquette , et. al., "Fabrication issues of oxide-confined VCSELs", SPIE, Vol. 3003, 1997, pp. 69-74.

[8] Paul L. Gourley, Kevin L. Lear, et. al. , "Surface –emitting lasers", IEEE Spectrum, Vol. 31 , Number 8 , August 1994, pp. 31-37

[9] Kent D. Choquette, Kevin L. Lear, et. al., "Fabrication and Performance of Selectivily Oxidized Vertical–Cavity Lasers, " IEEE Photonics Tec. Letters, Vol. 7 , No 11 , Nov. 1995, pp. 1237-1239.

[10] Stephen J. Pearton, "Processing of Wide-Band Gap Semiconductors, " 2000.

[11] T. Batchelder and J. Piatt , *Solid State Technology*, 26(8), 1983, p. 211.

[12] www.microresist.de.

[13] A Brief Review by Sean Donovan "OHMIC CONTACTS TO LARGE BANDGAP COMPOUND SEMICONDUCTORS,"1998 http://www.mse.ufl.edu/~caber/.

[14] E. H. Rhoderick and R. H. Williams, "Metal-Semiconductor Contacts," Clarendon Press, Oxford, Second Edition, 1988.

[15] B. L. Sharma, "Ohmic Contacts to III-V Compund Semiconductors," Semiconductors and Semimetals, 15,1981, p.1.

[16] http://people.bu.edu/efs/recipes.htm.

[17] Kim, T.-J., "Evaluation of Interfacial Phases and Their Effects on Ohmic Contacts on n-GaAs in Ni-Ge-Ti Metalizations," , Ph.D. dissertation, University of Florida, 1996.

[18] http://www.epimbe.com.

[19] Hung Nguyen, Microwave and optical technology letters, 1997, 16, 2, pp. 66.

[20] Phillip E. Garrou, IEEE Transaction on advanced packing, 1999, 22, 3, pp. 487.

[21] www.hdmicrosystems.com.

[22] http://www.shipley.com/

[23] Y. Travaly, L. Zhang, J. Mater. Res., (1999),14, 9, pp. 3673.

[24] S. J. Rehse, A. D. Glueck, S. A. Lee, A. B. Goulakov , C. S. Menoni, D. C. Ralph, K. S. Johnson and M. Prentiss, " Nanolithography with metastable neon atoms: Enhanced rateof contamination resist formation for nanostructure fabrication," Appl. Phys. Lett. 71 (10) , 8 September 1997, p. 1427-1429.

CHAPTER 4

Testing and Characterization of High-Speed Vertical-Cavity Surface Emitting Laser

4.1 Overview

In this chapter, testing and characterization for high speed VCSELs will be discussed. Two phases of testing will be presented. The first is the DC characterization of VCSELs and the second is the AC characterization of VCSELs, taking into account the different VCSEL sizes.

4.2 DC Testing and characterization of VCSELs.

The DC characteristic of VCSELs, which includes I-V plots as well as photodiode current vs. VCSEL current plots for different VCSEL sizes, were measured. Furthermore, plots for thermal resistance and threshold current density for different mesa sizes were obtained.

4.2.1 Testing setup

To carry out the DC measurements, an equipment setup consisting of a Micromanipulator probe station with a constant temperature chuck, an Hp 4145A semiconductor parameter analyzer, and a silicon photodiode with a 10x10 mm^2 active area and ~0.6A/W responsivity for 850nm wavelength [1] were used.

Figure 4.1 shows the DC testing setup. Channels 1 and 2 from the semiconductor parameter analyzer were connected to the VCSEL pads to provide current and measure voltage. Channels 3 and 4 were connected to the photodiode to provide the DC reverse bias voltage and to enable the semiconductor parameter analyzer to measure the photodiode current. The VCSEL voltage and photodiode current were plotted as a function of the VCSEL bias current. The photodiode was aligned on top of the VCSEL

with a 1cm clearance so that most of the light from the VCSEL would hit the photodiode surface, while providing enough working space to make sure that the photodiode would not be damaged by hitting the probes.

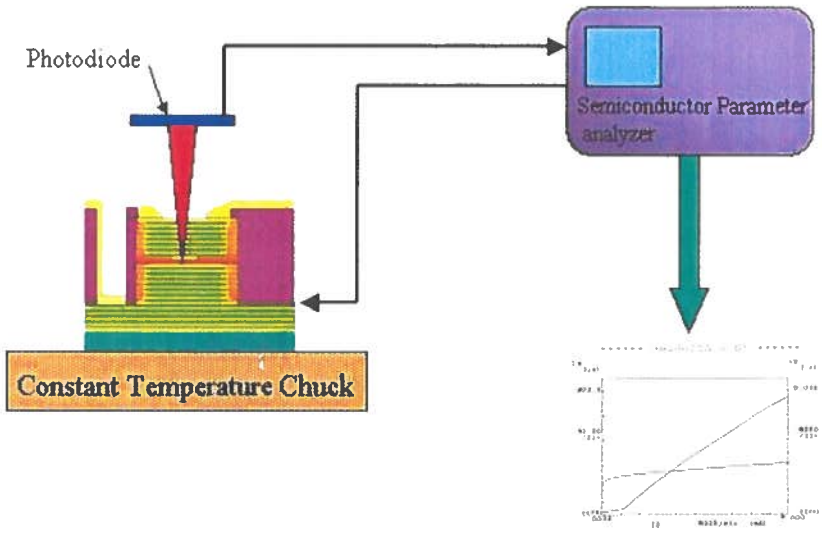


Figure 4.1 General drawing of the setup

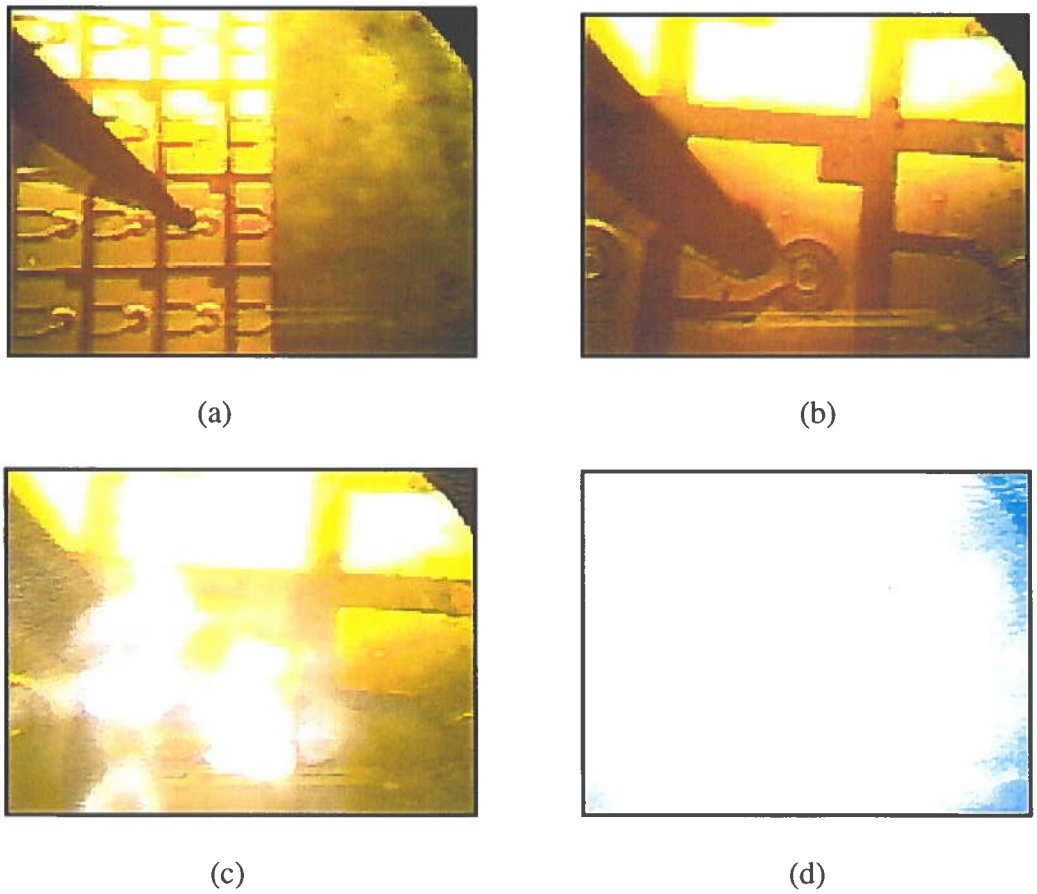
The semiconductor parameter analyzer was programmed to provide the VCSEL under test with the required DC voltage and to sweep the current up to ~$10I_{th}$. In fact, pushing the current significantly above $10I_{th}$ could result in damaging the VCSEL under test. It is therefore recommended to program the parameter analyzer to sweep the current in a small range first to get a feeling of the VCSEL I_{th}, and then the maximum limit for the applied bias current can be decided.

The VCSEL first worked as a LED when the applied current was less than I_{th}. Since there is only spontaneous emission in this current range, only a small photodiode current was measured (1-2 μA). As soon as the applied current reached the VCSEL I_{th}, the VCSEL began operating as a laser and the output light intensity was enough to

produce a current in the photodiode in the range of (0.5-1.0 mA), depending on the VCSEL output light intensity. Using a digital camera which was fixed on the probe station, it was possible to obtain some images for the VCSEL under test during the three biasing situations mentioned above.

4.2.2 DC testing results

All the plots that were obtained on the semiconductor parameter analyzer screen were plotted using an Hp 7574A plotter and then scanned into .bmp file format images that were subsequently digitized using Gragula software [2]. Both I-V curves and photodiode current vs. VCSEL current curves were measured for eight different mesa sizes at room temperature. Figure 4.2 below presents images for the VCSEL under test at bias currents of I~0 I_{th}, I~2I_{th}, and I ~ 10 I_{th}. In Figure 4.2, only one probe is shown and that is the top contact probe. No probe was used for the substrate contact since the backside of the sample was covered with gold. So the chuck was used as the substrate contact.



(a) (b)

(c) (d)

Figure 4.2: (a) VCSEL under test, (b) VCSEL at I~0 I_{th}, (c) VCSEL at I~2I_{th}, (d) VCSEL at I ~ 10 I_{th}.

The relationship between the photodiode current and the VCSEL bias current for a 28um mesa diameter with a 7um oxide aperture is presented in Figure 4.3 below. At low bias currents, $I<I_{th}$, the VCSEL will have spontaneous emission only and it will look like an LED with a broad spectral width and low output light intensity. As the bias current exceeds the threshold current, the spectral width becomes narrow and a sharp increase in photodiode current is observed due to the sharp increase in output light intensity.

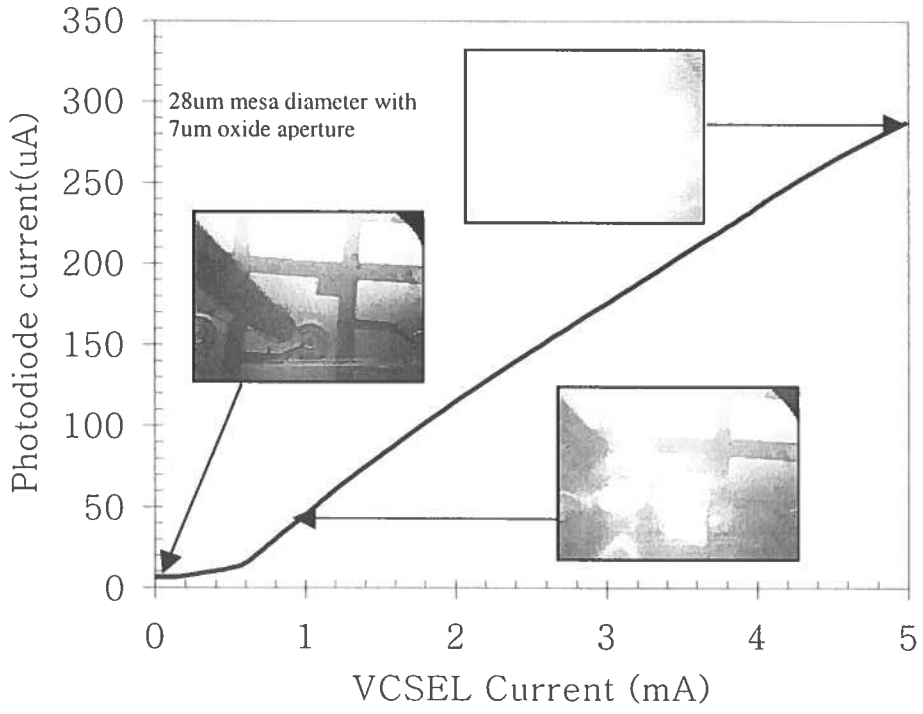


Figure 4.3 Photodiode current vs. VCSEL bias current for VCSEL under test. Below the threshold, the optical output is a spontaneous LED-type emission

Photodiode current, as well as VCSEL voltage over VCSEL bias current for different VCSEL diameters, were measured and plotted as shown in Figure 4.4 below.

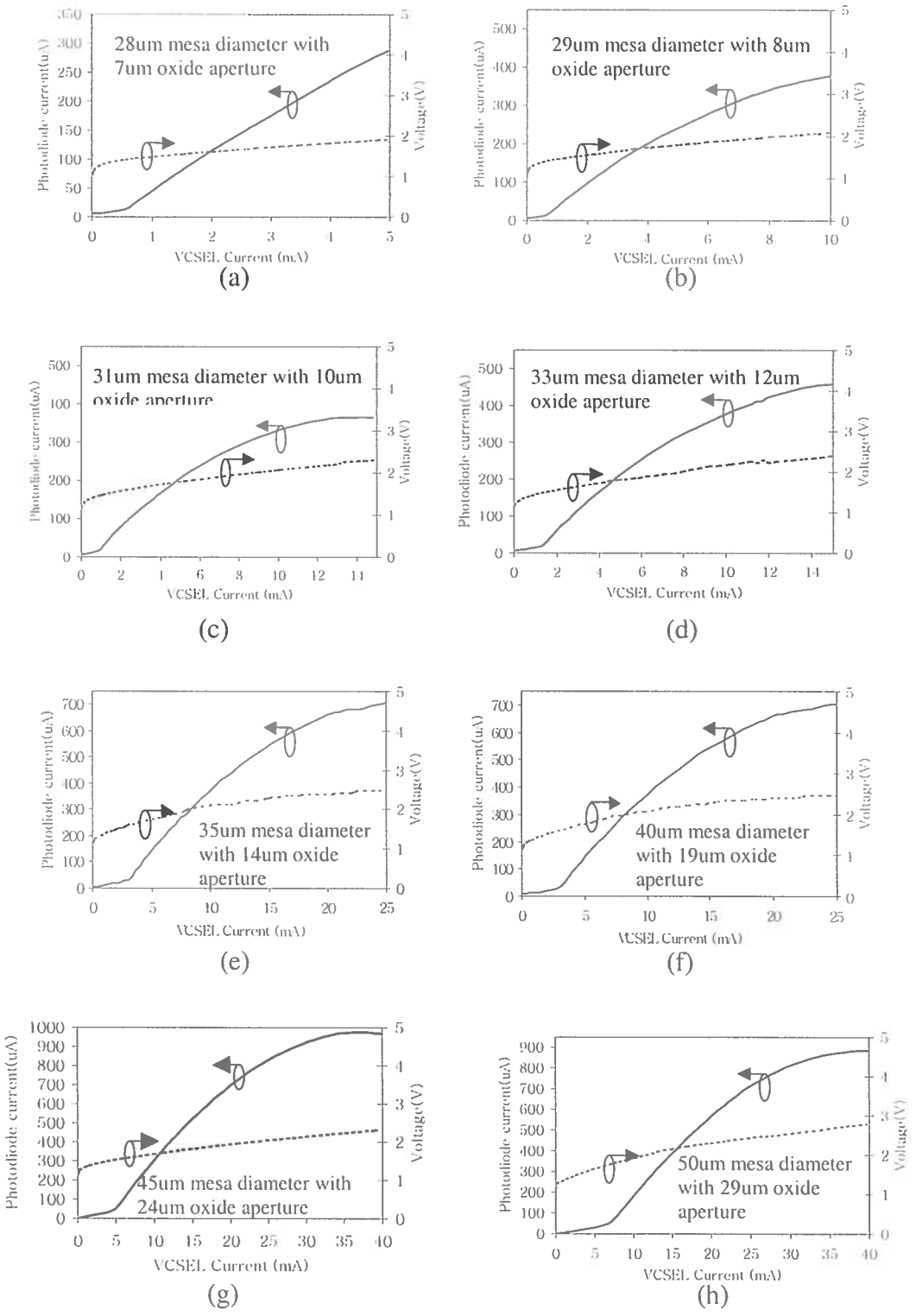
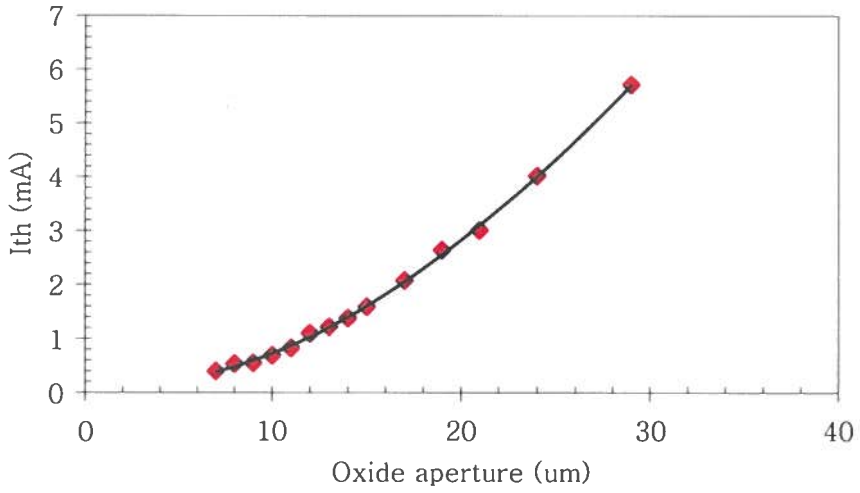
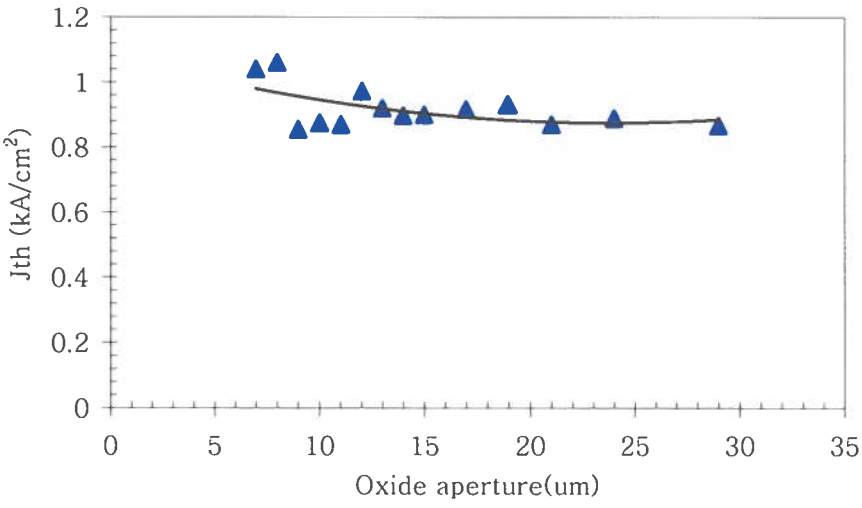


Figure 4.4 Photodiode current and VCSEL voltage over VCSEL bias current for different VCSEL diameters.

Threshold current was measured for 14 different VCSEL oxide apertures. As shown in Figure 4.5.a, it is clear that the threshold current increases as the oxide aperture diameter increases. Also, Figure 4.5.b illustrates the average threshold current density over different VCSEL oxide aperture diameters. The average threshold current density remains relatively constant at about 1kA/cm^2 over the range of oxide aperture diameters tested.



(a)



(b)

Figure 4.5: (a) Threshold current over different VCSEL oxide aperture diameters. (b) Current density different VCSEL oxide apertures

Uniformity was investigated by measuring the threshold current for different mesas having the same diameter and oxide aperture size located in different places on the sample. Table 4.1 below shows the different threshold currents measured for the same mesa size. Also, different oxide apertures were investigated, as shown in the table.

Oxide aperture (um)	I_{th} (mA)	Average I_{th} (mA)	Max. Percent variation
13	1.22	1.21	1.4%
	1.19		
	1.23		
14	1.38	1.42	6.1%
	1.51		
	1.38		
15	1.59	1.61	3.7%
	1.59		
	1.65		
17	2.08	2.17	2.9%
	2.23		
	2.19		
19	2.6	2.59	1.8%
	2.54		
	2.64		
21	3.01	3.04	5.3%
	2.91		
	3.2		
24	4.05	4.04	0.4%
	4.02		
	4.06		
29	5.82	5.88	3.6%
	5.72		
	6.09		

Table 4.1: Threshold currents measured for the same mesa (different oxide apertures were investigated)

As shown in the table above, the wafer shows good current uniformity over a 1 cm by 1 cm test sample. The highest maximum percent variation was about 6.1%, while the lowest was about 0.4%.

The differential resistances for the VCSELs were calculated from the measured I-V curves shown in Figure 4.4 simply by using the following equation;

$$R_d = \frac{\Delta V}{\Delta I} . \qquad (4.1)$$

Figure 4.6 below illustrates the relationship between the VCSEL differential resistance and its oxide aperture. It is clear from the plot that VCSELs with small oxide apertures will have larger differential resistances than those of large oxide aperture VCSELs.

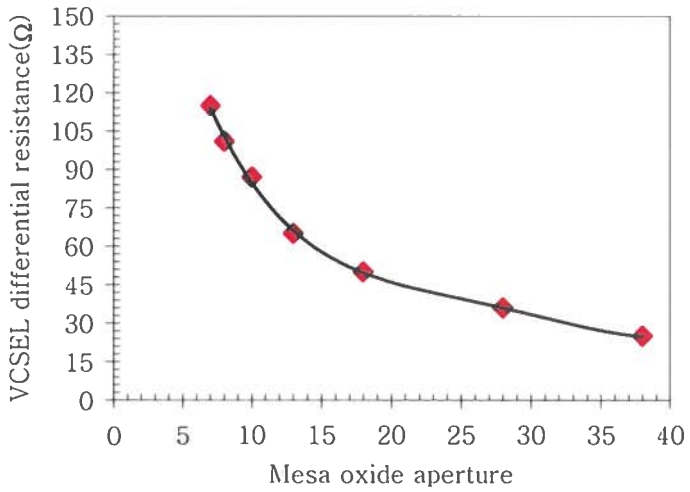


Figure 4.6 VCSEL differential resistance vs oxide aperture

VCSEL heating stability is an important issue and worth some discussion. Heat in a VCSEL will cause what is called thermal wavelength shift, due to the change in the refractive index of the resonator and the thermal expansion of the semiconductor mirrors. Also, VCSEL heating will cause the optical gain peak to decrease as the VCSEL heats up. Heating in the VCSEL can be described by the VCSEL thermal resistance, R_{th}, which is used to quantify how easily heat power flows out of the VCSEL toward the heat sink. Thermal resistance is defined as the ratio of VCSEL temperature rise ΔT and dissipated

electrical power P_d. Assuming that heat flows from a circular area with a diameter $2a$ into a relatively thick substrate of thermal conductivity ξ, the thermal resistance follows the simple relation [4], [5],

$$R_{th} = \frac{1}{4\xi \cdot a} \quad . \tag{4.2}$$

A plot of equation 4.2 for different oxide apertures with $\xi = 0.45W/cm \cdot C.$ for GaAs [5] is shown in Figure 4.7 below.

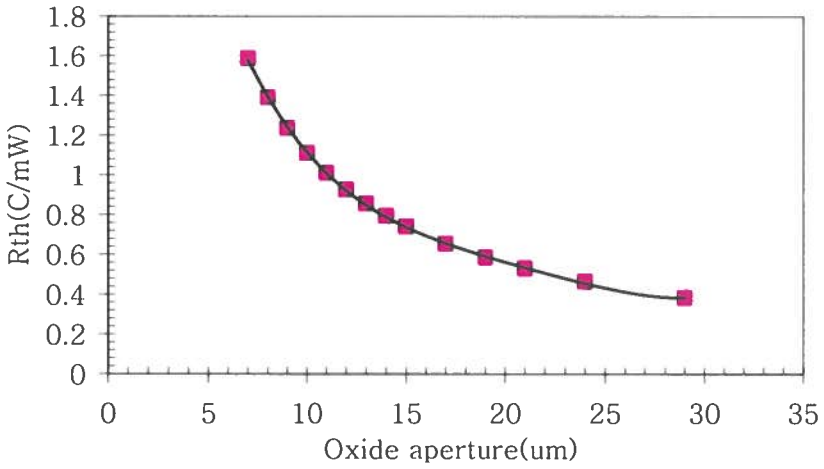


Figure 4.7 Thermal resistance (R_{th}) as a function of the VCSEL oxide aperture

For uniform current injection in to the active area, the temperature rise at lasing threshold is expressed as

$$\Delta T = R_{th} \cdot P_d = R_{th} \cdot V_{th} \cdot i_{th} \quad , \tag{4.3}$$

where $i_{th} = j_{th} \cdot \pi a^2$. Substituting an i_{th} expression and R_{th} from equation 4.2, we get that the temperature rise at lasing threshold is expressed as

$$\Delta T = \frac{\pi a}{4\xi} \cdot V_{th} \cdot j_{th} \quad . \tag{4.4}$$

Using the measured values for threshold voltage V_{th} and threshold current density j_{th} along with equation 4.4, ΔT was calculated and plotted as shown in Figure 4.8 below:

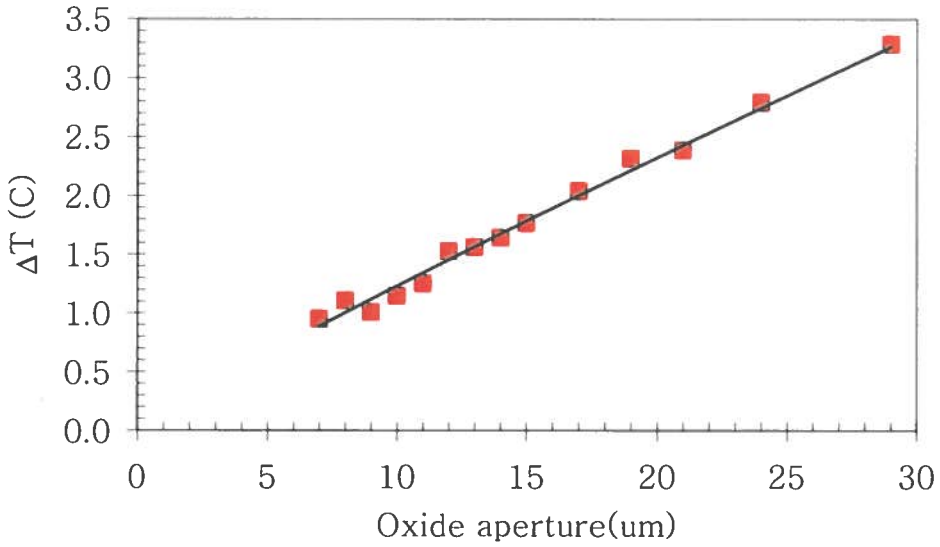


Figure 4.8 Temperature rise at lasing threshold as a function of VCSEL oxide aperture

The roll-over current at which the output power from the VCSEL begins to decrease while increasing the VCSEL bias current was measured for different mesa diameters. Table 4.2 below represents the measured roll-over currents for different VCSEL diameters. Figure 4.9 below illustrates the relationship between the $I_{rollover}/I_{th}$ and the oxide aperture.

Ith(mA)	$I_{roll\text{-}over}$ (mA)	Oxide aperture (μm)
0.4	8	7
0.532	12	8
0.688	14	10
1.1	17	12
1.38	20	14
2.64	25	19
4.02	35	24
5.72	40	29

Table 4.2

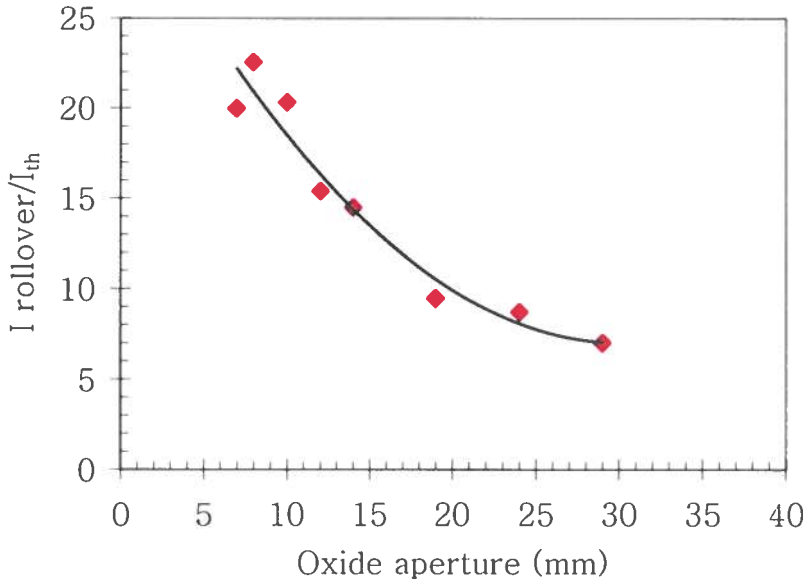


Figure 4.9 the $I_{rollover}/I_{th}$ vs. VCSEL oxide aperture

It is clear from Figure 4.9 above that the output power of VCSELs with large oxide apertures tends to roll-over earlier than that of small oxide aperture VCSELs. In our research, we were able to fabricate a VCSEL with a mesa diameter of 28 μm and an oxide aperture of 7.0μm that withstands a bias current up to $20I_{th}$ before its output power begins to roll-over.

A VCSEL with a mesa diameter of 50μm and an oxide aperture of 29μm was fabricated. This large-size VCSEL was able to endure only $7.0I_{th}$ bias current before its output power began to roll-over. It was concluded from the AC experimental results, which will be discussed later in this chapter, that the VCSEL modulation frequency increases as the bias current to threshold current ratio increases. As a result, smaller VCSELs will survive higher bias currents ratios and will result in higher modulation frequencies.

It is clear from the plots discussed above that VCSEL heating is affected by the oxide aperture, which makes the oxidation step a critical one in deciding VCSEL temperature stability and maximum output power. Under-oxidized VCSELs will increase the oxide aperture, causing the VCSEL temperature to rise, which means that the output power of the VCSEL will saturate early. Furthermore, the temperature rise at threshold in large VCSELs is greater than that in small VCSELs.

As Figure 4.10 below demonstrates, as the bias current increases above the VCSEL threshold current, the ΔT increases, and as a result the optical output power characteristic rolls-over.

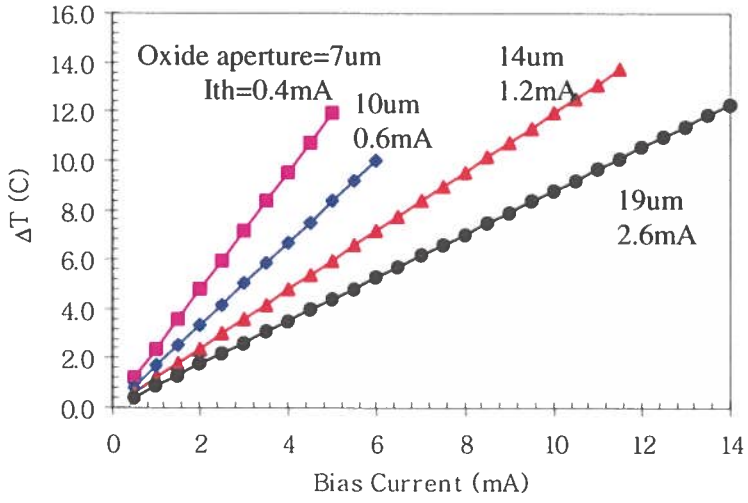


Figure 4.10 Calculated temperature rise ΔT as a function of the VCSEL bias current

A comparison can be made between our VCSEL thermal resistances and that of other VCSELs reported by others. The VCSEL that once held the record of output power efficiency has R_{th} = 2.5 C/mW for a VCSEL with 7-μm active area [6] , and the inter-cavity contacted VCSEL, also with a 7-μm diameter aperture, has R_{th} =2.65 C/mW [7]. The plot from Figure 4.6 shows that R_{th} for our VCSELs at 7-μm diameter aperture is 1.6 C/mW, based on the model implicit in equation 4.2, Since there were some approximations and assumptions in deriving equation 4.2 this means that our calculated R_{th} is about 40% lower than the thermal resistance reported in [6], [7]. Table 4.3 below represents a comparison between three VCSEL thermal impedances.

Sample	R_{th} (C/mW)
[6]	2.50
[7]	2.65
our sample	1.60

Table 4.3

In summary, we have calculated the thermal resistance of our VCSEL and shown that its thermal resistance is comparable to the thermal resistance reported in [6], [7].

An important issue to deliberate in the application of VCSELs is temperature dependence of threshold current $I_{th}(T)$. This parameter increases with temperature in all types of semiconductor lasers due to various complicated temperature-dependent aspects [11]. The complexity of these factors averts the formulation of a single equation that holds for all devices and temperature ranges.

To investigate the temperature effect on VCSEL threshold current, the sample was placed on a thermoelectric cooler. The photodiode current over the VCSEL bias current was then measured and plotted. The thermoelectric cooler was on for about five minutes

before measurements were taken. The VCSEL under test has a 50μm diameter with a 29μm oxide aperture. Figure 4.11 below demonstrates the two curves

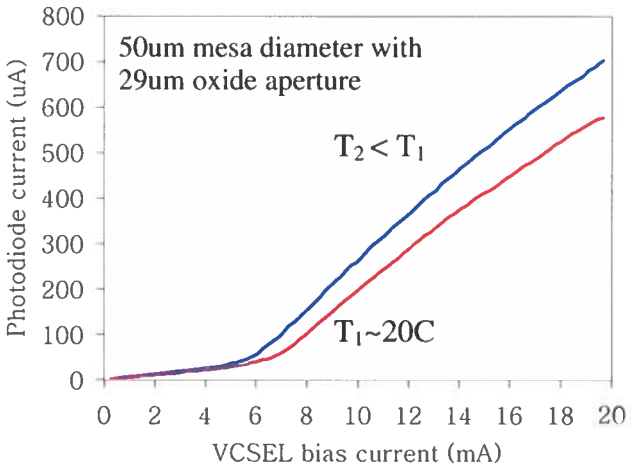


Figure 4.11: Photodiode current vs. VCSEL bias current at T_1 and T_2, where at $T_1 > T_2$

4.3 AC Testing and characterization of VCSELs

The modulation response of VCSELs with a range of diameters was measured for varying bias currents. Also S_{11}, the electrical reflection coefficient commonly used parameter for determining device input impedance, was measured at microwave frequencies.

4.3.1 Testing setup

Because of the need for specialized microwave equipment including a vector network analyzer, AC measurements were carried out at Cielo Communications, Inc.. These measurements were carried out by Dr. David Galt, a device characterization engineer at Ceilo [8]. The test apparatus consisted of a probe station equipped with a constant temperature chuck and Cascade Microtech air co-planar probes, 1-2 meters of multimode fiber, a high-speed New Focus photodiode and attached New Focus amplifier, a HP 4145 semiconductor parameter analyzer, and a HP8510B vector network analyzer. Figure 4.12 on the next page gives a schematic illustration of the AC testing setup. The semiconductor parameter analyzer operation is similar to that described in Section 4.2.1. The sample was mounted on the constant temperature chuck at 20C and was aligned so that the output light would be collected by the fiber. The active alignment was done by biasing the VCSEL above threshold and adjusting the position of the fiber tip using an x-y-z positioning stage until the DC optical power in the fiber was maximized. The fiber was probably within 0.1 mm or less of the sample.

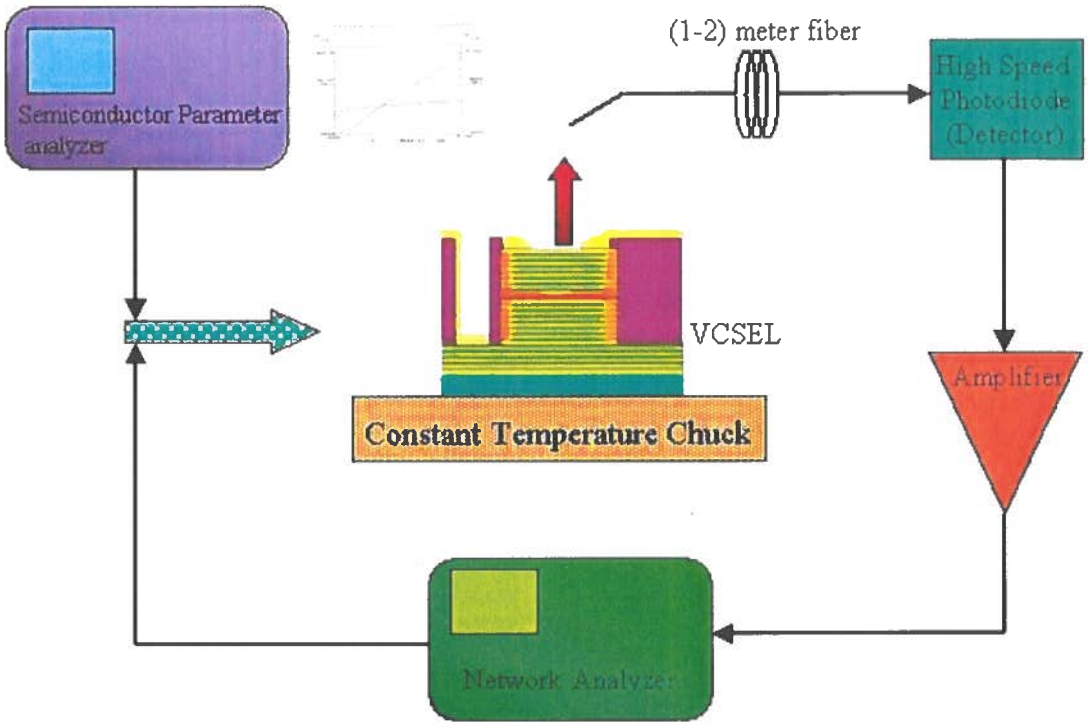


Figure 4.12 Experimental setup for AC measurements prepared at Cielo Communications, Inc.

The output light was collected by the fiber and guided to an optical high-speed photodiode. The electrical AC signal from the photodiode was amplified and input to the network analyzer.

The modulation response of different diameter VCSELs for various bias currents was measured. The magnitude and phase of the system response, S_{21}, as well as the laser reflection, S_{11}, were measured at microwave frequencies over a range of 100MHz to 26.5 GHz. The modulation response of a small VCSEL with a -0.4mA threshold current, 28μm diameter, and an oxide aperture of 7μm, was measured as a function of the bias current using the setup shown in Figure 4.12. It was presumed that this laser operated in a single mode for some range of currents near threshold. The maximum bandwidth at -3dB from the low frequency response was approximately 17.0 GHz, as shown in Figure

4.13.a. The modulation response for the same VCSEL at different bias currents is shown in Figure 4.13.b.

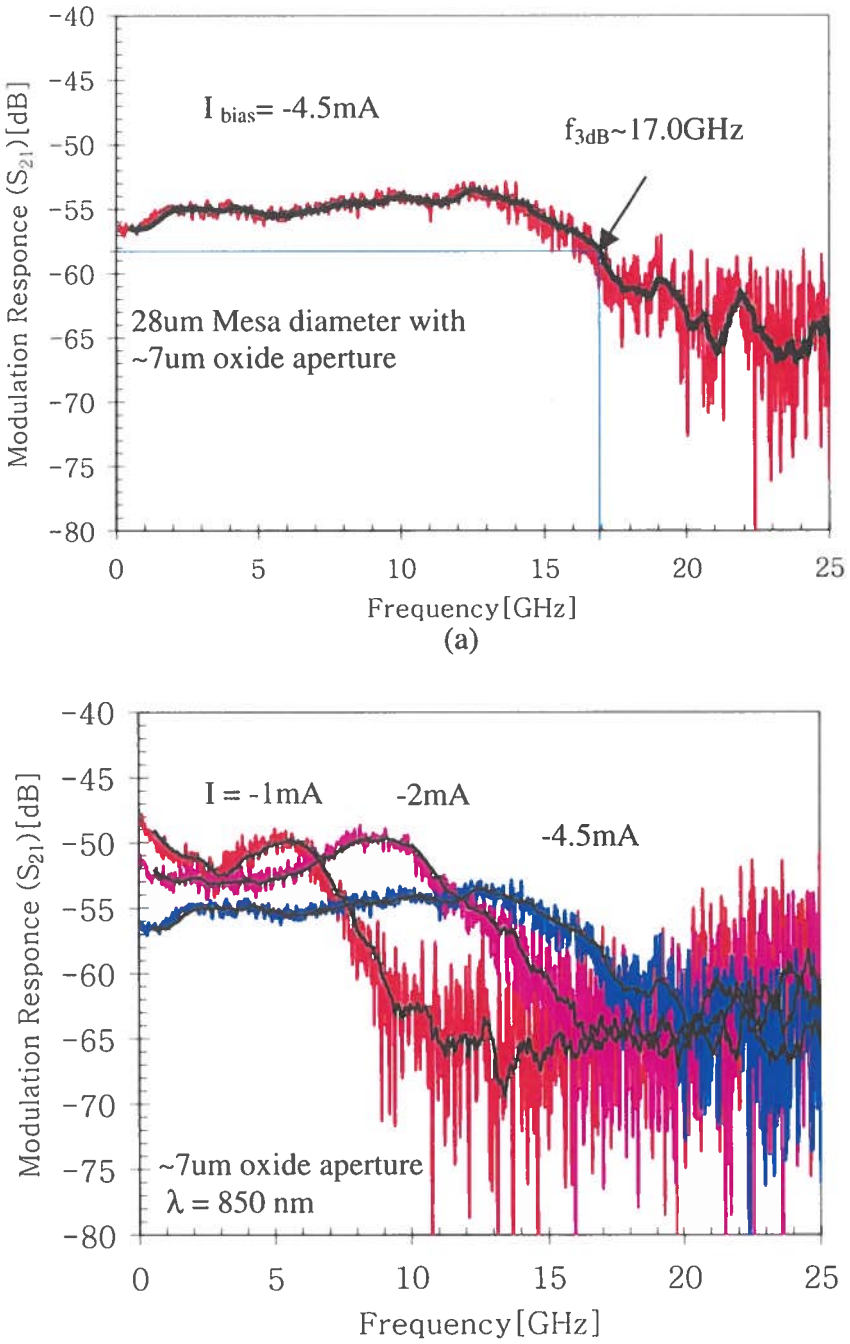


Figure 4.13: (a) The modulation response of a small VCSEL at –4.5 biases current, (b) the modulation response of the small VCSEL at various bias currents

It is apparent from Figure 4.13 that as the bias current increases the -3dB modulation frequency also increases. Figure 4.14 below illustrates the effect of increasing the bias current on the modulation -3dB bandwidth at room temperature for our fabricated VCSELs. The solid line shown in Figure 4.14 is a theoretical fitting curve based on the theory of how the modulation bandwidth should increase as the bias current increases. The modulation frequency depends on both the spontaneous lifetime and photon lifetime. Theoretically, assuming a linear dependence of the optical gain on carrier density, the modulation frequency occurs at [11]

$$f_{-3dB} = a\sqrt{\left[\frac{I}{I_{th}} - 1\right]} . \qquad (4.5)$$

Equation 4.5 was used to plot the theoretical fitting curve,

where: a is a fitting parameter given by equation 4.6:

$$a = \left[\frac{1}{2\pi\sqrt{\tau_{sp}\tau_{ph}}}\right]. \qquad (4.6)$$

τ_{sp} : carrier spontaneous lifetime

τ_{ph} : photon lifetime

The value of a that best fits our measured data was determined using the MathCAD built-in fitting function genfit.

First, the data to be fitted was entered as vectors I_{bias} in mA and f_{-3dB} in GHz, as shown below:

$$I_{bias} = \begin{bmatrix} 1.0 \\ 1.5 \\ 2.0 \\ 2.5 \\ 3.0 \\ 3.5 \\ 4.0 \\ 4.5 \\ 5.0 \end{bmatrix} \qquad f_{-3dB} = \begin{bmatrix} 6.5 \\ 9.7 \\ 11.5 \\ 13.0 \\ 14.4 \\ 15.8 \\ 16.8 \\ 17.0 \\ 17.0 \end{bmatrix}$$

The function F that is shown in equation 4.7 below was defined as a function that consists of a 2-element vector containing the f_{-3dB} function, shown in equation 4.5, and its partial derivative with respect to the fitting parameter a:

$$F(I,a) = \begin{bmatrix} a\sqrt{\frac{I}{I_{th}} - 1} \\ \sqrt{\frac{I}{I_{th}} - 1} \end{bmatrix} . \qquad (4.7)$$

After that, a guessing value (a_g) for the fitting parameter, was defined, such that

$a_g = 5.0 \times 10^9$.

a was then defined as follows:

$a = genfit(I_{bias}, f_{-3dB}, a_g, F)$.

The fitting value that was calculated by MathCAD which best fit our measured data was

$a = 5.47 \times 10^9 \text{ sec}^{-1}$.

As predicted, our measured modulation frequency at different bias currents follows the theoretical expectation for $I_{bias} \leq 10 I_{th}$. After that, our modulation frequency tends to saturate with further increase in the bias current, as shown in Figure 4.14 below.

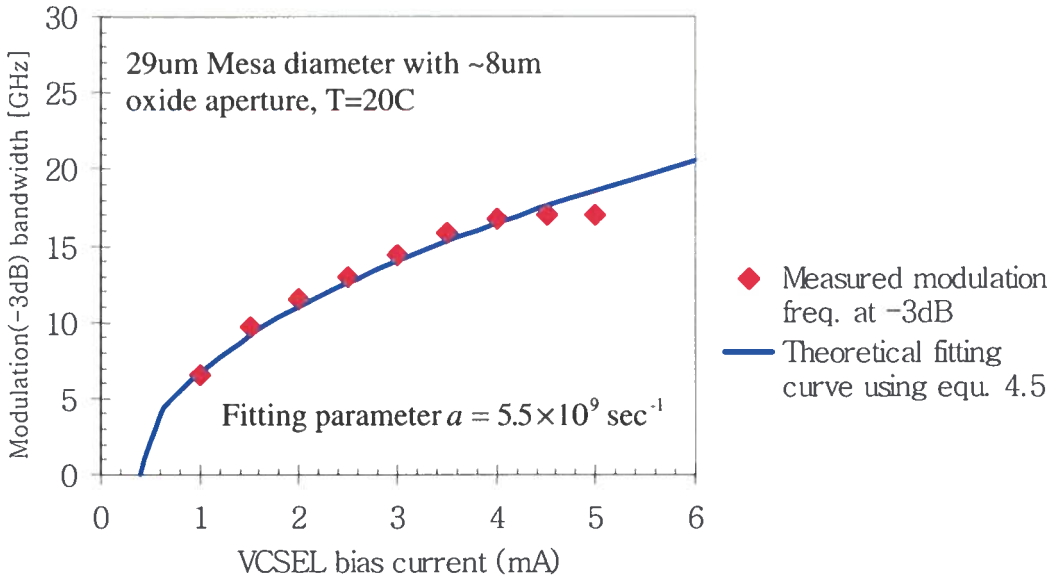
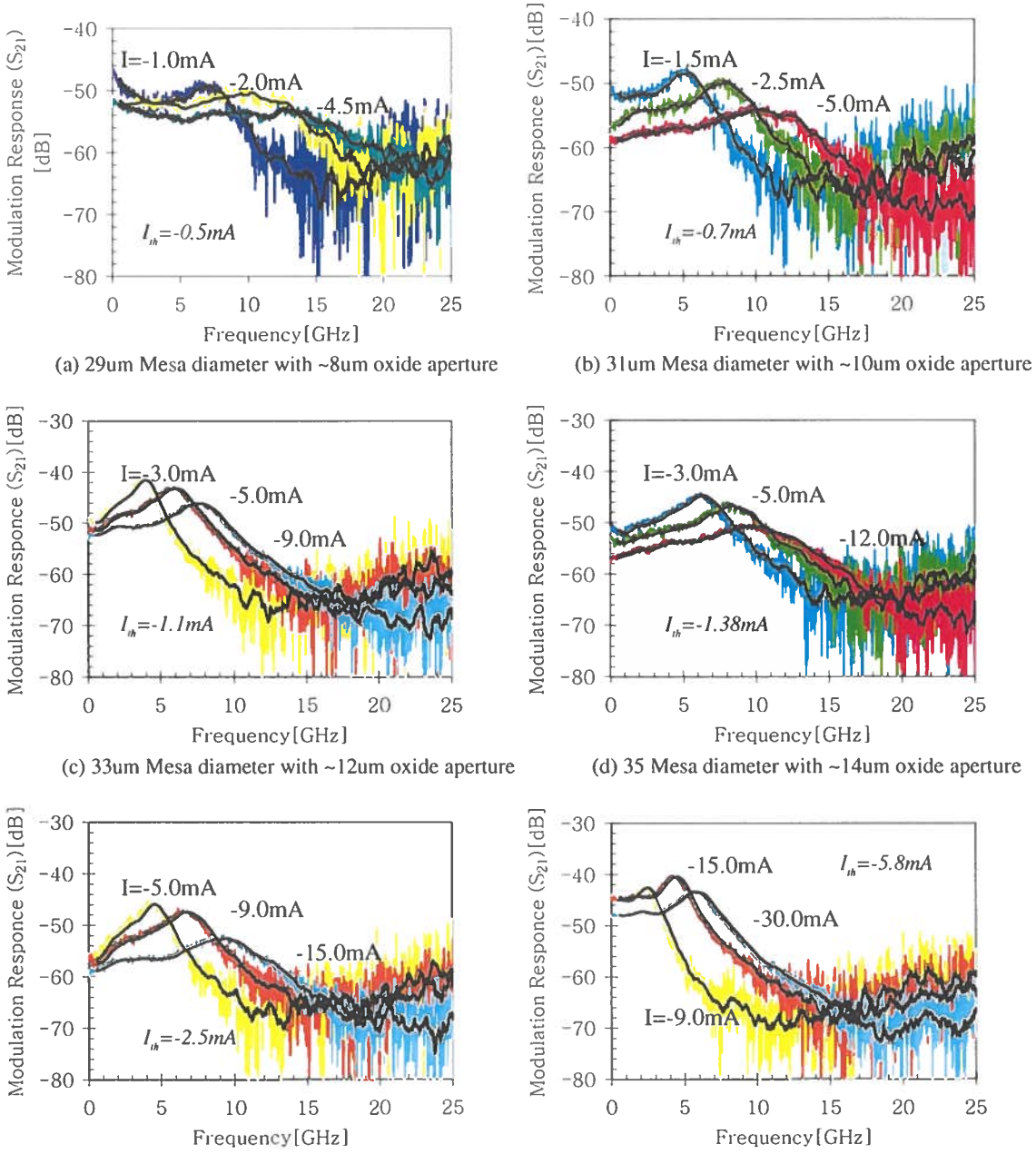


Figure 4.14 VCSEL bandwidth vs. Bias current at room temperature

The measurements that were performed on the 28um mesa diameter with ~7um oxide aperture were repeated for (29, 31, 33, 35, 40, 50) μm mesa diameters with (8, 10, 12, 14, 19, 29) μm oxide apertures, respectively. These results are shown below in Figure 4.15.



(a) 29um Mesa diameter with ~8um oxide aperture

(b) 31um Mesa diameter with ~10um oxide aperture

(c) 33um Mesa diameter with ~12um oxide aperture

(d) 35 Mesa diameter with ~14um oxide aperture

(e) 40um Mesa diameter with ~19um oxide aperture

(f) 50 Mesa diameter with ~29um oxide aperture

Figure 4.15 The modulation response of different VCSELs sizes at various bias currents

Figure 4.16 below illustrates the relationship between the –3dB modulation frequency and the VCSEL oxide aperture. All the –3dB frequencies were measured when the bias current (I_{bias}) was ten times the threshold current (I_{th}) for each individual VCSEL. It is clear from the plot that smaller VCSELs will result in higher modulation frequencies than those for large VCSELs. The explanation for this type of a relationship was discussed earlier in Chapter 2

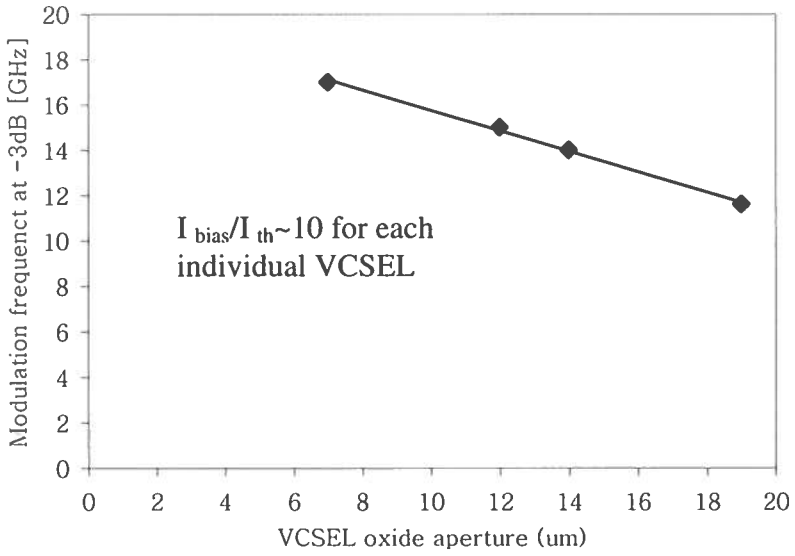


Figure 4.16 Modulation frequency vs. VCSEL oxide aperture for different mesa sizes

4.3.2 VCSEL impedance (S_{11} parameters)

A suitable approach for determining the electrical equivalent circuit of a VCSEL is to use S parameter measurements made with a vector network analyzer. In fact, it is the only one that can be used for this. The S parameter used for measuring impedance is S_{11}, which is the reflection coefficient of the sample's complex impedance, Z, referenced to 50 ohms [9]. The S_{11} parameter and the impedance under test are related by:

$$S_{11} = \frac{Z - 50\Omega}{Z + 50\Omega} . \qquad (4.8)$$

Extracting an electrical circuit model from the measurements shown in Figure 4.17, as well as the S_{11} data measurements for different VCSEL sizes, will be discussed in more detail in Chapter 5.

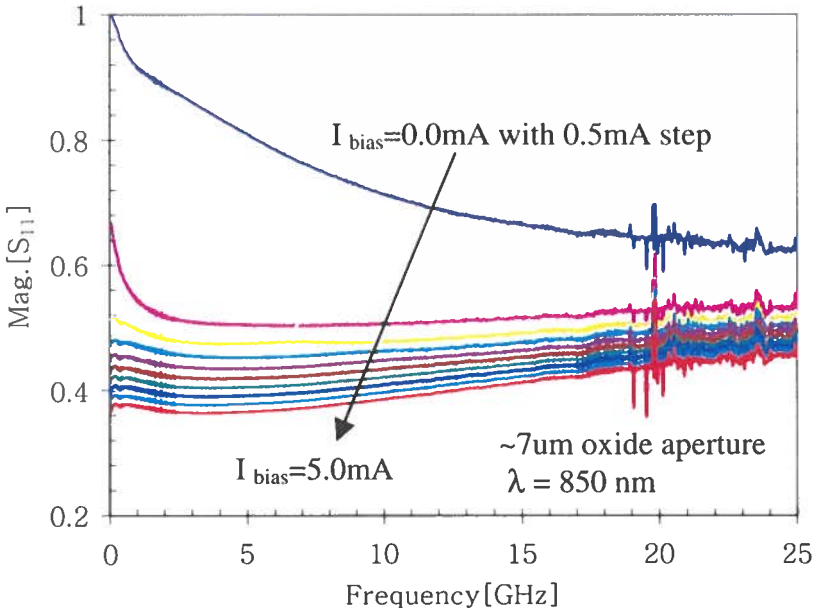


Figure 4.17 (a) S_{11} magnitude vs. frequency, (b) S_{11} phase vs. frequency. Both plots will be used in Chapter 5 to extract the VCSEL equivalent circuit

In the next chapter, modeling and simulation of high-speed VCSELs will be discussed, including the presentation of an electrical model for the VCSEL using the S_{11} parameter data that were discussed earlier in this chapter and a fitting technique. A SPICE simulation of the suggested electrical model for different mesa sizes will be shown, and a comparison is made between the testing and simulation results.

References:

[1] Thorlabs data sheet for item # FDS1010 (http://www.thorolabs.com)

[2] Gragula software website http://home.comset.net/wesik/grafula3/grafula3.htm.

[3] A. Miller, M. Ebrahimzadeh, D. M. Finlayson, "Semiconductor Quantum Optoelectronics," 1999.

[4] L. A. Coldern and S.W. Corzine, diode lasers and photonic integrated circuits, Wily series in Microwave and optical engineering, 1995.

[5] Michael H. , Jon Geske , et. al., "Thermal Impedance of VCSEL's with AlO_x – GaAs DBR's," IEEE Photon. Tech. Lett., Vol. 8, No. 1 , pp 15-17, Jan. 1998/

[6] K.L. Lear, K. D. Choquette, et. al.," Selectively oxidized vertical cavity surface emitting lasers with 50% power conversion efficiency," Electron. Lett. Vol. 31, pp. 208-209 , 1995.

[7] J. W. Scott, "Design, fabrication and characterization of high-speed inter-cavity contacted vertical-cavity lasers," Ph.D. dissertation, University of California at Santa Barbara.

[8] http://www.cieloinc.com/.

[9] Fiberoptic product news .6.2000.

[10] www.honeywell.com.

[11] Gerd Keiser, "Optical Fiber Communication," Third Edition, 2000.

CHAPTER 5

Modeling and Simulation of High-Speed Oxide-Confined Vertical Cavity Surface Emitting Lasers

5.1 Modeling

Vertical-Cavity Surface-Emitting Lasers are the most promising light source for fast and dense parallel optical interconnect solutions. In order to facilitate the design of such advanced datacom systems, including both electrical and optical components, an appropriate VCSEL model for system-oriented simulations must be developed. Modeling also enhances our understanding of important device issues and how parameter changes will affect the overall device function.

Figure 5.1 below illustrates a schematic cross-section of high speed VCSEL structure with the corresponding equivalent circuit [11]. C_a representing the junction capacitance and the aluminum oxide capacitance (Al_2O_3), R_a corresponding to the junction resistance. R_s stand for the top n-mirror stack resistance, which is between the active area and contact. C_p represents the capacitance between the interconnect and the bottom p-mirror stack. R_p is the resistance of the unetched bottom p-mirror stack.

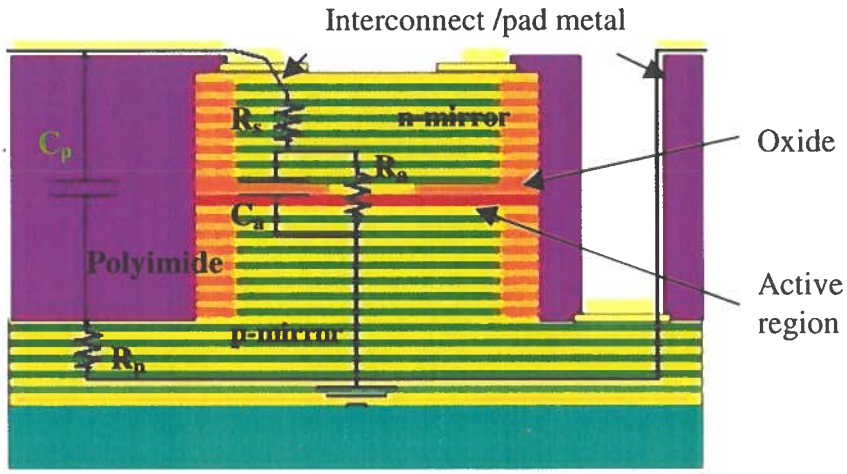


Figure 5.1 A cross section of high speed VCSEL with superimposed equivalent circuit (Reproduced after [11])

To obtain the values for all the VCSEL equivalent circuit parameters C_a, R_a, R_s, C_p and R_p, the measured S_{11} reflection coefficient parameter data was used.

First, the VCSEL impedance was obtained at zero bias current, since the active area resistance R_a can be assumed to be infinite when the p-n junction is not biased, which will reduce the number of unknown elements in the VCSEL equivalent circuit. As a result, the VCSEL equivalent circuit is reduced, as shown figure 5.2 below.

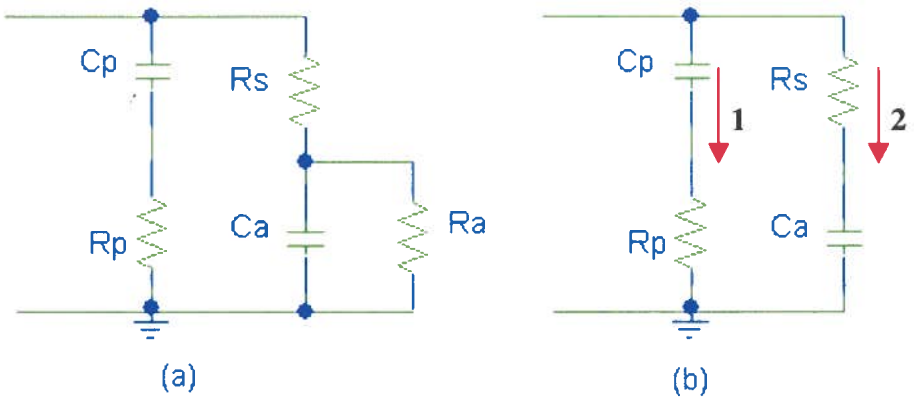


Figure 5.2 VCSEL equivalent circuit (a) $I_{bias}>0$ (b) $I_{bias}=0$

The VCSEL total impedance Z_T at zero bias is simply the parallel combination of branches 1 and 2 shown in Figure 5.2.b.

$$Z_1 = R_p - \frac{j}{2\pi f C_p} \qquad (5.1.a)$$

$$Z_2 = R_s - \frac{j}{2\pi f C_a} \qquad (5.1.b)$$

$$Z_T = \frac{Z_1 Z_2}{Z_1 + Z_2} \quad . \qquad (5.2)$$

The S_{11} reflection coefficient can be calculated using equation 5.3 below:

$$S_{11} = \frac{Z_T - 50}{Z_T + 50} . \qquad (5.3)$$

The real and imaginary parts of the S_{11} parameter measured at zero bias for a VCSEL with a 28μm diameter mesa and a 7μm oxide aperture as a function of frequency were loaded and plotted using MathCAD. Then the real and imaginary parts of equation 5.3 were plotted after providing initial estimated values for the four unknown elements C_a, R_s, C_p and R_p. In order to get the best fit, the least square error between the measured S_{11} data and the predicted S_{data}, as well as the values of C_a, R_s, C_p and R_p that minimize the error, were calculated in MathCAD using equations 5.4 and 5.5, respectively,

$$err(R_s, C_a, R_p, C_p) = \sum_i \left| S_{11}(f_i, R_s, C_a, R_p, C_p) - S_{data} \right|^2 \qquad (5.4)$$

$$ans = Minimize(err, R_s, C_a, R_p, C_p) . \qquad (5.5)$$

Guessing various values for C_a, R_s, C_p and R_p was attempted until the error was minimized to about 1.6. The resulting values that give the best fit depending on MathCAD calculations were as follows:

$$Minimize(err, R_s, C_a, R_p) = \begin{pmatrix} 45 \\ 135 \times 10^{-15} \\ 17 \\ 65 \times 10^{-15} \end{pmatrix},$$

where:

$R_s = 45\Omega, C_a = 135 fF, R_p = 17\Omega, C_p = 65 fF$.

Then to determine the active area resistance, the measured S_{11} parameter at non-zero bias was used. The total impedance of the VCSEL was recalculated, including the active area

resistance R_a, as shown in Figure 5.2.a. Z_1 stays the same, as shown in equation 5.1.a, but Z_2 will have a new term R_a, as shown in equation 5.6:

$$Z_2 = R_s - \frac{jR_a}{2\pi f C_a R_a - j} \quad . \qquad (5.6)$$

Similar to the procedure used to fit the zero bias data, the least square error between the measured S_{11} data and the predicted S_{data}, as well as the value of R_a that minimizes the error, were calculated in MathCAD using equations 5.7 and 5.8, respectively, this time with only one variable R_a, since it is the only element that depends on the biasing current.

$$err(R_a) = \sum_i \left(\left|S_{11}(f_i, R_a) - S_{data}\right|\right)^2 \qquad (5.7)$$

$$ans = Minimize(err, R_a) \quad . \qquad (5.8)$$

Starting from the initial estimated values for R_a, MathCAD returns different values of R_a for different biasing currents that result in a minimum least square error. Table 5.1 below illustrates the different biasing currents and their corresponding active area resistance, R_a, as well as the minimum error that was calculated.

Bias current I_{bias} (mA)	**Active area resistance R_a (Ω)**	**Error(Ω)**
0.0	∞	1.60
1.0	98.98	0.13
1.5	91.31	0.10
2.0	85.33	0.01
2.5	80.36	0.11
3.0	75.96	0.09
3.5	71.84	0.10
4.0	66.07	0.01
4.5	64.36	0.11

Table 5.1

Figure 5.3 illustrates the least square error over the VCSEL bias current. It is clear from the plot that our electrical model represents the fabricated high speed VCSEL at bias currents greater than zero, since the least square error is approximately zero. The only concern is that the best least square error at zero bias current is about 1.6, which means that our model underestimates a parameter that has some effect at zero bias.

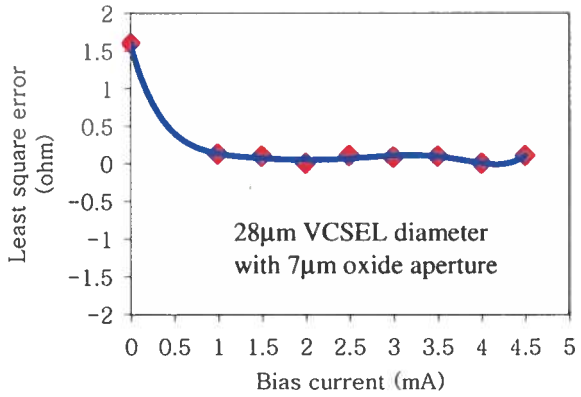


Figure 5.3 Least square error over the VCSEL bias current

To obtain an electronic EXCEL file for the S_{11} data that was used in this fitting send email to ahmad@engr.colostate.edu or kllear@engr.colostate.edu.

Figure 5.4 below illustrates the real and imaginary parts for both the measured S_{11} and that obtained from the proposed VCSEL electrical model. It is clear from this plot, as well as the plots for the same VCSEL at different bias currents, which are shown in Figure 5.5 below, that our predicted model and the value of its components are in good agreement with the real VCSEL.

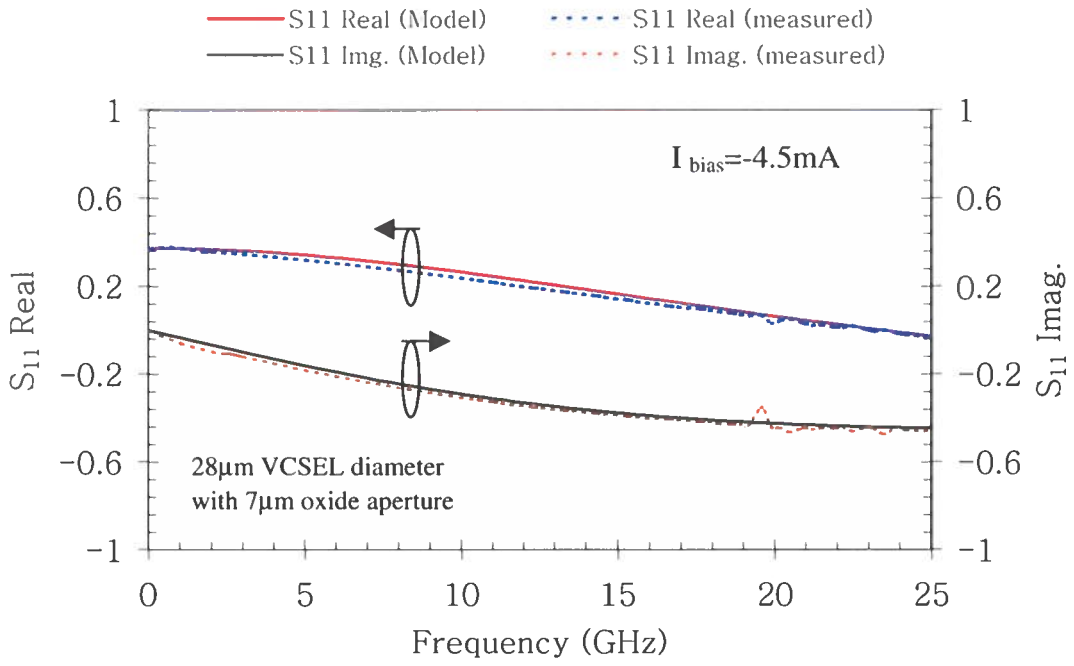


Figure 5.4 Real and imaginary S_{11} parameter Vs frequency from both the model and the measured data

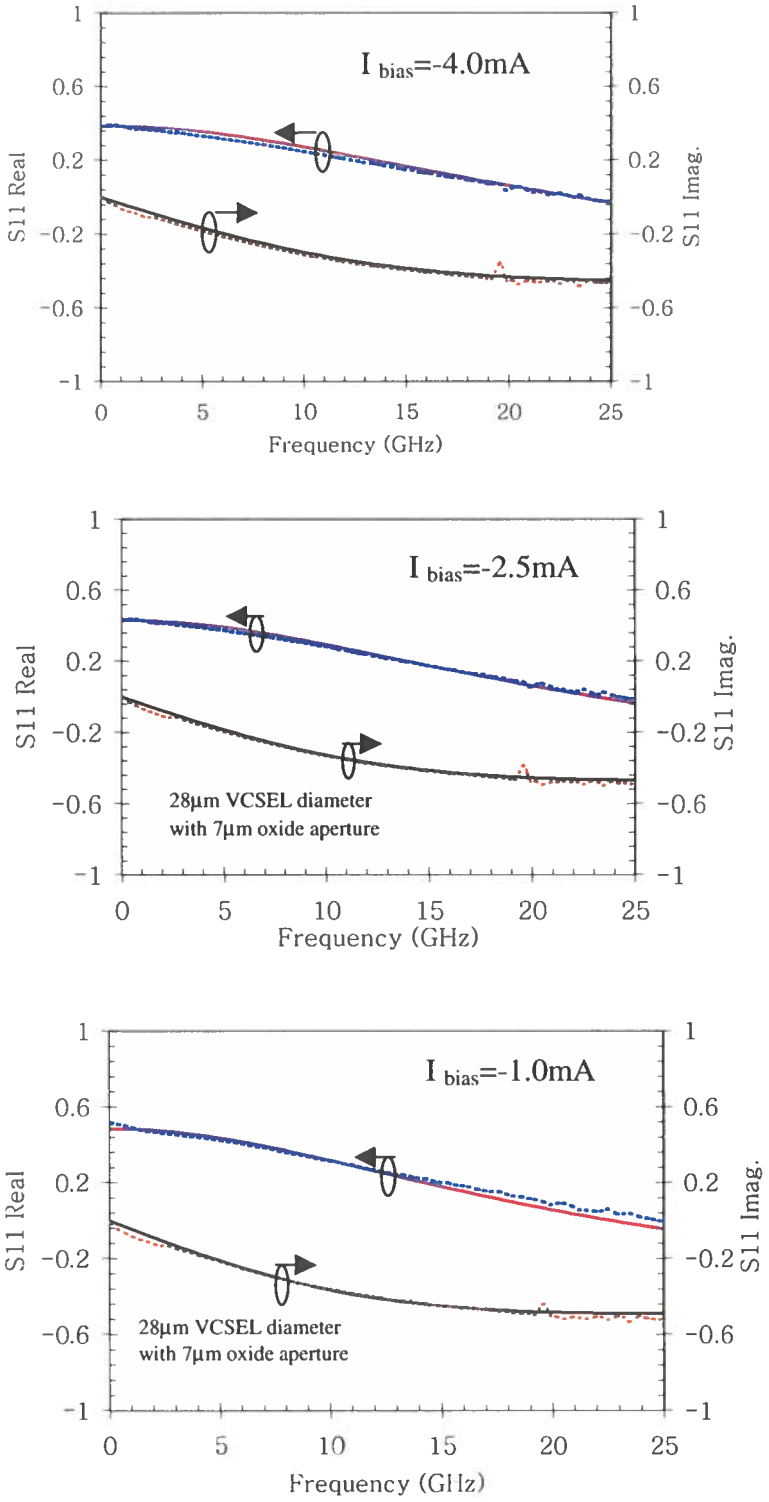


Figure 5.5 Real and imaginary S_{11} parameter Vs frequency from both the model and the measured data at different bias currents

Figure 5.6 below represents the complete electrical model for a VCSEL with 28μm mesa diameter and 7 μm oxide aperture. R_a was left variable since it is a function of the biasing current. As the frequency, increases the capacitors C_a and C_p begin to shunt current away from the active region, so the VCSEL response decreases with frequency. To check what limits our VCSEL modulation response, the –3dB electrical frequency response for the model shown in Figure 5.6 was calculated. In the calculations below we have ignored the effect of pad capacitance C_p, as well as mirror resistance R_p, on the VCSEL modulation frequency.

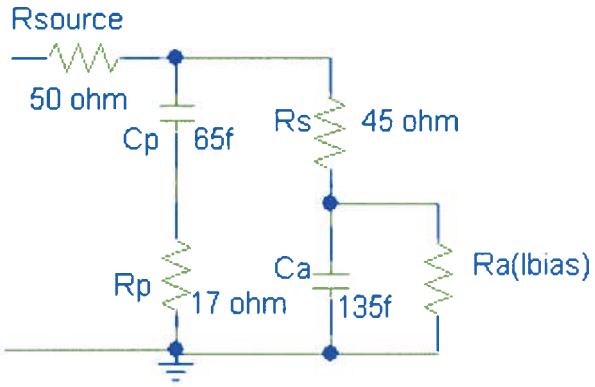


Figure 5.6 VCSEL electrical model

$$\frac{R_a // C_a}{(R_s+50)+R_a // C_a} = \frac{\dfrac{R_a \dfrac{1}{j\omega C_a}}{R_a+\dfrac{1}{j\omega C_a}}}{(R_s+50)+\left(\dfrac{R_a \dfrac{1}{j\omega C_a}}{R_a+\dfrac{1}{j\omega C_a}}\right)} = \frac{\dfrac{R_a}{R_a+\dfrac{1}{j\omega C_a}}}{j\omega(R_s+50)C_a+\dfrac{R_a}{R_a+\dfrac{1}{j\omega C_a}}}$$

$$= \frac{R_a}{j\omega(R_s+50)C_a\left(R_a+\dfrac{1}{j\omega C_a}\right)+R_a} = 0.5 \Longrightarrow \omega(R_s+50)C_a = 1+\frac{(R_s+50)}{R_a}$$

$$f_{-3dB} = \frac{\left(1 + \frac{R_s + 50}{R_a}\right)}{(R_s + 50)C_a} . \qquad (5.9)$$

Using equation 5.9, the electrical f_{-3dB} for the VCSEL was calculated and compared with the measured optical modulation frequency at –3dB for different bias currents. Results are listed in Table 5.2 shown below. It is clear from the results that our VCSEL is not limited by its extrinsic parasitics but rather limited by its intrinsic modulation response of the VCSEL. As a result, finding the proper solution for the intrinsic parastics will result in an optical modulation frequency of up to more than 30 GHz.

Bias current I_{bias} (mA)	**$f_{-3dB\ ele}$ (GHz)**	**$f_{-3dB\ opti}$ (GHz)**
1.0	24.32	6.5
1.5	25.32	9.7
2.0	26.22	11.5
2.5	27.08	13
3.0	27.93	14.4
3.5	28.82	15.8
4.0	29.73	16.8
4.5	30.73	17

Table 5.2

5.2 Pad, oxide and junction capacitance calculations

The physical dimensions of the pad, as well as the polyimide thickness, were measured to calculate the pad capacitance C_p so that the number of unknown circuit elements could be reduced to three. The dimensions measured using a scaled microscope and the polyimide thickness was measured using the α-step surface profilometer. The ploy imide thickness (d) was measured to be about 5.5μm. The pad dimensions are shown in Figure 5.7 below.

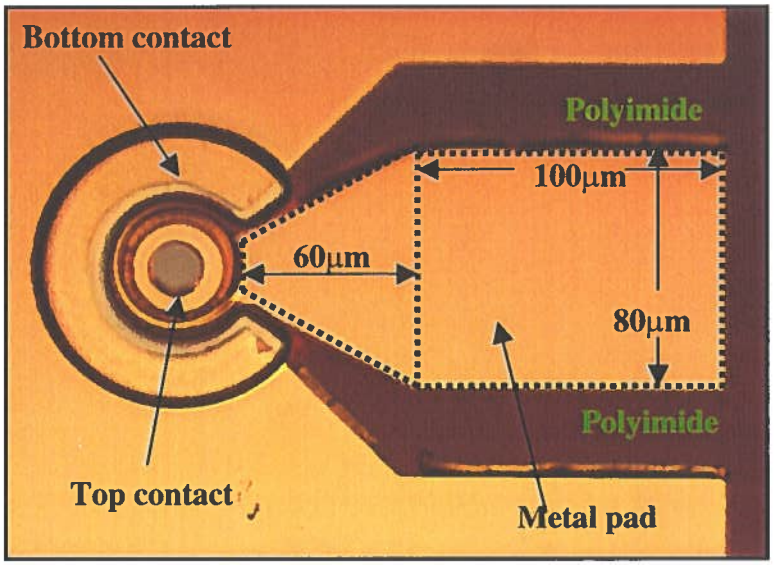


Figure 5.7 VCSEL top view with superimposed pad dimensions

$X_1 = 100\times10^{-4}\ cm,\ X_2 = 60\times10^{-4}\ cm,\ Y = 80\times10^{-4}\ cm$.

The rectangular area is $A_1 = X_1 \cdot Y = 100\times10^{-4} \cdot 80\times10^{-4} = 80\times10^{-6}\ cm^2$.

The triangular area is $A_2 = \frac{1}{2} \cdot X_2 \cdot Y = \frac{1}{2} \cdot 60\times10^{-4} \cdot 80\times10^{-4} = 24\times10^{-6} cm^2$.

The total pad area is $A_T = A_1 + A_2 = 104\times10^{-6} cm^2$.

The pad capacitance can then be calculated using equation 5.10 shown below,

$$C_p = \frac{\varepsilon_o \varepsilon_r A_T}{d}\ , \qquad (5.10)$$

where:

ε_o: Permitivity of free space ($8.85\text{x}10^{-14}$ F/cm)

ε_r: Dielectric constant (3.9 for HD-8000 polyimide at 1kHz)

A_T: Pad area

d: Polyimide thickness.

Substituting the corresponding values in equation 5.10, we get the following:

$C_p = \frac{3.9 \cdot 8.85 \times 10^{-14} \cdot 104 \times 10^{-6}}{5.5 \times 10^{-4}} = 62.3 \times 10^{-15} F = 62.3 fF$. This is in good agreement with the pad capacitance that was obtained using the measured S_{11} parameters, which was *65fF*.

Although it is expected that the relative permitivity will be changed with frequency, in our calculations we simply used its value at 1kHz, as provided by the manufacturer.

C_a is a combination of three capacitances, as shown in Figure 5.8 below. Ca can be calculated using equation 5.11 as follows:

$$C_a = \left(\frac{C_{ox} C_{j1}}{C_{ox} + C_{j1}} \right) + C_{j2} \quad . \qquad (5.11)$$

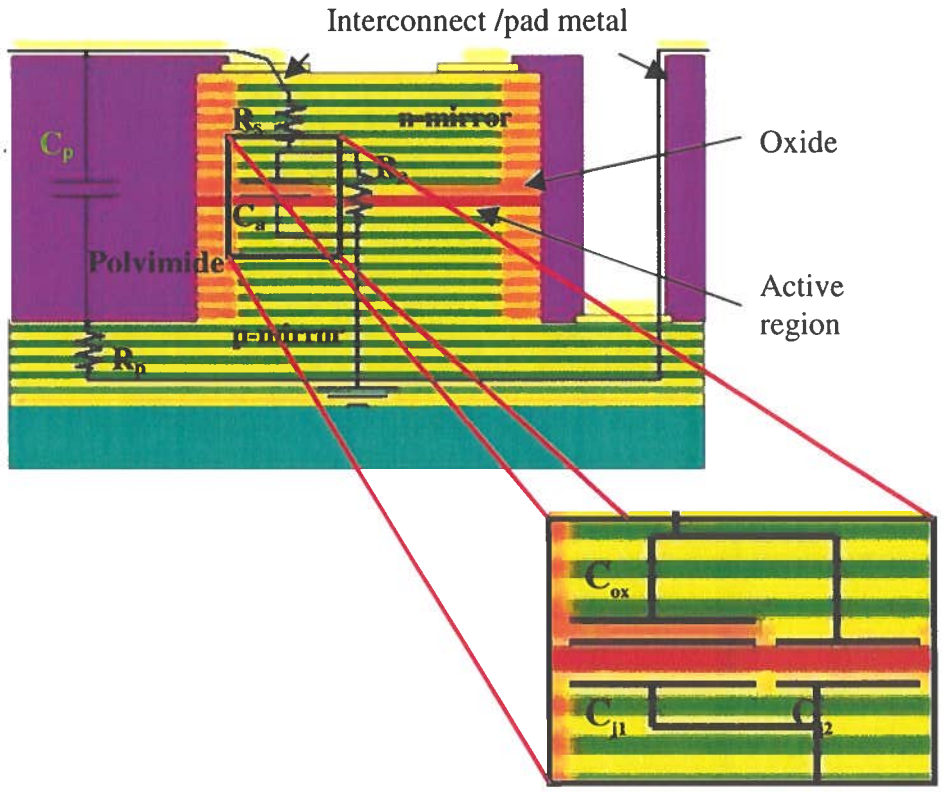


Figure 5.8 A cross section of high speed VCSEL with superimposed equivalent circuit. (Reproduced after [11])

As for the oxide capacitance per unit area, it can be calculated using equation 5.12 shown below,

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox}}{d_{ox}}, \qquad (5.12)$$

where:

ε_{ox}: Al_2O_3 dielectric constant ~ 9.0 [12]

d_{ox}: Oxide thickness, which in this case is equal to the thickness of the high aluminum composition layer $Al_{0.98}Ga_{0.02}As$ ($60x10^{-7}$cm).

Substituting the corresponding values in equation 5.11 we get the following:

$$C_{ox} = \frac{9.0 \cdot 8.85 \times 10^{-14}}{60 \times 10^{-7}} = 1.328 \times 10^{-7} F = 132.8 nF / cm^2 .$$

The junction capacitance per unit area is calculated using equation 5.4, but with the corresponding values for the GaAs:

ε_r: GaAs dielectric constant ~13.1

d: GaAs thickness, which in this case is equal to the total thickness of the quantum well layers ($171x10^{-7}$cm).

Substituting the corresponding values in equation 5.10, we get the following:

$$C_j = \frac{13.1 \cdot 8.85 \times 10^{-14}}{171 \times 10^{-7}} = 6.783 \times 10^{-8} F = 67.83 nF / cm^2 .$$

The active area equivalent capacitance is simply the combination of C_{ox}, C_{j1} and C_{j2}, where C_{j1} and C_{j2} can be calculated using equations 5.13.a and 5.13.b, respectively.

$$C_{j1} = C_j \left(\left(\frac{R_{mesa}}{2} - \frac{1}{3}\left(\frac{R_{mesa}}{2} - \frac{R_{ox}}{2} \right) \right)^2 - \left(\frac{R_{ox}}{2} \right)^2 \right) \qquad (5.13.a)$$

$$C_{j2} = C_j \pi \left(\frac{R_{ox}}{2} \right)^2 . \qquad (5.13.b)$$

where:

R_{mesa} : The diameter of the mesa (28×10^{-4}cm)

R_{ox} : The diameter of the oxide aperture (14×10^{-4}cm).

The active area total capacitance can be calculated be substituting the values of C_{ox}, C_{j1} and C_{j2} into equation 5.11, which will result in equation 5.14 below:

$$C_a = \left[\pi \left(\frac{C_{ox} C_j}{C_{ox} + C_j} \right) \cdot \left(\left(\frac{R_{mesa}}{2} - \frac{1}{3} \left(\frac{R_{mesa}}{2} - \frac{R_{ox}}{2} \right) \right)^2 - \left(\frac{R_{ox}}{2} \right)^2 \right) \right] + C_j \pi \left(\frac{R_{ox}}{2} \right)^2 \qquad (5.14)$$

Solving for C_a, we get $C_a = 174.9fF$. This is in acceptable agreement with the active area capacitance, which was obtained by using the measured S_{11} parameters, *135fF*.

5.3 PSPICE equivalent circuit simulation.

The VCSEL equivalent circuit shown in Figure 5.8 below was simulated using PSPICE software. The value of R_a was changed to cover all the values listed in Table 5.1. Simulation results are shown in Figure 5.9 below.

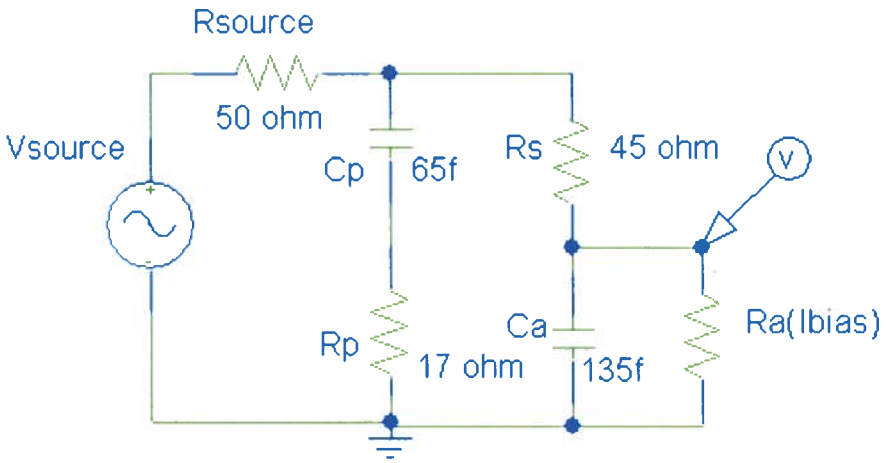


Figure 5.8 PSPICE equivalent circuit

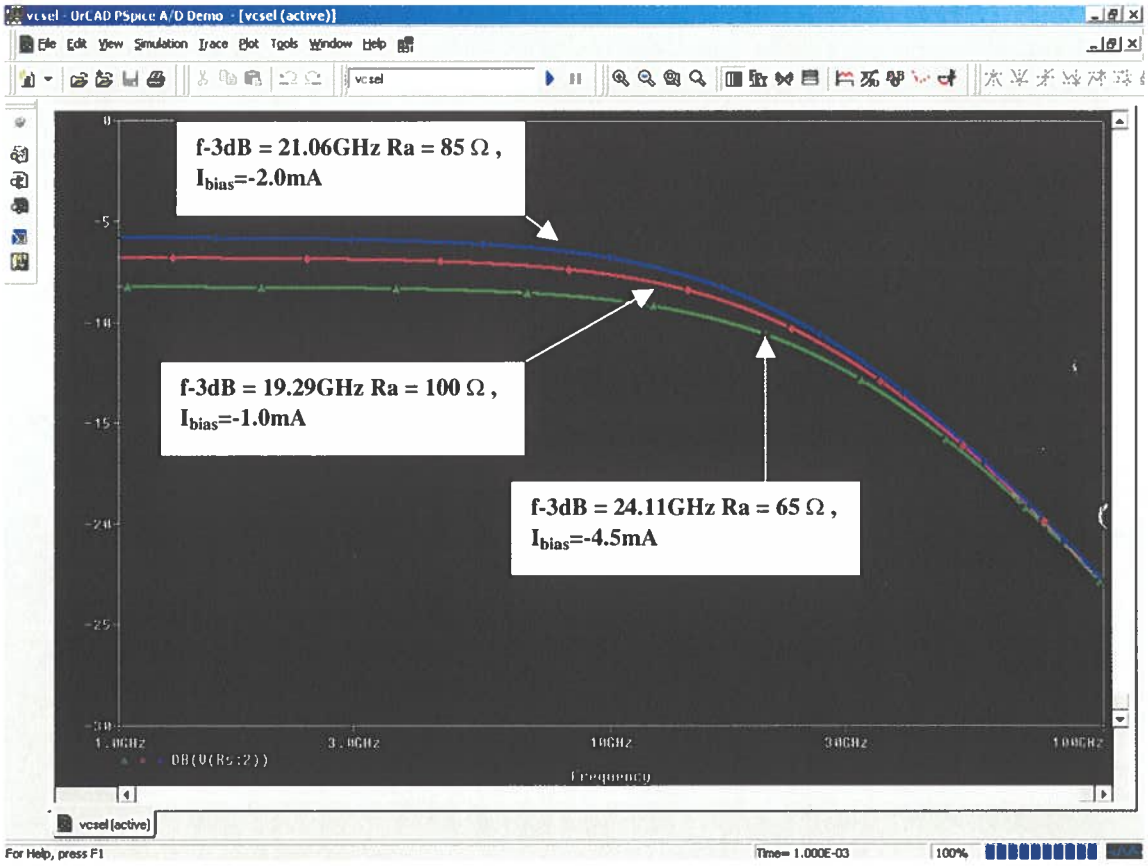


Figure 5.9 PSPICE screen capture simulation results

Figure 5.10 below illustrates the difference between the –3dB calculated frequency using equation 5.9 and the –3dB frequency obtained from PSpice simulation. The difference between theory and simulation is expected to be due to ignorance of the effect of the pad capacitance C_p and the mirror resistance R_p in deriving equation 5.9, or due to the assumption we made earlier which stating that the dielectric constant of the polyimide is constant as a function of frequency.

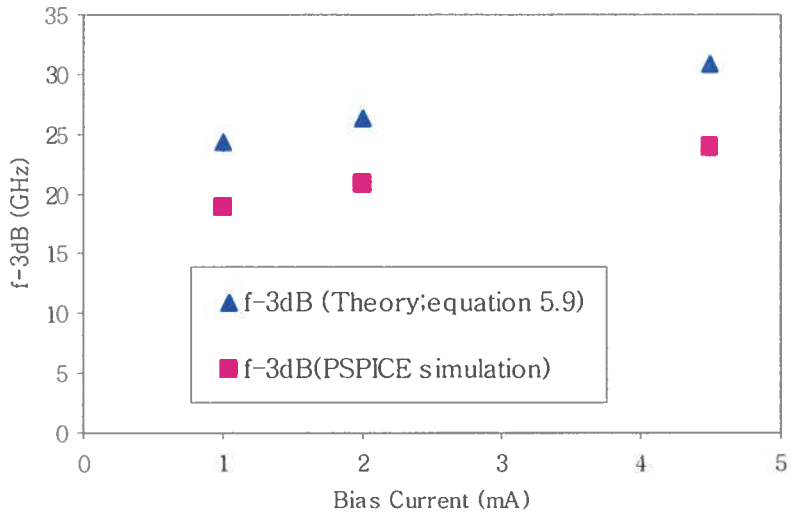


Figure 5.10 f_{-3dB} as a function of the bias current

5.4 Ion implantation

With the proper wafer VCSEL design and reduction of the intrinsic parasitics that limit geometry, together with good VCSEL performance and good thermal characteristics, we will reach the point at which the VCSEL modulation response is limited by its extrinsic parasitics. In this section, further improvements in the VCSEL extrinsic parasitics are presented and discussed.

Ion implantation, which is applied to semiconductor technology, is defined as a process by which energetic impurity atoms can be projected into a single crystal substrate for the purpose of changing its electronic properties. Ion implantation is usually carried out with ion energies in the range of 30-400 keV and doses in the range of 10^{12} to 10^{14} atoms/cm^2 [5].

There are a number of areas in which ion implantation technology has already been demonstrated successfully. Proton bombardment has been used to create isolation regions around a number of devices [5]. This includes photodiodes and field effect

transistors, in addition to transfer electron devices, avalanche transmit time oscillators and lasers [1, 9]. In many of these devices, the special doping profile provided by multiple implants has allowed improved performance and extended operating frequencies as well as power outputs. Moreover, a unique application for proton bombardment has been found in providing optical isolation in couplers and optical wave-guides. Ion implantation has also been used to make ohmic contacts to a number of microwave and optelectronic devices [1].

5.4.1 Overview

Several requirements are essential for an ion implantation system. These are ion sources and means for their extraction [2], acceleration, purification, beam deflection and scanning to impingement on the substrate [1, 3]. Ion sources are usually impure, so methods must be provided for mass separation and for rejection of unwanted species. The choice of materials for the ion source is very wide [1, 2]. As for acceleration, there is usually a spread of energies attained by ions upon acceleration. Energy is imparted to the ion beam by passing it through a long column across which there is acceleration potential.

The energetic ion undergoes many collisions with the lattice atoms before losing its kinetic energy and finally coming to rest. All the way through this process, energy is transferred to the lattice. As a result, the lattice atoms can be dislocated, often with substantial energy. These in turn can displace other atoms in the lattice, which results in a cascade of collisions. The displacement energy for both silicon and gallium arsenide is

about 14-15 eV. As a result, about 10^3 -10^4 lattice atoms are displaced by each incident ion [1].

Ion implantation can be used for forming heavily doped regions [4], as well as producing isolation regions [1, 5]. As for our application, the ion implantation will be used to produce damage in the crystal lattice to make the DBRs insulating. More discussion will be provided on this point later in this chapter.

The nature of the damage created by the implanted ion will depend on whether the implanted ion is light or heavy relative to the lattice atoms. A light atom will normally transfer a small amount of its energy during each encounter with the sample, and will be redirected through a large scattering angle during this target. The dislocated target atom will have a small amount of energy introduced into it, and will most likely not create further displacements of its own. The damage created by a single, light incident ion will thus take the form of a branching dislocation track, as illustrated in Figure 5.11 below [1].

Heavy ions implantation has a quite different effect. In this case, a large amount of energy is passed on with each collision, and the incident ion is diverted through a quite small scattering angle. Each displaced atom is itself capable of producing a large number of displacements as it moves away from the path of the incident ion. At the same time, the range is small, and most of the energy is transferred to the lattice. Consequently there is significant lattice damage within a fairly small volume. This damage takes the form shown in Figure 5.11 below. It consists of a somewhat straight dislocation track, surrounded by an ellipsoidal region with a high density of interstitial atoms [1].

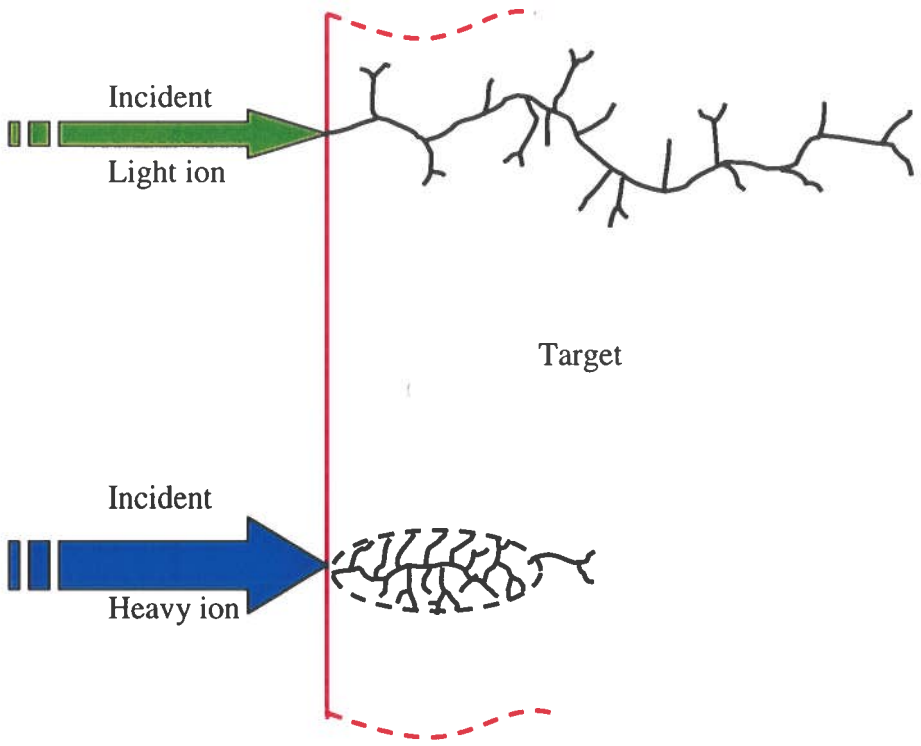


Figure 5.11 Target damage due to (a) light ions and (b) heavy ions using same target material (Reproduced after [1])

Ions are typically implanted at a slight angle to the crystal axes of the substrate, on the order of 6^{o} to 10^{o} [7]. This is done to prevent an effect called channeling. If the crystal lattice is viewed in an appropriate direction, there are open cells which contain no atoms, as shown in Figure 5.12 below; these are called channels. An ion moving parallel to a channeling direction can travel deep into the crystal before scattering occures. As a result, channeling produces implant profiles that are very difficult to predict and

reproduce [7]. In some cases, channeling is used as a trick to get deeper ion implantation depths.

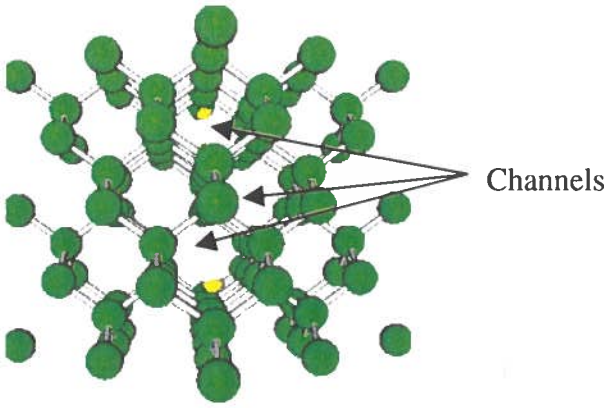


Figure 5.12 Illustration for channeling effect [6]

5.4.2 VCSEL ion implantation

The VCSEL structure data, which includes the different layer thicknesses and their chemical compositions, was loaded into the TRIM software [8]. The angle of incident was chosen to be 7^{o} to reduce the channeling effect. As for the implantation species, hydrogen (H^{+}) was selected since its atomic weight is 1.00794, which is considered light compared to other elements [10]. As a result there is no need to use high values of implantation energy to carry out the deep implantation. Moreover the hydrogen atom's radius is $37x10^{-12}$ m, which is considered small, compared to other elements [10]. As a result, the implantation will cause less damage to the surface of the sample. Damaging the surface will result in high contact resistance when depositing the metal contacts, which will affect the device's performance, as mentioned earlier in Chapter 4. Figure 5.13 illustrates the relative sizes of gallium, arsenic and hydrogen atoms.

Figure 5.13 Gallium, arsenide and hydrogen atoms. (values from [10])

Four implantations at different energies were simulated, since one or two are not enough to create continuous, sufficient damage from the surface to a depth of 2.5μm where the active region is located. The number of implantations was determined based on the distribution of vacancies using the simulation results. Different energies were tried until the required distribution of vacancies was obtained, as shown below in Figure 5.14.

The energy values that result in this vacancies distribution are (310, 250, 190, 130) eV, with (1600, 900, 600, 600) number of ions per implant respectively.

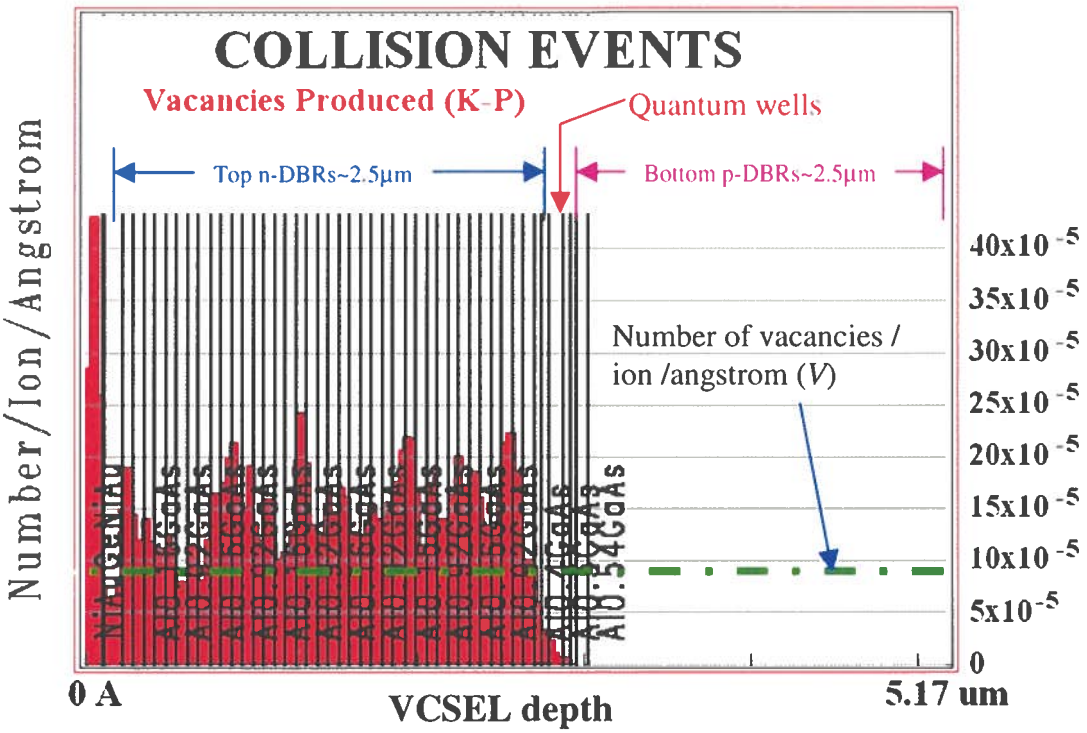


Figure 5.14 Ion implantation simulation results using TRIM

From the simulation results, the number of vacancies per ion per angstrom (V) equals

$V = 10\times10^{-5} / Ion / A^{o} \rightarrow V = 1\times10^{4} / Ion / cm$.

The total dose (Q_o) can be calculated using equation 5.15 shown below,

$$Q_o = \frac{N}{V}, \qquad (5.15)$$

where N is the doping concentration and V is the number of vacancies per ion per angstrom.

Since the doping of the mirrors $N = 1\times10^{18} cm^{-3}$, then the total dose ($Q_o$) will be,

$$Q_o = \frac{N}{V} = \frac{1\times10^{18}}{1\times10^{4}} = 1\times10^{14} ions / cm^{2}$$

The total number of ions implanted (T_o) will be,

$$T_o = T_{o1} + T_{o2} + T_{o3} + T_{04} = 1600 + 900 + 600 + 600 = 3.7 \times 10^3 ion$$

The dose (Q_{ox}) for the x implant with implantation energy of y eV can be calculated using the equation 5.16:

$$Q_{ox} = \left(\frac{T_{oy}}{T_o} \right) \cdot Q_o \ , \qquad (5.16)$$

where T_{oy} is the number of implanted ions at y energy

T_o is the total number of implanted ions at all energies.

For the first implantation we have:

$$Q_{o1} = \frac{1600}{3700} \cdot 1 \times 10^4 \rightarrow Q_{o1} = 4.324 \times 10^{13} ion/cm^2$$

Similarly, for the other three implants we get,

$$Q_{o2}(energy = 250eV) = 2.432 \times 10^{13} ion/cm$$

$$Q_{03}(energy = 190eV) = 1.266 \times 10^{13} ion/cm$$

$$Q_{o4}(energy = 130eV) = 1.266 \times 10^{13} ion/cm$$

The ion implantation step is usually carried out after applying the top contact metals because the implantation process sometimes leaves a small amount of photoresist contamination on the surface of the sample that would interfere with the formation of low resistance contacts. After deciding the number of implants, energies and doses the sample has to undergo the same fabrication steps mentioned in Chapter 4 are used with some changes when applying the top contact. The evaporated metals for the top contact should be less than 100nm so that the implanted ions can penetrate through the contact easily. After applying the thin top contact metals, the implantation photomask is patterned using the standard photolithography process discussed earlier in Chapter 4. The photoresist mask used should be thick enough so that it can prevent the implanted ion

from penetrating through it, thereby implanting undesired parts of the sample. After that, the sample is implanted. Then the fabrication steps are resumed from the bottom contact step up to the end of the fabrication steps. The expected result, using the above values of the angle, dose and energies for ion implant of the oxidized VCSEL is shown below in Figure 5.15. As a result of this ion implantation, the oxide capacitance is expected to be reduced, which is expected to increase the modulation frequency of the VCSEL and to further confine the current path, which will result in reducing the VCSEL self-heating.

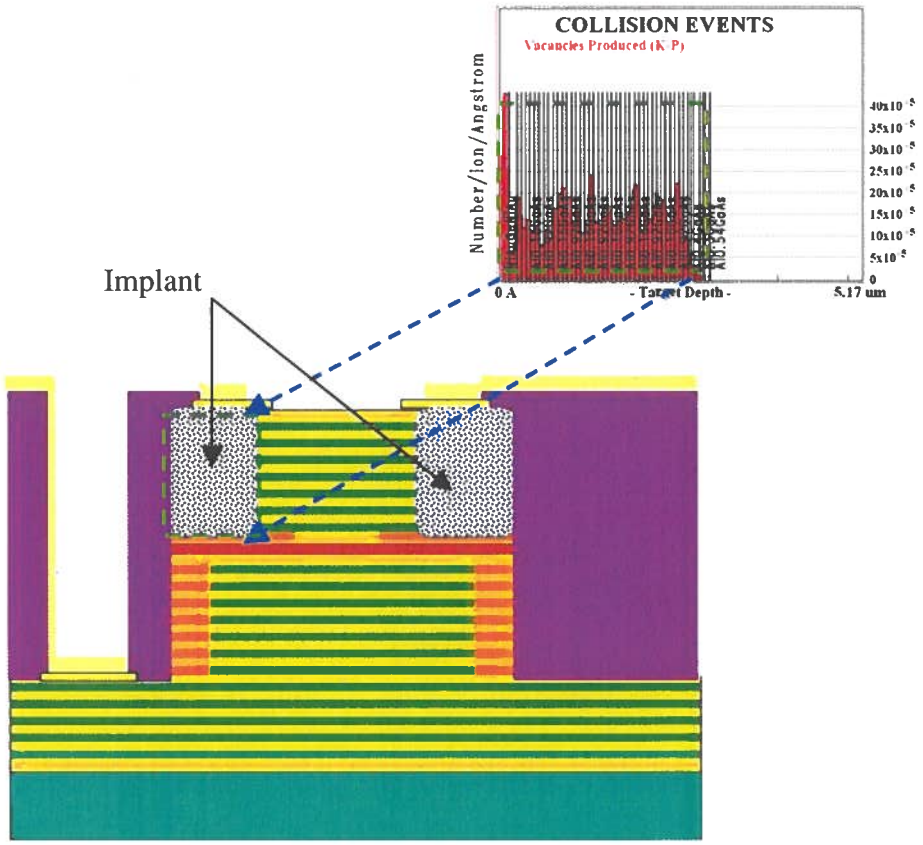


Figure 5.15 A cross section of oxidized and ion implanted VCSEL.

We now rexamine the value of C_a after the ion implantation. Figure 5.16 below shows in details all the capacitance components that contribute to Ca.

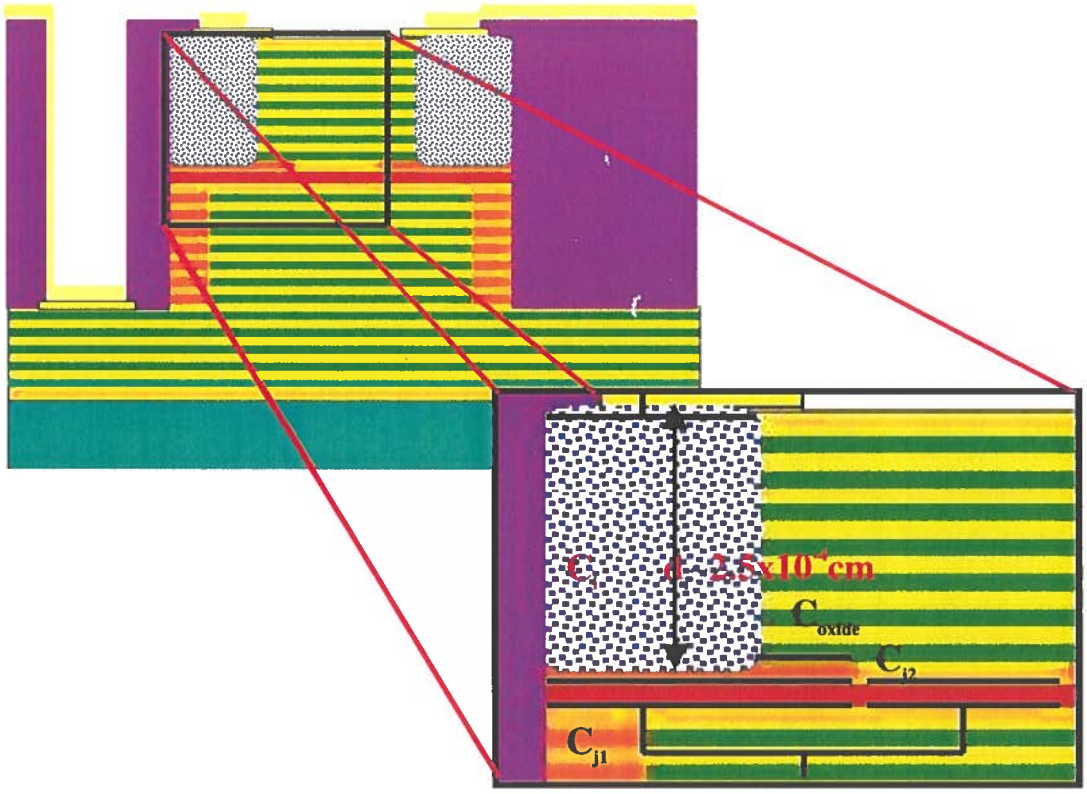


Figure 5.16 Ion implanted VCSEL cross-section illustrating the capacitance components that contribute to Ca

The oxide capacitance per unit area and the junction capacitance per unit area were calculated earlier using equation 5.12 and they were found to be

$C_{ox} = 132.8nF/cm^2$

$C_j = 67.83nF/cm^2$.

The active area total capacitance C_a can be calculated using equation 5.17 below,

$$C_a = \left[\pi \left(\frac{(C_{oxide} + C_i) C_{j1}}{(C_{oxide} + C_i) + C_{j1}} \right) \right] + C_{j2} \quad , \qquad (5.17)$$

where:

C_{j1} and C_{j2} can be calculated using equations 5.13.a and 5.13.b respectively. As for C_i and C_{oxide}, they can be calculated using the corresponding equations 5.18.a and 5.19.b. Values used for ε_i and d_i are 9 and 2.5×10^{-4}cm.

$$C_i = \frac{\varepsilon_o \varepsilon_i}{d_i} \left[\left(\left(\frac{R_{mesa}}{2} - 0.3 \left(\frac{R_{mesa}}{2} - \frac{R_{ox}}{2} \right) \right)^2 - \left(\left(\frac{R_{mesa}}{2} - 0.3 \left(\frac{R_{mesa}}{2} - \frac{R_{ox}}{2} \right) \right)^2 \right) \right) \right] \qquad (5.18.a)$$

$$C_{oxide} = C_{ox} \left[\pi \left(\frac{\left(\frac{R_{mesa}}{2} - 0.3 \left(\frac{R_{mesa}}{2} - \frac{R_{ox}}{2} \right) \right)}{2} \right)^2 - \left(\frac{R_{ox}}{2} \right)^2 \right] \quad . \qquad (5.18.b)$$

Solving for C_a, we get $C_a = 83.75fF$. Comparing this value to the oxide capacitance value before ion implantation, $C_a = 174.9fF$, we find that by ion implantation the value of C_a is expected to be reduced to less than 52% of its current value.

Assuming that the values of the other electrical components we obtained earlier will stay the same after implantation, we run the PSPICE simulation to get the electrical -3dB frequency for the circuit diagram shown in Figure 5.8, using the two values of C_a (i.e., with and without implantation). Figure 5.17 represents a screen capture for the PSPICE simulation screen. The electrical f-3dB without implantation is about 19GHz, while the electrical f-3dB with ion implantation is about 32GHz. This means that in terms of the frequency response, we expect that ion implantation will increase the VCSEL modulation frequency by 30% more.

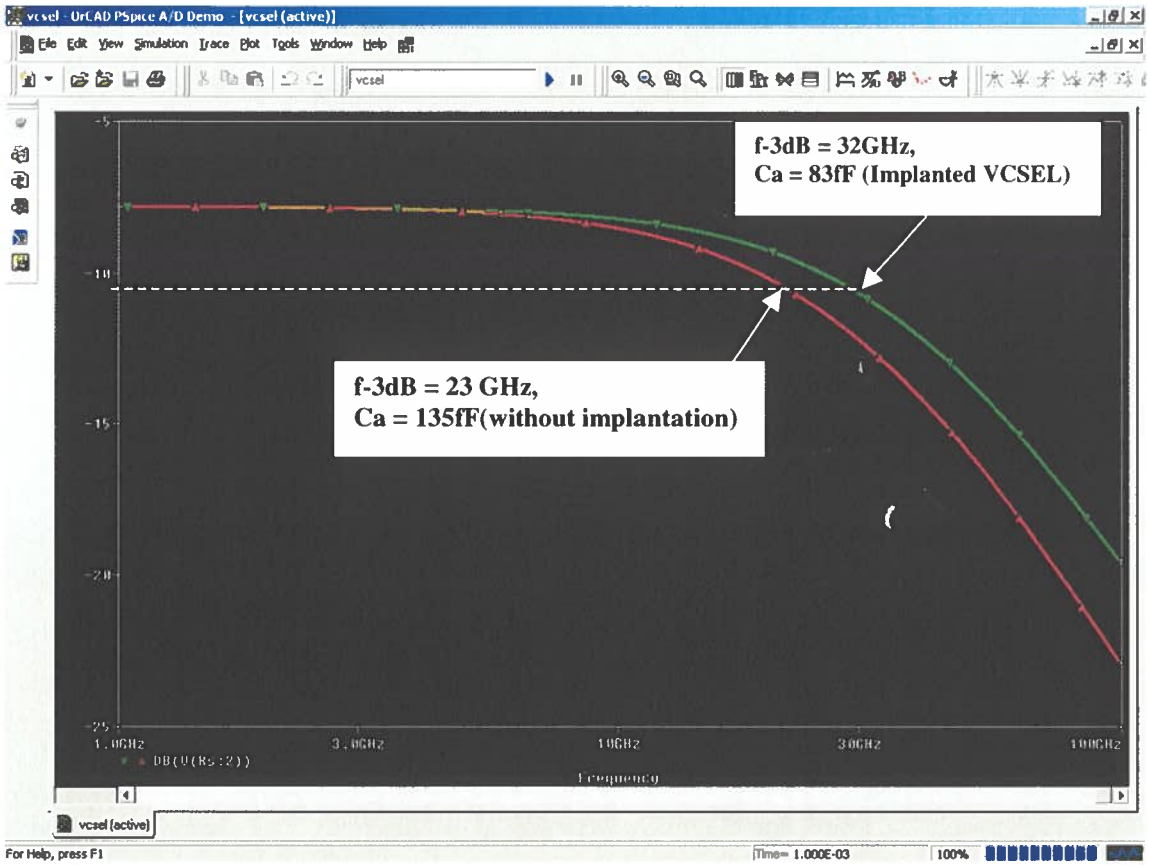


Figure 5.17 Screen capture for the SPICE simulation screen

References:

[1] Sorab K. Ghandhi, "VLSI Fabrication Principles Silicon and Gallium Arsenide," 1983.

[2] A. Axmann, "Ionizable Materials to produce Ions for Implantation," Solid State Technol., p. 36, Nov., 1974.

[3] G. Dearnaley, J. H. Freeman, "Ion Implantation," North Holland, New York, 1973.

[4] R. Heckingbottom and T. Ambridge, "Ion Implantation in Compound Semiconductors - An Approach Based on Solid State Theory," Rad. Eff., 71, 31, 1973.

[5] G. E. Stillman, C. M. Wolfe, "Electro-absorption Avalanche Photodiodes," Appl. Phys. Lett. 25, 671, 1974.

[6] http://www.iue.tuwien.ac.at/.

[7] Ralph Williams, " Modern GaAs Processing Methods," 2nd edition , 1990.

[8] http://www.SRIM.org.

[9] Stephen J. Pearton, " Processing of Wide Band Gap Semiconductors," 2000.

[10] Brady, Holum," Fundamentals of Chemistry," 3rd edition, 1988.

[11] Lear, K.L.; Hietala, V.M.; Hou, H.Q.; Banas, J.; Hammons, B.E.; Zolper, J.; Kilcoyne, "Small and large signal modulation of 850 nm oxide-confined vertical-cavity surface-emitting lasers," Lasers and Electro-Optics, 1997. CLEO '97. Summaries of Papers Presented at the Conference on , Volume: 11, pp.: 193 –194.

[12] http://www.accuratus.com/Aluminum_Oxide.htm.

CHAPTER 6

Conclusions and Future Work

This chapter summarizes the achievements of the research work of this thesis. Conclusions and suggestions for future work are given based on these achievements.

6.1 Achievements

The objective of this thesis research is to develop a reliable technique for fabricating High-Speed Oxide-Confined Vertical-Cavity Surface Emitting Lasers. The achievements include:

1) A complete and standard fabrication process for High-Speed Oxide Confined Vertical-Cavity Surface Emitting Lasers was developed.
2) High-Speed Oxide Confined Vertical-Cavity Surface Emitting Lasers were fabricated with a 3dB modulation frequency bandwidth up to 17.0GHz with about a 0.4mA threshold current at about 7μm oxide aperture diameter.
3) The critical fabrication steps that effect the Oxide Confined Vertical-Cavity Surface Emitting Lasers speed were determined.
4) The electrical and optical characteristic of the Oxide Confined Vertical-Cavity Surface Emitting Lasers were measured.
5) Two different types of polyimide, photosensitive and non-photosensitive, were examined. The effect of using an adhesion promoter on the cured polyimide at high temperature was investigated.
6) The fabricated VCSEL pad capacitance was reduced by attaining the maximum cured polyimide thickness (5.5 μm) which equalled the height of the etched mesa.

7) Metal pad adhesion to polyimide was investigated and improved. Adhesion strength was measured using scotch tape.

8) An equivalent circuit model for high-speed oxide-confined Vertical-Cavity Surface Emitting Lasers was obtained and simulated using PSPICE. This model can be used for designing high-speed interfacing circuits to VCSELs.

9) The effect of Ion Implantation on high-speed oxide confined Vertical-Cavity Surface Emitting Lasers modulation frequencies was modeled. Implantation doses as well as implantation energies for our particular VCSEL dimensions were determined and simulated using the SRIM software.

6.2 Conclusions

We have fabricated and characterized high-speed oxide-confined VCSELs with excellent high-speed performance.

Mesa dry etching should be used due to its advantages over wet etching. Also accurate control of oxidation process parameters, such as water bath temperature, sample temperature and gas flow rate, is important for repeatable and identical oxide-confined VCSEL fabrication. Moreover, scaling down the active area will reduce the VCSEL self-heating since the threshold current will be reduced.

The use of photosensitive polyimide instead of non-photosensitive polyimide gives reliable and repeatable results. Furthermore, the cured polyimide thickness should be maximized up to a certain limit since it will reduce the pad capacitance, which increases the modulation frequency of the oxide-confined VCSELs.

Utilizing the heat treatment improved the metal-to-polyimide adhesion strength. The use of ion implantation will result in higher modulation frequency for oxide-confined VCSELs due to reducing the oxide capacitance. Also, additional improvements can be obtained with improved heat sinking.

With the proper wafer VCSEL design and no parasitic limited geometry along with good VCSEL performance and good thermal characteristics we expect that it is possible to achieve VCSELs suitable for 40 Gb/s transmission.

6.3 Future work suggestions

Due to the lack of time and the breakdown of the e-beam evaporator in the cleanroom, some future work is suggested as an extension to this research in the pursuit of high-speed oxide-confined VCSELs.

More fabrication runs need to be done to optimize the High-Speed Oxide-Confine VCSEL fabrication process. Theoretical analysis of VCSELs, fabricated by the same fabrication process presented in this thesis but with additional ion implants is suggested, since this will result in reducing oxide capacitance and increasing VCSEL modulation bandwidth beyond other factors.

Redesigning the structure of the VCSEL so that the detrimental effects of ion implantation on resistance can be reduced and resistance vs. capacitance tradeoff can be optimized. The investigations of other factors that affect the VCSEL speed and optimize them. VCSEL self-heating is a factor that is worth investigating since the VCSEL is believed to be thermally limited.

Metal to polyimide adhesion needs more exploration. A well-defined research plan and a researcher in the field of chemistry are needed for this investigation. The change in the polyimide dielectric constant (ε_o) as a function of frequency needs to be studied, since this will help in predicting the actual value of the VCSEL pad capacitance.

Appendix A

STANDARD CLEANROOM OPERATION MANUAL

A.1 INTRODUCTION

In certain ways, the use of the CSU cleanroom is akin to driving a car. First and foremost, both are a *privilege* and not an inherent right; those who do not follow all of the appropriate rules and procedures can and may have their privilege to use the facilities revoked. Second, the use of the cleanroom, like a car, requires appropriate training and experience before being allowed to operate the equipment unsupervised. Since the cleanroom is a laboratory used by a number of research groups from multiple departments, some special requirements are made of each user in order to maintain a clean, safe, and successful working environment.

This cleanroom manual is intended to be part of that learning experience and to serve as a reference guide for appropriately trained users. **It is not a substitute for appropriate training.** In order to qualify as an approved cleanroom user for full use of the facilities, an individual must complete certain requirements. First, the one day Hazardous Waste Generator Training seminar given by the Environmental Health Services department on campus *must* be taken and passed. This is a university and state requirement for all hazardous waste generators, and since almost every cleanroom process results in such waste, ***all*** users must have documented training. Second, each user should obtain *and read* a personal copy of this manual. Before entering and using the cleanroom, all users should have a thorough understanding of the General Guidelines below and of the Cleanliness and Safety issues on the following pages. Ignorance is not an excuse for damaging equipment or, even worse, for injuring yourself or others.

The combination to the cleanroom door is only to be issued to those individuals who have demonstrated an understanding of the appropriate safety and cleanliness procedures. **Only the Cleanroom Manager has the authority to give out the combination, and under no circumstances should anyone else do so**. Users who give away the combination face the possibility of losing their cleanroom privileges. Also, never leave the door from the hall into the gowning room unlocked.

A.2 General Guidelines

Everything contained in this manual has a specific purpose, either to help maintain the cleanliness and safety of the cleanroom working environment, or to ensure appropriate use of the equipment, or both. Following everything herein will help keep people safe, and also will provide a guide toward successful research.

Due to the small scale nature of the semiconductor processing work performed in the cleanroom, maintaining a clean and safe environment is of utmost importance. **Everything brought into the cleanroom must be thoroughly wiped down to eliminate dirt and dust.** The single greatest source of contamination in the cleanroom is the people, so using the shoe brush and wearing the proper attire is *required* to minimize particulates. The HEPA filters and laminar air flow are expensive measures taken to provide an appropriate environment, but it is up to the users to maintain that environment. Hazardous chemicals are routinely used in the cleanroom, and proper procedures for handling, storing, and disposing of these chemicals is required. This is for the safety of everyone, and to comply with federal statutes. Please read and understand the Cleanliness and Safety sections of this manual before using the lab.

The equipment in the cleanroom is all delicate, expensive, and/or dangerous if used improperly. Therefore each piece of equipment, from the mundane (such as a microscope or a fume hood) to the complex (such as the evaporator or mask aligners), requires special training before an individual will be authorized to use it. This training is a two step process for each and every piece of equipment. First, one must receive detailed instruction in how to properly and safely operate a specific piece of equipment from someone who themselves is an authorized user of that equipment. Second, you *must* obtain authorization from the Cleanroom Manager to be able to use that equipment unsupervised. Authorization is typically granted after demonstrating competence by running the equipment under the observation (not assistance) of the Manager. An Authorized Cleanroom User Sheet is included with the official copy of this manual in the entry way to the lab. All users are required to be included on this list, and the sheet provides columns for checking off equipment each user is allowed to operate. *Any user found to be operating equipment for which they are not authorized will forfeit their cleanroom privileges.* The procedures contained in this manual are not a substitute for appropriate training. Additional information for the cleanroom equipment can be obtained from the binders and manuals currently located in C-17.

It is understood that, as in any facility used by many various individuals, accidents will happen and equipment will malfunction. Equipment users will not be blamed or punished for these occurrences, however that does not grant immunity from all responsibility. If something is found to be broken or not functional, report it immediately to the Cleanroom Manager. Then, since all users are presumably intelligent and well educated, as well as being some type of engineer or scientist, the responsibility of that

individual extends to repairing, or assisting in the repair of, the problem. If that individual is not knowledgeable or experienced enough to repair the problem, it is *still their responsibility* to notify the appropriate people and see the solution through. **Users that damage equipment and do not take this responsibility for their actions will lose their cleanroom privileges**. Remember, everyone using the cleanroom has their own problems and research work to do, and it is not fair to expect someone else to drop everything and solve your problems for you. Of course, most cleanroom users are considerate, and will stop to help fix a problem, especially if they have experience with the particular equipment and know the idiosyncrasies; also, those who are not considerate, and expect others to do the dirty work for them, will not be looked upon too kindly.

A.3 Cleanliness

As previously mentioned, due to the small scale nature of the semiconductor processing work done in the cleanroom, it is very important to keep a clean environment. Cleanliness is vital to the success and reproducibility of the various processes. The HEPA filters and laminar air flow are designed to limit the particle count to less than 1000 per cubic foot (a Class 1000 cleanroom). The initial certification of the room, before much of the equipment was installed, was at Class 100. In order to maintain this level of cleanliness, everyone using the cleanroom *must* follow the procedures outlined below.

1. When entering the cleanroom, *always* use the shoe brush and step both feet on the tacky mat.

2. Booties, hoods, and Tyvek coveralls must be put on while in the gowning room; never enter the actual cleanroom without being fully suited. Wearing the Nitrilite, powder free, cleanroom gloves also cuts down on particulates, so gloves should be worn at all times in the yellow room, and while working at the hoods or with samples at various pieces of equipment.
3. When bringing in items from outside (personal tools, samples, containers, etc.), be sure to thoroughly dust or clean them; a 70:30 mixture of propanol and deionized water (DI H_2O) can be used to wipe these items down and help minimize contaminants.
4. Never open the two doors in the gowning room at the same time, and do not hold either open for extended periods of time.
5. The door from the yellow room outside to the service corridor is an **emergency exit only**, and is not to be used for any other reason.
6. Nothing which generates particulates is to be used in the cleanroom. This includes, but is not limited to:
    - Pencils and paper (write only in pen and on the cleanroom paper provided).
    - Powdered gloves (only use the gloves supplied by the cleanroom).
    - Aerosols of any kind.
    - Food or drink of any kind.
    - Tobacco products.
7. Remember, when the above rules are observed, people become the greatest source of contamination, so be aware of your actions. If you feel a coughing/sneezing fit coming, exit to the gowning room. Hair spray, perfume, cologne, etc. are large

sources of particulates. Do not run in the cleanroom; people shed many more skin cells running than walking.

Be conscious of cleanliness issues and courteous to other users. Your mother is not on staff to clean up after you, so be sure to clean up after yourself. ***Always leave the cleanroom cleaner than it was when you entered.***

A.4 Safety

Safety is a primary concern in the cleanroom, as it should be in any laboratory. The key to maintaining a safe environment is for each and every user to take an active role, being concerned for not only their individual safety but also for the safety of everyone. First, **assume every chemical, solution, and piece of equipment is dangerous and may cause injury.** Even mundane things such as DI H_2O, which by the way should never be consumed, must be treated with caution and care. It is better to err on the side of caution than to learn the hard way.

Chemical Safety

Always use appropriate personal protection. **When handling chemicals always wear eye goggles and appropriate gloves.** The Nitrilite cleanroom gloves are designed to be chemically resistant to most solvents and acids. However, when using strong acids, especially HF and buffered HF, users should wear the thicker, rubber, acid resistant gloves. Periodically check gloves for tears or holes, and replace as necessary. The full IsoClean Tyvek suits will keep small splashes off your skin. The cleanroom policy is to label an individual suit and reuse it every time; however it should periodically be checked for holes or damage from chemical spills and be replaced as necessary. If in doubt, consult the Cleanroom Manager.

Eyewash/shower stations are located in the cleanroom, by the door from the gowning room, and also in the service corridor. If something splashes up around the face or eyes, even if unsure whether a chemical is on the skin, use the eyewash. If something gets around the eye goggles, thoroughly flush the eyes with water for several minutes and seek assistance and first aid. In the instance of a major spill and the saturation of all or part of the Tyvek suit, immediately go to the gowning room and remove the coverall. Check your clothes and skin for sign of contact with any chemicals and use the shower if necessary. If your clothes are soaked, remove them while using the shower. A few moments of personal embarrassment is easier to get over than a severe chemical burn. Never take chances with a chemical spill, and always report any such incidents to the Cleanroom Manager so that the cause of the accident, be it procedural, equipment, or human error, can be discovered and corrected to prevent similar occurrences.

Always use chemicals inside one of the two fume hoods (keeping the sash at or below the appropriate level), and never carrier open chemical containers around the room. Acids and bases are stored in separate locations and should not be used together. Never pour **w**ater **o**nto **a**cids or bases (w.o.a means stop); acids and bases should always be poured slowly into water. Solvents should never be mixed with acids or bases, and are stored separate from both. See the Hazardous Waste Procedures below for proper disposal guidelines.

Chemical containers should be dated with their purchase date, *and when opening a new bottle, the first user must label it with the date* (i. e. "opened 1/13/00").

When mixing a solution that will be temporarily be stored in the cleanroom, whether for several hours in the fume hood or for weeks in the appropriate cabinet, it must be **clearly** labeled. Labels must include chemical formula and concentrations of the solution components, the date mixed, and the user's name. Be sure solutions are stored in proper sellable containers and not in open specimen containers. Improperly labeled solutions will be disposed of, and if the contents are unknown this could be a very expensive process through EHS, which will be charged to the user and/or the sponsoring advisor.

If an individual wishes to bring a new chemical into the cleanroom, it must first be approved by the Cleanroom Manager. This should be done *prior* to procurement of the chemical. To obtain approval, two (2) copies of the Material Safety Data Sheet (MSDS) for that chemical must be given to the Manager, along with a description of the reason for its use. The user bringing in a new chemical is responsible for researching and implementing its appropriate storage, use, and waste accumulation/disposal procedures for the safety of everyone. The Cleanroom Manager may refuse admission of any materials on the grounds of general safety or for any other reasonable cause. Anyone bringing in a chemical without approval may lose his or her cleanroom privileges.

Hydrofluoric acid (HF) is an **extremely** corrosive acid. It can cause burns that can be painless and may exhibit delayed symptoms, and can also cause death in large exposures. HF users should read its MSDS very carefully to learn accident and first aid procedures (actually, this is a very good suggestion before using any chemical in the cleanroom). Always use thick acid gloves and eye protection, and only open and use HF

under the fume hoods (HF etching can produce toxic fumes). *HF readily attacks glass, and should only be used in Fluoroware containers.* Always follow etch recipes carefully because **HF can react violently with several common chemicals** including, but not limited to, nitric, sulfuric, and lactic acids, and sodium and ammonium hydroxides. Large HF spills, such as a spilled or broken bottle, should be cleaned up *only by trained personnel*; contact the Cleanroom Manager and/or EHS (1-6745) if such a spill occurs. HF spills can generate large quantities of H_2, which is explosive, and it can readily penetrate soluble materials, such as concrete, rendering them hazardous even when dried. HF use requires caution and careful attention to detail for the safety of all cleanroom users.

Hazardous Waste Procedures

Properly dealing with hazardous waste is one of the most important components of cleanroom safety. The following is a guide for current cleanroom waste procedures, and is not a substitute for appropriate training. The first part of that training is, as mentioned before, that all cleanroom users must pass the Hazardous Waste Generators Training course offered by EHS. This includes obtaining a personal copy of the Hazardous Chemical Waste System Manual from EHS. *It is the responsibility of each user to obtain this training* and then provide documentation of it to the Cleanroom Manager. The second part of this training includes specific instruction from an authorized cleanroom user in current cleanroom waste accumulation/disposal procedures as part of the training and approval process required for authorization to use the fume hoods.

Several important guidelines for current cleanroom hazardous waste accumulation and disposal procedures include:

- Acetone and methanol (or propanol) waste is collected together in glass 4 liter bottles (with appropriate waste labels) in the fume hoods.
- TCE and chlorobenzene wastes are collected individually in 500 ml glass bottles (with appropriate waste labels), and are stored in the flammables cabinet in the yellow room.
- A waste container is defined as full when the waste level is at 90% of the container volume (usually just above the "shoulder" of the bottle); **No More than 90%.** Overfilled bottles will not be taken by EHS for disposal.
- Full waste bottles are to be stored in the appropriate service corridor flammable cabinet.
- Most acids or bases can be neutralized and then poured down the sink; be sure to flow lots of city water down with it (approx. 4 liters of water per 100 ml of neutralized waste). **Always use the pH meter when neutralizing, and never dump anything down the drain unless the pH is between 6 and 8.**
- Glass slides, cover slips, and other sharp objects are to be collected in marked containers (usually a capped specimen container) near the corner sink in the yellow room and in the white room fume hood; never throw them in the trash cans.
- Waste GaAs/InP wafer material is to be considered hazardous and should be collected separately (a capped specimen container works well) for EHS disposal.
- **NEVER PUT ANY TYPE OF LIQUID WASTE INTO THE TRASH CANS.**

These guidelines and procedures are subject to change, so if unsure please ask the Cleanroom Manager. **Remember, according to federal law, individuals are legally responsible for their own hazardous waste.**

Fire Safety

In case of fire, place the safety of people above that of the equipment. Many fires, especially potential cleanroom fires with all of the available chemicals, emit toxic fumes, so be sure to establish personnel safety before attempting for fight any fire. A fire alarm pull box is located at the north end of the c-wing basement hallway. Fire extinguishers are located in the service corridor, the gowning room, and the yellow room. Before using these dry chemical ABC extinguishers, especially in the cleanroom since the powder will clog the HEPA filters, be sure it is appropriate for the type of fire being fought (see the label on the extinguishers).

Be safety conscious of potential fire starters in the cleanroom. Keep combustibles away from hot plates and heating elements in various equipment such as the evaporator, BioRad, CVD, etc. Flammable chemicals should always be stored in approved containers and in the appropriate flammable cabinets. Remember that acetone and methanol are flammable and should never be heated on a hot plate. Waste flammable liquids should be poured into proper containers and not left to evaporate in an open beaker.

A.5 Supply Storage Inside the Cleanroom

General use consumable supplies such as gloves, wipes, beakers, etc., are located in the drawers situated throughout the cleanroom, typically near the areas where they are frequently used. Chemicals commonly used in the cleanroom must be stored in

appropriate locations according their individual properties. Each of these locations has specifically assigned chemicals as listed below. **Do not mix and match chemical storage locations, as they are selected on the basis of safety.** When any supply runs low, replacements may be found in the consumable stock locations outlined on the next page.

White Room Fume Hood

- Working surface: 4 liter solvent waste bottle, squeeze bottles for DI H_20, acetone, methanol, and the acid & base neutralizers.
- Bottom-left doors: compatible acids (HCl, phosphoric, sulfuric, Br, HBr) well separated.
- Bottom-right doors: compatible bases (NH_4OH) and Polaron dry chemicals (in tub).

Yellow Room Fume Hood

- Working surface: 4 liter solvent waste bottle, squeeze bottles for DI H_20, acetone, methanol, and the acid & base neutralizers.
- Exhausted Acid Cabinet (bottom right): photoresists, nitric acid, and concentrated HF (both in individual Nalgene boxes for primary containment).
- Under sink (bottom left): Buffered HF in individual Nalgene box for primary containment.

Yellow Room Below the Corner Sink

- Photoresist developers.
- C-20 primer and its waste bottle.

Yellow Room Flammable Cabinet

- 4 liter acetone and methanol bottles for refilling the squeeze bottles.
- TCE and its waste bottle.
- Chlorobenzene and its waste bottle.

Refrigerator/Freezer in Service Corridor

- Refrigerator: Hydrogen peroxide (H_2O_2).
- Freezer: PI-2555 polyimide and VM-651 adhesion promoter.
- Use the pass-through to transport chemicals into and out of the cleanroom.

A.6Consumable Stock Locations

In general, frequently used consumables are located in the drawers or in the chemical cabinets throughout the cleanroom, usually close to the area where they are typically used. Extra supplies are located either in the gowning room or in the service corridor. **When using the last of an item in the cleanroom, go to its storage area and obtain a replacement.** If taking the last of an item from storage, make a note of the item (physically write it down), and be sure the Cleanroom Manager knows that it needs to be replaced. This should be done both for the general supplies and for the chemicals. If unable to locate an item, or if some other supply should be added to the general inventory, consult the Cleanroom Manager.

Small Flammables Cabinet in Service Corridor

- Acetone
- Methanol
- Trichloroethylene
- Chlorobenzene
- Xylene
- C-20 Primer
- Empty bottles for hazardous waste collection

Large Flammables Cabinet in Service Corridor

- Acids: HF, B-HF, nitric, sulfuric, phosphoric, HCl, bromine, HBr
- Bases: ammonium hydroxide, developers
- Acid and Base Neutralizers

Small cabinet in the gowning room

- Apparel: gloves, suits, hoods (in closet), and protective arm sleeves
- Containers: 50 ml & 250 ml Fluoroware beakers, specimen containers, Petrie dishes
- Lithography goods: syringes & filters, pipettes, microscope slides & cover slips
- Cleaning stock: Crew Wipes (large), Tex Wipes (4x4), cotton swabs
- Miscellaneous: filter paper, cleanroom paper, polishing paper, crystal bond, etc.

Large "J" cabinet in the gowning room

This is an overstock cabinet, and during normal cleanroom operations it is to remain locked. The Cleanroom Manager or a trusted assistant will have the key and be able to restock the smaller cabinet when notified that supplies are running low. Do not attempt to get supplies from this large cabinet.

A.7 Exiting the Cleanroom

Before leaving the cleanroom, *each and every time*, make sure the following items have been taken care of:

- DI H_20 is off in both hoods and in the corner sink (running the DI H_20 overnight will saturate the filters and result in a costly, premature replacement).
- Refilled supplies that are low or out, *including* the squeeze bottles.
- Acetone/methanol waste beakers emptied into 4 liter waste bottles.
- Fume hood sashes lowered below their maximum heights, and fume hood lights off.
- Photoresist spinner cleaned and glove box ports closed.
- Valve(s) for applying compressed air to the mask aligners off.
- All equipment in its idle configuration.
- All counter tops, inside of the hoods as well as elsewhere, wiped clean (no sticky neutralizer stains or puddles of unknown liquids left behind).
- Turn off the lights, especially in the yellow room, if you are the last one out at the end of the day or if nobody else remains and you will not be back that day.
- Make sure both combination-lock doors are locked and not set in the pass mode.

A.8 EQUIPMENT

This section provides details and operating procedures for various pieces of equipment used throughout the cleanroom. The information for any given piece of equipment may range from a simple outline of operational steps to a thorough discussion of the procedures. In many cases, there exists separate manuals for the equipment provided by the manufacturer. There also may be folders or binders containing information on specific equipment. This extra documentation is currently located in C-

17; there is a partial bookcase dedicated to cleanroom manuals as well as to catalogs for supplies typically used in the cleanroom.

Once again, it is important to note that the following information is not to be a substitute for appropriate training in the operation of the cleanroom equipment. Those authorized equipment users wishing to print out select pages of process steps for use as a guide during operation may feel free to do so. Be sure, however, that the pages are printed on cleanroom paper (found in the gowning room), because regular paper is *not* allowed inside the cleanroom. Many pieces of equipment already have laminated procedures located near them inside the cleanroom. These may be duplicates of the information contained here, or they may be more concise outlines of process steps. Misuse of any equipment, or operation by an uncertified user, can result in the loss of all cleanroom privileges. Any additional questions concerning the equipment should be directed to the Cleanroom Manager.

Guidelines For Appropriate Fume Hood Use

1. Be courteous of other users, and conscientious of *their* safety as well as your own.
2. ***Always* clean up after yourself**; seek assistance if you spill a chemical and are unsure of how to safely clean it up and dispose of it.
3. Keep all chemicals inside the hood (never carry open chemical containers around the cleanroom), and never raise the sash above the indicated height.
4. Check to make sure the drains (both inside the hood and at the floor behind the hood) are working properly before starting.

5. When using solvents:
    - Acetone and methanol waste can be collected in the 500 ml glass beaker; empty the beaker into the 4 liter waste bottle whenever 150 ml is collected, or when finished.
    - TCE waste must be collected in a *separate* 500 ml glass waste bottle.
    - Chlorobenzene is only to be used in the yellow room hood, *and its waste must be collected in its own, separate 500 ml glass waste bottle.*
    - **NEVER DUMP SOLVENTS DOWN THE DRAIN.**
6. When using acids and bases:
    - Keep acids and bases separated.
    - When mixing solutions, always pour the acid or base into the water.
    - Collect used acids or bases in the 500 ml Teflon beakers for neutralization.
    - When neutralizing, *always use the pH meter*, adding neutralizer until the pH of the solution is between 6 and 8.
    - When dumping neutralized solutions down the drain, be sure to flow lots of *city* water down with it (several gallons for 500 ml).
7. **LABEL ALL SOLUTIONS** (chemical names and concentrations, user name, date & time) whenever walking away from the hood for any reason, especially when leaving the cleanroom; *this is important for the general safety of you and other cleanroom users.*
8. When finished working in the hood, do each of the following:
    - Be sure all acids/bases have been properly neutralized and disposed.

- Empty any solvent waste into the appropriate bottle, making sure the cap is on tight.
- **Be sure the water faucets, ESPECIALLY THE DI H_20, are OFF.**
- Take a 4x4 Tex Wipe, wet it with propanol or methanol, and wipe down all of the working surfaces inside the hood (*make it cleaner than when you started*); when cleaning the Plexiglas shields, use only DI H_20.
- Be sure the sash is at or below the maximum safe height.
- Turn OFF the hood light.

E-Beam Evaporator Procedure

The evaporator is one of the oldest pieces of equipment in the cleanroom, but it is still very functional and provides good metal films. Users must exercise care while operating this machine and should be observant to any anomalies, such as increased pressures or pump times (indicating problems with the vacuum) or increased e-beam powers (indicating problems with the source material, the controller, or the e-beam itself). Always check to be sure the cooling water is flowing (about 1.5 gal./min) and the diffusion pump is running fine, and watch to be sure the automatic valve sequence operates properly. If any problems are encountered which the user is unfamiliar with, *immediately* contact the Cleanroom Manager or other qualified person for assistance. The following evaporator procedure is usually run after a chlorobenzene photolithography process and a native oxide surface etch using the plasma asher and B-HF.

1. **Sign in the evaporator log book** (make sure it is not already being used).

2. Make sure the cooling water is running at about 1.5 gal./min. Push the STOP button on the Automatic Valve Sequencer. The Hi-Vacuum gate valve below the bell jar should close and then the Air Release valve should open to vent the bell jar using N_2 gas.
3. When the VENTED light comes on (after several minutes), raise the bell jar by flipping the HOIST switch to the UP position; the bell jar will stop automatically. Then return the switch to its median OFF position.

NOTE: Always wear gloves while working inside the evaporator bell jar and handling its sample holder, source crucibles, etc.

4. Remove the sample holder and copper heat sink disk, and rotate the source selector knob to check that all the necessary sources are loaded in the source holder. If a source needs to be changed, it is recommended that an arm sleeve (to keep your suit clean) and a dusk mask be worn. **Be sure to place removed crucibles in their properly labeled storage slots, and insert crucibles ONLY in their designated positions in the source holder.** This is to make sure the identity of the metal in each crucible is maintained and not confused. Then rotate the selector knob so that the desired initial source is in the evaporating position.
5. Verify that the rate monitor crystal is functioning by pushing the START button on the Deposition Rate Controller twice, and wait for the XTL VERIFY message to disappear and the controller to start as normal; then push the STOP button on the controller. If the crystal fails or is below 70%, replace it (consult a qualified individual if unsure how to do this).

6. Mount sample(s) on the sample holder, and place the holder, with heat sink on top of it, in the evaporator. Be sure both shutters are in their closed positions.
7. Lower the bell jar by holding the HOIST switch in the DOWN position until it is firmly seated on the base-plate; then release the HOIST switch back to its OFF position.
8. Push the START button on the valve sequencer. The Air Release valve and Foreline valve should close and the Roughing valve open. The mechanical pump will rough the bell jar down to a set level (below 50 mT), and then the sequencer will close the Roughing valve and open the Foreline valve and the Hi-Vacuum bell jar gate valve. Users should monitor this to be sure everything proceeds normally.
9. **LET THE EVAPORATOR PUMP FOR TWO HOURS BEFORE PROCEEDING.** For critical evaporations, where contamination is a serious issue, let it pump overnight. Turn ON the ion gauge; typical pressures are in the $5x10^{-6}$ torr range.
10. Fill the small LN_2 dewar (open the valve before unscrewing the top to relieve any pressure). Wipe down the dewar, especially the wheels, before bringing it back into the cleanroom.
11. Make the appropriate LN_2 dewar connections: dewar nozzle to the rubber hose on the back of the evaporator, and N_2 gas bayonet to the dewar pressurization connector. Open the LN_2 valve on the dewar all the way, then back closed one full turn. The dewar should pressurize to around 3 psi; this should be preset so that no adjustment is necessary.

12. Start the LN_2 flow into the LN_2 trap by flipping the LN_2 Level Controller switch to AUTO. The light should come on and LN_2 should be heard flowing into the trap. ***Let the system continue to pump for another 30 minutes.*** Typical pressures are $1x10^{-6}$ torr or less.
13. Turn on the MAIN POWER supply breaker for the e-gun, and check that all of the interlock lights come on. *If not, notify the Cleanroom Manager immediately and do not attempt to fix the problem alone.*
14. Set the crystal monitor for the proper type of metal (using Menu 2 on the Rate Controller).
15. Check to be sure the sample and crucible shutters are closed (covering their namesakes).
16. Push the HIGH VOLTAGE ON button next to the breaker switch on the e-gun power supply.
17. Push the START button on the Deposition Controller twice, and once the crystal has verified push MAN to place it in manual mode. The rate monitor and time should still be running, but the controller itself will not be trying to crank up the e-beam power (which is not tied to this controller anyway).
18. Slowly turn up the emission current by turning the GUN 1 knob on the Remote Gun Control Unit to the 10-15% range on the scale; the filament under the crucibles should be lit.
19. Open the crucible shutter, and, while looking inside the bell jar, use the LONG and LAT control knobs on the remote unit to position the beam in the center of the crucible; use the SWEEP control knobs to adjust the extent the beam sweeps across

the crucible. A nice even sweep, covering the source material and not hitting the crucible, is desired. Forgetting to sweep the beam may result in a hole being bored through the metal and, eventually, through the crucible (that would be a bad thing). The beam is typically left in an acceptable setting, but should be checked and adjusted as needed during every evaporation.

20. While monitoring the deposition rate on the controller, slowly increase the current to the desired rate (typically 5 to 15 Å/sec and 20 to 30% on the GUN 1 scale). Be sure to evaporate at least 100 Å of the metal (50 Å of Au) to remove any surface contaminants before opening the shutter for the actual deposition; note that the thickness scale reads in kÅ.
21. Open the sample shutter slowly; **do NOT bang it on the glass bell jar**. Evaporate until the desired film thickness is obtained on the monitor (GUN 1 may be adjusted during deposition to change the rate and slowly approach the final thickness for increased accuracy).
22. Close the sample shutter and slowly reduce the emission current to zero.
23. Push the STOP button on the controller.
24. If additional metal layers are desired, wait *at least* 5 minutes for the crucible to cool, and then rotate the source selection knob to the position of the next source crucible. The substrate heating lamp may be used to aide in seeing the crucible position inside the bell jar. Do this by flipping the heater power switch ON and slowly turning the knob to increase the lamp current until the crucibles are visible (typically about 30%). Once the crucible position is set, slowly turn down the lamp current and turn OFF the

power switch. Do not leave the lamp on long, as the extra heat may cause more contaminants to move around the bell jar.

25. Repeat steps 14 through 24 until all required metal layers have been deposited.
26. Push the HIGH VOLTAGE OFF button, and turn OFF the e-gun power supply breaker. Turn OFF the LN_2 controller, close the LN_2 dewar valve, and *turn OFF the ion gauge.*
27. Allow the system *and ion gauge* to cool for *at least* 30 minutes before venting the bell jar
28. Push the STOP button on the valve sequencer (the same actions should occur as before).
29. When VENTED, raise the bell jar as before (step 3).
30. While wearing gloves, remove samples; then put the holder and heat sink back in position.
31. Lower the bell jar as before (step 7). Push the START button on valve sequencer, and monitor process to be sure it runs smoothly. *Always leave the system under vacuum.*
32. **Sign out of the log book**, recording all pertinent information (including sponsor if Au used).

Karl Suss Mask Aligner Procedure

The two Karl Suss mask aligners, the new one on the left and the older version on the right as facing them in the yellow room, are essentially identical. Extreme care must be exercised when using either aligner, as these are delicate, expensive pieces of equipment. Only thoroughly trained, authorized cleanroom users should operate them. Even once properly trained, any time a question arises while using an aligner, whether it is an uncertainty of procedure or an unusual occurrence, an operator should consult the Cleanroom Manager or other knowledgeable user just to make sure the equipment will not be damaged. As usual, the following procedures are not meant as a substitute for authorized training.

1. The first person to use the aligner on a given day must power up the entire system: Turn on the power strip controlling the mask aligner to be used (the new aligner power strip is below its table; the old aligner power strip is on the tabletop behind the new aligner). Push the POWER button on the front of the aligner (the red LED should come on), and flip on the POWER switch on the UV lamp controller box. The lamp controller will go through a self test process and the display will read RDY if all passes. Push the START button on the controller, and the lamp should fire and begin to warm up, flashing COLD while doing so. When it is warm a numerical power reading should appear on the display. The aligner is generally operated in the constant intensity mode CI2, so press that pad on the controller to activate it, and press DS to toggle between the base power (around 275 W) and the activated power (in mW; should read 0.0; will read in the teens during exposure) on the display corresponding to the CI2 channel. If something goes wrong in this long Step 1 (such

as the self test failing or the lamp not firing), turn the POWER off and then on to try again; if the failure persists, consult the Cleanroom Manager for assistance.

- If the lamp is already on (meaning someone used the aligner earlier in the day), simply push the red POWER button to turn on the aligner.

2. Turn ON the valve to activate Compressed Air flow to the appropriate mask aligner (both valves are located between the two aligners). The cleanroom does not have an unlimited supply of high pressure, so this should be on only when the aligner is in use.
3. Clean the photo-mask to be used by rinsing it in acetone and methanol (properly collecting the solvent waste) and then blow drying it with N_2 gas. Always hold the photo-mask by its edges, and never scrub the mask, as this may scratch or damage the pattern.
4. Place the mask, film side up/glass side down, on the mask holder plate, and press VACUUM MASK to secure it. Insert the plate, with the mask down, into the stage and tighten the holding screws.
5. Place the sample on the chuck, and slowly slide it under the mask and microscope; be sure there is enough clearance so the sample and/or mask are not damaged. Move the microscope around, by pressing the buttons on the microscope handle on the left to allow free movement, until it is above the sample. Turn the MICROSCOPE ILLUMINATION knob to adjust the brightness of the light (typically set around 5 on that scale).

6. Slowly rotate the contact lever (bottom left side of aligner) toward the back of the aligner while using the microscope to watch a corner of the sample for premature contact with the mask. (Contact is visually indicated by interference fringes emanating from the point of contact between the mask and the photoresist on the sample; this usually occurs on a corner or edge because the resist is thicker there.) Premature contact is when visual contact occurs before the lever reaches all the way back and the blue CONTACT light come on. If this occurs, *first* rotate the contact lever all the way toward the front, then turn the thickness adjustment knob on the bottom front of the aligner to lower (clockwise) the sample stage as necessary. If visual contact does not occur even after fully rotating the lever to the back, rotate it all of the way to the front and use the thickness adjustment knob to raise (counter clockwise) the stage. Continue this process, rotating the contact lever back and forth and turning the knob, until the mask/sample contact is visually observed at the same time as the blue light coming on. NOTE: if the chuck stage is too high, rotating the contact lever all the way to the back can result in a broken sample AND mask; use caution.
7. Select a contact mode:
    - Vacuum Contact (HP): A vacuum is placed between the mask and sample immediately before exposure. This gives the highest possible resolution since the sample is literally sucked into contact with the mask. An edge bead removal must be used beforehand, otherwise this will cause the sample to bend/break under vacuum.
    - Standard contact (ST):

- Hard Contact: Achieved by lighting the ST button only. N_2 is used to press the sample against the mask, so this mode is similar to HP except the exerted pressure is not as great, resulting in less resolution and in a smaller chance of breaking the sample. This mode is good for cases where the edge bead exists but high resolution is still important.
- Soft Contact: Achieved by lighting the ST button and the SOFT CONTACT light. The substrate and mask are kept in contact with mechanical pressure only. This offers lower resolution, but is the safest and gentlest on the sample.

Align and expose the sample to the UV: If this is the first exposure for the sample, alignment is not critical, but rather done to be sure the sample is in a desired position. If this is a subsequent mask level, alignment between the mask pattern and the sample pattern is key.

- Pull the Separation lever (located on the left near the contact lever) forward to introduce a space between the mask and sample, thus allowing the sample to be moved without damage. The green SEPARATION light should come on.
- Use the X, Y, and Rotation micrometers to adjust the sample until it is properly aligned. Do NOT crank any of these dials to their extreme positions; the sample chuck should always be slid out (after rotating the contact lever to the front) and the sample manually moved to accommodate any large position adjustments that may be necessary.

- Once aligned, push the Separation lever back until the CONTACT light comes on. Then check the alignment again. Repeat as necessary until satisfied with alignment.
- Check the exposure time, and set it as desired for the sample.
- Sit back from the microscope (so as to avoid being hit by it when it moves forward for exposure), and press the EXPOSE button.

8. After exposure, slowly rotate the Contact lever to the front until it stops. Pull out the chuck and remove the sample to develop it. If there are more samples to expose, repeat the above for each one.
9. When done with all samples, re-adjust the positioning micrometers to their central settings, and push the chuck back in.
10. Unscrew the holding screws and remove the mask plate. Set the plate down, *then* turn off the VACUUM MASK button and remove the mask. *Never* turn off the vacuum while the plate and mask are still in the stage.
11. Turn OFF the Compressed Air valve.
12. Press the POWER button to turn off the power to the aligner. If it is the end of the day, or if no others users will be using the aligner that day, then turn off the POWER on the UV lamp controller and turn OFF the appropriate power strip.
13. Clean the photomask by rinsing it with acetone and methanol, and blow drying it with N_2 gas, to remove any resist or other contamination before putting it away.

Plasmaline Asher Operational Procedure

1. Open the oxygen cylinder in the service corridor and set its regulator to 10 psi.
2. **Sign in the log book by the Plasmaline.**
3. Turn on the mechanical pump; open the O_2 line valve at the inner cleanroom wall.
4. Turn on the Plasmaline by pressing the AC ON button (STOP button should light).
5. Once the chamber is vented, open the door and load the sample onto the glass dish *(be sure to wear gloves while handling the sample and the dish)*.
6. Set the desired ashing time (in minutes) using the thumb wheels.
    - Typical time for sample cleaning before metal evaporation is 5 minutes.
7. Place the MODE switch in AUTO, and the METER switch in PRES.
8. Press START to begin the run; the chamber should begin to pump down.
9. When the pressure reaches a low enough value (around 0.05 Torr), typically in 10-20 minutes, the system automatically applies the RF power to the electrodes and the RF ON button will light up.
10. Set the RF power to the desired level by switching METER to FWD and varying the PWR ADJ knob.
    - Typical power is 80-100 Watts for sample cleaning before metal evaporation.
11. Switch METER to REF and minimize the RF reflected power (should be < 10 W) by adjusting the TUNING knob.
12. Check for proper O_2 flow by a) adjusting the left hand flow controller on top of the Plasmaline until the steel ball is at 100 sccm, and b) switching METER to FLOW and turning the FLOW ADJ knob until the needle is somewhere between 1.5 and 2 on the flow scale.

- **Note**: If the previous user ran the system at the desired power level, steps 10-12 may not be necessary; cautiously skip them at your own discretion.

13. When the time is up and the ashing is completed, the RF ON light will go off. Allow the sample to cool 5-10 minutes, then press STOP. Once the chamber has vented, open the door and remove the sample (while wearing gloves).
14. Shut down: close the door, press AC ON to toggle the system off, switch off the mechanical pump, and **fill out the log book completely**; close the O_2 line valve and the O_2 cylinder.

BioRad Ohmic Contact Alloying Furnace Operating Procedure

1. **Completely fill out the log book.**
2. Clean the sample and perform a native oxide etch (if using eutectic alloys and it will not damage the sample).
3. Turn ON the MAINS switch; set BYPASS/RESET switch in its neutral position.
4. Open the exhaust valve.
5. Set etch flow to mid-scale of the gauge to flow N_2 through the reaction chamber.
6. Cut <u>new</u> contacts (fresh cuts on all sides) and place them on the corners of the sample. (Note: Skip this step if alloying evaporated metal contacts.)
7. Unscrew the reaction chamber from the base and *carefully* lift it off; make sure to not hit the microscope. (Note: *<u>Always</u> wear cleanroom gloves while handling the chamber and while cutting the contacts.*)
8. Place sample on the heating stand and screw the reaction chamber into place. (Note: If using the graphite cap, get it out of the N_2 box and *carefully* place it over the glass heating stand before situating the sample.)

9. Let the chamber purge for 3 minutes with the N_2 flow.
10. Enter the desired temperature set point (using the arrow keys) and the desired alloying time (using the thumb wheel switches).
    - Note: The set point temperature is displayed on the *lower* LEDs, and the measured temperature is on the *upper* LEDs. The digital time displays seconds (right two digits) and minutes (left two).
11. Begin alloying by turning the HEATER switch ON.
12. At the end of the alloying cycle the alarm sounds. Turn OFF the HEATER switch and push the toggle switch to RESET to silence the alarm.
13. Let the sample cool to below 75EC before removing it. (Note: If the graphite cap was used, return it to the N_2 box.)
14. Shut down:
    - Turn off the N_2 flow and close the exhaust valve.
    - Be sure to secure the reaction chamber back on its base.
    - Turn OFF the MAINS switch.

Melting points of some relevant materials:

Eutectic Alloy	Melting Point (EC)	Element	Melting Point (EC)
InZn (p-type)	143	In	157
InSn (n-type)	117	Sn	232
AuZn (p-type)	642	Zn	420
AuGe (n-type)	356	Au	1065
		Ge	937

Polyimide Cure Furnace Operating Procedure

1. Open exhaust valve and nitrogen gas inlet valve; set N_2 flow controller to 4-5 sccm.
2. Remove the flange and place the sample on the stage inside the chamber; close the chamber by bolting the flange back on, and tightening the four nuts finger tight. *Always wear gloves while loading and unloading the sample and working inside the chamber.*
3. Flip the HEATER POWER switch to ON.
4. Press START on the Omega temperature controller to begin cure cycle.
    - Standard polyimide cure cycle: 1 hour ramp to 200EC
      4 hour soak at 200EC
      1 hour ramp to 25EC
    - To change the ramp cycle, consult the Omega controller manual.
5. After the completion of the cure cycle:
    - Remove sample and replace the flange.
    - Flip HEATER POWER switch to OFF.
    - Set N_2 flow controller to zero.
    - Close N_2 source valve and the exhaust valve.

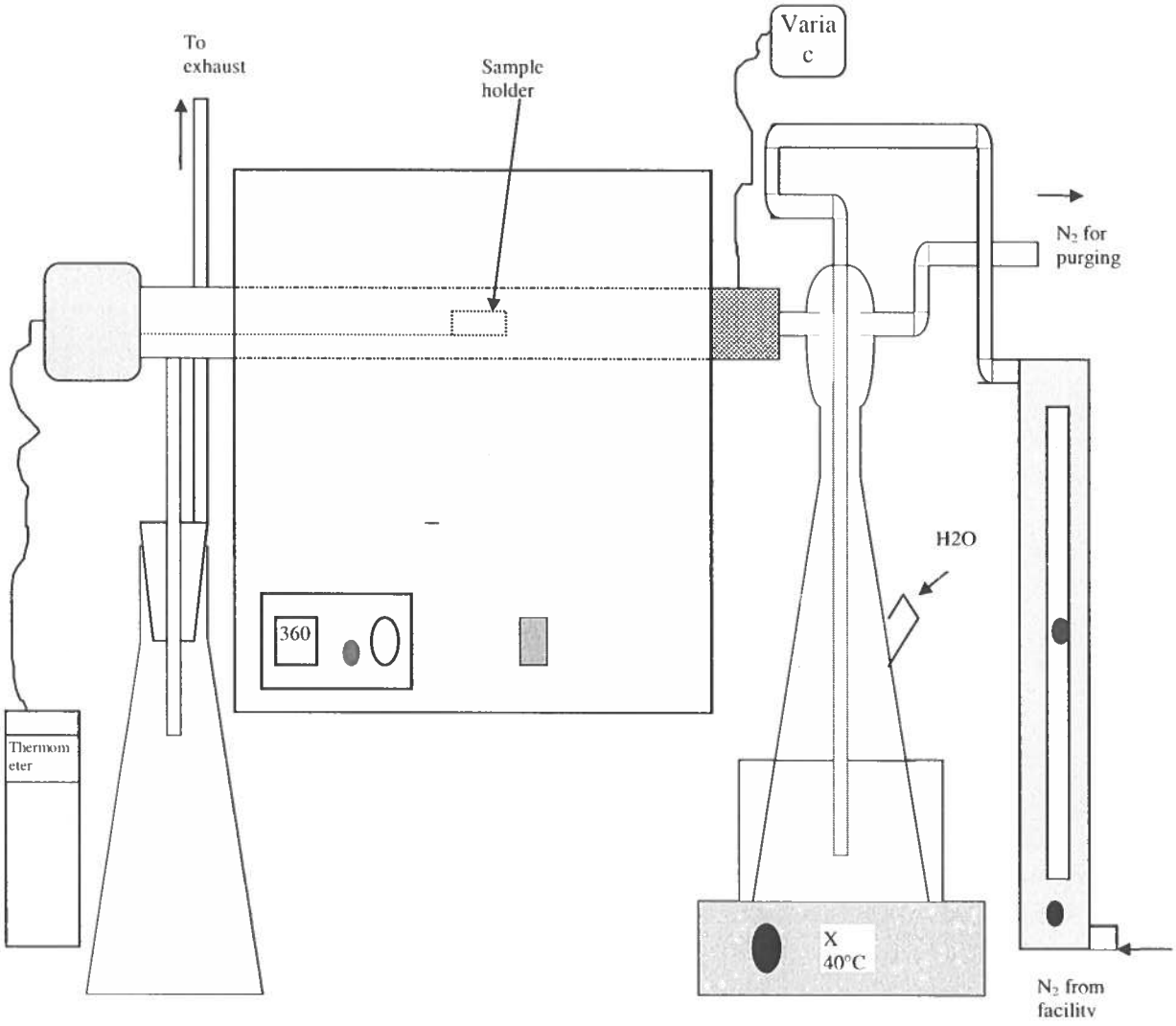
Oxidation Furnace Operating Procedure

The oxidation furnace is setup using a furnace with a quartz tube that allows water vapor to flow through the furnace. The water vapor is provided by heating the water in a flask at 75°C on a hot plate. N_2 will bubble through the water to bring the vapor into the furnace. The inlet tubing has to be heat tape at 75°C to prevent condensation of the vapor before entering the furnace. Please refer to the diagram of the oxidation furnace setup on the next page.

Detail instructions are as follow:

1. Connect the exhaust at the left side of the furnace outlet to collect the condensate from the oxidation process.
2. Do not connect the tube fully into the furnace, this might make it very difficult to be removed after the furnace is being heated up.
3. Fill the flask and the bath with DI water. Make sure that the water level in the flask and in the bath is sufficient for the oxidation process. The water level for the bath should be higher than the water level in the flask to ensure even heating of the water.
4. Adjust the N_2 flow meter to 90 sccm. You will see bubbles in the flask. Adjust the pressure regulator if the pressure is too low or if the flow fluctuates too much.
5. Turn on the TC thermometer for the sample.
6. Turn on the VARIAC for heat tape at the inlet of the furnace.
7. Turn on the furnace power switch. Press the red setpoint button to view the setpoint, furnace setpoint should be at 360°C.
8. Turn on the hot plate. Setting on the hot plate is around 4.5 for temperature of 75°C.
9. Allow the furnace to stabilize for one hour before loading the sample.
10. To **LOAD** sample, detached the exhaust from the tube, remove the tube on the left of the furnace slowly, place your sample on the metal holder and insert the holder back into the furnace. Be careful so that you do not drop your sample into the quartz tube during loading.
11. Connect the exhaust back to the tube after inserting the tube into the furnace.
12. To **UNLOAD** sample, detached the exhaust from the tube, remove the tube on the left of the furnace slowly, remove your sample on the metal holder. Insert the holder back into the furnace. Be careful of the sample, it is hot and might stick to texwipe. Place sample on micro slides.
13. After the oxidation is completed, please follow the turn off sequence below:
    - Turn off the Hot plate
    - Switch off the furnace
    - Switch off the VARIAC
    - Switch off the TC thermo
    - Turn off the N_2 supply
    - Disconnect the exhaust

Diagram for the Oxidation Furnace:



Appendix B

VCSEL FABRICATION

Detailed recipes including times, temperatures, chemical brands and inspection images

Mesa Etching,

Sample preparation,

A detailed recipe for sample preparation including temperatures, times, chemical brands and some inspection images are listed below.

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Spin on positive tone photo resist Shipley 1818 6000rpm/30sec
4. Soft bake for 2 min at 95C
5. Clean the edges of the sample using acetone.
6. Align Mesa mask and expose for 8-11 sec at 15mW/ cm^2
7. Developing for 45-50 Sec using AZ400K: H2O (1:4)
8. Post –bake sample for 2 min at 120C. ***Optional***
9. α-Step & Microscope camera

   (Expected thickness~ 2 μm thick film)

Allow samples to cool down after each baking step before proceeding with the next step

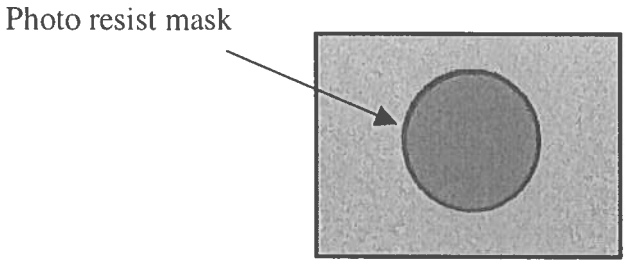


Figure B.1 Top view for the photo resist mask with a ~ 2 μm thick

10. Hard Bake at 120C for 2 min.

This step is necessary to harden the photo resist enough so that it will withstand the dry etching process

11. Microscope camera

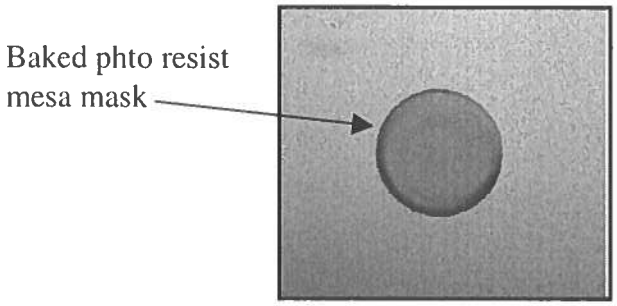


Figure B.2 Top view for baked photo resist mask

Dry Etching,

1. Loading the sample in to the chamber
2. Etching for about 3 min & 50 sec. with 10 sccm of Argon gas and 2.5 sccm of Chlorine gas
3. Microscope camera

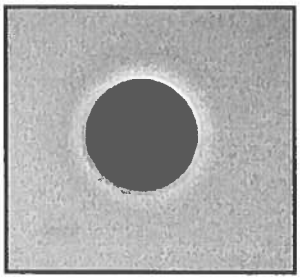


Figure B.3 Top view for photo resist mask after etching

4. Striping the photo resist,

1.Hot DI water path for 5 min

2. 6 min UV

3. Hot AZ400K developer in an ultra sonic path.

4. α-Step & Microscope camera

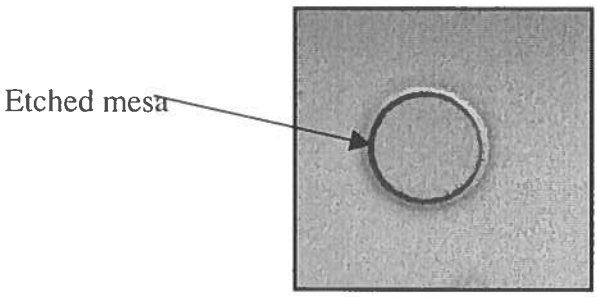


Figure B.5 Mesa top view

Wet Oxidation

1.Set the furnace Temp. to 420 C

2. Stair = 3 and Heat = 8.5 ⟶ Water Temp. (75-80) C

3.Leave the Oxidation Furnace to stabilize for 1 hour before loading the sample

4. Sample Temp. $(410C)_{t=0}$, $(420C)_{t=20\ min}$

5. Oxidation time: 20 min

6.Microscope camera [a Golden or Green ring around the top of the mesa should be clearly seen]

7.Oxide Investigation using IR source (Mask aligner) & using SEM lab,

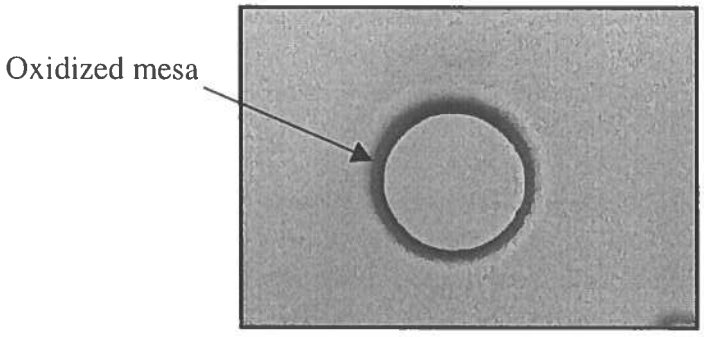


Figure B.6 Oxidation Furnace

Ohmic Contacts

1.Cleaning with acetone, methanol and DI

2.Per- bake for 2 min at 120C

3.Spin on negative tone photo resist ma-N 490 2800rpm/30sec

(Expected thickness~ 7.5 μm thick film)

4.Bake for 10 min at 95C

5.Clean the edges of the sample using a blade

6.Align Top contact mask and expose for 1:30 min at 9.6mW/cm^2, which gives an exposure dose of 864-mJ/ cm^2 for 2.5 μm

7.Heat the developer ma-D 332S until it's temperature is between 20-25 C then develop the sample for [45-60] Sec with its full strength

8.α-Step & Microscope camera

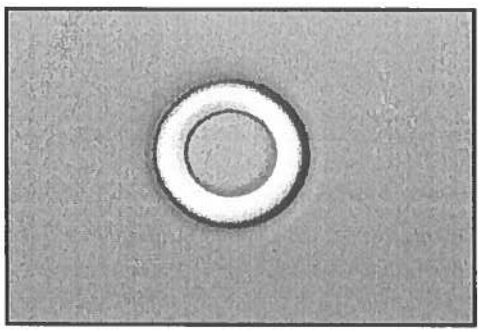


Figure B.7.a Photo resist mask for top contact

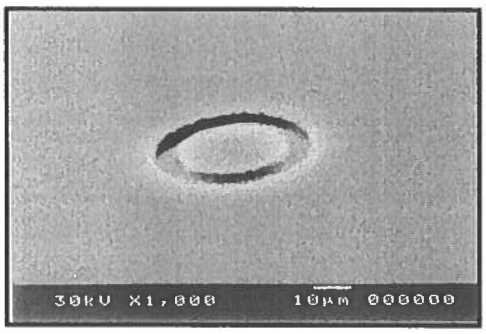


Figure B.7.b Photo resist mask for top contact

9.Plasmaline Asher 100W for [3 -5] min. Try to avoid this step since Plasma line Asher will damage the lift off profile for small mesas or you can try a lower power and shorter time

10.Microscope camera

11.Sample preparation procedure for lift-off:

Leave for 15 sec. in HCl / H2O = 1 / 1 solution for removal of oxide layer formed on the GaAs surface. Blow-dry with nitrogen gas. Mount in evaporator and pump down.

12.Evaporate Ni/Ge/Au/Ni/Au (150/330/600/150/70) Å

13.Lift off using acetone with an ultra sonic path

14.Microscope camera

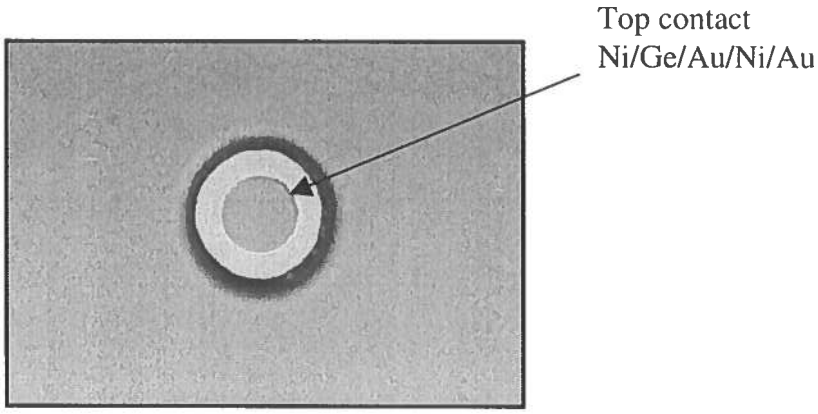


Figure B.8 Top contact after lift-off

Bottom contact (p-contact)

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Spin on negative tone photo resist ma-N 490 3000rpm/30sec (Expected thickness~ 7.5 μm thick film)
4. Bake for 10 min at 95C
5. Clean the edges of the sample using a blade
6. Align Bottom contact mask and expose for 3:20 min at 9.6mW/cm^2 which gives an exposure dose of 1900mJ/cm^2 for 7.5 μm

7. Heat the developer ma-D 332S until it's temperature is between 20-25 C then develop for 2:30 min with it's full strength
8. α-Step & Microscope camera
9. Plasma line Asher 100W for [6 -10] min.
10. Microscope camera

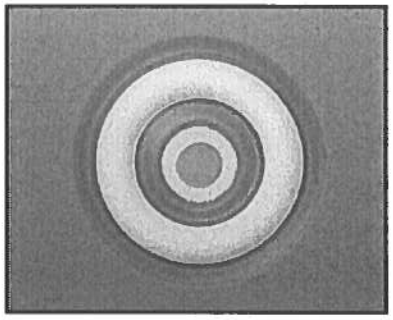


Figure B.9 Photo resist mask for bottom contact

11. Sample preparation procedure for lift-off:

Leave for 15 sec. in HCl / H2O = 1 / 1 solution for removal of oxide layer formed on the GaAs surface. Blow-dry with nitrogen gas. Mount in evaporator and pump down.

12. Evaporate BeAu/Ti/Au (1500~3000) Å
13. Lift off using acetone in an ultra sonic path
14. Microscope camera

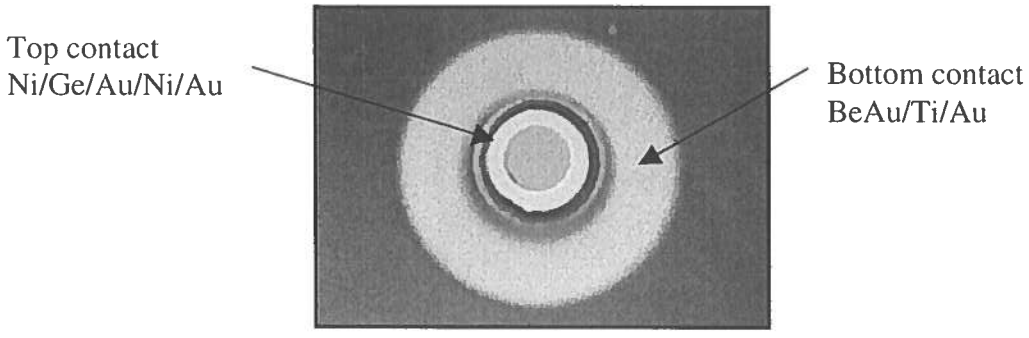


Figure B.10 Mesa with top and bottom contacts

15. Alloy at 420C for 30 sec. using the alloy furnace.

16. Microscope camera

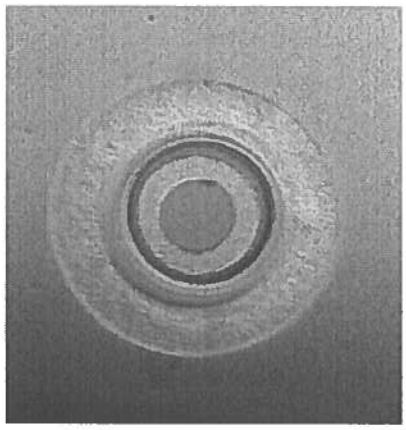


Figure B.11 Alloyed top and bottom contacts

Polyimide

HD-8000 Polyimide Photolithography

1.Cleaning with acetone, methanol and DI

2.Per- bake for 2 min at 120C

3.Apply VM-651 [0.5 ml VM-651: 100 ml DI H_2O]

4.Allow the puddle to stand on the wafer for 20 sec

5.Spin dry at 3000 rpm/30 Sec

6.To improve adhesion bake at (110-130) C for 1 min.

7.Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

8.Spin at 5000 rpm/30sec (final cured thickness~ 5 μm thick film)

9.Bake for 1:40 min at 115C [thickness ~7.5-8 μm]

10.Sample should be cooled to ambient temperature prior UV exposure(30 min) ,

Otherwise the cured polyimide will have sever crakes .see figure B.12

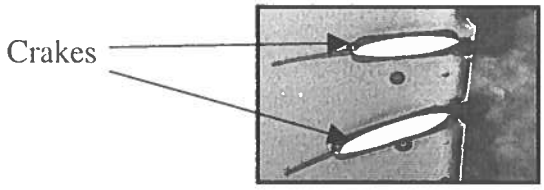


Figure B.12 creaked polyimide

11.Align Polyimide mask and expose for 25 Sec at 9.6mW/cm^2, which gives an exposure dose of 240mJ/cm^2

12.Heat the developer AZ400K: H2O (1:4) until it's temperature is between 20-25 C then develop for (1:10-2:20) min, use the microscope with UV filter to see exactly when the sample is fully developed. [Developed thickness 7.5-8 μm]

13.Rinse with DI H_2O 1000rpm/10 Sec

14.Spin dry for 3500rpm/10 Sec

15.α-Step & Microscope camera

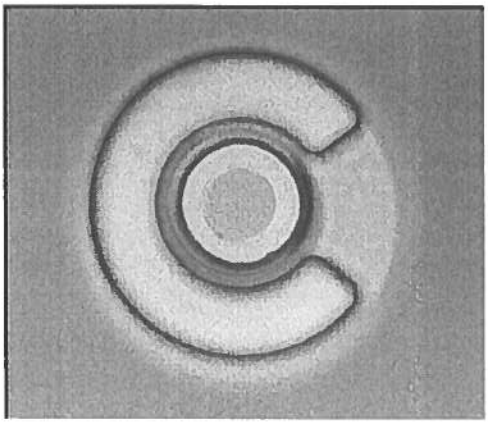


Figure B.13 Polyimide before curing

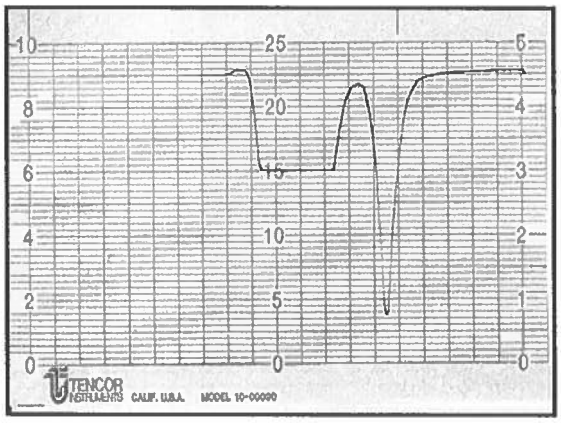


Figure B.14 Polyimide before curing
α-Step (scale at 100kA=10μm)

19.Cureing

Load into oven or furnace at 20C

- ❖ Ramp from 20C to 350C over 60 min period *(Furnace setting ~240C)*
- ❖ Hold at 350C for 30 min *(Furnace setting ~240C)*
- ❖ Substrate can be unloaded immediately or allowed to cool down.
- ❖ Thickness 6 μm with a brown color

20.Cured Ployimide testing

- ❖ Using the probe station, press using on of the tips on the polyimide surface .
- ❖ Note the craks shape.

Figure B.14 Polyimide after curing

21. α-Step & Microscope camera

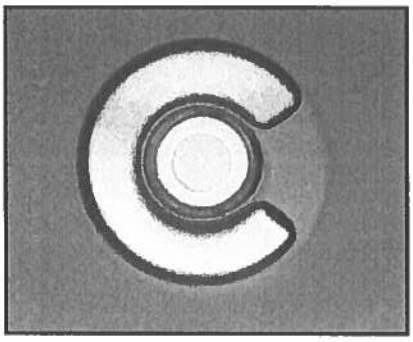


Figure B.15 Polyimide after curing

4.2.6. Metal Interconnection

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Spin on positive tone photo resist AZ 4400 4000rpm/30sec

4. Soft bake for 2 min at 95C
5. Clean the edges of the sample using acetone.
6. Align Mesa mask and expose for 22 sec at 15mW/cm^2
7. Soak in Chlorobenzene for 4 min; blow dry with N2 gas *(Don't rinse with DI H2O)*
8. Developing for 75 Sec using AZ400K: H2O (1:4)
9. Post –bake sample for 2 min at 120C. ***Optional***
10. α-Step & Microscope camera

(Expected thickness~ 4 μm thick film)

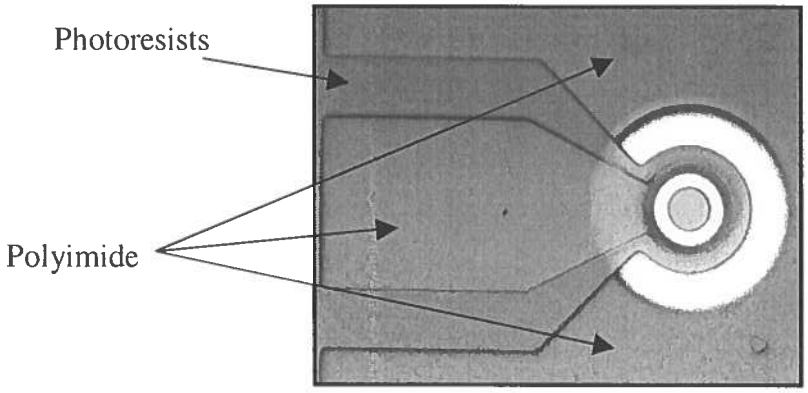


Figure B.16 sample after developing

10.Evaporation Ni/Au (200/3000) Å

(Total contact thickness = 0.32 μm)

11.Lift off using acetone with the help of an ultra sonic path.

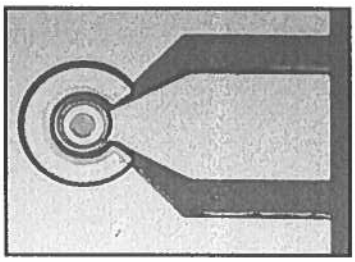


Figure B.17 sample after lift-off

Appendix C

Typical CSU Cleanroom Photolithography Processes

Typical CSU Cleanroom Photolithography Processes

The following are typical photolithography processes. They all use the General Photolithography Procedures just discussed, and each process is designed for a specific purpose or around a specific property of the sample or of the resist. The positive photoresist Shipley 1818 is the workhorse resist used in most of the CSU cleanroom applications. Film thickness values for the CSU spinner range from about 2.7 μm down to 1.9 μm for spin speeds from 3000 rpm up to 6000 rpm. Shipley SJR5440 and Hoechst Celanese AZ P4400 are also positive photoresists, with the difference being the process can result in thicker resist layers which may be useful for certain applications. AZ 5214-E is a negative photoresist. All of the above use the AZ 400K developer, mixed 1:4 with DI H_2O, except for the SJR5440 which requires the use of undiluted Microposit 453 developer.

General Shipley 1818 Mesa Etch Process

1. Prepare sample using the Clean and Mount Procedure.
2. Pre-bake sample for 2 minutes on the 120°C hot plate.
3. Spin on Shipley 1818 for 30 seconds at 6000 rpm (this gives about a 2 μm thick film).
4. Soft bake sample for 2 minutes on the 95°C hot plate.
5. Align and expose at 15 mW/cm^2 for 8-11 seconds (personal experience will dictate time).
6. Develop in AZ 400K: DI H_2O (1:4) for around 45 seconds .
7. Post-bake sample for 2 minutes on the 120°C hot plate.

Modification for Photoresist on SiO_2

When processing samples coated with a film of SiO_2, the use of an adhesion promoter is required. Photoresist cannot interact with the insulator, so the adhesion promoter is used to help the photoresist stick. The adhesion promoter used in the cleanroom is Microposit C-20 Primer. When needed, a small amount (20 ml) of pure C-20 is poured into a specimen container and placed inside the photoresist spinner box, and a pipette is used to apply it to the sample. Always label the container with "C-20 Primer," the date, and user name, and be sure the cap is placed *tightly* on the container when done. When the primer gets old (3-4 weeks) it may not be as effective, and should be collected in the C-20 Primer waste bottle. To apply the adhesion primer, insert the following steps into the general procedure above:

2.5a) Place sample on spinner chuck and cover with C-20; let stand for 5 seconds.

2.5b) Spin C-20 for 30 seconds at 5000 rpm.

AZ 5214-E Negative Photoresist Process

1. Prepare sample using the Clean and Mount Procedure.
2. Pre-bake sample for 2 minutes on the 120°C hot plate.
3. Spin on AZ 5214-E for 30 seconds at 3300 rpm (about 1.5 μm thick film; see table).
4. Soft bake sample for 1.5 minutes on the 95°C hot plate.
5. Align and expose at 9 mW/cm^2 for 20 seconds (personal experience will dictate time).

6. Post-bake sample for 45 seconds on the 120°C hot plate.
7. Flood exposure at 9 mW/cm^2 for 2.5 minutes.
8. Develop in AZ 400K : DI H_2O (1:4) for around 35-40 seconds.
9. Post-bake sample for 2 minutes on the 120°C hot plate (if required).

Measured spin data for AZ 5214-E photoresist

Spin Speed (rpm)	Thickness (μm)
3000	1.63
4000	1.41
5000	1.26
6000	1.15
7000	1.01

Shipley SJR5440 Process

1. Prepare sample using the Clean and Mount Procedure.
2. Pre-bake sample for 2 minutes on the 120°C hot plate.
3. Spin on Shipley 5440 for 30 seconds (use table below to obtain desire thickness).
4. Soft bake sample for 3 minutes on the 95°C hot plate.
5. Align and expose at 15 mW/cm^2 for 2+ minutes (personal experience will dictate time).

6. Develop in undiluted 453 developer for 2 to 3 minutes (").

Measured spin data for Shipley 5440 photoresist

Spin Speed (rpm)	Thickness (μm)
2000	7.0
3000	5.5
4000	5.0
5000	4.5
6000	4.0

AZ P4400 Process

1. Prepare sample using the Clean and Mount Procedure.
2. Pre-bake sample for 2 minutes on the 120°C hot plate.
3. Spin on AZ 4400 for 30 seconds at 5000 rpm (gives about 4 μm thick film; no other data available at this time).
4. Soft bake sample for 2 minutes on the 95°C hot plate.
5. Align and expose at 15 mW/cm^2 for 22 seconds (personal experience will dictate time).
6. Develop in AZ 400K : DI H_2O (1:4) for around 75 seconds (").
7. Post-bake sample for 2 minutes on the 120°C hot plate (if required).

It should be noted here that many of the exposure and development times may vary from those included in the above recipes. This is because photolithography is part art as well as being a science. Various parameters, from the conditions in the lab such as

humidity, to the age of the chemicals and the UV light source, to the type and topology of the sample, can affect the process to some degree. In some cases these recipes will work perfectly exactly as written (they were, after all, refined by multiple users over many years). However, there are no guarantees. These processes should be used as a baseline. From there, it is up to each individual user to do some experimenting, changing parameters, and to find a process that works well for the given sample set and research goals. It is also a good idea to continually monitor the results, and make adjustments along the way as conditions change.

Appendix D

HD-8000 Data sheet

Rev. 2

HD MicroSystems

Photodefinable HD-8000 Series
Positive Tone, Aqueous Developable Polyimide

Table of Contents

1. Introduction

The HD-8000 series product line was developed around an industry need for a polyimide that could be imaged and processed like common positive tone photoresists. HD-8000 and HD-8001 polyimides are positive-tone, aqueous developing, photodefinable polyimides developed for all passivation stress buffer and flip chip bonding applications. These products can be readily processed using standard I-line, G-line and broad band lithography tools and common TMAH-based developer tracks. HD-8000 series products utilize a newly developed, fully aromatic, polyimide backbone. Cured films have the corresponding thermal and mechanical stability associated with polyimide materials. New photopolymer technology was utilized to achieve pattern definition which greatly exceeds that of earlier-generation aqueous developing products. The resolution capability of HD-8000 and HD-8001 should meet or exceed the requirements of all contemporary semiconductor target applications.

2. Product Description

HD-8000 and HD-8001 are positive tone, self-priming photodefinable polyimide precursors that can be patterned to cleanly resolve micron-scale relief patterns with controlled size and side-wall profiles without the need for photoresist. Because of this unique combination of properties, HD-8000 reduces the number of process steps required for patterning polyimide overcoat layers. Its fine line resolution and inherent durability as a dry-etch mask make it ideal for most "single-mask" passivation stress buffer applications.

In a "single-mask" stress buffer process, the polyimide stress buffer layer or (secondary passivation layer) is also used as a resist layer to pattern the underlying silicon nitride primary passivation. HD-8000 has a cured film thickness range of 5 to 10 microns. HD-8001 offers finer resolution and has a cured film thickness range of 2 to 3.5 microns.

Key Features:

- Positive tone
- Process with positive resist developers
- High exposure sensitivity
- High resolution
- Wide process latitude
- Good room temperature (RT) viscosity stability
- Excellent cured film properties
- Good selectivity in dry etch processing
- Wide process latitude from soft-bake to exposure and exposure to develop

HD-8000 is supplied as a liquid coating and typically packaged in 1 or 4 liter high-density polyethylene or polypropylene bottles. The solution properties are shown in Table 1.

Table 1. Liquid properties (typical values)

Item	Condition	Units	HD-8000	HD-8001
Viscosity	25°C (E-type)	cPs	1500±100	350±50
Non-volatile content	200°C/1 hr +350°C/1 hr	%	38±1	32±2
Water content	Karl Fisher	%	<0.5	<0.5
Metal impurity	MIP-MS (Hitachi P-7000)			
Na		ppm	<1.0	<1.0
K		ppm	<0.5	<0.5
Cu		ppm	<0.5	<0.5
Fe		ppm	<0.5	<0.5
U		ppb	<0.5	<0.5
Th		ppb	<0.5	<0.5
Chloride*	Ion chromatography	ppm	<2	<2
Particles	LPC (Rion KL-01)	/ml	<5000	<5000

*Extracted from cured film

3. Storage and Availability

HD-8000 series products are formulated to provide 2–10 µm cured film thicknesses under nominal process conditions as described in Table 2. HD-8000 solutions should be stored in a freezer at –18°C upon receipt for long-term storage; room temperature (RT) stability is 2 weeks. Stored solutions should be allowed to warm up to room temperature before opening to avoid moisture condensation on the inside of the bottle. To avoid solvent loss, bottles should be kept tightly sealed when not in use.

4. Safety and Handling

During handling of HD-8000, adequate ventilation must be provided. Skin and eye contact should be avoided. Exposed areas should be flushed with water immediately. Solvent-resistant gloves, goggles and safety masks should be utilized; consult the individual product Material Safety Data Sheet (MSDS) for additional toxicity/health hazards information.

5. Processing

5.1 Clean Room Conditions

The processing of HD-8000 should be performed in standard clean room conditions under yellow light. Temperature and relative humidity conditions should be controlled for consistency (± 2.0°C, ± 2% RH) to obtain the best processing results.

5.2 Substrate Preparation

Substrates should be clean and dry prior to use. In some cases, oxygen plasma cleaning followed by a wet cleanup with an organic stripper solution such as Tokyo Ohka S-106 to remove trace organic contaminants is recommended during rework. (Trace organic contaminants can degrade adhesion to the substrate during processing or after curing.)

5.3 Spin Coating Process and Film Thickness

Nominal process conditions for HD-8000 and HD-8001 are shown in Table 2. The volume of solution dispensed should remain constant for each wafer to ensure wafer-to-wafer uniformity. Low spin speed and/or short spin times can impact film uniformity; the recommended spin speed range is 1,000-4,000 rpm. The recommended spin time is 30–60 seconds.

A spin speed curve for HD-8000 is shown in Figure 1. The standard deviation for a soft-baked film on an 8 inch wafer can be as low as 0.2 µm. The actual coating thickness obtained for a given set of spin coating conditions will depend on a number of parameters such as equipment type, wafer size, surface topography, ambient conditions and soft-bake conditions. Refractive indices together with Cauchy coefficients for measuring coating thickness are given in Table 3 for pre-cured and cured films of HD-8000. A film thickness reduction of approximately 15–25% can be expected after development; approximately 43–47% after final cure (as compared to original soft-bake thickness).

Table 2. Processing conditions

Process		Units	Target Thickness HD-8001		Target Thickness HD-8000		
			2 microns	3.5 microns	5 microns	8 microns	10 microns
Coating	Pre-spin	rpm/sec	1000/5	1000/5	1000/5	1000/5	1000/5
	Spin	rpm/sec	4000/30	1900/30	3400/30	1900/30	1400/30
Pre-bake		°C/sec	120/100	120/100	120/130	120/180	120/260
Pre-baked thickness		microns	3.6	6.6	9.4	14.7	18.7
Exposure	Dose	mJ/cm²	140	150	240	500	700
	Focus	microns	0	0	0	0	0
Development	Puddle 1	sec	15	20	35	60	90
	Puddle 2	sec	15	20	35	60	90
	Rinse	rpm/sec	1000/10	1000/10	1000/10	1000/10	1000/10
	Spin-dry	rpm/sec	3500/10	3500/10	3500/10	3500/10	3500/10
Developed thickness		microns	2.5	5.0	7.2	11.5	15.2
Post-bake		°C/min	150–350/60	150–350/60	150–350/60		
		°C/min	350/30	350/30	350/30		
Cured thickness		microns	2.0	3.5	5	8.2	10.8

Figure 1. Spin speed vs. film thickness after soft-bake

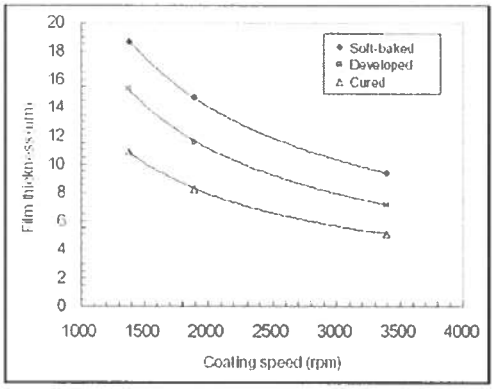


Table 3. Refractive indices for thickness measurements

Film	Refractive Index	Filter*
Soft-baked	1.551	R-60
Developed	1.550	R-60
Cured	1.618	R-60

*Short wave length sharp cut filter at 660 nm

Cauchy law on n and k

Film	N1	N2	N3	K1	K2	K3
Soft baked	1.651	-1.172e-2	2.250e-3	2.813e-5	-9.527e-5	2.656e-5
Developed	1.656	-1.548e-2	2.462e-3	2.116e-5	-1.086e-4	2.643e-5
cured	1.663	-1.033e-2	2.877e-3	-5.776e-4	3.735e-4	7.317e-5

$n(\lambda) = N1 + N2/\lambda^2 + N3/\lambda^4$ $k(\lambda) = K1/\lambda + K2/\lambda^3 + K3/\lambda^5$ λ(μm)

5.4 Soft-bake Process

Primary Objectives: 1) to drive off carrier solvents from the polyimide coating and producing a tack-free surface for exposure; 2) to provide sufficient chemical resistance and adhesion so that the unexposed areas of the coating will not be attacked or delaminated by the developer. Coated substrates should be soft-baked on one or more hot plates in the proximity mode at 120°C/130–260 seconds for HD-8000 or at 100°C/100 seconds for HD-8001. (In the contact mode the temperature should be re-adjusted downward to obtain the recommended film thickness after development.)

The substrates must remain in a horizontal (level) position during the soft bake since the coating is still liquid after spin application.

Coated substrates should be cooled to ambient temperature prior to UV exposure. A chill plate is recommended for cooling after the bake. The coated substrates can be stored for up to 72 hours in a wafer cassette box under clean room conditions prior to exposure and development. (See Section 5.8.) The effect of soft-bake temperature and times on photolithographic properties are given in Table 4.

5.5 Exposure Process (Exposure Dose, Focus)

The amount of incident radiation required for optimum resolution and CD depends on the coating thickness (Figure 2), structure size, side-wall profile and feature uniformity. The coated substrates can be stored for up to 72 hours in a wafer cassette box under clean room conditions prior to development. Depth of focus will impact resolution and feature size; generally, focus latitude for the best resolution is +3.0 to –3.0 μm from the top of the film surface (Figures 3 and 4). CD control as a function of mask linearity is plotted in Figure 5 and as a function of exposure energy in Figure 6.

Figure 2. Exposure sensitivity curves at various cured thicknesses

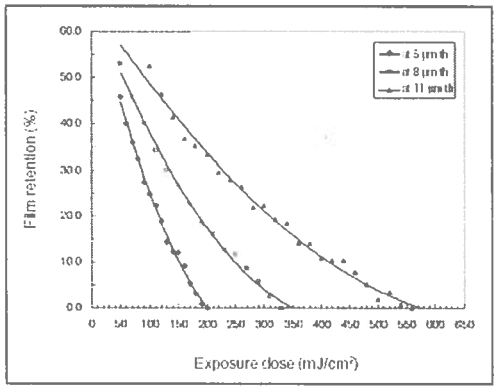


Figure 3. Effect of varying focus margin on resolution (5 µm cured)

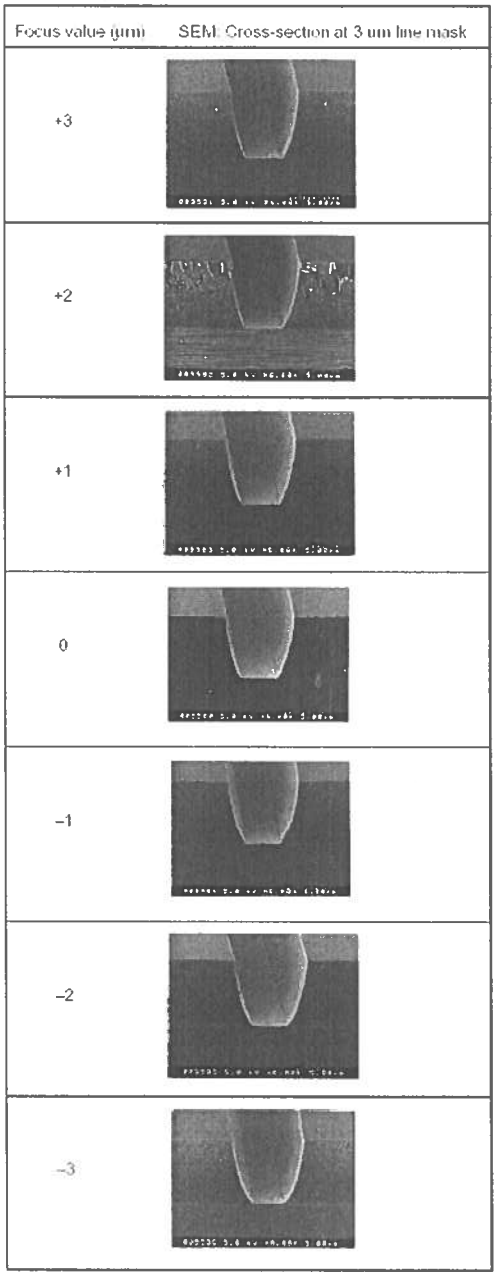


Figure 4 Effect of varying focus margin at various exposure energies on CD (5 µm cured)

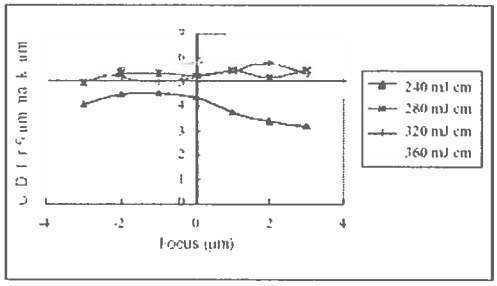
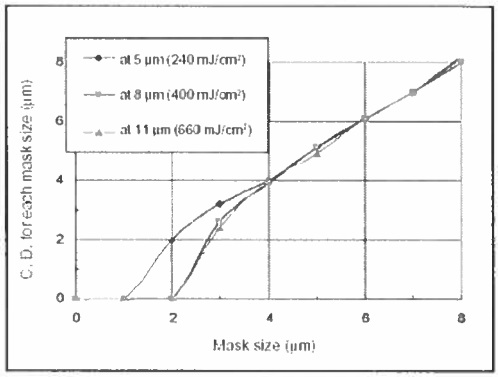


Figure 5. CD control as a function of mask linearity at various cured film thicknesses



5.6 Single Wafer Development Processing

After exposure the wafer can be developed on a standard positive photoresist developer track using a standard TMAH-based positive photoresist developer with a normality of 0.25 to 0.27 (2.27 to 2.46%).

No post exposure bake is required. Exposed films can be held for up to 72 hr prior to development without significantly impacting resolution using a puddle development process.

In a typical single wafer puddle process, the wafer is positioned on the developer chuck and developer solution is puddled onto the stationary wafer for a set period of time. The developer solution is then spun off. A second puddle of developer is then dispensed for a set time period that is predicated by film thickness and general process conditions. Since the development process will continue as long as the polyimide coating is in contact with the developer, develop time is a critical factor in defining the parameters of a robust process (Table 4). After development the wafer should be rinsed with water while the wafer is spun at a moderate rpm level. After rinse, the wafer is spun dry.

5.7 Resolution

Resolution as a function of film thickness after development and after cure is illustrated in the micrographs pictured in Figure 7.

The side wall profiles of soft baked and cured films of HD-8000 as a function of film thickness are pictured in Figure 8.

Feature size can be impacted by varying exposure conditions and other processing variables (Table 4). Figure 9 plots film retention as a function of minimum exposure dose, using the conditions detailed in Table 4.

Figure 6. Exposure dose margin for a 5 µm square hole CD at various cured film thickness

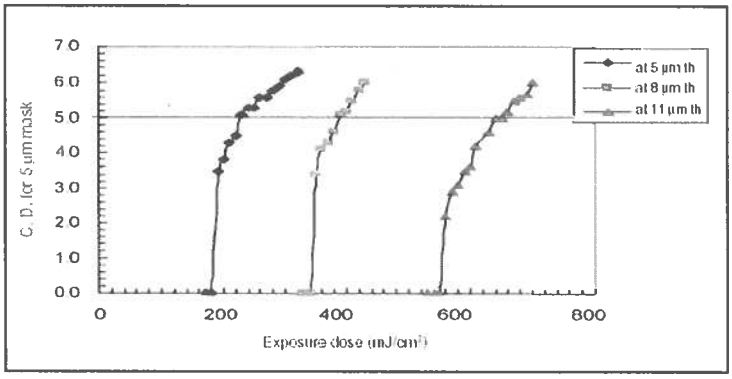


Figure 7. Micrographs depicting resolution after development (left) and after cure (right). For each picture, 1, 2, 3, 4, 5 and 6 um square hole and space patterns are shown from the right to left side.

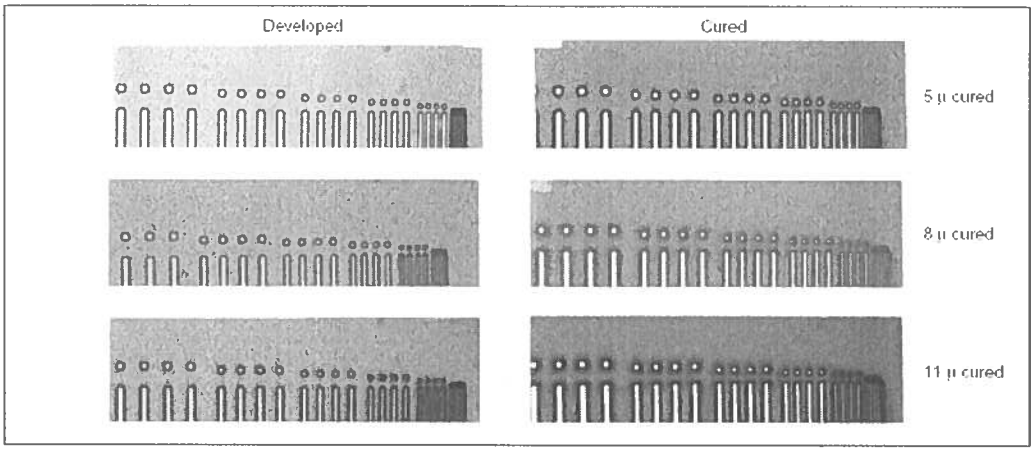


Figure 8. SEM photographs showing resolution after development (left) and after cure (right).

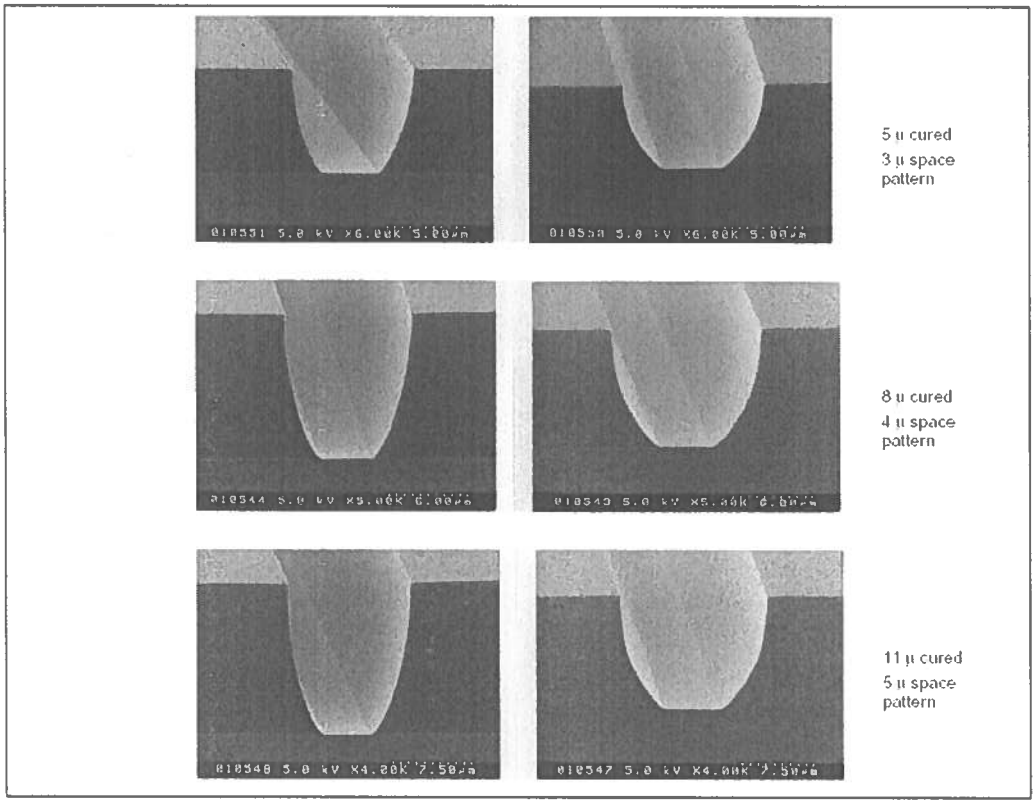
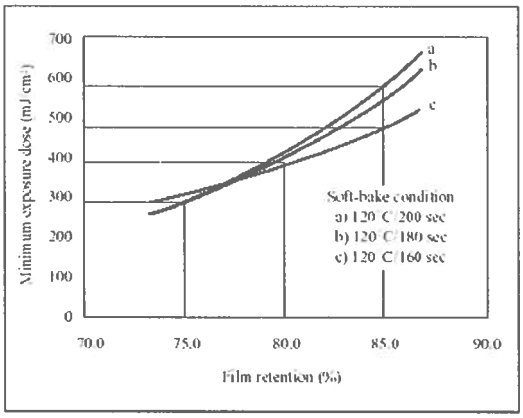


Table 4. Effect of soft-bake time and development time on photolithographic properties* (8 μ cured)

Spin speed (rpm)	Soft-bake** (C/sec)	Film thickness after soft-bake (microns)	Dev. time (sec)	Film thickness after dev. (microns)	Film retention (%)	Minimum exposure (mJ/cm²)	Film thickness after cure	10 micron line size
1350	120/160	14.6	90	12.3	84.5	480	8.7	11.1
			120	11.8	80.5	370	8.4	10.8
			150	11.3	77.3	340	8.0	10.6
			180	10.8	73.3	280	7.7	9.1
1350	120/180	14.6	90	12.5	85.8	600	8.9	10.7
			120	11.8	81.4	400	8.4	10.2
			180	11.5	78.7	360	8.2	10.4
			270	11.2	75.6	310	7.9	9.7
1350	120/200	14.7	90	12.7	86.9	690	9.0	10.4
			120	12.2	82.9	480	8.7	10.4
			150	11.7	79.4	380	8.3	10.5
			180	11.3	76.6	330	8.0	9.8

*See Appendices C and D
**Proximity bake temperature at 100 μ

Figure 9. Film retention vs. minimum exposure dose (8 μ cured)



5.8 Hold-Time Latitude

HD-8000 series polyimides exhibit wide hold time process latitude between soft-bake and exposure, as well as from exposure to development. After soft-bake or exposure, coated substrates can be stored for up to 72 hours in a wafer cassette box under clean room conditions prior to moving on to the next process step. Figures 10–13 compare minimum exposure energy, film retention and critical dimension control as a function of hold time.

Figure 10. Minimum exposure dose and film retention vs. hold time between soft-bake and exposure with 8 µm-cured standard condition

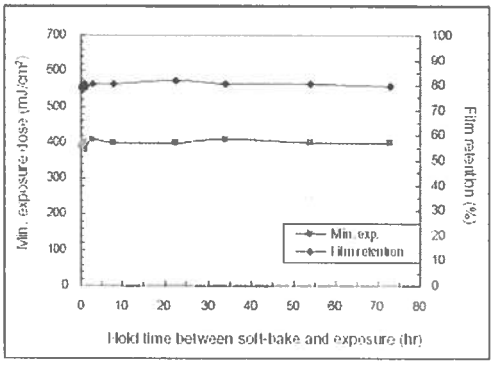


Figure 11. Minimum exposure dose and film retention vs. hold time between exposure and development with 8 µm-cured standard condition

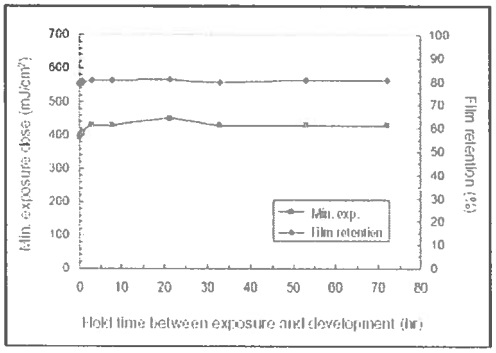


Figure 12. Critical dimension for 5 µm mask vs. hold time between soft-bake and exposure (5 µm cured)

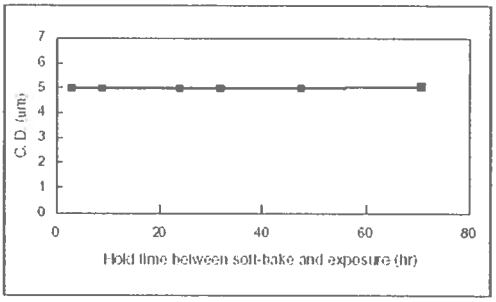
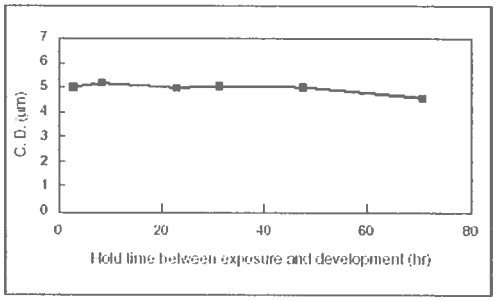


Figure 13. Critical dimension for 5 µm mask vs. hold time between exposure and development (5 µm cured)



5.9 Cure Process

The objectives of a proper cure schedule are to: 1) remove residual solvents, 2) complete the imidization process, 3) complete the adhesion process. Because all three of these actions can occur simultaneously at a given temperature, the cure schedule is a very important process step which can impact cured film quality and associated mechanical properties (see Table 6). The following variables need to be considered in curing polyimide films:

- Curing tool
- Atmosphere
- Loading temperature
- Ramp rate
- Soaks (holding temperatures)
- Final Cure temperature
- Ramp down

Curing is typically done as a batch process using programmable ovens or furnaces. (Single wafer curing tools that utilize a series of hot plates have also been developed for in-line processing. This technique has been frequently used with non-photodefinable polyimides.)

Curing should be performed under a nitrogen atmosphere (oxygen conc. <1000 ppm). Some programmable ovens are designed to cure under a vacuum. A partial vacuum may be used with a nitrogen atmosphere.

Loading temperatures, ramp rate, soaks (intermediate holding temperatures), final cure temperature and cool down rate can be optimized for optimum throughput and cured film properties. A basic cure schedule is given below for a typical "single-mask" stress buffer application.

Basic Cure Schedule for HD-8000 Series Products

- Load into oven or furnace at <150°C
- Ramp from loading temperature to 350°C over a 60 minute period.
- Hold at 350°C for 30 minutes
- Substrates can be unloaded immediately or allowed to cool down.

Furnaces can be routinely cleaned with a 700°C cycle for 1 hour under air atmosphere.

5.10 Rework

Before curing, HD-8000 can be stripped with commercial cleaners commonly recommended for polyimide removal. Oxygen plasma etching can be used to remove both uncured and cured polyimide. Typical rework conditions are detailed in Table 5.

Table 5. Rework conditions

		Reagent	Condition	Remarks
After soft-bake and after development	strip	S-106	23°C/3 min	dip
	rinse	D.I. water	23°C/2 min	dip/spin dry
After cure	strip	S-106	105°C/3 min	dip
	rinse	D.I. water	23°C/2 min	dip/spin dry
After cure (Option)	strip	O_2 plasma	300W	Yamato RFG-500A/PC-101A
	strip	2.5% HF	105°C/1 min	dip
	rinse	D.I. water	23°C/2 min	dip/spin dry

6. Cured Film Properties

6.1 General Properties

Cured films of the HD-8000 series exhibit a relatively high Tg, a moderate CTE and good elongation, as detailed in Table 6.

Table 6. Cured Film Properties

	Units	HD-8000	HD-8001
Tg	°C	300	296
CTE	ppm/°C	47	52
Tensile strength	MPa	122	146
Elastic modulus	GPa	2.5	2.9
Elongation	%	11	14
Weight loss temp.	°C		
1%		403	403
3%		421	421
5%		433	433
Adhesion	hr	>500	>500
Dielectric constant at 1 kHz		3.4	3.4
Dissipation factor		0.0097	0.0097

6.2 Cured Film Properties as a Function of Cure

The cured film properties can vary with final cure temperature. Some of these variances are detailed in Table 7.

6.3 Optical Properties

The optical transmittance and optical density as a function of film thickness are plotted in Figures 14 and 15.

Figure 14. Optical transmittance spectrum of 5.7 µm cured film

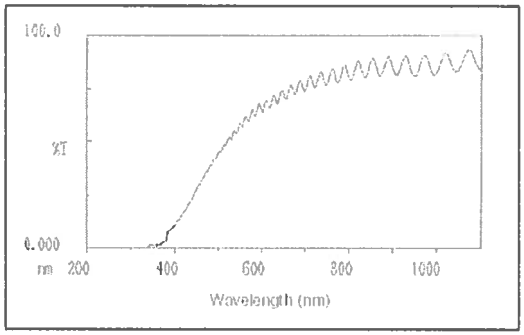


Figure 15. Cured film optical density normalized by thickness

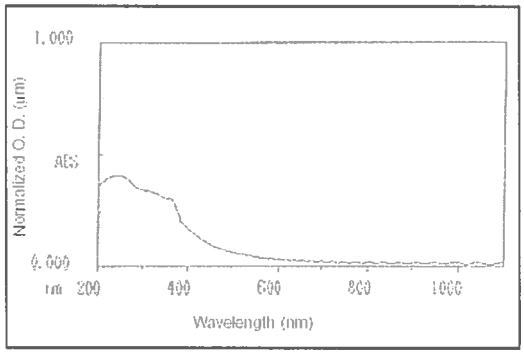


Table 7. Dependence of cured film properties on cure temperature

No.	Cure temp (°C)	Tensile strength (MPa)	Elastic modulus (GPa)	Elongation (%)	5% Wt. Loss (°C)	Tg (°C)	CTE (ppm/°C)
1	300	139	2.80	11.5	424	286	53
2	320	129	2.70	11.5	430	293	49
3	350	122	2.50	11.0	433	300	47

6.4 Residual Stress

Residual or the internal stress in cured films was measured using a wafer bending technique. The measured stress is compared to a self priming wet etch polyimide, PIX-3400, in Table 8.

Table 8. Internal Stress (Wafer Bending)

		R_1 (m)	R_2 (m)	t (μm)	σ (MPa)
HD-8000	1	−129.3	213.1	5.01	29.1
	2	−1668	84.05	5.01	29.3
	Ave.	—	—	—	29.2
PIX-3400 (ref.)	1	−3278	88.00	4.58	28.8
	2	−134	229.0	4.91	28.3
	Ave.	—	—	—	28.55

σ : Internal stress (MPa)

$$\sigma = E\,h^2 / (1-\nu) 6\,R t$$

R_1 : Radius of bare Si wafer (original bend)
R_2 : Radius of Si wafer after PI cure (bend by PI)

$$R = R_1 R_2 / (R_1 - R_2)$$

t : PI thickness (μm)
h : Wafer thickness (625 μm)
$E/(1-\nu)$: Elastic modulus of Si wafer (1.805×10^5 MPa)

7. Dry Etch Resistance

Both soft-baked and cured films exhibit excellent resistance to dry etch processing chemicals. This versatility makes HD-8000 and HD-8001 well suited for most single-mask wafer overcoat processes.

Silicon nitride and cured films of HD-8000 were measured after dry etch processing for film thickness, depth and pattern size.

The impact of etching gas composition on film thickness reduction and etch rate is shown in Table 9 and Figures 16 and 17. A higher O_2 ratio resulted in a larger film thickness reduction and a higher etch rate. Soft-baked films of the HD-8000 series have also shown good RIE resistance.

Table 9. Dry etch tolerance (etch rate μm/min)

Gas composition CF_4/O_2	SiN	HD-8000
60/40	0.20	0.17
75/25	0.30	0.07
90/10	0.080	0.036

Figure 16. Dry etch rate of SiN and polyimide as a function of gas composition

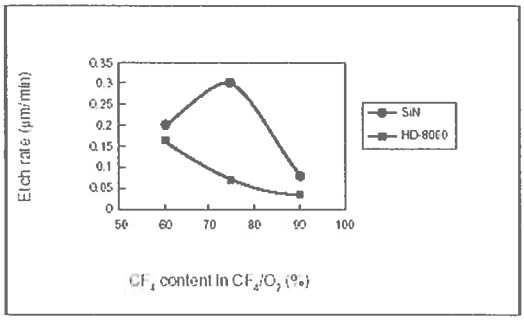
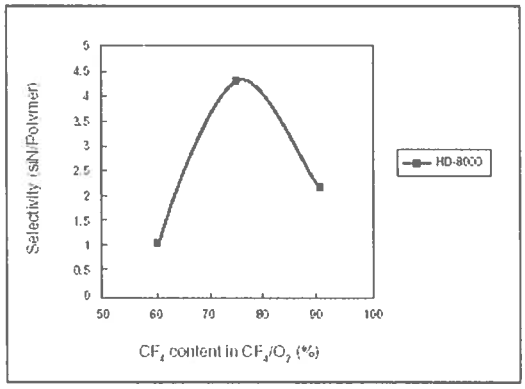


Figure 17. Selectivity of dry etch rate to SiN as a function of gas composition



8. Package Reliability

For packaging reliability, cured films were tested for adhesion to two types of molding compound types as a function of final cure temperature. PIX-3400 is an established self-priming, wet etch polyimide stress buffer product and is included for reference purposes. Test results are shown in Table 10 and indicate that HD-8000 exhibited improved performance, independent of final cure temperature when tested with CEL-9200 and CEL-4690SX-4RU molding compounds.

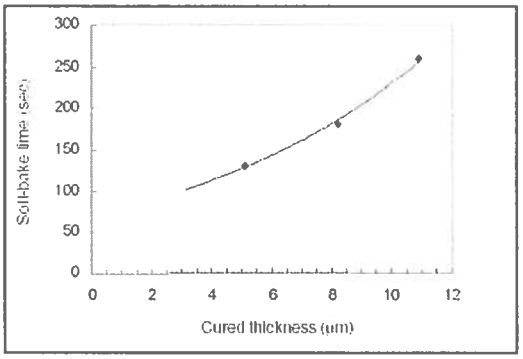
Table 10. Adhesion Strength to Molding Compounds

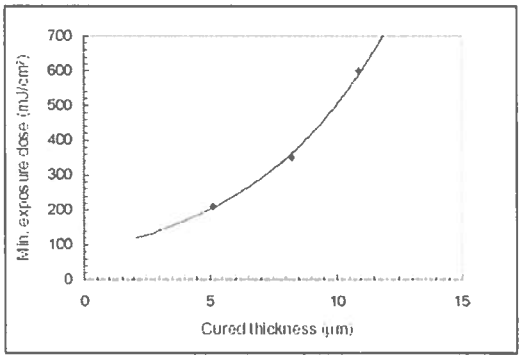
	CEL-9200	CEL-4690SX-4RU
HD-8000 300°C cure	4.9	7.4
HD-8000 325°C cure	4.5	6.7
HD-8000 350°C cure	4.6	6.4
PIX-3400 (ref.)	3.2	4.5

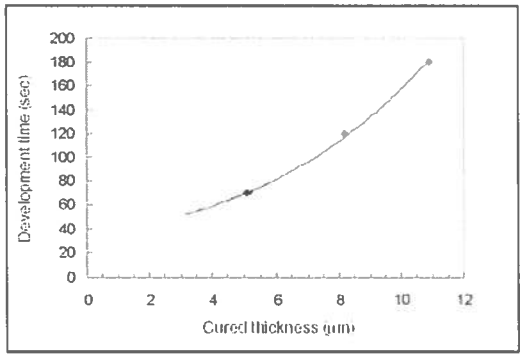
Stud pull method:
stud ϕ 3.65 mm
unit kgf/10.2 mm²
after PCT 85°C / 85% RH / 168 hr
measure temp. 250°C
shear speed 100 µm/sec
Molding compound
CEL-9200: biphenyl type
CEL-4690SX-4RU: cresol-novolac type

9. Appendices

9.1 Appendix A—Cured film thickness and recommended process conditions (Table 2)

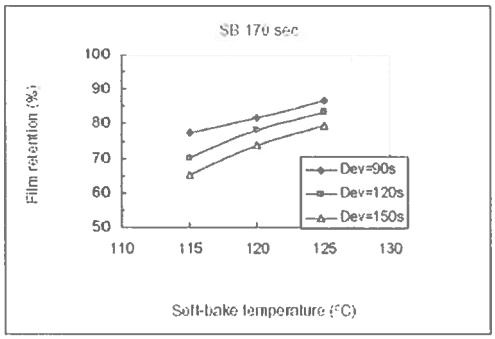


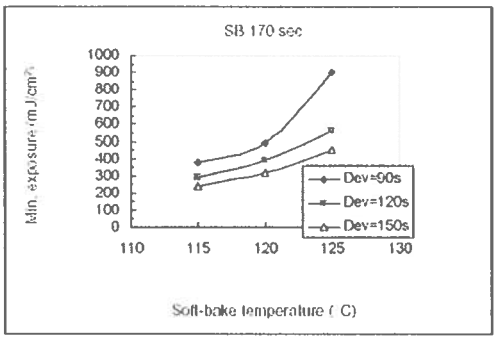


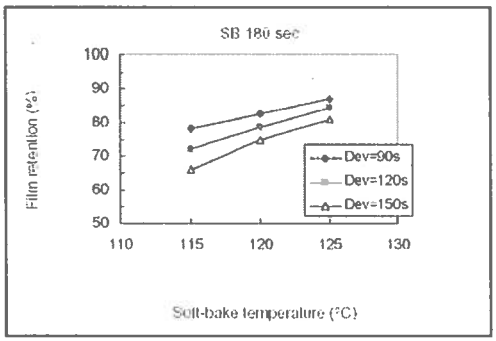


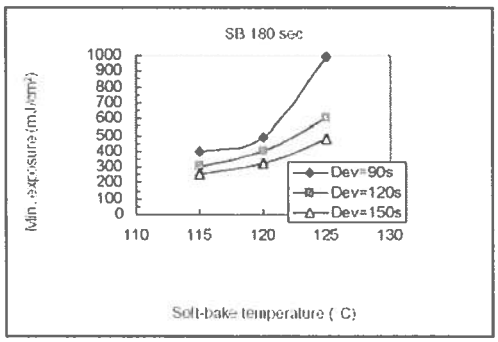
9.2 Appendix B—Soft-bake (SB) temperature margin (at 8 μm cured)

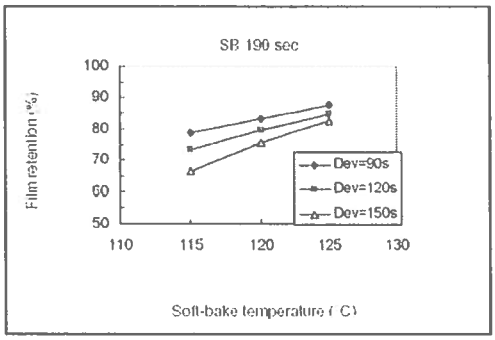
Film retention (left) and minimum exposure dose (right) as a function of soft bake temperature at various development times. Soft bake times are fixed at 170, 180, and 190 sec, respectively, from the upper.

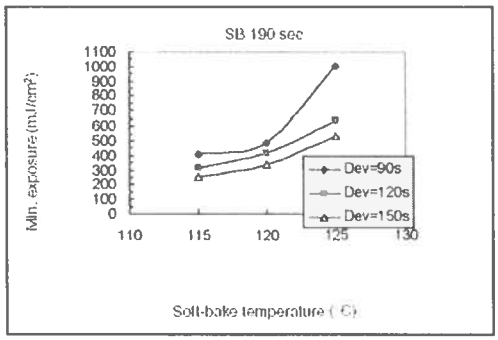






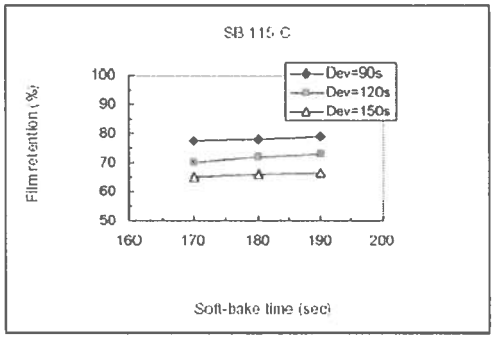


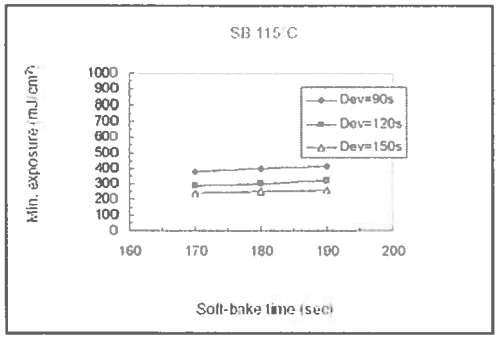


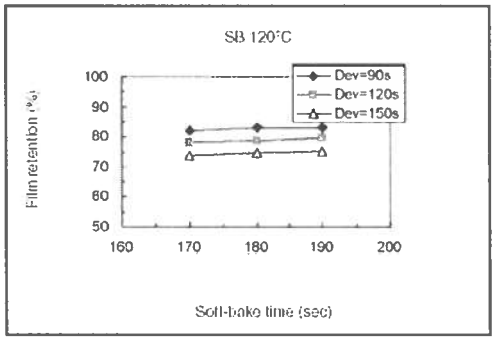


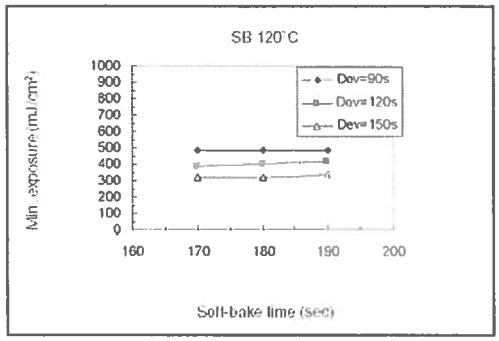
9.3 Appendix C—Soft-bake (SB) time margin (at 8 μm cured)

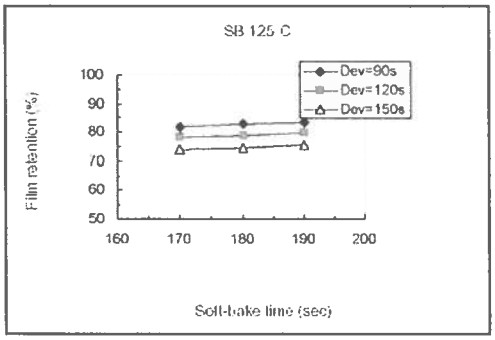
Film retention (left) and minimum exposure dose (right) as a function of soft bake time at various development times. Soft bake temperature is fixed at 115, 120, and 125 °C, respectively, from the upper.

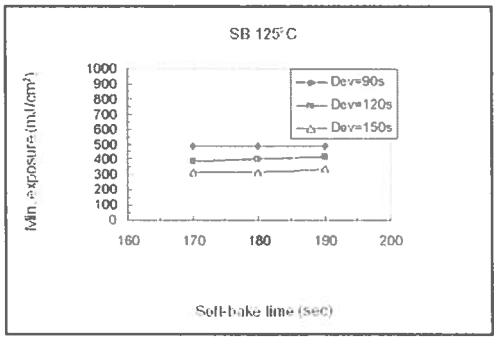






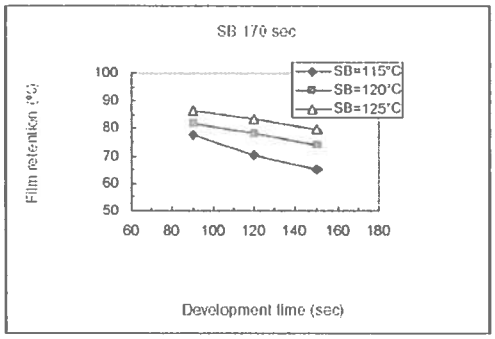


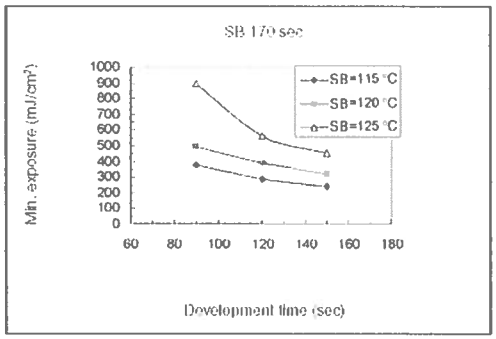


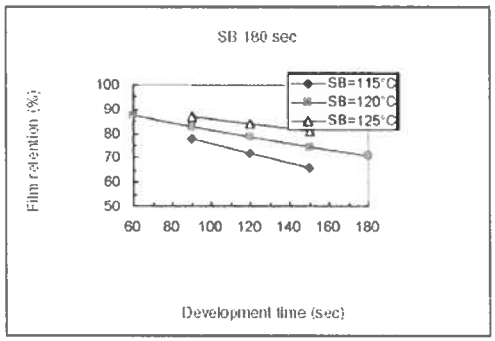


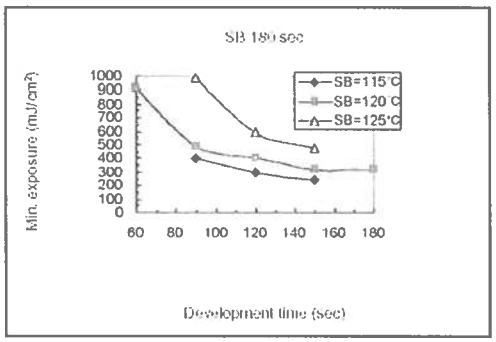
9.4 Appendix D—Development time margin (at 8 μm cured)

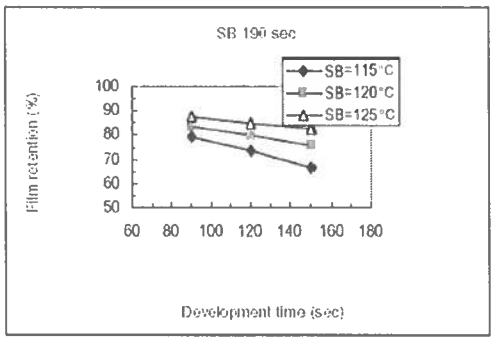
Film retention (left) and minimum exposure dose (right) as a function of development time at various soft-bake temperatures. Soft-bake times are fixed at 170, 180, and 190 sec, respectively, from the upper.

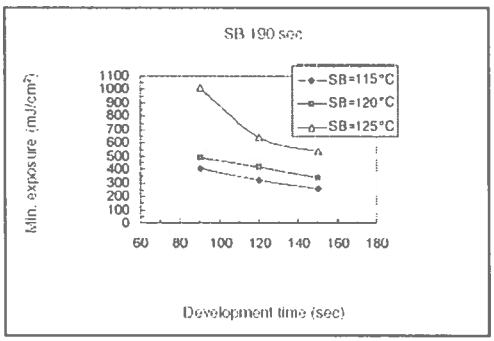












Summary

The HD-8000 series of photodefinable polyimides were developed through the collaborative efforts of the HD MicroSystems R&D laboratories in Hitachi City, Japan, and Wilmington, Delaware. The resulting products are high-resolution, positive-tone photodefinable polyimides which can be imaged on I-line, G-line and broad band photo tools with tight CD control. As formulated, HD-8000 has excellent process latitude, with 72-hour hold-time stability and two week RT viscosity stability. Cured films of HD-8000 were measured to have good elongation, low stress and a high Tg. HD-8000's resistance to both wet chemicals and dry etch processing conditions is excellent, and make it well suited for various wafer overcoat processes.

Technical Service

HD MicroSystems has dedicated technical service facilities in Hitachi City, Japan and Parlin, New Jersey. Technical support personnel are available to work in-house on dedicated process tools, or on location throughout the world to assist in process development or to help resolve technical problems. For more information, contact your regional HD MicroSystems Technical Representative.

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HDM-2 6/01

Appendix E

HD-8000 Polyimide inspection processes

Process for Sample (S1)

1. Cleaning with acetone, methanol and DI

2. Per- bake for 2 min at 120C

3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

4. Spin at 3400rpm/30sec

5. Bake for 2:10 min at 120C

6. Rinse with DI H2O2 1000rpm/10 Sec

7. Spin dry for 3500rpm/10 Sec

8. Cure Schedule

· Load into oven or furnace at 20C

· Ramp from 20C to 350C over 60 min period.

· Hold at 350C for 30 min

· Substrate can be unloaded immediately or allowed to cool down.

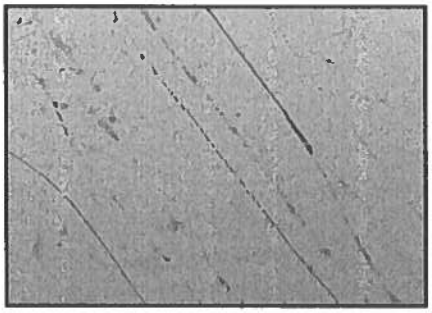

Figure E.1

Process for sample2 (S2)

1. Cleaning with acetone , methanol and DI

2. Per- bake for 2 min at 120C

3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

4. Spin at 3400rpm/30sec

5. Bake for 2:10 min at 120C

6. Apply developer for 2 minutes

7. Rinse with DI H2O2 1000rpm/10 Sec

8. Spin dry for 3500rpm/10 Sec

9. Cure Schedule

· Load into oven or furnace at 20C

· Ramp from 20C to 350C over 60 min period

· Hold at 350C for 30 min

· Substrate can be unloaded immediately or allowed to cool down.

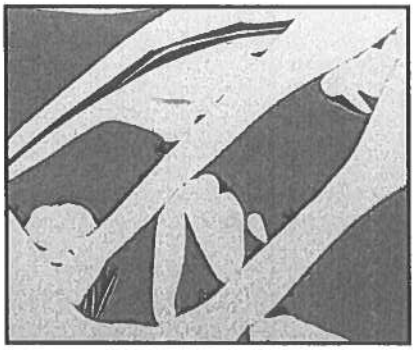

Figure E.2

Process for Sample (S3)

1. Cleaning with acetone , methanol and DI

2. Per- bake for 2 min at 120C

3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

4. Spin at 3400rpm/30sec

5. Bake for 2:10 min at 120C

6. Cure Schedule

- Load into oven or furnace at 20C

- Ramp from 20C to 200C over 40 min period

- Hold at 200 for 15 min period

- Ramp from 200C to 350C over 30 min period

- Hold at 350C for 30 min

- Substrate can be unloaded immediately or allowed to cool down.

Dark areas are polyimide and light areas are GaAs .

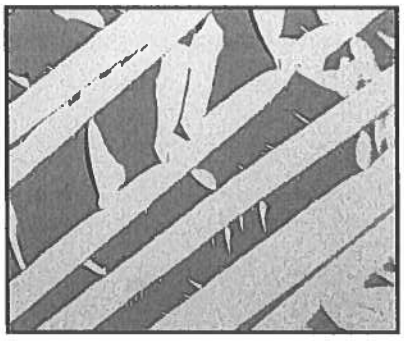

Figure E.3.a

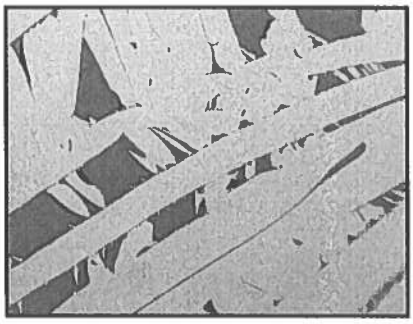

Figure E.3.b

Process for Sample (S4)

1. Cleaning with acetone , methanol and DI

2. Per- bake for 2 min at 120C

3. Apply VM-651[95 ml methanol:5 ml DI H2O:1 ml VM-651]as an adhesion promote at 5000rpm/30 Sec

4. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

5. Spin at 3400rpm/30sec

6. Bake for 2:10 min at 120C

7. Cure Schedule

- Load into oven or furnace at 20C

- Ramp from 20C to 200C over 40 min period

- Hold at 200 for 15 min period

- Ramp from 200C to 350C over 30 min period

- Hold at 350C for 30 min

- Substrate can be unloaded immediately or allowed to cool down.

Dark areas are polyimide and light areas are GaAs .(polyimde thickness is ONLY 0.4 micron.)

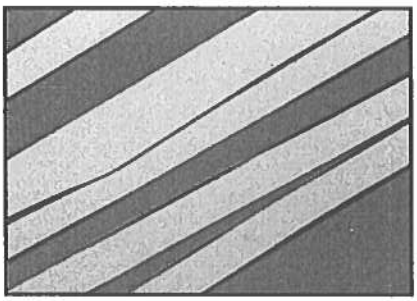

Figure E.4

Process for sample (S5)

1. Cleaning with acetone , methanol and DI

2. Per- bake for 2 min at 120C

3. Apply VM-651[95 ml methanol:5 ml DI H2O:1 ml VM-651]as an adhesion promote at 5000rpm/30 Sec

4. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

5. Spin at 3400rpm/30sec

6. Bake for 2:10 min at 120C

7. Rinse with DI H2O2 1000rpm/10 Sec

8. Spin dry for 3500rpm/10 Sec

9. Cure Schedule

- Load into oven or furnace at 20C

- Ramp from 20C to 200C over 40 min period .

- Hold at 200 for 15 min period

- Ramp from 200C to 350C over 30 min period .

- Hold at 350C for 30 min

- Substrate can be unloaded immediately or allowed to cool down.

Dark areas are polyimide and light areas are GaAs (both pictures are for the same sample) (polyimde thickness is ONLY 0.4 micron.)

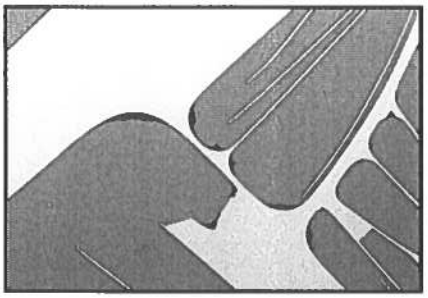

Figure E.5.a

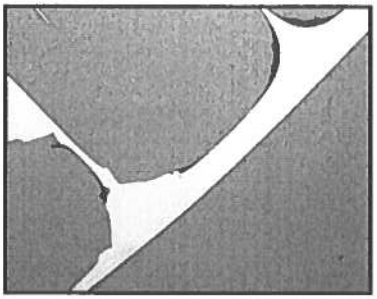

Figure E.5.b

Process for sample (S6)

1. Cleaning with acetone , methanol and DI

2. Per- bake for 2 min at 120C

3. Apply VM-651 [95 ml methanol:5 ml DI H2O:1 ml VM-651]as an adhesion promote at 5000rpm/30 Sec

4. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

5. Spin at 3400rpm/30sec

6. Bake for 2:10 min at 120C

7. Apply developer for 2 minutes

8. Rinse with DI H2O2 1000rpm/10 Sec

9. Spin dry for 3500rpm/10 Sec

10. Cure Schedule

- Load into oven or furnace at 20C

- Ramp from 20C to 200C over 40 min period

- Hold at 200 for 15 min period

- Ramp from 200C to 350C over 30 min period

- Hold at 350C for 30 min

- Substrate can be unloaded immediately or allowed to cool down.

Dark areas are polyimide and light areas are GaAs (both pictures are for the same sample) (polyimde thickness is ONLY 0.4 micron.)

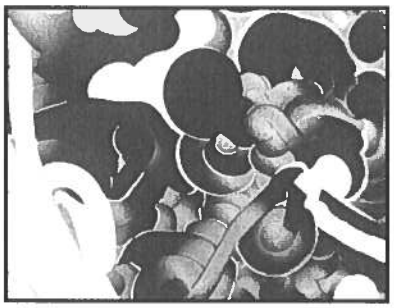

Figure E.6.a (Failed)

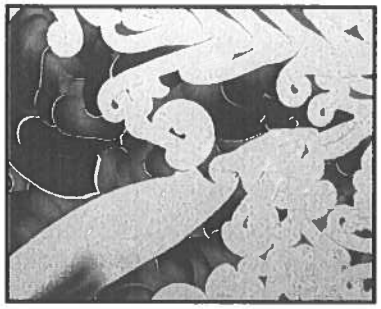

Figure E.6.b (Failed)

Process for Sample (S7a)

1. Cleaning with acetone , methanol and DI

2. Per- bake for 2 min at 120C

3. Apply VM-651[0.5 ml VM-651:100 ml DI H2O]

4. Allow the puddle to stand on the wafer for 20 sec

5. Spin dry at 2000-3500 rpm/30 Sec

6. To improve adhesion bake at (110-130)C for 1 min.

7. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

8. Spin at 3400rpm/30sec

9. Bake for 2:10 min at 120C

10. Cure Schedule

- Load into oven or furnace at 20C

- Ramp from 20C to 200C over 40 min period

- Ramp from 200C to 350C over 30 min period

- Hold at 350C for 30 min

- Substrate can be unloaded immediately or allowed to cool down.

Thickness ~0.5 μm + craks

Process for Sample (S8)

1. Cleaning with acetone , methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.
4. Spin at 3400rpm/30sec
5. . Bake for 2:10 min at 120C
6. Rinse with DI H_2O 1000rpm/10 Sec
7. Spin dry for 3500rpm/10 Sec
8. Cure Schedule
    a. Load into oven or furnace at 20C
    b. Ramp from 20C to 200C over 40 min period
    c. Ramp from 200C to 350C over 30 min period
    d. Hold at 350C for 30 min
    e. Substrate can be unloaded immediately or allowed to cool down.

Thickness ~1.0 μm + cracks

1.Evaprote (Ti/Au) (200/3000) A.

2.Using adhesion tape, stick the tape on top of the gold then pull; see if there is some gold on the adhesion tape.

Process for Sample (S9)

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

4. Spin at 5000rpm/30sec
5. Bake for 1:40 min at 115C
6. Curing *(See Table and plot in the Curing Furnace Characterization section before proceeding)*
    - Load into oven or furnace at 20C
    - Ramp from 20C to 350C over 60 min period *(Furnace setting ~240C)*
    - Hold at 350C for 30 min *(Furnace setting ~240C)*
    - Substrate can be unloaded immediately or allowed to cool down.
    - Thickness 5 μm with a brown color
7. Evaporation Ti/Au (300/3000) A (Total contact thickness = 0.33 μm)
8. Microscope camera

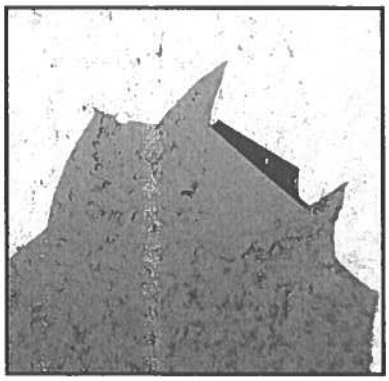

Figure E.7 (Failed)

Process for Sample (S10)

1. Cleaning with acetone , methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.
4. Spin at 5000rpm/30sec
5. Bake for 1:40 min at 115C

6. Evaporation Ti/Au (200/3000)A (Total contact thickness = 0.32 μm)
7. Bake to cure
8. Microscope camera

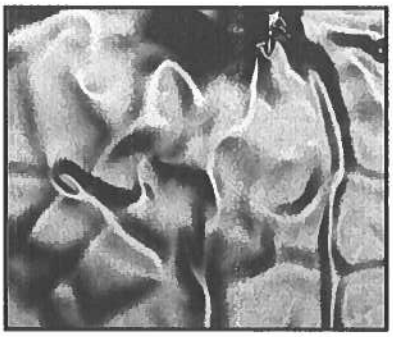

Figure E.8 (Failed)

Process for Sample (S11)

1. Cleaning with acetone , methanol and DI
2. Per- bake for 2 min at 120C
3. Apply VM-651[0.5 ml VM-651:100 ml DI H2O]
4. Allow the puddle to stand on the wafer for 20 sec
5. Spin dry at 3000 rpm/30 Sec
6. To improve adhesion bake at (110-130)C for 1 min.
7. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.
8. Spin at 5000rpm/30sec
9. Bake for 1:30 min at 115C
10. Spin on positive tone photo resist AZ 4400 4000rpm/30sec
11. Soft bake for 2 min at 95C
12. Clean the edges of the sample using a blade
13. Align Mesa mask and expose for 22 sec at 15mW/cm^2

14. Developing for 75 Sec using AZ400K:H_2O (1:4)

15. Post –bake sample for 2 min at 120C. ***optional***

16. α-Step & Microscope camera(expected thickness~ 4 μm thick film)

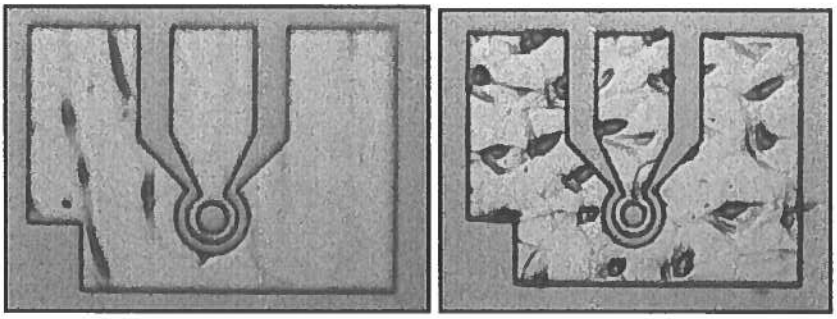

Figure E.9 (Failed)

17. Evaporation Ni/Au (200/3000) A (Total contact thickness = 0.32 μm)

18. 11.Lift off using acetone [Don't use Air Brush]

19. Microscope camera

Failed , acetone removes both the photoresist and the uncured polyimie

Process for Sample (S12)

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.
4. Spin at 5000rpm/30sec
5. Bake for 1:40 min at 115C
6. Curing *(See Table and plot in the Curing Furnace Characterization section before proceeding)*
    a. Load into oven or furnace at 20C
    b. Ramp from 20C to 350C over 60 min period *(Furnace setting ~240C)*
    c. Hold at 350C for 30 min *(Furnace setting ~240C)*

d. Substrate can be unloaded immediately or allowed to cool down.

e. Thickness 5 μm with a brown color

7. Evaporation Ti/Au (300/3000) A (Total contact thickness = 0.33 μm)
8. Bake for 1 min at 120C
9. Microscope camera

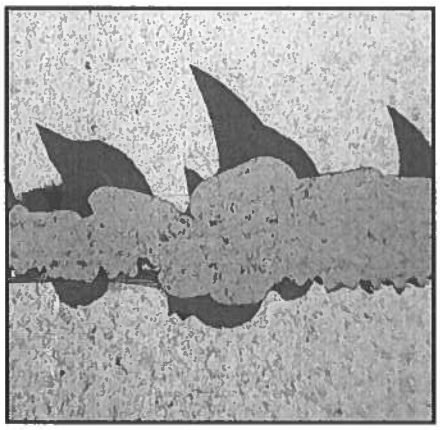

Figure E.10

Process for Sample (S13)

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.
4. Spin at 5000rpm/30sec
5. Bake for 1:40 min at 115C
6. Curing *(See Table and plot in the Curing Furnace Characterization section before proceeding)*

    a. Load into oven or furnace at 20C

    b. Ramp from 20C to 350C over 60 min period *(Furnace setting ~240C)*

    c. Hold at 350C for 30 min *(Furnace setting ~240C)*

d. Substrate can be unloaded immediately or allowed to cool down.

e. Thickness 5 μm with a brown color

7. Apply VM-651 [0.5 ml VM-651: 100 ml DI H2O]
8. Allow the puddle to stand on the wafer for 20 sec
9. Spin dry at 6000 rpm/30 Sec
10. To improve adhesion bake at (110-130) C for 1 min.
11. Evaporation Ti/Au (300/3000) A (Total contact thickness = 0.33 μm)
12. Bake for 3 min.
13. Microscope camera

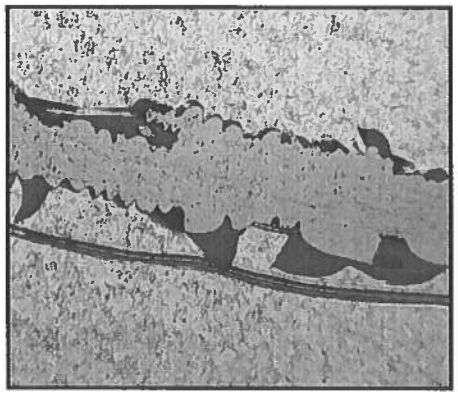

Figure E.11

Process for Sample (S14)

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.
4. Spin at 5000rpm/30sec
5. Bake for 1:40 min at 115C
6. Curing *(See Table and plot in the Curing Furnace Characterization section before proceeding)*

- Load into oven or furnace at 20C
- Ramp from 20C to 350C over 60 min period *(Furnace setting ~240C)*
- Hold at 350C for 30 min *(Furnace setting ~240C)*
- Substrate can be unloaded immediately or allowed to cool down.
- Thickness 5 μm with a brown color

7. Apply VM-651[0.5 ml VM-651:100 ml DI H2O]
8. Allow the puddle to stand on the wafer for 20 sec
9. Spin dry at 6000 rpm/30 Sec
10. To improve adhesion bake at (110-130) C for 1 min.
11. Evaporation Ti/Au (300/3000) A (Total contact thickness = 0.33 μm)
12. Bake for 6 min at 120C
13. Microscope camera

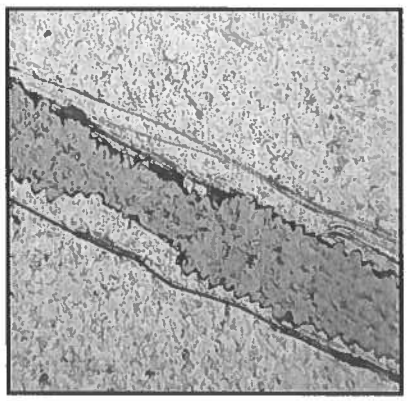

Figure E.12

Process for Sample (S15)

1. Cleaning with acetone, methanol and DI
2. Per- bake for 2 min at 120C
3. Apply positive tone polyimide HD-8000 and let stand for 30 Sec.

4. Spin at 5000rpm/30sec
5. Bake for 1:40 min at 115C
6. Curing *(See Table and plot in the Curing Furnace Characterization section before proceeding)*
    a. Load into oven or furnace at 20C
    b. Ramp from 20C to 350C over 60 min period *(Furnace setting ~240C)*
    c. Hold at 350C for 30 min *(Furnace setting ~240C)*
    d. Substrate can be unloaded immediately or allowed to cool down.
    e. Thickness 5 μm with a brown color
7. Apply VM-651[0.5 ml VM-651:100 ml DI H2O]
8. Allow the puddle to stand on the wafer for 20 sec
9. Spin dry at 6000 rpm/30 Sec
10. To improve adhesion bake at (110-130) C for 1 min.
11. Evaporation Ti/Au (300/3000) A (Total contact thickness = 0.33 μm)
12. Bake for 10 min at 120C
13. Microscope camera

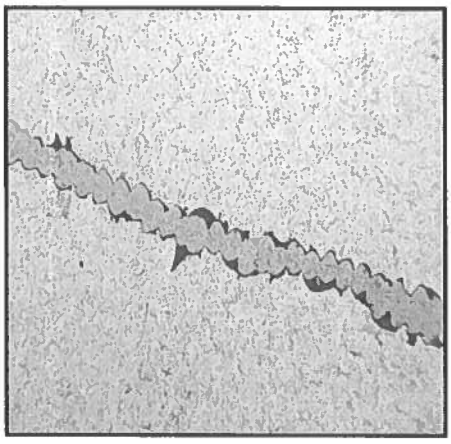

Figure E.13