THESIS

INVESTIGATING CDTE SOLAR CELL PERFORMANCE THROUGH GLASS/TCO SELECTION AND CDSE-BASED WINDOW LAYER ENGINEERING

Submitted by

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ABSTRACT

INVESTIGATING CDTE SOLAR CELL PERFORMANCE THROUGH GLASS/TCO SELECTION AND CDSE-BASED WINDOW LAYER ENGINEERING

As energy demand continues to rise, it is imperative that energy production becomes more efficient. Thin-film cadmium telluride (CdTe) photovoltaic technology is advantageous compared to many other energy sources due to its low material cost, ease of manufacturing, and high throughput. However, several challenges remain before CdTe photovoltaics reach full commercial maturity. This research is divided into two specific aims. The first is to investigate the optical and electronic properties of commercially available glass/TCO superstrates to identify those most suitable for high-performance CdTe devices. The second is to explore the mechanics of device structures that do not rely on magnesium-doped zinc oxide (MZO) as the n-type buffer layer.

To address the first aim, three glass/TCO superstrates (TEC10, TEC12D, and a proprietary glass/TCO stack) were compared using optical transmission and reflection measurements, along with Hall effect characterization. Devices fabricated using the proprietary glass/TCO exhibited superior performance, with higher current density attributed to increased optical transmission, especially above 700 nm.

To address the second aim, a series of experiments were conducted on alternative device structures that utilized CdSe. These experiments explored various CdSe thicknesses and $CdCl_2$ treatment conditions to evaluate their impact on CdSe based devices. While thicker CdSe

improved V_{OC}, it reduced J_{SC} due to parasitic absorption. To overcome this tradeoff, a $CdSe_xTe_{1-x}$ (CST) ternary alloy was introduced to help control Se diffusion and improve band alignment. Devices incorporating CST showed improved performance across both voltage and current, highlighting its effectiveness in balancing interface properties and enabling high-efficiency, CdSe based device architectures. These results underscore the importance of front contact optimization and buffer layer engineering in advancing CdTe photovoltaic efficiency.

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TABLE OF CONTENTS

LIST OF FIGURES

1 INTRODUCTION

Energy is an essential part of the modern world. From the lights in residential homes, to power large scale industrial processes, to powering large data centers for AI computing, electricity is a key necessity. With the innovation of more and more technology for the modern world, energy demand will only continue to rise. As of 2024, total global electricity consumption was estimated to be 27,000 TWh out of which about 1.5 – 1.7% i.e., 400 – 450 TWh was consumed for AI computing and crypto currency mining. By 2034, this is estimated to reach 34,000 – 38,000 TWh with nearly 7% or 2,700 TWh used for AI computing and crypto mining while addition of electric vehicles accounting of nearly 10% or 3,500 TWh of new electricity consumption.

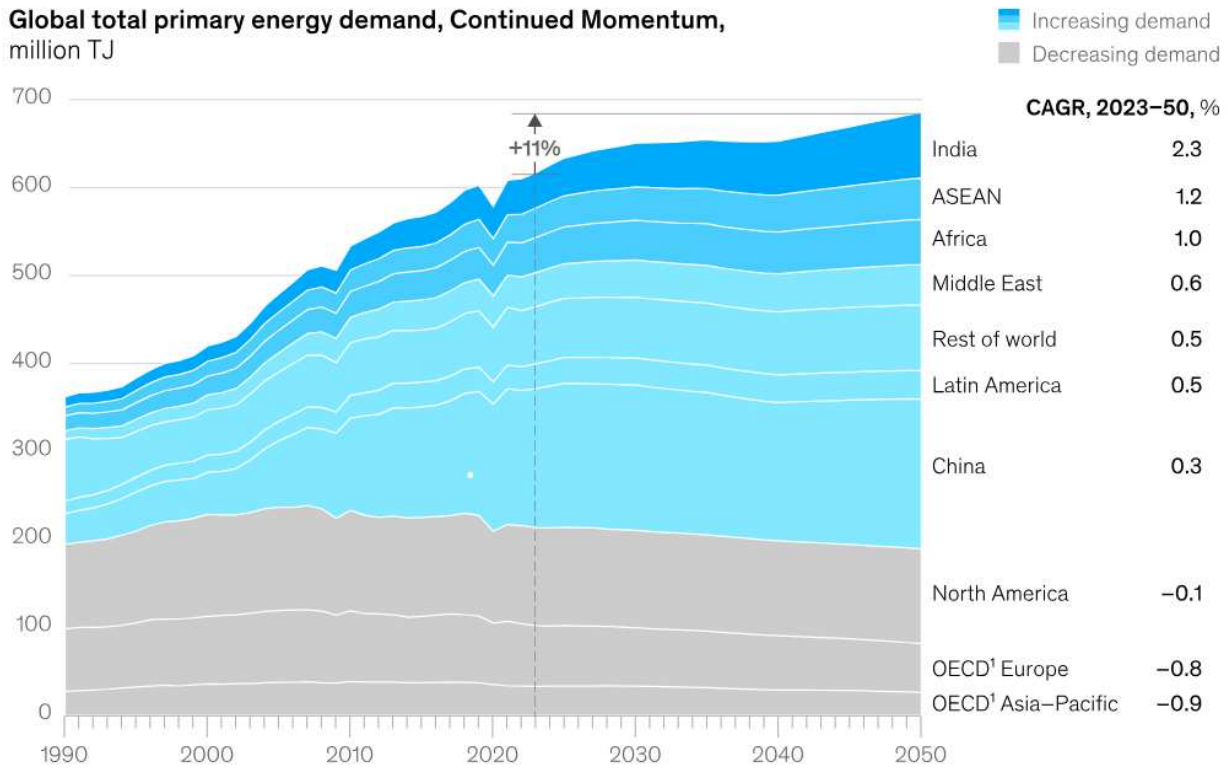


Figure 1.1: Graph depicting forecast energy demand by country. Imagen taken from [1].

To meet global demand, innovation of energy generation methods must be made, to aid in meeting global demand in a cost-effective way. Solar energy is currently the leading renewable energy solution with an installed capacity of about 1.6 TW of photovoltaics (PV) installed worldwide as of the end of 2024 [2]. Majority of the installed PV capacity is primarily comprised of mono-crystalline (c-Si) silicon technology. As of 2023 CdTe made up more than 30 GW_p (gigawatt peak) installed worldwide. Although a small fraction of the total installed capacity, CdTe offers significant advantages over mono-silicon.

CdTe PV is advantageous compared to most other technologies owing to the low cost of material, relative ease of manufacturing, and high manufacturing throughput. However, further improvements in cell efficiency are essential for the technology to become more impactful. One way to decrease the cost of technology is to improve the efficiency of CdTe solar cells while maintaining cost of manufacturing. The goal of this research will be to improve CdTe device performance through the investigation of the impact glass and transparent conducting oxide (TCO) has on devices performance, and the development of different CdTe devices structures that do not utilize MZO. Preliminary studies were conducted to investigate various commercial glass and TCO combinations for key material, optical and electronic characteristics. To properly assess new glass/TCO combinations a fabrication process was optimized to produce high performing CdTe devices that mimic generally known industry standard procedures to ensure research solution scale to commercial application.

1.1 Photovoltaics Basics

1.1.1 Radiation from the Sun

Photovoltaic devices convert energy from the sun in the form of light into energy. Due to its temperature, the sun primarily emits electro-magnetic radiation within the visible spectrum. This spectrum can be seen as the AM0 line on the plot below.

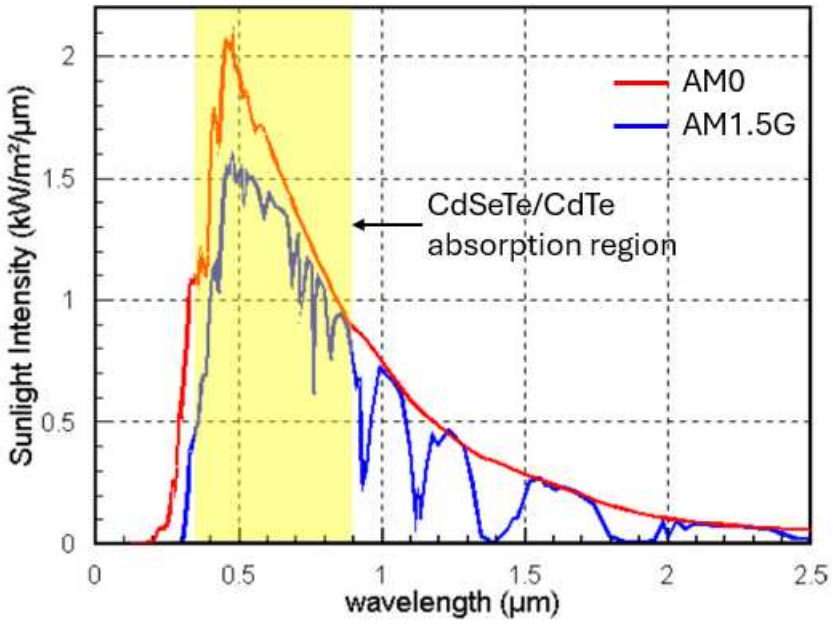


Figure 1.2: Graph of AM0 and AM1.5G spectrum. Highlighted in yellow is the absorption spectrum of CdSeTe/CdTe devices. Image taken from [3] and then modified.

AM0 represents the spectrum of irradiation from the sun in space. The blue line below is the AM1.5G spectrum, which is AM1.5G is a globally accepted standardized solar spectral irradiance distribution that approximates the solar radiation received at the Earth's surface at a 48.2° solar zenith angle, including both direct and diffuse components, for a clear-sky condition at mid-latitudes (around 37°N). The AM1.5G spectrum exhibits a jagged, non-smooth appearance compared to the relatively smooth AM0 spectrum. This irregularity in AM1.5G arises from wavelength-specific absorption and scattering by Earth's atmosphere. It is used as the

reference spectrum under Standard Test Conditions (STC) for testing and rating solar cells and modules. Standard Test Conditions (STC) are internationally defined parameters used to standardize the testing and performance characterization of photovoltaic (PV) devices. According to the International Electrotechnical Commission (IEC 61215) and the American Society for Testing and Materials (ASTM E948 and G173-03), STC specify the following conditions:

1. Irradiance: 1000 W/m² of total incident solar radiation,
2. Cell temperature: 25°C,
3. Solar spectrum: Air Mass 1.5 Global (AM1.5G), as defined by ASTM G173-03.

The AM1.5G spectral distribution corresponds to solar radiation received at the Earth's surface with the sun at a 48.2° zenith angle, for an observer located at 37°N latitude and 275 m altitude, under clear-sky conditions. It includes both direct normal and diffuse hemispherical components of sunlight. These standardized conditions ensure that measured photovoltaic performance metrics such as open-circuit voltage, short-circuit current, and power conversion efficiency are comparable across different technologies and testing facilities.

1.1.2 Semiconductor Basics

Materials are broadly classified into three categories based on their electronic and electrical properties: conductors, semiconductors, and insulators. This classification is primarily determined by the material's band gap. The bandgap of a material is the difference in energy between the valence band and the conduction band. The band gap represents the minimum energy required to excite an electron from a bound state in the valence band to a free, mobile state in the conduction band. Materials with no band gap or a very small one allow electrons to

move freely, behaving as conductors. In contrast, materials with wide band gaps inhibit electron movement under normal conditions and act as insulators. Semiconductors fall in between these two extremes, possessing moderate band gaps that enable controlled electrical conductivity, especially under thermal or optical excitation.

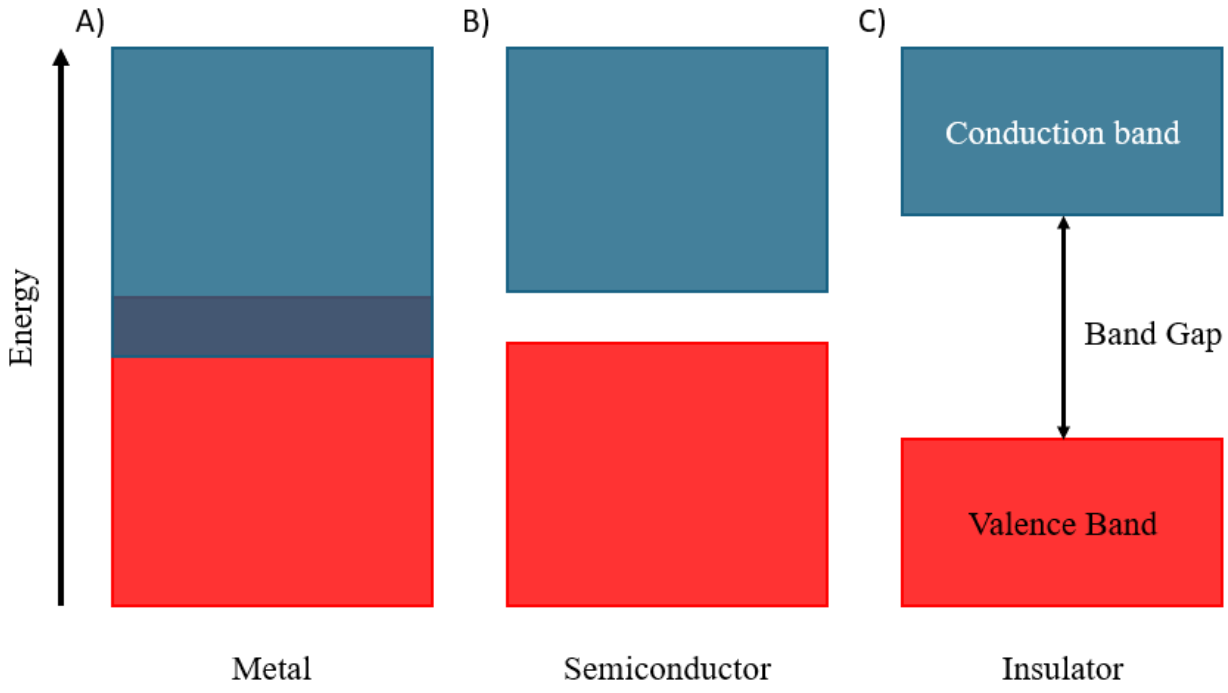


Figure 1.3: Schematic depicting the relative locations of the valence and conductions bands of a metal (A), semiconductor (B), and insulator (C).

As seen in figure 1.3(A), a conductor is characterized by an overlap in the valence and conduction band. Without a gap in energy between the bands, charge carries can move freely within the lattices. This is what characterizes metals and their high electrical conductivity. Figure 1.3(C) shows the band diagram of an insulator. An insulator is characterized by a large band gap separating the conduction and valence band. Due to the large band gap, thermal energy at room temperature is not sufficient to promote electrons to the conduction band and therefore, this material will resist conducting electricity at room temperature. Figure 1.3(B) depicts the bandgap of a semiconductor, unlike in the conductor there is a bandgap, and unlike the insulator the

bandgap is relatively small. The band gap is small enough that at room temperature, some thermally excited carriers can be promoted into the conduction band and contribute to conduction of charge. Due to this property, semiconductor materials can conduct charge carriers at room temperature and insulate near 0K.

On the periodic table, elemental semiconducting materials are either group IV, or an alloy between either group III and group V (called III-V semiconductors), or group II and VI (called II-VI semiconductors). Silicon is the most widely used semiconductor and is in group IV, gallium arsenide is a high performing III-V semiconductor, and CdTe is the most widespread II-VI semiconductor used in photovoltaic solar cells.

1.1.3 Generation of Charge Carriers

In semiconductors, the current flows due to two types of charge carriers: electrons and holes. Electrons are negative charge carriers; modeled as positive charge carriers. Electron-hole pairs form when an electron gains enough energy to jump from the valence band to the conduction band, leaving behind a void. This void behaves like a positive charge carrier, known as a hole and is often treated as a positively charged particle counterpart of an electron.

Electron hole pairs can be created thermally, or through absorption of incident radiation. If an incident photon has energy equal to or greater than the band gap of the semiconductor, an electron may absorb the energy of the photon and jump to the conduction band, creating an electron hole pair. This forms the basis for how charged carriers are created in photovoltaic devices.

1.1.4 Annihilation of Charge Carriers

While charge carriers are created through absorption of light, they are annihilated through recombining with the opposing charge carrier (and electron meeting a hole). This is aptly called recombination. There are two basic types of recombination, radiative recombination, and non-radiative recombination. As their names suggest, radiative recombination results in the release of a photon, usually of equal energy to the band gap, and non-radiative recombination is recombination without the emission of a photon. Radiative recombination is not as detrimental to device performance non-radiative recombination due to the emission of a photon equal to the band gap. This re-emission can then be reabsorbed within the lattice and create another electron hole-pair. Non-radiative recombination is more detrimental because the energy cannot be recaptured and turned into photocurrent.

Non-radiative recombination can occur through either defect state recombination, or interface recombination. Therefore, creating high quality absorber material with small number of detrimental defects as well as optimized interphases are key to reducing harmful non-radiative recombination. William Shockley and Hans-Joachim Queisser describe the thermodynamic efficiency limits that can be achieved through require elimination of all non-radiative recombination and having a device with only radiative recombination [4].

1.1.5 Doping

Doping is the process of intentionally adding defects (dopants) to the semiconductor to increase the density of electrons or holes. To illustrate this process, a diagram showing a silicon lattice is shown below.

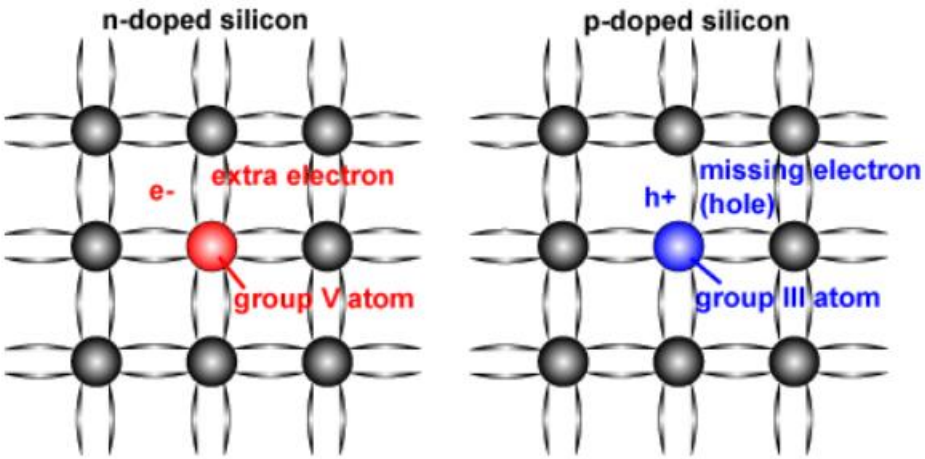


Figure 1.4: 2D representation of donor and acceptor dopants in a silicon lattice. Image taken from [5].

Silicon is a group IV element and therefore has four valence electrons. In a crystalline silicon lattice, each of those four electrons form covalent bonds with neighboring silicon atoms. Now replace some of those silicon atoms with a group V atom such as phosphorus or arsenic. Group V elements have five valence electrons. When incorporated into a silicon lattice, four of these electrons form covalent bonds with neighboring silicon atoms, while the fifth remains weakly bound to the Group V element. It takes a relatively small amount of energy to promote this fifth electron into the conduction band so it can participate in conduction of charge and may be deemed as a carrier. Once the carrier electron is free, the group V element becomes a positively charged ion, thus maintaining a net neutral charge on the material. Elements that donate an electron to the lattice are called donors. Increasing donors in the lattice increases the density of free electrons in the semiconductor. Therefore, the electron density within the semiconductor can be controlled by suitable incorporation of donors. Similarly, one can create holes within the lattice through replacing silicon with Group III elements such as boron. Boron has three valence electrons, and when bound within a crystalline silicon lattice creates a hole. Once this hole moves away from the boron atom (the boron atom accepts an electron) it becomes

a negative ion. Elements that accept electron in the lattice are considered acceptors. Thus, by controlling the concentration of acceptors in a material one can control the concentration of holes. Semiconductors doped with donor defects are called n-type due to the increase in electron concentration, and semiconductors doped with acceptors are p-type due to the increased hole concentration. It is important to note that while both materials have increased negative and positive charge carriers, both remain neutrally charged due to the formation of positive and negative ions within the lattice.

1.1.6 P-N Junction

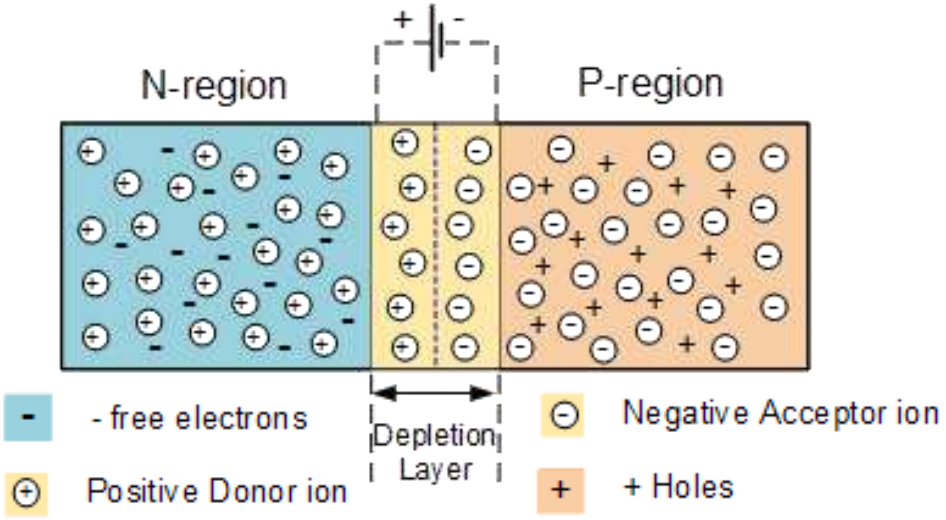


Figure 1.5: Diagrams showing a P-N junction with n-type (blue), p-type (orange), and he depletion region (yellow). Image taken from [6].

A P-N junction is formed when n-type and a p-type materials are brought together to form an interface junction. An electric field is formed between the stationary ions in each of the n-type and p-type material. This electric field acts as a barrier for most charge carriers in each material, thus keeping the electrons within the n-type material and holes in p-type material. This region in which the electric field exists and there are very little charge carriers is call the “space

charge region" or "depletion layer" and is key to the fundamental performance of photovoltaic devices. Fundamentally, most photovoltaic devices comprise one or multiple P-N junctions. The space charge regions of these junctions can be tuned via the concentration of dopants to change the width and strength of the space charge region.

1.1.7 The Photovoltaic Effect

Electrons and holes that are generated within the space charge region of the photovoltaic cell are separated due to the electric field present in the junction, which drives holes toward the p-type material and electrons toward the n-type material. The photovoltaic effect refers to this process—where light generates charge carriers and the built-in electric field separates them, resulting in the development of a voltage across the device. This separation of charge is what gives rise to the photovoltage of the cell. Cadmium Telluride Photovoltaics

Cadmium Telluride (CdTe), a semiconductor alloy, is an advantageous material for PV devices. It has a bandgap of ~1.45eV at 300K, which is close to optimal for single P-N junction, as well as can be manufactured using thin-film technology. The commercially viable high throughput manufacturing of high performance CdTe PV enables the technology to compete with leading edge monocrystalline silicon PV panels making CdTe the second most commercially implemented PV technology.

A homojunction is formed between two regions of the same semiconductor material with different doping types, such as a p–n junction in silicon. In contrast, a heterojunction involves a junction between two different semiconductor materials with differing bandgaps and electron affinities, such as the CdS/CdTe interface in thin-film solar cells. Heterojunctions introduce band discontinuities at the interface, allowing for enhanced control over carrier transport and selective

contact behavior, whereas homojunctions have a continuous band structure across the junction. CdTe PV devices in industry and at CSU are manufactured in a superstrate configuration. A superstrate configuration means the device is built starting from the side that will eventually face the light source, typically through a transparent substrate like glass. In this structure, layers are deposited in reverse order, beginning with a transparent conducting oxide (like FTO or ITO) on the glass, followed by the n-type window layer (such as CdS, CdSe, or $Mg_xZn_{1-x}O$), then the p-type CdTe absorber layer, and finally the back contact. Light enters the device through the glass superstrate, passes through the front layers, and is absorbed in the CdTe layer where electron-hole pairs are generated. This configuration is advantageous for CdTe solar cells because it allows high-temperature processing of the absorber and back contact layers without damaging the transparent substrate, and it simplifies large-area module manufacturing.

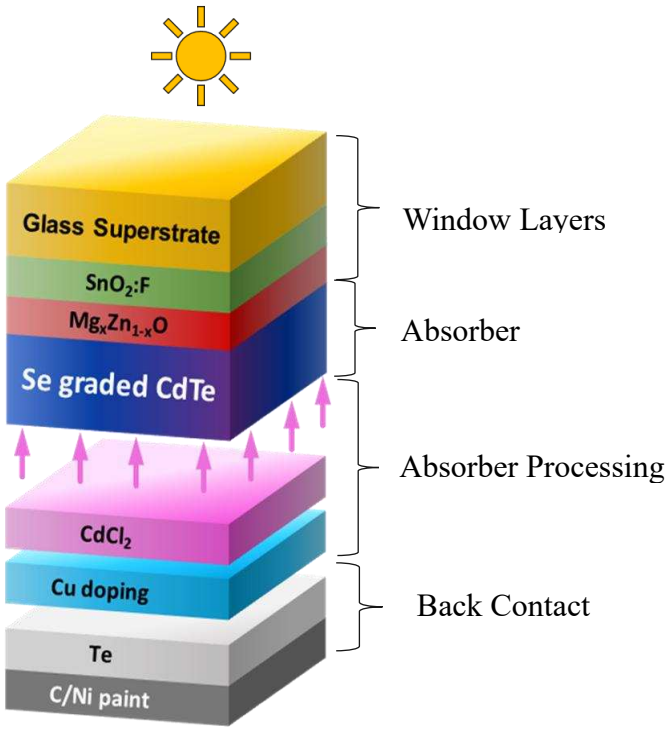


Figure 1.6: Diagram of the baseline device structure at CSU. (Not to Scale)

The schematic above depicts the baseline structure of PV devices fabricated at CSU. All layers before the CdTe absorber layer are considered window layers, followed by the CdTe layer referred to as the absorber, followed by the back contact. Incident light enters the cell through the glass at the top of the device. It must then pass through all window layers before being absorbed in the absorber where useful charge carriers are created and separated due to the electric field established at the PV junction. These charge carriers are then conducted through the back (holes) and front (electrons) contact of the PV devices to generate power.

1.1.8 Window Layers

Window layers are layers placed between incident radiation and the semiconductor absorber. Light must pass through these layers before they can be absorbed in the absorber and generate useful charge carriers. Thus, all window layers must be as transparent to the absorption spectrum of the semiconductor absorber, in this device CdTe (alloyed with Se as is explained later), as possible to maximize the energy available to be absorbed.

The first window layer and the basis for all CdTe PV construction is the glass substrate. Low iron soda lime glass is a cost-effective glass used due to its high transparency and relative affordability compared to alternatives. Boro-silicate glass offers a higher transmission of light than low iron soda lime glass but is cost prohibitive for most large-scale applications.

Deposited on the glass substrate is a transparent conducting oxide (TCO). TCO forms the front contact of these PV devices. It is highly n-type doped making it a degenerate semiconductor. A degenerate semiconductor is a semiconductor that is heavily doped to the point where the Fermi level lies inside the conduction band (n-type) or the valence band (p-type) rather than within the band gap as in typical (non-degenerate) semiconductors. This causes it to behave

more like a metal in terms of electrical conductivity. Thus, it is highly conductive and suitable to serve as the electron contact for the PV device. While there are many different materials that can be used as TCO they all have high bandgaps, around ~3.5 eV, making them transparent to most light that is desirable to be absorbed in the semiconductor absorber layer.

Following the TCO is the buffer layer, or a n-type window layer or both. Due to the extreme doping of TCO to make it an efficient front contact, and the relatively lower doping concentration of the p-type CdTe absorber, intermediate window layers are needed to avoid unfavorable effects from creating a P-N junction with a high disparity in doping concentrations. The detrimental effects of contacting CdTe to TCO are described elsewhere [7]. The buffer layer serves as a "buffer" between the TCO and CdTe and can as the n-type material that forms a P-N junction with the p-type CdTe. The n-type window layer commonly follows a buffer if it is not serving as the n-type material. Common n-type window layers include Cadmium Sulfide (CdS) Cadmium Selenide (CdSe) are some of the effective n-type window layers used in thin film CdTe PV. Magnesium doped zinc oxide ($Mg_xZn_{1-x}O$ or MZO) is used as both a buffer and n-type window layer for devices fabricated at CSU. A more detailed description and analysis of these layers is provided in latter sections of this work. Note, while the exact definition of buffer and n-type window layers differ, I will use the term "buffer" when discussion optimal n-type window layer thickness for device performance. This is not implying the n-type window layer is necessary acting like a buffer but is instead swerving as a buffer between the TCO and p-type absorber.

1.1.9 Absorber and Absorber Processing

After the buffer or n-type window layer, the p-type CdTe absorber is deposited. Theoretically, CdTe is supposed to be an intrinsic semiconductor, meaning it is neither n- nor p-

doped. However, CdTe films deposited by thermal processes such as evaporation, sublimation, or vapor transport deposition (VTD) typically exhibit p-type conductivity due to the formation of cadmium vacancies (V_{Cd}), which act as acceptor defects. This tendency arises because cadmium has a higher vapor pressure than tellurium, making it more likely to re-evaporate or sublimate during deposition. The resulting Cd-deficient (Te-rich) conditions promote the formation of V_{Cd}, leading to intrinsic p-type behavior in the as-deposited CdTe films. The CdTe film may be p-doped using arsenic, copper, antimony, phosphorous, etc. during or following the thin film growth to enhance the p-type characteristics.

CdTe after deposition requires further processing to passivate active defects detrimental to semiconductor performance and favorable grain growth of the as deposited film. Cadmium Chloride ($CdCl_2$) heat treatment is used to accomplish both. During $CdCl_2$ thermal treatment CdTe films undergo rapid recrystallization and grain growth creating a high performing absorber, capable of generating high voltage and current collection. A more detailed description of the $CdCl_2$ process and its effects are illustrated elsewhere [8]. To form an ohmic back contact as well as increase the p-type carrier concentration of CdTe absorbers, p-type dopants such as copper, arsenic, and/or phosphorous are incorporated into the absorber.

1.1.10 Back Contact

Development of material for suitable back contacts for CdTe devices has been a topic of extensive research in recent years. Due to the band structure of CdTe devices, particularly its high work function, it is difficult to find back contact material for efficient hole extraction. The work function is the minimum energy required to remove an electron from the Fermi level of a material to vacuum. In a photovoltaic (PV) device, a high work function is crucial for forming an efficient p-type contact, as it ensures good energy level alignment with the valence band of the

absorber, enabling efficient hole extraction and minimizing barrier formation at the back contact. Most materials used have a hole barrier that prevents effective extraction of the holes. This barrier is called the Schottky Barrier, which is formed when creating a junction between a semiconductor and a metal. Schottky barrier is the potential energy barrier formed at the junction between a metal and a semiconductor due to the difference in their work functions. When a metal with a lower work function is in contact with an n-type semiconductor, or a metal with a higher work function is in contact with a p-type semiconductor, a barrier forms that restricts carrier flow. This barrier affects charge carrier transport across the interface, often resulting in rectifying (diode-like) behavior. In photovoltaic devices, an undesired Schottky barrier at the contact can hinder efficient carrier extraction and be detrimental to the device performance. In the device structure shown in figure 1.6, a Cu doped back surface of CdTe along with a thin Te film (~30 nm) thermally evaporated at room temperature forms an effective contact to act as an Ohmic contact and mitigate the formation of a Schottky Barrier.

1.2 Device Structure

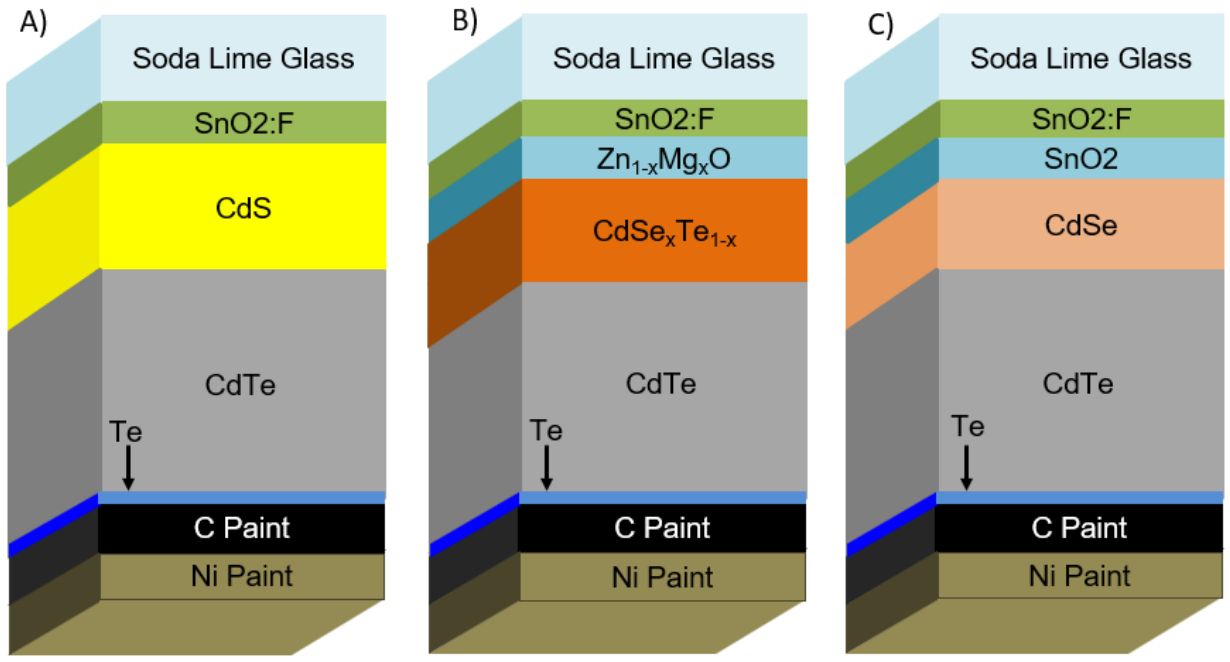


Figure 1.7: Figure of three different device structures, a CdS based device structure (A), a MZO based devices structure (B), and the chosen CdSe based device structure (C).

Structures depicted in figure 1.7 are the deposited, pre-$CdCl_2$ treated device structures. Figure 1.7C depicts the chosen deposited device structure for this optimization project. TEC12D by NSG Pilkington was chosen as the starting substrate. The substrate consists of a low iron soda lime glass with a thin film of fluorine doped tin oxide (FTO) acting as TCO and another thin film of intrinsic tin oxide (SnO_2) on top that acts as a buffer layer. Glass is received with these layer prefabricated from the manufacturer. Deposited on top of the fluorine doped tin oxide (FTO) is CdSe, which acts as a selenium source for grading the absorber as well as an-type window layer. Following CdSe is CdTe. After CdTe is deposited, the absorber undergoes a vacuum vapor $CdCl_2$ activation treatment, to promote grain growth and interdiffusion of selenium into the absorber. This process is explained in more detail here [8]. Next, the absorbers were doped with copper, to improve carrier concentration and create an ohmic back contact. A thin layer of tellurium is then

deposited on the back to aid in the creation of the back contact. To finish the device carbon and nickel paint are sprayed onto the back of the devices.

To better understand why this structure was chosen, it's helpful to reference earlier designs and show how they evolved into the current configuration. Figure 1.7A shows a CdS based device. Cadmium Sulfide was first used as a pigment in the 1800s. It was used to create vibrant yellow paints dubbed the name "Cadmium Yellow." In 1954 it was utilized to manufacture 6% efficient CdS/$Cu_{2-x}S$ photovoltaic device. This was one of the first observations of the photovoltaic effect in II-VI semiconductors. Later, CdS was utilized as the n-type material to form a PN junction with thin film CdTe. These heterostructure devices utilized a superstrate configuration with CdS being deposited on top of TCO and then CdTe following on top of the CdS layer. The primary roles of CdS serve as both a window and n-type window layer or n-partner in CdS/CdTe PV devices. Due to its lower bandgap, it would parasitically absorb a large portion of blue light from the AM1.5G spectrum. This parasitic absorption prevented significant portion of high energy blue photons from reaching the absorber and contributing to photo current generation and thus limiting the performance of CdS-based devices.

To solve this issue, new buffer/window layer materials with higher bandgaps were developed. MZO was among the most advantageous due to the ease of tuning the bandgap of the device through varying the concentration of magnesium in the material. An example of this structure is seen in figure 1.7B. The larger band gap allowed more transmission of sun light to the absorber making a greater portion of the incident light available for charge creation, thus increasing the power output of PV devices compared to CdS based devices.

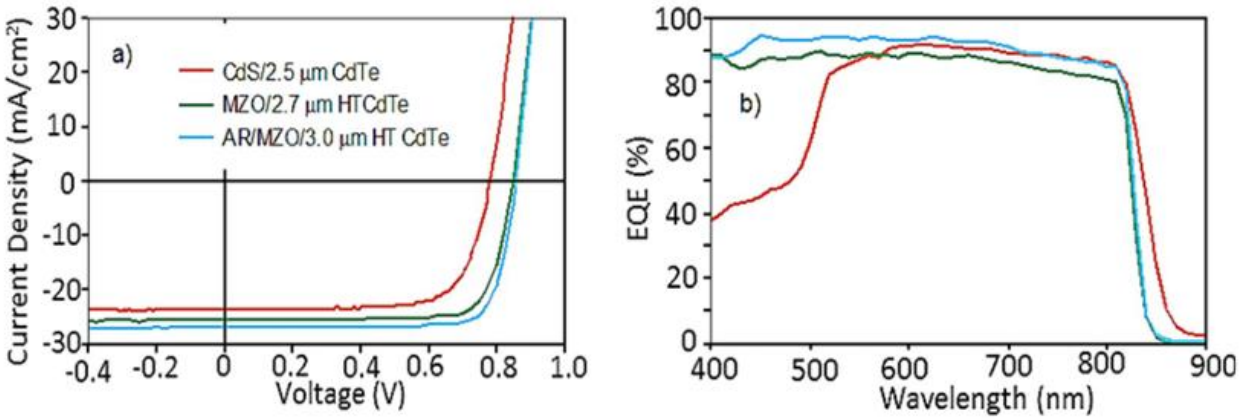


Figure 1.8: JV curves (a) and EQE curves (b) comparing CdS to MZO to and antireflection coating with MZO. Image taken from [9].

As seen, in figure 1.8b, the addition of MZO improved the EQE response between 400nm and 500nm of light. This resulted in a J_{SC} improvement as seen in the figure 1.8a. While, quite advantageous, the technology has not yet been utilized commercially.

For better representation of commercial technology, CdSe based device structures were chosen for this research. CdSe has a smaller band gap than both CdS and MZO. Thus, to prevent large amounts of parasitic absorption, the thickness of the CdSe layer must be optimized to allow maximum transmission of light and to provide an adequate buffer. Unlike CdS, CdSe readily diffuses into CdTe during $CdCl_2$ processing. This poses an advantage to manufacturing. By optimizing the deposited CdSe layer thickness and $CdCl_2$ processing conditions, devices can be produced with enough CdSe to function as a buffer layer while also acting as a Se source for grading the CdTe absorber, leading to improvements in both voltage and current collection. Incorporating selenium into the CdTe absorber lowers its bandgap, allowing absorption of more light, thus higher current collection. Thus, this structure was chosen for optimization due to its widespread commercial use making findings through this research applicable for industry.

1.3 Why is a Buffer/N-type Window Layer Essential for High Performance CdTe

As shown in earlier description in device structures, each utilizes a buffer or an n-type window layer that resides between the TCO and absorber material of the device. This layer is essential for high performance devices for a multitude of reasons. Buffer/ n-type window layers can serve as much better n-type material to form a PN junction with CdTe due to more similar doping concentration as well as aiding in improving band alignment, carrier extraction, and reduced recombination. If these layers are not included a poor junction is formed between CdTe and TCO. This poor junction can behave like a leaky diode, limiting built-in potential and narrowing the effective depletion width. This results in increased interface recombination and suppressed carrier separation, both of which reduce open-circuit voltage (V_{OC}) [7], [10], [11], [12]. Thus, buffer layers and n-type window layers are utilized to form more favorable junctions with the CdTe absorber and suppress the parasitic diode behavior.

1.3.1 Voltage and Current Balance

To maximize the efficiency of a PV device the output power of the device must be maximized. The maximum theoretical power and thus efficiency was described by William Shockley and Hans-Joachim Queisser in 1961. In doing so they describe the maximum theoretical performance of various semiconducting materials with differing bandgaps when illuminated by a black body spectrum of 6000K and a device temperature of 300K. These are known as the Shockley Queisser limits. In 2016 Sven Rühle expanded upon this topic through the calculation of the Shockley Quessier limits of devices illuminated under AM1.5G spectrum with device temperatures of 25˚C [13]. These calculated limits represent the maximum efficiency possible for a single junction terrestrial PV device based among its bandgaps. Plotted

below is the tabulated data of open circuit voltage (V_{OC}), and short circuit current density (J_{SC}) which are key parameters for the calculation of solar cell efficiency.

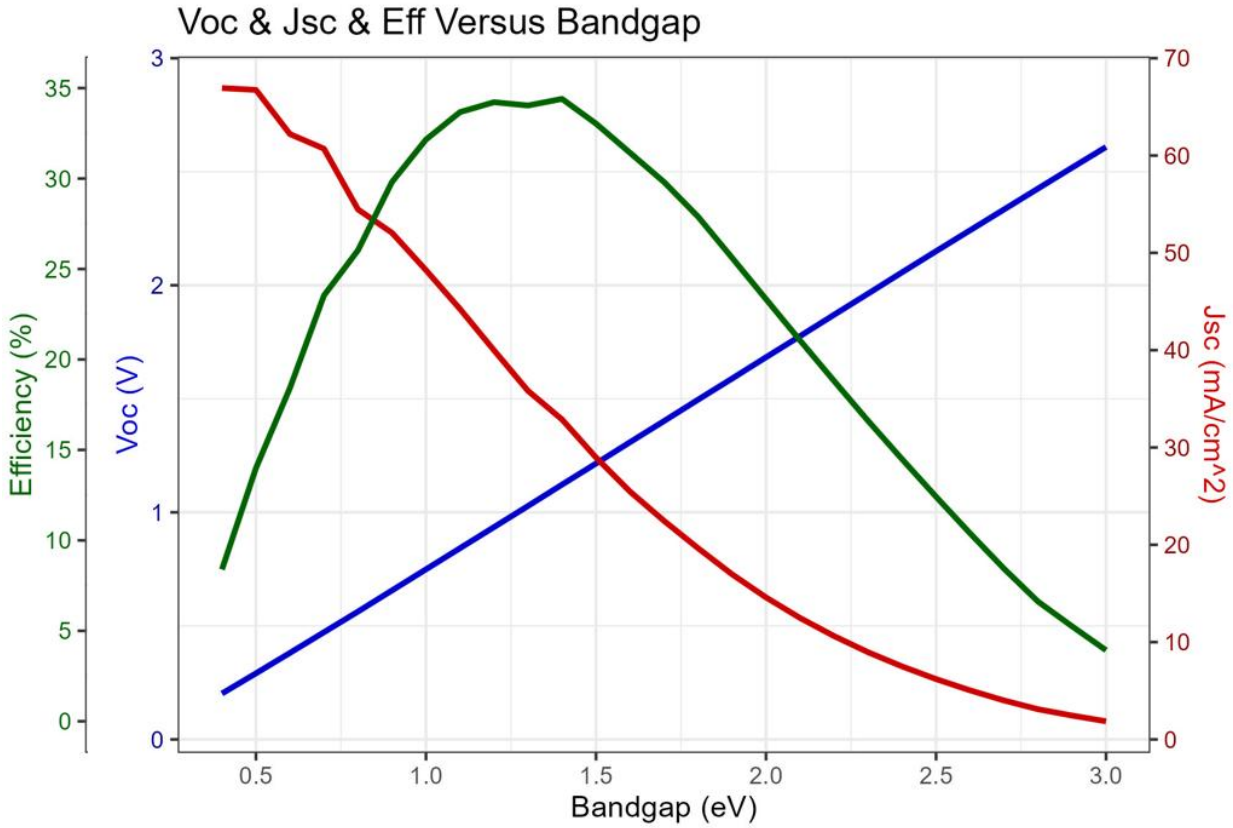


Figure 1.9: Theoretical maximum V_{OC} (Blue), J_{SC} (Red), efficiency (Green) versus bandgap. Data from Rühle [13].

As seen, voltage increases with bandgap and J_{SC} decreases with bandgap. To maximize efficiency, the product of V_{OC} and J_{SC} must be maximized. This occurs around 1.5eV which is the bandgap of CdTe, making it highly suited for single junction PV terrestrial applications. Graphed in figure 1.9 are the Shockley Quessier limits as calculated by Rühle for efficiency versus bandgap.

The maximum efficiency occurs at 1.4eV. Note, fill factor is another important parameter in calculating efficiency and is not shown in the pervious plots but was used to calculate the efficiency plot. This illustrates the importance of maintaining a balance between both the V_{OC}

and the J_{SC}. To attain a good balance between V_{OC} _ and J_{SC} with the current CdTe device structures a proper front contact mut be utilized. Without a buffer layer and a suitable n-type window layer poor performance will result due to increased recombination at the front contact and poor diode behaviors from poor PN junctions formed with TCO. A window layer stack that is made of poor materials or is too thin will result in poor voltage while too thick of a stack will result in large amounts of parasitic absorption or inefficient carrier extraction hurting current collection.

1.4 Key Advantages and Challenges of Utilizing CdSe as a N-type Window Layer

1.4.1 Advantages

During the $CdCl_2$ activation treatment Se diffusion from CdSe and Te diffusion from CdTe creates the ternary alloy $CdSe_xTe_{100-x}$ (CST) [14]. CST is a versatile material, as shown by Akash et. al. the bandgap of the material can be controlled via the selenium concentration.

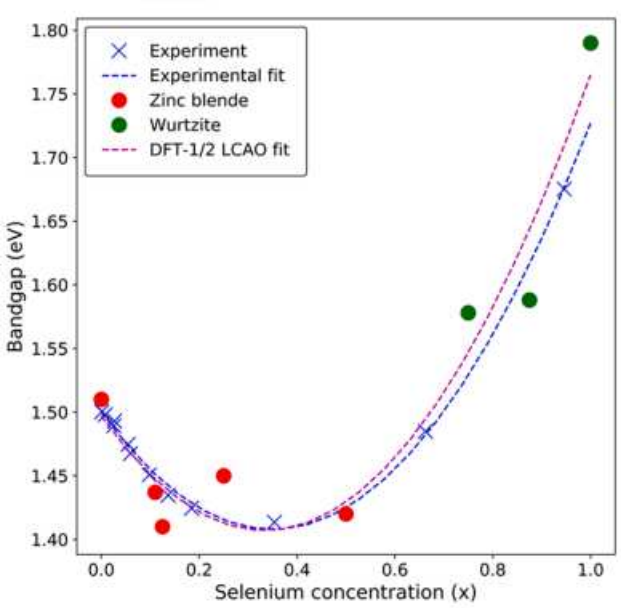


Figure 1.10: Experimental and modeled bandgap versus the selenium concentration withing CST. Graph from Akash et. al. [15].

As seen, the bandgap forms a U-shape, with the lowest bandgap occurring around a selenium fraction of 0.4. Increasing the Se concentration withing the CST increases the bandgap favorably while maintaining its n-type nature, allowing for an effective n-type window layer. Through deposited CdSe and $CdCl_2$ treatment, Se concentration can be controlled throughout the absorber to maximize PCE. Ideally, the resulting device would have a region of high Se concentration acting as a n-type window layer as well as the n-type material. The front of the p-type absorber would have a selenium fraction of ~0.4. $CdSe_{0.4}Te_{0.6}$ (CST40). CST40 has the lowest bandgap possible of the CST ternary alloy at a bandgap of ~1.4eV. This allows for maximum absorption of the AM1.5G spectrum and thus boosts J_{SC}. Following this region, the Se would taper off until binary CdTe alloy without Se is left. Due to the discrepancy in bandgaps, a transition is formed between the CST and CdTe. Shah et. al. describes this transition and model it.

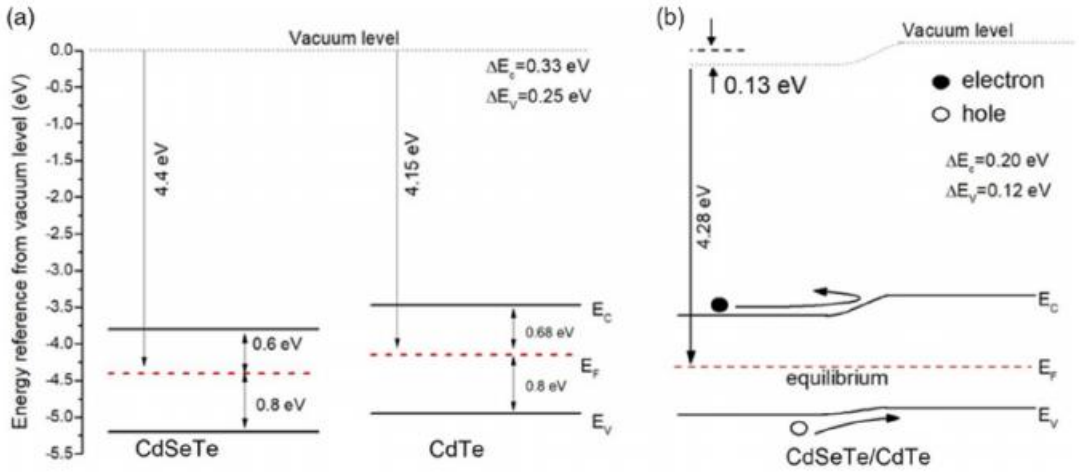


Figure 1.11: a) Energy band position of CdSeTe an CdTe based on the UPS measurement. b) Projected band alignment at CdSeTe/CdTe interface. Image taken from Shah et. al. [15].

As seen, the transition from CST to CdTe allows for more efficiency carrier extraction though repelling electrons to the front contact and allowing holes to travel to the back contact.

By controlling deposited CdSe thickness as well as $CdCl_2$ treatment one can fabricate a device with an adequate “buffer”, optimal Se gradient, and improved carrier extraction.

1.4.2 Challenges

To utilize the bandgap of the absorber to its fullest extent the n-type window layer must be as transparent as possible to the device’s absorption region. Historically, CdS devices have suffered from parasitic absorption losses due to its bandgap of 2.4eV. This causes losses in the blue region, resulting in poor current collection. To mitigate parasitic absorption as well as voltage loss the CdS layer thickness must be optimized. The CdS layer must be made as thin as possible while remaining thick enough to act as a n-type window layer between the TCO and absorber. CdSe is a chalcogenide similarly to CdS and has a bandgap of 1.7eV. When used to form a n-type window layer it faces many of the same challenges that CdS does. Excess CdSe has been shown to be detrimental to device performance due to large amounts of parasitic absorption and high rates of recombination at the front interface. Too thin of deposited CdSe will result in a large voltage losses due to insufficient “buffer” between the TCO and CdTe absorber. One key difference between CdS and CdSe is that CdSe interdiffusion into CdTe more readily than CdS during $CdCl_2$ activation treatment. Thus, as stated earlier, the resultant Se grading throughout the device depends on both deposited CdSe thickness as well as $CdCl_2$ treatment. Wet $CdCl_2$ treatments have been shown to be effective at producing high quality devices that utilize similar structures to was shown in figure 1.7C. Yet, research has not yet confirmed if this is achievable utilizing vapor $CdCl_2$ processing utilized here at CSU.

1.5 Summary and Goal

In summary, this research aims to investigate two key areas in CdTe photovoltaics. The first goal is to study the glass/TCO stack to achieve optimal opto-electronic properties, as identifying suitable materials and configurations is essential for further improvements in CdTe device efficiency. The second goal is to investigate CdSe based device structures as well as how to fabricate them to identify key device structures and fabrication processes.

2 LITERATURE REVIEW

This research is focused on studying the impact that the substrate and front contact layers have on device performance as well as the improvement and development of CdSe based devices without $Mg_xZn_{1-x}O$ at CSU Center for Advanced Photovoltaics (CSU CAP). An extensive literature review was conducted to get a historical context of the development of substrates and front contact materials, highlight areas of needed research, and to get a detailed understanding of work done in the field.

2.1 The Effect of Glass and TCO on Device performance

The glass substrate serves as the base for all other layers to be deposited on while TCO serves as the electron contact of the devices. Other layers are included such as sodium barriers and anti-reflection coatings to improve the stability and performance of the glass/TCO stack. Typically, these layers are deposited together by the glass manufacturer and then shipped to a PV manufacturing facility for deposition so other layers. Therefore, this research will focus on the holistic attributes of glass/TCO combination and how that affects performance of these devices. Incident radiation first passes through the glass and transparent conducting oxide (TCO) layers

of the solar cell, so this front layer plays an important role in overall CdTe device performance. The starting substrate affects performance in two keyways: it influences light transmission and impacts film morphology.

2.1.1 Glass/TCO Substrates Effect on Performance

Bittau et al. compared the optical, electronic, and physical morphology of five differing glass/TCO combinations including Titanium-doped indium oxide (ITiO), tin-doped indium oxide (ITO), aluminum-doped zinc oxide (AZO), and fluorine-doped tin oxide (FTO). They correlated these properties to device performance to highlight how glass/TCO affect device performance.

Table 2.1 Summary of TCO properties. Table gotten from Bittau et al. [12].

Material	FTO (SLG)	ITO (SLG)	AZO (SLG)	AZO (BSG)	ITiO (BSG)
Thickness [nm]	450	250	900	700	230
R_{sheet} [Ω/ϒ]	10	4	10	10	8
Carrier Density × 10^{20} [cm^{-3}]	5.6	18.0	3.7	3.6	3.9
Mobility [cm^2/V s]	25	34	19	26	89
Resistivity × 10^{-4} [Ω cm]	4.4	1.0	9.0	6.75	1.8

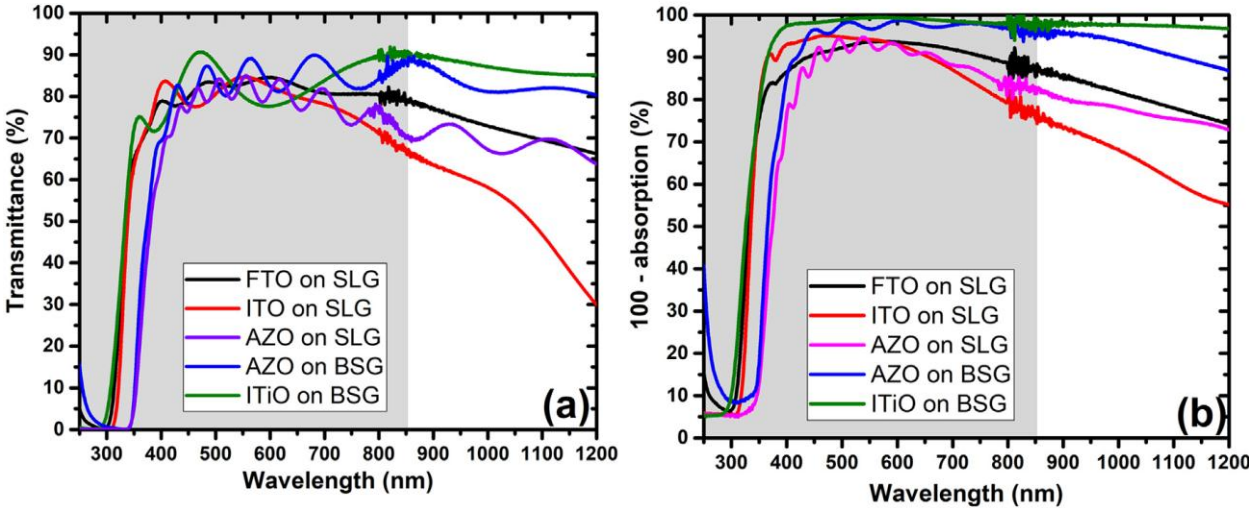


Figure 2.1 Transmission (A) and 100-absobrtion (B) of different glass and TCO combinations. Shaden region represents the absorption region of CdTe. Image taken from Bittau et al. [12]

They chose 4 mm thick low-iron soda lime glass (SLG), and 1mm thick boro-aluminosilicate glass (BSG) for the comparison. Details of various differentiating TCO films and electronic properties are shown in table 2.1. A Varian Cary 5000 UV–VIS–NIR spectrophotometer was used to measure the optical properties shown in figure 2.1. To yield $100 - \mathrm{A}(\%)$ spectrum was calculated by equation 2.1.

$$100 - \mathrm{A}(\%) = \mathrm{T}(\%) + \mathrm{R}(\%) \qquad 2.1$$

Where T (%) is the percentage of light transmitted through the glass/TCO, R (%) is the percentage of reflected light due to the glass/TCO. The $100 - \mathrm{A}(\%)$ spectrum represents the total available light if reflection was minimized at air/glass and TCO/air interfaces. Therefore, it represents potentially available light if absorption was the only optical loss of light within the glass/TCO stack. As seen in figure 2.1a, the ITO has a loss in transmittance in longer wavelengths, the increase in absorption in longer wavelength suggests larger amount of absorption in free carriers due to the high carrier concentration in ITO. ITiO does not exhibit this loss due to its low concentration of free carriers and maintains extremely low absorption at

longer wavelengths. Comparing the AZO deposited on SLG to BSG shows BSG strongly improves the transparency of the stack, due to its lower iron content compared to the soda lime glass. ITiO and the AZO on BSO have very high $100 - A(\%)$ within the visible and near IR regions, but there is a difference in UV absorption. This is due to the lower bandgap of the zinc oxide based TCOs compared to the indium oxide (In_2O_3) TCOs with bandgaps of 3.3eV to 3.93eV, respectively.

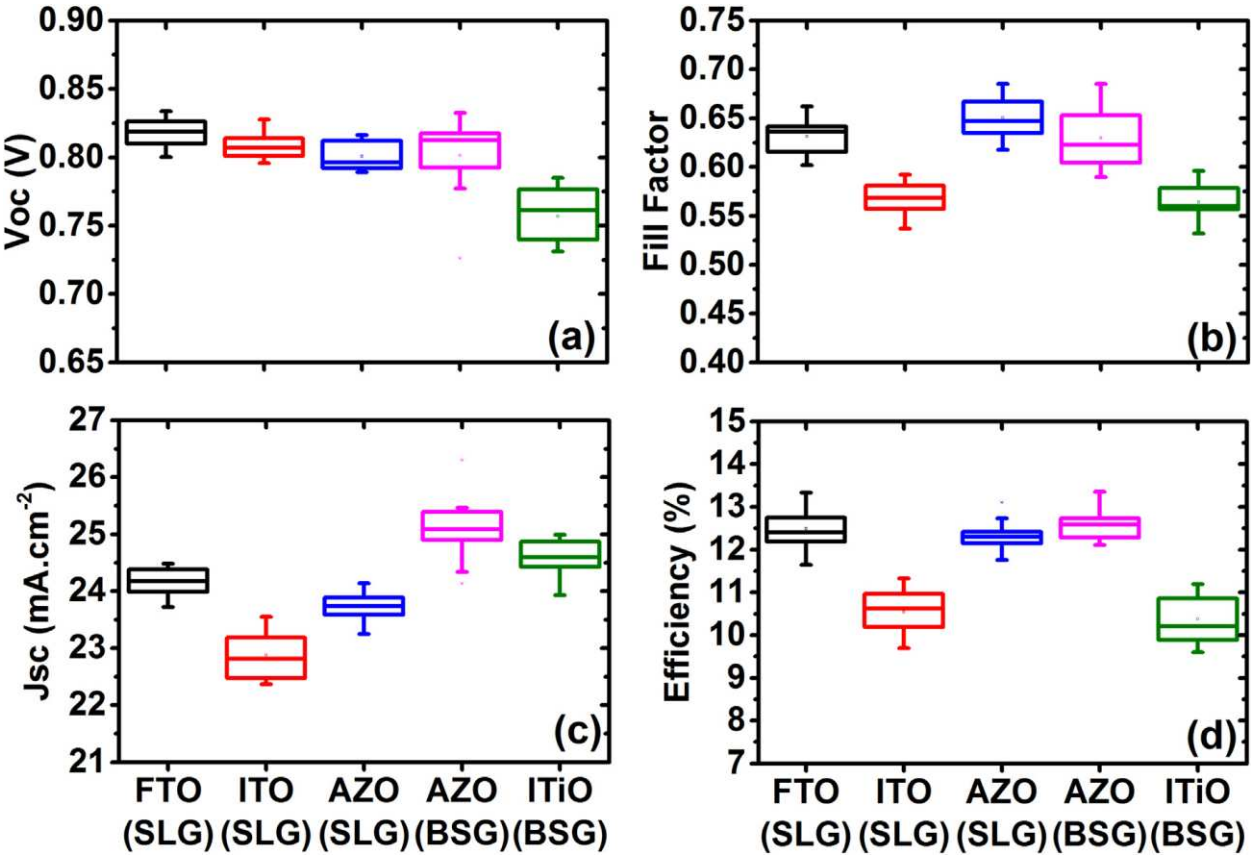


Figure 2.2: JV parameters of devices deposited on different glass/TCO stacks. Plot taken from Bittau et al.

Figure 2.2 shows device performance results with various glass/TCO stacks. AZO on SLG produced comparable devices to FTO on SLG. When comparing it to AZO on BSG, improvement in the current collection was reported. This is due to the higher transmissivity of the BSG glass, allowing for more light to reach the semiconductor absorber that contributes to

photo-current generation. ITiO also exhibited high J_{SC} due to its high transmissivity. Despite having great opto-electronic properties (high transmission, and good conductivity due to highly mobile charge carriers) it performed poorly in fill factor and V_{OC}. The morphology of the film stack matters, and the interface between the glass/ITiO/MZO plays an important role in device performance. The growth of MZO on ITiO may be suboptimal causing recombination losses at the interface and decreasing device V_{OC} and fill factor. ITO also performed poorly mainly due to higher parasitic absorption of longer wavelength light due to its high concentration of free carriers. This results in devices with lower J_{SC}.

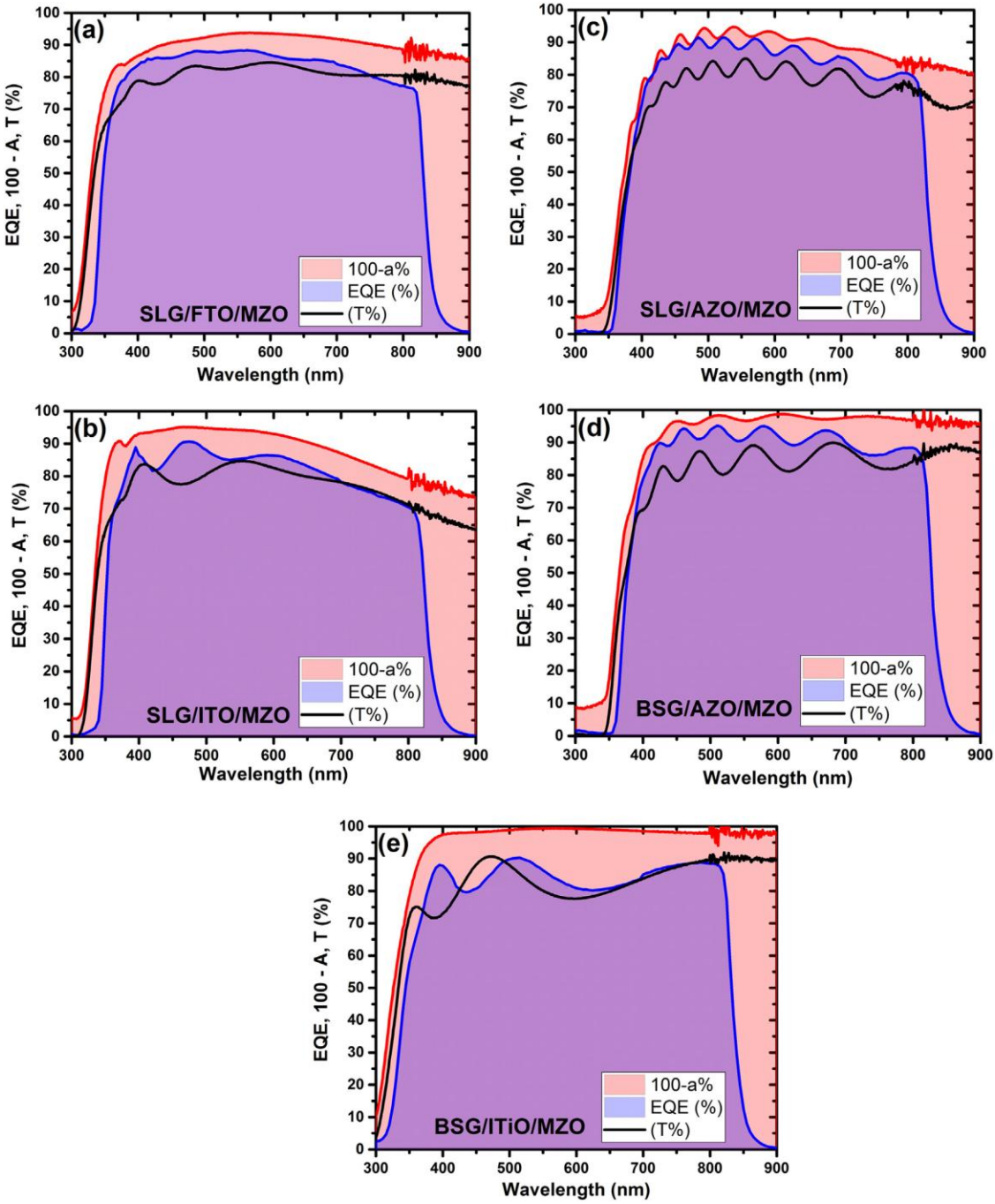


Figure 2.3: The EQE spectra of CdTe solar cells deposited on FTO on SLG (a), ITO on SLG (b), AZO on SLG (c), AZO on BSG (d) and ITiO on BSG (e) plotted against transmission and 100 – absorption data. Image taken from [12].

Figure 2.3 depicts transmission, $100 - A(\%)$, and the external quantum efficiency (EQE) spectra of each glass/TCO overlayed to show at what point in the spectral losses are most

significant. As seen, the EQE response is larger than that of the transmission through just glass/TCO. This is due to a decrease in the interface reflectance when adding additional layers onto the glass/TCO stack such as MZO and CdTe. Optimal device performance for each glass/TCO if EQE response was equal to the $100 - \mathrm{A}(\%)$ spectra. To minimize this gap, photocurrent generation, and extraction efficiencies must be maximized. To fully quantify the gap in 100 – A and EQE response due to differing glass/TCO the two equations below were used.

$$J_{SC,max} = q \int_{250\ nm}^{826\ nm} \big(100 - A(\lambda)\big)\Phi(\lambda)d\lambda \qquad 2.2$$

$J_{SC,max}$ is the theoretical maximum J_{SC} after absorption losses in the glass/TCO. To visualize this, it would be if the EQE response was equal to the 100 – A(%) spectral response. The variable q is the charge of an electron, $A(\lambda)$ is the wavelength depended on absorption, and $\Phi(\lambda)$ is the photon flux of sunlight on earth (AM1.5G).

$$J_{SC,EQE} = q \int_{250\ nm}^{826\ nm} EQE(\lambda)\Phi(\lambda)d\lambda \qquad 2.3$$

$J_{SC,EQE}$ is the J_{SC} produced by the device under AM1.5 according to its EQE spectral response, and $EQE(\lambda)$ is the EQE response of the device. The quotient between $J_{SC,EQE}$ and $J_{SC,max}$ give the fraction of potentially available photons converted by the devices. Results from this analyses are summarized in table 2.2.

Table 2.2: Table of the fraction of potentially available photons converted by the device.

SLG/FTO	SLG/ITO	SLG/AZO	BSG/AZO	BSG/ITiO
86%	84%	90%	86%	81%

As seen, the AZO on SLG was most efficient at converting available photons not absorbed by the glass/TCO stack. This was more so than AZO on BSG converting only 86% of potentially available photos. This was equivalent to the SLG/FTO device. Following, SLG/ITO devices converted 84% of potentially available photons while BSG/ITiO converted the smallest fraction of 81%.

This published literature served as a comprehensive study of how glass/TCO affect the performance of MZO/CdTe devices This published study contributes to this research through the investigation of the impact of glass/TCO on MZO/CST/CdTe devices. After optimization of a CdSe based structure, this important research helped by guiding the development and investigation of optimal glass/TCO for CdSe based solar cells.

2.2 CdS

2.2.1 Role of CdS in CdTe Photovoltaics

CdS is a II-VI semiconductor with a band gap of 2.42eV. Making it transparent to majority of the solar spectrum except for high energy blue photons. Fabrication of the CdS layer can be accomplished through a plethora of fabrication processes including physical vapor deposition (PVD), chemical-bath deposition (CBD), and pulse DC or RF-sputtering techniques. Following deposition CdS films require annealing to promote grain growth and improve its quality. Each method produces n-type CdS thin films due to intrinsic donor defects such as sulfur vacancies and cadmium interstitials. CdS has a wurtzite crystalline structure deposited on tin oxide (SnO_2).

CdS is a good candidate for a window and an n-type window layer for CdTe devices due to its desirable opto-electronic properties, and ease of fabrication. Its intrinsic donor defects

during deposition makes it a favorable partner to CdTe to form a PN junction and its higher band gap allows most of the incident radiation to reach the CdTe absorber.

There are two main issues with CdS and its use in CdTe PV. The first is its bandgap of 2.42eV which is transparent to most of the AM1.5G spectrum except for blue light. Light absorbed in the CdS does not create useful charge carriers, therefore all light absorbed in the CdS is detrimental for the current generation in the device. This phenomenon is known as parasitic absorption.

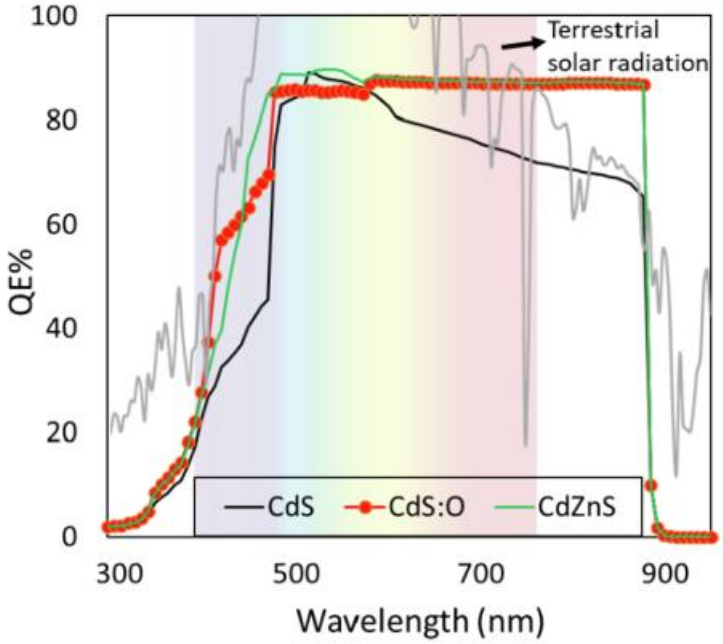


Figure 2.4: EQE response of devices utilizing three different CdS based window layers. Figure taken from [16].

Below 500nm the EQE response of the CdS/CdTe devices drop due to parasitic absorption of the high energy blue photons within the CdS window layer. To minimize this effect the thickness of the CdS layer must be minimized to reduce the amount of parasitic absorption while also maintaining enough thickness to establish a window layer between the CdTe and TCO. Too thin of a CdS film leads to sufficient thickness to avoid pinholes formed into the film

which shunt the device and hurt performance. Thus, to establish a good buffer, some parasitic absorption must occur within the CdS layer. The second issue is due to CdS wurtzite structure which has a ~11% lattice mismatch between it and CdTe. This large mismatch can lead to a large defect density as well as more pronounced defects in grown CdTe films [17]. These two issues have been the primary drivers in limiting CdS/CdTe films to efficiencies of ~13%. Thus, research focused on the development and research of other buffer layers and window layers to improve upon the shortcomings of CdS.

2.3 Advancements in Performance Utilizing MZO and Selenium

Magnesium doped zinc oxide (MZO) is a buffer layer with a tunable band gap. The band gap is tuned through varying the concentration of magnesium in the material. This feature allows for optimal band alignment with subsequent layers, leading to higher efficiency. ZnO has a band gap of 3.28eV, which only increases with magnesium incorporation. This wider band gap allows higher transmission of the incident solar spectrum to the absorbers making for a higher percentage of irradiation available for charge creation. Thus, increasing the current collection of PV devices compared to CdS based devices. This is apparent when looking at the EQE plot of CdS and MZO based devices. As seen, the use of MZO increased the EQE response in the lower wavelength as compared to CdS due to its higher band gap.

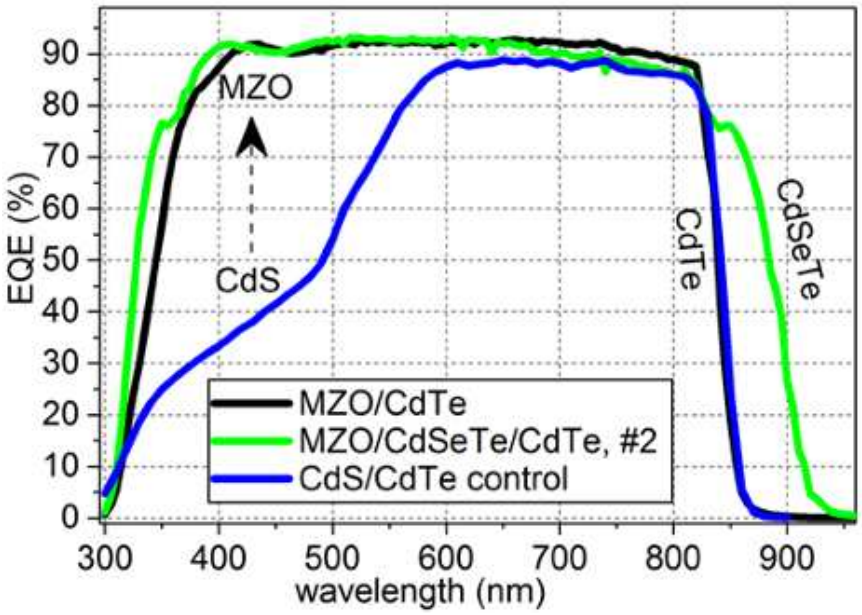


Figure 2.5: EQE response for three differing devices structures, CdS, MZO, and MZO/CST. Figure taken from [18].

MZO also provides a boost in V_{OC}. This improvement in performance is due to better interphase passivation and band alignment. MZO is also stable at higher temperatures than CdS, allowing elevated temperature processing. Elevated temperature processing leads to better V_{OC} and fill factor. This allowed for improvement of MZO/CdTe device performance to efficiencies of 18.7%. This is explained in detail literature publishing by Munshi et. al. [19].

Incorporation of selenium into the absorber allowed further improvements to device performance. Incorporating selenium (Se) into CdTe forms an alloy called cadmium selenide telluride, or CdSexTe1−x (CST). At around 40% selenium concentration ($CdSe_{0.4}Te_{0.6}$ or CST40), the bandgap is approximately 1.4 eV which is narrower than CdTe. Bilayer devices were created with both CST40 and CdTe, with CST40 being at the front and CdTe at the back. After $CdCl_2$ activation, the selenium from the CST and tellurium from CdTe diffuse through a portion of the absorber. This created a Se graded absorber, and thus a bandgap graded absorber[8]. The narrower bandgap of CST40 allows a greater amount of current collection in the

near IR region, while the graded bandgap assists in carrier extraction. This is seen in figure 2.5, with the bump in EQE response of MZO/CST/CdTe devices in the near IR region. Typically, a lower band gap decreases the overall voltage of the devices. This is not seen in the gradient bilayer devices despite the lower band gap at the front of the devices due to the passivating effect of selenium on in the absorber. Selenium fills defects in the CdTe lattice and improves charge carrier lifetimes and subsequentially voltage which makes up for losses due to its smaller band gap [20].

2.4 CdSe

Cadmium Selenium (CdSe) is also a chalcogenide n-type window layer like CdS, therefore they share similar properties. CdSe also takes on a wurtzite structure, and when deposited is n-type due to natural n-type defects. Its bandgap is ~1.7eV, therefore it must be relatively thin as to not cause excessive parasitic absorption. To give more process flexibility CdSe is typically paired with a very thin buffer layer such as intrinsic tin oxide (SnO_2) which is easily deposited on top of TCO. This thin buffer gives the devices resiliency to extra thin CdSe, making it so optimal device performance can be achieved over wider set of process conditions.

2.4.1 Role of CdSe in CdTe Photovoltaics

Bastola et al. have optimized a similar structure and have identified key processing steps to create high performing CdSe based solar cells. An experiment conducted by them varied the thickness of CdSe. All other processing steps and conditions can be read in this published literature [21].

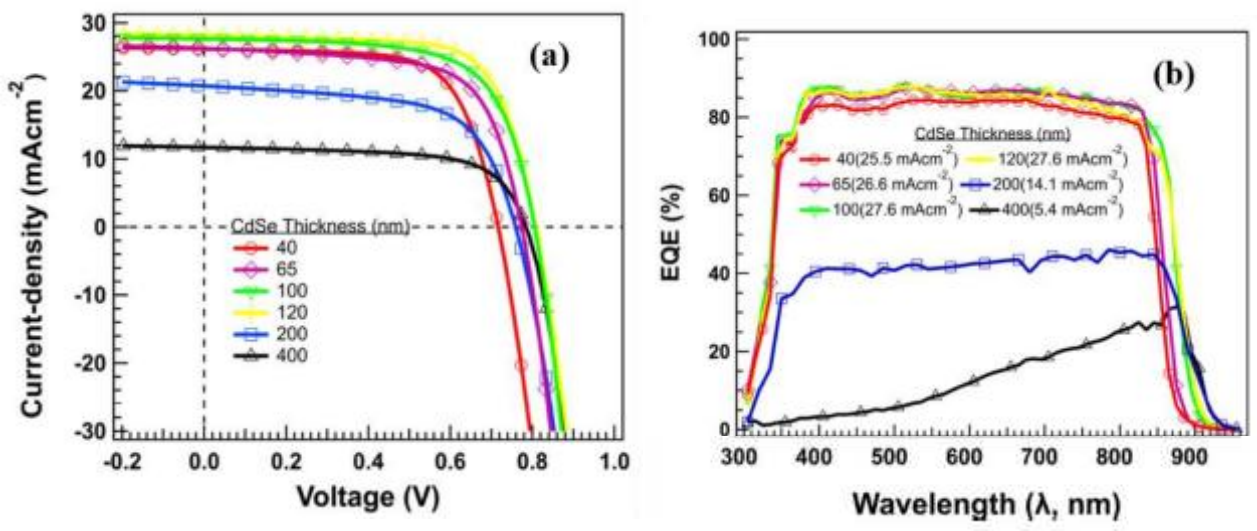


Figure 2.6: JV (a) and EQE (b) results from varying CdSe thickness. Image taken from [21].

As seen in figure 2.6, varying CdSe thickness has a large effect on J_{SC} and a small effect on V_{OC}. Both follow a similar trend where the performance increases with increasing CdSe thickness until 120nm, any thickness greater than 120nm perform worse in both V_{OC} and J_{SC}. Where thicker devices lost J_{SC} across the spectrum can be seen in the EQE plot, figure 2.6 (b). Each thickness appears to have good EQE response across the spectrum except for 200nm and 400nm of CdSe where parasitic absorption is occurring across the entire spectrum. This suggests 200nm and up of CdSe was too thick for these process conditions and resulted in a large layer of CdSe parasitically absorbing light, reducing overall J_{SC}. A second experiment was conducted where the copper annealing temperature was varied from 200˚C – 260˚C on devices with 200nm of CdSe.

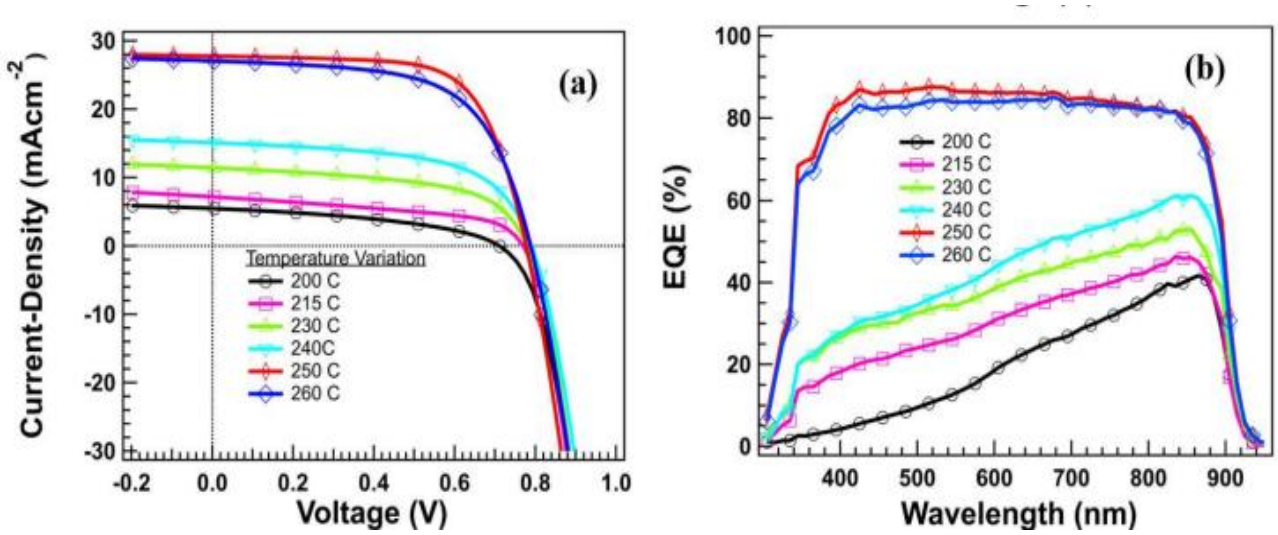


Figure 2.7: JV (a) and EQE (b) results from varying copper annealing temperatures (200˚C – 260˚C). Image taken from [21].

As seen, there is a positive correlation of copper annealing temperature to device performance up to 250°C. Although, due to there not being a baseline annealing plate at the same temperature, it is difficult to gauge whether the increase in performance is due to the annealing temperature, the copper, or both. Nevertheless, this process was able to passivate the front interface of the device and prevent majority of the parasitic absorption caused by excess CdSe.

Another piece of literature published by Liu et al. dives deeper into these samples with spectroscopic methods such as electron backscatter diffraction (EBSD), cathodoluminescence (CL), as well as other device measurements such as capacitance, and EQE measurements. They use these measurements and imaging techniques to describe what they call a 'remnant CdSe layer' with remnant meaning after $CdCl_2$ treatment. This layer was seen cross sectional images of the 400nm CdSe devices described in the pervious publication.

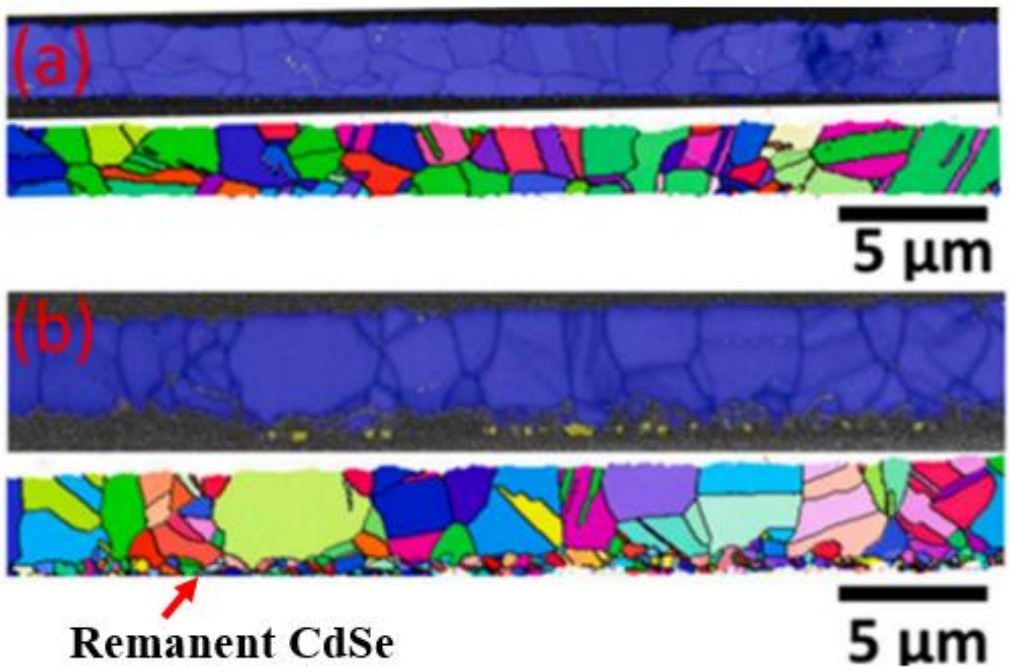


Figure 2.8: Cross sectional EBSC images of 120nm (a) and 400nm (b) of CdSe devices. Image taken from [22].

As seen in the EBSD images, the 400nm CdSe device has a remaining layer of CdSe with very small grains. When these grains are analyzed using cathodoluminescence (CL), they appear to have become highly photoactive due to the $CdCl_2$ treatment. The grain boundaries of the remnant CdSe layer that were dark in comparison to the grain interiors, indicated they may be centers for recombination despite having $CdCl_2$ diffused along them. The remnant CdSe layer is detrimental to device performance due to its high photoactivity and small grains. High photoactivity of the remnant CdSe layer parasitically absorbs light across the majority of the CdTe absorption spectrum, decreasing available light to the absorbers and decreasing overall photocurrent generation. The smaller the grains the higher the density of grain boundaries, and if these grain boundaries are sites for recombination, they would decrease V_{OC} and fill factor due to high rates of recombination at the front. The high temperature copper annealed plates were not included in this manuscript, therefore the mechanism for increased performance with increasing copper annealing temperatures remains unknown.

These two published articles highlight the necessity for proper alloying structures for high performance CdSe/CdTe devices. Excess CdSe results in poor performance due to high parasitic absorption, as well as high interface recombination rates. This facilitates the necessity for more research on these structures and the connection of process conditions to device performance. This research will be the focus on the development and optimization of a similar structure with differing absorber processing. At CSU we use sublimation for both the $CdCl_2$ activation treatment and copper doping process. Thus, there is a necessity for the development of new structures and processing methods to create high performance devices that are applicable to industry and will serve as a good platform for comparing glass/TCO combinations for CdSe based device structures.

3 METHODOLOGY

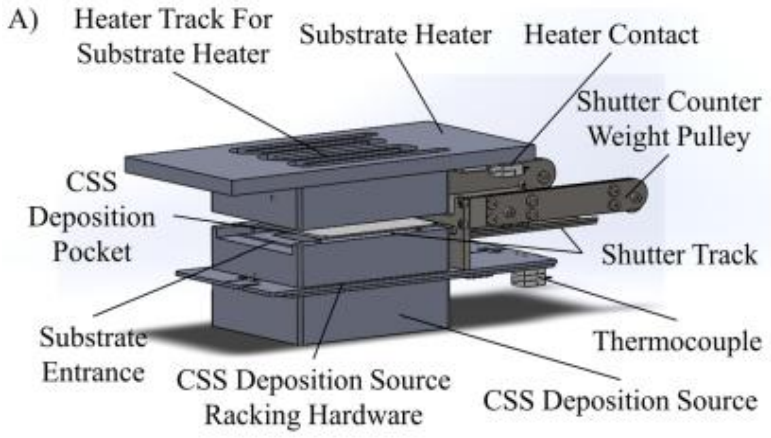
3.1 Device Fabrication

CSU receives glass/TCO substrates from glass vendors. Typically, the glass received is a Transparent Electric Contact (TEC) series by NSG Pilkington. The glass manufacturer cuts the 2mm thick glass into 3.6” X 3.2” rectangles. To clean the glass prior to deposition, glass substrates are placed in a bath of isopropyl alcohol (IPA) for thirty minutes. They are then rinsed and ultrasonic cleaned for an hour using the International Products Corporation’s Micro-90 Cleaning solution. They are then rinsed and ultrasonic cleaned for another hour in deionized water. Substrates are dried using IPA vapor.

MZO is deposited on devices via a RF sputter deposition process. Process conditions for deposition are 5mTorr at 3% oxygen in argon. The target used has a composition of 11% MgO

with 89% ZnO. Substrates are not intentionally heated during MZO film growth. Film thickness is typically about ~100nm.

CdSe, CST, and CdTe are deposited via sublimation within the Advanced Research Deposition System (ARDS). An in-depth description of the system can be found here [23]. The ARDS consists of 9 sublimation stations allowing deposition of multiple layers without breaking vacuum. As the system was configured during this investigation, CdSe, CST, and CdTe can be deposited and undergo a $CdCl_2$ treatment without breaking vacuum. Before absorber deposition, the glass/TCO substrates are preheated to bring the substrate temperature up. Typical deposition temperatures consist of the source temperatures of ~575°C for CdSe and CST, and ~560°C for CdTe deposition. Substrate temperatures range from 440°C to 475°C and will be noted when different. Films thicknesses are measured via XRF counts or a Bruker stylus contact profilometer. Process gas during film deposition is maintained at ~40mTorr of pure nitrogen.



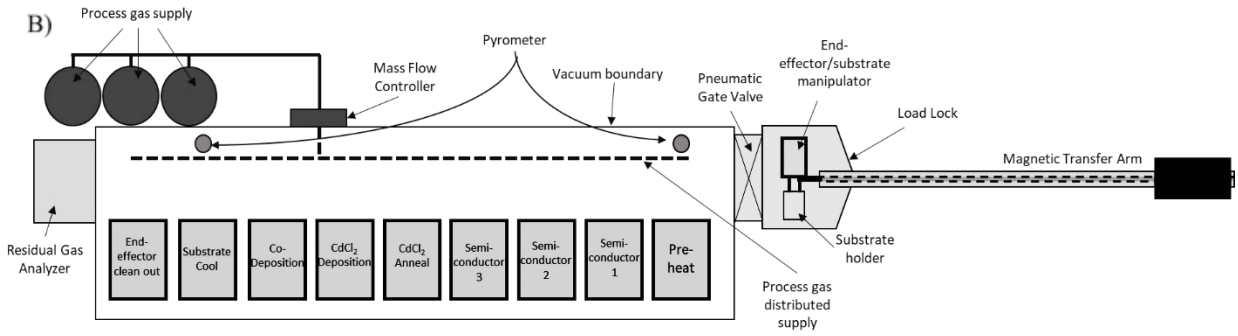


Figure 3.1: Schematic of sublimation station (A) and Advanced Research Deposition System (ARDS) (B). Image taken from [23].

The $CdCl_2$ activation treatment is performed within the ARDS via annealing films within $CdCl_2$ vapor. A more in-depth description of this process can be found here [23]. Typical process conditions for $CdCl_2$ consist of a ~450°C source temperature, and a 387°C substrate temperature. The time of treatment depends on thickness and composition of absorber layers. During $CdCl_2$ treatment the system is maintained at 40mTorr of 2% oxygen in nitrogen. The Exceptions to these conditions will be noted. After treatment, the films are allowed to cool in vacuum for three minutes. After sufficient cooling films are taken out of the chamber and rinsed in deionized water to remove excess $CdCl_2$ deposited on the surface.

Substrates were then transferred to a separate chamber for copper doping. The copper chamber has three different stations, preheat (P1), CuCl deposition (P3), and annealing (P2). To start, films are preheated for 2 minutes with heater temperatures at 330°C. Then they are transported to the CuCl source where they are treated with CuCl for 270 seconds. The source temperature of the CuCl source is ~190°C and the substrate temperature is ~170°C. Substrates are then moved to the anneal station in situ where they are annealed at 200°C for 9 minutes. After the substrates have sufficiently cooled, they are transferred from the machine and taken to

the tellurium evaporator. A 30nm layer of tellurium is deposited on the back of the absorber, via evaporation.

Substrates were then taken to the paint booth where subsequent carbon and nickel paint is sprayed onto the back of the film to form the back contact. After sufficient drying, the films are delineated into 25 small area solar cells via shadow mask media blasting. Resulting cells had an approximate area of ~0.62 cm^2. An alternate process utilizes a disposable shadow mask. After painting, the disposable shadow mask is then removed, and the remaining film can be carefully removed via media blasting. This results in 16 1.3 cm^2 cells. Indium is then soldered onto the exposed TCO after blasting to ensure good front contact for measurements.

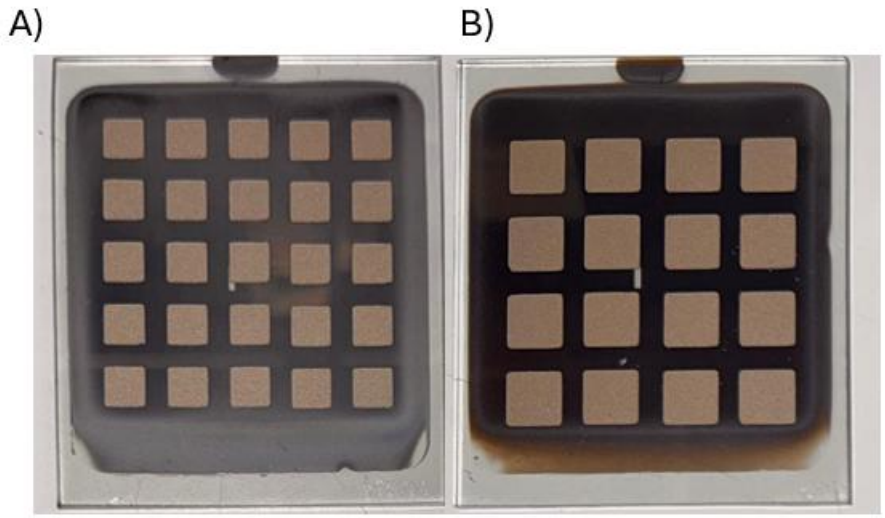


Figure 3.2: Picture of 25 0.6cm^2 area devices (A) and 16 1.3cm^2 area devices (B) before excess films removed.

3.2 Measurement and Characterization Methods

To compare different aspects of glass/TCO combination as well as develop an optimized fabrication process and plethora of measurement and characterization methods were used. These measurements can be utilized to develop a comprehensive understanding of the impact of glass

and TCO on device performance, as well as to establish process conditions for creating a CdSe based structure.

3.2.1 Optoelectronic Measurements

As stated, both the glass and TCO are window layers of the device. To quantify their optical properties, it is useful to obtain transmission and reflection data across the absorption spectrum of CdTe. These spectrums quantify the amount of light transmitting to the absorber and thus the total available power available to the absorber. The PerkinElmer Lambda 2 UV-Vis spectrometer was used to take the transmission and reflectance spectra across 400nm – 900nm of light. Before measurement, all glass/TCO are cleaned via the typical lab cleaning process to ensure the spectra is not affected by contaminants from the cutting and shipping process.

Two plots were generated with the transmission and reflection spectra of each glass/TCO. The first is a simple transmission plot, which was used to assess the baseline transmission of the glass/TCO. The next is a 100 – absorption (100-A) plot which utilizes the reflection data as well as the transmission data. To yield the plot, the equation 3.1 was used.

$$100 - \mathrm{A} = \mathrm{T} + \mathrm{R} \qquad 3.1$$

Equation 3.1 assumes that the transmission, reflection, and absorption sum to 100. The 100-A spectra represent the total possible transmission if reflection was minimized. This is a useful plot to assess the compatibility of glass/TCO with anti-reflective coatings. Glass/TCO with a high performing 100-A spectrum would yield a better return on investment regarding light transmission when anti-reflective coatings are incorporated.

The UV-Vis spectrometer was also used to measure the transmission and reflection spectra of 120nm CdSe films. Utilizing the transmission and reflection data, a Tauc plot was

created to assess the bandgap of the deposited CdSe film. A Tauc plot is a graphical methods used to assess the bandgap of semiconducting material utilizing the absorption spectra of the material. To compute the absorption coefficient from reflection and transmission data beer-lambert law is rearranged to yield equation 3.2.

$$\alpha = -\frac{1}{t}[\ln(T) - 2\ln(1 - R)] \tag{3.2}$$

In equation 3.2, α is the absorption coefficient, and t is the thickness of the film. For a direct bandgap semiconductor, Fermi's Golden rule tells us that the absorption coefficient as a function of energy is proportional to the joint density of states of the material [24]. This relationship is shown in equation 3.3.

$$\text{For } \hbar\omega > E_g, \qquad \alpha \propto \left(\hbar\omega - E_g\right)^{\frac{1}{2}} \tag{3.3}$$

To make Tauc plots of direct bandgap semiconductors such as CdTe or CdSe, energy is plotted on the x-axis while the square of the absorption coefficient is plotted on the y-axis. This results in a linear region near the bandgap of the material as described by equation 3.3. A line is fitted to the linear region of the graph, and the point where this line intersects the x-axis represents the bandgap of the material. An example of this relationship can be seen in the plot below as well as a more in-depth explanation of this relationship can be read here [24].

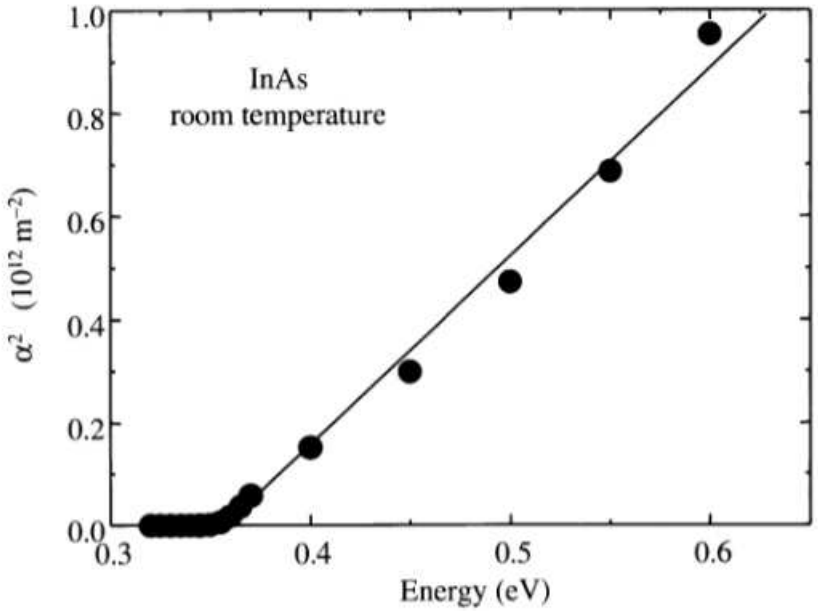


Figure 3.3: Plot of the absorption coefficient versus photon energy of InAs at room temperature. The bandgap was found to be 0.35eV through extrapolating the absorption to zero. Image taken from [24]

To assess the electronic properties of the TCO Hall Effect measurement were used. Hall Effect measurements help to understand the doping levels, carrier mobility and electrical conductivity of various TCO films. An in-depth description of the theory behind hall effect measurements can be found here [25]. This is critical to study to develop a better understanding of how the electronic properties of the TCO affect performance from completed devices. Each glass/TCO combination was isolated into three 1cm^2 squares with a laser to avoid geometric effects on the measurement. Indium was then soldered onto the vertices of each square to ensure proper electrical contact with the hall effect measurement system.

3.2.2 Spectroscopy (SEM)

Scanning electron microscopy (SEM) is a powerful tool to look at film morphology. SEM images were taken of TCO, MZO, and CdSe surfaces to characterize film morphology. The morphology of these films affects subsequent film growth. Therefore, different window layers

will result in differing absorber layers and may require different process conditions for optimal performance. SEM was also be used to characterize the morphology of the CdSe surface. To investigate the sublimation deposition method of CdSe and compare it to other methods such as evaporation used at other institutions.

3.2.3 Current Voltage Measurements

Current density-Voltage (JV) measurements are the most widely used PV device characterization method. The measurement is performed by varying the applied voltage and measuring the current of the PV device under a simulated 1000 W/m^2 AM1.5G spectrum. Doing so yields a diode curve which useful parameters can be extracted from such as open circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF), and power conversion efficiency (PCE).

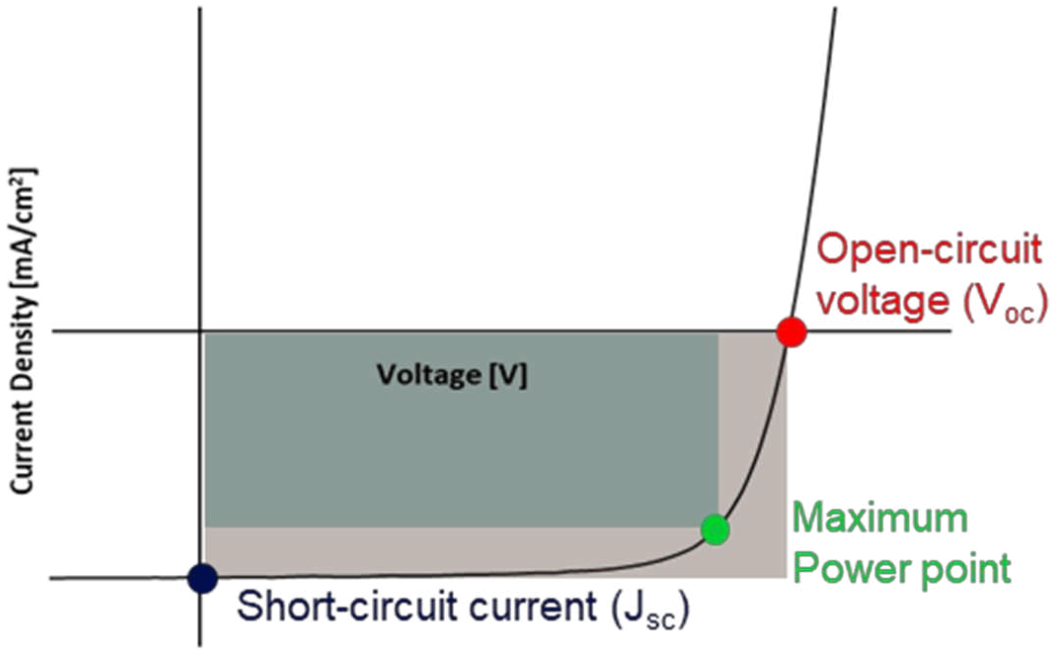


Figure 3.4: Diagram of a JV curve with V_{OC}, J_{SC}, and max power point labeled.

$$PCE = \frac{V_{OC}\, J_{SC}\, FF}{P_{in}} \quad 3.4$$

As seen in the diagram, J_{SC} is yielded from where the curve intersects the voltage axis, V_{OC} is yielded from where the curve intersects the current axis. The fill factor can be visualized graphically by the "squareness" of the JV curve. Represented by the ratio of the smaller blue square to the larger red square in the visual. A perfectly square curve where V_{OC} and J_{SC} are the max per point would translate to a 100% fill factor. Equation 3.4 describes the relationship between these three parameters to the PCE. Where P_{in} is the power of irradiation onto the PV device which is equal to 1000 W/m^2 under standard testing conditions. Each of these factors relate to key aspects of the PV device, making JV measurements a powerful tool for connecting device processing to performance.

Open circuit voltage is a good indicator of the overall quality of a PV device. V_{OC} of PV devices are primarily controlled by the material bandgap, doping, and the amount of recombination present within the PV device. A materials bandgap is proportional to the theoretical maximum V_{OC} available to a PV device. Thus, CdTe with a bandgap of 1.5 eV has a larger theoretical voltage than silicon at 1.1 eV. Doping also plays an important role in the V_{OC} of a PV device. Higher carrier concentrations allow for a greater potential in energy to develop across the P-N junction, allowing for higher V_{OC}. Recombination also plays a very important role in generating Voltage. The theoretical V_{OC} is achieved in an absorber that is only limited by radiative recombination, as described by Shockley Queisser. Any non-radiative recombination occurring within the bulk of the absorber or at interphases within the device negatively impact overall V_{OC} of the device. Therefore, V_{OC} can be used to gauge the quality of the device produced. Two processing parameters that have a large impact on V_{OC} are the thicknesses of

various layers, as well as the $CdCl_2$ activation treatment. Suboptimal thickness of the window layer stack cause shunting to occur inside the device, thus decreasing overall V_{OC}. Suboptimal $CdCl_2$, may cause insufficient passivation of defects and material interphases within the device. Insufficient passivation within the devices increases recombination and negatively impacts V_{OC}.

Short circuit current density is directly correlated to the amount of light reaching the absorber, the bandgap of the absorber, and the extraction efficiency of the front and back contact of the device. The more light transmitted to the absorber, or the less light that is parasitically absorbed within the window layer of the device, the more current can be produced. Thus, this relates to the thickness of the CdSe window layer. The layer must be thin enough to allow for maximal transmission of light while also maintaining a "buffer" between the absorber and TCO. Devices produced with lower J_{SC} may exhibit too thick of a CdSe layer that is causing large amounts of parasitic absorption. In researching this optimal structure, the bandgap of the absorber and the consistency of the front and back contacts should remain unchanged, ensuring they do not significantly impact J_{SC} results. Extraction efficiency will be investigated as part of the preliminary research of how glass/TCO affect MZO based CdTe PV devices.

Fill Factor is a complex parameter that incorporates many different aspects of device performance. To be put simply it can be calculated by the equation below.

$$FF = \frac{V_{mp}\, J_{mp}}{V_{OC}\, J_{SC}} \tag{3.2}$$

Where V_{mp} is the voltage at the max power point, and J_{mp} is the current density at the max power point. Where the max power point is located depends on the diode ideality factor as well as parasitic resistances within the PV device. The diode ideality factor is representative of what

predominant recombination mechanisms are present within the device. Parasitic resistance can be represented by the circuit drawn below.

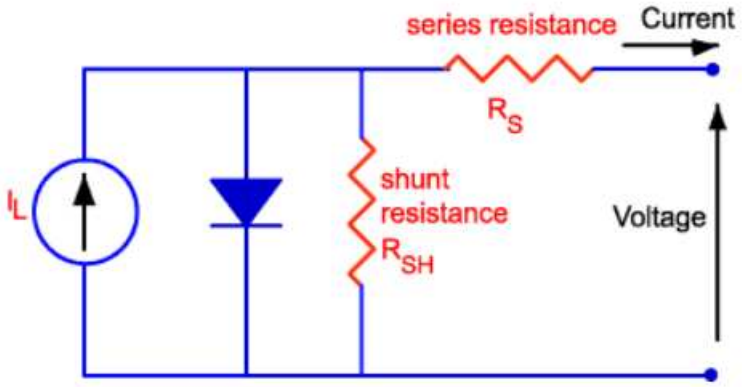


Figure 3.5: Circuit diagram of a PV device. Where I_L is the photocurrent, R_{SH} is the shunt resistance, and R_S is the series resistance. Image taken from [26].

Where I_L is the photocurrent, R_{SH} is the shunt resistance, and R_S is the series resistance. As seen in the diagram, shunt resistance acts parallel to the photocurrent. How resilient a device is to shorting across the diode is represented as shunt resistance. The more resistant to shorting, the higher the shunt resistance and higher the performance. To increase shunt resistance, a thick enough buffer/window layer must be present between the CdTe absorber and TCO. If too thin, pinholes in the thin film may remain after processing. These pinholes act as shunt pathways at the front contact and decrease overall performance of the PV device. Series resistance acts in series to the photocurrent. Series resistance is representative of resistance of charge to flow through the PV device, Common areas of high resistance in heterostructure PV devices are in the interfaces between layers. Therefore, to reduce losses from series resistance interphases withing the PV device must be passivated to decrease the series resistance. At CSU we utilize copper doping to both improve the carrier concentration of our CdTe absorbers as well as decrease the

Shockey barrier at the back of the device. This improves fill factor through decreasing the series resistance of the back contact, or creating an "ohmic" back contact.

Due to the comprehensive nature of the fill factor, it is difficult to assign direct processing conditions that contribute most to its improvement. Therefore, optimization will first be focused on rising V_{OC} and J_{SC} of the PV devices. This should also improve the fill factor passively. If optimal V_{OC} and J_{SC} conditions are achieved but fill factors remain low, attention should be directed towards process conditions such as the window layers and their thicknesses, CdCl2 activation treatments, and back contact passivation through copper treatments.

3.2.4 External Quantum Efficiency

External Quantum Efficiency (EQE) is the ratio of electrons extracted from a PV device to the photons injected into the PV device. A 100% quantum efficiency would be a PV device that produces one electron per photon. EQE is a powerful tool to analyze how the PV device is interacting with the irradiance spectrum. To perform the measurement, the PV device is first contacted to allow current measurement. A monochromator is then used to illuminate the device with specific wavelengths of light across its absorption spectrum. The current is then measured from the PV device for each given wavelength. The EQE (%) for each wavelength is calculated by the equation below.

$$\mathrm{EQE}(\%) = \frac{\mathrm{I_{photo}}}{\mathrm{e}\Phi} \tag{3.3}$$

Where I_{photo} is the photocurrent generated by the incident radiation, e is the charge of an electron and Φ is the photon flux. Once the EQE is measured for each wavelengths. It is plotted

with EQE response on the y-axis and wavelength on the x-axis. This results in the EQE spectral response.

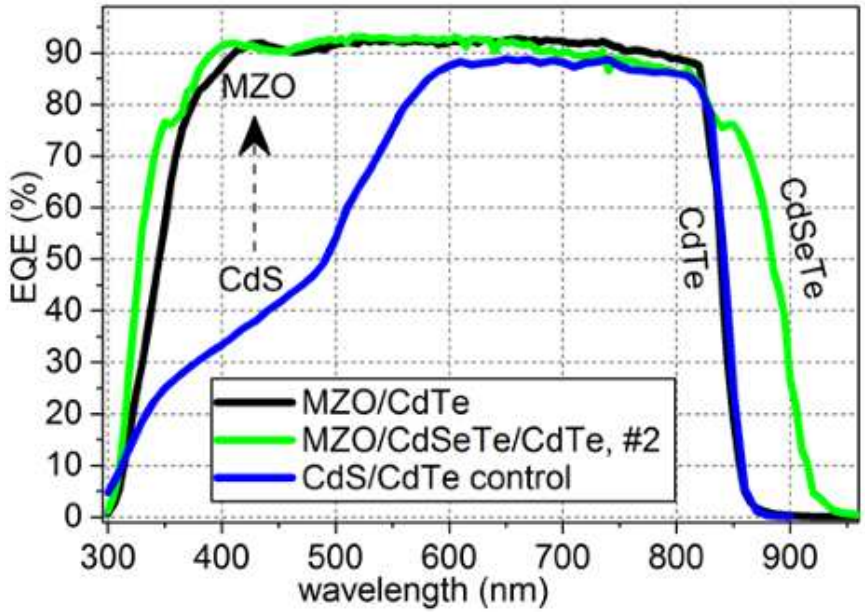


Figure 3.6: EQE response for three differing devices structures, CdS, MZO, and MZO/CST. Figure taken from [18].

The EQE response of three different device structures are plotted in figure 3.6. As seen EQE can identify where in the absorption spectrum a device may gain or lose photocurrent. The CdS device exhibits poor low wavelengths EQE. This is characteristic of parasitic absorption of blue light withing the CdS layer. The MZO/CdTe device also supports this theory. MZO has a large bandgap than CdS and therefore does not parasitically absorb blue light, resulting in an improved EQE response in lower wavelengths. Similarly, the MZO/CST/CdTe has an EQE response that extends into longer wavelengths than devices without CdTe. CST has a smaller bandgap than CdTe at 1.4 eV. This allows for the CST device to absorb farther into the near IR region. EQE can also be paired with transmission and reflection spectra to characterize the amount of power lost due to parasitic absorption in the window layer of the device and reflection

losses, Bittiou et al. utilized this method to quantify the glass/TCO effect on CdTe device performance.

3.3 System Trends

During device fabrication, parameters are set to yield the most uniform films possible while maintaining good process parameters for PV device performance. The more uniform a device is, the more accurately process conditions can be quantified to device performance. While this is the goal, 100% uniformity is not possible withing these fabrication system due to the nature of sublimation processing and the system design.

3.3.1 Thermal Gradients

Sublimation is a thermal process. Heat is used to sublimate source material. This source material travels upwards and deposits onto a substrate that is heated from the top. Excess heat is re-irradiated from the substrate or conducted into the substrate holder. The substrate holder utilized within the ARDS can be seen below.

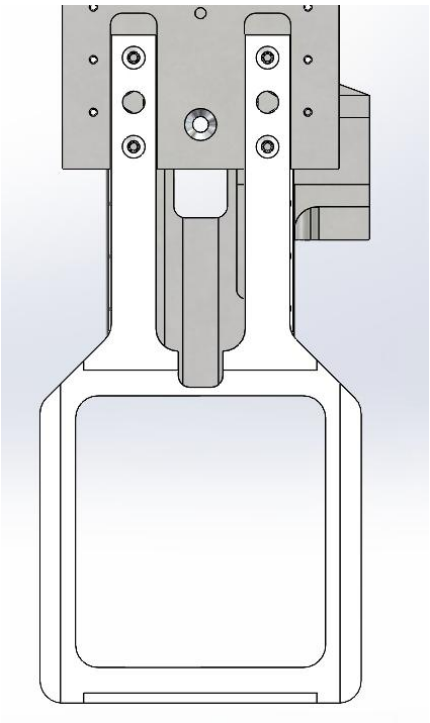


Figure 3.7: A CAD model of the end effector used withing the ARDS.

The ARDS utilizes a transfer mechanism and end-effector to manipulate the substrate withing the vacuum chamber. Heat is transferred to this end-effector through conduction from the substrate, as well as any contact the holder makes with the heaters within the chamber. Early on during deposition, the end end-effector remains relatively cool, and heat is transferred evenly out of the substrate. This results in a substrate with very little temperature change. During longer deposition time, the end-effector begins to become excessively hot. This results in uneven heat transfer out of the substrate, causing temperature gradients to develop. Deposition rates are dependent upon substrate temperature; therefore, film thickness gradients appear on the substrates. Similarly, during long $CdCl_2$ processing some parts of the substrate may become hotter and thus those areas get a more aggressing $CdCl_2$ treatment.

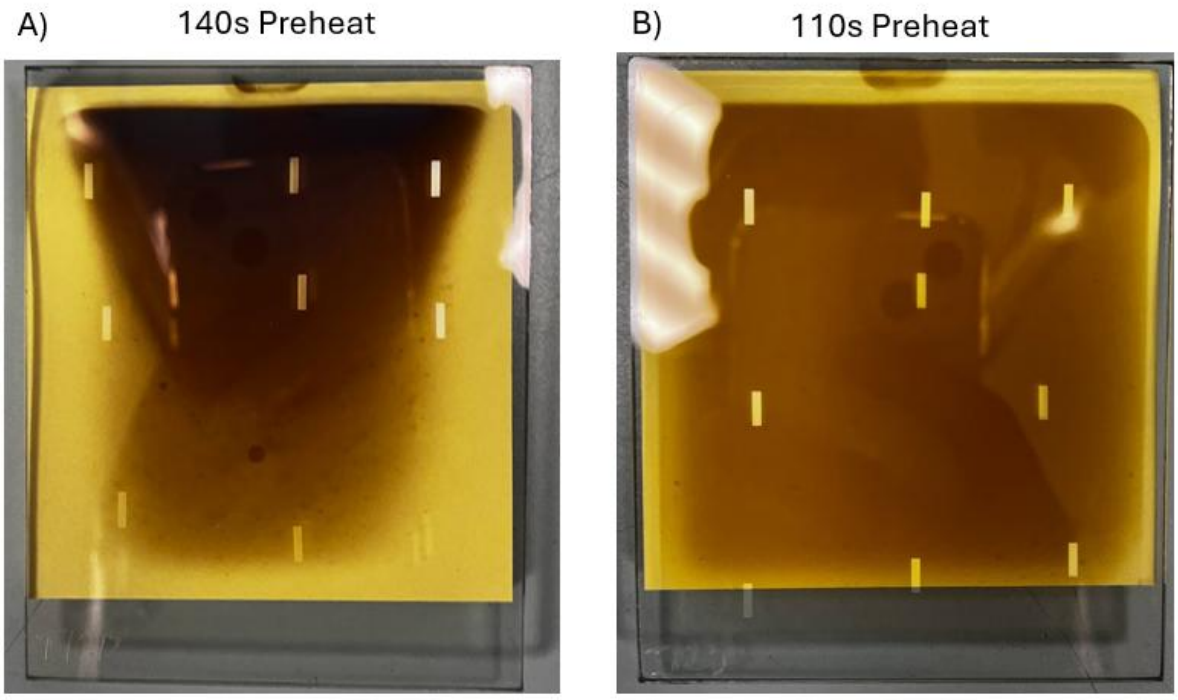


Figure 3.8: Image (A) is a CdSe film deposited with a 140s preheat while image (B) was deposited with a 110s preheat. CdSe deposition conditions remained constant.

Figure 3.8 depicts two different CdSe films. The films were deposited in identical pressures and temperatures within the ARDS. The film on the left was preheated for 140s, in the preheat station. The preheat station withing the ARDS has top and bottom heaters kept at 620°C. The film on the right was preheated for 110s before deposition. As seen, the substrate with a longer preheat resulted in a U-shaped deposition caused by the U-shaped thermal contours on the substrate. Although the lower preheat time resulted in a more even film, this trend continues in the deposition of subsequent films due to excess heating of the substrate. This can also be seen in different film layer dependent upon time of deposition. To better illustrate this idea, thickness measurements were taken across the films at different points withing film fabrication to assess how the films thickness gradients occur during fabrication.

To characterize films uniformity, CdSe is deposited first, and then CdTe. Nine thickness measurements were taken across the substrates to quantify film uniformity across the plate. Heatmaps of the results can be seen in figure 3.9.

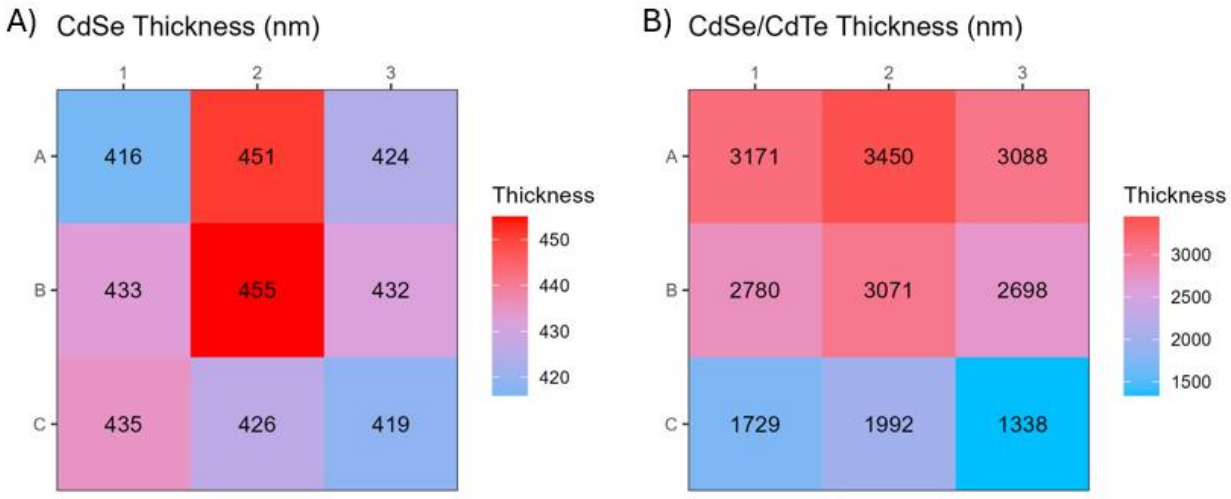


Figure 3.9: Heat maps showing the total thickness measurements across a CdSe film (a) and CdSe/CdTe film (b) deposited on TEC12D. Note, the thickness of the TCO layer was not subtracted from the total thickness measurement.

As seen, the CdSe film exhibits great uniformity. CdSe has a variance of ~30nm of change across the measured areas of the plate. The CdSe/CdTe plate shows drastic change in variation at about 1.5micron difference from top to bottom. CdTe is deposited last, therefore the end-effector has had sufficient time to heat up, resulting in temperature contour forming on the substrate during CdTe deposition. This is translated to performance gradients across the devices, figure 3.10.

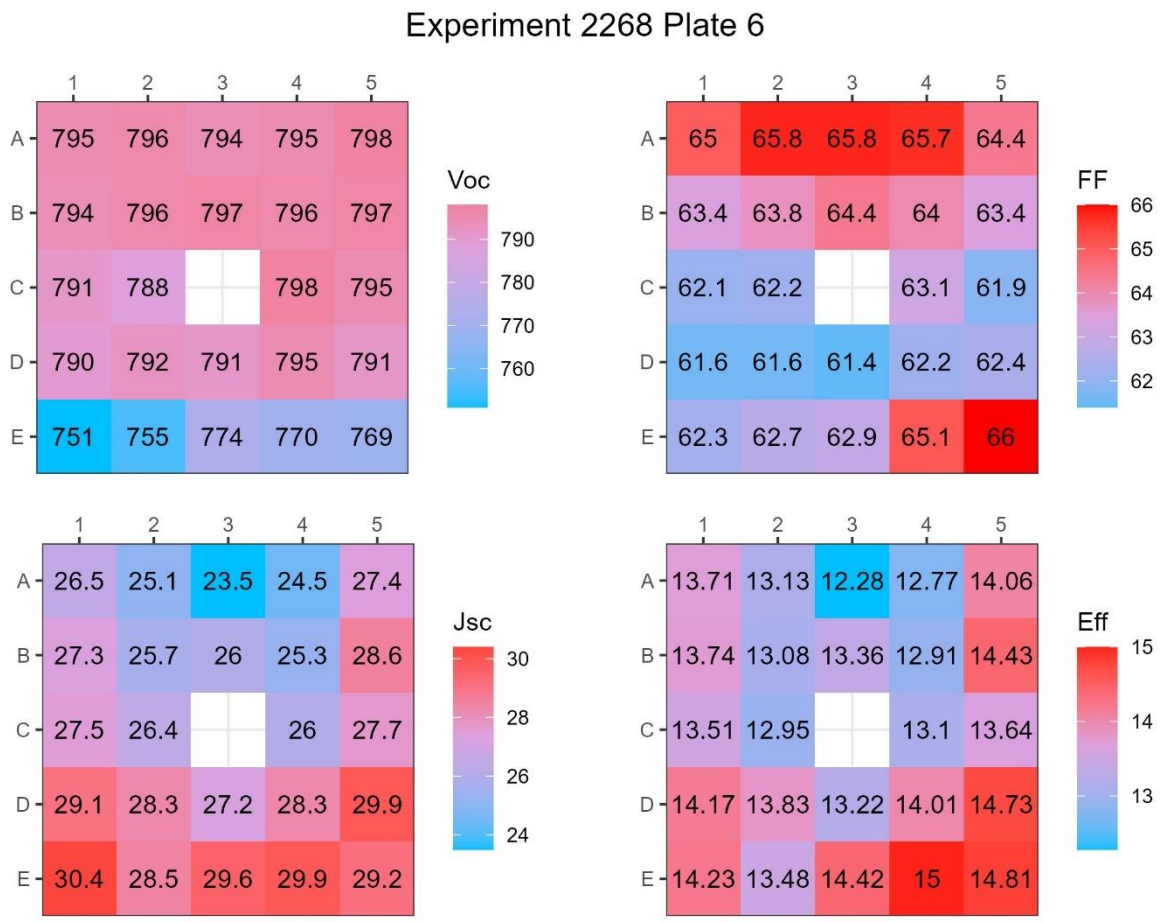


Figure 3.10: Heat map of JV performance of a CdSe/CST/CdTe device.

Similarly, the copper process also introduced a gradient, although the substrate holder causes a gradient left to right across the substrate, versus the ARDS which causes an gradient roughly vertical gradient. Evidence for this gradient can be seen in the trends into two experiments where the substrates are placed opposite directions within the copper tool. This results in the opposing side having optimal performance. Figure 3.11 shows a rough approximation of the orientation of the thermal contours caused by each substrate holder.

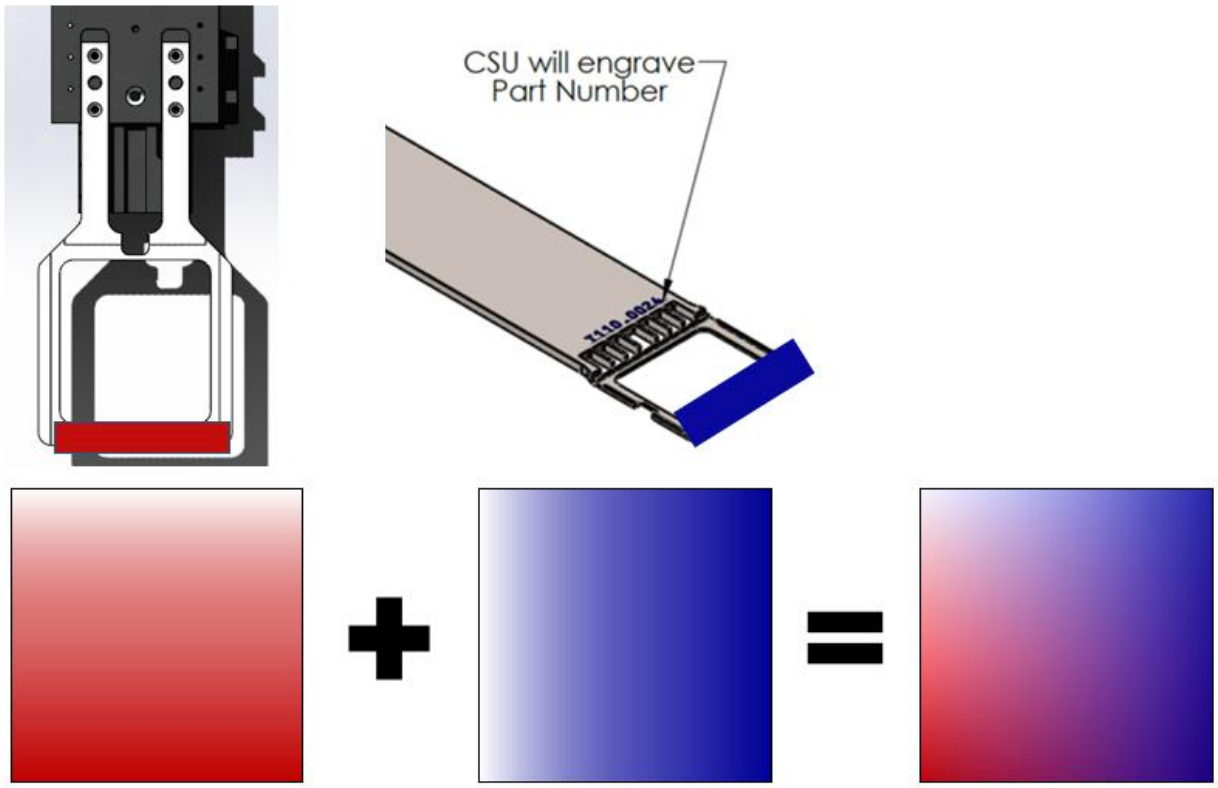


Figure 3.11: Diagram depicting the ARDS substrate holder (left) and the copper tool substrate holder (right) and the general trends of the thermal gradients caused by each substrate holder. Gradient in color represents an approximate gradient in temperature, and as shown when overlayed cause for a diagonal pattern. This diagonal pattern was seen in device performance before the implementation of corrective processing conditions.

Thickness of each substrate is measured at the center. This is the value used to calibrate the thicknesses of each layer deposited. It is important to note these nonuniformities and how they relate to the center thickness as well as how they may affect the $CdCl_2$ processing conditions. If understood, these nonuniformities can give hints to what direction process conditions should go to optimize the fabrication process for device performance.

3.4 Experimental Design

Due to system variability, experimental design was focused on isolating high impact variables through the isolation and manipulation of one variable during experimentation. To compare data across experiments refence devices were made in each experiment to reference

past experiments. While tedious, it enabled the understanding of how different conditions affect each other as well as their impact on overall device performance. This methodology also aids in the avoidance of system effects on the performance of devices. Having isolated control and baseline connecting devices allows for a direct comparison of how changing variables affect device performance as well as a comparison of the overall performance of the experiments versus another.

4 PRELIMINARY RESEARCH

Before investigation of CdSe based device's structure, it was important to develop an understanding of how the glass/TCO stack affects the MZO based devices fabricated at CSU. Understanding these relationships will aid in the development of the CdSe based device as well as serve as a platform for comparison to novel glass/TCO structures.

4.1 Commercial Glass and TCO Stacks

Three different glass and TCO stacks were chosen for the comparison and to serve as the baseline. Two were from Pilkington NSG Transparent Electric Contact (TEC) glass, and the third a proprietary high-performance glass/TCO stack. To clarify, both the glass and the TCO deposited on top are proprietary. Diagrams of each non-proprietary stack are shown in figure 4.1.

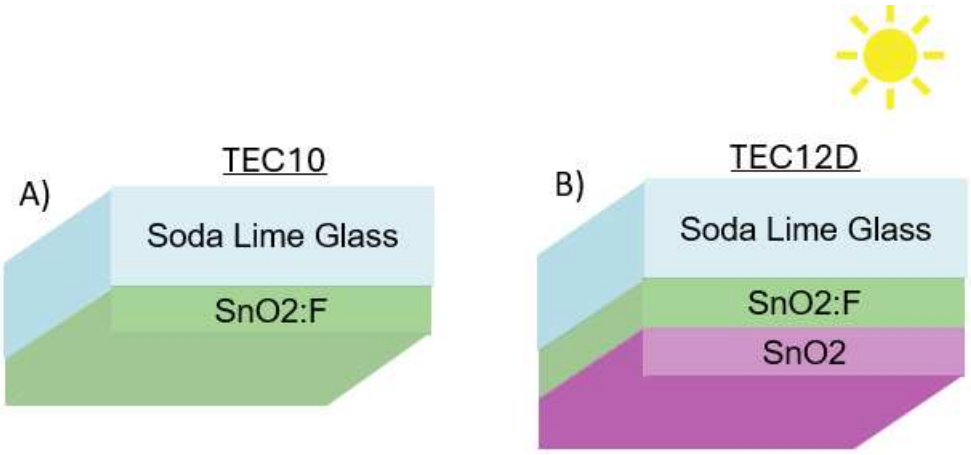


Figure 4.1: Diagram of TEC10 (A) and TEC12D (B) device stacks. The sun signifies what direction light enters the layers. Schematic not to scale.

TEC10 is a basic glass/TCO combination. The glass substrate is a float low-iron soda lime glass. Deposited on top is a fluorine dope tin oxide (FTO) that acts as the TCO of the stack. TEC12D is similar, except the FTO thickness is slightly different as well as there is a third layer thin layer of intrinsic tin oxide on top of the FTO. This intrinsic layer acts as a buffer between the TCO and the absorber material of the devices and allows for greater variability in process conditions for high performance devices.

These glass/TCO were chosen to provide a comprehensive review of different glass and TCO and how they affect device structure. TEC10 was chosen for device fabrication within CSU. Therefor data about how this structure affects device performance was translated to devices fabricated at CSU. The high-performance proprietary glass/TCO, gives reference to whether the performance gains are worth the extra cost of manufacturing these substrates. Finally, TEC12D was chosen because of its use within the CdSe based device structures. It was chosen due to its simplicity of manufacturing. Making a good reference for baseline performance of a simple Glass/TCO stack. It was also chosen because of its extra layer of intrinsic tin oxide that is included which will aid in the development of CdSe based device structures.

4.2 Optical Spectra of Glass and TCO

Glass and TCO lay in between the incident radiation and the absorber of the devices (i.e., they are window layers). Therefor they must be as transparent as possible to the absorption spectrum of the device to maximize the available light to the absorber. To quantify the optical differences between the glass and TCO the lambda 2 UV/Vis spectrometer was used to assess the transmission and reflection of light at different wavelengths across the absorption spectrum.

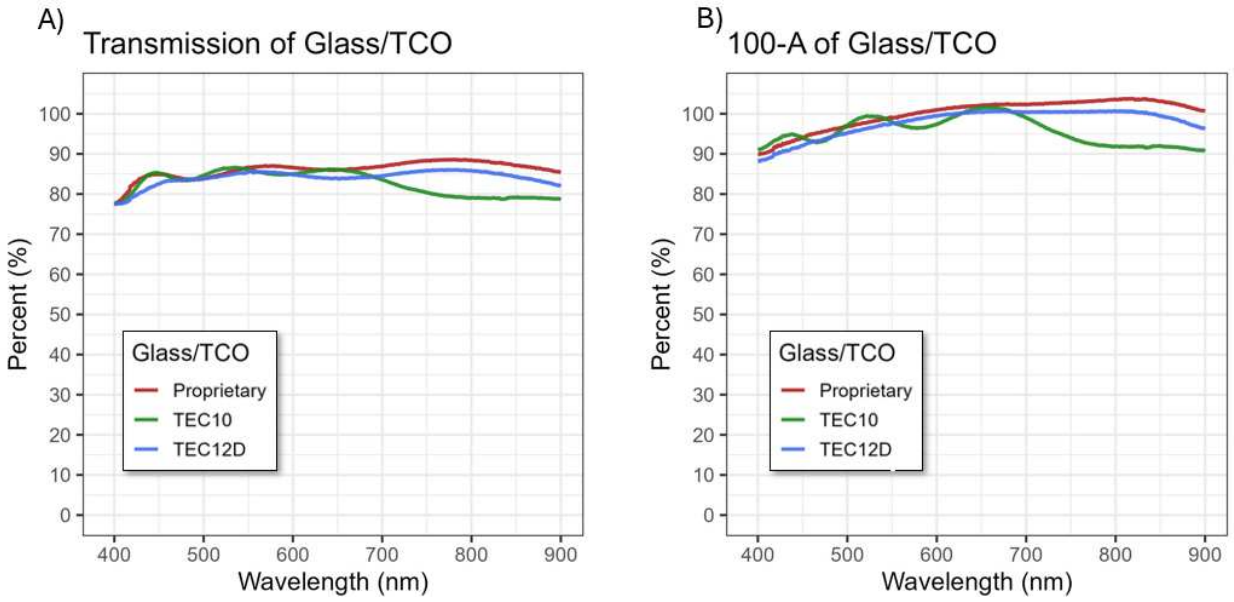


Figure 4.2: Transmission (A) and 100 - A (B) plots of glass/TCO combinations.

As seen, the proprietary glass/TCO has the highest overall transmission of light over 400nm-900nm of with. TEC10 had higher transmission the proprietary glass/TCO at select wavelengths of light but has a dip in transmission above 700nm of light. TEC12D performed similarly to the proprietary glass/TCO except for lower overall performance. These trends are similar in the 100-A plot, the proprietary glass/TCO has the best spectra across 400nm- 900nm with TEC10 yielding the highest transmission at select wavelengths.

4.3 Electronic Properties of Glass and TCO

To assess the electronic properties of the glass and TCO, Hall effect measurements were taken. To ensure comparable results each sample was cut into a $1cm^2$ square, and indium was soldered onto the corners to ensure good contact. The results from the measurements are shown in figure 4.3.

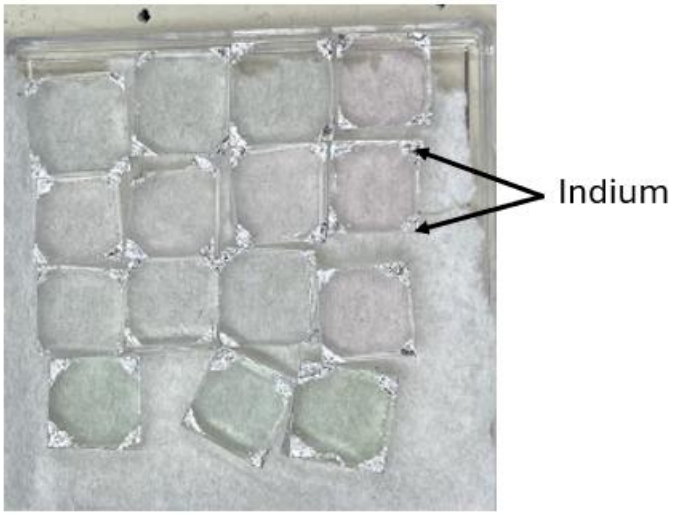


Figure 4.3: Image of prepared samples for Hall effect measurements. Note the indium soldered on the vertices of the squares.

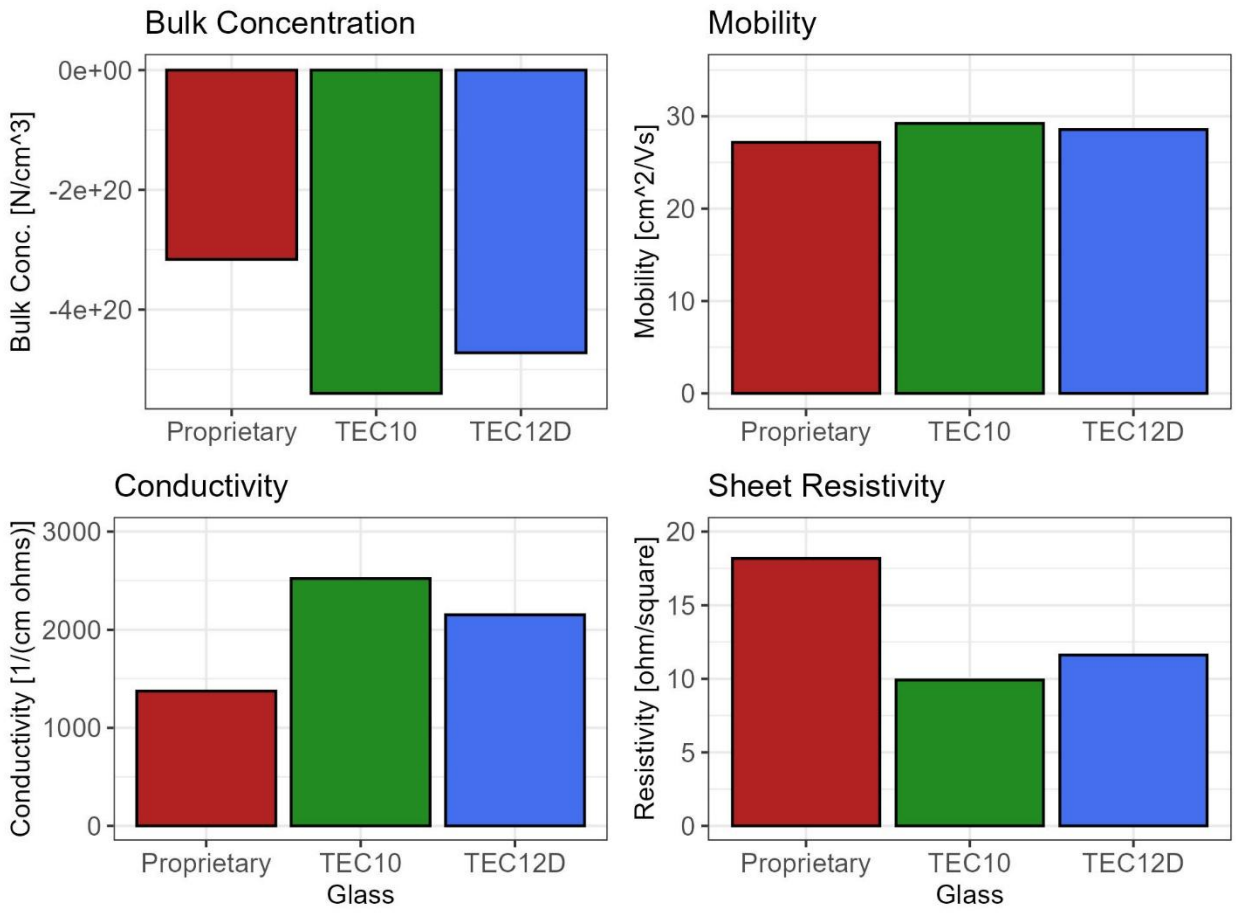


Figure 4.4: Electronic properties of TEC10, TEC12D and the proprietary TCO.

As seen in figure 4.4, the mobility is very similar across all TCO with the number being ~28 cm^2/Vs. Bulk concentration varies from ~$-3*10^{20}$ N/cm^3 with the proprietary TCO to ~$5.3*10^{20}$ N/cm^3 for TEC10. The reason the bulk concentration is negative is due to the donor dopants used to make the TCO N-type and highly conductive. Thus, conductivity follows a similar trend. Due to very similar mobility, the TCO conductivity is tuned via doping concentration (bulk concentration). TEC10 is the most conductive and thus has the highest doping. The 10 in TEC10 stands for 10 ohms/square. The sheet resistivity was measured to assess the quality of electronic measurement. Both the TEC10 and TEC12D measured to have a

sheet resistivity of 10 ohms/square, and 12 ohms/square respectively which suggests a sound hall effect measurement.

4.4 MZO Based Device Optimization

To investigate how glass/TCO affect high performing CdTe devices it was imperative to optimize a MZO based device fabrication process. A series of experiments were performed to improve the overall device efficiency of MZO based devices. Results of these experiments can be seen in the figure below.

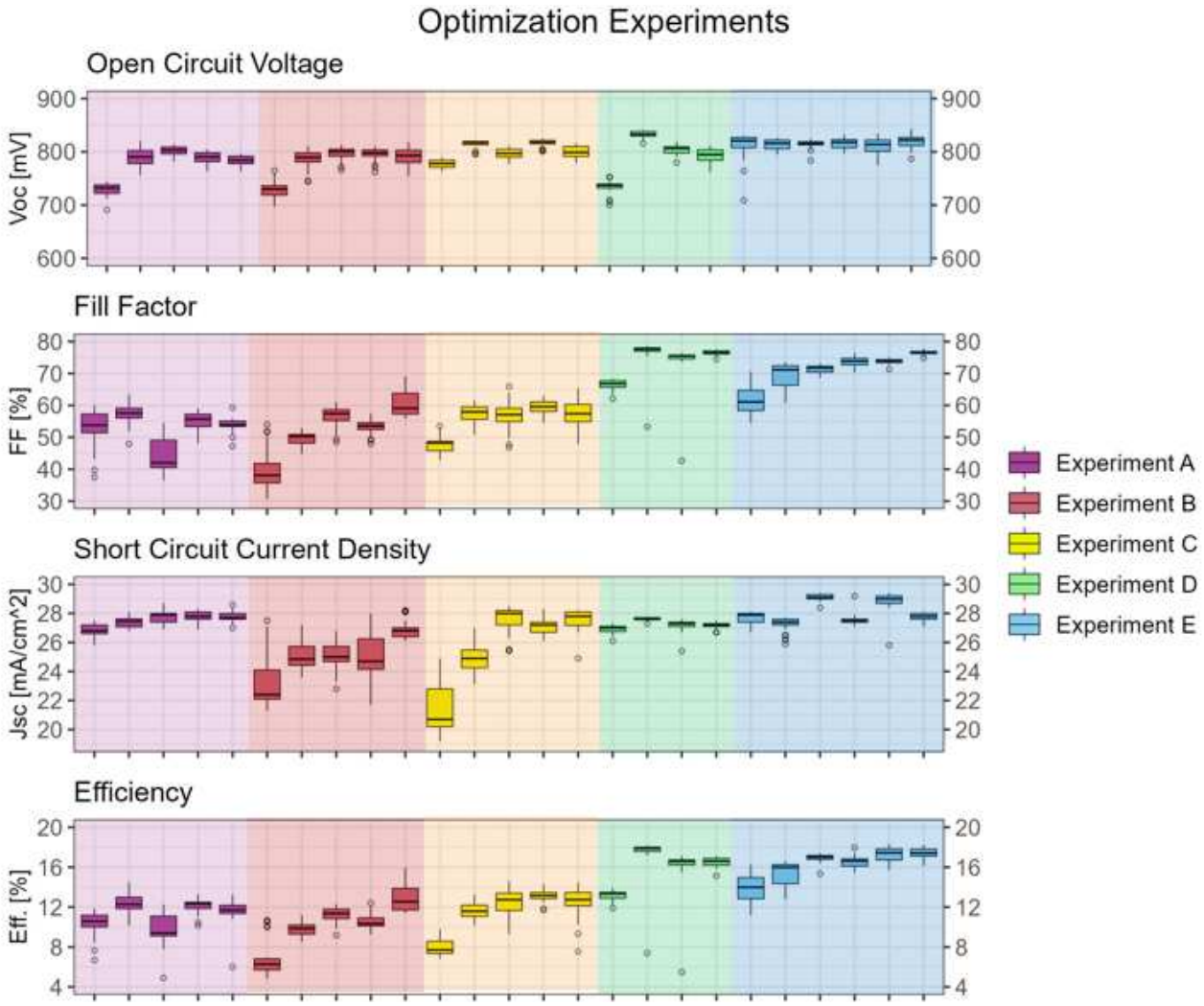


Figure 4.5: JV data from optimization experiments for MZO based devices. Specifics of experimental parameters for experiment A-E can be seen in table 4.1.

Due to limited supply of proprietary glass/TCO, the device structures were optimized on TEC10 and TEC12D. A summary of experimental parameters is shown in table 4.1.

Table 4.1 Experimental changes and results of MZO based optimization experiments

Experiment	Glass/TCO	Key Changes	Results
A	TEC10	TEC10 baseline	Poor FF
B	TEC12D	TEC12D baseline	Poor FF, Lower Jsc than TEC10
C	TEC12D	Cadmium Chloride processing time sweep	Cadmium Chloride process time at these temperatures had a negligible change on performance Plates suffered from poor FF
D	TEC10 & TEC12D	Hotter Substerate temperatures and Mixed gas during CdCl2	Durastice Improvement in FF
E	All Three	Optmized comparison experiment	TEC10 and TEC12D yeild similar performance, higher Jsc from the proprietary substrates

Experiments A and B were focused on baselining the fabrication process for both TEC10 and TEC12D. Similar deposition temperatures and $CdCl_2$ treatments were used for each. Performance for each experiment was poor due to the fill factor. To improve fill factor through better passivation, experiment 2234 was performed. The $CdCl_2$ process time was swept from 300s to 700s in increments of 100s. Manipulation of this variable showed no appreciable change on device performance. Review of legacy data suggested the performance could be improved though raising the substrate temperature and time the $CdCl_2$ activation treatment is performed. It was also found that performing the treatment is a 2%O_2 in nitrogen gas environment may aid in the effectiveness of the treatment. Published literature on the inclusion of oxygen during $CdCl_2$ treatment can be found here [27]. These changes were implemented in experiment D. Experiment D included both TEC10 and TEC12D. Both glass/TCO combinations were chosen for this experiment to ensure that the device structure was not becoming too tailored to one combination over the other. These key changes have caused for a drastic improvement in fill factor, boosting it from ~55% to around ~80%. This improvement caused a climb in efficiency from ~12% to

~17%. With such good performance, the device structure and fabrication process were chosen for comparison of the glass/TCO combinations.

To start, 100nm of MZO was deposited onto each substrate via the RF sputtering process utilizing an 11% MgO with 89% ZnO target in a 5mTorr at 1% oxygen in argon environment. Following MZO deposition, absorbers and $CdCl_2$ treatments were performed within the ARDS. Before the absorber deposition each substrate is preheated in a source with 620°C top and bottom temperatures. TEC10 and TEC12D are similar enough to utilize the same preheat time. TEC series substrates were preheated for 140s while the proprietary substrate (is thinner) was preheated for 110s. Different preheat times were utilized between differing substrates to ensure comparable absorber deposition temperatures. Substrate and source temperatures were 430°C /585°C for CST deposition and 500°C /565°C for CdTe deposition. Deposition rates for CST and CdTe deposition on the TEC series glass/TCO were 2.2nm/s and 27nm/s, respectively. The rates for the proprietary glass/TCO were slightly slower at 1.6nm/s and 24nm/s. This resulted in a 500nm layer of CST and 3.5micron layer of CdTe on each substrate. Without breaking vacuum, each substrate underwent identical vapor $CdCl_2$ activation treatments. Substrate and source temperatures for the $CdCl_2$ process remained at 390°C /450°C respectively and were treated for 900s each. All processes carried out within the ARDS were done in 40mTorr 2%O_2 in nitrogen environment. After sufficient cooling, the substrates were rinsed with deionized water. The standard copper doping and tellurium evaporation were done in accordance to CSU baseline processing. The standard back contact and delineation process was also utilized to finish the devices. Results to the comparative experiment can be seen below.

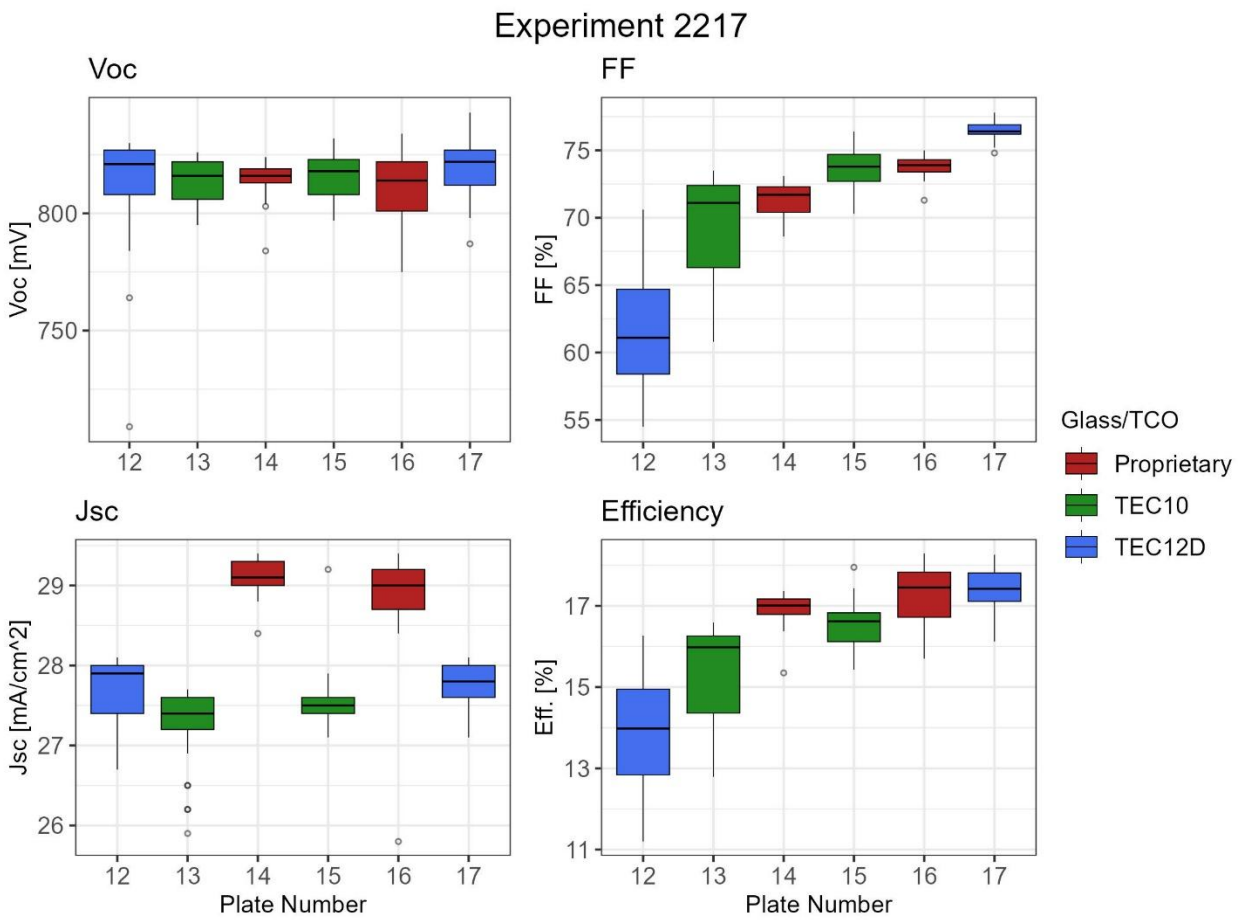


Figure 4.6: JV Results from glass/TCO comparison experiment.

A seen in figure 4.6, The V_{OC} across the experiment remained high with a median around 830mV for each plate, regardless of the glass/TCO used. This suggests the fabrication process produced comparable high-quality absorbers across the substrates. Devices fabricated on the TEC series glass/TCO combinations had high J_{SC} with a mean around ~27.5mA/cm^2. Devices on TEC12D had a slightly larger median than the devices on TEC10. The devices fabricated on the proprietary glass/TCO had much higher J_{SC} with both substrates having a median of 29mA/cm^2 or higher. This resulted in a ~1mA/cm^2 higher J_{SC} than the devices on the TEC series. This is due to the higher transmission of light through proprietary glass and TCO. This higher transmission allows for a greater percentage of light available for current generation in the device and allows

for the proprietary glass/TCO devices to produce more current. The fill factor climbed throughout the experiment regardless of the glass/TCO used. This resulted in the TEC12D glass/TCO performing the best and the worst as it was the first substrate and last substrate of the experiment. This ramping in performance has been seen in most experiments performed with the ARDS. When looking at figure 4.5, it can be seen in every experiment with the first substrate being the worst performing. When looking at experiment 2217, the high V_{OC} and ramping fill factor suggests this is an extraction issue far away from the P-N junction. The JV plots, figure 4.7, also suggest an extraction issue with the 12^{th} plate devices exhibiting a roll over kink, and in devices fabricated later in the experiment exhibit lower series resistance.

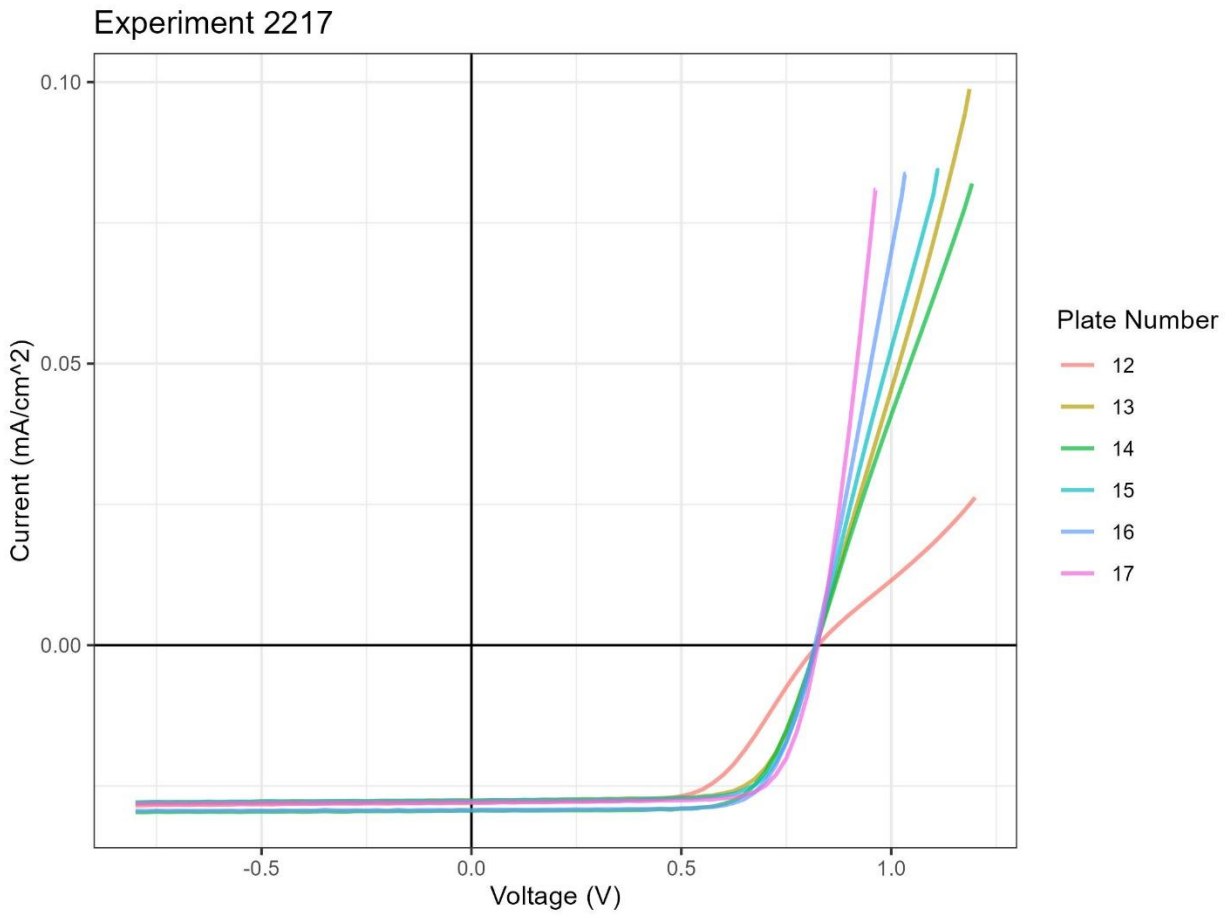


Figure 4.7: JV curves of the B3 devices across all plates in experiment 2217.

The kink occurs independent of glass/TCO, and all devices have high V_{OC}, this suggests an issue at the back contact. The Cu doping process was identified as the reason behind this ramping effect seen in each experiment. Due to the sublimation process used, the system and end-effector must be thoroughly warmed up to produce optimal processing conditions. The system had not been warmed up properly until after a few substrates had been treated. This resulted in suboptimal copper doping of the first few plates and such poor back contact which resulted in high series resistance from the Shockey barrier at the back of the devices.

As seen in figure 4.5, this trend occurred in every experiment, with the first substrate performing worse the rest. To avoid this inconsistency in the future, steps were taken to ensure all systems had been properly heated up before treatment to ensure repeatability across experiments.

Thus, the efficiencies of this experiment were largely affected by the Cu doping and not the glass/TCO used. If FF was not a main driver for efficiency the devices made on the proprietary glass/TCO would be the best performing due to increased current generation from high transmission. To further explore this advantage EQE data was taken of median performing devices of each substrate. Each device was chosen from the center of the plate to avoid any performance variation that may occur across the substrate.

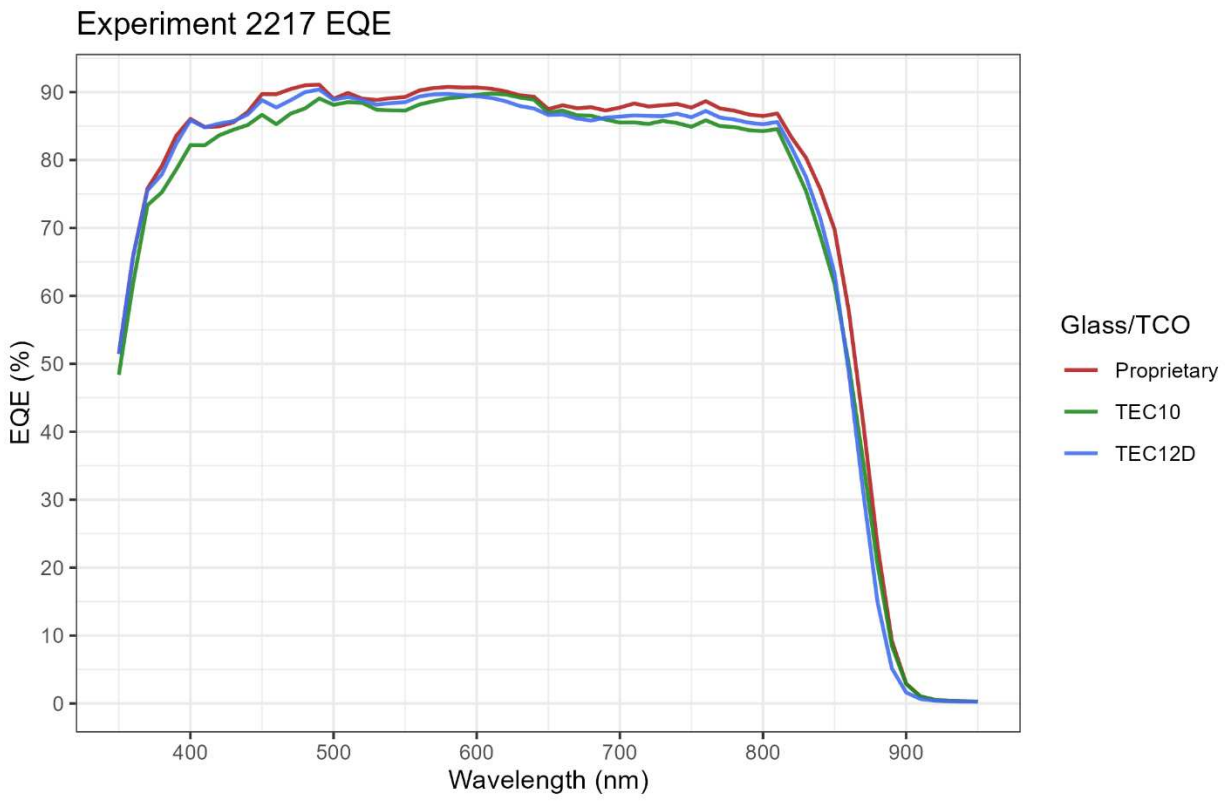


Figure 4.8: EQE spectra of highest performing substrates o each glass/TCO combination.

As seen in the EQE plot, the device on the proprietary glass/TCO has the best overall EQE curve with it being the consistently highest EQE across the measured spectrum. The device made on the proprietary glass/TCO exhibits a better red response than the device made on TEC12D. Although, EQE responses of the devices made on the proprietary glass/TCO and TEC12D did perform quite similarly. This may be due to a higher flux of long wavelength light through the proprietary glass/TCO. To investigate the impact of the optical properties of the glass/TCO plots the EQE plots overlayed onto an optical plot.

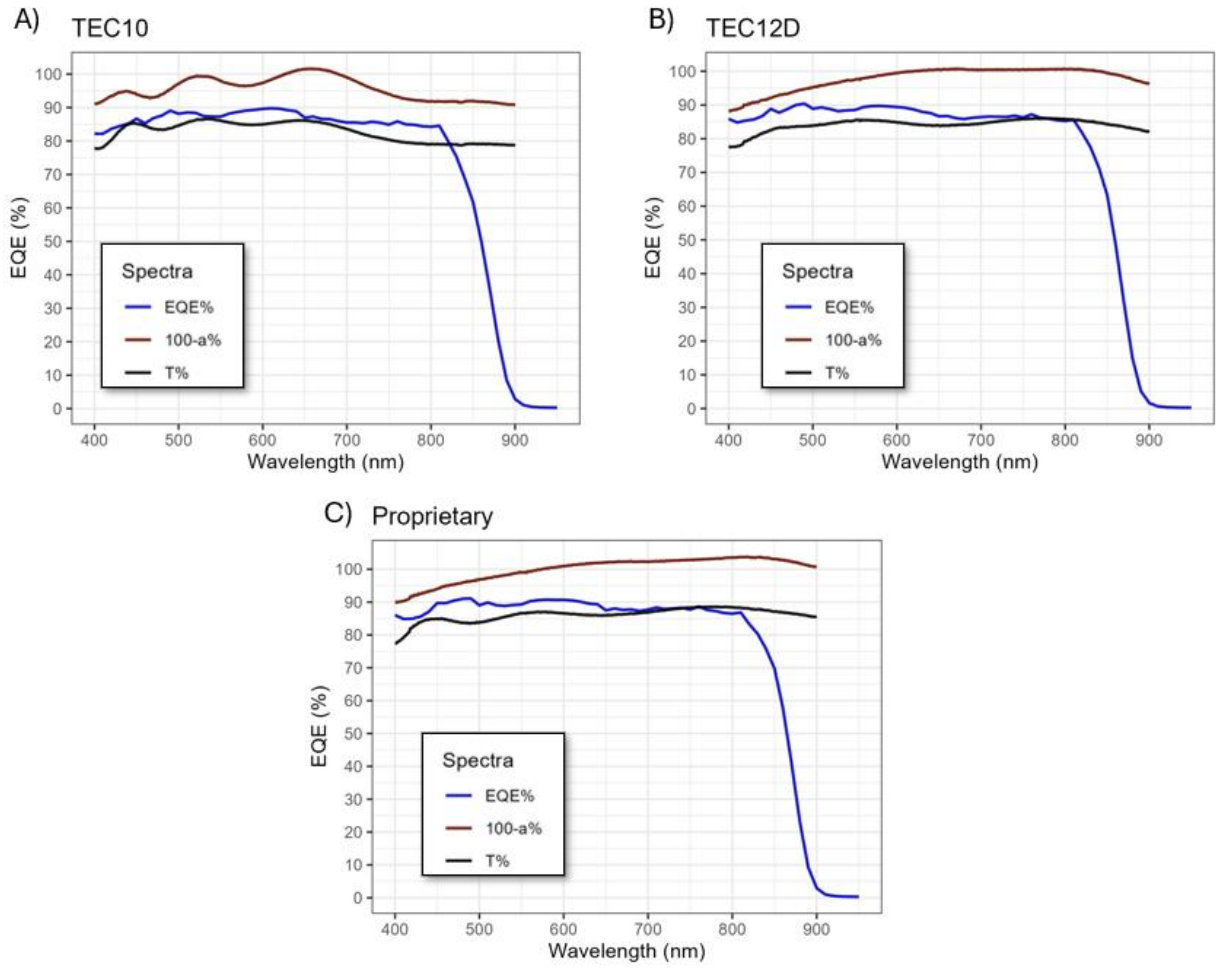


Figure 4.9: EQE spectra overlaid onto transmission and 100 - absorption spectra. A) is TEC10, B) is TEC12D, and C) is proprietary glass and TCO

For most of the measured spectrum the EQE response outperformed the transmission for each glass/TCO, indicating that the addition of MZO and the subsequent layers is reducing interfacial reflectance. Although more light is entering the devices than the transmission plots suggest, it is probable that the light is still proportional to the values seen, thus the reason the red response of the device made on the proprietary glass/TCO is due to a higher flux of photons in the red region as seen by a higher transmission at those wavelengths. To better characterize how the glass/TCO affect the performance of the device, the EQE spectra was compared to the 100-A% spectra to quantify how the glass/TCO affect performance as well as the possible future of

performance. This analysis was done by Bittou et. al. and utilizes equations 2.2 and 2.3 to calculate the maximum potential J_{SC}, which assumes the only losses in EQE are from absorption loss withing the glass/TCO stack, and the actual J_{SC} which is calculated using the measured EQE spectra. Dividing the actual J_{SC} yielded by equation 2.3 by the max J_{SC} yielded from equation 2.2 give the percent of potentially available photons converted by each device [12]. The analysis was performed from 400nm to 900nm due to the limitations of the UV Vis spectrometer used to take the transmission and reflection data. The TEC series glass/TCO bother performed well at 83% conversion of potentially available photons. Although, the device on TEC12D performed better with a higher actual and theoretical J_{SC}. The device on the proprietary glass/TCO had the worse collection efficiency of ~81% although an equivalent current to TEC12D. Its drop in efficiency is due to the increase in the potential current around 32.4mA/cm^2 from 31.4 4mA/cm^2 shown from TEC12D. Thus, the proprietary glass/TCO has the highest potential if the current efficiency is improved.

5 BASLINE OPTIMIZATION

5.1 Introduction

To make results of this study more applicable for commercial use, a new devices structure was chosen to be optimized for the comparison of different glass/TCO. The key difference is the use of CdSe at the front of the devices. Please note that this is an investigation of an alternative structure that does not use the MZO buffer layer. This does not imply that CdSe is a replacement to MZO or that they are mutually exclusive. The structure utilizes TEC12D, because of the commercial viability and the inclusion of the intrinsic tin oxide layer on top of the FTO, this layer aids in fabrication by acting as an additional buffer to the absorber and TCO.

Deposited on top of the TEC12D is CdSe, followed by the rest of the absorber material (either CdTe or CST40/CdTe), followed by $CdCl_2$ treatments and copper doping. A thin layer of tellurium followed by standard back contact fabrication and declination was used to complete devices. Diagrams of possible device structures can be seen in figure 5.1.

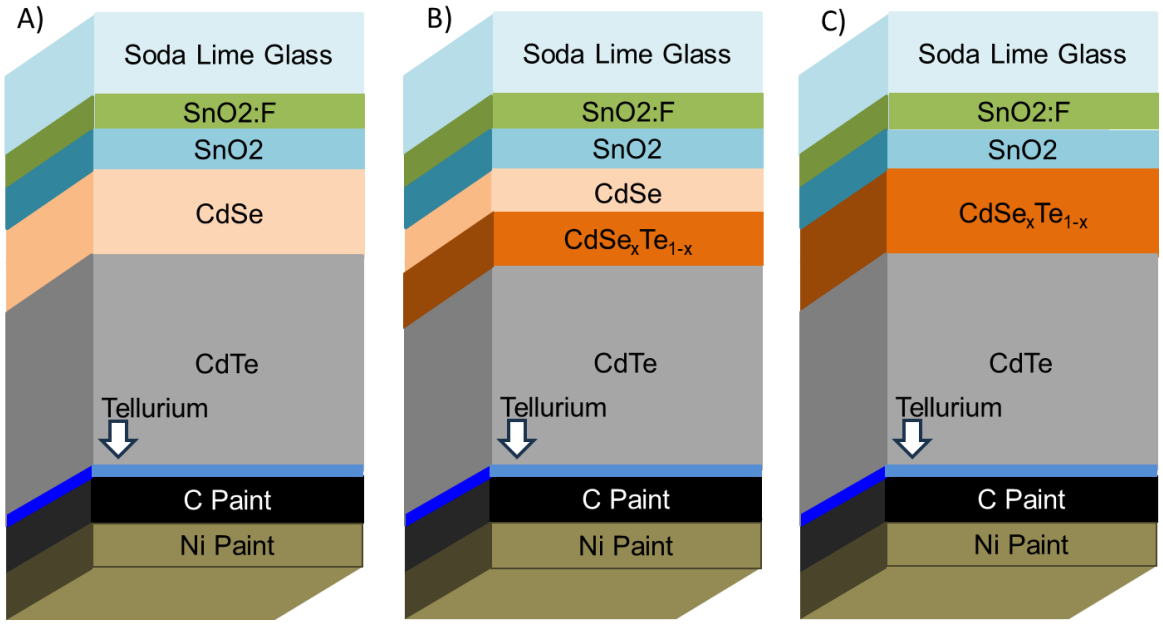


Figure 5.1: Diagram of the device structures, CdSe/CdTe (A), CdSe/CdSexTe1-x (CST)/CdTe (B), and CdSexTe1-x (CST)/CdTe (C)

5.1.1 Key Challenges

CdSe is typically evaporated to form the thin film at the front of the device. This results in a film with very fine grains. Bastola et al has shown performance of up to 16% efficiency utilizing evaporation of the CdSe layer. The deposition rate of this process was reported to be ~15nms^{-1} and the substrate was maintained at 400˚C. While CdSe deposited for these devices will be via sublimation with deposition rates closer to ~1nms^{-1} and a substrate temperatures ranging from 440˚C to 475˚C. To asses' differences in the sublimation deposited CdSe, a Tauc

plot was created to ensure the correct bandgap of CdSe. SEM images will also be taken of the film surface to get an estimate on grain size as well as an overall impression of film morphology.

Most literature discussing CdSe based devices utilized wet/solution based $CdCl_2$ treatment, these vary greatly from the vacuum vapor $CdCl_2$ treatment done at CSU. The wet treatments involve applying a layer of $CdCl_2$ onto the surface of the absorber via a $CdCl_2$ solution before annealing the substrate withing an oven. These treatments typically last ~1 hour. In contrast the $CdCl_2$ performed at CSU is much shorter, (typically around 10 min – 20 min) as well as the substrates are annealed in a constant flux of $CdCl_2$ during the duration of the treatment. While steps can be taken to better mimic the wet treatment (through dosing within the $CdCl_2$ source followed by annealing in another), the processes do differ which would possibly necessitate a need for different structure for high performance.

5.2 CdSe at CSU

To better inform processing conditions for the CdSe base devices. The CdSe films deposited in the ARDS were analyzed to compare the sublimation film deposited by the ARDS to other deposition techniques. An Uv-Vis spectrometer was used to take transmission and reflection data of three different CdSe films. Each films were 120nm thick, and one was as deposited, another was annealed for three minutes at 400°C and the third was $CdCl_2$ treated for three minutes at 400°C substrate and source temperatures. The absorption coefficient was derived from the transmission and reflection data using beers law, equation 3.2.

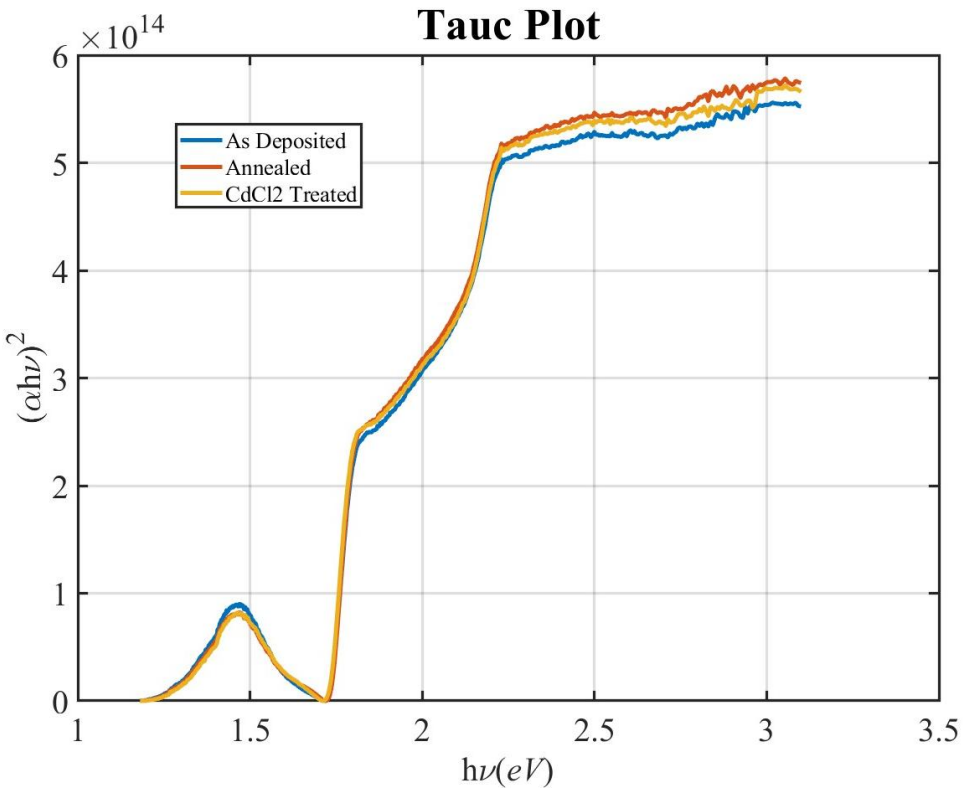


Figure 5.2: Tauc plot of all three CdSe films.

Figure 5.2 shows the Tauc plots of each CdSe film. The post deposition treatments seem to have a negligible effect on the optical spectra. Shown below are the spectra of the as deposited film with the linear region fitted to it.

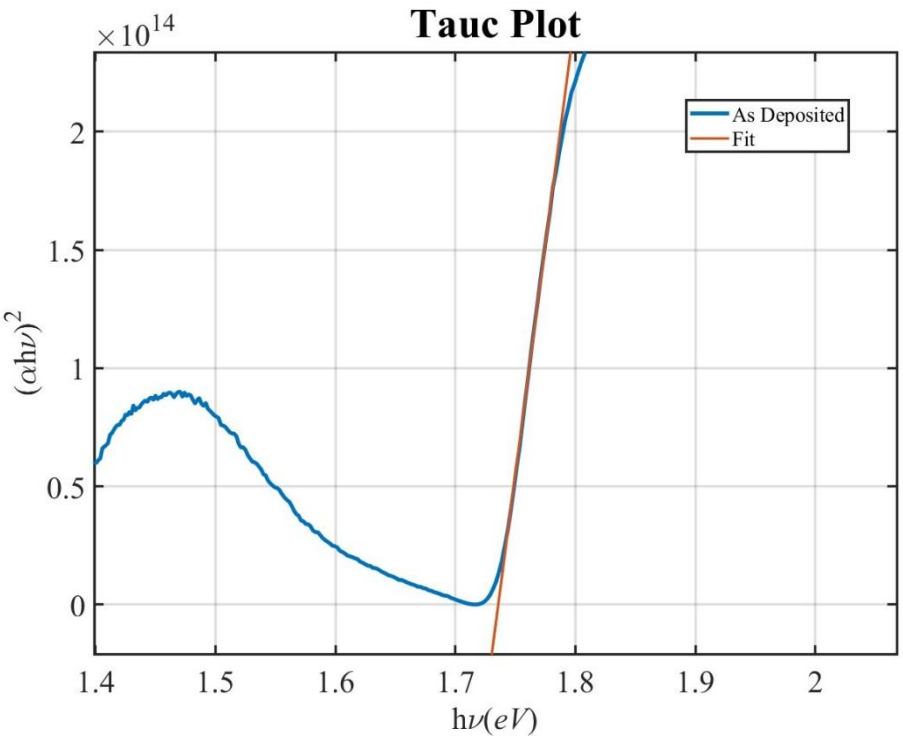


Figure 5.3: Tauc plot of as deposited film and the line fit on the linear region.

Lines were fitted to the linear region of each film. Where the linear fit crosses the x-axis is the estimated bandgap of the material. Each fit yielded a bandgap of ~1.74eV which agrees with the known bandgap of CdSe [28]. Note the increase in absorption at energies lower than the bandgap of CdSe is identified as an unknown optical anomaly. SEM images were taken of each film to characterize the film surface.

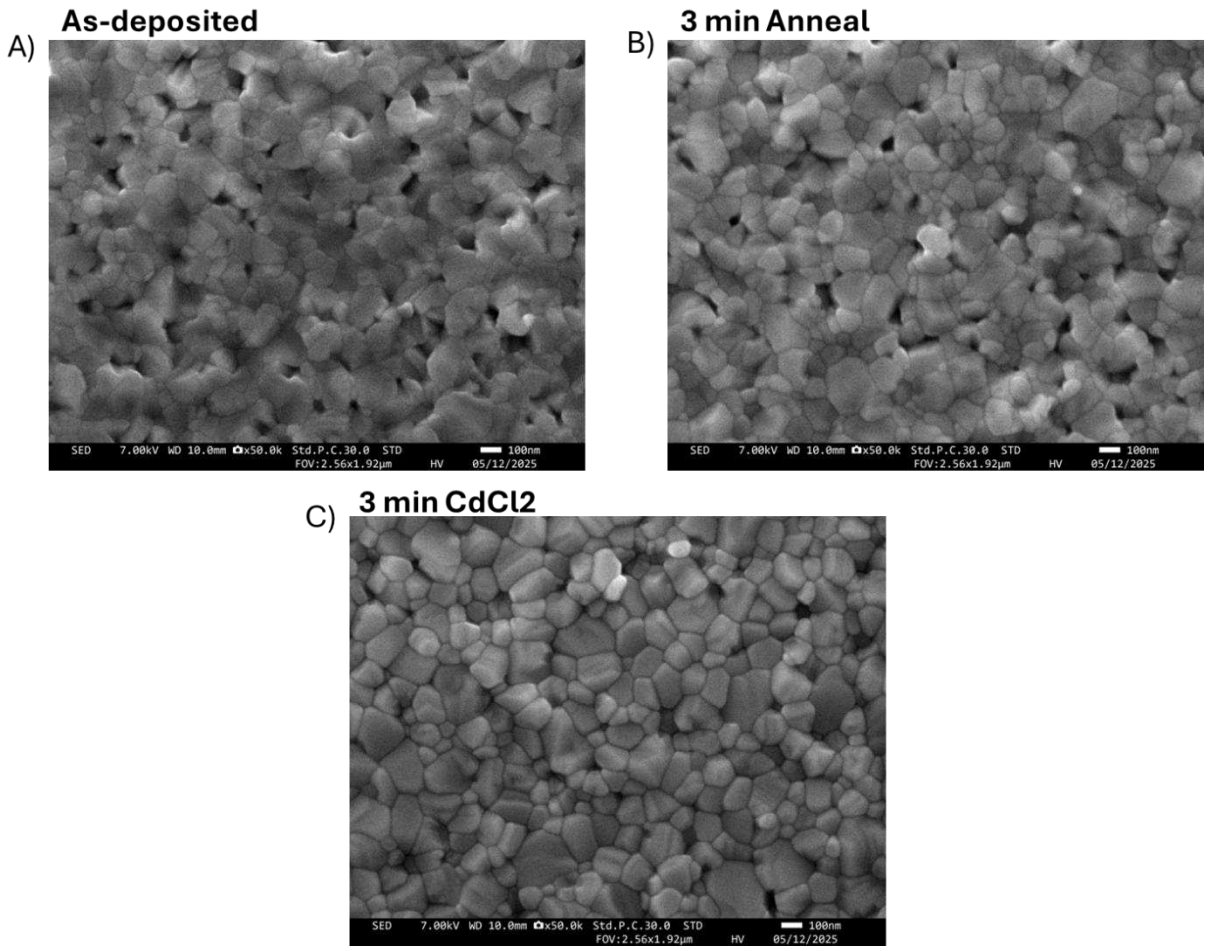


Figure 5.4: SEM images of CdSe films, A) is as-deposited, B) had a 3min anneal, and C) has a 3 min $CdCl_2$ treatment.

The resultant films surface is made up of nodular grains with ferret diameters averaging around ~170nm but ranging from ~100nm to ~300nm. The post deposition treatments such as the 3min anneal as well as 3 min $CdCl_2$ treatments resulted in films that wouldn't charge as quickly and thus were easier to clearly image. Other studies in which the film morphology of CdSe was studied from with cross-sectional EBSD noted a columnar grain growth from an evaporation deposition technique [22]. If similar growth is seen in sublimation deposited CdSe then these grains would be on average wider with a diameter either equal to or larger than the film thickness. While these films did exhibit similar characteristics to the evaporated films, it is

important to note that the deposition rate varied greatly as well as the substrate temperatures during deposition. This may cause changes in film morphology not assessed within this investigation [19], [29], [30].

5.3 A n-type window/buffer layer is necessary to mitigate voltage loss

To investigate the CdSe device structure, experimentation was focused on the function and role CdSe plays on device performance. To directly compare CdSe to MZO based devices, an experiment was designed so that CdSe would replace the MZO layer in typical CSU baseline devices. Thus, the overall structure of the devices was CdSe, followed by CST and CdTe. CdSe varied from 0nm to 125nm. The CST layer thickness varied in the inversely to maintain a total combined thickness of 350 nm between the CdSe and CST. For example, the 50nm CdSe devices had 300nm CST. Process conditions for the experiment remain consistent with baseline with the exception for lower substrate temperatures to aid in uniformity, which were 440°C for both CdSe and CST deposition while CdTe was deposited at 490°C.The $CdCl_2$ treatment was maintained at 900s for all devices.

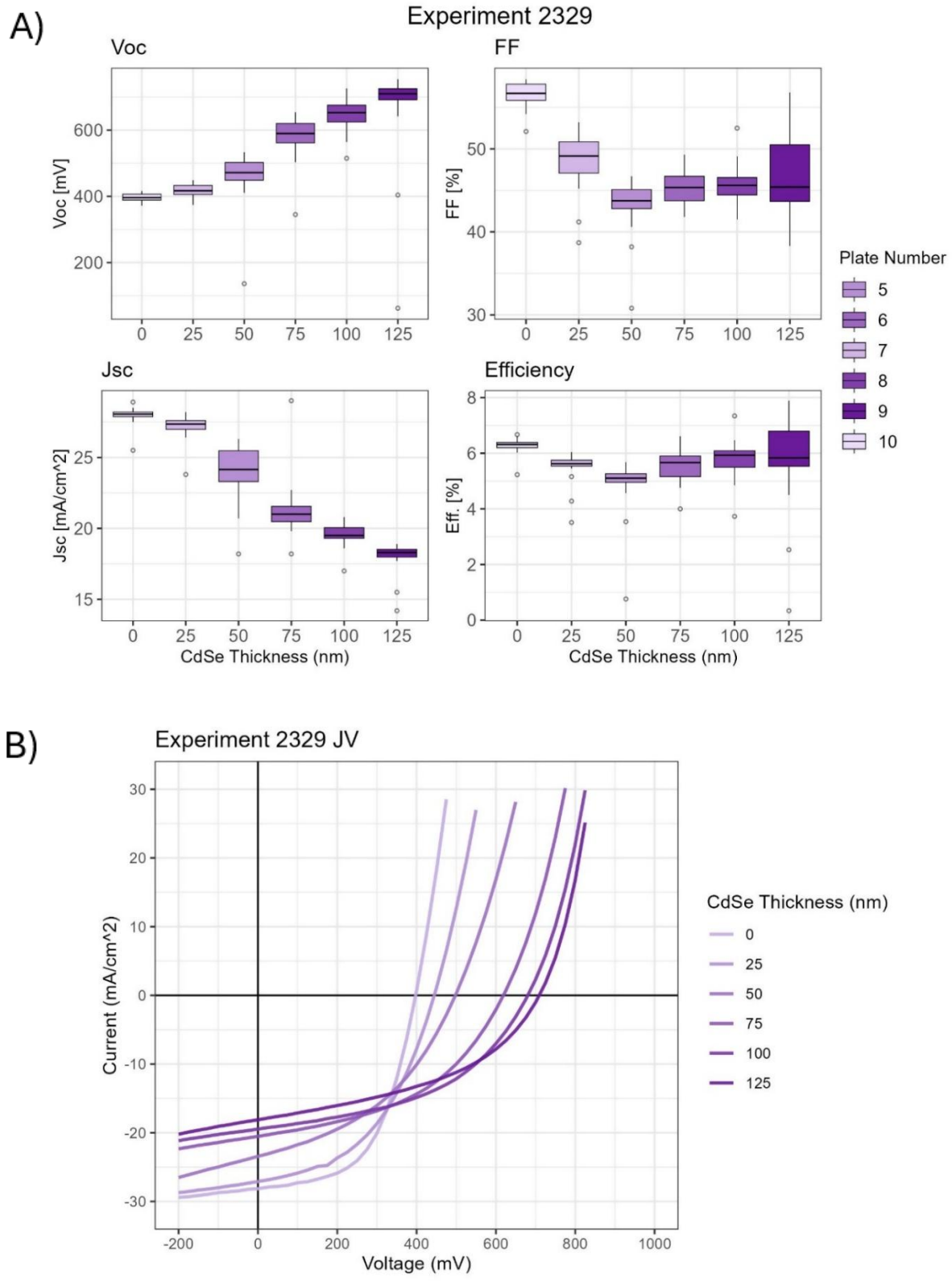


Figure 5.5: Boxplots of JV results (A) and JV curves (B) from experiment 2329 where CdSe and CST thickness varied across 6 different substrates.

Results from experiment 2329 show that CdSe thickness is integral for the V_{OC} of the device. The 0nm of CdSe devices resulted in very poor V_{OC}, although having good fill factor and good J_{SC}. Increasing CdSe thickness with this $CdCl_2$ treatment did have a negative impact on J_{SC} with the thickest CdSe devices at 150nm having a mean J_{SC} of ~18mA/cm^2. Fill factor was highest in the CST only device, although increasing CdSe thickness did result in a substrate with a wider variance of fill factor with some devices with equivalent fill factor as to the 0nm CdSe devices.

5.4 CdSe window layer thickness is directly correlated to V_{OC} and inversely correlated to J_{SC}.

For optimal device performance the CdSe layer must be thick enough to establish a "buffer" between the absorber and TCO as well as thin enough to avoid a large amount of parasitic absorption due to its bandgap of 1.7eV. Because CdSe easily interfuses with CdTe during $CdCl_2$ treatment to form CdSeTe, the final CdSe layer thickness depends on both the initial deposition thickness and the $CdCl_2$ treatment conditions. Experiments were designed to explore the relationship between the thickness of deposited CdSe and the conditions of $CdCl_2$ processing, aiming to determine how these factors contribute to optimal performance.

5.4.1 Deposited CdSe thickness Effect

To investigate the effect CdSe thickness has on device performance. Two experiments were performed. Each utilized processing conditions, which produced high performance-based devices to establish performance comparisons to those devices. CdSe and CdTe films were deposited withing the ARDS [23] via sublimation in nitrogen at ~40mTorr for both experiments. For experiment 2231, substrate and source temperatures were kept at baseline deposition

temperatures, 475°C / 575°C for CdSe deposition and 500°C / 565°C for CdTe deposition. Thickness of CdSe was varied by varying the deposition time from 140s – 360s to get a varying thickness from 100nm to 300nm across 5 experimental substrates. Each substrate had a thickness of ~3.3 microns. All substrates underwent the same $CdCl_2$ treatment to isolate CdSe effect on device performance. The substrate temperature was kept at 387°C and source temperature at 450°C over the course of 360s and then moved to an annealing station with substrate and source temperatures kept at 400°C for another 360s. After $CdCl_2$ the substrate is moved to a separate vacuum chamber where the substrates are Cu doped via standard CSU baseline processing procedures. Following the copper doping process, a 30nm tellurium was thermally evaporated on the back, and the back contact is formed via carbon and nickel paint.

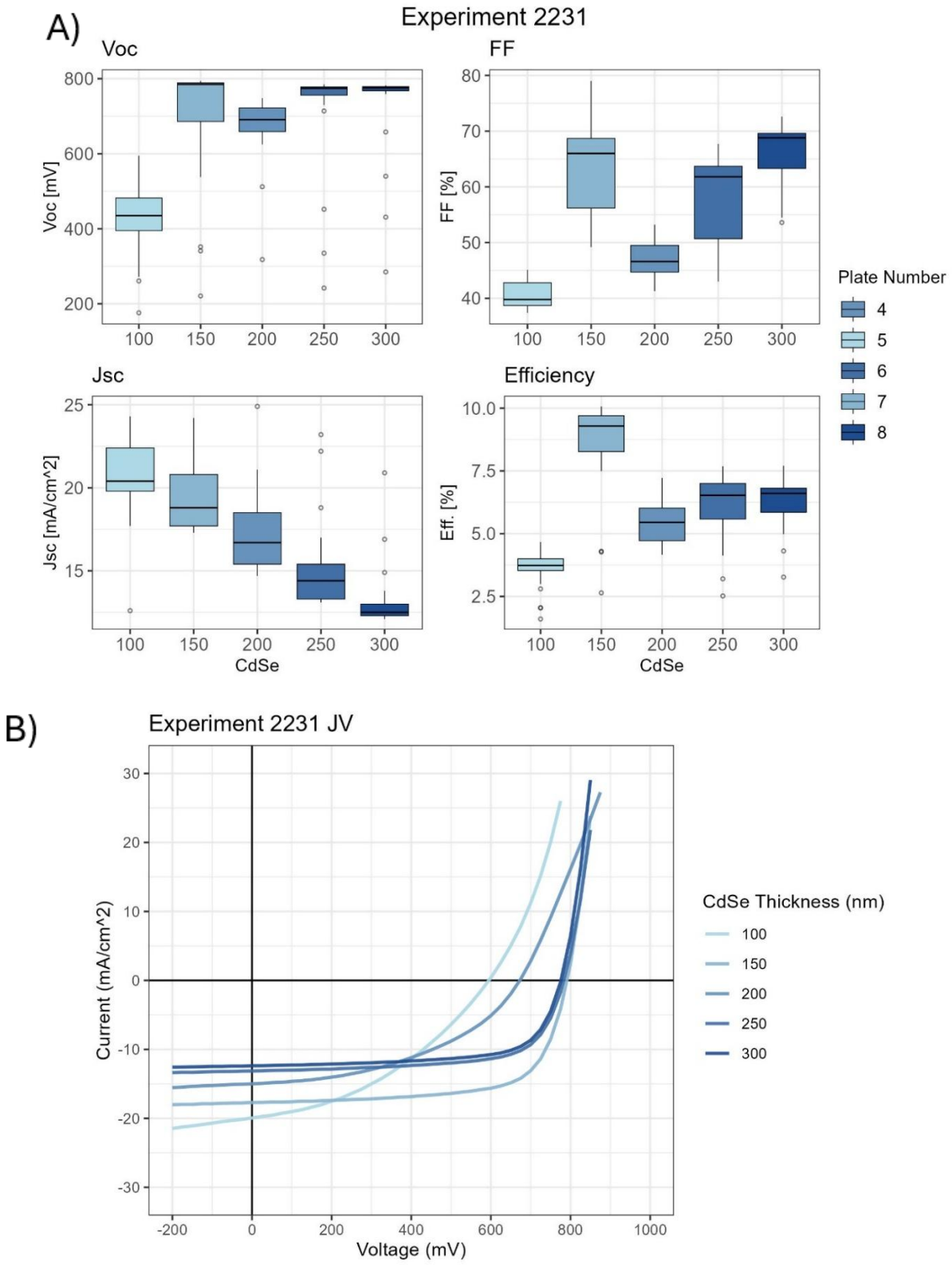


Figure 5.6 Boxplots of JV results (A) and JV curves (B) for experiment 2231. CdSe thickness varied while all other conditions remained constant.

As seen in figure 5.6, a strong correlation exists between V_{OC} and CdSe thickness at this $CdCl_2$ processing time and temperature with V_{OC} increasing from ~440mV at 100nm CdSe to ~780mV at 150nm. Increasing the thickness past 150nm did not result in a performance gain in V_{OC} with performance plateauing around ~780mV. J_{SC} is seen to have a strong inverse correlation to CdSe thickness at these $CdCl_2$ times and temperatures. The mean J_{SC} drops from ~21mA/cm^2 to ~12.5mA/cm^2. Literature supports optimum thickness of CdSe to be ~120nm to ~3.5 microns of CdTe [21], [31]. Devices from literature achieve higher current than the 100nm sample, suggesting this $CdCl_2$ treatment time and/or temperatures are suboptimal. The fill factor had a positive correlation to CdSe thickness although 150nm thick CdSe performed well with a fill factor comparable to 300nm. This may suggest that the fill factor is independent of CdSe thickness within the range tested. When looking at data from order of substrates, the familiar trend of increasing fill factor can be seen, with the first plates performing worse than the last. Plate numbers indicate the order in which these devices were fabricated with 1 being the first and the highest number being the last. 150nm and 300nm CdSe were the last two plates to be fabricated therefore that may be why 150nm has a comparable fill factor to 300nm. This experiment was performed before preheating of systems was implemented therefore this is a likely outcome.

Experiment 2248 utilized the same processes conditions except for the substrate source temp for CdSe was kept at 480°C. CdSe deposition time was swept from 188s – 235s to yield a thickness variation of 100nm across 7 substrates. CdTe thickness was maintained at ~3.5 microns. JV performance of these devices is shown in figure 5.7.

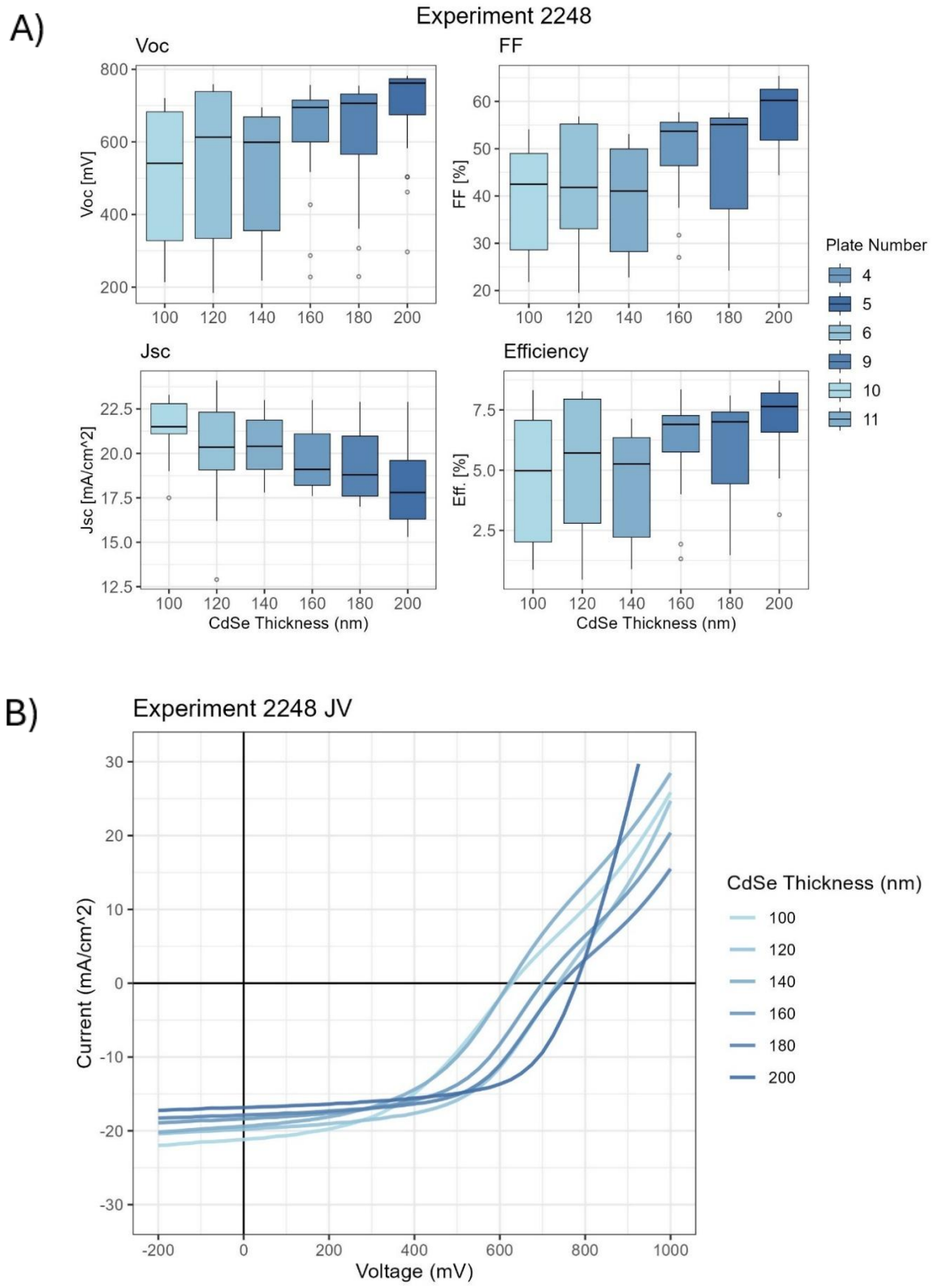


Figure 5.7: Boxplots of JV results (A) and JV curves (B) from experiment 2248. CdSe thickness varied from 100nm to 200nm while maintaining all other process conditions.

Firstly, when comparing the 100nm and 200nm CdSe plates from experiments 2231 and 2248, performance is similar between the experiments expect for the fill factor between the 200nm plates. This again suggests the fill factor is not solely controlled by the CdSe thickness and may be influenced by other process conditions within fabrication. The overall trend from experiment 2248 follows closely to experiment 2231 with a positive correlation between CdSe thickness and V_{OC}, and a negative correlation to J_{SC}. The fill factor had a positive correlation to CdSe thickness above 140nm regardless of fabrication order.

5.4.2 $CdCl_2$ Activation Effects on Device Performance

To investigate the effect of $CdCl_2$ treatment time on device performance experiment 2234, 2360 and 2377 were performed. Experiment 2234 was designed to investigate the effect $CdCl_2$ has on CdSe based devices utilizing the baseline $CdCl_2$ process used at CSU. Experiment 2234 device fabrication followed the baseline fabrication process outlined earlier in this text. $CdCl_2$ treatment varied from 600s to 900s for substrates with 200nm and 250nm of CdSe. The treatment time was split evenly between the $CdCl_2$ source and the annealing source. The $CdCl_2$ source was kept at baseline 397°C substrate temperature and 450°C source temperature, while the heaters in the anneal station were kept at the baseline temperature of 400°C. Fo example for a $CdCl_2$ time of 600s, the substrate was treated in the $CdCl_2$ source for 300s and annealed for 300s. CdTe thickness was ~3.5 microns.

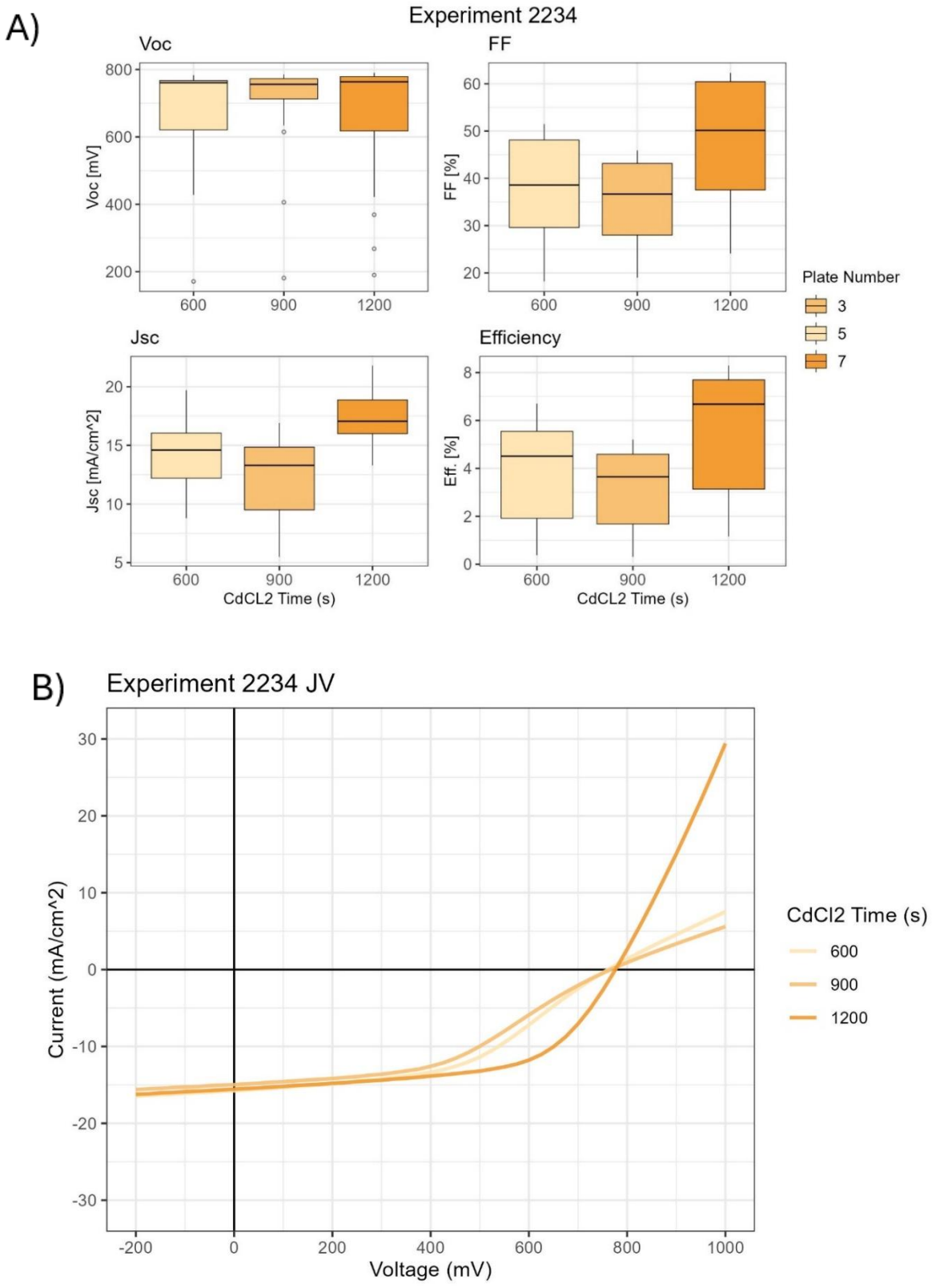


Figure 5.8: Boxplots of JV results (A) and JV curves (B) from experiment 2234. $CdCl_2$ treatment time varied from 600s to 1200s while maintaining all other process parameters.

Shown in experiment 2234, variation for $CdCl_2$ treatment time had negligible effect on V_{OC}, and a small positive correlation to J_{SC} with an increase of ~2mA/cm^2. Fill factor increased at 1200s of $CdCl_2$ treatment although this cannot be directly correlated to $CdCl_2$ process time because 1200s was the final process time tested and there is a positive trend in fill factor as the experiment was conducted. Fill factor was poor due to large amounts of series resistance as well as roll over kinks exhibited by the devise that were treated with 600s and 900s of $CdCl_2$. The trends were identical on the 250nm thick CdSe plates apart from overall lower J_{SC} and thus performance. J_{SC} remained low regardless of $CdCl_2$ activation time, suggesting the activation temperatures were suboptimal for performance.

Wet $CdCl_2$ treatments have shown to make successful, high performance CdSe based devices. The wet process that produced high performing devices with a similar structure is described here [21]. To investigate a better $CdCl_2$ treatment part of experiment 2377 was designed to minic the wet process using the vapor $CdCl_2$ process used at CSU. To simulate the process, films do not undergo preheat before they are transferred to the $CdCl_2$ source. There, $CdCl_2$ is deposited on the surface for 3 minutes. The source and substrate temperatures and kept at the baseline temperatures. After 3 minutes the substrate is moved to the annealing station where the heater is kept at 420°C. The annealing time was swept from 450s to 1650s and was done in a 40mTorr of 2% oxygen in nitrogen environment. To improve film thickness uniformity, the preheat time was dropped from 140s to 110s. This was discussed in earlier sections and did show uniformity improvement in the CdSe layer. Another difference is that lower substrate temperatures were utilized to help maintain film uniformity and improve deposition rates. Extensive warm up procedures for all systems have also been implemented to improve consistency across the experiments. Thus, the substrate temperature for CdSe deposition is

440°C instead of 475°C. CdTe deposition was kept constant. The absorbers in experiment 2377 utilized these changes. The delineation utilized the 1.3cm^2 area mask. All other process conditions remain consistent with baseline conditions.

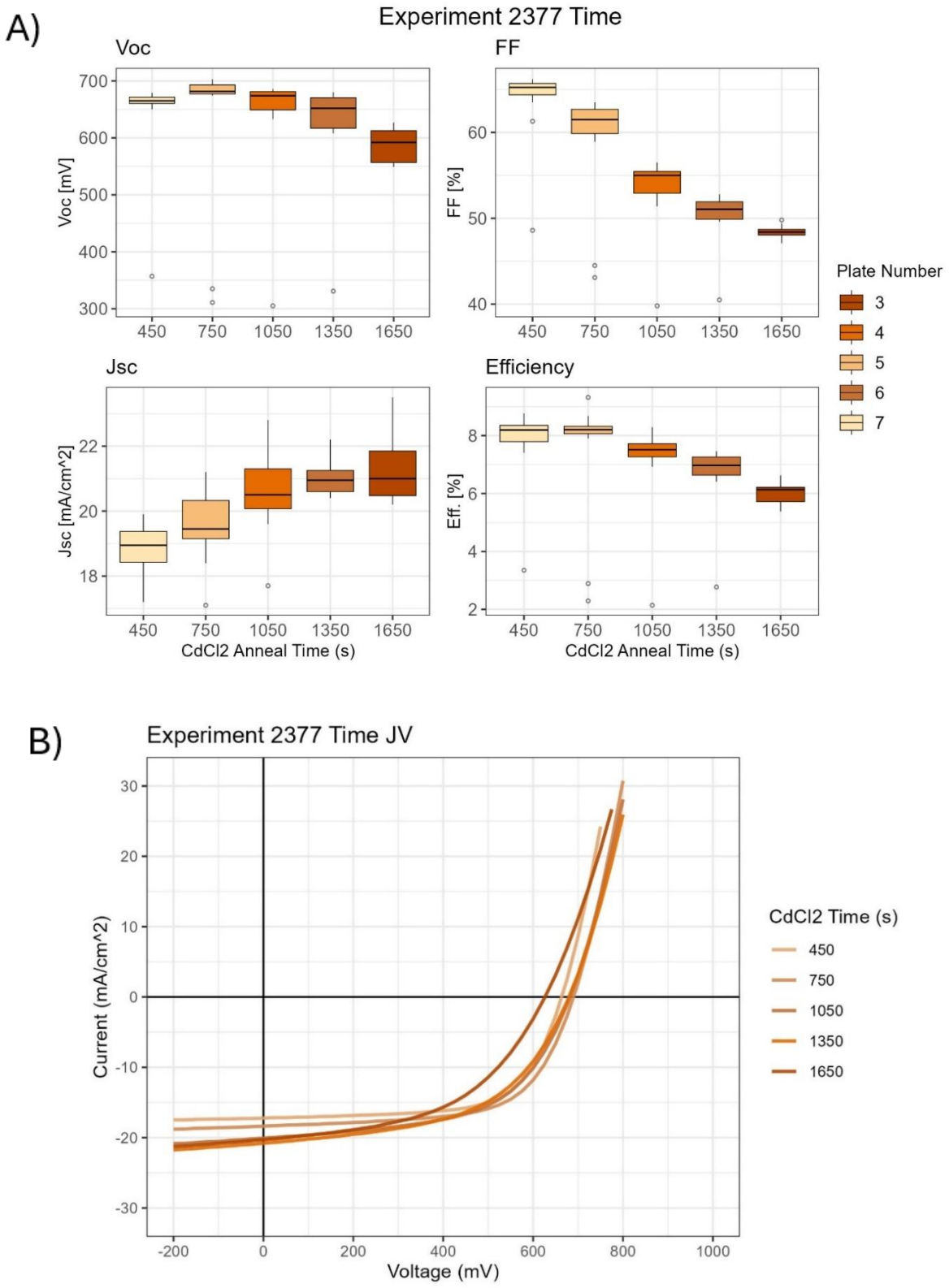


Figure 5.9: Boxplots of JV results (A) and JV curves (B) of experiment 2377. $CdCl_2$ anneal time varied from 450s to 1650s while all other process parameters remained constant.

At these $CdCl_2$ activation process conditions, anneal time had an overall negative effect of device performance. V_{OC} was maximized at the 750s anneal time and then worsened with higher anneal times. J_{SC} is maximized at the largest anneal time of 1650s. Fill factor worsened drastically with the shorted anneal time providing the best overall fill factor at ~65% and dropping to less than 50% at 1650s. Substrates were staggered to avoid substrate order affecting performance therefor the drop in fill factor is likely caused by the anneal time. To further investigate these processing conditions, EQE spectra was taken on the center device of each substrate.

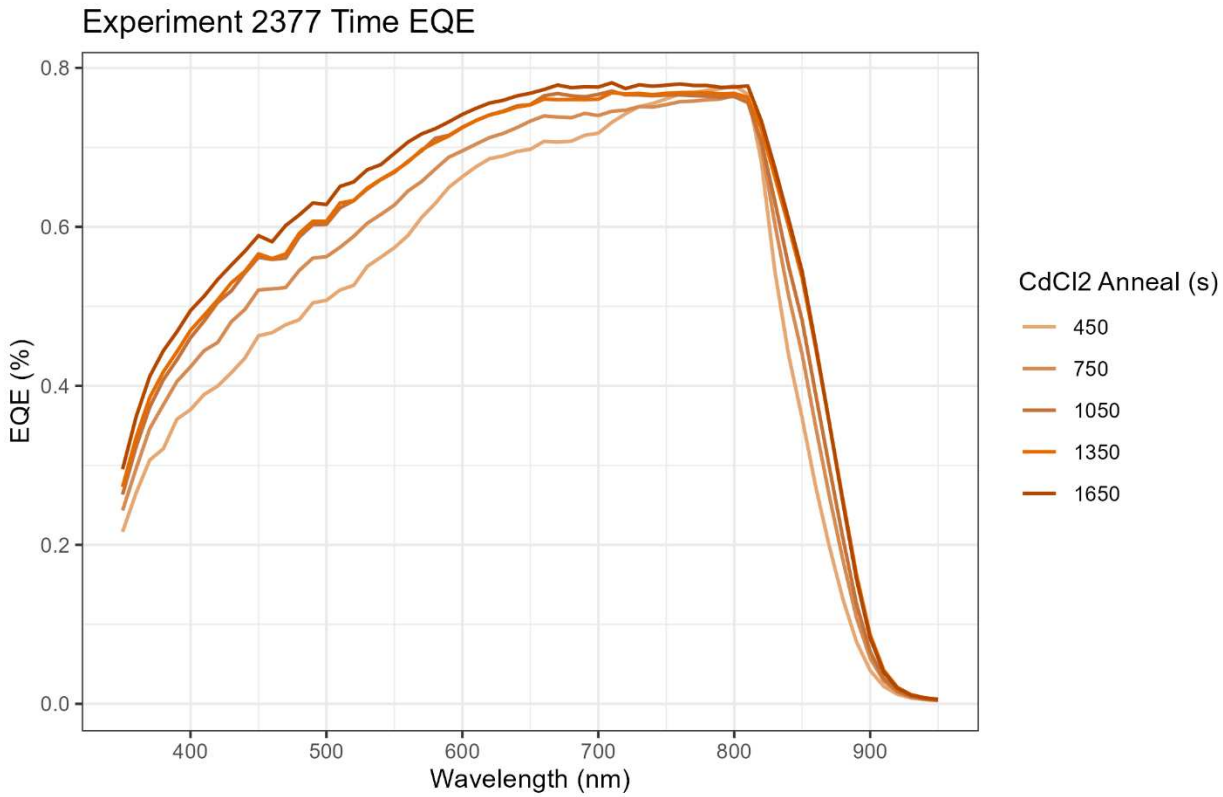


Figure 5.10: EQE spectra of experiment 2377.

Each device across each substrate exhibits poor current collection under 650nm of light, although the spectral response does improve with $CdCl_2$ anneal time. The low wavelength

response gradually improves with anneal time as well as the longer wavelength becomes higher and flatter with increased anneal time. EQE response in the near band region is improved for longer anneal times as well.

Experiment 2360 was conducted to explore different temperatures and time to see how it affected the 120nm/3.5-micron CdSe/CdTe devices. $CdCl_2$ treatment was within the $CdCl_2$ source only, without any time spent in a dedicated annealing station. Thus, the films were annealed in $CdCl_2$ vapor for the entire process listed. The substrate temperature for the $CdCl_2$ station was held at 420°C, which is a ~20°C increase from experiment 2234, while the source temperature dropped 10C from 450C to 440C. $CdCl_2$ process time was swept from 600s to 1050s. 120nm of CdSe and 3.5 microns of CdTe were chosen for the structure for reference to literature.

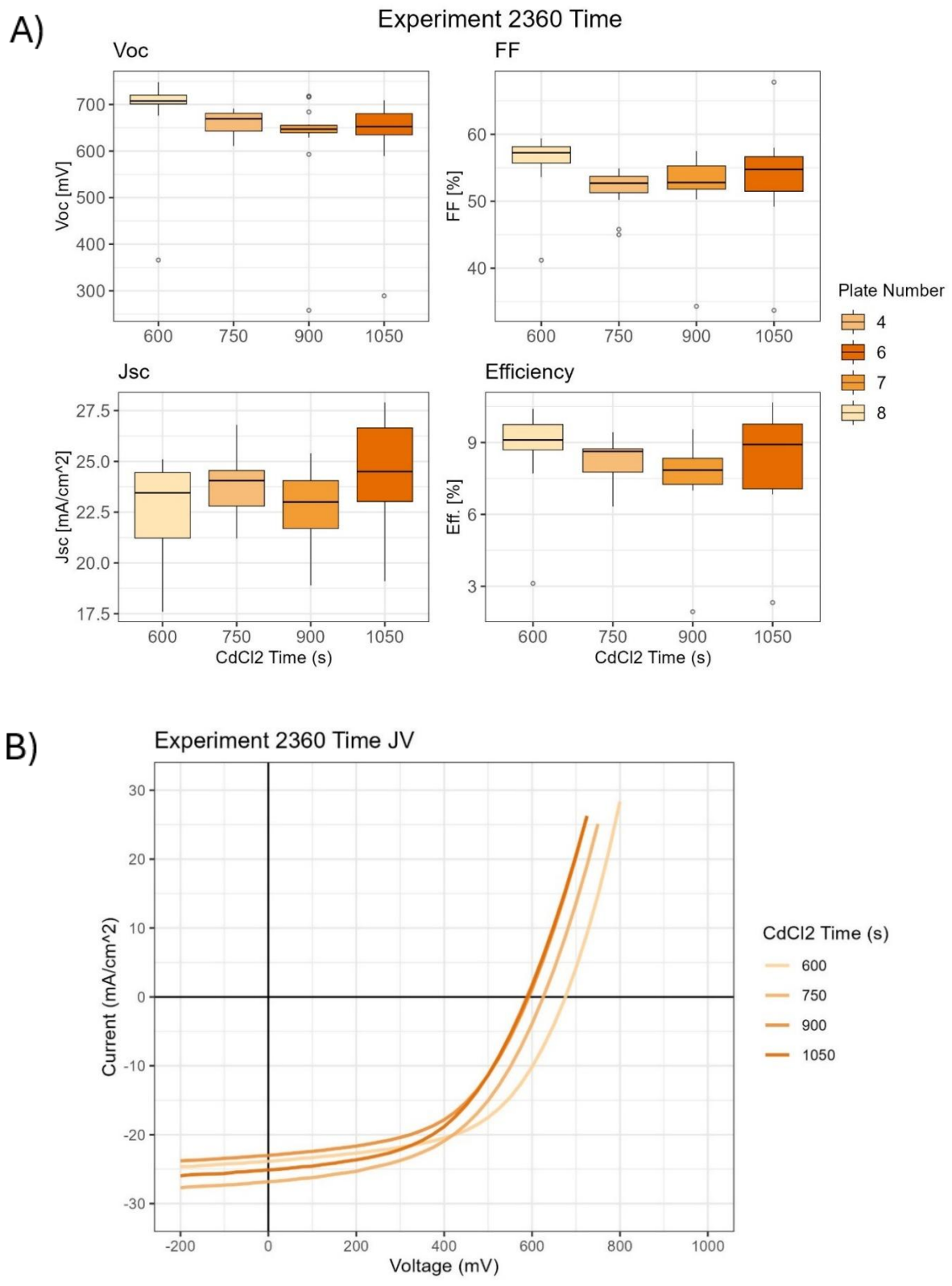


Figure 5.11: Boxplots of JV results (A) and JV curves (B) of experiment 2360. $CdCl_2$ treatment time was varied from 600s to 1050s while all other process parameters remained constant

JV results from experiment 2360 show a decrease in V_{OC} from 700mV above 600s $CdCl_2$ treatment time at these elevated temperatures. A very weak positive correlation to $CdCl_2$ time and J_{SC}, with a marginal increase of ~1mA/cm^2 with longer times. The overall fill factor of the experiment was low, around ~55%. 600s of $CdCl_2$ produced the highest fill factor with a median of 57%.

When comparing experiment 2360 to experiment 2234 at the 600s and 900s treatment time marks, it becomes apparent the new process conditions improved performance by ~5% efficiency Whether this improvement is due to the preheating conditions, new CdSe fabrication temperature, or the elevated $CdCl_2$ substrate temperature is unclear, although this fabrication process is better suited to CdSe/CdTe devices.

To further investigate elevated temperatures effect on CdSe device processing at CSU data analysis combined with experimentation was performed. Similar devises were taken from multiple experiments with comparable fabrication as well as $CdCl_2$ process time. The largest difference between these experiments was the substrate temperature during $CdCl_2$ processing. These were culminated and plotted to show a trend in substrate temperature versus performance. Each device had ~120nm CdSe, and 3.5 microns of CdTe. For sake of clarity, this plot will be called experiment F. Another key difference to the processing of these plates is there is no preheating of the samples before $CdCl_2$ activation. In contrast, the baseline 80s of preheating is standard.

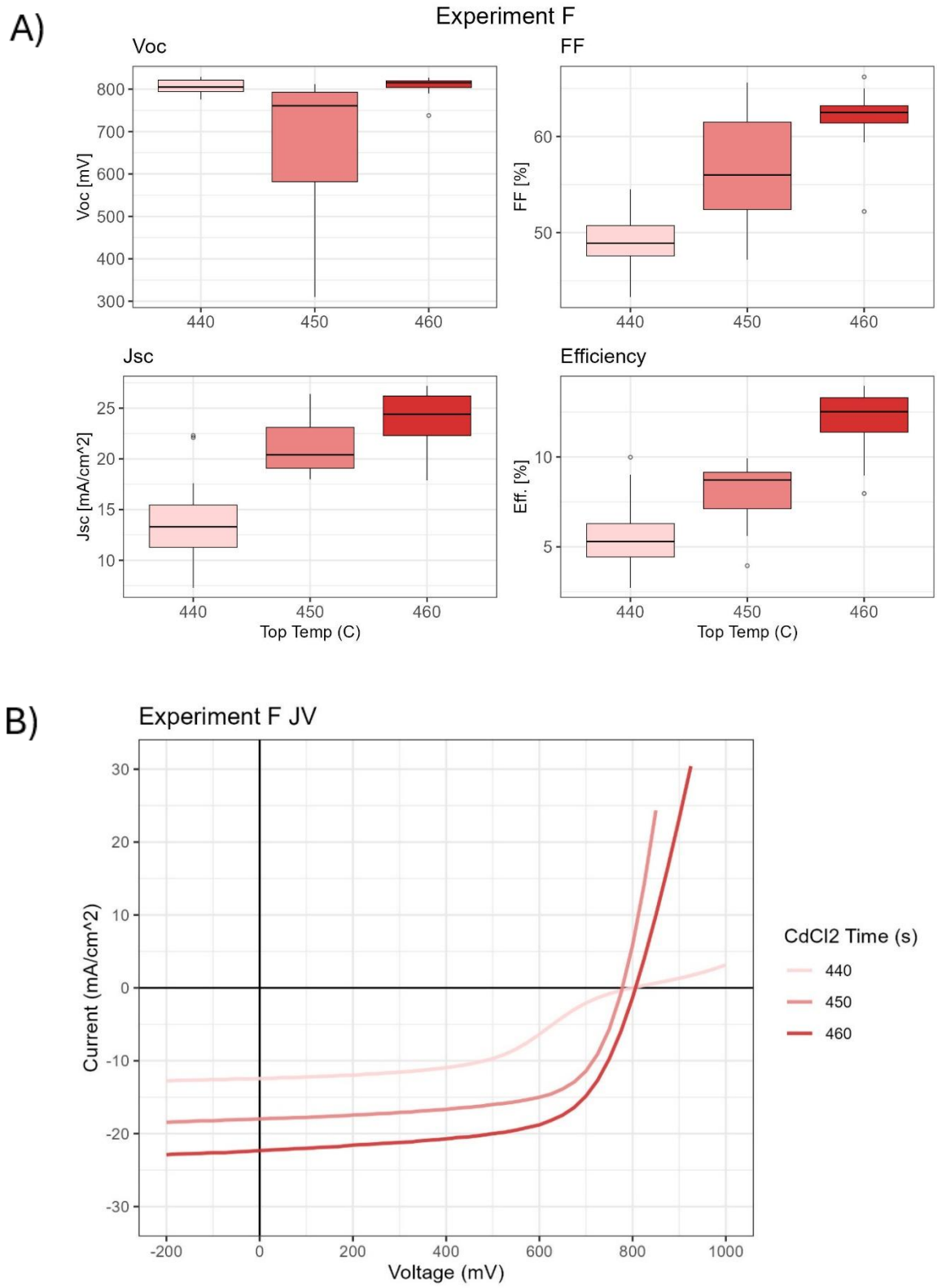


Figure 5.12: Boxplots of JV results (A) and JV curves (B) of experiment F. devices plotted maintained the same $CdCl_2$ time and source temperatures but varying top source temperatures from 440°C – 460°C.

All plates were treated for 10 min. Figure 5.12 clearly shows the improvement to J_{SC} and fill factor due to higher top source temperatures. The drop in V_{OC} of the devices annealed at 450°C is most likely due to other factors due to the rise back again at 460°C. These devices were fabricated before the known copper warm up time was implemented, driving the cause for the kink seen in devices treated at 440°C. This strong positive correlation between substrate temperature and performance may indicate the necessity for hotter temperatures due to the shorter annealing time due to the vapor $CdCl_2$ process. Due to this promising trend an dedicated experiment was performed to investigate $CdCl_2$ substrate temperature effect, to isolate other variations that may have occurred between the experiments where this data was pulled from.

Fabrication process for experiment 2360 maintained the lower CdSe substrate temperature at 440°C. No other differences were established from baseline other than a 60s preheat on copper doping instead of 120s. This change was made earlier in experimentation and kept for repeatability although it did not show an appreciable effect on device performance. Device structure was maintained at 120nm CdSe and 3.5micron CdTe for comparison to the previous results. Another difference in $CdCl_2$ processing was the incorporation of a substrate preheat before $CdCl_2$ activation.

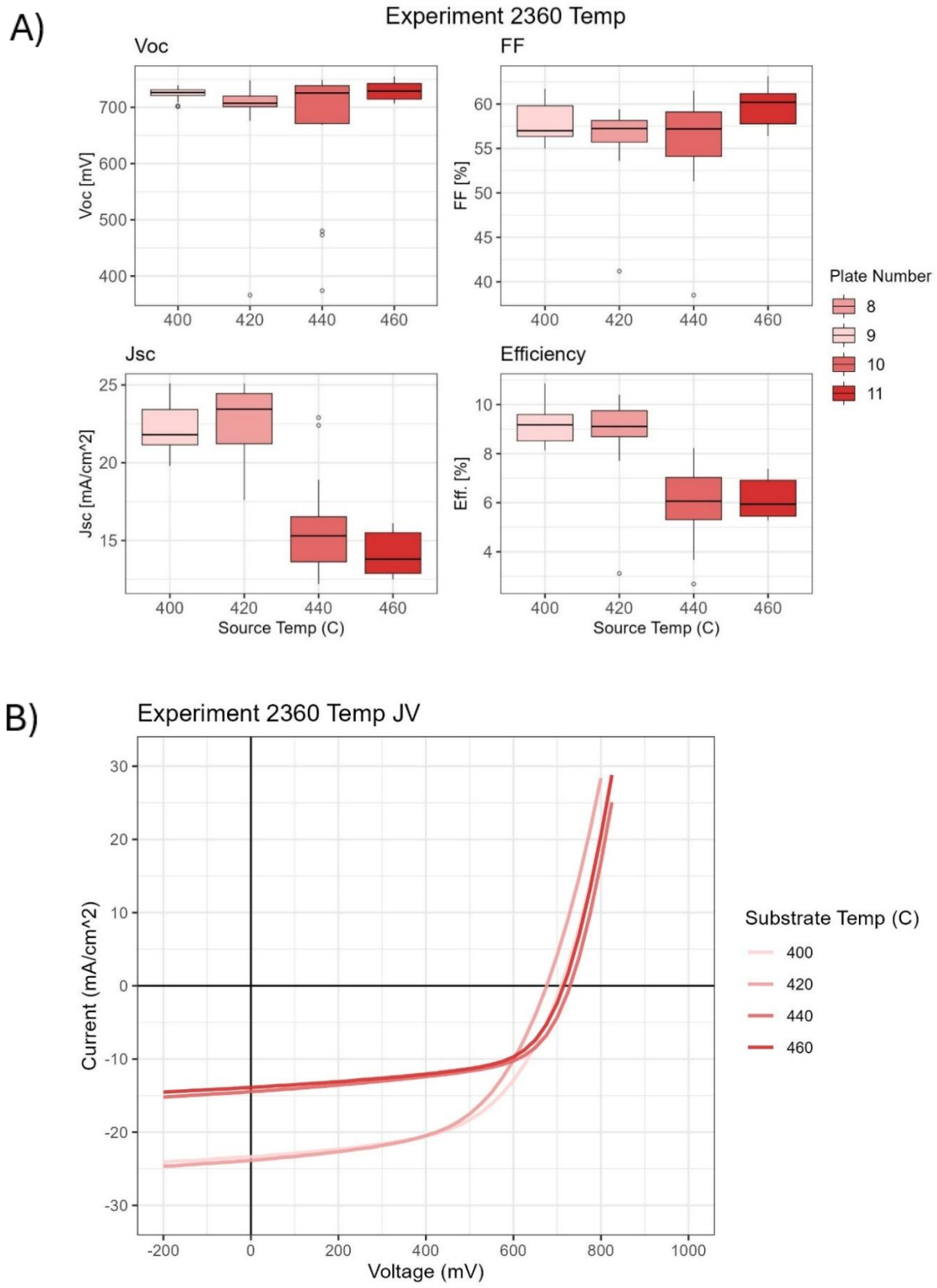


Figure 5.13: Boxplots of JV results (A) and JV curves (B) from experiment 2360. Substrate temperature varied from 400°C to 460°C during $CdCl_2$ treatment. Note, these treatments included a preheat.

V_{OC} remained independent of $CdCl_2$ substrate temperature, remaining around 720mV through the experiment. This is ~50mV less than experiment F. Substrate temperatures equal to 420°C and less have good J_{SC} with median sitting around 24mA/cm^2. Above these temperatures J_{SC} dropped dramatically to ~14mA/cm^2. Lower substrate temperature for experiment 2360 produce higher current by ~10mA/cm^2 than the 440°C annealed substrate of experiment F. Fill factor remained stable across the experiment with a slight improvement at the hottest substrate temperature.

The second part of experiment 2377 investigated the effect of elevated substrate temperatures without the including of a preheat step during $CdCl_2$ treatment. $CdCl_2$ source temperature remained consistent with experiment 2360 for easy comparison of the preheated and non-preheated samples. The substrate temperature was changed from 420°C to 460°C across three substrates. All other processes are listed above when discussing the first part of the 2377 experiment.

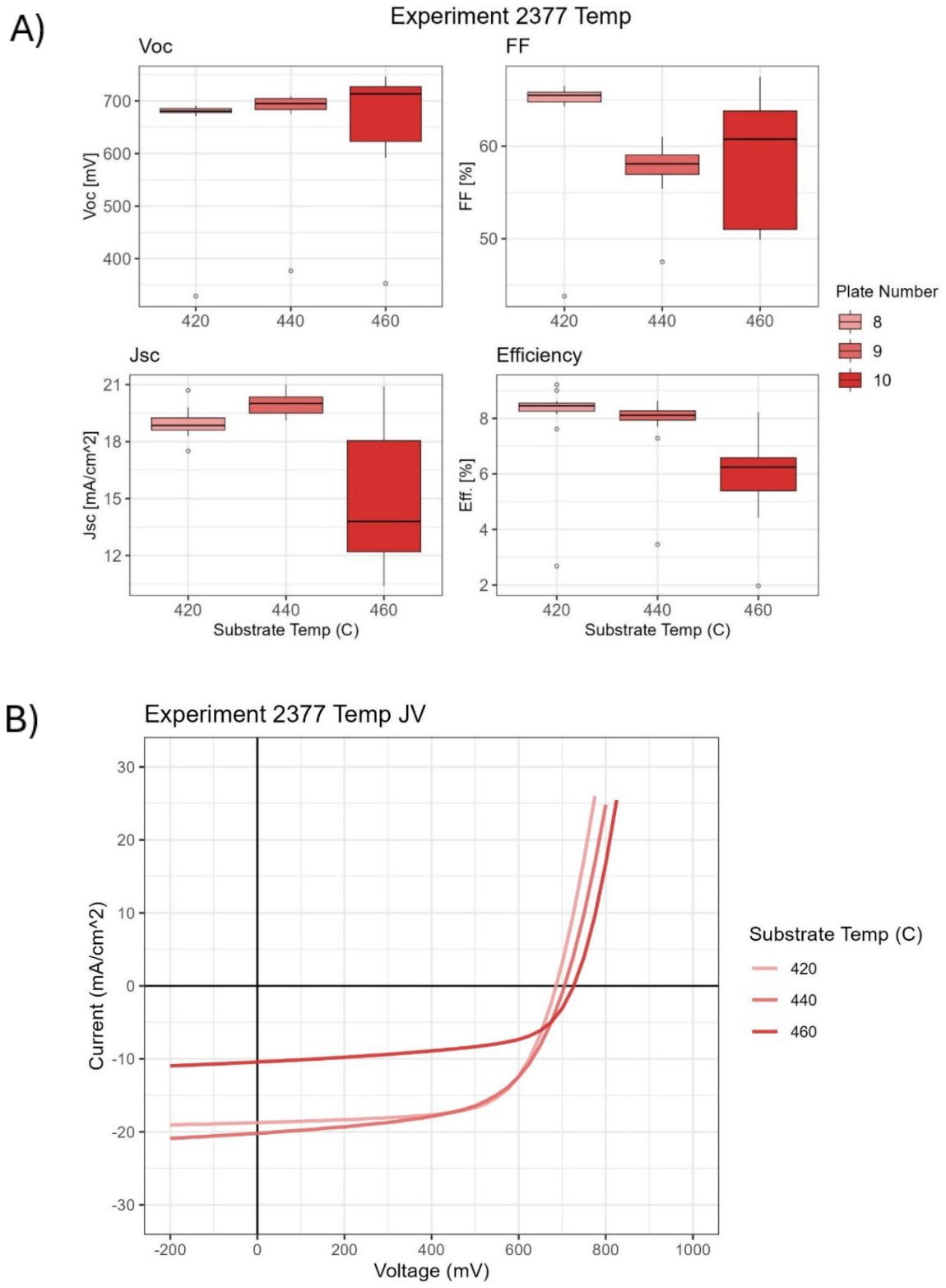


Figure 5.14: Boxplots of JV results (A) and JV curves (B) of experiment 2377. Substrate temperature varied from 420°C to 460°C during $CdCl_2$ treatment. Note, these treatments did not included a preheat.

V_{OC} improved with increasing substrate temperature during $CdCl_2$ treatment. Although, devices had an overall lower V_{OC} than experiment 2360. J_{SC} was maximized at 440°C although, still poor performing with a median at ~19mA/cm^2. This is contrasting to experiment 2360 where J_{SC} dropped significantly with substrate temperatures above 440°C. Although J_{SC} of the 420°C devices in experiment 2360 are higher than that of experiment 2377. The fill factor decreased from the maximum at ~66% to about a mean of 60% for elevated substrate temperatures. Although, increased variation of the hottest substrate saw some devices at comparable fill factor percentages to the 420°C substrate. Overall, the fill factor is improved in the devices without the use of the preheat step. Experiment 2360 saw fill factor percentage at ~57% or lower for most of the top source temperatures. EQE was taken of the center devices of each substrate to compare how the top source temperature effects the spectral response of each device.

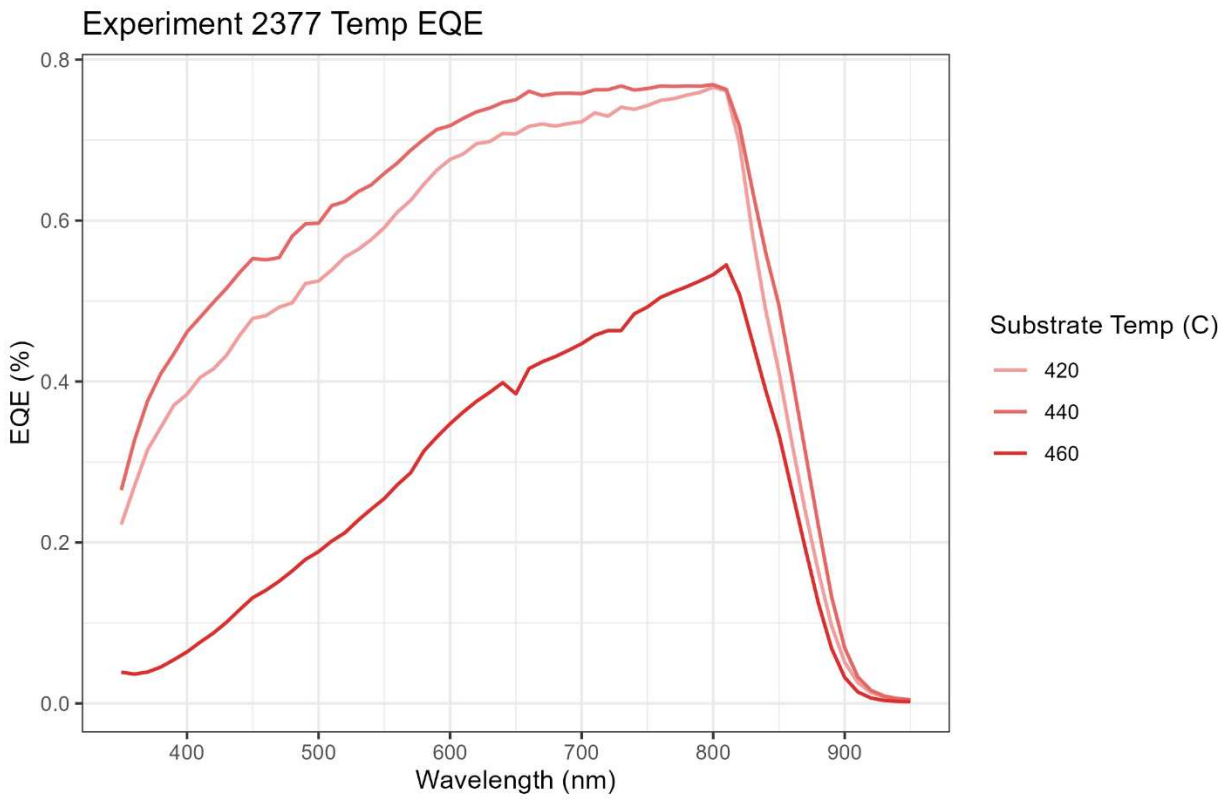


Figure 5.15: EQE spectra of experiment 2377 substrates with varying substrate temperature during $CdCl_2$ treatment.

The highest performing EQE spectra is of the device made with a substrate temperature of 440°C. The device made at 440°C has a good EQE response above 650nm and has an increase in response of the red region. Suggesting the 440°C treatment led to a better passivation of the absorber. The 420°C device exhibited a worse overall response across the spectrum. The 460°C response is very poor with poor absorption across the spectrum.

5.5 Introduction of CST ternary alloy aids in modulating Se diffusion for a more suitable band alignment

Optimal band grading is integral to high performance CdTe [15], [20]. Therefore, a second alloying scheme has been investigated to aim for high performance and ease of processing conditions. An additional layer of $CdSe_xTe_{1-x}$ (CST) is deposited in between CdSe

and CdTe via sublimation in the ARDS. Source material for sublimation deposition of CST is an allow of 40% selenium to 60% tellurium ($CdSe_{.4}Te_{.6}$ or CST40). While the actual stoichiometry is process dependent, it is expected to deposit a film with Se anywhere for 30% to 40% [32]. Due to difficulties achieving optimal band grading via a vapor $CdCl_2$ treatment, the ternary alloy of CST was introduced in between the CdSe and CdTe layer. In practice, this pre-grades the absorber with Se, before $CdCl_2$ treatment.

To begin investigating the effect of the additional layer of CST on device performance and process conditions, a baseline structure was chosen based on literature and the MZO based device structures. The structure chosen was 50nm CdSe, 300nm CST, and 4 micron of CdTe. The first experiment utilized known high performance fabrication techniques used for MZO based devices to contrast the CdSe/CST structure to MZO/CST structures as well as CdSe only structure, For the $CdCl_2$ treatment, baseline temperatures were used (390°C substrate, and 450°C source) as well as the baseline preheat of 80s. The time of the $CdCl_2$ activation was swept from 300s to 1800s. The entire duration of the $CdCl_2$ was within the $CdCl_2$ source, like MZO based processing.

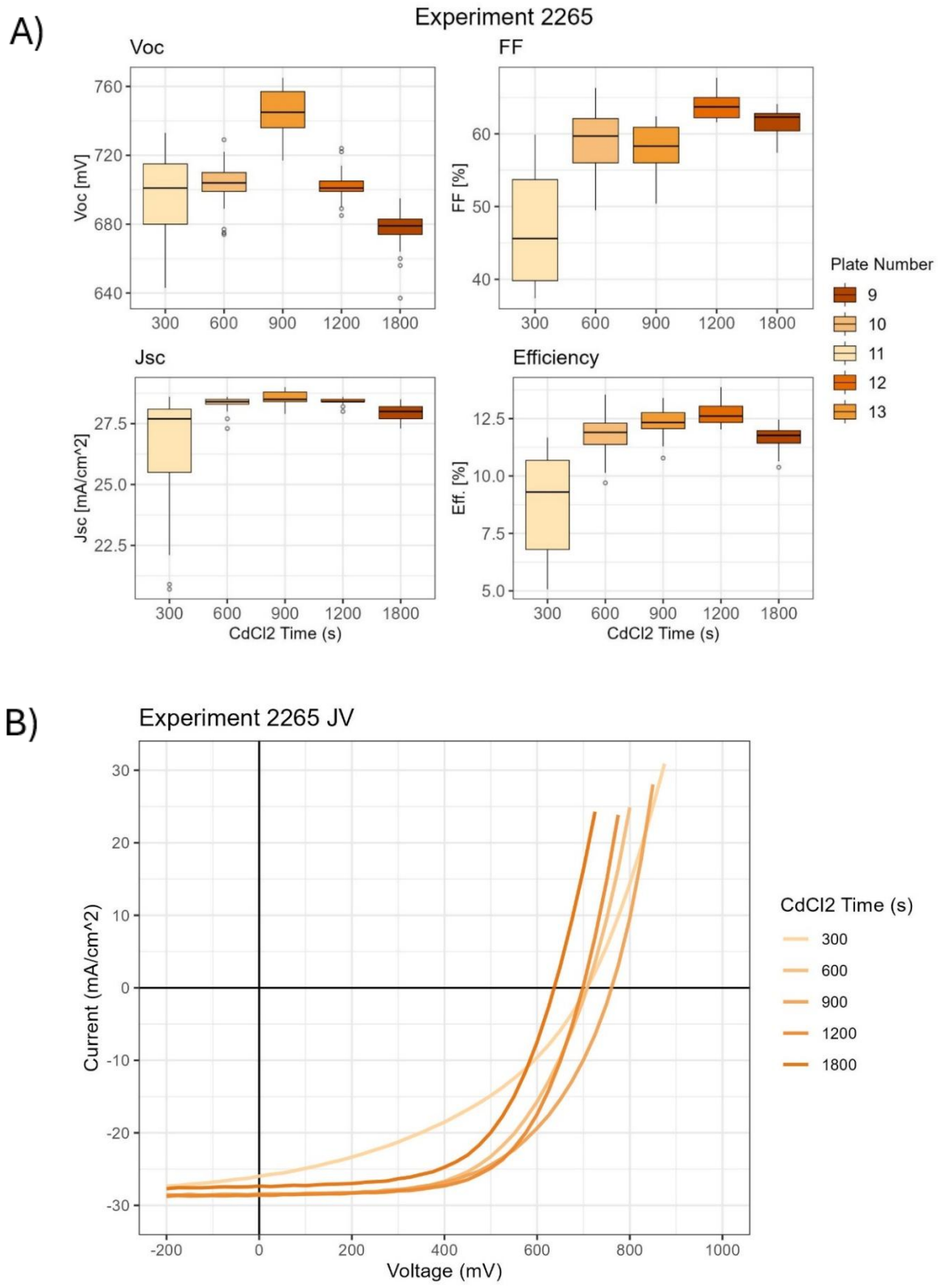


Figure 5.16 Boxplots of JV results (A) and JV curves (B) of experiment 2265. Experiment implemented the novel CdSe/CST/CdTe absorbers while the $CdCl_2$ process time was swept from 5 - 30 min.

As seen, the introduction of CST into the absorber increases short circuit current density from ~22mA/cm^2 in CdSe/CdTe devices to ~28mA/cm^2 at these $CdCl_2$ treatments. Although these devices do exhibit lower overall V_{OC} was lower with the highest performing substrates having a mean of ~760mV at 15 minutes versus some CdSe/CdTe devices exhibiting 800mV. V_{OC} and J_{SC} began to drop past 15 min of $CdCl_2$ suggesting overtreatment of the $CdCl_2$ activation process. There seems to be no correlation to fill factor and the order of fabrication as previously seen. Therefore, it is unlikely, the trend played a large role in influencing the increase in fill factor with increase in $CdCl_2$ time. A follow experiment was performed to investigate an improvement of fill factor at the 15min $CdCl_2$ process time. Fill factor did improve with higher process times, indicating better interface passivation of the front contact.

With decent performance yielded from experiment 2265, and literature and experimental evidence supporting a change in the copper doping process [21], an experiment was performed to investigate the effect of substrate preheat time on device performance. Devices were fabricated utilizing the same process as was used in experiment 2265. The 900s $CdCl_2$ process was chosen due to its high performance shown in experiment 2265. The variable tested was the preheat on the copper doping process. The preheat time varied from 0s to 120s. The 120s time is the baseline for this process. The goal of the experiment was to identify if substrate temperature, when beginning the copper dosing process had an appreciable effect on device performance.

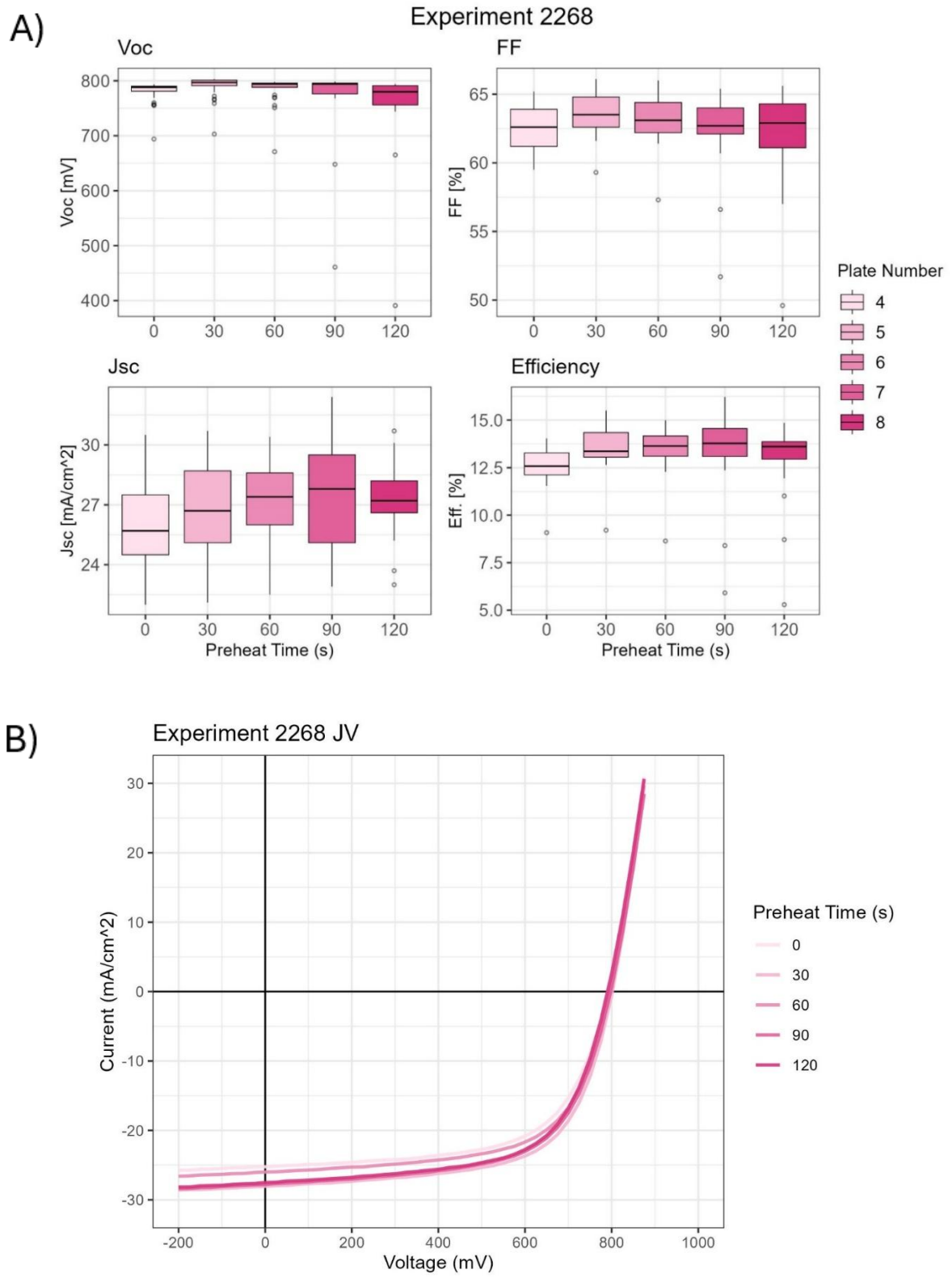


Figure 5.17 Boxplots of JV results (A) and JV curves (B) of experiment 2268. Experiment 2268 utilized the same structure as 2265 while CuCl preheat time swept from 0 – 120 s.

All performance parameters improved regardless of preheat time during the Cu process. Standard copper preheat time is 120s and when referencing this baseline to experiment 2265, it shows this experiment resulted in higher V_{OC} (~40mV improvement) and higher fill factor (~5% improvement) despite identical $CdCl_2$ and CuCl process conditions and times. Suggesting the improvement in performance is not due to either process. The absorbers layer thicknesses were kept constant between the two experiments to avoid any thickness differences contributing to the variation in the data. Due to the impressive performance of these devices, and without clear evidence as to why these devices performed so well, further measurements and analysis were conducted to investigate the mechanisms as to why these devices performed so well.

To identify any trends in device performance caused by processing conditions withing the ARDS, heatmaps of device performance were plotted. This spatial representation of the device performance gives insight into what processing conditions are optimal for performance based off fabrications trends.

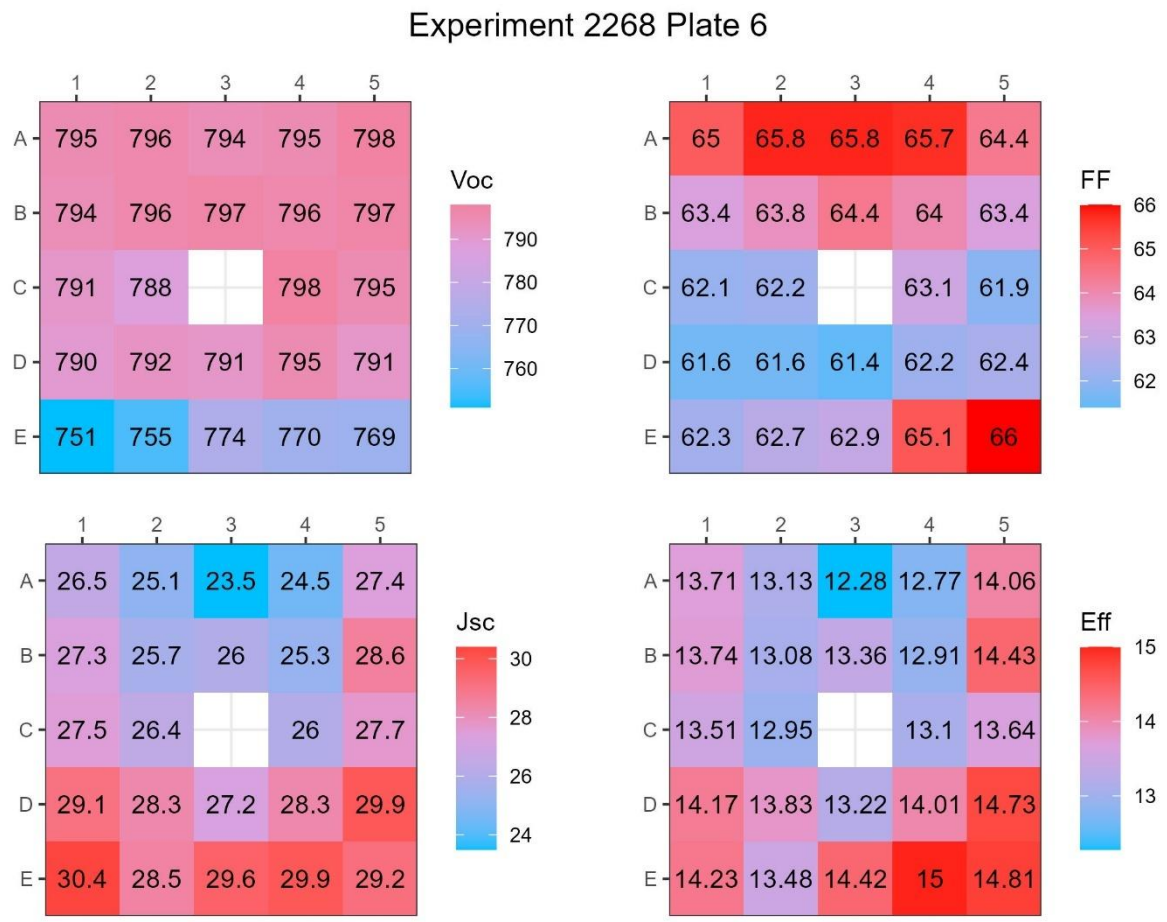


Figure 5.18: JV performance heat map of the 6th plate of experiment 2268. Note the center device was removed in the plot for each plate due to it being the place for thickness calibration and therefore poor performance.

V_{OC} remains constant until the bottom row which drops about ~40mV. J_{SC} rose in a U-shape, the bottom and right rides of the U performed best and the center the worst. The fill factor was highest on the top row as well as the E4 and E5 devices. When combined into efficiency, this resulted in a U-shaped efficiency across the substrate with the E row as well as 5th column performing best. The E4 device was also measured because it was best performing. This is common upon devices made at CSU as stated earlier. To characterize the difference in current collection EQE was taken of devices within the 5th row.

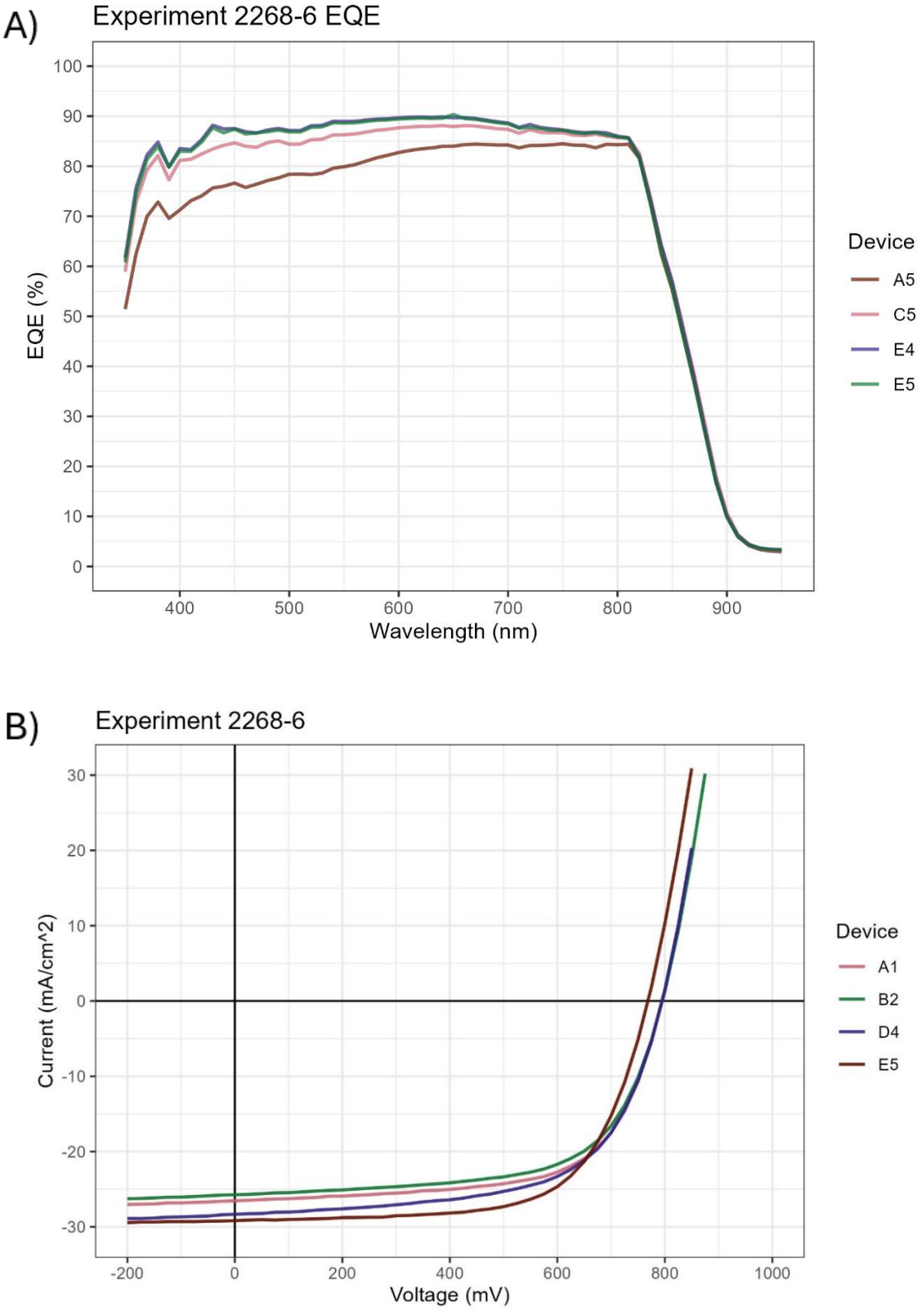


Figure 5.19: EQE spectra (A) and JV data (B) of devices from the 6th plate of experiment 2268.

As seen, the two devices at the bottom of the device exhibit the best overall EQE response across the measured spectrum. Devices higher up on the substrate exhibit worse respond across the spectra with the top device A5 having the worst overall performance. The performance of the A5 device is worse in shorter wavelengths and slowly grows until ~650nm of light. Above 650nm the response flattens out although it is still worse than devices E5 and E4. Suggesting parasitic absorption of excess CdSe contributing the poor response under 650nm. The JV curves reveal an improvement in fill factor of the E5 devices though increased shunt resistance as compared to the other devices.

Due to large change in performance from experiment 2265, with no obvious change in processing conditions, the calibration for thickness was doubted. A series of experiments were performed to investigate a possible thickness change in the structure that led to this performance gain. CdSe thickness varied while utilizing the same $CdCl_2$ and copper processing. Comparable substrates were compared across each experiment. For the sake of clarity this analysis will be called experiment G.

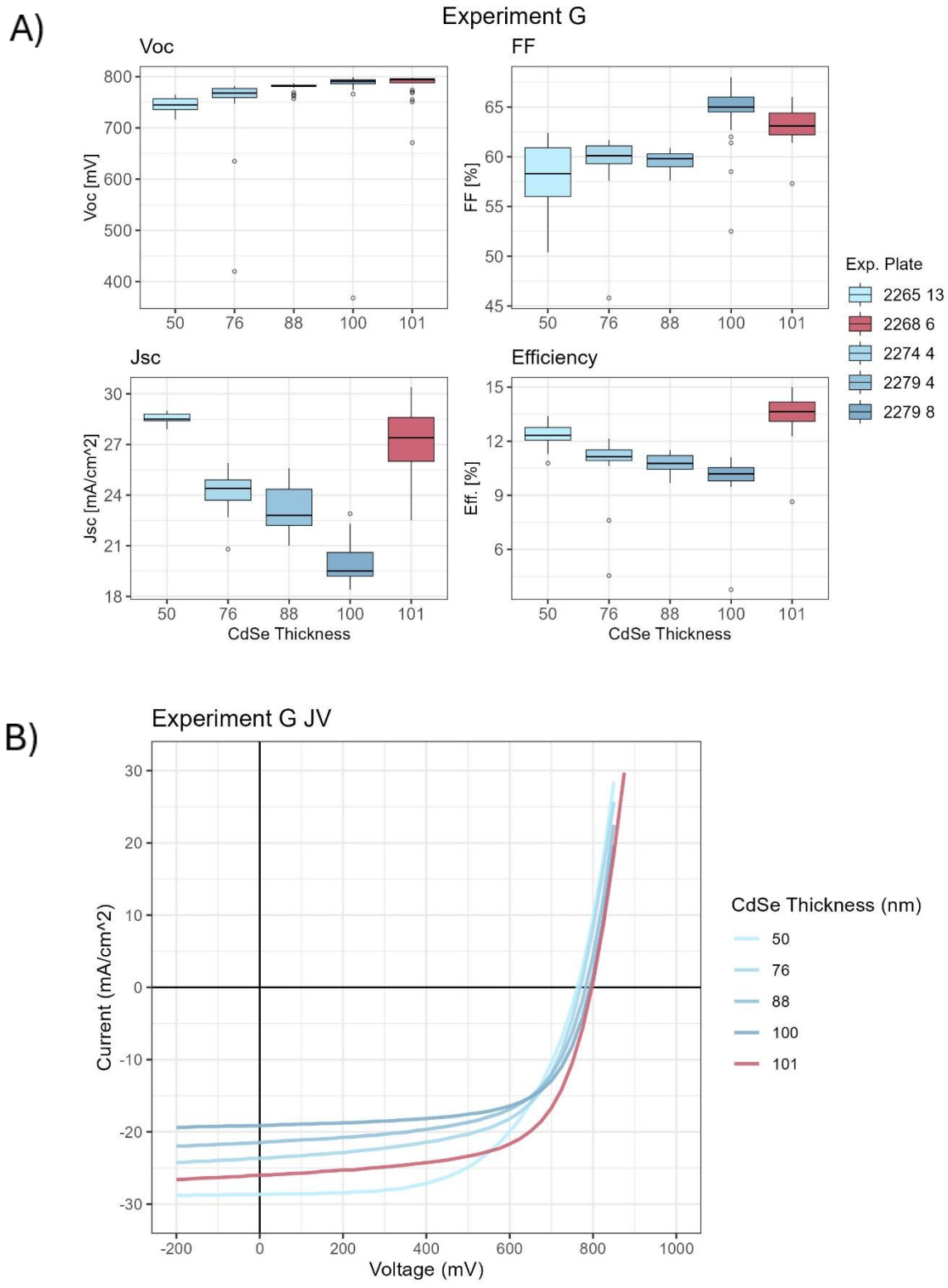


Figure 5.20: JV parameters of experiment G. Blue color indicate a variation of CdSe thickness while red indicates an unknown thickness, 101nm is simply a place holder. The experiment and substrate numbers can be seen in the legend.

For reference, blue indicates a known thickness of CdSe, while red indicates unknown. The 2268 plate (red), thickness was originally calibrated to 50nm, although due to a drastic performance increase this calibration was doubted. When looking at the V_{OC} plot, the 2268 plate looks as if it has ~100nm of CdSe. The opposite is true of the J_{SC} plot. Fill factors plot seems to place the CdSe thickness around 100nm. Therefor it remains unknown the exact reason why 2268 experiment performed so well.

6 DISCUSSION

6.1 A n-type window/buffer layer is necessary to mitigate voltage loss

Although experiment performance was worse overall for experiment 2329, the trend in performance is useful. As seen, as the ratio of CdSe to CST was increasing a clear positive correlation to V_{OC} is shown. The devices with no CdSe (0nm of CdSe) had very poor V_{OC}. Similarly, this trend appears in experiments 2231and 2248. Where increasing deposited CdSe thickness positively correlates to increasing V_{OC}. This evidence supports the hypothesis that an n-type window layer aids in mitigating voltage loss. Devices with “too thin” to little CdSe deposited result in devices with poor voltage. Although, the introduction of CdSe at these processing conditions, does decrease overall J_{SC} as well as fill factor as compared to MZO. The loss in current is likely attributed to parasitic absorption from excess CdSe at the front at the device. The loss in fill factor may be resultant from the excess CdSe at the front of the device as well. The very small grains of CdSe layer results in a large density of grain boundaries, which serve as recombination centers at the front of the device.

6.2 CdSe window layer thickness is directly correlated to V_{OC} and inversely correlated to J_{SC}.

CdSe layer readily diffuses into CdTe during $CdCl_2$ activation treatment. Therefore, it serves multiple purposes. It serves as the selenium source for grading selenium into the absorber to create a graded absorber as well as being responsible for creating the n-type window layer for the device. Therefore, to investigate the thickness effects of CdSe on device performance it is important to assess both the precursor thickness and well as the $CdCl_2$ treatment.

Experiment 2231 and 2248, investigated the relationship of the deposited thickness of CdSe to CdSe/CdTe device performance, with respect to a constant $CdCl_2$ process. Results showed increasing CdSe thickness led to higher V_{OC}, although V_{OC} did not crest above 800mV. Fill factor also improved with increasing CdSe thickness regardless of order of fabrication as seen in experiment 2248 where CdSe is varied from 100nm to 200nm. Although, as seen in 2231, the order of fabrication played a large role in fill factor, therefore another process condition may also play a large role in fill factor of the device regardless of CdSe. J_{SC} was reduced as CdSe thickness increased throughout the experiment. Due to consistent $CdCl_2$ activation, and if the thickness of the CdSe layer does not have an appreciable effect diffusion rate of CdSe into CST, thicker CdSe precursor layers would result in a thicker residual layer after treatment. This thicker layer, if too thick, would greatly contribute to parasitic absorption of light due to its bandgap of 1.7eV. Improvement of V_{OC} and fill factor may be attributed to a better diode quality due to the establishment of a proper “buffer” between TCO and the active layer.

Experiments 2234, 2377, and 2360 were performance to investigate the relationship between $CdCl_2$ activation time with respect to variance processing conditions. 2234 was performance to investigate the effect of a $CdCl_2$ process used to create high performance MZO

based devices. The variance on $CdCl_2$ activation time was performed on substrates with 200nm and 250nm of CdSe. The variance of time from 600s to 1200s had very little effect on V_{OC}, and an undetermined effect on fill factor and J_{SC} due to system trends discussed earlier. J_{SC} remained quite low, and even lower for the 250nm CdSe plates. Again, suggesting excess CdSe at the front of the device parasitically absorbing light. Trends for the 250nm CdSe devices were similar apart from even lower current collection, again supporting excess CdSe. Poor performance is due to either too thick CdSe, and/or suboptimal $CdCl_2$ processing.

Experiment 2377 similarly investigated the effect of $CdCl_2$ activation time though utilizing various process conditions. Aimed to better mimic known wet $CdCl_2$ treatments, devices in experiment 2377 were done with $CdCl_2$ withing a source and then annealed in another with varying times from 450s to 1650s. CdSe thickness was 120nm and CdTe was 3.5microns. The device structure was modeled after a literature supported device structure for direct compassion of the methods. V_{OC} was maximized at 750s of treatment time. Increasing anneal time decreased overall V_{OC}. Fill factor was maximized at the lowest activation time and became worser with higher performance. J_{SC} did increase as time increased but remained relatively low with a median of 21mA/cm^2. Low overall voltage and a decreasing fill factor suggest this activation treatment was suboptimal for this structure. The EQE spectrum improved as $CdCl_2$ anneal time increased, agreeing with the increase in J_{SC}, although all devices did maintain poor EQE response in low wavelengths, characteristics of parasitic absorption. EQE response in the near band region has improved for longer anneal times. Possibly suggesting a reduced recombination at the rear surface interphase, or possibly longer diffusion lengths due to more selenium passivation [33]. Although, parasitic absorption was not eliminated through anneal time alone, suggesting either a different dose time or anneal temperature is needed for high performance.

The first part of experiment 2360 utilized higher temperatures, and a treatment style like how the MZO devices are treated, in which the entire treatment was done withing the $CdCl_2$ source. The activation time was swept from 600s to 1050s, while the substrate temperature was kept at 420°C. This treatment did not have an appreciable effect on V_{OC} as compared to 2377. The fill factor was worse for lower treatment times as compared to 2377. This method dd improved J_{SC} considerably with a much larger portion of devises producing currents larger than 22.5mA/cm^2. Through these experiment it has become apparent that varying treatment time is not sufficient to fabricate high performing CdSe devices.

To gain more insight about the effect of differing substrate temperatures during $CdCl_2$ activation, data of comparable structure and the same $CdCl_2$ treatment time were collected. The only difference between these substrates was the substrate temperature during $CdCl_2$ treatment as well as the 440°C and 460°C substrates were deposited previously via a different method than. All other processing such as $CdCl_2$ and copper treatments were done at CSU. As seen, these devices exhibit higher voltage, improve fill factor and current with increased substrate temperature. The large variance in the substrate fabricated at CSU can be attributed to uniformity issues in film thickness due to trends within the ARDS. This may be an indication that higher temperature and required to fully grow the grains of CdSe/CdTe based devices within a shorter time. Mahisha Amarsinghe et. al. showed similar results for a vapor $CdCl_2$ treatments annealed at 475°C resulted in larger grains than 420°C. EBSD, imaging of the absorbers showed complete grain growth, front to back of the absorber and the annihilation of horizontal grin boundaries of thinner CdSe samples ~75nm [34]. Therefore, the improvement in overall performance may be due to better grain growth during $CdCl_2$ treatment. The variation in performance is most likely due to uniformity thickness issues currently experienced in the ARDS at the time.

With these promising results, experiment 2360 was dedicated to establishing repeatability with absorber deposited at CSU. Results from the experiment showed a lower overall V_{OC}, and a higher average fill factor. J_{SC} improved from 400C to 420C but dropped off significantly above 440C. Results from the experiment are dominated by the sudden drop in J_{SC}. Performance at 440C for both experiments are similar, but performance of 460C is drastically different in terms of J_{SC}. Devices treated at 420°C in experiment 2360 have poor performance similar to undertreated device. This in conjunction with the performance disparity of the 460°C devices may suggest the inclusion of the preheat step in experiment 2360 inhibited full treatment of devices above 420°C. It's possible that the matching performance for the 440°C plates is of different causes for different experiments, i.e., not enough temperature or time in experiment F caused for an undertreated devices but an excess in temperature caused the undertreated device in experiment 2360. This is possible due to the mechanics of the vapor $CdCl_2$ processing, in that a temperature differential between the source and substrate is partially responsible for the transfer of source material to the substrate. If the substrate is at a much higher temperature than the source temperature, this may cause problems with the transfer of material to the substrate. Thus, when including a preheat, the substrate temperature may be too high for effective transfer of chlorine to the substrate for treatment. Experiment 2377 was performance to show the contrast to not utilizing the preheat step during $CdCl_2$ treatment. Results were much better performance at 440°C than 2360, although a drop in performance again occurred at 460°C. J_{SC} did improve from 420°C to 440°C. Due to the trend of improvement between 420°C and 440°C, and a decrease in response from 440°C to 460°C suggest the dip in performance is from overtreatment of the device. Although, it is important to note the mechanics of the vapor $CdCl_2$ process. At a substrate temperature of 460°C the substrate would be at a much greater temperature than the source

temperature. This may cause an disruption of vapor flow to the substrate and result in an undertreated device. When the 460°C substrate was removed from the ARDS it had very little $CdCl_2$ haze, which supports this theory. The EQE spectra of the device treated at 460°C bears a similar resemblance to the spectra of a device made with excess CdSe at the front which also suggest an understatement occurred [21], [22]. The authors cited the excess CdSe caused amount of parasitic absorption.

Devices that are $CdCl_2$ treated with lower substrate temperatures reveal a trend that matches the hypothesis posed. V_{OC} tends to increase with increasing CdSe window layer thickness while J_{SC} decreases. Devices that experience elevated substrate temperatures during $CdCl_2$ treatment do not follow the hypothesis. V_{OC} increases while J_{SC} also increases with substrate temperatures that are not above 440°C. Thus, due to the inconsistency of data trends, the second hypothesis remains inconclusive.

6.3 Introduction of CST ternary alloy aids in modulating Se diffusion for a more suitable band alignment

Difficulties in achieving high V_{OC} and J_{SC} on CdSe based devices drove the motivation for incorporating the ternary CST alloy between the CdSe and CdTe. The preliminary experiment 2365 shows the immediate improvement of J_{SC} with currents reaching ~27.5ma/cm^2. The 900s $CdCl_2$ time with a substrate temperature of 390°C produced the highest V_{OC}. Indicating the best quality grading of the absorber to achieve the highest voltage. When investigating Cu preheat the performance drastically improved (experiment 2268), although the comparison plate of 120s was the identical fabrication process. Although the reason why this improvement is unknown, the higher performance shows promise for this device structure. The heatmaps of JV data for 2268 show the bottom areas yielding the highest performance. Known ARDS trends correlate these

areas to hotter substrate temperatures, meaning thinner CdTe layer thickness and hotter $CdCl_2$ substrate temperatures during activation. Further looking into the variation of performance across the plate via EQE shows the bottom device exhibiting the best overall EQE curve, with the highest response across the entire spectrum. Due to the very high uniformity of the CdSe layer, this improvement in performance is most likely due to $CdCl_2$ activation temperature or CdTe thickness/deposition temperature. Meaning the devices higher on the plate have a thicker residual CdSe layer after $CdCl_2$ treatment contributing to the small amount of parasitic absorption as seen in the EQE spectra. This is also supported by the heatmaps of V_{OC} with the highest voltage seen at the top of the devices, indicating a thicker CdSe layer. To establish repeatability many following experiments were conducted with varying CdSe thickness. Comparable substrates were plotted on and called experiment G. As seen, the CdSe thickness is not the only impactful variable given the high voltage and high current of the 2268 experiment.

Plots comparing substrates across each hypothesis were made to better discuss the impact of the introduction of deposited CST onto device performance. The first figure below depicts JV curves from devices with varying performance.

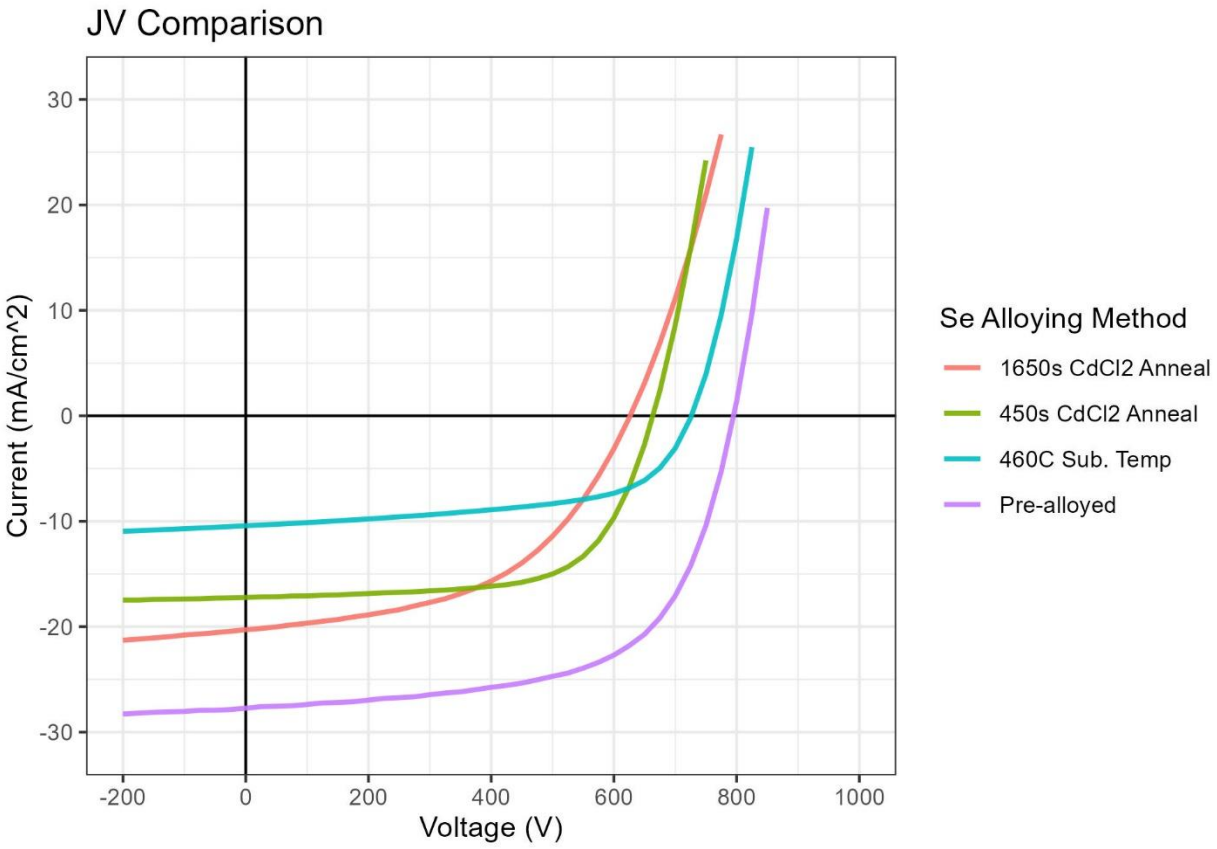


Figure 6.1: JV curves of devices with varying performance.

Shown in figure 6.1 are JV curves from four devices. Red, green, and blue each have the same structure of 120nm of CdSe and 3.5 microns of CdTe while utilizing different $CdCl_2$ treatments, these devices were fabricated in experiment 2377. Purple is a pre-alloyed device fabricated in experiment 2268. Each devices are from similar areas on the substrate to avoid variation in non-uniformity affecting the comparison. The blue device is representative of the devices fabricated early on in experimentation. These devices exhibited decent voltage but very poor current. The 460°C substrate temperature during $CdCl_2$ treatment produced devices like those with excess residual CdSe, resulting in very poor J_{SC} due to large amounts of parasitic absorption. Red and green devices are representative to what was achieved through optimizing $CdCl_2$ treatments and CdSe thicknesses utilizing the vapor $CdCl_2$ activation treatment. As seen,

these devices exhibit better J_{SC} although they remain low with an average of ~23mA/cm^2. The improvement of J_{SC} to acceptable values often resulted in the drop in V_{OC} due to insufficient CdSe layer thickness. The purple device represents what was possible through the introduction of CST as an intermediate layer between CdSe and CdTe. The reintroduction of CST allowed for the fabrication of devices that exhibited much greater J_{SC} and improved V_{OC} suggesting a more optimal band alignment was achieved utilizing the vapor $CdCl_2$ treatment. To further show the progress in device performance, EQE of each of these devices was taken and plotted.

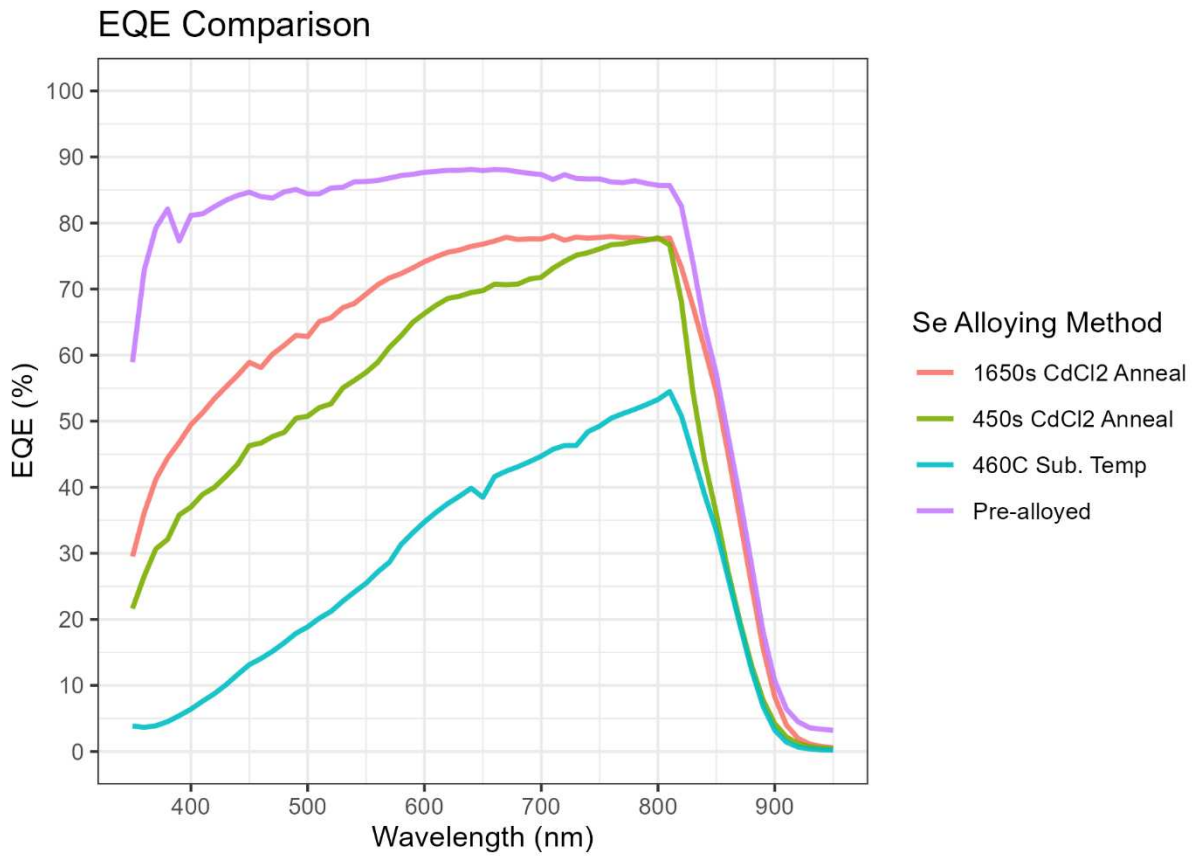


Figure 6.2: EQE spectra of devices of varying performance.

As seen, the EQE response of the blue device is very poor with large amounts of parasitic absorption and overall low response throughout the spectrum. The effective bandgap of this device is also larger than that of the better performing devices which may indicate an ineffective

interdiffusion of CdSe into CdTe to create a CST. This spectrum matches closely to those shown in literature to have excess CdSe at the front of the device [22]. The green devices have a much larger improvement in performance, yet it still exhibits large amounts of parasitic absorption and the same effective bandgap as the blue device. The red devices utilized the same $CdCl_2$ treatment as the green devices did with the exception that it was treated for much longer. As shown in the JV curve, this improved the current collection of devices. This is supported by the improved EQE response as well as the smaller effective bandgap, shown by the shift in the band edge. Although this improvement in J_{SC} was accompanied by a drop in V_{OC}. The introduction of CST allows for the improvement of both the V_{OC} and J_{SC}. This large improvement in J_{SC} is shown in the EQE plot where the purple device has good response throughout the entire spectrum. This improvement in J_{SC} does not come at a cost to V_{OC} as the other methods for improving J_{SC}. Kephart et al explains in detail of the importance of proper band alignment at the front contact for performance [7]. Thus, introduction of CST as an intermediate layer to pre-alloy the CdSe to CdTe interface improves performance utilizing vapor $CdCl_2$ activation treatments. This improvement of performance suggests the introductions of CST as an intermediate layer to pre-allay the CdSe to CdTe aids in achieving a more optimal band alignment although more research is required to confirm if this is the cause for improved performance.

7 SUMMARY

- **Q 1: What are the optimal optical and electronic properties of commercially available glass/TCO superstrate for CdTe performance?**

  Methodology: Three different commercially available glass/TCO superstates (TEC10, TEC12D, and a proprietary glass/TCO) were chosen for

experimentation. To assess the optical properties of each glass and TCO, the transmission and reflection spectra was measured utilizing a UV-Viz spectrometer. To measure the electronic properties, all effect measurements were taken of prepared TCO samples. Finally, to measure impact on device performance, a fabrication process was optimized to ensure high performing consistent devices for comparison of the different glass/TCO. This process was used to fabricate devices for JV and EQE measurements.

Key Finding: Overall, the proprietary glass/TCO had the highest overall transmission when measured from 400nm – 900nm. This resulted in the devices performance having the highest J_{SC} with an average of ~1mA/cm^2 higher than devices fabricated using TEC10 or TEC12D. Electronic properties varied greatly due to changes in the carrier concentration of each TCO. There was no correlation to these electronic properties and JV device performance. Although, TEC10 had the highest overall carrier concentration as well as the poorest transmission of light above 700nm. This may indicate a higher rate of free carrier absorption of lower energy light. The proprietary substrate maintained the lowest overall carrier concentration as well as the highest transmission of light above 700nm.

- **Hypothesis 1: A n-type window/buffer layer is necessary to mitigate voltage loss**

  Methodology: To verify if an n-type window/buffer is necessary to mitigate voltage loss in CdTe devices an experiment was performed in which MZO was replaced with CdSe while all other parameters of the CSU baseline structure remained constant. Note, a total thickness of 350nm of CdSe and CST was

maintained to mitigate thickness effects. The CdSe thickness varied from 0nm to 125nm to show a contrast of varying CdSe layer thickness to no CdSe.

Key Finding: Devices fabricated with no CdSe (0nm) suffered from the largest voltage loss when compared to MZO based devices. Introduction of CdSe did mitigate voltage loss with devise with CdSe exhibiting better V_{OC}. A positive correlation was shown between V_{OC} and the CdSe thickness. Thus, A n-type window/buffer is necessary to mitigate voltage loss.

- **Hypothesis 2: CdSe window layer thickness is directly correlated to V_{OC} and inversely correlated to J_{SC}.**

  Methodology: To investigate the relationship of CdSe thickness to JV parameters such as V_{OC} and J_{SC} a series of experiments were performed. The remaining CdSe thickness after device processing depends on both the initial CdSe deposition thickness and the $CdCl_2$ activation treatment. Therefore, experiments were designed to explore both parameters, along with literature-supported structures, to provide a comprehensive understanding of the effect of CdSe thickness. NOTE, device structures utilized in the experiments within this section do not utilize any deposited CST.

  Key Finding: Deposited thickness experiment revealed strong positive correlation between CdSe thickness to V_{OC} as well as a strong negative correlation to J_{SC}. Note, J_{SC} remained relatively low even at small thicknesses of CdSe. Following this, experimentation revolved around investigating $CdCl_2$ treatment time versus various CdSe thicknesses. Results from these experiments revealed the same trends between CdSe thickness to V_{OC} and J_{SC} with negative

trends between treatment time (less CdSe) to lower V_{OC} and shorter treatment times to (more CdSe) to higher V_{OC}. In contrast, J_{SC} showed the opposite trend. Due to low overall J_{SC} across all experimentation and experiment was performed to mimic known $CdCl_2$ treatment supported by literature as well as experiments revolving around elevated substrate temperatures. Each trend remained consistent with longer anneal times resulting in lower V_{OC} and higher J_{SC}. Elevated substrate temperature had a more nuanced effect on V_{OC} and J_{SC}. Elevated substrate temperature seemed to slightly increase/maintain V_{OC} while J_{SC} has a positive trend with substrate temperature until above 440C when preheat was included and 460C when preheat was not included. The drop in performance at these high substrate temperatures is most likely due to the elevated substrate temperature preventing adequate $CdCl_2$ diffusion leading to an undertreated device. Elevated substrate temperatures should allow for more Se diffusion and create a thinner CdSe layer after $CdCl_2$ activation treatment. The common trend in V_{OC} was not seen when analysis device that remained under the low performance threshold. Therefore, either the trend remains, and the elevated temperature is allowing for better passivation of the front contact which is compensating for a thinner CdSe layer, or some other factor is driving this trend. Thus, the result of this hypothesis is inconclusive due to inconsistency in the trends of the data. Also note that J_{SC} was improved but remained relatively low. Throughout experimentation J_{SC} did not crest above 25mA/cm^2. Looking at EQE data from these devices consistently shows poor EQE response below 700nm indicating large amounts of parasitic absorption from the CdSe layer. Even when utilizing literature supported

deposited CdSe thickness this issue remained, suggesting the vapor $CdCl_2$ process used may be unsuitable for processing CdSe/CdTe devices and/or the sublimation of CdSe creates a suboptimal films for processing PV devices.

- **Hypothesis 3: Introduction of CST ternary alloy aids in modulating Se diffusion for a more suitable band alignment**

  Methodology: Due to low overall J_{SC} and poor EQE response of CdSe/CdTe devices, CST was reintroduced into the device structure to investigate the effects of modulating Se diffusion when combined with the vapor $CdCl_2$ activation process.

  Key Finding: Reintroduction of CST into the device structure immediately allowed for improved J_{SC} from ~23mA/cm^2 to ~27.5mA/cm^2. The following experiment showed even between performance with higher V_{OC} and higher J_{SC} than what was achieved without deposit CST. The EQE spectra of these devices is a good flat EQE curve that is comparable to the MZO based devices and shows little to no parasitic absorption from the CdSe layer. When analyzing comparative plots of JV curves the contrast can be seen from excess CdSe resulting in higher V_{OC} and low J_{SC}. To better $CdCl_2$ treatments allowing for higher J_{SC} at the cost of some V_{OC}. To the reintroduction of CST allowing for both high V_{OC} as well as good J_{SC}. The comparative EQE curves also represent this trend and show large amounts of parasitic absorption until the reintroduction of CST allowed for a good EQE response across the entire spectrum. The drastic improvement in performance enforces the hypothesis that the reintroduction of CST aids in modulating the Se diffusion and suggests a better band alignment has been

achieved. Although more research is required to confirm the reason for improvement.

8 FUTURE WORK

The purpose of this research was to better understand how different process parameters of the front contact affect CdTe devices and to investigate an alternative structure that uses CdSe. Although these experiments revealed important trends between the fabrication process and device performance, as well as methods to improve performance, there is still significant work needed to further advance this research. Based upon the learning of this research, here are some suggestions for future research.

- Ebin et al. has shown good devise performing utilizing almost identical device structures of 120nm CdSe and 3.5micron CdTe devices fabricated here at CSU. The fabrication process at CSU differs from Ebin et al. in two important ways. They use thermal evaporation for the CdSe and CdTe deposition and they utilize a solution based $CdCl_2$ treatment [21]. Due to the challenge in matching performance using sublimation as well as vapor $CdCl_2$ processing further research should be performed focusing on the effect of differing deposition conditions/methods have on the CdSe film. In conjunction with this research and due to the inconsistent trend shown when elevating substrate temperature during $CdCl_2$ activation treatments, further experimentation should be performed. Research should focus on the interplay between the CdSe films attributes and

$CdCl_2$ treatments to connect how and why certain processing conditions are more advantageous.

- Further investigation into the varied thickness of CST could show further improvement to device performance. A CST thickness of 300nm was shown to greatly improve device performance within this research and further optimization of this layer may reveal improved performance of CdSe based devices.
- Further analysis of the pre-alloyed device structure using cross-sectional EBSD and TEM imaging would provide valuable insight into how process conditions influence device structure. This research primarily relied on device performance to infer structural characteristics and to understand why performance gains occur with the reintroduction of CST. Employing more advanced imaging and spectroscopic techniques could reveal structural features that enable improved performance, as well as those that hinder it. For example, electron energy-loss spectroscopy (EELS) could be used for bandgap mapping of TEM samples. When combined with modeling of the band structure in CdSe-based devices, these analyses would significantly aid in designing device architectures and optimizing layer thicknesses. Such insights would better guide the development of CdSe-based devices to further enhance performance. A similar analysis was performed here [22].
- Ebin et al. has also connected interesting effects of differing Cu treatments and its effect on CdSe based devise. The literature reported improvements in current collection and EQE response through only changing the substrate temperature during the copper doping process [21]. The back contact remained consistent

throughout almost all this research. The process used is suited for MZO based devices. Research into differing dopo process as well as back contacts may reveal the back contact utilized within this research was suboptimal.

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