THESIS

APPLICATION OF DISTRIBUTED DC/DC ELECTRONICS IN PHOTOVOLTAIC SYSTEMS

Submitted by

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ABSTRACT

APPLICATION OF DISTRIBUTED DC/DC ELECTRONICS IN PHOTOVOLTAIC SYSTEMS

In a typical residential, commercial or utility grade photovoltaic (PV) system, PV modules are connected in series and in parallel to form an array that is connected to a standard DC/AC inverter, which is then connected directly to the grid. This type of standard installation; however, does very little to maximize the energy output of the solar array if certain conditions exist. These conditions could include age, temperature, irradiance and other factors that can cause mismatch between PV modules in an array that severely cripple the output power of the system.

Since PV modules are typically connected in series to form a string, the output of the entire string is limited by the efficiency of the weakest module. With PV module efficiencies already relatively low, it is critical to extract the maximum power out of each module in order to make solar energy an economically viable competitor to oil and gas.

Module level DC/DC electronics with maximum power point (MPP) tracking solves this issue by decoupling each module from the string in order for the module to operate independently of the geometry and complexity of the surrounding system. This allows each PV module to work at its maximum power point by transferring the maximum power the module is able to deliver directly to the load by either boosting (stepping up) the voltage or bucking (stepping down) the voltage.

The goal of this thesis is to discuss the development of a per-module DC/DC converter in order to maximize the energy output of a PV module and reduce the overall cost of the system by increasing the energy harvest.

ACKNOWLEDGEMENTS

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To my family and friends. You all know how important this master's degree is to me. Without your encouragement, I never would have finished.

DEDICATION

For my family and friends

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CHAPTER 1. INTRODUCTION

1.1 Introduction to PV Energy

With rising world-wide energy demands, soaring prices of fossil fuels, limited reserves of our primary sources of energy, the threat of nuclear accidents and the unpredictable international political situation, interest in renewable energy sources has increased exponentially over the last few decades. This is even truer with the appearance of a new world problem, which is the reheating of the planet due to increasing concentrations of greenhouse gasses in our atmosphere such as carbon dioxide (CO_2) and methane [1]. Among all the renewable energy sources, solar/photovoltaic (PV) energy has seen the most growth over the years resulting in decreased prices of PV modules as production capacity increases at a fast pace [2]. The solar industry is the fastest growing segment in the alternative energy sector. For more than two decades, worldwide growth of photovoltaics has been fitting an exponential curve with no signs of slowing down. Forecast shows an annual installation to increase from 40.0 GW to 135.0 GW and global cumulative capacity to reach almost 700.0 GW by 2020 [3]. The driving force behind this increase include proliferating consumer demands, environmental consciousness, new federal and state subsidies/mandates and new government R&D programs [4].

Specifically, there has been a lot of research into driving the cost of PV modules down as well as finding technology to make the PV system smarter and more efficient to bring the levelized cost of electricity (LCOE) down to grid parity. One way of doing this would be to integrate power electronics directly into the system. Currently there are more than 30 countries where solar energy has reached grid parity with conventional energy [5] and with power electronics integrated into the system this number will continue to increase.

Yet, even if solar was the most cost effective alternative energy solution. The costliest per-watt expenditure in a photovoltaic system arises in power generation [6]. This is true due to the fact that harnessing solar energy and the amount of power that is generated is nonlinear and depends on the change in solar irradiance, ambient temperature, mismatch in the system as well as many other factors [2, 7]. These factors are constantly changing throughout the day and in turn can severely affect the efficiency and output power of the PV modules. Since PV modules are relatively inefficient to begin with, crystalline silicon comprising of 90.0 % of the global market has a theoretical maximum efficiency of only 33.7 % [8, 9]. Any fluctuation in efficiency can lower the amount of energy being generated significantly. Therefore, due to these characteristics, much attention has been given to the development of power electronics that extract the maximum power of the PV module thus increasing the efficiency of the power processing stage, improving the power yield and enabling cost reduction of the overall system that interfaces to the grid [2].

This thesis will examine the benefits and challenges of the PV system as it exists today and will study the developing technology of DC/DC converters that allow the PV system to operate with autonomous control for tracking the maximum power point of PV modules thus utilizing the module to its fullest capability [4].

1.2 Organization of Thesis

Chapter 1 of this thesis introduces the need for PV energy in today's world and the issues that currently plague the solar industry. It also introduces the concept of DC/DC converters and power electronics in use with photovoltaic systems.

Chapter 2 gives an overview of the operation of PV modules and how they behave in a system. In addition, it will introduce how module level electronics can benefit a PV system.

Chapter 3 introduces different DC/DC converter topologies that exist and examines the advantages and disadvantages of using certain converter topologies. This chapter will also introduce the basic math to calculate the critical components (inductor, capacitor and MOSFETs) used in each DC/DC converter.

Chapter 4 examines, in detail, the chosen boost-buck converter design and its associated components that will be used to optimize the energy output of the PV module. This chapter will also describe the losses associated with the converter as well as additional functions and features that will help the PV system.

Chapter 5 presents the results of testing the boost-buck converter. This chapter will show the simulated results using software and then the actual results based on a real working design.

Chapter 6 summarizes the current work and speculates on future work on this topic.

CHAPTER 2. ANALYSIS OF DC/DC CONVERTER TOPOLOGIES

2.1 Introduction

2.1.1 PV Cells and Modules

Solar cells, also known as PV cells, are the building blocks of a PV module. A PV cell is a p-n semiconductor junction fabricated in a thin wafer or layer of semiconductor (usually silicon). In the dark, the I-V output characteristic of a PV cell has an exponential characteristic like that of a diode [10]. When exposed to light, a DC current is generated which varies proportionally to the incident radiation [11]. When solar energy (photons) hits the PV cell, with energy greater than the band gap energy of the semiconductor, electrons are knocked loose from the atoms in the material creating an electron-hole pair. These carriers are swept apart under the influence of the internal electric fields of the p-n junction and create a current proportional to the incident radiation. When the PV cell is short circuited, this current flows in the external circuit, when open circuited, this current is shunted internally by the intrinsic p-n junction diode. The characteristics of this diode therefore set the open circuit voltage characteristics of the cell [10]. The simplest circuit model of an ideal PV cell is a current source in parallel with a diode, shown in Figure 1, where the output current is directly proportional to the light falling on the cell. During darkness, the PV cell is not an active device; it works as a diode (p-n junction). It produces neither a current nor a voltage. However, if it is connected to an external supply with a relatively large voltage, it generates a current called diode current or dark current. Therefore, the diode determines the I-V characteristics of the cell [10]. However, since an ideal cell does not exist, a shunt resistance and series resistance component are added to the model.

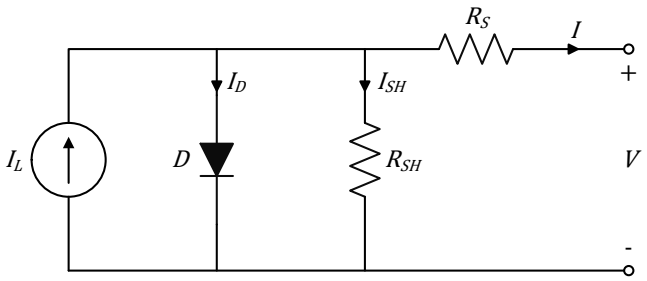

Figure 1: Equivalent Circuit of a PV Cell

The basic equation that describe the (I-V) characteristics of the PV cell is given by:

$$I = I_L - I_o\left(e^{\frac{q(V+IR_s)}{kT}} - 1\right) - \left(\frac{V + IR_s}{R_{sh}}\right)$$

Where:

$I = \ PV\ cell\ output\ current\ (A)$

$I_L = Light\ generated\ current\ (A)$

$I_o = Diode\ reverse\ saturation\ current\ (A)$

$q = Charge\ of\ electron\ (1.602x10^{-19}\ \mathrm{C})$

$k = Boltzmann\ constant\ (1.38x10^{-23}\ J/K)$

$T = PV\ cell\ temperature\ (K)$

$R_s = PV\ cell\ series\ resistance$

$R_{sh} = PV\ cell\ shunt\ resistance$

$V = PV\ cell\ output\ voltage$

$n = Diode\ ideality\ factor\ (1\ for\ ideal\ diode)$

In a typical PV cell, the open circuit voltage is measured to be anywhere between 0.5 V to 0.6 V (0.58 V typically) no matter how large they are [12]. The cell voltage remains constant as long as there is sufficient irradiance falling upon it. Open circuit voltage means the PV cell is not connected to any external load and therefore not producing any current flow. When connected to an external load the output voltage of the individual cell drops to around 0.46 V to

0.52 V as electrical current begins to flow and will remain around this voltage level regardless of the suns intensity (temperature also affects this voltage).

Unlike a PV cells voltage, the output DC current does vary in direct relationship to the amount or intensity of the sunlight falling onto the face of the PV cell. Also, the output current is directly proportional to the cells surface area as the larger the cell, the more light energy enters the cell. PV cells with higher current outputs are generally more desirable but the higher the current output the more they will cost.

Most typical PV cells found in residential, commercial and industrial applications fall within a (12.5 cm x 12.5 cm) or (15.6 cm x 15.6 cm) area. Given the typical short circuit current density of a crystalline silicon solar cell is 35.0 mA/cm^2 (42.0 mA/cm^2 lab and 46.0 mA/cm^2 theoretical) [13] this would make the short circuit current of a PV cell to be 5.4688 A and 8.5176 A respectively.

$$I = (12.5\ cm * 12.5\ cm) * 0.035\ A/cm^2 \quad \Rightarrow \quad 5.4688\ A$$

$$I = (15.6\ cm * 15.6\ cm) * 0.035\ A/cm^2 \quad \Rightarrow \quad 8.5176\ A$$

Using this information and assigning values to the PV cell equation, an I-V and power curve can be generated using the Matlab code found in Appendix A to show the characteristics of a typical (12.5 cm x 12.5 cm) PV cell shown in Figure 2.

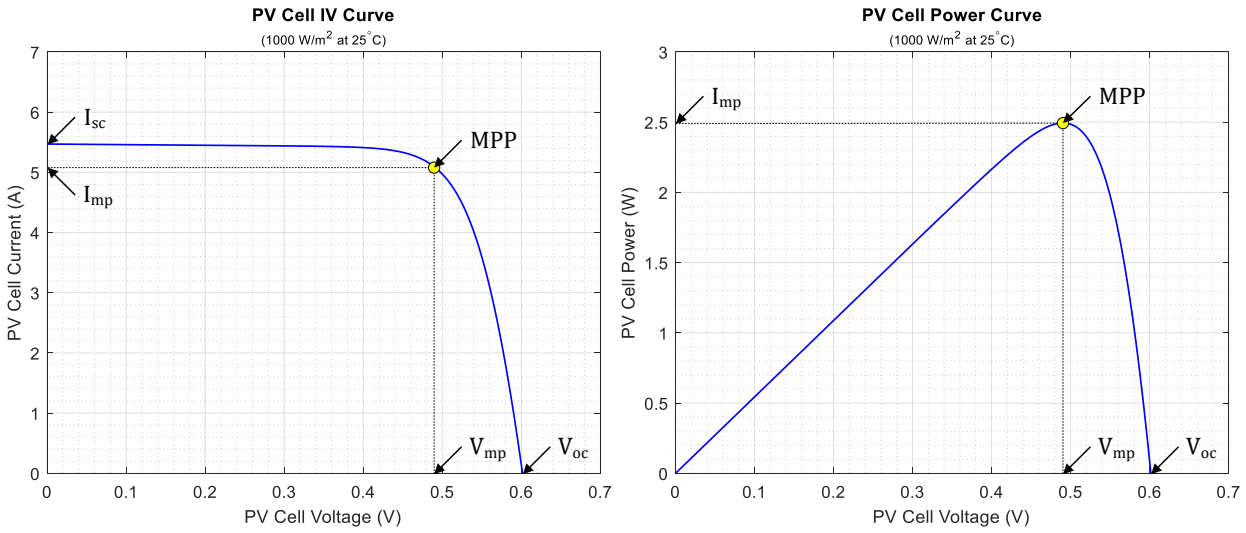

Figure 2: PV Cell I-V and Power Curve for a Typical (12.5 cm x 12.5 cm) Cell

From the PV cell equation and the plots generated in Figure 2, values for the characteristics of a PV cell can be calculated for both types of cell sizes shown in Table 1, which will be used as a basis of all the calculations used throughout this paper.

Table 1: Simulated Values for Typical PV Cells

Cell Type	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
12.5 cm x 12.5 cm	0.6021	0.4902	5.0860	5.4688	2.5023
15.6 cm x 15.6 cm	0.6158	0.4908	7.9299	8.5176	3.8920

There are 4 parameters that define a PV cell (short circuit current, open circuit voltage, maximum power point and the fill factor).

- The open circuit voltage (V_{oc}) is the maximum voltage available from the solar cell when the generated current is zero. The open circuit voltage corresponds to the amount of light forward bias on the solar cell due to the bias of the solar cell junction with the light generated current [14].

- The short circuit current (I_{sc}) is the greatest value of current generated by a cell when the voltage across the solar cell is zero. It is the greatest value of the current generated by a cell [13].
- The maximum power point (MPP) is the operating point at which the power dissipated in the resistive load is at a maximum. It is equal to the product of V_{mp} and I_{mp} [15].
- The fill factor (FF) is the ratio of the maximum power that can be delivered to the load and is equal to the product of the V_{oc} and I_{sc}. The fill factor is a measure of the real I-V characteristic of the cell. Its value is higher than 0.7 for good cells. The fill factor diminishes as the cell temperature increases [15].

The output power of a PV cell is given in watts and is equal to the product of the voltage and current. Alone, a PV cell does not have enough power to do much work given that each cell contributes a fraction of a volt. Normally a small solar cell (a few square inches in size) generates about one watt [7]. This is not a lot of power considering a typical light bulb uses anywhere from 40.0 to 100.0 watts of power. Individual cells can be connected in series to achieve the desired voltage and can be connected in parallel to achieve a desired current. Any combination of two or more PV cells in series or in parallel is called a PV module. The PV cells within the module can be connected to give a desired voltage, current and power output creating modules with power outputs of 50.0 to 400.0 watts or more, which is enough power to do some serious work. Figure 3 shows a representation of a 96-cell PV module where 96-cells are connected in series to produce a module with the output power capability of 230.0 W.

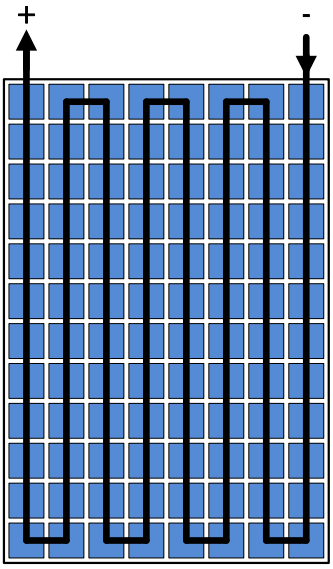

Figure 3: 96-Cell PV Module

By adding more PV cells in series, it will increase the output voltage of the module with the current remaining the same. The result of stringing the cells in series is an I-V characteristic of the module shown in Figure 4. Figure 4 models the output voltage and current of the PV module (96-cells) over the entire load range from short to open circuit at standard test conditions (STC) of 25.0 °C and 1000.0 W/m^2.

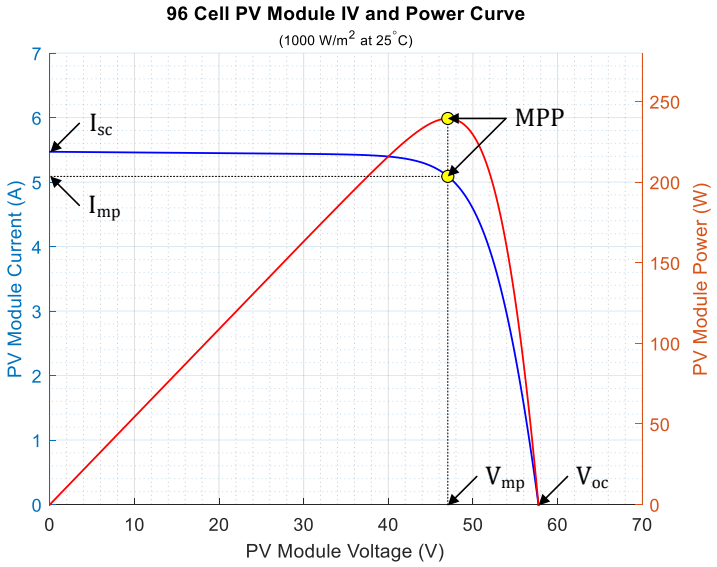

Figure 4: Output Characteristics of a 96-Cell PV Module

The way these PV cells are connected in series brings many complications. When cells are put in series, they are all constrained to conduct the same current. However, it is extremely hard to manufacture cells that are exactly alike so the cells are mismatched with one another. When mismatched cells are put in series the string current will be dictated by the least efficient cell and the overall efficiency of the module is then reduced to the efficiency of this one cell [16]. In addition to cell mismatch, temperature and irradiance play a role in the amount of power a module can produce. The current that a PV module can generate is directly correlated to the amount of sunlight. Figure 5 shows how at different irradiance the current of the module drops due to cloud cover. This figure looks the same on the cell level where once again the current generated by the module is dictated by the lowest producing cell.

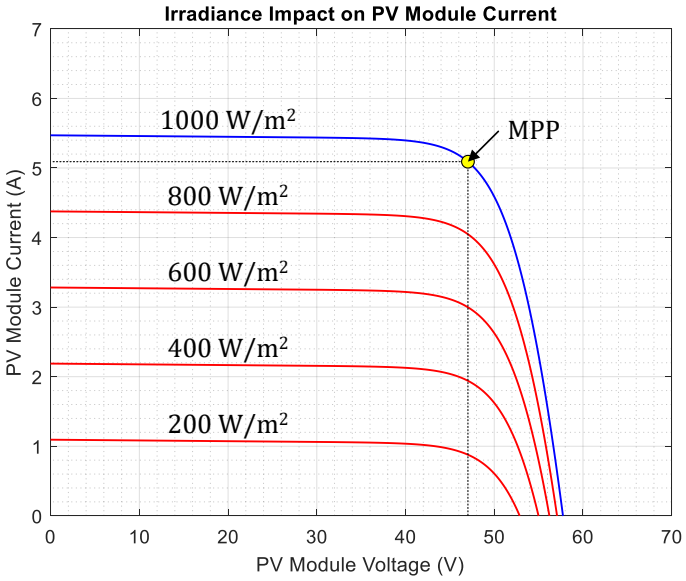

Figure 5: Irradiance Impact on PV Module Current

Likewise, the amount of voltage a PV module can produce is inversely related to the temperature of the PV module. That is, when the PV module temperature increases, the voltage decrease lowering the overall output power of the module as seen in Figure 6.

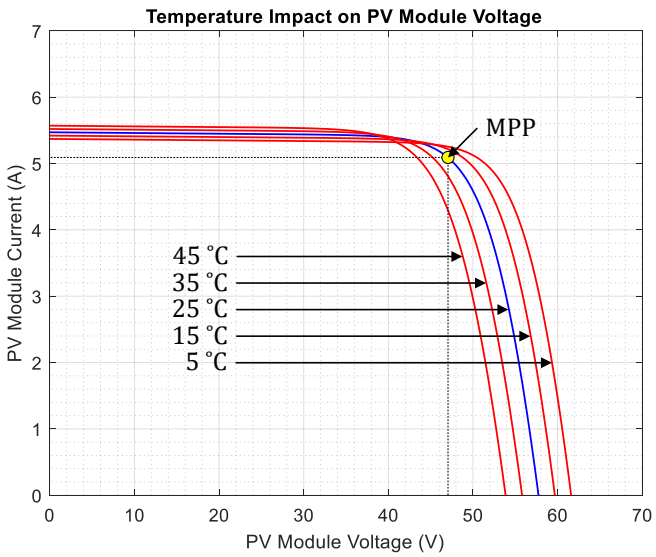

Figure 6: Temperature Impact on PV Module Current

From Figure 5 and Figure 6, it can be seen that the open circuit voltage increases logarithmically with the ambient irradiation, while the short circuit current is a linear function of the ambient irradiation. The dominant effect with increasing cells temperature is the linear decrease of the open circuit voltage, which results in the cell being less efficient. The short circuit current slightly increases with cell temperature [15].

2.1.2 Building a PV Array

Much like the way PV cells are connected in parallel or series, PV modules are connected in the same manner to create PV arrays or strings. These strings can increase the power being sent to the inverter. The modules can be tied together in series to increase the voltage or in parallel to increase the current to provide power to lower power applications or to power residential, commercial or industrial loads. Much like PV cells connected in series, the current is dictated by the weakest module and the efficiency of the entire string in an array is reduced to the efficiency of this one module. This is due to the serial nature of the PV modules in a string which

creates a “Christmas tree effect” where current reduction in one series connected module causes mismatch losses in the rest of the string [17]. As mentioned earlier, mismatch is caused by temperature, irradiance, shading, soiling and physical degradation over time [17]. Studies have revealed that even minor shading on one cell can cause major reduction in solar power output of the photovoltaic array crippling a PV system. In fact, even small amounts of shade could drop the photocurrent generated in a cell by 20.0 % [16] and even small amounts of shade can reduce the power of the module up to 50.0 %. Take for example a conventional string of PV modules in an array shown in Figure 7.

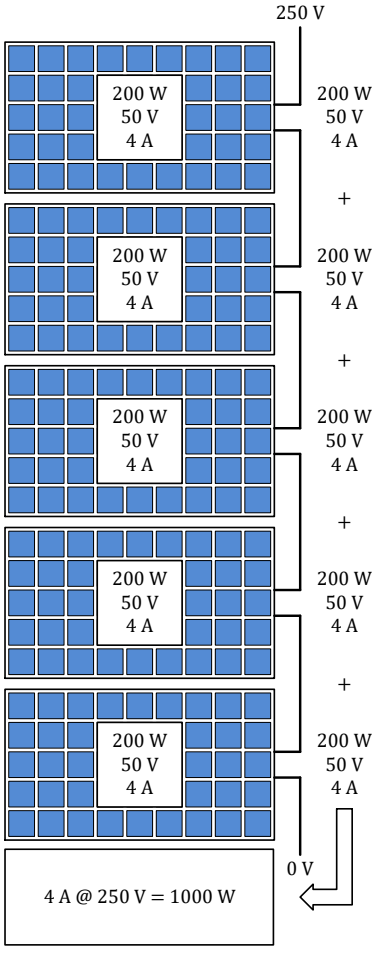

Figure 7: Conventional PV String

Figure 7 shows a conventional string of modules with made-up values for the voltage and current to make the calculations easier. The output capability of the four modules on top is 200.0 W at 50.0 V and 4.0 A. Now consider the bottom PV module is not working properly. Perhaps this module is shaded so it is subjected to less irradiance. Its maximum output power capability is only ($50.0\ V * 3.0\ A = 150.0\ W$). Although the four modules have the capability to deliver 4.0 A of current, they are limited by the laws of physics to only deliver 3.0 A because that is the weakest module in the string. Therefore, the series string output is limited to 750.0 W of power (Figure 8).

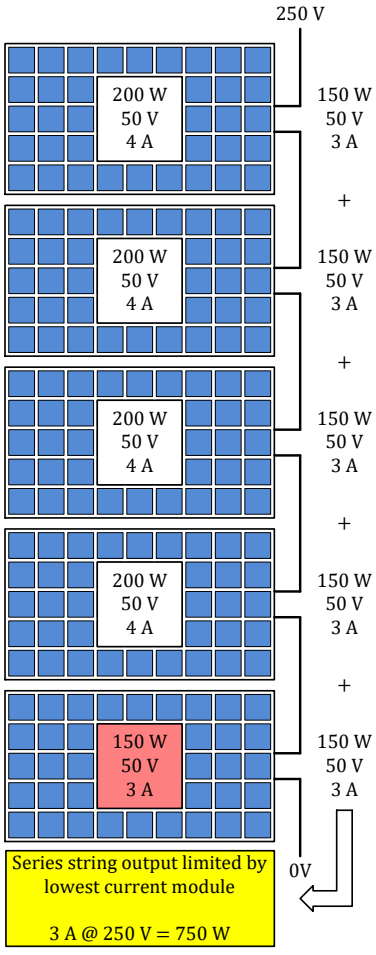

Figure 8: Conventional PV String with Limited Output

Looking at the output power curve of these PV modules shown in Figure 9, the four modules on top can deliver 4.0 A and want to operate at a higher level of power (blue curve), but their power is limited by the bottom module which is the weakest (red curve). All the modules will be operating at this level (red curve) indefinitely, until the conditions change, and the total system is now at a 150.0 W loss in total power.

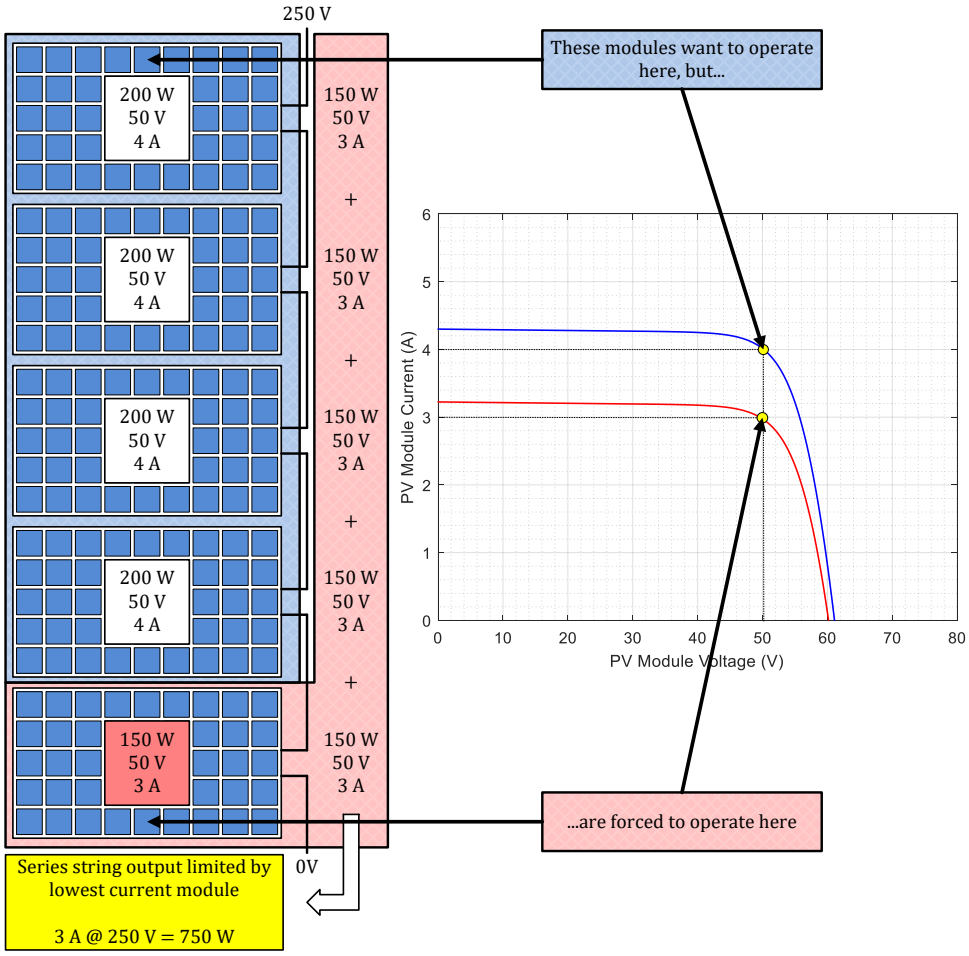

Figure 9: Conventional PV String with I-V Curves

2.1.3 Module Level Electronics

Under conventional installations, the performance of all PV modules in Figure 9 are stuck operating at this lower power level. Keeping a system this way can lose a substantial amount of

energy due to mismatch of each module tied in a string. One very effective solution to solve this issue is with the use of a maximum power point tracker (MPPT). A maximum power point tracker is a power electronic DC/DC converter inserted in between the PV module and its load to achieve optimum matching by using an intelligent algorithm which ensures the PV module will always operate at its maximum power point as the temperature, insolation and load vary [11]. A traditional central inverter will have a few input channels that independently track the maximum power point of the PV system. With large utility scale inverters going up to megawatts in size, over 5000 PV modules are connected and could potentially operate at one common peak power point. Nevertheless, a reduction in output power of one or more of these PV modules can lead to mismatch in the maximum power point between the various PV modules and strings [17]. Placing dedicated DC/DC converters on each module would de-couple the maximum power operating point of the individual modules or string from the overall maximum power point of the system [17]. This allows each converter to track the maximum power point of the solar module connected to it and either increase (boost) or decrease (buck) the output voltage to match the optimum voltage requested by the central inverter [17]. Essentially this turns the PV module into a power supply where, by varying the output voltage and current a constant power can always be achieved at MPP. It was mentioned previously that a conventional PV string has many issues associated with it as seen in Figure 9. Under conventional installation the performance of all PV modules in a string are stuck operating at a low level (red curve). Now, with DC/DC electronics with MPPT control attached to each module, the modules are converted from a current source into a power source meaning the PV modules will always deliver their maximum power.

Mathematically speaking, under a conventional installation, the amount of power a string can deliver is given by the voltage induced across the string by the inverter (250.0 V in this case) and the current flowing through that string (3.0 A). In other words:

$$V_{inverter} * I_{string} = P_{string}$$

$$(250.0\ V * 3.0\ A) = 750.0\ W$$

However, with a module level DC/DC converter, the power delivered by the string is always the maximum. So, the string current is given by the maximum power divided by the voltage induce by the inverter.

$$\frac{P_{maximum}}{V_{inverter}} = I_{string}$$

$$\frac{950.0\ W}{250.0\ V} = 3.8\ A$$

To understand how the output curves of the PV modules are affected by DC/DC converters understanding of the current and voltage curves for constant power must be examined.

If there is a device that delivers a constant 100.0 W regardless of the load, then this device will change its voltage and current so that 100.0 W of power is always delivered. Figure 10 shows combinations of voltages and currents that create 100.0 W of power and the associated curve.

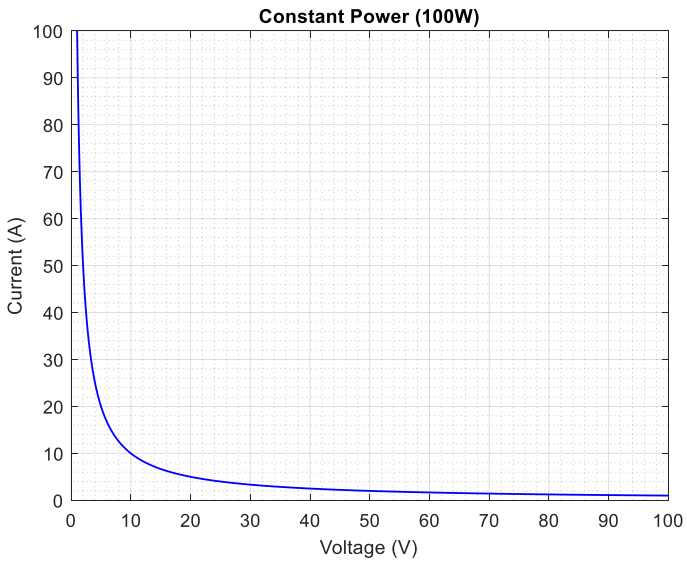

Figure 10: 100.0 W Constant Power Curve

If the device is operating at 10.0 V and 10.0 A (100.0 W) and a situation happens where the device is only able to deliver 4.0 A of current. The device will increase its voltage from 10.0 V to 25.0 V so it still delivers ($25.0\ V * 4.0\ A = 100.0\ W$). When the output voltage is increased above the input voltage to maintain a given power level this is referred to as boosting the voltage.

Likewise, if the device is operating at 10.0 V and 10.0 A (100.0 W) but this time something happens where the device must suddenly deliver 25.0 A of current. The device will decrease its voltage from 10.0 V to 4.0 V so it continues to deliver a constant ($4.0\ V * 25.0\ A = 100.0\ W$). When the output voltage is decreased below the input voltage to maintain a given power level this is referred to as bucking the voltage. Both boosting and bucking scenarios of a constant power curve can be seen in Figure 11.

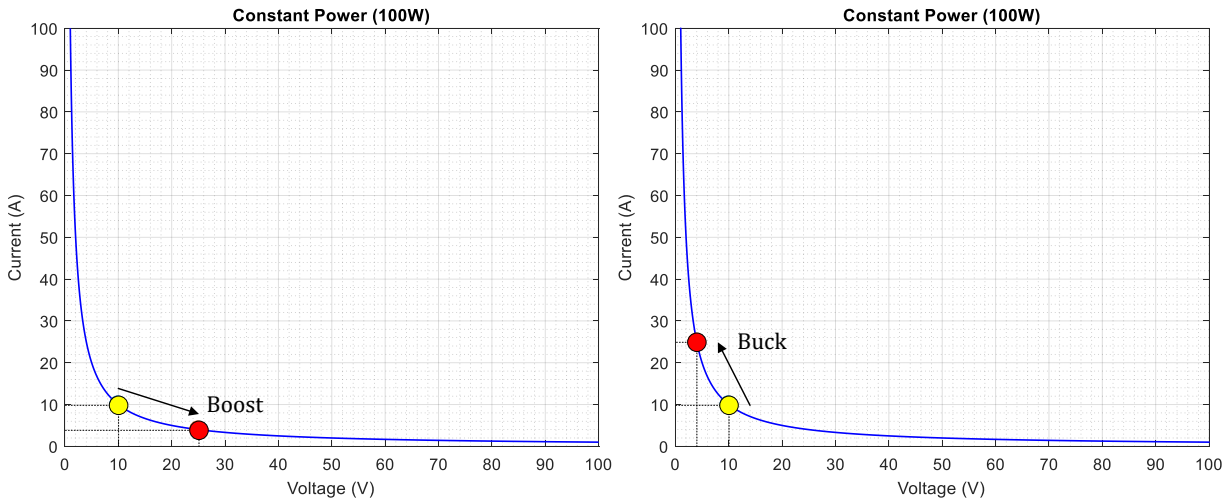

Figure 11: 100.0 W Constant Power Curve with Boosting and Bucking

Recall the operating curves under a conventional installation in Figure 9 and how the power output for the string is limited by the weakest module in the string. DC/DC converters allow the PV module to operate like a constant power device described earlier. The converters find and deliver the maximum power point for each PV module and vary its output voltage and current to deliver the constant power needed by the load. Figure 12 illustrates how the voltage is boosted or bucked so the current is the same across the string and maximum power is delivered from each PV module.

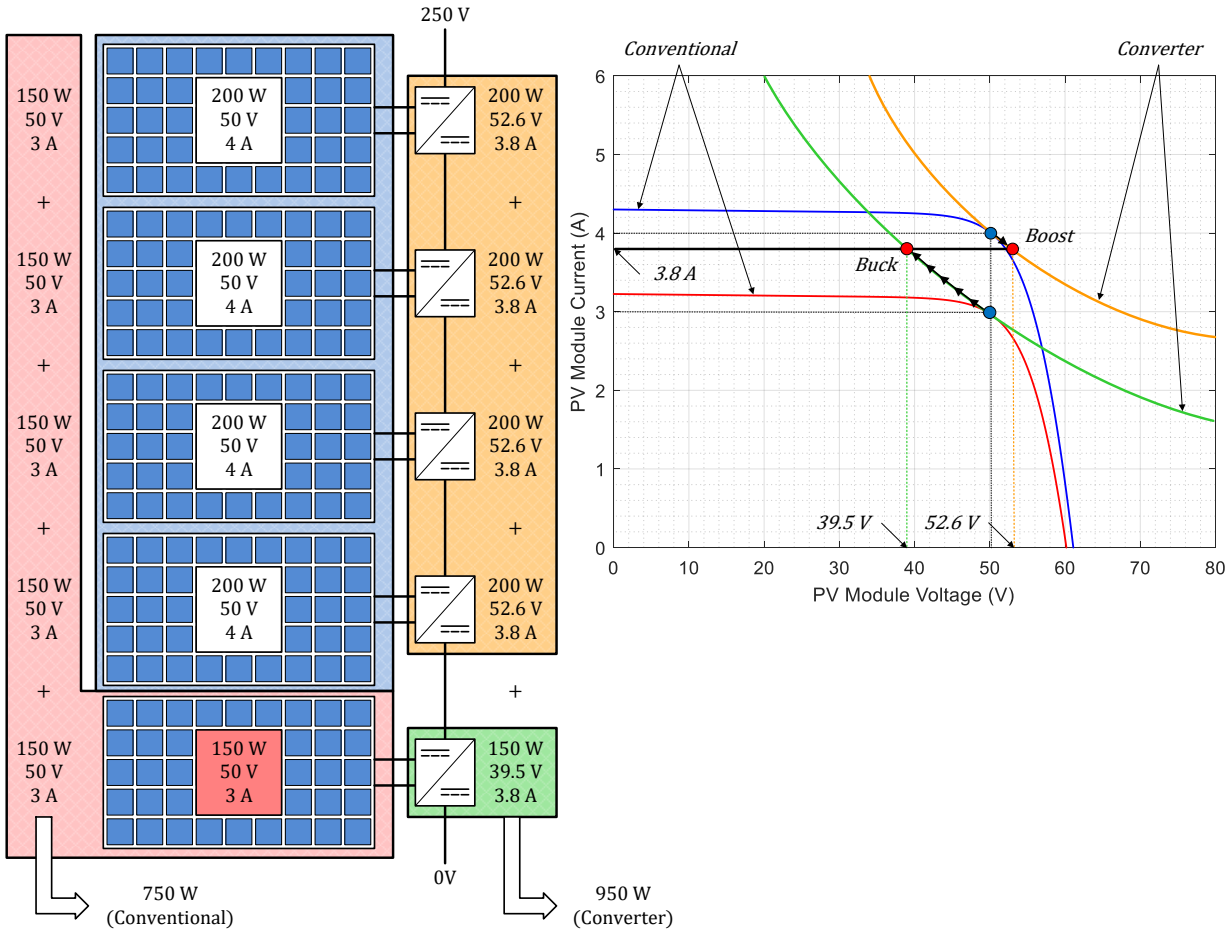

Figure 12: String with DC/DC Converter

The voltage of the weakest module (red curve) will buck its voltage along the green line increasing its current output while at the same time the voltage of the other modules (blue curve) will boost their voltage along the orange line decreasing its current until an equilibrium is met. Now the bottom module is producing 150.0 W at 39.5 V and 3.8 A while the top four modules are producing 200.0 W at 52.6 V and 3.8 A. Instead of the string producing 750.0 W of power to the load with a conventional PV system (Figure 8), the whole system is now producing 950.0 W where the only loss of power is due to the shading on the bottom PV module totaling 50.0 W.

CHAPTER 3. DC/DC CONVERTER TOPOLOGIES

3.1 Introduction

DC/DC converters at a module level can convert each module from a current source into a power source thus allowing each module to deliver its maximum power to the load despite any mismatches in the system. There are several topologies and algorithms available to achieve this. For the sake of this paper, the most common topologies available will be analyzed to understand each advantage and disadvantage and how it applies to the system. The three most common topologies are buck (step down), boost (step up) and buck-boost (step down/step up).

3.2 Converter Topologies

3.2.1 Buck Converter

In a buck converter, the output voltage must always be lower than the input voltage [18]. A simple buck converter circuit is shown in Figure 13 consisting of a MOSFET, diode, inductor, capacitor and a load. While the MOSFET is on, current is flowing through the load via the inductor. The action of any inductor opposes changes in current flow and also acts as a store of energy. In this case, the MOSFET output is prevented from increasing immediately to its peak value as the inductor stores energy taken from the increasing output. This stored energy is later released back into the circuit as a back-electromotive force (back-EMF) as current from the switching MOSFET is rapidly turned off [18].

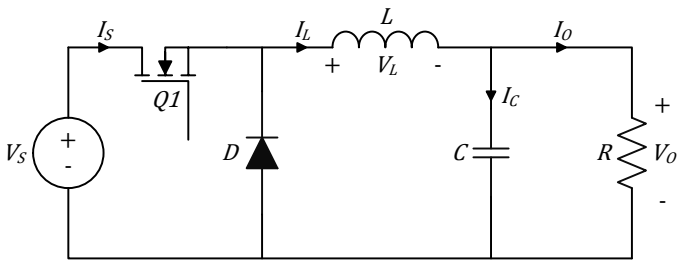

Figure 13: Conventional Buck Converter

There are two modes in which this converter can operate. The first mode is when the MOSFET is in position 1 (on state) and the second mode is when the switch is in position 2 (off state).

In the on state, shown in the circuit in Figure 14, the MOSFET is supplying the load with current. Initially, current flow to the load is restricted as energy is also being stored in the inductor. Therefore, the current in the load and the charge on the capacitor builds up gradually. During this on state, there is a large positive voltage on the diode so the diode will be reverse biased and play no role in the circuit. The voltage across the inductor and current through the capacitor is represented by the following equations:

$$V_L = V_s - V_o$$

$$I_c = I_L - \frac{V_o}{R}$$

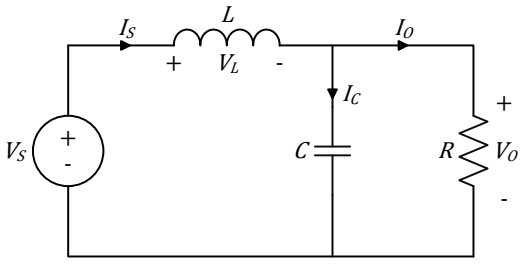

Figure 14: Buck Converter (On State)

During the on state, the current through the inductor rises linearly given by:

$$V_L = L\left(\frac{dI_L}{dt}\right)$$

$$\left(\frac{dI_L}{dt}\right) = \frac{V_L}{L} \Rightarrow \left(\frac{V_s - V_o}{L}\right)$$

$$\Delta I_{L(on)} = \int_0^{t_{on}} \frac{V_L}{L} dt \Rightarrow \left(\frac{V_s - V_o}{L}\right) t_{on} \; where \; t_{on} = DT$$

$$\Delta I_{L(on)} = \left(\frac{V_s - V_o}{L}\right) DT$$

The voltage across the capacitor is given by:

$$I_c = C\left(\frac{dV_o}{dt}\right)$$

$$\left(\frac{dV_o}{dt}\right) = \frac{I_c}{C} \Rightarrow \left(\frac{I_L - \frac{V_o}{R}}{C}\right)$$

$$\Delta V_{c(on)} = \int_0^{t_{on}} \frac{I_c}{C} dt \Rightarrow \left(\frac{I_L - \frac{V_o}{R}}{C}\right) t_{on} \; where \; t_{on} = DT$$

$$\Delta V_{c(on)} = \left(\frac{I_L - I_o}{C}\right) DT$$

During the off state, shown in Figure 15, the energy stored in the magnetic field around the inductor is released back into the circuit. The voltage across the inductor is not in reverse polarity to the voltage across the inductor during the on period, and sufficient stored energy is available in the collapsing magnetic field to keep current flowing for at least part of the time the transistor switch is open. The back-EMF from the inductor now causes the current to flow around the circuit via the load and the diode, which is now forward biased. Once the inductor has returned a large part of its stored energy to the circuit and the load voltage begins to fall, the charge stored in the capacitor becomes the main source of current, keeping current flowing

through the load until the next on period begins. The current across the inductor and current through the capacitor is represented by the equations:

$$V_L = -V_o$$

$$I_c = I_L - \frac{V_o}{R}$$

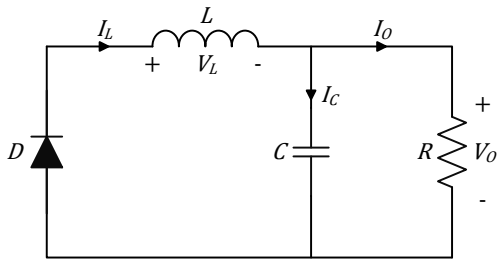

Figure 15: Buck Converter (Off State)

During the off state, the current through the inductor is given by:

$$V_L = L\left(\frac{dI_L}{dt}\right)$$

$$\left(\frac{dI_L}{dt}\right) = \frac{V_L}{L} \Rightarrow \left(\frac{-V_o}{L}\right)$$

$$\Delta I_{L(off)} = \int_{t_{on}}^{T=t_{on}+t_{off}} \frac{V_L}{L} dt \Rightarrow \left(\frac{-V_o}{L}\right) t_{off} \; where \; t_{off} = (1-D)T$$

$$\Delta I_{L(off)} = \left(\frac{-V_o}{L}\right)(1-D)T$$

The voltage across the capacitor is given by:

$$I_c = C\left(\frac{dV_o}{dt}\right)$$

$$\left(\frac{dV_o}{dt}\right) = \frac{I_c}{C} \Rightarrow \left(\frac{I_L - \frac{V_o}{R}}{C}\right)$$

$$\Delta V_{c(off)} = \int_{t_{on}}^{T=t_{on}+t_{off}} \frac{I_c}{C} dt \Rightarrow \left(\frac{I_L - \frac{V_o}{R}}{C}\right) t_{off} \; where \; t_{off} = (1-D)T$$

$$\Delta V_{c(off)} = \left(\frac{I_L - I_o}{C}\right)(1-D)T$$

From the steady state perspective, magnitude of the inductor current increment during switch on is equal to the inductor current decrement during switch off. In other words, the net change in inductor current or the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state. Therefore, the output voltage is directly dependent on the duty cycle and the input voltage.

$$\Delta I_{L(on)} + \Delta I_{L(off)} = 0$$

$$\left(\frac{V_s - V_o}{L}\right)DT - \left(\frac{-V_o}{L}\right)(1-D)T = 0$$

$$(V_s - V_o)DT - (-V_o)(1-D)T = 0$$

$$V_o - DV_s = 0$$

$$V_o = DV_s$$

Likewise, from the steady state perspective, magnitude of the capacitor voltage increment during switch on is equal to the capacitor voltage decrement during switch off. In other words, the net change in capacitor voltage or the total area (or charge balance) under the capacitor current waveform is zero whenever the converter operates in steady state. Therefore, the output current is directly dependent on the input current.

$$\Delta V_{c(on)} + \Delta V_{c(off)} = 0$$

$$\left(\frac{I_L - I_o}{C}\right)DT - \left(\frac{I_L - I_o}{C}\right)(1-D)T = 0$$

$$(I_L - I_o)DT - (I_L - I_o)(1-D)T = 0$$

$$I_L - I_o = 0$$

$$I_L = I_o$$

The output waveforms of the voltage and current during one cycle period are shown in Figure 16.

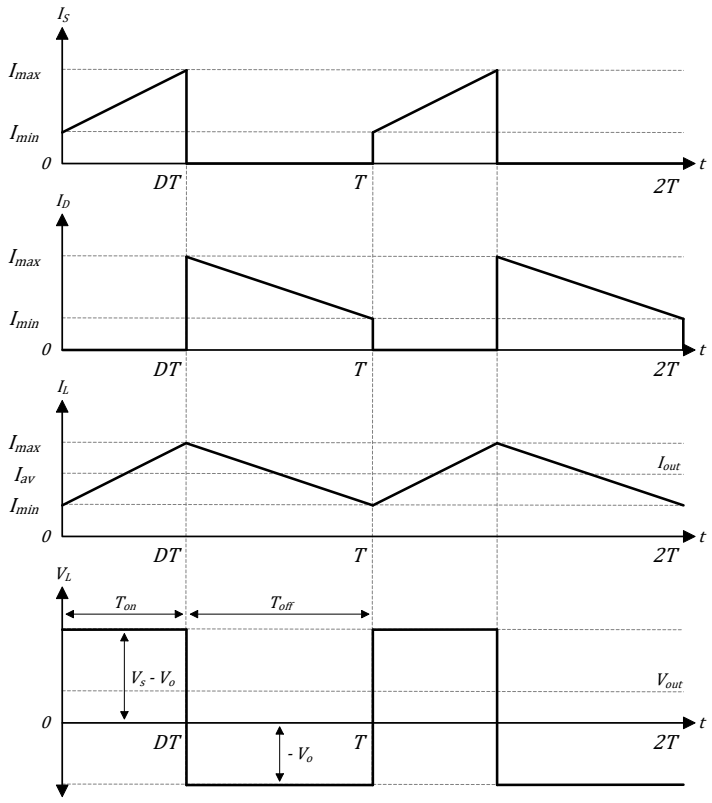

Figure 16: Buck Converter Voltage and Current Waveforms

3.2.2 Boost Converter

In a boost converter, the output voltage is always higher than the input voltage [18]. Much like the buck converter, the boost converter consists of a MOSFET, diode, inductor, capacitor and a load but in a lightly different configuration. Figure 17 shows a basic boost converter with ideal components.

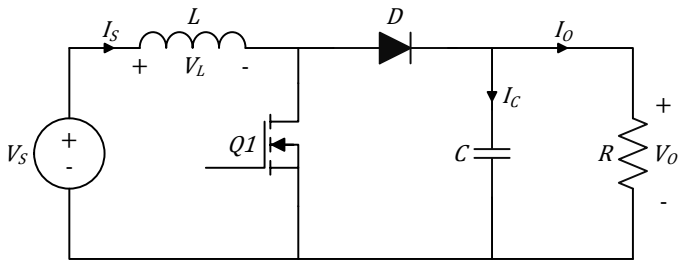

Figure 17: Conventional Boost Converter

In this circuit, there are two modes in which it can operate. The first mode is when the switch is in position 1 (on state) and the second mode is when the switch is in position 2 (off state).

When the boost converter is initially in the on state as shown Figure 18, a short is created from the right-hand side of the inductor to the negative input of the supply terminal. Current flows between the positive and negative supply terminal through the inductor, which stores energy in its magnetic field. There is virtually no current flowing in the remainder of the circuit as the combination of the diode and capacitor represent a much higher impedance that the path directly through the MOSFET.

After the initial startup on state, every other time the circuit is in the on state the cathode of the diode is more positive than its anode, to the charge on the capacitor. The diode is therefore turned off so the output of the circuit is isolated form the input. However, the load continues to be supplied with $(V_{in} + V_L)$ from the charge of the capacitor. Although the charge of the capacitor drains away through the load during this period, the capacitor is recharged each time the MOSFET switches off, so maintaining an almost steady output voltage across the load. The voltage across the inductor and current through the capacitor is simply:

$$V_L = V_s$$

$$I_c = \frac{-V_o}{R}$$

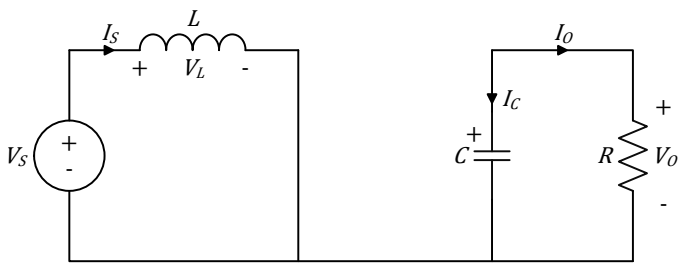

Figure 18: Boost Converter (On State)

During the on state the current through the inductor rises linearly given by:

$$V_L = L\left(\frac{dI_L}{dt}\right)$$

$$\left(\frac{dI_L}{dt}\right) = \frac{V_L}{L} \Rightarrow \left(\frac{V_s}{L}\right)$$

$$\Delta I_{L(on)} = \int_0^{t_{on}} \frac{V_L}{L} dt \Rightarrow \left(\frac{V_s}{L}\right) t_{on} \; where \; t_{on} = DT$$

$$\Delta I_{L(on)} = \left(\frac{V_s}{L}\right) DT$$

The voltage across the capacitor is given by:

$$I_c = C\left(\frac{dV_o}{dt}\right)$$

$$\left(\frac{dV_o}{dt}\right) = \frac{I_c}{C} \Rightarrow \left(\frac{-V_o}{R * C}\right)$$

$$\Delta V_{c(on)} = \int_0^{t_{on}} \frac{I_c}{C} dt \Rightarrow \left(\frac{-V_o}{R * C}\right) t_{on} \; where \; t_{on} = DT$$

$$\Delta V_{c(on)} = \left(\frac{I_o}{C}\right) DT$$

During the off state when the MOSFET is rapidly turned off, as shown in Figure 19, there is a sudden drop in current causing the inductor to produce a back-EMF in the opposite polarity to the voltage across the inductor during the on period, to keep current flowing. This results in two voltages, the supply voltage V_{in} and the back-EMF voltage across the inductor in series with each other. This higher voltage forward biases the diode ($V_{in} + V_L$), now that there is no current path through the MOSFET. The resulting current through the diode charges up the capacitor to ($V_{in} + V_L$) minus the small forward voltage drop across the diode, and also supplies the load. The voltage across the inductor and current through the capacitor is:

$$V_L = V_s - V_o$$

$$I_c = I_L - \frac{V_o}{R}$$

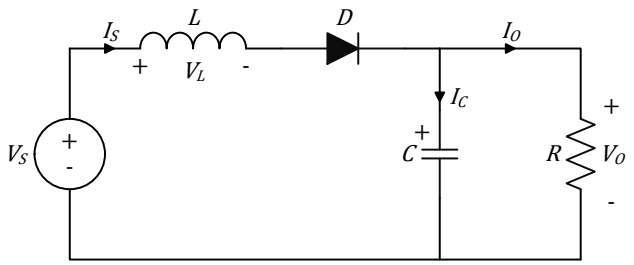

Figure 19: Boost Converter (Off State)

During the off state, the current through the inductor is given by:

$$V_L = L\left(\frac{dI_L}{dt}\right)$$

$$\left(\frac{dI_L}{dt}\right) = \frac{V_L}{L} \Rightarrow \left(\frac{V_s - V_o}{L}\right)$$

$$\Delta I_{L(off)} = \int_{t_{on}}^{T=t_{on}+t_{off}} \frac{V_L}{L} dt \Rightarrow \left(\frac{V_s - V_o}{L}\right) t_{off} \; where \; t_{off} = (1-D)T$$

$$\Delta I_{L(off)} = \left(\frac{V_s - V_o}{L}\right)(1-D)T$$

The voltage across the capacitor is given by:

$$I_c = C\left(\frac{dV_o}{dt}\right)$$

$$\left(\frac{dV_o}{dt}\right) = \frac{I_c}{C} \Rightarrow \left(\frac{I_L - \frac{V_o}{R}}{C}\right)$$

$$\Delta V_{c(off)} = \int_{t_{on}}^{T=t_{on}+t_{off}} \frac{I_c}{C} dt \Rightarrow \left(\frac{I_L - \frac{V_o}{R}}{C}\right) t_{off} \; where \; t_{off} = (1-D)T$$

$$\Delta V_{c(off)} = \left(\frac{I_L - I_o}{C}\right)(1-D)T$$

Like the buck converter, the net change in inductor current or the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady

state. By applying the inductor volt-second balance equation for a boost converter and breaking it down, the output voltage equation for a boost converter can be obtained in terms of the output voltage, input voltage and duty cycle:

$$\Delta I_{L(on)} + \Delta I_{L(off)} = 0$$

$$\left(\frac{V_s}{L}\right) DT + \left(\frac{V_s - V_o}{L}\right)(1 - D)T = 0$$

$$(V_s)DT + (V_s - V_o)(1 - D)T = 0$$

$$V_o = \left(\frac{V_s}{1 - D}\right)$$

Also, the net change in capacitor voltage or the total area (or charge balance) under the capacitor current waveform is zero whenever the converter operates in steady state. By applying the capacitor charge balance equation, the output current can be obtained in terms of the output current, input current and duty cycle:

$$\Delta V_{c(on)} + \Delta V_{c(off)} = 0$$

$$\left(\frac{I_o}{C}\right) DT + \left(\frac{I_L - I_o}{C}\right)(1 - D)T = 0$$

$$(I_o)DT + (I_L - I_o)(1 - D)T = 0$$

$$I_L = \left(\frac{I_o}{1 - D}\right)$$

The output waveforms of the voltage and current during one cycle period are shown in Figure 20.

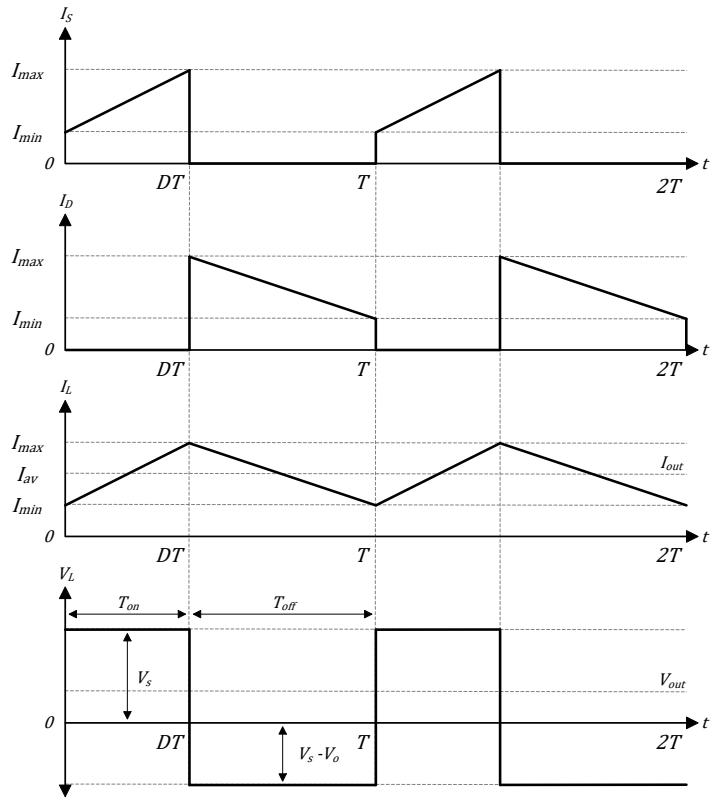

Figure 20: Boost Converter Voltage and Current Waveforms

3.2.3 Buck-Boost Converter

In a buck-boost converter, the output voltage magnitude is either greater than or less than the input voltage magnitude [18]. It is a type of switch mode power supply that combines the principles of the buck converter and the boost converter in a single circuit. With this topology, there are essentially two modes in which it can operate, inverting and non-inverting.

3.2.3.1 Inverting Buck-Boost Converter

A basic inverting buck-boost converter has a negative output voltage with respect to ground [19]. In addition to input and output capacitors, the power stage consists of a MOSFET, a diode and an inductor as shown in Figure 21.

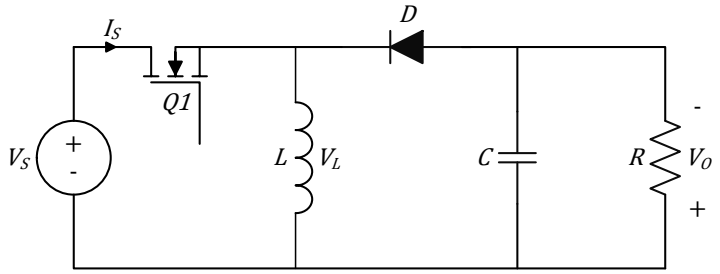

Figure 21: Conventional Inverting Buck-Boost Converter

In the on state, shown in Figure 22, the input voltage source is directly connected to the inductor causing the inductor current to ramp up at a rate that is proportional to the input voltage. This results in accumulating energy in the inductor. At this state, the output capacitor supplies the entire load current. The voltage across the inductor is simply:

$$V_s = V_L$$

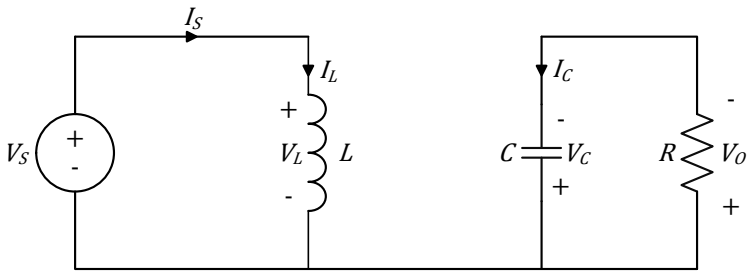

Figure 22: Inverting Buck-Boost Converter (On State)

During the on state the current through the inductor is given by:

$$V_L = L\left(\frac{dI_L}{dt}\right)$$

$$\left(\frac{dI_L}{dt}\right) = \frac{V_L}{L} \Rightarrow \left(\frac{V_s}{L}\right)$$

$$\Delta I_{L(on)} = \int_0^{DT} \frac{V_L}{L}\,dt \Rightarrow \left(\frac{V_s}{L}\right) t_{on} \; where \; t_{on} = DT$$

$$\Delta I_{L(on)} = \left(\frac{V_s}{L}\right) DT$$

During the off state, shown in Figure 23, the diode becomes forward-biased and the inductor current ramps down at a rate proportional to V_{out}. While in this state, energy is transferred from the inductor to the output load and capacitor. If zero voltage drop in the diode is assumed, and a capacitor large enough for its voltage to remain constant then he voltage across the inductor is:

$$V_o = V_L$$

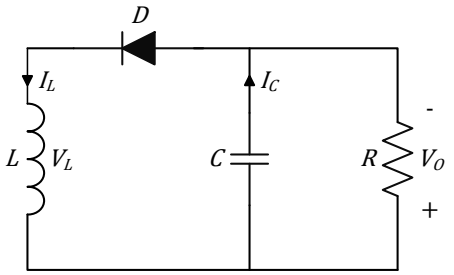

Figure 23: Inverting Buck-Boost Converter (Off State)

During the off state, the current through the inductor is given by:

$$V_L = L\left(\frac{dI_L}{dt}\right)$$

$$\left(\frac{dI_L}{dt}\right) = \frac{V_L}{L} \Rightarrow \left(\frac{V_o}{L}\right)$$

$$\Delta I_{L(off)} = \int_0^{(1-D)T} \frac{V_L}{L} dt \Rightarrow \left(\frac{V_o}{L}\right) t_{off} \; where \; t_{off} = (1-D)T$$

$$\Delta I_{L(off)} = \left(\frac{V_o}{L}\right)(1-D)T$$

By applying the inductor volt-second balance equation for a buck-boost converter and breaking it down, the output voltage equation can be obtained for a boost converter in terms of the output voltage, input voltage and duty cycle [19].

$$\Delta I_{Lon} + \Delta I_{Loff} = 0$$

$$\left(\frac{V_s}{L}\right) DT + \left(\frac{V_o}{L}\right)(1-D)T = 0$$

$$(V_s)DT + (V_o)(1-D)T = 0$$

$$V_o = -\left(\frac{D}{1-D}\right) V_s$$

This equation indicates that the magnitude of the output voltage could be either higher when $D > 0.5$ or lower when $D < 0.5$ than the input voltage. However, the output voltage always has an inverse polarity relative to the input. The output waveforms of the voltage and current during one cycle period are shown in Figure 24.

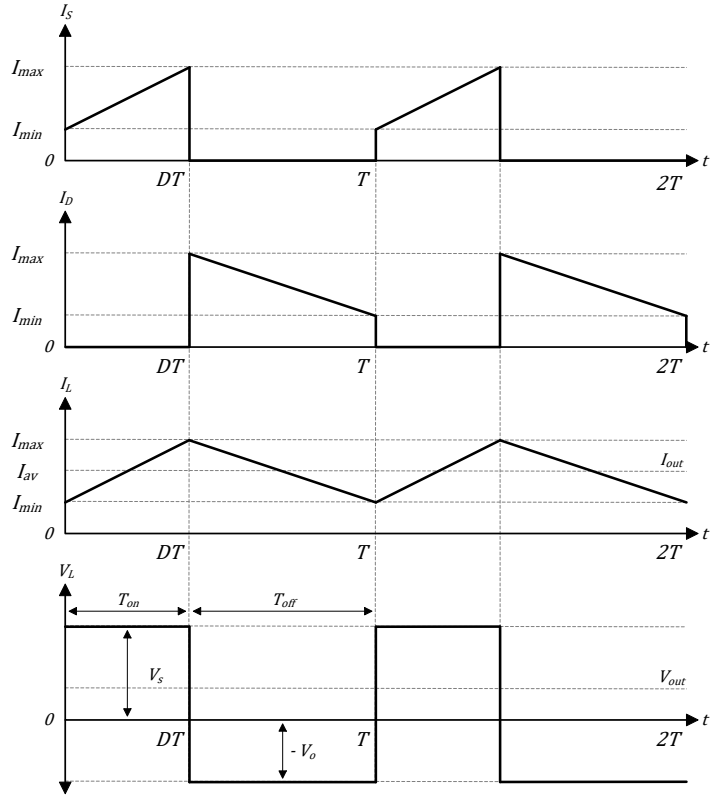

Figure 24: Buck-Boost Converter Voltage and Current Waveforms

3.2.3.2 Non-Inverting Buck-Boost Converter

The inverting buck-boost converter does not serve the needs of applications where a positive output voltage is required. To solve this issue, the SEPIC, Zeta and two-switch buck-boost converter are three popular non-inverting buck-boost topologies with a positive output. Each topology has its advantages and disadvantages however in the scope of this paper the two-switch buck-boost converter will be discussed.

The two-switch buck-boost converter is a cascaded combination of a buck converter followed by a boost converter seen in Figure 25. By combining these two converter designs, it is possible to have a circuit that can cope with a wide range of input voltages both higher or lower than that needed by the load. Since both buck and boost converters use very similar components; they just need to be re-arranged depending on the level of the input voltage. A conventional two-switch buck-boost converter uses a single inductor. However, it has an additional MOSFET and diode compared to an inverting buck-boost converter. By switching the MOSFETs $Q1$ and $Q2$ on and off simultaneously, the converter operates in buck-boost mode with a non-inverting conversion.

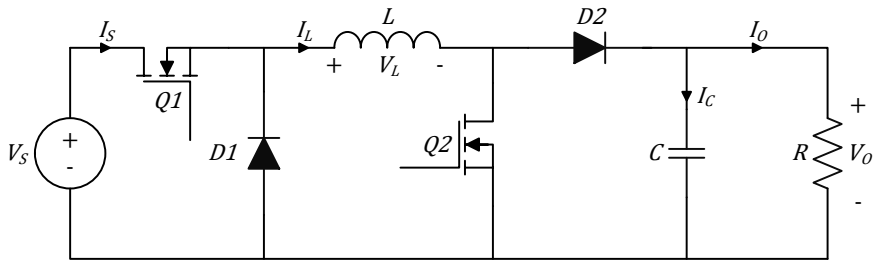

Figure 25: Conventional Non-Inverting Buck-Boost Converter

In buck mode, $Q2$ is controlled to be always off and the output voltage is regulated by controlling $Q1$ as in a typical buck converter. The circuit with $Q2$ off is shown in Figure 26.

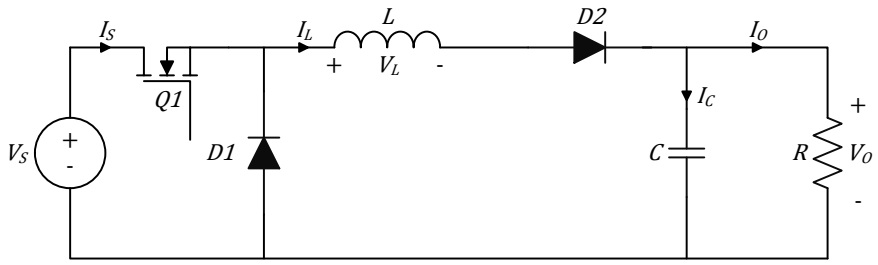

Figure 26: Non-Inverting Buck-Boost Converter (Buck Mode)

The voltage conversion ratio in this mode of operation is the same as that of a typical buck converter given by:

$$V_o = DV_s$$

Where D is the duty cycle of $Q1$. In buck mode, the output voltage is always lower than the input voltage since D is always less than one. In boost mode, $Q1$ is controlled to always be on, $D1$ is reverse biased disconnecting it from the circuit and the output voltage is regulated by controlling $Q2$ as in a typical boost converter as shown in Figure 27.

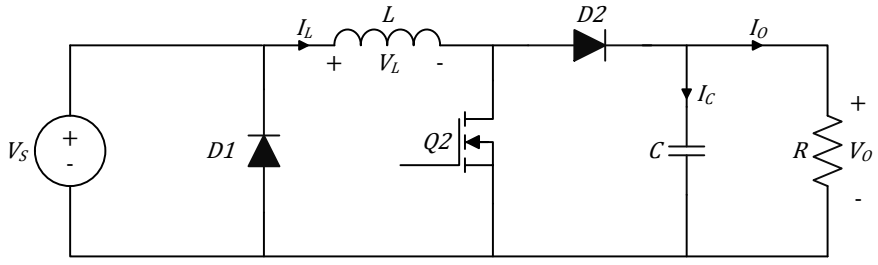

Figure 27: Non-Inverting Buck-Boost Converter (Boost Mode)

The voltage conversion ratio in this mode of operation is the same as that of a typical buck converter given by:

$$V_o = \left(\frac{V_s}{1-D}\right)$$

In this equation, D is the duty cycle of $Q2$. In boost mode, the output voltage is always greater than the input voltage because D is always greater than zero [19].

3.3 Modes of Operation

3.3.1 Discontinuous vs. Continuous Conduction Mode

One of the most important parts of a converter is the inductor [20]. Sizing the inductor and setting its operation mode makes the converter function correctly. The shape and magnitude of current of the inductor are dictated by the inductance of the inductor itself. Therefore, choosing the right inductor value is very important. The inductor current of a converter can be classified in three types; continuous, discontinuous or boundary. A continuous current means that the minimum level of the inductor current waveform is never touching zero in any switching period [20]. A discontinuous current is the other way around. The minimum level of the inductor current is touching zero before the next PWM high or on state occurs. In boundary, current, the inductor current waveform minimum level is always at zero every switching cycle [20].

Discontinuous conduction mode (DCM) (Figure 28) is characterized by the inductor current being zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle as shown in the figure below. As the DC load current is reduced to a value that causes the average inductor current to be less than half the inductor ripple current. When the inductor current becomes zero, the power to the load is supplied by the capacitance alone. The output voltage depends on the circuit component values and the duty ratio of the MOSFET.

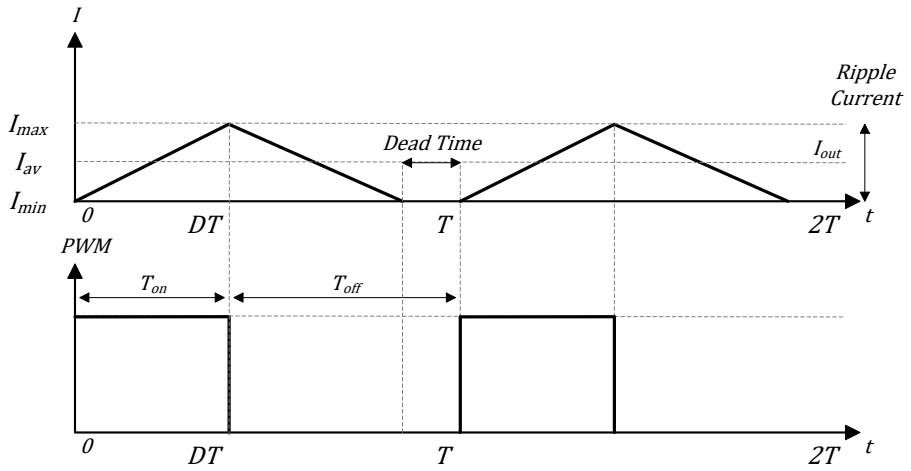

Figure 28: Discontinuous Conduction Mode (DCM)

Letting the current on the inductor become discontinuous yields very high peak value and the root mean square (RMS) currents of the inductor as well as the active devices are high. These correspond to high power losses that jeopardize efficiency and needs more rugged and expensive devices [20]. The inductor ripple current is high as well. Converters with high power ratings are not deliberately set to operate at DCM. As illustrated there is a dead time on the inductor current meaning that the energy on the inductor is already consumed before the next charging period occurs.

Continuous conduction mode (CCM) (Figure 29) is characterized by current flowing continuously in the inductor during the entire switching cycle in steady state operation.

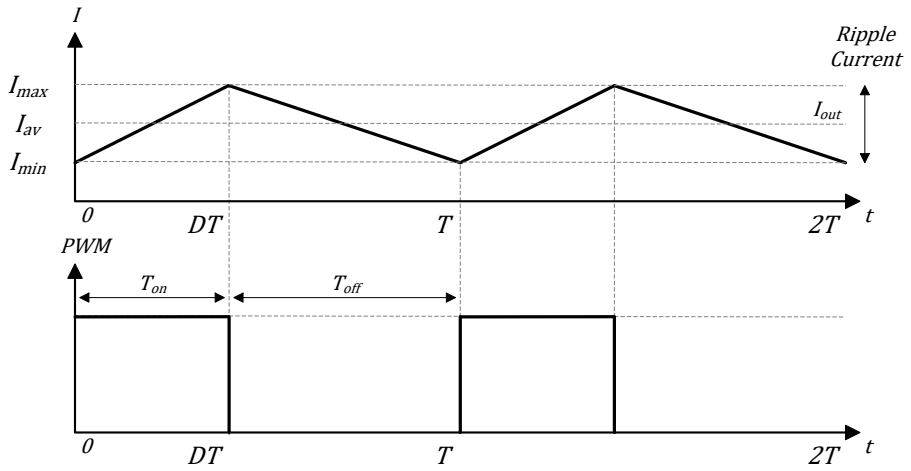

Figure 29: Continuous Conduction Mode (CCM)

To ensure the operation of the converter in the CCM region, the inductor must be big enough such that its energy will not be depleted until the next charging cycle occurs [20]. Provided the load current is higher than half the ripple current of the output inductor, the converter will operate in this mode. When the inductor current is continuous, it will not go to zero at any switching cycle. Because of this, the ripple current is small. A smaller ripple current corresponds to lower losses on the inductor as well as on the active power devices. Thus, this is more preferred for higher efficiency requirement. The drawback on setting the inductor current of for example a buck converter to CCM is that it needs a larger inductance. A larger inductance means a bulky physical size and there is a price increase.

The advantages of CCM over DCM include the DC conversion ratio is independent of the load, which makes DC analysis of converters operating in CCM easier. While operating in DCM, the output voltage depends on the load and the duty ratio of the switch, which makes DC analysis of converters operating n DCM more complicated. Also, to deliver the same power in DCM as in CCM, the peak currents are higher, resulting in greater losses in the conduction paths leading to

reduced efficiency and higher peak current can also cause switch stress and greater input and output current ripple that adversely affect the noise issues.

3.3.2 Non-Synchronous vs. Synchronous

Power converters are becoming increasingly commonplace in the electrical industry. Product manufacturers and suppliers of electrical equipment are demanding ever increasing functionality (lower input and output voltages, higher currents, faster transient response) from their power supply systems. While earlier DC/DC power converters relied on the use of diodes for current rectification (which is necessary for the converters operation) increased performances have been achieved by adopting synchronous rectification in the design of the power supply instead. Synchronous rectification means that the functionality once provided by the diode -i.e. current rectification – is now undertaken by a rectifying transistor (MOSFET). Such rectification improves efficiency, thermal performance, power densities, manufacturability, reliability as well as having typically faster switching transients and decreases the overall system cost for power supplies [21].

Conventional converters like those mentioned above consisted of a MOSFET, diode, capacitor, inductor and load. This configuration, where a diode is used instead of a MOSFET, is considered to be nonsynchronous meaning only the MOSFET is being switched while the diode (typically Schottky) only acts as a switch. The Schottky diode in this circuit is selected by its forward voltage drop and reverse leakage current characteristics alone. However, physical limitations prevent he forward voltage drop of diodes from being reduce below approximately 0.3 V so as the output voltage drops the diodes forward voltage becomes more significant which reduces the converters efficiency [21].

In a synchronous converter, the diode is replaced with a power MOSFET and controlled to be either on or off mimicking what the diode would be doing. Figure 30 shows a buck converter in the non-synchronous and synchronous configuration to illustrate the difference between the two converters.

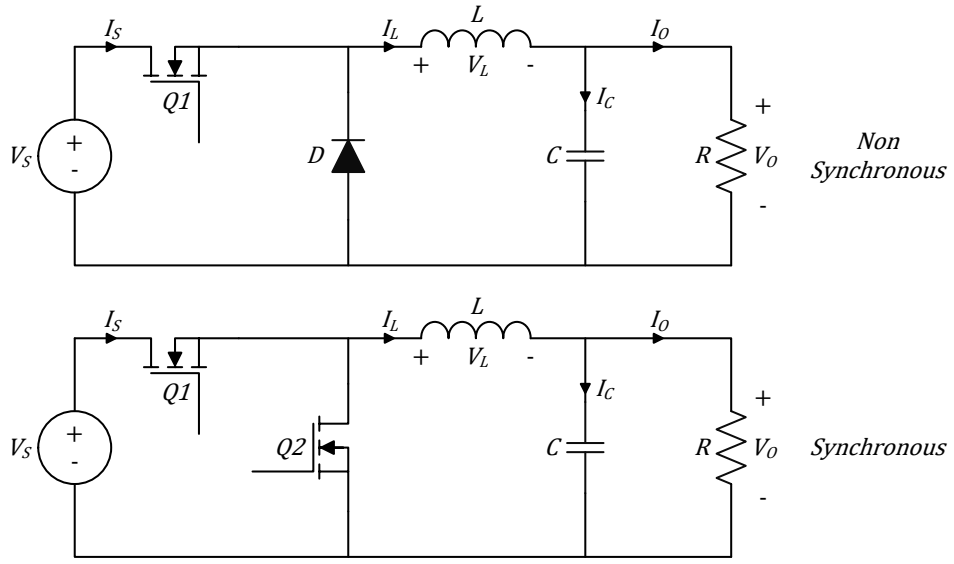

Figure 30: Non-Synchronous and Synchronous Buck Converter

The main advantage of a synchronous rectifier is that the voltage drop across the MOSFET can be lower than the voltage drop across the diode of the nonsynchronous converter. If there is no change in power level, a lower voltage drop translates into less power dissipation and higher efficiency [22]. This can be seen in the Figure 31 below. The plot shows the efficiency comparison between the non-synchronous and synchronous buck converters shown in Figure 30 if the power level remains the same. When the converter is not bucking, there is very little difference between the two converters. However, as the converter begins to buck its voltage and current begins to rise, the difference in efficiency between the two becomes present.

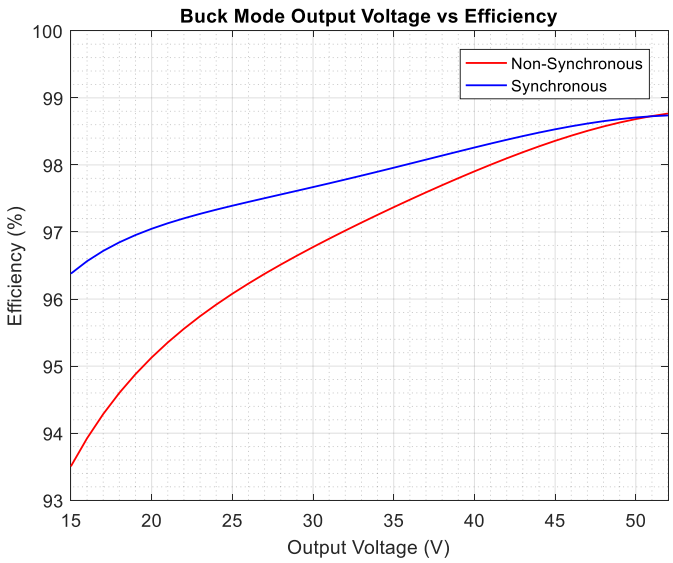

Figure 31: Buck Converter Synchronous vs. Non-Synchronous Efficiency

There are many advantages for using a synchronous topology vs. non-synchronous such as higher efficiency, lower power dissipation, better thermal performance, lower profile, increased quality and optimal current sharing when MOSFETs are paralleled. Yet, with all these benefits they have their disadvantages. The MOSFETs must be driven in a complimentary manner with a small dead time between their conduction intervals to avoid shoot-through which essentially shorts the power supply to ground through the MOSFET. This current introduces a large switching loss, and in the worst case, the MOSFET or the power supply can be damaged [23]. In addition to switching losses, conduction losses play a big role in the overall efficiency of the converter. Using MOSFETs in place of the diode reduces the conduction loss significantly, however, it does not eliminate it entirely. Therefore, MOSFETs must be chosen with a low R_{dson} to reduce conduction losses as much as possible. In addition, MOSFETs can be paralleled to handle higher output currents and because the effective R_{dson} is inversely proportional to the number of paralleled devices, conduction losses can be reduced. Since R_{dson} has a positive

temperature coefficient, the MOSFETs will automatically share current equally making this an attractive solution to reduce the R_{dson}.

Another drawback is that by using MOSFETs in place of the diode, it prohibits the converter from entering the discontinuous conduction mode and thus degrades the efficiency at light loads. Here the CCM operation at light load (implies low output power) in synchronous converters is a drawback if standby efficiency is a major concern. In short, the MOSFETs conduction loss comes into play and the total power dissipation will be relatively large. In DCM operation, there is no conduction loss when the inductor current is zero. In addition, zero current switching operation helps reduce switching loss. To summarize, a synchronous converter yields high efficiency at high output current but low efficiency at low output power [23].

Even though there are many disadvantages to using a synchronous converter topology. The increased efficiency outweighs any disadvantage over a conventional converter especially with regards to PV systems since efficiencies are already relatively low. Therefore, the synchronous converter topology is the preferred method to extract the maximum power from the PV modules.

CHAPTER 4. BOOST-BUCK DESIGN DETAILS

4.1 Introduction

This chapter expands on the concepts of the previous chapters where chapter 2 defined the high-level issues associated with the PV array and chapter 3 introduced power electronic topologies to alleviate the system issues. This chapter will be broken down into the following sections:

- Converter Specification
    - Target Specifications
    - Design Specifications
- Power Stage Design
    - Topology Selection
    - Switch Frequency Selection
    - Minimum and Maximum Duty Cycle
    - Component Selection
    - Component Losses
- Control and Operation
    - General Converter Operation
    - Maximum Power Point Tracking Algorithm
    - Boost-Buck Control Loop
    - Over Voltage and Over Current
    - Module On/Off and MPP On/Off
- Microprocessor Control

Choosing the right DC/DC converter for an application can be a daunting challenge. Not only are there many available, such as the ones mentioned earlier, but there are an incredible number of trade-offs to consider such as size, efficiency, cost, temperature, accuracy etc. Designers want to improve efficiency without increasing cost, especially in a high-volume consumer electronics application where reducing power consumption by one watt can save megawatts from the grid. Besides deciding which converter to use a designer must also decide which mode of operation the converter will be running in.

4.2 Converter Specifications

As time goes by in the solar industry, newer technologies emerge driving the cost of PV down, increasing efficiency and increasing the power output. To keep up with this trend the DC/DC converter must be able to accept a wide variety of voltage and current to maximize the power output of each module to the grid. When it comes to PV modules, the five variables of primary interest are V_{oc}, V_{mp}, I_{mp}, I_{sc} and P_{mp}. These values of a PV module dictate the specifications that must be designed to.

4.2.1 Target Specifications

As mentioned in Chapter 2, the number of individual PV cells required to complete a single PV module depends on how much power is required and the type of PV cells being used; monocrystalline, polycrystalline or thin film. PV modules come in all sorts of configurations and sizes to help meet the energy needs. Most module manufactures produce standard PV modules with common output voltages and currents. These standard module cell configurations are: 36, 48, 54, 60, 72, 96, 108, and 128.

For a typical residential and commercial installation, PV modules up to 96-cells are used with 60, 72 and 96 being the most common size where most cell dimensions are the standard size of either 12.5 cm x 12.5 cm (12.5 cm^2) or 15.6 cm x 15.6 cm (15.6 cm^2).

Based on the information from Table 1 in chapter 2, a new table can be made (Table 2) to approximate the different PV modules that can be found today for residential and commercial installations. These values presented will be used as the basis for the calculations needed to design the converter.

Table 2: Calculated Values for PV Modules of Different Sizes

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
36	12.5 cm^2	21.6772	17.6490	5.0860	5.4688	89.7622
36	15.6 cm^2	22.1691	17.6681	7.9299	8.5176	140.1068
48	12.5 cm^2	28.9030	23.5319	5.0860	5.4688	119.6829
48	15.6 cm^2	29.5588	23.5575	7.9299	8.5176	186.8091
54	12.5 cm^2	32.5159	26.4734	5.0860	5.4688	134.6433
54	15.6 cm^2	33.2536	26.5022	7.9299	8.5176	210.1602
60	12.5 cm^2	36.1287	29.4149	5.0860	5.4688	149.6036
60	15.6 cm^2	36.9485	29.4469	7.9299	8.5176	233.5113
72	12.5 cm^2	43.3545	35.2979	5.0860	5.4688	179.5243
72	15.6 cm^2	44.3381	35.3362	7.9299	8.5176	280.2136
96	12.5 cm^2	57.8060	47.0639	5.0860	5.4688	239.3658
96	15.6 cm^2	--	--	--	--	--

These modules are just an approximation of cells on the market. The voltage and current can fluctuate due to many reasons however it is just to show the range of input the DC/DC converter must be able to accept. Notice that the 96-cell module with 15.6 cm x 15.6 cm dimensions has no information. This module has been omitted because this module is just too large to be practically usable for a residential installation.

Appendix B has a list of PV modules with different cell numbers and sizes that can be bought and used today as a comparison to the calculated values derived earlier. The tables show the most common parameters that would typically be seen when purchasing a PV module. Notice that even though a module has the same cell count the numbers are slightly different and even the maximum power output is slightly different. This is because of the manufacturing process and physical size. An average is given for each cell number to give an approximation of the specification of a module with a certain cell number.

Comparing the actual PV modules in Appendix B with the values calculated in Table 2 shows that the values are not very different from each other. As such, the calculated parameters in Table 2 will be used for simulating and testing the design later in the paper.

At a minimum voltage and maximum current scenario, the smallest PV module that would be used as an input would be a 36-cell module with the specifications in Table 3.

Table 3: Minimum Voltage Maximum Current PV Module Specifications

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
36	15.6 cm^2	21.6772	17.6490	7.9299	8.5176	140.1068

With this PV module, the maximum power that can be extracted is 140.1068 W. There are other modules that would produce lower power however this module will be used to stress the design in the worst-case scenario when the input voltage is low. Using Matlab, the I-V and power curve of this module can be generated and is shown in Figure 32.

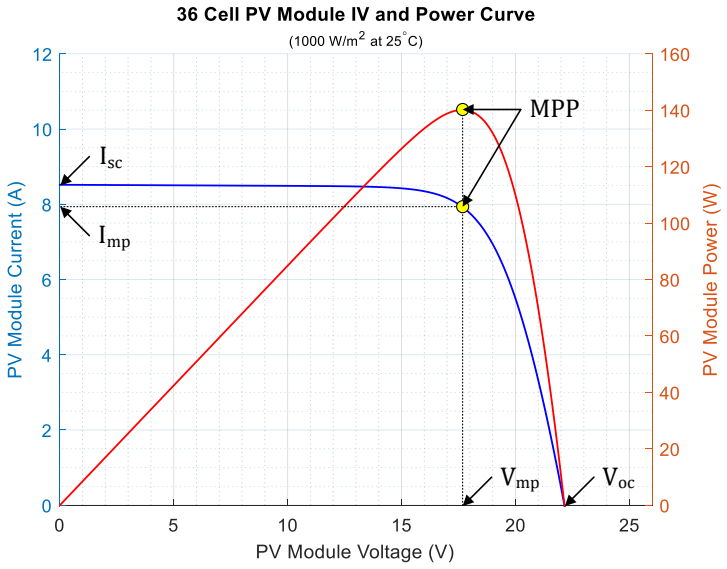

Figure 32: Output Characteristics of a 36-Cell PV Module

At a maximum voltage and minimum current scenario, the largest PV module that would be used as an input would be a 96-cell module with the specifications in Table 4.

Table 4: Maximum Voltage Minimum Current PV Module Specifications

Cells	*Cell Type*	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
96	12.5 cm²	57.8060	47.0639	5.0861	5.4688	239.3658

With this PV module, the maximum power that can be extracted is 239.3658 W. This module will be used to stress the design in the worst-case scenario when the input voltage is high. The I-V and power curve of this module is shown in Figure 33.

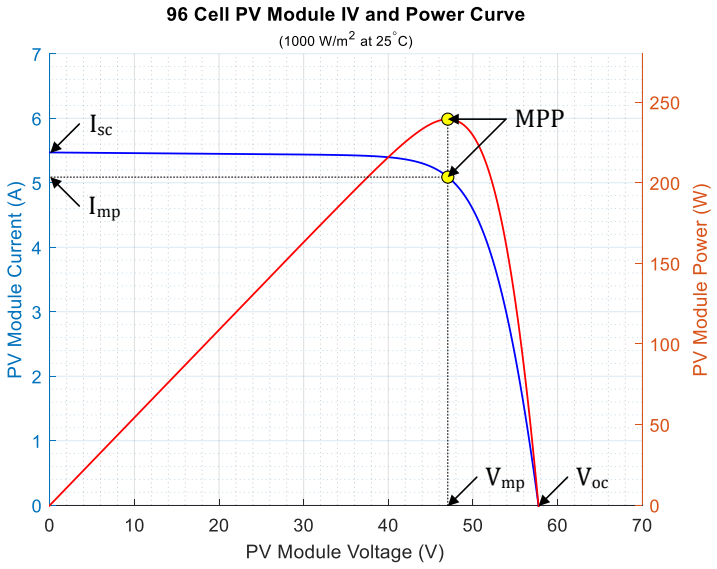

Figure 33: Output Characteristics of a 96-Cell PV Module

At a maximum power scenario, the highest power PV module that would be used as an input would be a 76-cell module with the specifications in Table 5.

Table 5: Maximum Power PV Module Specifications

Cells	*Cell Type*	$V_{oc\,(V)}$	$V_{mp\,(V)}$	$I_{mp\,(A)}$	$I_{sc\,(A)}$	$P_{mp\,(W)}$
76	15.6 cm²	44.3381	35.3362	7.9299	8.5176	280.2136

With this PV module, the maximum power that can be extracted is 280.2136 W. This module will be used to stress the design in the scenario when the input power is high. The I-V and power curve of this module is shown in Figure 34.

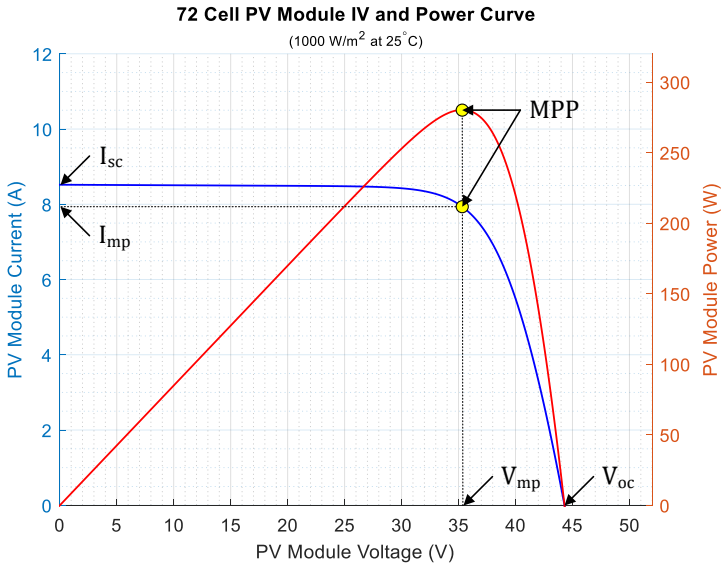

Figure 34: Output Characteristics of a 72-Cell PV Module

Based on these three PV module sizes for residential and commercial modules, the following assumptions about the specification for the DC/DC converter can be made.

- The maximum input power from the module must be below 280.0 watts based on the P_{mp} of the 72-cell module.
- The minimum input the converter must track down to is 17.0 volts based on the V_{mp} of the 36-cell module.
- The maximum input the converter must track up to is 48.0 volts based on the V_{mp} of the 96-cell module.
- The maximum input current from the module will be 8.5 amps I_{sc} based on the 15.6 cm^2 cell size.
- The maximum output voltage must be no more than 58.0 volts based on the V_{oc} of the 96-cell module.
- The maximum output current must be no more than 9.2 amps given the fuse requirements in a residential system to be outfitted with 12.0 A fuses.

- The maximum efficiency must be around 99.0 % to be a cost-effective solution.

Therefore, the specifications the converter will be designed to are in Table 6:

Table 6: DC/DC Converter Target Specifications

Input	
Max Module Power	280.0 W
Max Module DC Voltage	58.0 V
Module MPP DC Voltage Range	17.0 - 48.0 V
Max Module DC Current	8.5 A
Output	
Max DC Output Voltage	58.0 V
Max DC Output Current	9.2 A
Max Efficiency	99.0 %

4.2.2 Design Specifications

Although the target specifications in Table 6 are what the converters nominal input and output characteristics should be, it does not take into account abnormalities that may push the converter beyond its limits. If such anomalies are to occur the converter must be overdesigned to be able to function properly and not become damaged.

It was discussed that the temperature and irradiance both affect the voltage and current of the PV module. Based on the plots in Figure 5 and Figure 6, as the ambient temperature drops, the output voltage of the module increases. Also as the irradiance increases, the output current of the module will also increase.

There is a phenomenon in the PV world called the edge-of-cloud effect where as a cloud begins to cover the sun or when the sun is emerging from behind a cloud, there is a sudden burst of energy that produces more power than normal. This is caused by light refraction through the

water molecules in the cloud [24]. This power increase can be upward to 25.0 % in current output meaning that if the convert was designed to the target specification of the input current being no more than 8.5 A then this could damage the device. Common practice is to add 20.0 to 25.0 % of the amperage ratings to account for this over-sun condition [24].

$$8.5\ A + (8.5\ A * 25\ \%) = 10.63\ A$$

$$9.2\ A + (9.2\ A * 25\ \%) = 11.50\ A$$

Another consideration is temperature. If a PV module is installed in a hot climate such as the desert, the voltage of the module will decrease as the ambient temperature increases. This would not be a problem to the converter because the voltage would always be lower than the maximum. However, if a PV module is installed in a cold climate region where the temperature rarely gets above 0.0 °C, this could pose a problem to the converter because the voltage would be greater than the nameplate V_{oc} and V_{mp}. There is a temperature coefficient associated with each PV module to de-rate the voltage of the module due to temperature. This coefficient depends on the module but has a range generally between -0.2 to -0.5 %/C [25]. It's a negative coefficient meaning the cooler the temperature is, the more voltage the module will produce. By taking the average temperature coefficient of -0.35 %/°C and assuming an average ambient temperature of 0.0 °C, new voltage values can be calculated and used for the design.

$$((25.0\ °C - 0.0\ °C) * 0.0035\ \%/°C)) * 48.0\ V = 52.20\ V$$

$$((25.0\ °C - 0.0\ °C) * 0.0035\ \%/°C)) * 88.0\ V = 63.08\ V$$

To account for these conditions, the DC/DC converter will be designed to meet the specification in Table 7. The I_{mp} and I_{sc} current are both increased by 25.0 % to account for over sun conditions while the voltage V_{mp} will increase by 0.35 %/°C based on a 0.0 °C ambient temperature. The open circuit voltage will still be limited to 58.0 V to protect the MOSFETs that will be used in the design.

Table 7: DC/DC Converter Design Specifications

Input	
Max Module Power	350.0 W
Max Module DC Voltage	58.0 V
Module MPP DC Voltage Range	17.0 - 52.2 V
Max Module DC Current	10.63 A
Output	
Max DC Output Voltage	58.0 V
Max DC Output Current	11.5 A
Max Efficiency	99.0 %

4.3 Power Stage Design

The power stage is the heart of the DC/DC converter and it consists of power MOSFETs, inductors and capacitors. It is responsible for converting the power from the input to the output via switching by either bucking or boosting to achieve the desired output. These components are critical in ensuring optimum performance and efficiency. If not selected properly, excessive heat dissipation and other factors could reduce the life of the product.

The first step after the operating parameters of the converter are solidified is to do the necessary calculations to the power stage to select the proper components for the engine to work at its peak efficiency. The necessary parameters to calculate the power stage components are:

- Switch frequency
- Minimum and maximum duty cycle
- Input and output voltage range
- Input and output current range

Yet, even before any of these calculations can be done, the topology of the DC/DC converter must be selected.

4.3.1 Topology Selection

Per the design specifications listed in Table 7, many converter topologies mentioned in chapter 3 can be eliminated from a list of possible choices for this design as well as the modes in which the converter will operate. The converter must be able to handle a wide input voltage range that fluctuates below or above the desired output voltage [26]. This eliminates the standard buck and boost converter as they can only handle converting in one direction. It must have a positive output voltage eliminating the inverting buck-boost converter. The converter must also be as efficient as possible which eliminates the non-inverting buck-boost topology that uses two MOSFETs and two diodes shown in Figure 25. This conventional two-switch buck-boost converter works well and is a good low-cost converter with a simple controller, however, it suffers from high current stress and high conduction losses [26]. The excessive power dissipation associated with low efficiency makes the conventional two-switch buck-boost converter impractical for high power applications [26]. This leaves only a synchronous non-inverting buck-boost converter in Figure 35.

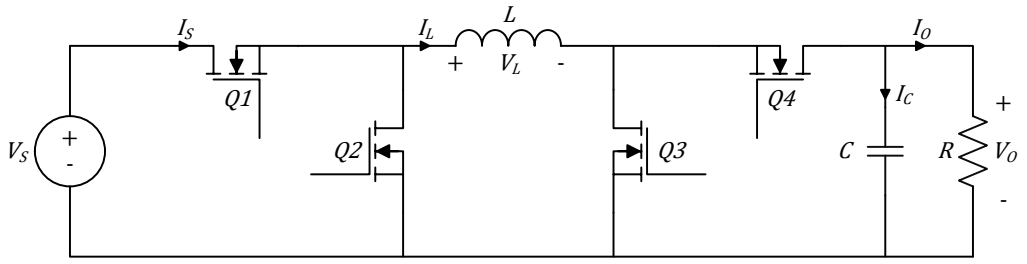

Figure 35: Non-Inverting Synchronous Buck-Boost Converter

Notice how the diodes are replaced with MOSFETs. The added benefit to this is the requirement that it must work in the continuous conduction mode which is already taken care of

by using synchronous switching. A four-switch, buck-boost topology combines a single inductor design with synchronous rectification for both buck and boost legs. Moreover, as a cascaded combination of a buck converter followed by a boost converter, a four-switch buck-boost converter can operate in buck mode or boost mode rather than the conventional buck-boost mode. As such, its efficiency can be further improved [26]. The operation is divided into three different modes. When V_{in} is close to V_{out}, it operates in a buck-boost mode. When V_{in} is much higher or much lower than V_{out}, it operates as a buck converter or a boost converter. Since this topology is a cascade buck converter with a boost converter, it can also be configured in the boost-buck configuration where the first stage is the boost stage and the second is the buck stage shown in Figure 36.

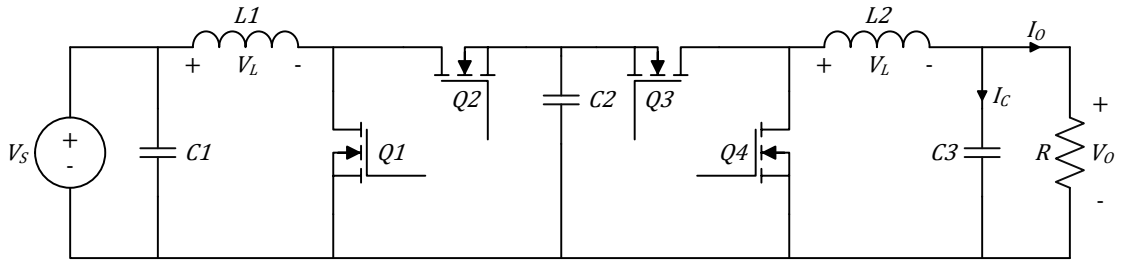

Figure 36: Non-Inverting Synchronous Boost-Buck Converter

In this approach, the boost converter creates an intermediate bus which is then stepped down using a buck converter. The input and output currents are continuous because of the presence of a series inductor and it has an added benefit of an output PI filter when in boost mode which helps reduce output voltage ripple. The operation is divided into three different modes, much like the buck-boost converter, which can be seen more clearly in Figure 37.

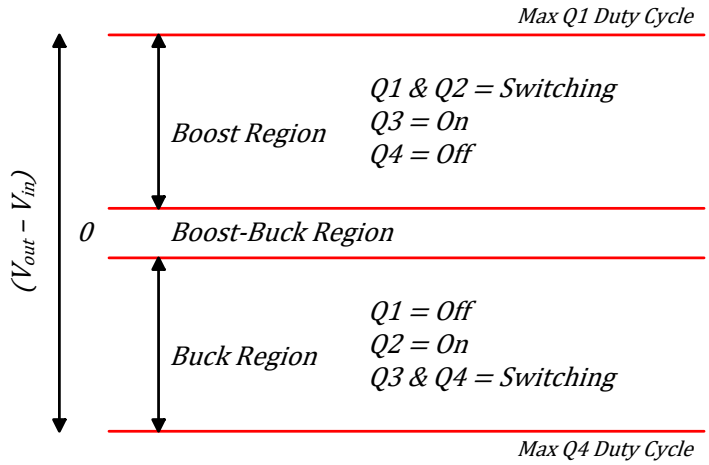

Figure 37: Boost-Buck Switching Diagram

Both configurations work, however, in the scope of this thesis, the focus will be on the boost-buck configuration.

4.3.2 Switch Frequency Selection

Before any calculations are done, the first step is to choose a switch frequency in which the converter will be operating in. This is an important parameter to consider because it determines the size and value of the components that will be needed to build the converter. It affects nearly every performance characteristic of the supply [27]. A higher switching frequency makes it possible to use smaller inductors and capacitors. It also improves the overall step load behavior of the converter. However, as frequency increases and size decreases, so does the efficiency due to an increase in switching losses [28]. Another consideration is as frequency increases, the electromagnetic interference (EMI) radiation starts to become a problem and can affect other parts of the circuit. Higher switching frequency can also limit the maximum step up and step-down ratio that can be achieved.

High frequency converters greater than 1.0 MHz are often used when the input voltage is relatively low (5.0 V or less). This is because the switching losses at low input voltages are less and the maximum step-down ratios for these applications are lower as well. On the other hand, at higher frequencies, the EMI starts to become a problem. For most 12.0 V applications, switching frequencies between 500.0 to 800.0 kHz are suitable providing a good compromise between switching losses, efficiency and component size. In high current applications with input voltages greater than 18.0 V, it is better to use switching frequencies lower than 500.0 kHz to reduce the switching losses and still allow high step-down ratios. At these lower frequencies, EMI is lower, efficiency is higher, switching losses are lower and core losses become negligible. The only exception is that the size of these components become much larger. Since the maximum voltage of the converter is 60.0 V and low EMI is preferred with high step-up and step-down ratios, a frequency of 100.0 kHz is chosen [29].

4.3.3 Minimum and Maximum Duty Cycle

The first step after selecting the operating parameters of the converter is to calculate the maximum duty cycle for the boost side and the minimum duty cycle for the buck side. These values are important because at these duty cycles, the converter is operating at the extremes of its operating range.

4.3.3.1 Boost Mode

For the boost stage of the converter, the duty cycle for the minimum input voltage must be found because the minimum input voltage leads to the maximum switch current at the maximum duty cycle as seen in Figure 38 [30].

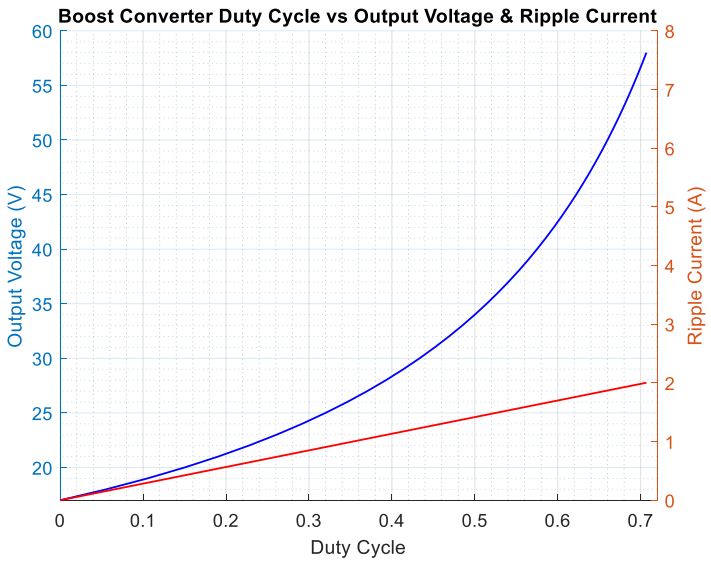

Figure 38: Boost Converter Duty Cycle vs. Output Voltage and Current Ripple

The maximum duty cycle for the boost side is given by the equation:

$$D_{boost} = 1 - \frac{V_{in(\min)} * \eta}{V_{out}}$$

From the design specifications, the minimum input voltage is going to be 17.0 V with a maximum operating output voltage of 52.0 V. Therefore, the maximum duty cycle for this scenario is:

$$D_{boost} = 1 - \frac{17.0\,V * \eta}{52.0\,V} = 0.673$$

4.3.3.2 Buck Mode

For the buck stage of the converter, the duty cycle for the maximum input voltage must be found because the maximum input voltage leads to the maximum switch current at 50.0 % duty cycle as seen in Figure 39 [30].

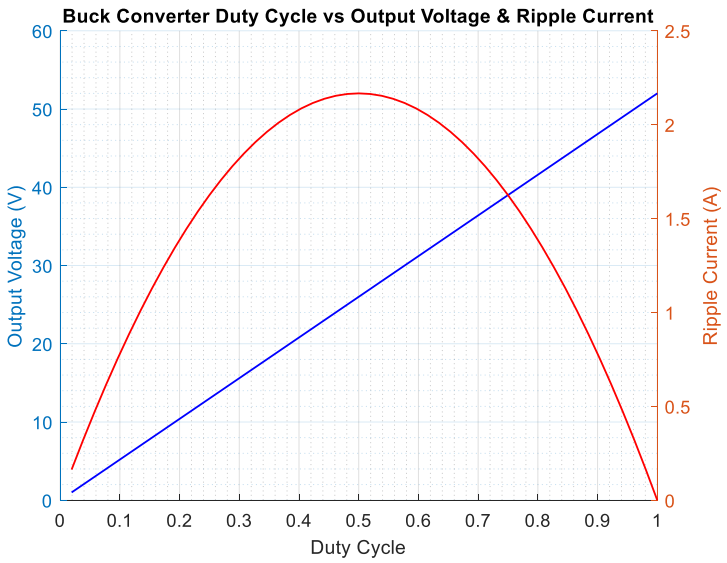

Figure 39: Buck Converter Duty Cycle vs. Output Voltage and Current Ripple

For the buck engine, the duty cycle is given by:

$$D_{buck} = \frac{V_{out} * \eta}{V_{in(\max)}}$$

Also, from the design specifications, the maximum operating input voltage will be 52.0 V and an output voltage of 26.0 V. The converter can go lower in voltage however at this duty cycle is where the most stress will be on the device. Therefore, the minimum duty cycle for this scenario is:

$$D_{buck} = \frac{26.0\,V * \eta}{52.0\,V} = 0.50$$

For both the boost and buck duty cycle calculations, the efficiency η is added because the converter must deliver the energy dissipated. Normally a value is assigned here to give a more realistic duty cycle than just the equation without the efficiency factor, however, all calculations will be based on the ideal scenario and then later the efficiency will be calculated. Therefore, the efficiency here is assumed to be 100.0 %. Now that these parameters are known all other components can be calculated.

4.3.4 Component Selection

The components for the boost-buck engine need to be calculated in a way that they will work for both the boost engine and buck engine separately. To do this each converter's components will be calculated separately at the extremes of their operating conditions and then combined.

The components for the boost engine will be calculated using the lowest operating voltage and highest operating current to stress the converter at its maximum duty cycle. Likewise, the components for the buck engine will be calculated using the highest operating voltage and lowest operating current to stress the buck engine at 50.0 % duty cycle where current stresses are at a maximum. Normally this would be done by using the values of the modules taken from Table 2, however, it does not account for over-sun and cold temperature conditions described earlier therefore the values of the components will be based off the design specifications from Table 7 summarized below in Table 8.

Table 8: Summary of Design Specifications for Boost-Buck Converter

$Cells$	$Converter\ Mode$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
36	Boost	-----	17.000	9.912	10.630	168.510
96	Buck	58.000	52.000	3.241	-----	168.510

- Appendix C shows the input and output characteristic of a 36-cell module with over-sun conditions connected to a boost converter with ideal components.
- Appendix D shows the input and output characteristics of a 96-cell module with over-sun conditions connected to a buck converter with ideal components.

4.3.4.1 Inductor

In switch mode power supplies, the main function of inductors is to store energy in its magnetic field and attempt to maintain a constant current or equivalently to limit the rate of change of current flow to the output [31]. Selecting an inductor is very important in the overall design of the converter as there are many tradeoffs associated with this choice. For example, the higher the inductor value, the higher the possible maximum output current because of the reduced ripple current but the larger the size and lower the frequency. On the other hand, the lower the inductor value, the lower the maximum output current because of the increased ripple but smaller size and higher the frequency. Depending on whether a boost converter or buck converter is being designed, there are different requirements needed for each topology. Since the chosen topology is boost-buck, the requirements must be able to work with both engines.

Normally the value of inductance of either a boost converter or buck converter is selected to limit the peak-to-peak ripple current flowing to the output. However, since the design is a high efficiency boost-buck converter, the requirements for the inductor are stricter and must meet the following criteria:

- The inductor must operate at the chosen switching frequency.
- Low DC resistance (DCR) in the windings of the inductor to reduce I^2R losses.
- Peak current should be less than the saturation current as to minimize core losses.
- Inductance at the maximum current must be sufficient to generate a low ripple current. Low ripple current will allow smaller output capacitance to be used while still achieving the desired output ripple voltage.
- The inductor must be able to handle the average DC and peak current to ensure that it does not overheat or saturate. Saturation is especially bad because in over-current or short

circuit conditions, the inductor may have currents greater than twice the normal maximum rated output current. This reduces the effective inductance of the inductor as the current through it increases. In such conditions, the load and MOSFETs can be damaged due to being unprotected [28].

An inductor that satisfies these requirements in both boost and buck mode conditions will be chosen. The inductance for each stage will be calculated and the largest inductance of the two stages will be used for the remainder of the design.

4.3.4.1.1 Boost Mode

For the boost stage of the DC/DC converter, the estimated value of inductance is given by the equation:

$$L = \frac{V_{in} * D}{f_{sw} * \Delta I_L}$$

Where:

$L = Inductance\ (H)$
$V_{in} = Minimum\ input\ voltage\ (V)$
$D = Duty\ cycle$
$F_{sw} = Switch\ frequency$
$\Delta I_L = Inductor\ current\ ripple\ (A)$

Since the inductor current ripple is unknown, it must be estimated using the equation:

$$\Delta I_L = (0.2\ to\ 0.4) * I_{out} * \frac{V_{out}}{V_{in}}$$

Where (0.2 to 0.4) is the percent of ripple based on the output current that is deemed acceptable. A value of 40.0 % output current will be acceptable in this design. Using the information given, the inductor ripple can be calculated to be:

$$\Delta I_L = (0.4 * 2.905\ A) * \frac{58.0\ V}{17.0\ V} = 3.965\ A$$

Using this estimated value and calculating for the inductance gives a calculated inductor value of:

$$L = \frac{17.0\ V * 0.673}{100.0\ kHz * 3.965\ A} = 28.86\ \mu H$$

By using these equations and plotting the inductance over the entire duty cycle range, it can be seen that 28.86 µH is the largest inductor value that would satisfy the boost converters operation at all duty cycles as seen in Figure 40.

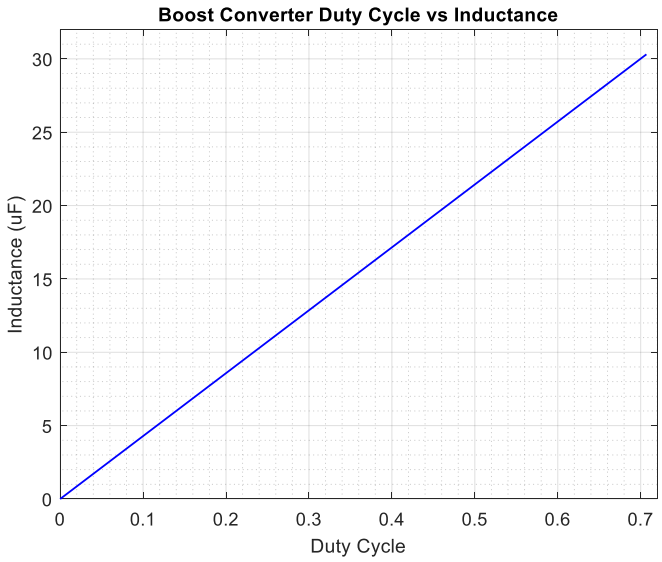

Figure 40: Boost Converter Duty Cycle vs. Inductance

4.3.4.1.2 Buck Mode

For the buck stage of the DC/DC converter, the estimated value of inductance is given by the equation:

$$L = \frac{V_{out} * (1 - D)}{f_{sw} * \Delta I_L}$$

Where:

$L = Inductance\ (H)$

$V_{out} = Maximum\ output\ voltage\ (V)$

$D = Duty\ cycle$

$F_{sw} = Switch\ frequency$

$\Delta I_L = Inductor\ current\ ripple\ (A)$

Once again, the inductor current ripple is unknown, therefore it must be approximated using the following equation:

$$\Delta I_L = (0.2\ to\ 0.4) * I_{out(\max)}$$

Where just like in the boost stage, 40.0 % output current ripple will be acceptable. Using the information given, the inductor ripple current at 50.0 % duty cycle is calculated to be:

$$\Delta I_L = (0.4 * 6.482\ A) = 2.593\ A$$

Substituting this estimated ripple current back into the buck converter inductance equation gives an inductor value of:

$$L = \frac{26.0\ V * (1 - 0.50)}{100.0\ kHz * 2.593\ A} = 50.14\ \mu H$$

Using these equations and plotting the inductance over the entire duty cycle (Figure 41), it can be seen that 50.14 µH is not the largest inductor that would work at all duty cycles for the buck converter. In fact, at a duty cycle of around 0.667 gives a calculated inductor value of 59.42 µH which is slightly larger than the one calculated which should be taken into consideration.

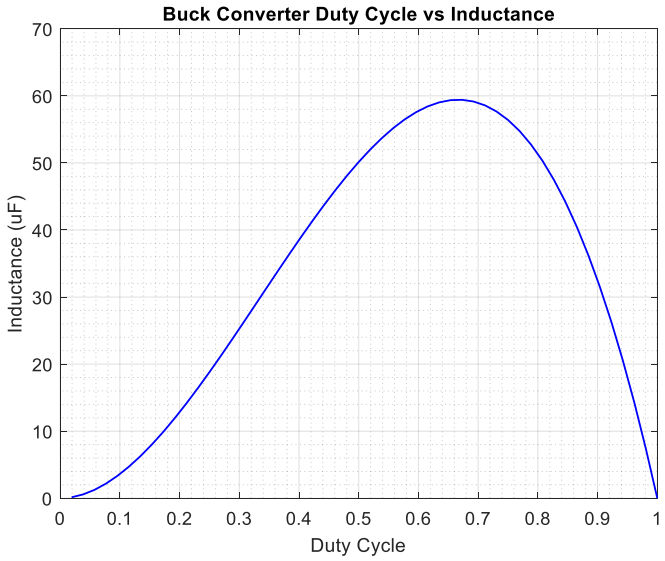

Figure 41: Buck Duty Cycle vs. Inductance

Through this exercise, two different inductors have been calculated. The inductor for the boost engine was calculated to be 28.86 µH while that of the buck engine is 50.14 µH. Both inductors could be used in this design with their respective topologies however it would make more sense to use a single inductance value for both converters. The 28.86 µH inductor will not work with the buck engine however the 50.14 µH inductor will work for both the boost and buck engine. It is a good practice to oversize the inductor slightly to give some margin for the inductors so they do not saturate. Selecting a higher inductor will generally give lower ripple current, lower core losses, lower RMS currents in the circuit and lower capacitance required to meet output ripple specifications [32]. Therefore, the inductor chosen for both engines will have a value of 60.0 µH essentially doubling the inductance calculated for the boost stage while also encompassing the 59.42 µH inductor calculated for the buck stage even when the duty cycle is 0.667. In addition to having the same inductor for both engines, it would make the boost-buck converter symmetrical thus making calculations easier.

With the new 60.0 µH inductor chosen, the new ripple current for the boost engine is calculated to be:

$$\Delta I_L = \frac{V_{in(\min)} * D}{f_{sw} * L}$$

$$\Delta I_L = \frac{17.0\ V * 0.673}{100.0\ kHz * 60.0\ \mu H} = 1.907\ A$$

While the maximum switch current on the inductor is:

$$I_{sw(\max)} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D}$$

$$I_{sw(\max)} = \frac{1.907\ A}{2} + \frac{3.241\ A}{1 - 0.673} = 10.866\ A$$

Likewise, for the buck engine, the new ripple current at 50.0 % duty cycle is calculated to be:

$$\Delta I_L = \frac{(52.0\ V - \ 26.0\ V) * 0.50}{100.0\ kHz * 60.0\ \mu H} = 2.167\ A$$

While the maximum switch current on the inductor is:

$$I_{sw(max)} = \frac{\Delta I_L}{2} + I_{out}$$

$$I_{sw(max)} = \frac{2.167A}{2} + 6.482 = 7.565\ A$$

Using Appendix C and Appendix D, the ripple current for both converters over the range of their respected duty cycles is plotted in Figure 42. These plots show that no matter the duty cycle, the ripple current for both converters with this inductor will not 2.167 A.

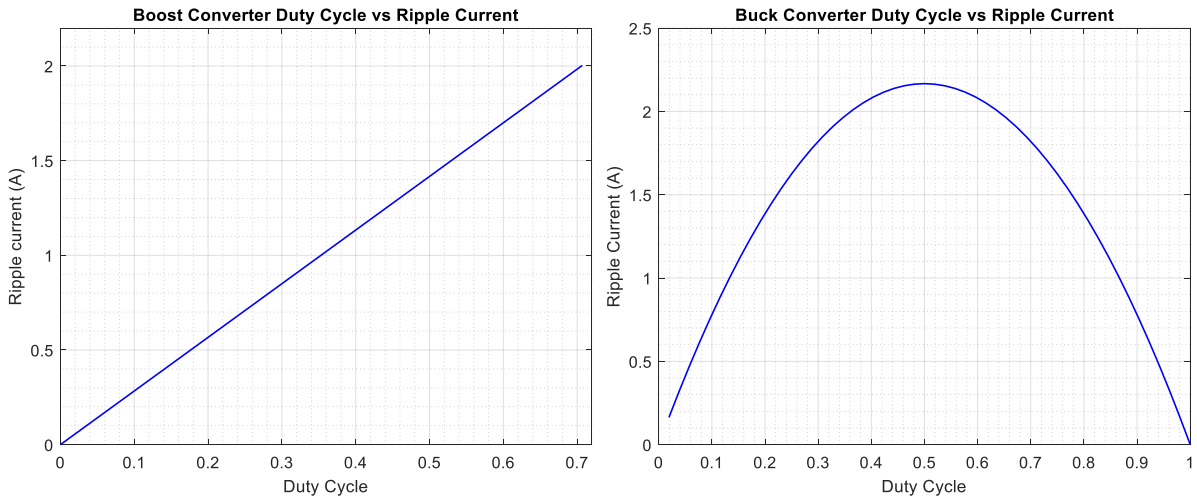

Figure 42: Duty Cycle vs. Ripple Current for Boost and Buck

4.3.4.1.3 Inductor Core and Wire

To decrease the DC conduction losses for a given inductance, a larger diameter wire for the coil should be used. To minimize the core losses a lower switching frequency should be selected. Both will result in a physically larger inductor that may be costlier but will achieve better efficiency [33]. Another consideration is the shape of the inductor. When wound around a ring or toroid, they are referred to as toroidal inductors. Since the toroid has a closed loop core, it has a higher inductance and Q factor than an inductor with straight core (solenoid) because of the symmetry, the magnetic flux leakage is very low making it a good choice for large current and high inductance [34]

Off the shelf inductors are available and usable for a first pass design. In some circumstances, it may be desirable to further optimize the inductor configuration to meet the requirements mentioned earlier. This design will require a custom inductor and will therefore be built using core with the specifications listed in Table 9.

Table 9: Inductor Core Specifications

Permeability (μ)	125.0 μ
Outer Diameter (OD)	22.9 mm
Inner Diameter (ID)	14.0 mm
Height (H)	7.62 mm
Cross Section Area (A_e)	31.7 mm^2
Path Length (l_e)	56.7 mm
Core Volume (V_e)	1800.0 mm^3

Using this information and the equation for an inductor, the number of turns can be calculated to be:

$$L = \frac{N^2 * (\mu_r * \mu_o) * A_e}{l_e}$$

Where:

$L = Inductance\ (H)$

$N = Turns$

$\mu_r = Relative\ Permeability$

$\mu_o = Permiability\ of\ free\ space = 1.26 * 10^{-6}\ Tm/At$

$A_e = Cross\ secional\ area\ of\ the\ core$

$l_e = Path\ length$

$$N = \sqrt{\frac{L * l_e}{(\mu_r * \mu_o) * A_e}}$$

$$N = \sqrt{\frac{60.0\ \mu H * 56.7\ mm}{\left(125.0 * 1.26 * 10^{-6}\frac{Tm}{At}\right) * 31.7\ mm^2}} = 26\ Turns$$

The inductor will be a toroid type inductor with 26 turns. One of the requirements is to have a low DRC to reduce I^2R losses. To do this a 16 AWG magnet wire will be used. The specifications for the wire are listed in Table 10.

Table 10: Inductor Wire Specifications

Gauge (AWG)	16.0
Diameter	1.36652 mm
Radius (r)	0.68326 mm
Resistance (1000.0 ft)	4.019 Ω

Knowing all the specifications for the inductor core and wire, the length of wire needed for this custom 60.0 µH inductor with 26 turns can be calculated:

$$L_{wire} = \sqrt{(N * ((4 * r) + (2 * H) + (OD - ID)))^2 + (pi * (ID + OD))^2}$$

$$L_{wire} = \sqrt{(26 * ((4 * 0.68326) + (2 * 7.62) + (22.9 - 14)))^2 + (pi * (14 + 22.9))^2}$$

$$L_{wire} = 708.244\ mm$$

With this calculated length, the DCR of the toroid inductor can also be calculated:

$$DCR = \frac{4.019\ \Omega * 708.244\ mm}{304800.0\ mm} = 9.3\ m\Omega$$

4.3.4.2 Capacitor

Capacitors perform several functions in switch mode power supplies (SMPS) designs such as energy storage, filtering, compensation, soft-start programming, etc. [32]. Typically, in switching power supply power stages, the capacitance stores energy in the electric field due to the voltage applied and attempts to maintain a constant input and output voltage. [31]. For both a boost and buck converter, there is typically an input capacitor and output capacitor. The primary purpose of the input capacitor is to provide energy to the power stage quickly when the switches close and charges the inductor during steady state operation [35]. It also filters the input current from the source and reduces both peak current drawn from the input supply and radiated noise to the other elements of the system. Small input capacitors can produce a large ripple voltage at the input of the regulator resulting in unsatisfactory performance [36]. The output capacitor is

generally selected to limit the output voltage ripple to the level required by the specification and help with the stability of the regulator. Contrary to the ideal capacitor model, the actual physical characteristics of a capacitor create several loss mechanisms [37]. These losses nibble away at SMPS efficiency since capacitors are used in the power circuit of the SMPS to stabilize voltage and filter both the input and output noise. There are essentially three elements of the capacitor that contribute to its impedance and output voltage ripple for continuous inductor current mode operation: the equivalent series resistance (ESR), equivalent series inductance (ESL) and its capacitance (C). Since the topology chosen has a boost converter cascade with a buck converter, the input and output capacitors will be shared between the two depending on the mode of operation. Each stage has certain requirements associated with them therefore capacitors must be chosen to satisfy both modes of operation.

4.3.4.2.1 Boost Mode

In a boost converter, the input capacitor will see a continuous ripple current therefore the capacitor should be chosen to have a low ESR to minimize the voltage ripple on the input. The output capacitor will see a large discontinuous ripple current. Low ESR and low ESL capacitors are required here [32]. When the converter is operating in boost mode the equivalent circuit is sown in Figure 43.

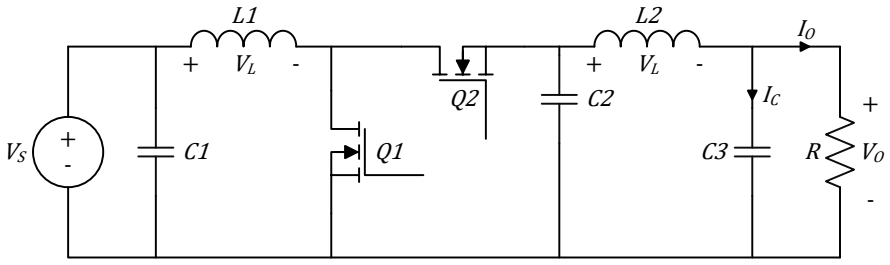

Figure 43: Synchronous Boost-Buck Converter (Boost Mode)

Notice there is an input capacitor ($C1$), an output capacitor ($C2$) and an LC filter ($L1$ and $C3$). Sometimes the DC/DC converter cannot provide adequate ripple performance on its own so a LC filter can be added to the converters output to help reduce the output voltage ripple further. Due to the nature of this topology being a boost converter cascaded with a buck converter, an output LC filter is already built into the design. Yet, an output capacitor ($C2$) is still needed for the original design of a boost converter so this value still needs to be calculated. A good rule of thumb is to have an output voltage ripple less than 75.0 mV for a boost mode DC/DC converter [38].

The maximum switching current occurs when the boost converter has a maximum duty cycle. It this case, referring to Appendix C, the input voltage is 17.0 V and the output voltage is 52.0 V with a duty cycle of 0.673. At this operating point, to match the input power, the output current was calculated to be 3.241 A with a ripple current across the inductor of 1.907 A. To solve for the output capacitor $C2$, the equation below is used assuming the output voltage ripple is 10.0 % of the total output voltage:

$$C_2 = \frac{I_{out} * D}{f_{sw} * \Delta V_{out}}$$

$$C_2 = \frac{3.241\ A * 0.673}{100.0\ kHz * (52.0\ V * 10.0\ \%)} = 4.19\ \mu F$$

An output voltage ripple of 10.0 % on the output is still very high since the desired output ripple voltage needs to be below 75.0 mV. The LC filter will attenuate the signal further and needs to be calculated so that the output voltage ripple is 100x less than that of the converter to meet the design specifications.

The LC filter acts as a voltage divider with the equation:

$$V_{\max(ripple)} = \frac{X_c}{X_c + L_c} * V_{boost(ripple)}$$

Using this equation along with the values calculated for the boost converter ripple voltage, inductance calculated earlier and knowing the desired ripple voltage, the capacitance ($C3$) can be calculated.

First the reactance of the inductor is calculated to be:

$$X_L = 2 * pi * f_{sw} * L$$

$$X_L = 2 * pi * 100.0\ kHz * 60.0\ \mu H$$

$$X_L = 37.699\ \Omega$$

Since the desired output voltage ripple is 100x less than the converter ripple voltage, the LC filter equation can be used to solve for the reactance of the capacitor:

$$52.0\ mV = \frac{X_c}{X_c + 37.669\ \Omega} * 5.2\ V = X_c = 0.3810\ \Omega$$

The reactance of the capacitor is given by the equation:

$$X_c = \frac{1}{2 * pi * f_{sw} * C_3}$$

Knowing the value of X_c of the PI filter, a value for the capacitor ($C3$) can be calculated:

$$0.3773\ \Omega = \frac{1}{2 * pi * 100.0\ kHz * C_3} = C_3 = 4.18\ \mu F$$

If the calculated capacitors are then used to plot the duty cycle vs. the output voltage ripple in Figure 44, the maximum ripple the converter will see in boost mode is 59.17 mV.

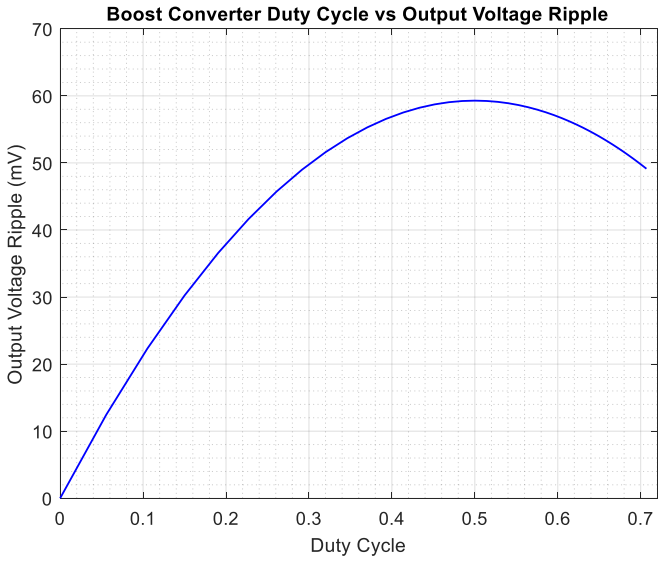

Figure 44: Boost Converter Duty Cycle vs. Output Voltage Ripple

Even though the output voltage ripple is acceptable, to reduce this further the output capacitor $C2$ and $C3$ can be increased which would in turn decrease the output voltage ripple. Therefore, for the sake of using standard capacitor values, capacitor $C2$ will be increased to 4.88 µF to reduce the output voltage ripple before the filter and capacitor $C3$ will be increased to a standard value of 4.22 µF. Plotting the duty cycle vs. the output voltage ripple with the new values gives a maximum output voltage ripple of 50.292 mV shown in Figure 45.

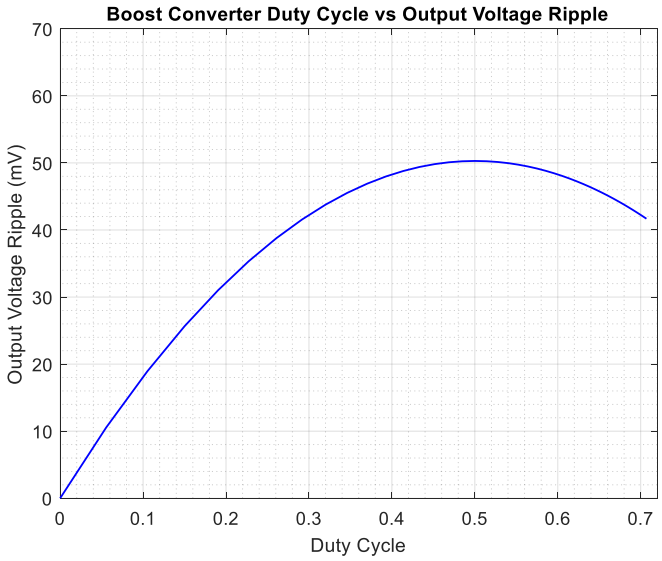

Figure 45: Boost Converter Duty Cycle vs. Output Voltage Ripple

There are no special requirements for the input capacitor. Its size is dependent on the source impedance of the application. In this case, the input source is a current source (PV module) with a finite current capacity and finite resistance so an input capacitor is used to store charge and smooth out the current drawn from the source. Since there is a continuous ripple on the input from the source, the input capacitor is chosen based on its ESR and current rating rather than its capacitance value. As with the output capacitor, low impedance at the switching frequency is what's important to minimize the input ripple current that the source sees. The best practice is to use a low ESR capacitor. Due to the symmetry of the boost-buck converter, the calculated output capacitance for $C3$ will also be a sufficient value for the input capacitance $C1$ where $C1 = C3 = 4.22\ \mu F$ for the boost stage of the boost-buck converter.

4.3.4.2.2 Buck mode

In a buck converter, the input capacitor will see a large discontinuous ripple current. This capacitor needs to be rated for high ripple currents meaning low ESR and low ESL values. If the input capacitor ESR is too high, this will cause I^2R power dissipation within the capacitor [32].

This will reduce the converter efficiency and potentially overheat the capacitor. The discontinuous nature of the input current will also interact with the ESL causing voltage spikes on the input. This will introduce unwanted noise into the system. The output capacitor in a buck converter will see continuous ripple currents which are generally low. The ESR should be kept low for best efficiency and load transient response. When the converter is operating in buck mode the equivalent circuit is sown in Figure 46.

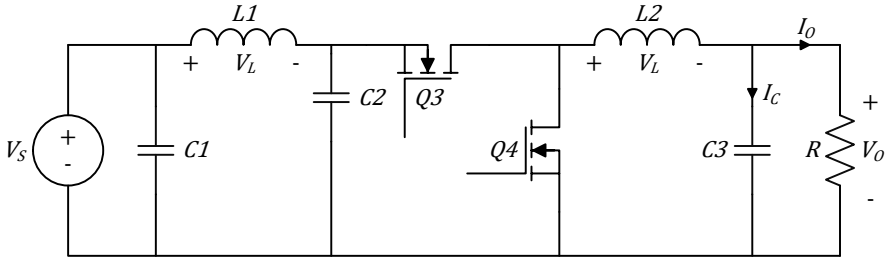

Figure 46: Synchronous Boost-Buck Converter (Buck Mode)

In this mode, the maximum switching current occurs when the converter is operating at 50.0 % duty cycle. The output capacitor for the buck mode is calculated using the equation:

$$C_3 = \frac{\Delta I_L}{8 * f_{sw} * \Delta V_{out}}$$

The ripple current will be greatest at a duty cycle of 50.0 %. At this duty cycle, and assuming 10.0 % voltage ripple on the output, the output capacitance ($C3$) is calculated to be:

$$C_3 = \frac{2.167\ A}{8 * 100.0\ kHz * (26.0\ V * 10.0\ \%)} = 1.04\ uF$$

If the output capacitor is plotted vs. the duty cycle in Figure 44, it can be seen that the maximum highest capacitance occurs when the duty cycle is at the absolute minimum. However, the converter will rarely be operating at such low duty cycles so the minimum capacitor to be chosen will be at 50.0 % duty cycle where the switch current is at a maximum.

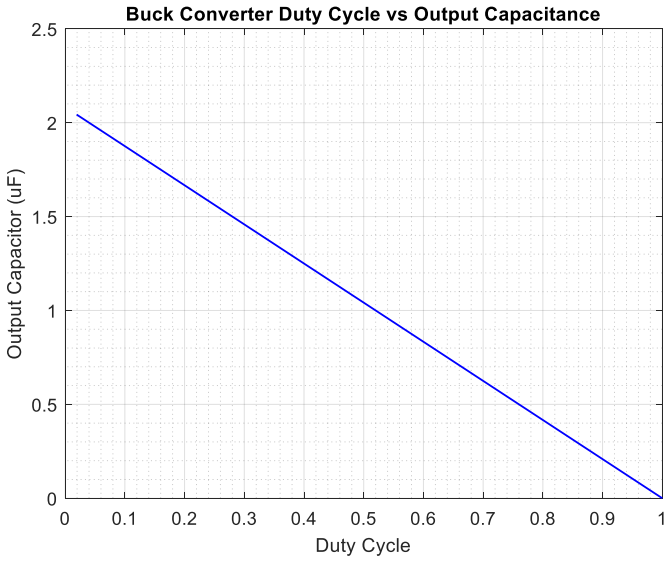

Figure 47: Buck Converter Duty Cycle vs. Output Capacitor

This capacitor value for $C3$ assumes an output voltage ripple of 10.0 % which may be too high. To reduce this output voltage ripple further, a larger capacitor needs to be chosen. $C3$ was already calculated for the boost converter to be 4.22 µF. Using this value instead of 1.04 µF at a 50.0 % duty cycle yields a new output voltage ripple of:

$$\Delta V_{out} = \frac{2.167\ A}{8 * 100.0\ kHz * 4.22\ \mu F} = 641.785\ mV$$

Not only does this capacitor lower the output voltage ripple of the buck converter, it also proves that it will work for both modes of operation. If the output voltage ripple vs. duty cycle is plotted from the data in Appendix D, Figure 48 confirms that the maximum output ripple will occur when the duty cycle is 50.0 % with a value of 641.785 mV.

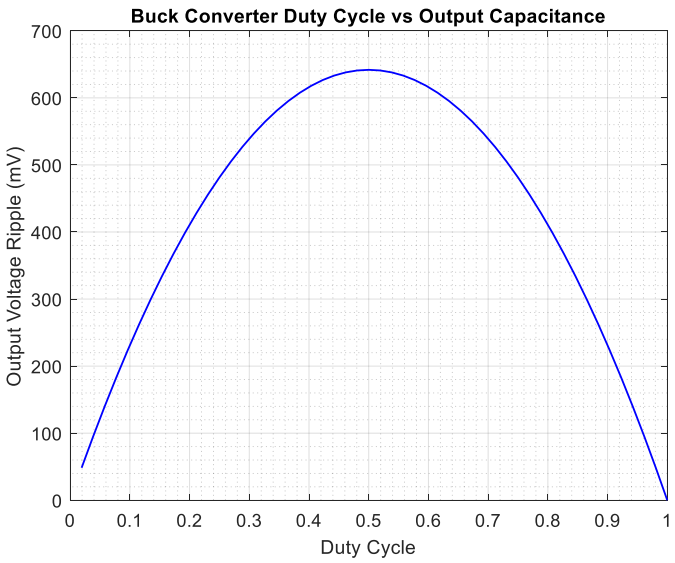

Figure 48: Buck Converter Duty Cycle vs. Output Capacitance

Once again, just like the boost converter, the buck converter input capacitance is chosen based on its ESR and current rating rather than its capacitance value as it is important to minimize the input ripple current that the source sees. This value was calculated in boost mode and chosen to be $C2 = 4.88\ \mu F$.

4.3.4.2.3 Capacitor Type

To reduce power loss due to capacitors, each capacitor ($C1$, $C2$ and $C3$) need to have low ESR values in order to have a small output deviation during transient load steps and low output voltage ripple. The output ripple is made up of two components: the ripple caused by the output capacitor discharging when the inductors are being charged and the ripple caused by the inrush current from the inductor into the ESR of the capacitors. The input and output capacitors will see continuous ripple currents so low ESR and low ESL capacitors need to be used with this topology. 100.0 kHz switching frequency is relatively low so ESL of the capacitors will hardly play a roll.

Selecting the right capacitor is though as each type has different characteristics that can drastically affect the performance of the converter. Below is a list of just a few common capacitors along with the advantages and disadvantages associated with them.

- Aluminum Electrolytic Capacitors
    - Advantage – These capacitors have large values at a very low cost. They also have a high ripple current survivability meaning that high ripple currents will not damage these capacitors.
    - Disadvantage – They have a high ESR which can be on the order of several ohms. In addition, they rely on an electrolyte which can dry out over time thus reducing the lifespan of the capacitor.
- Tantalum Capacitors
    - Advantage – The ESR of these capacitors is in the 100.0 mΩ range which is relatively small. They have a longer lifespan than aluminum and offer large values in smaller packages than aluminum.
    - Disadvantage – They respond violently to large instantaneous voltage steps and high current surges [39]. Sometimes they require a series resistance to limit inrush currents. These capacitors also cost more than all other capacitors on the market.
- Multi-Layered Ceramic Capacitor (MLCC)
    - Advantage – These have extremely low ESR values sometimes less than 10.0 mΩ all in a small surface mount package. They are available in sizes up to 100.0 µF with different types of dielectric materials. X7R and X5R dielectric capacitors have a better voltage coefficient and should always be chosen if stability is an issue.

- Disadvantage – Depending on the dielectric chosen, the capacitance will vary with the applied voltage called the voltage coefficient and can be very large. Y5V and X5R dielectric capacitors have poor voltage coefficients and can lose up to 80.0 % of their capacitance at their rated voltage and should not be chosen.

- Film Capacitors
  - Advantage – These capacitors have excellent thermal and electrical stability meaning unlike ceramic capacitors the capacitance does not change due to varying temperature and voltage. They have high current handling capability which is needed to work with high frequency ripple current up to 100.0 kHz. They also have relatively low ESR and ESL values much like ceramic capacitors. To protect the load, capacitors in the output filter deal with voltage and pulses with rapid voltage changes that lead to strong peak currents meaning high dv/dt. Luckily film caps have high pulse handling capability making them ideal for switch mode power supply applications. Also, capacitors must be able to withstand recurring and non-recurring peak voltage, which are induced by switching or any other disturbance of the system. Peak voltages could be 50.0 % higher than the capacitor rated voltage. Therefore, low ESR values, high RMS current capability, high insulation resistance, relatively high capacitance values, and self-healing are requirements this cap has and is idea for DC/DC converter applications [40].
  - Disadvantage – These capacitors cost a lot when compared with other capacitors such as ceramic and electrolytic capacitors. They have a limited range of values to choose from so if smaller values are needed film capacitors may not be the best option. Also, they are very large and take up a lot of real-estate on any printed circuit board.

To reduce power loss, ceramic capacitors with low ESR values are desired. However, this leads to a much higher cost in a boost-buck converter design. ESR on the other hand may also add additional output ripple if not selected properly. Therefore, it may be wise to use several capacitors in parallel to build a larger capacitance and reduce the ESR and ESL in addition to sharing the current to ensure reliable operation [32]. In this design, each capacitor ($C1$, $C2$ and $C3$) will be put in parallel with each other in order to increase the capacitance and reduce the ESR value. Ceramic capacitors will be selected to limit the amount of ripple voltage. Then bulk capacitors will be selected to minimize deviations in the input and output voltage should a large load transient occur [35].

Each capacitor $C1$, $C2$ and $C3$ will use a combination of ceramic and film capacitors shown in Figure 49. For $C1$ and $C3$ four 1.0 µF capacitors will be paralleled together to make up the bulk capacitance to ensure a stable voltage during large load transients. A smaller 0.22 µF ceramic capacitor will be placed in parallel with the bulk capacitors to minimize the voltage ripple the bulk capacitors see thus greatly increasing the bulk capacitors lifetime. Similarly, $C2$ will have the same four 1.0 µF capacitors but will include four 0.22 µF ceramic capacitors. $C2$ has more ceramic capacitors because this point has the largest voltage ripple for both boost converter and buck converter. The ceramic capacitor used has the specifications in Table 11.

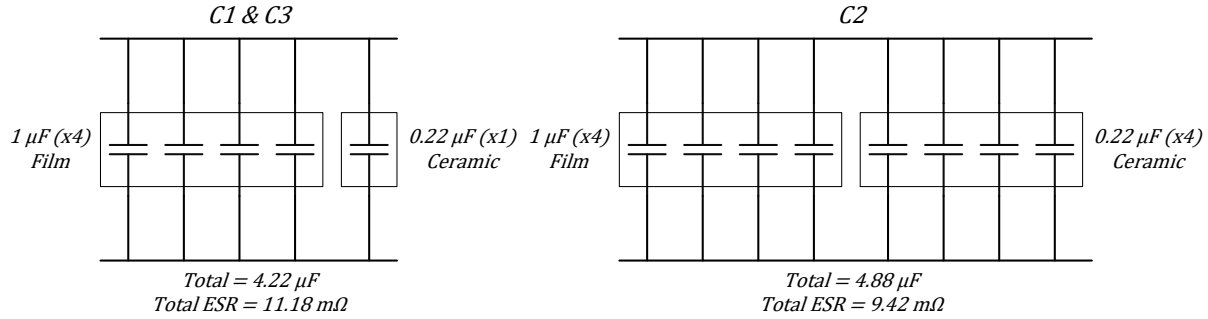

Figure 49: Equivalent Capacitor Network of Boost-Buck Converter

Table 11: Ceramic Capacitor Specifications

Capacitance (C)	0.22 µF
Voltage Rating	250.0 V
Dielectric	X7R
Dissipation Factor (DF)	0.025
Package	1210

To calculate the ESR of the ceramic capacitor the following equation is used:

$$ESR_{ceramic} = \frac{DF}{2 * pi * f_{sw} * C}$$

$$ESR_{ceramic} = \frac{0.025}{2 * pi * 100.0\ kHz * 0.22\ \mu F} = 180.0\ m\Omega$$

The film capacitors have the specifications listed in Table 12.

Table 12: Film Capacitor Specifications

Capacitance (C)	1.0 µF
Voltage Rating	63.0 V
Dielectric	PET
Dissipation Factor (DF)	0.030
Package	1210

The ESR of the film capacitor is calculated to be:

$$ESR_{film} = \frac{0.030}{2 * pi * 100.0\ kHz * 1.0\ \mu F} = 47.7\ m\Omega$$

4.3.4.3 Power MOSFETs

In switching power supply power stages, the function of the power switch is to control the flow of energy from the input power source to the output voltage [31]. The switch in switching power supplies is generally a MOSFET. MOSFETs come in two main varieties, N-channel and P-channel. Both have their advantages and disadvantages. N-channel MOSFETs

require a positive gate-to source voltage for turn on, have lower on resistance than P-channel and are less expensive. P-channels devices require a negative gate-to source voltage for turn on, have higher on resistance, and are a bit more expensive. Because of the positive gate-to-source voltage requirement, N-channel devices tend to be more difficult to drive, as the gate may need to be driven above the main supply in the system. This is usually handled by a simple gate-drive circuit; however, this adds cost and complexity to the system. P-channel devices, on the other hand, are much easier to drive and no additional circuitry is required. The consequence is that it costs more and has a higher on resistance.

In addition to choosing the type of MOSFET, there are several important parameters to pay attention to that defines the power loss and efficiency of the converter. The key parameters of a MOSFET are (R_{dson}, Q_g, I_d, V_{ds} and V_{gs}):

- R_{dson} is the on resistance of the device when the gate is driven and the MOSFET is turned on. This is the resistance in ohms exhibited across the channel between the drain and the source.
- Q_g is the gate charge of the MOSFET. This is the amount of charge that is required during the MOSFETs turn-on and turn-off transitions. The switching speed depends on the speed at which a gate driver can charge or discharge the input gate charge.
- I_d is the drain current. This is the maximum continuous current the device can carry when the device is fully turned on.
- V_{ds} signifies the breakdown voltage of the MOSFET. It is the maximum drain-to-source voltage that can be applied without causing avalanche breakdown.

- V_{gs} is the gate to source voltage. This is the voltage required to turn on the device. Like the V_{gs}, the $V_{gs(th)}$ is the minimum gate voltage that can form a conducting channel between the source and the drain and the point at which the MOSFET begins to turn on.

Power loss in a MOSFET is very important as it dictates the efficiency of the design. Power loss comes from two sources, conduction losses and switching losses. Every MOSFET has a resistive element, so it dissipates power as current is conducted through the device. These losses are proportional to the duty cycle and inversely proportional to the size of the MOSFET. The other source of power loss is through switching losses. As the MOSFET switches on and off, its intrinsic parasitic capacitance stores and then dissipates energy during each switching transition. The losses are proportional to the switching frequency and the value of the gate charge. As the size of the MOSFET increases, its capacitance increases and so does its switching loss. Therefore, at low frequencies and high duty cycles conduction losses dominate so it is important to minimize the gate charge. At higher frequency and low duty cycle switching losses tend to dominate so it is important to minimize the R_{dson} [33]. Unfortunately for a given MOSFET fabrication process, low R_{dson} devices will tend to have a higher gate-charge and vice-versa so deciding on which parameter to best optimize depends on the design requirements of the converter.

To select the optimum MOSFET, one must understand the converter and MOSFETs design requirements. For the boost-buck converter, the requirements for the MOSFET are:

- Low R_{dson} to reduce the I^2R losses within the device and increases its efficiency.
- Low gate charge and fast turn on/off switching to reduce the device switching losses.
- Must be able to handle continuous and peak current from both inductors of more than 12.0 A [41].

- V_{ds} of the MOSFET must be rated for more than 60.0 V which is greater than the voltage in the system.
- Gate to source turn on voltage of the MOSFET needs to be less than the input voltage to ensure the gate drive voltage can activate the MOSFET.
- Gate plateau must be near the middle of the gate drive range to balance turn-on/off losses.
- Low output capacitance for low switching energy to increase light load efficiency.
- Drain to source breakdown voltage large enough to handle spikes and overshoots.

Since the switching frequency is relatively low at 100.0 kHz, when selecting the MOSFET, it is better to select one with a low R_{dson} (less than 10.0 mΩ) and then find ones with a low gate charge. High voltage MOSFETs with a V_{gs} of 20.0 to 30.0 V should be ruled out for MOSFETs that are better suited to lower voltage designs. The MOFSET selected for this the boost-buck converter have the specifications listed in Table 13.

Table 13: MOSFET Specifications

MOSFET Type	N-FET
Drain to Source Voltage (V_{ds})	60.0 V
Drain to Source Resistance (R_{dson})	7.6 mΩ
Drain Current (I_d)	50.0 A
Gate Charge (Q_g)	37.0 nC
Gate to Source Voltage (V_{gs})	20.0 V
Total Power (P_{tot})	69.0 W
Rise Time (t_r)	40.0 ns
Fall Time (t_f)	5.0 ns

4.3.5 Component Losses

Each component in the power stage of the boost-buck converter dissipates power in one of two ways. Either through conduction losses which are current and duty cycle dependent, or switching losses which are frequency dependent. At lower frequencies, conduction losses are dominating and at higher frequencies, switching losses tend to take control. The inductor dissipates power in its DCR and in its core material. The input and output capacitors dissipate power in their equivalent series resistances, which is proportional to the ripple current flowing through them. Finally, the MOSFETs dissipates power in their R_{dson} and in their turn on and off transitions. Since many of the power stage component losses are proportional to frequency, increasing frequency increases power loss and thus lowers efficiency. At the selected frequency of 100.0 kHz which is relatively low, conduction losses will dominate so many of the switching losses are negligible. In the previous section, the components for the power engine were calculated. This section will introduce the losses to the system and estimate the efficiency of the boost-buck converter.

4.3.5.1 Inductor

Inductor power losses are mainly a result of the DC resistance of the winding (DCR), and hysteresis within the core magnetic material. Due to the nature of the topology, when operating in either boost mode or buck mode, both inductors will be connected to the circuit at any given time and both will contribute to the losses

- Conduction Losses

  The conduction losses in the inductor are given by the following equations:

$$P_{DCR} = I_{L(rms)}^2 * DCR_L$$

$$I_{L(rms)} = I_L * \frac{\Delta I_L}{(2\sqrt{3})}$$

Where:

$I_{L(rms)} = RMS\ current\ in\ the\ inductor\ (A)$
$DCR_L = DC\ resistance\ of\ inductor\ (\Omega)$

Depending on the mode of operation, the main switching inductor will use the RMS current while the filter inductor will use the average current through the inductor. The reason being the filter inductor has so much less ripple current flowing through it that the RMS component is negligible. The conduction loss equations for both the boost and buck mode are given in Table 14.

Table 14: Inductor DCR Loss Equations

Power Loss	*Boost*	*Buck*
$P_{DCR(L1)}$	$\left[I_{L1}^2 + \left(\frac{\Delta I_L^2}{12}\right)\right] * DCR_{L1}$	$I_{L1}^2 * DCR_{L1}$
$P_{DCR(L2)}$	$I_{L2}^2 * DCR_{L2}$	$\left[I_{L2}^2 + \left(\frac{\Delta I_L^2}{12}\right)\right] * DCR_{L2}$

- Core Losses

The core loss consists of hysteresis loss and eddy current loss which occurs in all magnetic components. Core loss is difficult to compute however it can be estimated using the following equations:

$$P_{core} = PL * V_e$$

$$PL = a * B_{pk}^b * f^c$$

$$V_e = l_e * A_e$$

$$B_{PK} = \frac{L * \Delta I_L}{(N * A_e)}$$

Where:

$PL = Core\ loss\ density\ (mW/cm^3)$
$V_e = Core\ volume\ (cm^3)$
$l_e = Core\ path\ length\ (cm)$
$A_e = Core\ corss\ sectional\ area\ (cm^2)$
$B_{PK} = Half\ of\ the\ AC\ flux\ swing\ (T)$
$f = frequency\ (kHz)$
$a, b, c = Constants\ determined\ from\ curve\ fitting$

The core loss in the switching inductor is much greater than the loss in the filter inductor because the filter inductor has significantly lower ripple current flowing through it. For this reason, the core loss of the filter inductor will be omitted from the overall power loss calculations. The core loss equation for both the boost and buck mode are given in Table 15.

Table 15: Inductor Core Loss Equations

Power Loss	*Boost*	*Buck*
$P_{core(L1)}$	$\left[a * \left[\frac{L * \Delta I_{L1}}{(N * A_e)}\right]^b * f^c\right] * l_e * A_e$	$Negligible$
$P_{core(L2)}$	$Negligible$	$\left[a * \left[\frac{L * \Delta I_{L2}}{(N * A_e)}\right]^b * f^c\right] * l_e * A_e$

The constants for the selected core are:

$$a = 91.58 \quad b = 2.2 \quad c = 1.63$$

4.3.5.2 Capacitor

Contrary to the ideal capacitor model, the actual physical characteristics of a capacitor create several loss mechanisms. These losses nibble away at the converters efficiency since the

capacitors are used to stabilize the voltage and filter both the input and output noise. There are essentially three elements of the capacitor that contribute to its impedance and output voltage ripple: The equivalent series resistance (ESR), equivalent series inductance (ESL) and its capacitance (C) for continuous inductor current mode operation. For simplicity, since the switching frequency is relatively low, the ESL power loss will be neglected. Therefore, the power loss of a capacitor due to the ESR element is given by:

$$P_{cap} = I_{cap(rms)}^2 * ESR_{cap}$$

$$I_{cap(rms)} = I_L * \frac{\Delta I_L}{(2\sqrt{3})}$$

Where:

$I_{cap} = Current\ in\ the\ capacitor\ (A)$

$ESR_{cap} = Equivalent\ series\ resistance\ in\ the\ capacitor\ (\Omega)$

The ESR power loss equations for both the boost and buck mode are given in Table 16.

Table 16: Capacitor ESR Loss Equations

$Power\ Loss$	$Boost$	$Buck$
$P_{cap(C1)}$	$\left(\frac{\Delta I_L^2}{12}\right) * ESR_{cap(C1)}$	$Negligible$
$P_{cap(C2)}$	$\left(\frac{\Delta V_{ripple}^2}{ESR_{cap(C2)}}\right)$	$\left[\left(\frac{I_o}{V_{in}}\right) * \sqrt{V_o * (V_{in} - V_o)}\right]^2 * ESR_{cap(C2)}$
$P_{cap(C3)}$	$Negligible$	$\Delta I_L^2 * ESR_{cap(C3)}$

4.3.5.3 Power MOSFETs

Power dissipation in the MOSFET is composed of three main loss mechanisms. These mechanisms are the conduction loss, switching loss and the gate loss [42]. Losses in a MOSFET can occur in many ways however they are either frequency dependent or not frequency

dependent. Conduction loss is usually the largest non-frequency dependent loss in a converter operating below 500.0 kHz while switching losses and gate-charge losses are the largest contributor to frequency dependent losses [43].

- Conduction Loss

Conduction losses are due to the channel resistance (R_{dson}) which is a function of the current. When the MOSFET is turned on, MOSFETs do not behave as an ideal switch with zero impedance, they instead behave like a small resistor where the only power dissipation comes from I^2R_{dson} losses. When the switch is turned off, the device dissipated zero power and therefore has no losses. The conduction losses of the MOSFETs in a synchronous converter are given by the equation:

$$P_{cond} = I_L^2 * R_{dson} * [D \ or \ (D-1)]$$

Where:

$I_L = Current\ in\ the\ inductor\ (A)$
$R_{dson} = On\ resistance\ of\ the\ MOSFET\ (\Omega)$
$D = Duty\ Cycle$

The conduction loss equations for both the boost and buck mode are given in Table 17.

Table 17: MOSFET Conduction Loss Equations

$Power\ Loss$	$Boost$	$Buck$
$P_{cond(Q1)}$	$I_{in}^2 * R_{dson} * D$	$OFF\ (No\ Losses)$
$P_{cond(Q2)}$	$I_{in}^2 * R_{dson} * (1-D)$	$I_{in}^2 * R_{dson}$
$P_{cond(Q3)}$	$I_{out}^2 * R_{dson}$	$I_{out}^2 * R_{dson} * D$
$P_{cond(Q4)}$	$OFF\ (No\ Losses)$	$I_{out}^2 * R_{dson} * (1-D)$

- Switching Loss

Switching losses are due to the power dissipated in the turn-on and turn-off transitions. Figure 50 shows a representation of how switching losses manifest itself. During turn on there is period when there is both voltage across the device and current flowing through the device which causes ($V * I$) power dissipation within the device. [32].

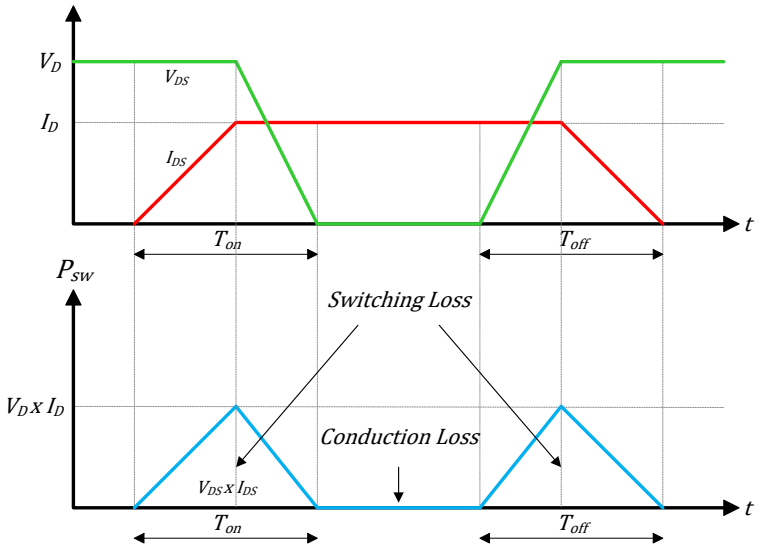

Figure 50: Switching Loss in a MOSFET

Higher frequency means more switching and more transitions through the high dissipation region of the MOSFET. Therefore, above a certain frequency these types of losses become dominant. Switching losses are difficult to calculate accurately due to the many variables associated with them but they can be estimated. Since the formula that calculates the areas of two triangles is similar to the formula that calculates the power loss during the rise and fall transitions of the MOSFET, the calculation of switching loss can be approximated using a simple figure calculation similar to the diagram in Figure 50. Switching losses can therefore be calculated using the following equation:

$$P_{sw} = \frac{1}{2} * I_{ds} * V_{ds} * (t_r + t_f) * f_{sw}$$

Where:

$I_{ds} = Drain\ to\ source\ current\ in\ the\ MOSFET\ (A)$

$V_{ds} = Drain\ to\ source\ voltage\ in\ the\ MOSFET\ (V)$

$t_r = MOSFET\ rise\ time\ (Sec)$

$t_f = MOSFET\ fall\ time\ (Sec)$

$f_{sw} = Switch\ frequency\ (Hz)$

The switching loss equations for both the boost and buck mode are given in Table 18.

Table 18: MOSFET Switching Loss Equations

$Power\ Loss$	$Boost$	$Buck$
$P_{sw(Q1)}$	$\frac{1}{2} * V_{in} * I_{in} * (t_r + t_f) * f_{sw}$	$OFF\ (No\ Losses)$
$P_{sw(Q2)}$	$Negligible$	$ON\ (No\ Losses)$
$P_{sw(Q3)}$	$ON\ (No\ Losses)$	$\frac{1}{2} * V_{in} * I_{out} * (t_r + t_f) * f_{sw}$
$P_{sw(Q4)}$	$OFF\ (No\ Losses)$	$Negligible$

The power loss of MOSFET $Q2$ for the boost side and $Q4$ for the buck side is negligible because when the MOSFET turns off, the load current continues flowing in the same direction through the body diode. Meaning this MOSFET turns on and off with its drain-source voltage equal to the body diode forward voltage drop. Therefore, the drain voltage remains low causing the switching loss to also be negligible in this application.

- Gate Loss

Gate loss is mainly caused by parasitic capacitance on the gate, both gate to source and gate to drain capacitances. These must be charged and discharged during each turn on and turn off transition to turn MOSFET on and off. Gate charge is presented by the parameter Q_g which is

the amount of charge needed to charge the gate of the MOSFET. For a given gate drive from the controller, the lower the gate-source capacitance or the total gate charge of the MOSFET, the quicker the MOSFET will turn on. Thus, the Q_g specification of the MOSFET is important and should be as low as possible. For typical low power DC/DC switching converters, Q_g is approximately 10.0 to 100.0 nC and V_{cc} is 5.0 to 10.0 V [43]. This gate charge (Q_g), together with the gate to source voltage V_{gs} that turns the transistor on, gives the energy spent every time the switch closes. Since heat is the product of voltage and current, if the gate charge is high and/or the switching frequency is high, the heat dissipation in the MOSFET will be high if the input voltage is high. Therefore, the power loss is given by the energy multiplied by the switching frequency and the total gate loss for a converter is the sum of the gate loss for each switch [43]. Gate loss can be calculated using the following equation for each MOSFET:

$$P_g = Q_g * V_{gs} * f_{sw}$$

Where:

$Q_g = Gate\ electric\ charge\ of\ the\ MOSFET\ (C)$
$V_{gs} = Gate\ drive\ voltage\ (V)$
$f_{sw} = Switch\ frequency\ (Hz)$

The gate loss equations for both the boost and buck mode are given in Table 19.

Table 19: MOSFET Gate Loss Equations

$Power\ Loss$	$Boost$	$Buck$
$P_{g(Q1)}$	$Q_g * V_{gs} * f_{sw}$	$OFF\ (No\ Losses)$
$P_{g(Q2)}$	$Q_g * V_{gs} * f_{sw}$	$ON\ (No\ Losses)$
$P_{g(Q3)}$	$ON\ (No\ Losses)$	$Q_g * V_{gs} * f_{sw}$
$P_{g(Q4)}$	$OFF\ (No\ Losses)$	$Q_g * V_{gs} * f_{sw}$

- Body Diode Conduction Loss

Body diode conduction losses are a result of the time interval when neither the upper or lower MOSFET is conducting and current flows through the body-diode of the synchronous rectifier MOSFET during this "dead time". This loss can be calculated using the following equation:

$$P_{bd} = V_{sd} * I_L * \left(t_{bd(r)} + t_{bd(f)}\right) * f_{sw}$$

Where:

$V_{sd} = Body\ diode\ forward\ voltage\ drop\ (V)$
$I_L = Current\ flowing\ through\ the\ inductor\ (A)$
$t_{bd(r)} = Body\ diode\ conduction\ time\ rising\ (ns)$
$t_{bd(f)} = Body\ diode\ conduction\ time\ falling\ (ns)$
$f_{sw} = Switch\ frequency\ (Hz)$

The body diode conduction loss equations for both the boost and buck mode are given in Table 20.

Table 20: MOSFET Body Diode Conduction Loss Equations

$Power\ Loss$	$Boost$	$Buck$
$P_{bd(Q1)}$	$Negligible$	$OFF\ (No\ Losses)$
$P_{bd(Q2)}$	$V_{sd} * I_{in} * \left(t_{bd(r)} + t_{bd(f)}\right) * f_{sw}$	$ON\ (No\ Losses)$
$P_{bd(Q3)}$	$ON\ (No\ Losses)$	$Negligible$
$P_{bd(Q4)}$	$OFF\ (No\ Losses)$	$V_{sd} * I_{out} * \left(t_{bd(r)} + t_{bd(f)}\right) * f_{sw}$

- Reverse Recovery Loss

The reverse recovery loss is a result of the charge required to recover the body diode in the synchronous rectifier MOSFET. This loss can be calculated using the following equation:

$$P_{rr} = Q_{rr} * V_{in} * f_{sw}$$

Where:

$Q_{rr} = Body\ diode\ reverse\ recovery\ (nC)$
$V_{in} = MOSFET\ input\ voltage\ (V)$
$f_{sw} = Switch\ frequency\ (Hz)$

The reverse recovery loss equations for both the boost and buck mode are given in Table 21.

Table 21: MOSFET Reverse Recovery Loss Equations

$Power\ Loss$	$Boost$	$Buck$
$P_{rr(Q1)}$	$Q_{rr} * V_{out} * f_{sw}$	$OFF\ (No\ Losses)$
$P_{rr(Q2)}$	$Negligible$	$ON\ (No\ Losses)$
$P_{rr(Q3)}$	$ON\ (No\ Losses)$	$Q_{rr} * V_{in} * f_{sw}$
$P_{rr(Q4)}$	$OFF\ (No\ Losses)$	$Negligible$

4.3.5.4 Other Losses

- Microprocessor

The microprocessors losses are due to the quiescent current of the microprocessor while the converter is in its operational mode. The microprocessor is always on and therefore these losses are static and given by:

$$P_{soc} = V_{in} * I_q$$

Where:

$V_{in} = Input\ voltage\ to\ the\ processor\ (V)$
$I_q = Quiescent\ current\ for\ the\ processor\ (A)$

From the datasheet, the microprocessor has an input voltage of 3.3 V with a quiescent current of 0.026 A. Therefore, the power loss is simply:

$$P_{soc} = 3.3\ V * 0.026\ A = 85.8\ mW$$

- Control Logic and PCB

There are other losses in the system that cannot be computed but can be estimated. These losses include power lost due to control logic, PCB traces, additional voltage regulators and measurement circuitry. These losses will be lumped into a single value that will be added on to the final power loss calculation in Appendix E and F. The additional power loss is:

$$P_{ext} = 1000.0\ mW$$

4.3.5.5 Total Losses

For each mode of operation (boost and buck), the power losses are calculated and presented in Appendix E for the boost converter and Appendix F for the buck converter. The total power loss for each converter is also presented over the entire duty cycle and output voltage range for each mode of operation for the boost-buck converter. Taking the calculated values, two plots can be generated showing the efficiency vs. the output voltage of each individual converter over their entire operating range.

- Boost engine

From the plot in Figure 51, it can be seen that the maximum calculated efficiency for the boost converter working at the extremes of its designed operating range is around 97.30 %. As the duty cycle increases, the efficiency will drop as the losses in the converter become higher. The maximum efficiency is achieved when the converter is slightly boosting its voltage and then begins to drop as losses increase due to higher output voltages and ripple currents in the system.

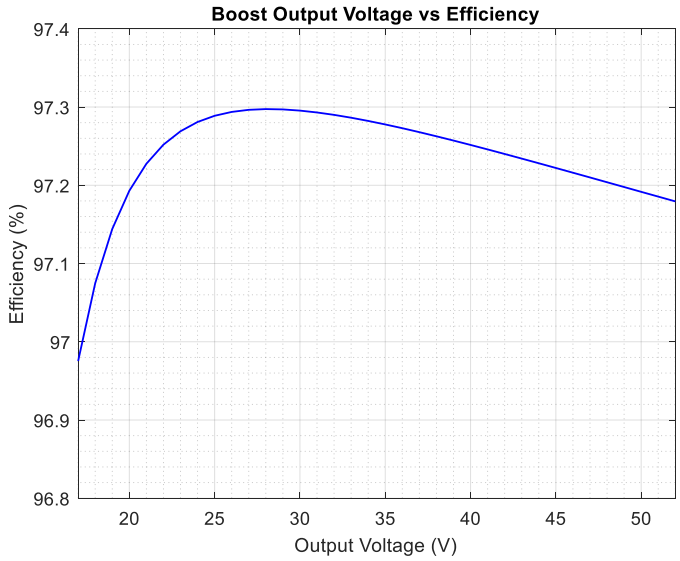

Figure 51: Calculated Boost Converter Efficiency vs. Output Voltage

- Buck engine

From the plot in Figure 52, it can be seen that the maximum efficiency for the buck converter working at the extremes of its designed operating range is around 98.74 % when the duty cycle is at its maximum. As the duty cycle decreases and current increases, the efficiency will drop as the losses in the converter become higher.

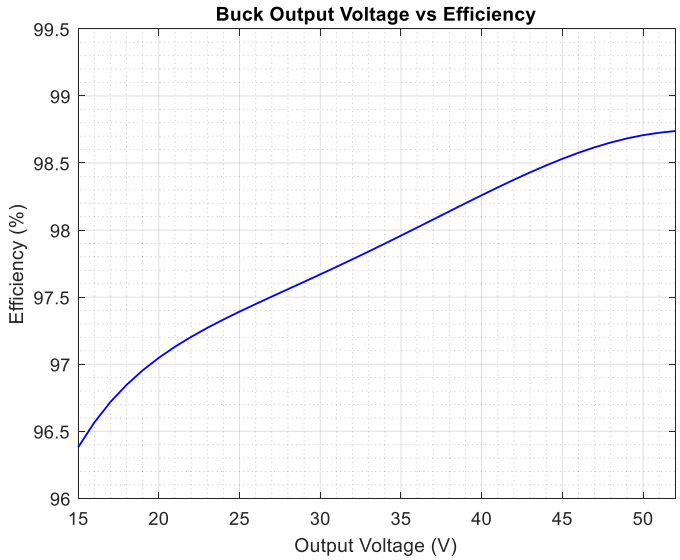

Figure 52: Calculated Buck Converter Efficiency vs. Output Voltage

The maximum efficiency when both converters are working together is when the input voltage is near the output voltage. At this point, the boost converters duty cycle will be at a minimum while the buck converter will be at a maximum. This spot is known as the sweet spot and is when the converter is neither boosting nor bucking essentially transferring the input directly to the output. The only losses in this mode of operation are the DCR of the inductors and the R_{dson} of the MOSFETs.

4.4 Control and Operation

4.4.1 General Converter Operation

As mentioned earlier in the paper, PV systems exist in many different configurations regarding their relationship to the inverter, external grid battery banks and other electrical loads [44]. Regardless of the ultimate destination of the PV power, the central problem addressed by maximum power point tracking (MPPT) is that the efficiency of power transfer from the PV cells depend on both the amount of sunlight falling on the PV modules and the electrical characteristics of the load. As the amount of sunlight varies, the load characteristic that gives the highest power transfer efficiency changes. The efficiency of the system is then only optimized when the load characteristics also change to keep the power transfer at the highest efficiency. This load characteristic is called the maximum power point (MPP) and MPPT is the process of finding this point and keeping the load characteristics there.

Every PV module has an I-V curve associated with it shown in Figure 53.

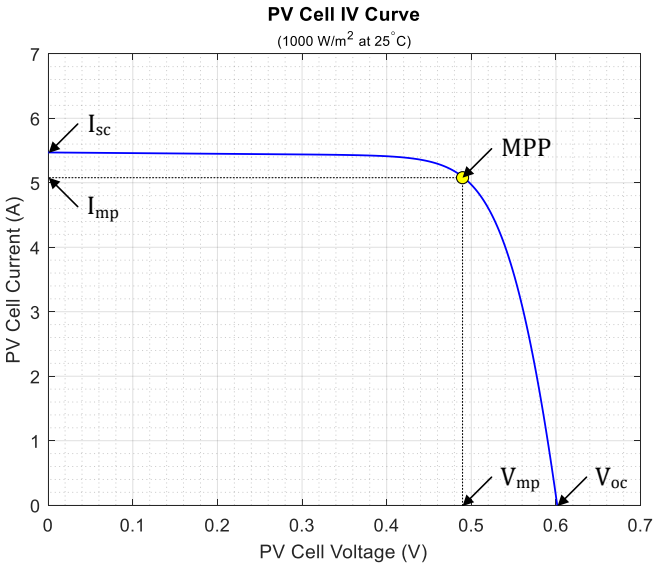

Figure 53: I-V Curve of PV Module

Normally in a typical system, a PV module would be connected to a load or several modules would be connected in series to increase the voltage which is then connected to a load. In either case, there is a maximum power point at which the module or string could be producing the maximum power to the load. For any given set of operational conditions, cells have a single operating point where the values of the current and the voltage of the cell result in a maximum power output [45]. These values correspond to a particular load resistance, which is equal to (V/I) as specified by Ohms law. This point is usually located on the knee of the curve as shown in Figure 53. If a load is chosen to operate the module at exactly this location, the maximum power would be extracted and the system would be as efficient as it could possibly be. As an example, a 72-cell module has a V_{mp} of 35.336 V and I_{mp} of 7.930 A. Using Ohms law ($V = I * R$), the ideal load for this module to operate at its maximum power point is 4.456 Ω. If the load nor the module change, this system would be working ideally with the maximum power of 280.214 W being delivered to the load. This example can be seen in Figure 54 below.

$$R_{Load} = \frac{V_{mp}}{I_{mp}} \Rightarrow \frac{35.336\ V}{7.930\ A} = 4.456\ \Omega$$

$$P_{mp} = V_{mp} * I_{mp} \Rightarrow 35.336\ V * 7.930\ A = 280.214\ W$$

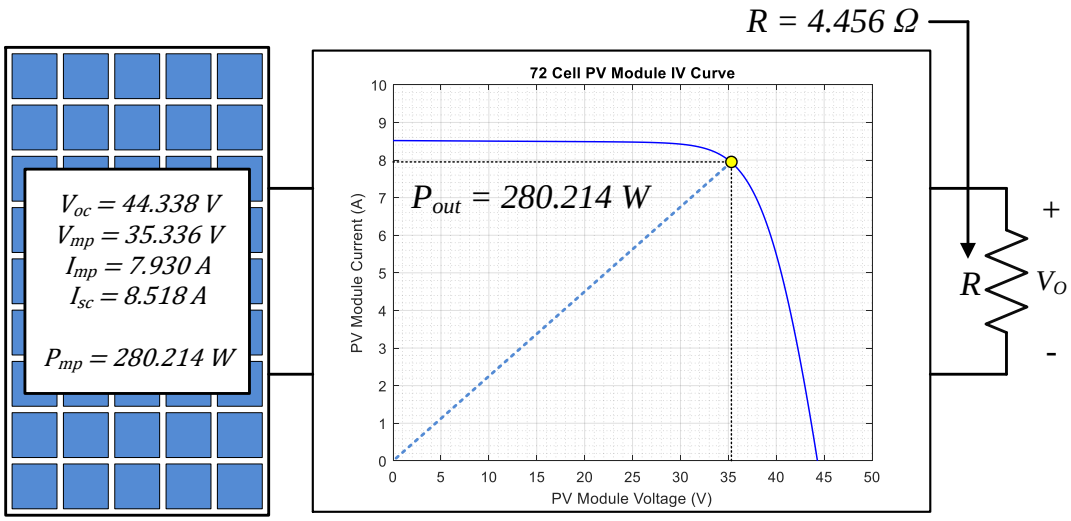

Figure 54: Conventional PV Module Connected to Resistive Load

However, due to the fluctuation of irradiance, temperature and load characteristics, this point can change and the system would not be able to extract the maximum power from the PV modules causing the overall efficiency to degrade. In a more ideal situation connecting a load directly to a module would look something more like Figure 55. In this situation, the conditions have changed where now the load has been increased to 6.0 Ω. The load wants a certain voltage and current, however, the module is unable to deliver exactly what the load requires. The voltage will ride along the I-V curve of the module to deliver the voltage required by the load but at a much less current thus reducing the amount of power the module can deliver to the load. In this case, the module will deliver approximately 41.0 V at 4.497 A which is equivalent to 184.5 W of power to the load. With this slight change in load resistance, nearly 100.0 W of power is lost due to mismatch between the module and the load.

$$P_{in} = \frac{V^2}{R_{load}} \Rightarrow V^2 = 280.214\ W * 6.0\ \Omega$$

$$V = \sqrt{280.214\ W * 6.0\ \Omega} = 41.003\ V\ and\ I = 4.497\ A$$

$$P_{out} = V * I\ \Rightarrow 41.003\ V * 4.497\ A = 184.5\ W$$

$$P_{lost} = P_{mp} - P_{out}\ \Rightarrow 280.214\ W - 184.5 = 95.714\ W$$

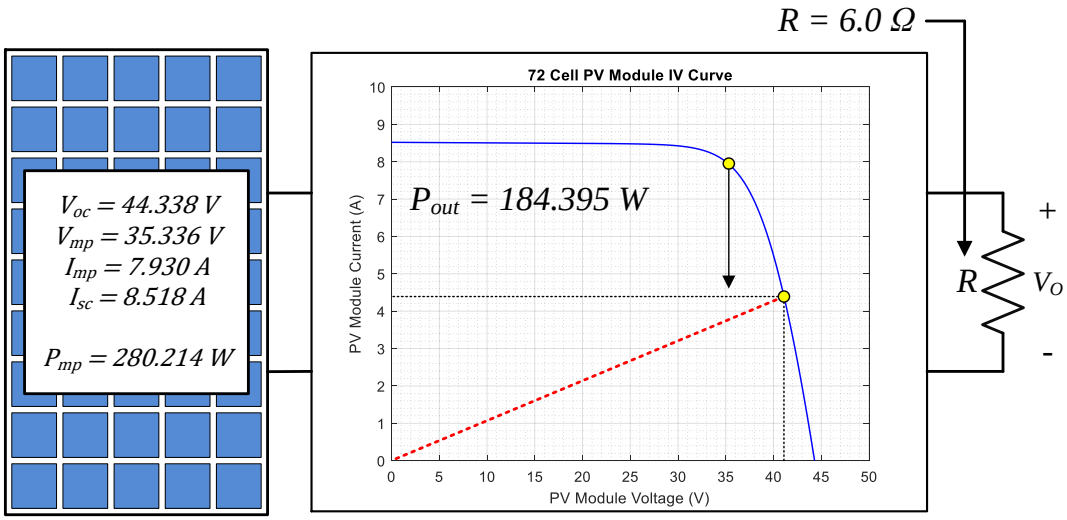

Figure 55: Conventional PV Module Connected to Changing Load

As seen in the examples of Figure 54 and Figure 55, a load with resistance ($R = V/I$) draws the maximum power from the PV module. This is sometimes called the characteristic resistance of the module. This is a dynamic quantity that changes depending on the level of illumination as well as other factors, such as temperature and the age of the cells. If the resistance is lower or higher than this value, the power drawn will be less than the maximum available, and thus the module will not be used as efficiently as it could be. In other words, the impedance seen by the PV module derives the operating point of the PV module itself.

Electrical circuits can be designed to present an arbitrary load to the PV module and then convert the voltage, current, or frequency to suit other devices or systems. Thus, by varying the impedance seen by the module, the operating point can be moved towards peak power point.

Since PV modules are DC devices, DC/DC converters must be utilized to transform the impedance of one circuit (sources) to the other circuit (load). By changing the duty ratio of the DC/DC converter, it results in an impedance change as seen by the module. At a given impedance (or duty ratio) the operating point will be at the peak power transfer point. PV cells have a complex relationship between temperature and total resistance that produces a non-linear output efficiency which can be analyzed based on the I-V curve. [46] Therefore, it is not feasible to fix the duty ratio with such dynamically changing operating conditions. It is the purpose of the MPPT system to sample the output of the PV module and apply the proper resistance (load) to obtain maximum power for any given environmental conditions [47].

Looking back at the previous examples in Figure 54 and Figure 55, the load connected to the PV module in an ideal situation changed from 4.456 Ω to a non-ideal 6.0 Ω which caused a large drop in available power that could potentially be extracted from the module. Now, by connecting a DC/DC converter, the converter varies its duty cycle and presents an arbitrary load to the module. In this case the impedance as seen by the module generated by the converter is 4.456 Ω which is the characteristic resistance of the module where the maximum power can be extracted. The converter then varies the output voltage and current moving along a constant power curve ultimately delivering the maximum power from the module to the load. In this case, the converter will output approximately 41.0 V as requested by the 6.0 Ω load and 6.834 A totaling 280.214 W of power being sent to the load which is the maximum the module can deliver. This can be seen in Figure 56.

$$P_{out} = \frac{V^2}{R_{load}} \Rightarrow V^2 = 280.214\ W * 6.0\ \Omega$$

$$V = \sqrt{280.214\ W * 6.0\ \Omega} = 41.003\ V$$

$$P_{out} = V * I\ \Rightarrow I = \frac{280.214\ W}{41.003\ V} = 6.834\ A$$

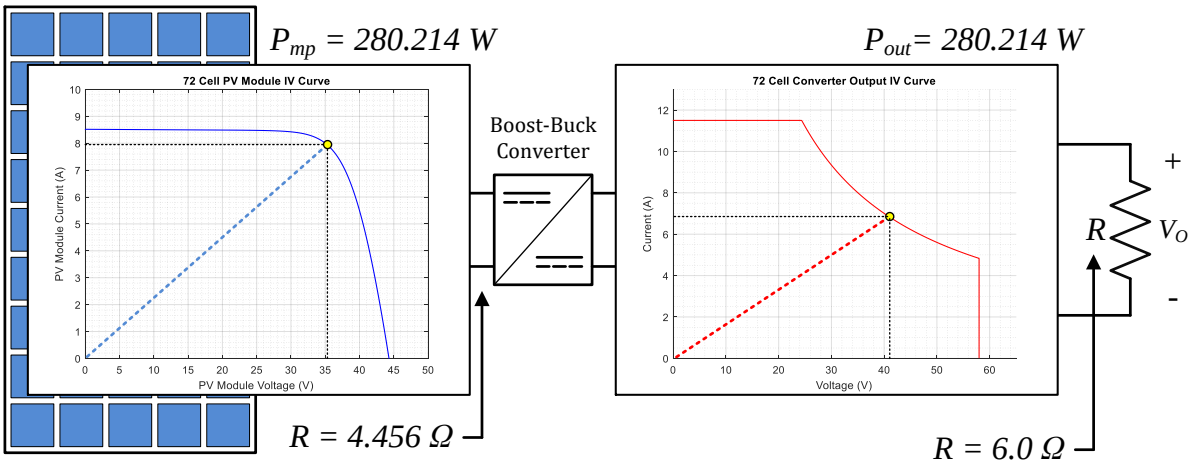

Figure 56: PV Module Connected to DC/DC Converter with Changing Load

MPPT utilizes different types of control circuits and algorithms to search for this point allowing the converter to extract the maximum power available from the PV module and deliver it to the load. These control circuits and algorithms will be discussed in detail throughout the following sections.

4.4.2 Maximum Power Point Tracking Algorithm

MPPT implementations utilize algorithms that frequently sample the PV modules voltages and currents. It then adjusts the duty ratio as needed to present an arbitrary load to the module to extract the maximum power. Microprocessors or logic circuitry are frequently employed to implement these algorithms.

There are many algorithms that can be implemented for this purpose such as incremental conductance, current sweep, constant voltage and perturb and observe. For the sake of this design, perturb and observe has been chosen as it is a common algorithm in MPP trackers.

The perturb and observe algorithm is a ‘hill climbing’ method that can find the local maximum of the power curve for the operating condition of the PV array and provide a true

maximum power point [48]. In the perturb and observe method, the controller adjusts the voltage by a small amount from the array and measures the power; if the power increases, further adjustments in that direction are tried until power no longer increases This method can be seen in Figure 57.

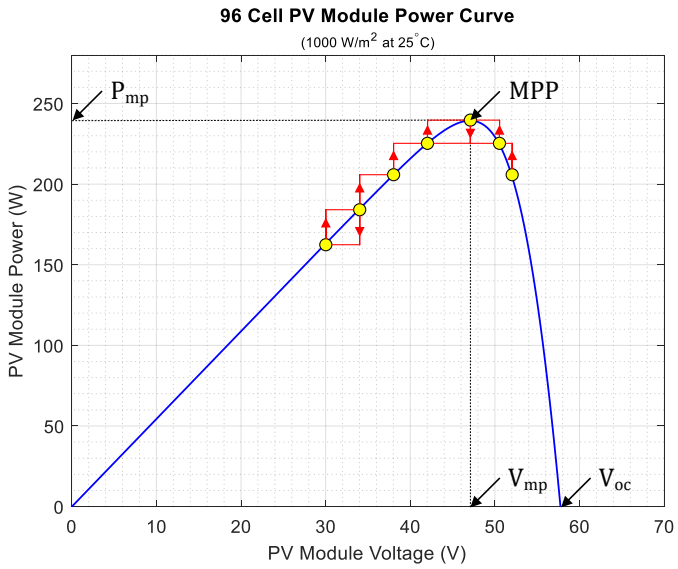

Figure 57: Perturb and Observe Algorithm at Work

Although this method can result in oscillations of power output [49], it is referred to as a 'hill climbing' method because it depends on the rise of the curve of power against voltage below the maximum power point, and the fall above that point [48]. The concept behind the "perturb and observe" (P&O) method is to modify the operating voltage or current of the PV module until you obtain maximum power from it. For example, if increasing the voltage to a module increases the power output of the module, the system continues increasing the operating voltage until the power output begins to decrease. Once this happen, the voltage is decreased to get back towards the maximum power point. This perturbation continues indefinitely. Thus, the output power oscillates around a maximum power point and never stabilizes [50]. This algorithm can be seen in the flowchart below (Figure 58).

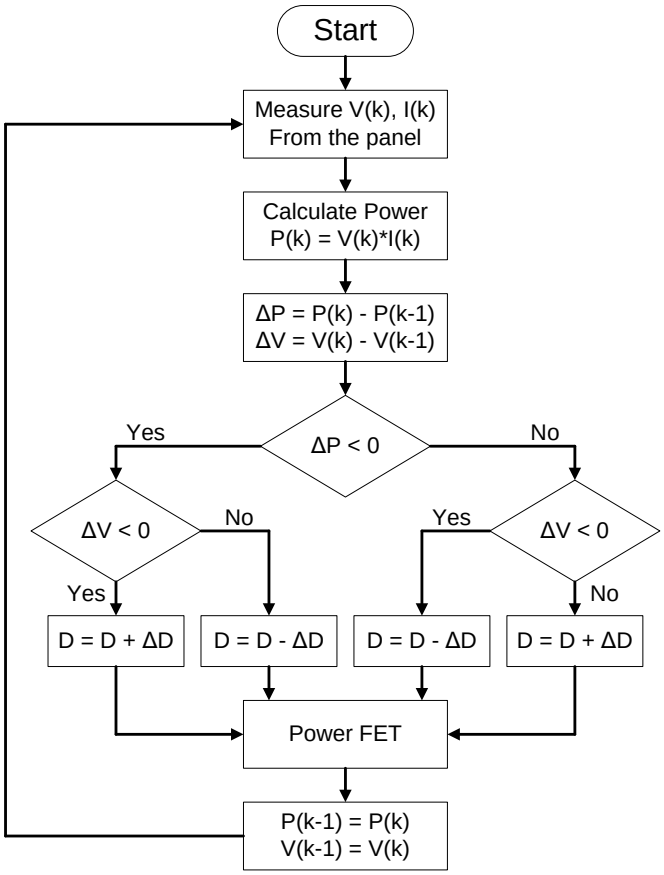

Figure 58: Perturb and Observe Flow Chart

Perturb and observe is the most commonly used MPPT method due to its ease of implementation [51]. The operating point of the PV module varies when the load condition varies. The maximum power point may be achieved through appropriate load selection. In most cases, the load is not likely to be optimal (regarding maximum power delivered from the PV module). Maximum power from the PV modules may be attained by incorporating an intelligent mechanism to alter the load resistance observed by the PV module. In a boost-buck converter the input voltage is controlled through appropriate adjustments of the duty ratio for the power MOSFETs of the converter (Figure 59).

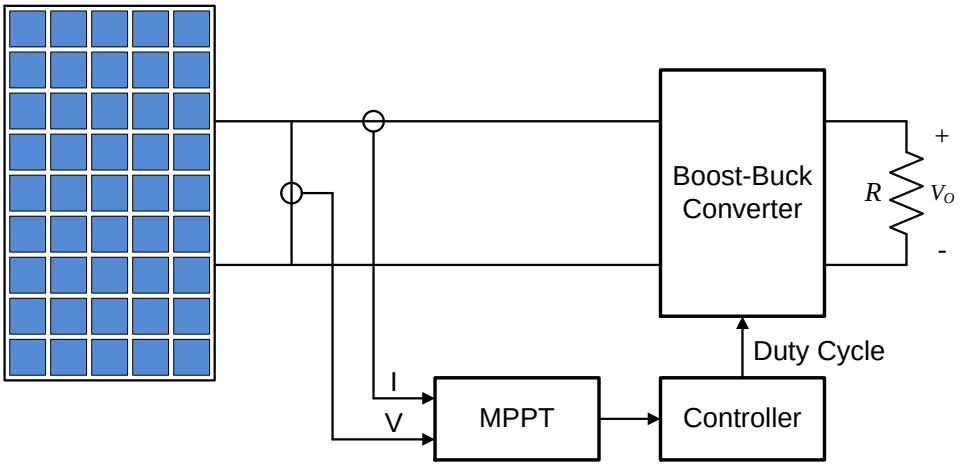

Figure 59: MPP Tracking Control Block Diagram

4.4.3 Boost-Buck Control Loop

The previous two sections explained the boost-buck converters general operation and the MPPT algorithm that is employed within the system. Diving further into detail, this section will explain how the boost-buck converter operates in a closed loop system. Appendix G shows the block diagram of the closed loop control system and how the converter chooses between boost mode and buck mode all while changing the duty cycle to track the maximum power point of the PV module.

When the converter is operating in steady state, the input voltage and input current are measured independently and sent to a multiplier generating a signal corresponding to the input power level from the PV module. This signal is then sent to an error amplifier which is compared to a reference voltage of 5.0 V. Depending on the value from the multiplier, the error amplifier has an output voltage signal from 0.0 V to 5.0 V where at a level of 0.0 V to 2.5 V, the converter is in boost mode and at a level of 2.5 V to 5.0 V, the converter is in buck mode. With an error amplifier output of 2.5 V, the converter is in a state where it is neither boost nor bucking and is in a transition between the two states also known as the ‘sweet spot’.

Once the error amplifier signal has been generated it then gets level shifted. For the boost side of the power engine, the error amplifier signal gets shifted in a way that 0.0 V now becomes 1.66 V and 2.5 V becomes 3.33 V. Similarly, for the buck side of the power engine, the error amplifier signal gets shifted in a way that 2.5 V becomes 1.66 V and 5.0 V becomes 3.33 V. The output of the error amplifier and the new level shifted voltages can be seen in Figure 60.

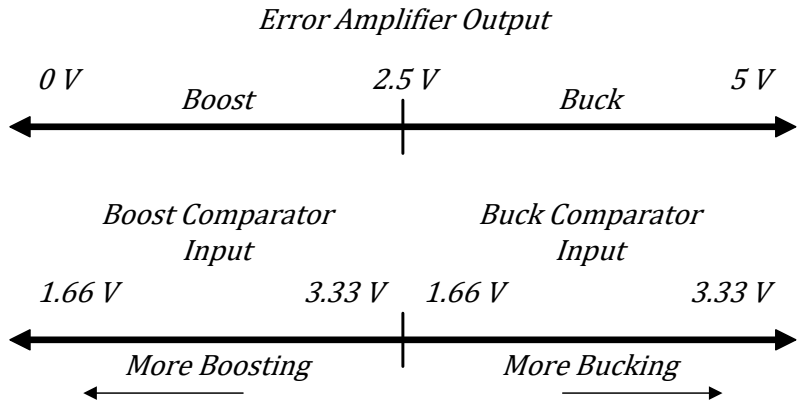

Figure 60: Error Amplifier Output and Boost-Buck Comparator Input Voltages

Once the error amplifier signal has been level shifted, it is sent to a boost comparator and a buck comparator where it is compared with a triangle waveform that has a frequency of 100.0 kHz and duty cycle of 50.0 %. The center of the triangle waveform lies at 2.5 V while the minimum value is 1.66 V and the maximum is 3.33 V. This waveform can be seen in Figure 61 below.

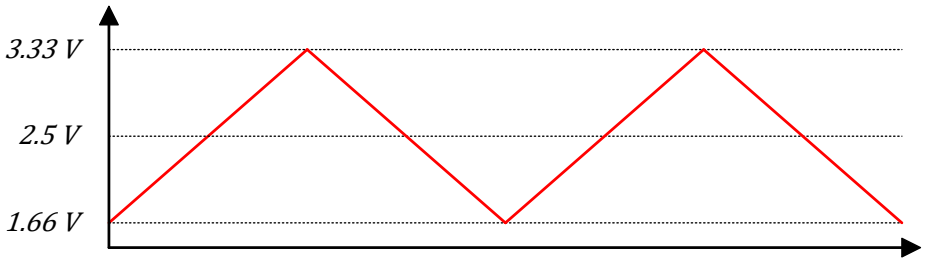

Figure 61: Boost-Buck Comparator Triangle Waveform

As the triangle waveform is being compared with the level shifted input from the error amplifier, the comparator generates a square wave on the output with a duty cycle corresponding to the intersection at which the level shifted input from the error amplifier crosses the triangle waveform. For the boost converter, this can be seen in Figure 62 where a smaller comparator input voltage means the converter will have a larger boost duty cycle corresponding to a larger output voltage compared with the input.

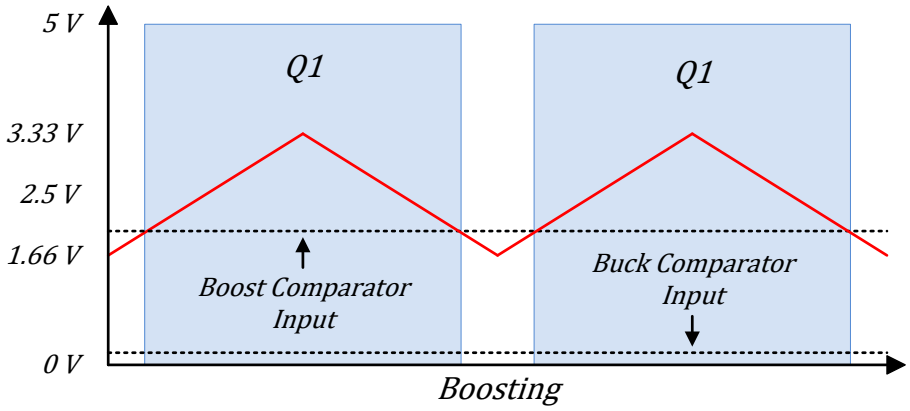

Figure 62: Boost Mode Comparator Input and Duty Cycle Generation

For the buck converter, this can be seen in Figure 63 where a larger comparator input voltage means the converter will have a smaller buck duty cycle corresponding to a smaller output voltage compared with the input.

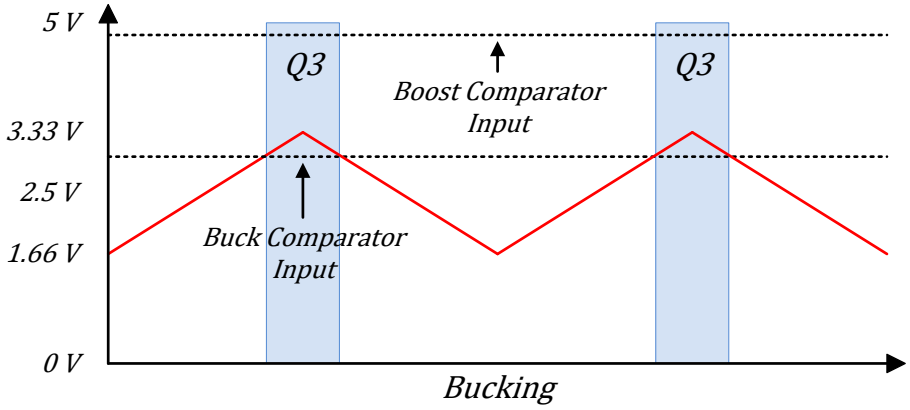

Figure 63: Buck Mode Comparator Input and Duty Cycle Generation

Due to the level shifting of the error amplifier output, only one comparator will be active at any given time. When the converter is in boost mode, the voltage level on the buck comparator input is below the level of the triangle waveform. At this moment, nothing is being compared and the buck engine is shut off (Figure 62). Likewise, when the converter is in buck mode, the voltage level on the boost comparator input is above the level of the triangle waveform and again nothing is being compared so the boost engine is shut off (Figure 63).

Depending on the mode of operation the boost-buck converter is in, the generated square wave from the active comparator is sent to the proper MOSFETs to begin switching and producing power on the output. Several times per second, the duty cycle is varied slightly and the input voltage and current are measured comparing the previous power measurement to the most recent measurement. If the most recent measured power is higher than the previous measured power, the error amplifier output voltage level varies slightly causing the duty cycle to also vary. At this moment, the input power is measured again and compared with the previous value and the duty cycle is adjusted again. This process continues until the input power stops increasing and begins to decrease meaning the maximum power has been achieved and the maximum power point of the PV module has been found. Once this point has been found, the duty cycle oscillates around this point indefinitely and never stabilizes until the conditions change.

4.4.4 Over Voltage and Over Current

PV modules come with an inherent open circuit voltage and short circuit current. Since the converter is a boost converter cascade with a buck converter, it has the ability to boost the voltage to a large value and buck the current in the same manner. This could cause multiple issues such as putting too much voltage or current into the system which can cause catastrophic

failures. If too much current is delivered, fires can spontaneously erupt or fuses can blow causing damage to various areas within the system. Likewise, if there is too much voltage on the output, the inverter could fail or potentially cause serious injury or death to anyone working on the system. In addition to these failures, the converter itself can be damaged. MOSFETs, capacitors and other components are sensitive to voltages and currents above their rated values for operation. Since the MOSFETs are only rated up to 60.0 V, any output voltage higher than this will most likely cause damage to them rendering the boost-buck converter useless.

The converter must have over voltage and over current protection so that if a certain level is detected on the output, the voltage and current will be regulated to not exceed a certain value. With the use of a microprocessor (discussed later), the output voltage and current can be measured and compared with a PWM signal generated from the microprocessor. If the output voltage or output current exceeds a certain reference value generated by the microprocessor, the main PWM generator for the MOSFETs will get bypassed and replaced with the PWM signal coming from the microprocessor until the output voltage or current become less than the reference value. The block diagram for this control loop can be seen in Figure 64.

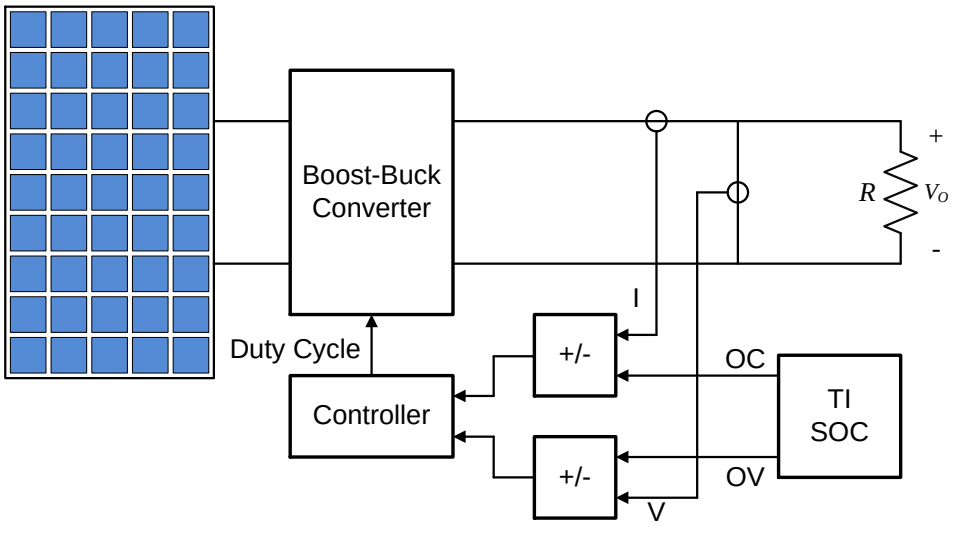

Figure 64: Over Voltage and Over Current Control Block Diagram

The PWM signal generated by the microprocessor is an 8-bit (256 values) signal with a fixed frequency of 100.0 kHz which is the same frequency as the main switching frequency for the boost-buck converter. At this frequency, with 256 values, the step size for the duty cycle is:

$$Step = \left(\frac{1}{256}\right) * \left(\frac{1}{100000.0}\right) = 39.06\ ns$$

For the over voltage register, a value of 256 should correspond to the maximum open circuit voltage the largest module could deliver. In this case that value is around 58.0 V for a 96-cell module. A value of 0 should correspond to the maximum open circuit voltage the smallest module could deliver. In this case that value is around 23.0 V for a 36-cell module. Given these values, a linear equation can be made to represent the output voltage of the converter based on the over voltage register value. In this case one over voltage step corresponds to roughly 0.13 V.

$$V_{step} = \left[\frac{58.0\ V - 25.0\ V}{256} * (OV) + 25.0\right] \xrightarrow{yields} [0.129 * (OV) + 25.0]$$

For the over current register, a value of 256 should correspond to the maximum operating current independent of the module. In this case, the maximum output current is 11.5 A and the minimum current is 3.5 A. The minimum value is based on the 36-cell module with full over-sun current boosting to its maximum operating voltage. At this voltage of 52.0 V, the current is roughly 3.5 A. Given these values, another equation can be made representing the output current based on the over current register value. In this case one step corresponds to roughly 0.0313 A.

$$V_{step} = \left[\frac{11.5\ V - 3.5\ V}{256} * (OV) + 25.0\right] \xrightarrow{yields} [0.0313 * (OC) + 3.5]$$

4.4.5 Module On/Off and MPPT On/Off

For diagnostic reasons, or if a catastrophic event happens in the PV array, full control over the boost-buck converter is a must. The ability to completely turn off the module and

disconnect it from the output, or to bypass the converter entirely is handled by the main microprocessor must like the over voltage and over current is controlled. The block diagram for this control loop can be seen in Figure 65.

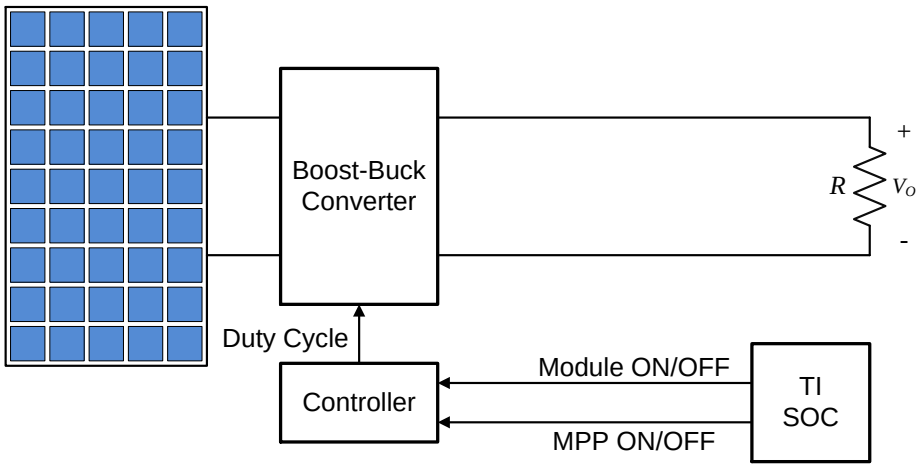

Figure 65: Module On/Off and MPP On/Off Control Block Diagram

To completely turn off the modules output, a single bit (0/1) is toggled causing the boost engines low side MOSFET ($Q1$) to be latched off and high side MOSFET ($Q2$) to be latched on. At the same time, this causes the buck engines high side and low side MOSFETs ($Q3$ and $Q4$) to be latched off. Even though the switching frequency is still active, it never reaches the MOSFETs due to the signal being bypassed thus disconnecting the output (Figure 66).

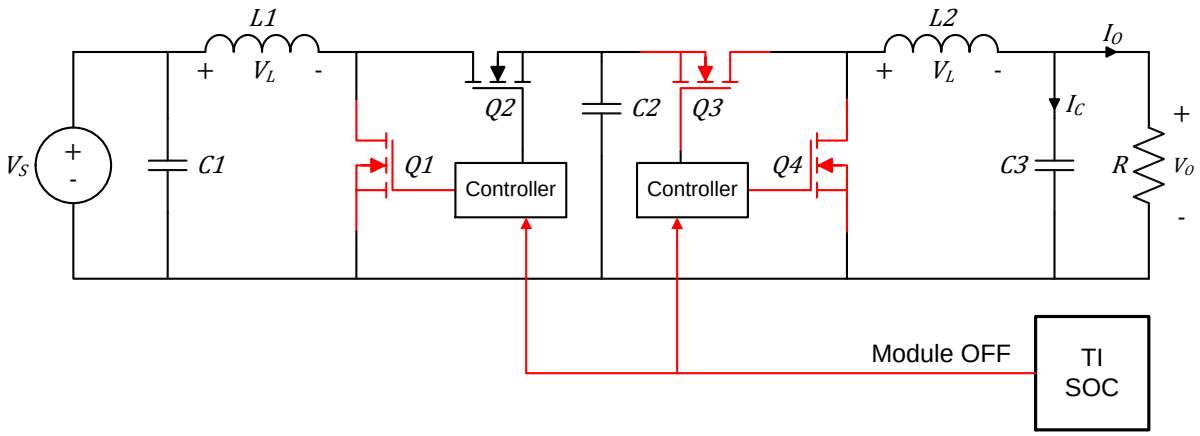

Figure 66: MOSFETs State During Module Off Conditions

To bypass the converter completely and send the modules power directly to the output, a single bit (0/1) is toggled causing the boost engines low side MOSFET ($Q1$) to be latched off and the high side MOSFET ($Q2$) to be latched on. At the same time, this causes the buck engines high side MOSFET ($Q3$) to be latched on and the low side MOSFET ($Q4$) to be latched off. This essentially turns off the MPPT circuit allowing the power from the module to be directly sent to the output. In this mode, it is as if the converter is not present in the system at all (Figure 67).

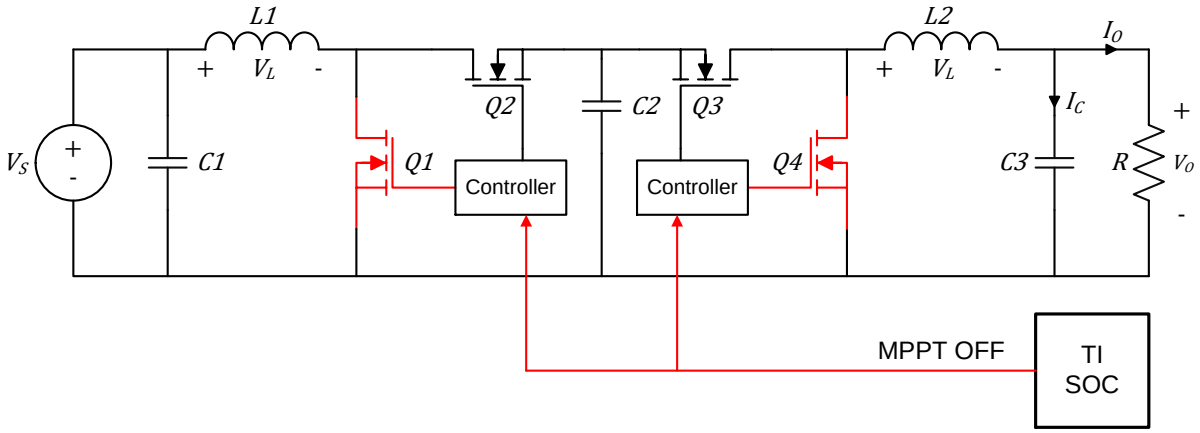

Figure 67: MOSFETs State During MPP Off Conditions

4.5 Microprocessor Control

The brains behind the converter is the microprocessor. The central processing unit (CPU) has several requirements for the boost-buck converter to function as specified in the design requirements. The microprocessor must be able to:

- Transmit and receive select commands to turn the module on and off, MPPT on and off, and set over voltage and over current limits.
- Measure and transmit all real-time data regarding input and output power values.
- Generate PWM signals for the over voltage, over current and MPPT frequency.

There are only a few requirements, but they are extremely important when it comes to the safety of the converter and the system it is connected to. The market is saturated with hundreds of microprocessors so choosing the right one is important. For this design, since cost is an issue, a relatively inexpensive microprocessor has been selected. This microprocessor is a complete system on a chip (SOC) that includes a radio module as well as a CPU. The input and output pins of the SOC are shown in Figure 68.

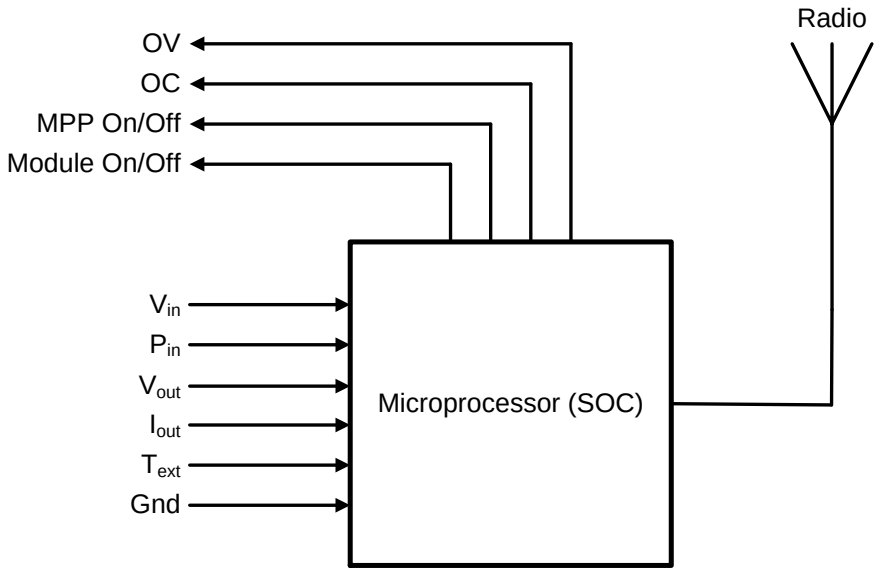

Figure 68: Microprocessor (SOC) Pinout Diagram

CHAPTER 5. RESULTS

5.1 Introduction

The results will be separated into two categories: Simulated and measured. These results will be based off the modules from the target specifications to be as close to real PV modules that exist in the world today. Using these PV modules as the input, in addition to the components calculated earlier, the boost-buck converter will be simulated using software and then measured using a printed circuit board (PCB) with real components. The converter will be simulated and measured using three different modes of operation. The first scenario will be with a 36-cell low voltage high current PV module that will test the lower limits of converter in boost mode. The next scenario will be with a 96-cell high voltage low current PV module that will test the upper limits of the converter in buck mode. Finally, a middle of the road 72-cell high power PV module will be used to test the converters ability to boost and buck with a variable load under different power inputs. In addition to the module inputs, the boost-buck converters control system will also be measured and discussed.

5.2 Simulated

The simulations will take place in a software program called NL5 Circuit Simulator. All the components that have been calculated earlier will be included and simulated based on certain operating criteria. The full schematic with control circuitry is shown in Appendix H, however, for simplicity reasons, the control circuitry will not be used in the simulation, and only the base components of the power engine with the associated losses will be included. The frequency and duty cycle will be directly sent to the MOSFETs gate without the use of any MPPT algorithm,

feedback loop, error amplifier or comparator circuitry. The circuit that will be simulated instead is shown in Figure 69.

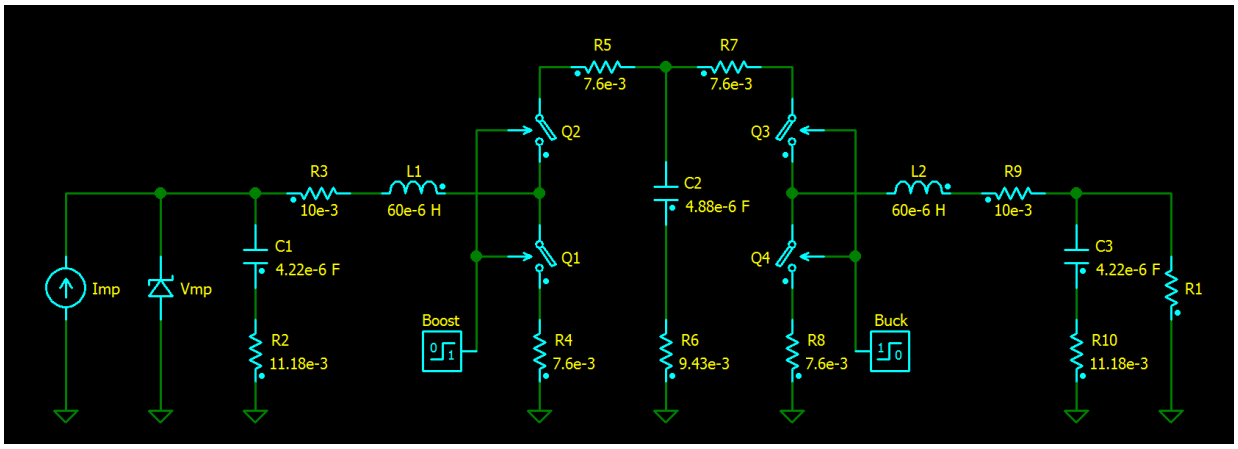

Figure 69: Simulated Boost-Buck Converter with Losses

5.2.1 Boost Mode Minimum Voltage Maximum Current (36-Cell PV Module)

The 36-cell module is the lowest voltage, highest current PV module that will stress the converters ability to boost. This module will put the boost-buck converter in the boost mode for most of its operation and allow the converter to go to its maximum duty cycle as specified in the target specifications. The PV modules input specifications to the converter are:

Table 22: 36-Cell PV Module Input Parameters for NL5 Simulation

Cells	*Cell Type*	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
36	15.6 cm^2	22.1691	17.6681	7.9299	8.5176	140.1068

The equivalent circuit to simulate the boost-buck converter in boost mode with all associated losses is shown in Figure 70. This equivalent circuit shows only the components active when the converter is in this mode of operation.

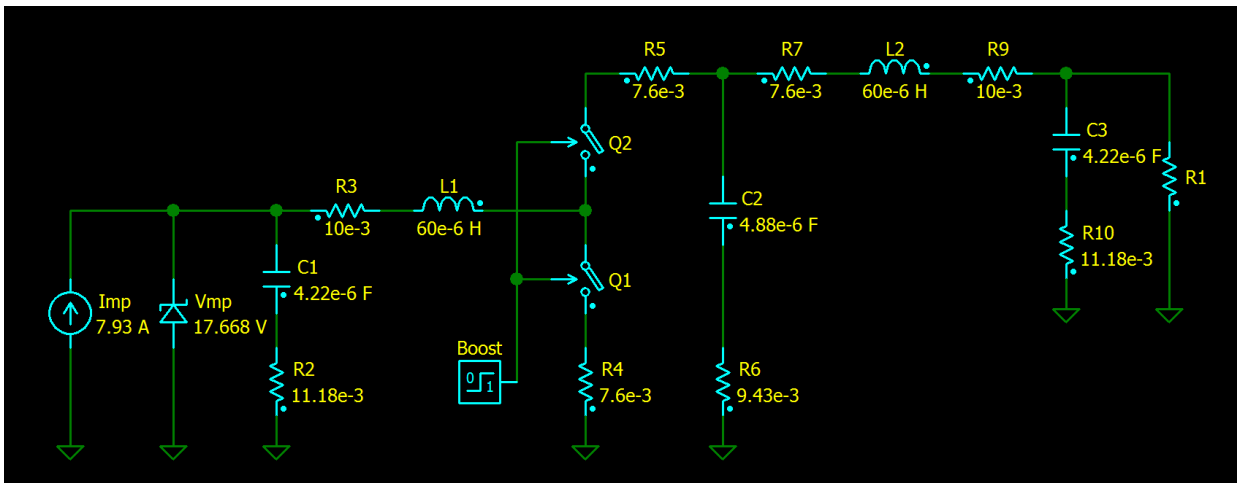

Figure 70: Simulated Boost Converter with Losses

By varying the duty cycle and the load $R1$, assuming the converter is working at the modules maximum power point, the I-V curve of the module and the output I-V curve of the converter can be simulated (Figure 71).

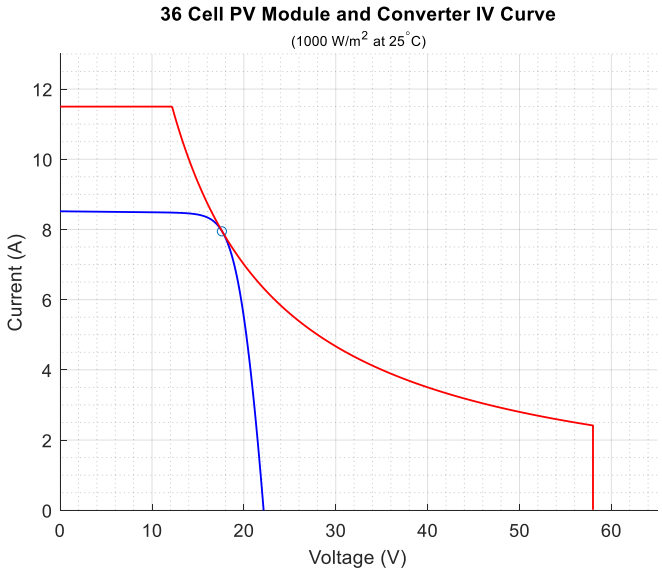

Figure 71: Simulated Boost Converter Output I-V Curve

Also by sweeping the output voltage from 52.0 V to 17.0 V and varying the duty cycle and load accordingly to maintain a constant power on the output, Table 23 can be generated.

Table 23: Simulated Data for Boost Converter Using NL5

D	$Load\ (\Omega)$	$P_{in\ (W)}$	$V_{out\ (V)}$	$I_{out\ (A)}$	$P_{diss\ (W)}$	$P_{out\ (W)}$	$\Delta I_{rip\ (A)}$	$\Delta V_{rip\ (mV)}$	%
0.660	19.300	136.094	51.000	2.643	2.641	132.129	1.924	29.104	97.086
0.647	17.843	136.111	49.039	2.748	2.594	132.181	1.884	29.786	97.113
0.607	14.453	136.171	44.139	3.054	2.465	132.334	1.771	31.448	97.182
0.558	11.420	136.268	39.242	3.436	2.321	132.528	1.628	32.841	97.256
0.495	8.743	136.434	34.350	3.929	2.159	132.790	1.445	33.430	97.329
0.411	6.424	136.719	29.464	4.587	1.981	133.160	1.200	32.078	97.397
0.293	4.461	137.213	24.585	5.511	1.798	133.691	0.856	26.417	97.433
0.117	2.855	137.886	19.699	6.900	1.649	134.266	0.341	11.770	97.374
0.018	2.313	137.832	17.716	7.661	1.622	134.095	0.054	1.893	97.288

Plotting the output voltage vs. the efficiency using the data in Table 23 shows that as the duty cycle increases, the efficiency of the converter decreases (Figure 72). This is like the calculated results (Figure 51) for the boost converter using the design specifications thus confirming that the simulated results match the calculated results. In this mode of operation, the maximum efficiency of the boost-buck converter in boost mode is 97.43 %.

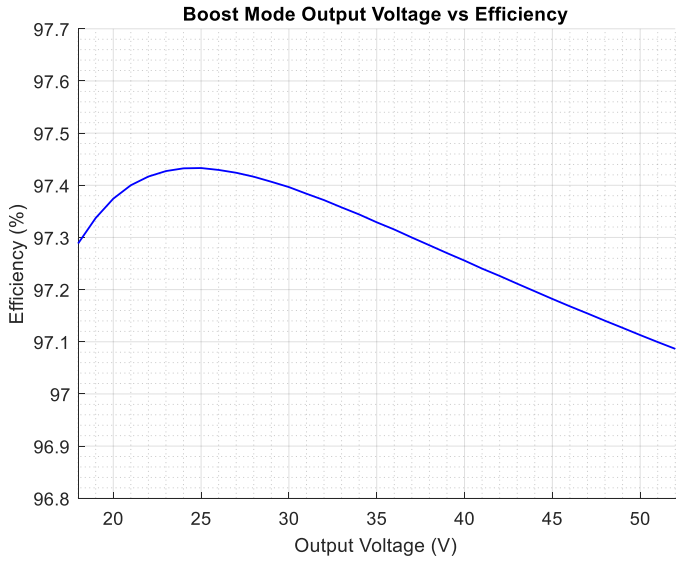

Figure 72: Simulated Boost Converter Output Voltage vs. Efficiency

Taking a looking at the worst-case scenario when the duty cycle and output voltage is at its maximum operating condition, the simulation shows the following waveform in Figure 73.

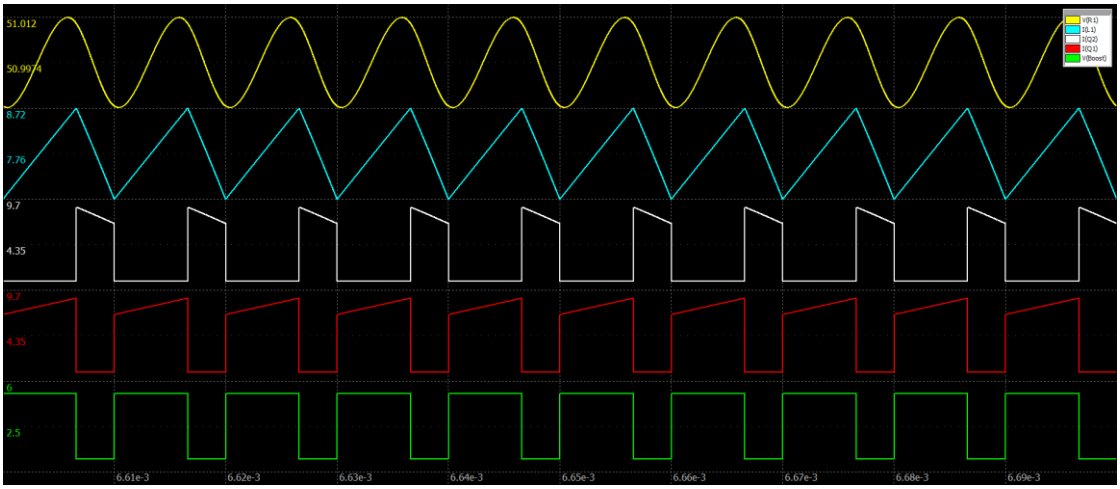

Figure 73: Simulated Boost Converter Output Waveforms at Maximum Duty Cycle

Using equations developed earlier in the paper, the simulated results (Table 23) where the duty cycle and output voltage are operating at their maximum conditions can be confirmed.

$$D_{boost} = 1 - \frac{V_{in(\min)}}{V_{out}} = 1 - \frac{17.663\ V}{52.0\ V} = 0.660$$

$$P_{in} = P_{out} = \left(V_{mp} * I_{mp}\right) = (17.663\ V * 7.93\ A) = 140.1068\ W$$

$$P_{out} = V_{out} * I_{out} = 140.1068\ W = 52.0\ V * \ I_{out} = 2.694\ A$$

$$R_{load} = \frac{V_{out}}{I_{out}} = \frac{52.0\ V}{2.694\ A} = 19.30\ \Omega$$

$$\Delta I_L = \frac{V_{in(\min)} * D}{f_{sw} * L} = \frac{17.663\ V * 0.660}{100.0\ kHz * 60.0\ \mu H} = 1.944\ A$$

$$\Delta V_{out} = \frac{I_{out} * D}{f_{sw} * C_2} * \frac{X_c}{X_c + L_c} = \frac{1.944\ A * 0.660}{100.0\ kHz * 4.88\ \mu F} * \frac{0.3771}{0.3771 + 37.699} = 36.102\ mV$$

$$P_{loss}\ @\ 52.0\ V = 3970.631\ mW$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} * 100.0 = \frac{140.107\ W - 3970.631\ mW}{140.107\ W} * 100.0 = 97.166\ \%$$

5.2.2 Buck Mode Maximum Voltage (96-Cell PV Module)

The 96-cell module is the highest voltage, lowest current PV module that will stress the converters ability to buck. This module will put the boost-buck converter in the buck mode for most of its operation and allow the converter to go to its minimum duty cycle as specified in the target specifications. The PV modules input specifications to the converter are:

Table 24: 96-Cell PV Module Input Parameters for NL5 Simulation

Cells	*Cell Type*	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
96	12.5 cm²	57.8060	47.0639	5.0860	5.4688	239.3658

The equivalent circuit to simulate the boost-buck converter in buck mode with all associated losses is shown in Figure 74. This equivalent circuit shows only the components active when the converter is in this mode of operation.

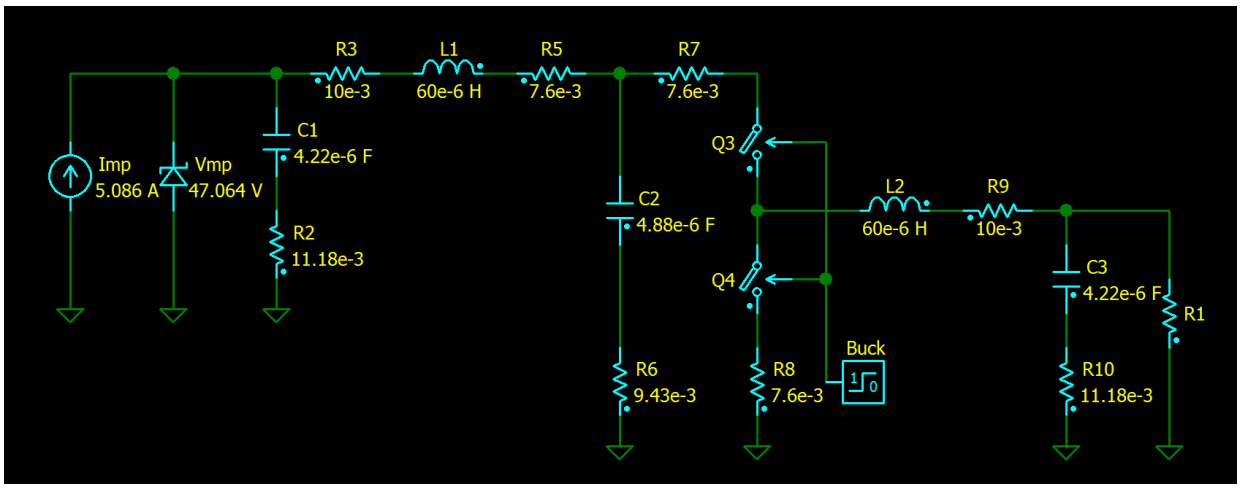

Figure 74: Simulated Buck Converter with Losses

By varying the duty cycle and the load $R1$, assuming the converter is working at the modules maximum power point, the I-V curve of the module and the output I-V curve of the converter can be simulated (Figure 75).

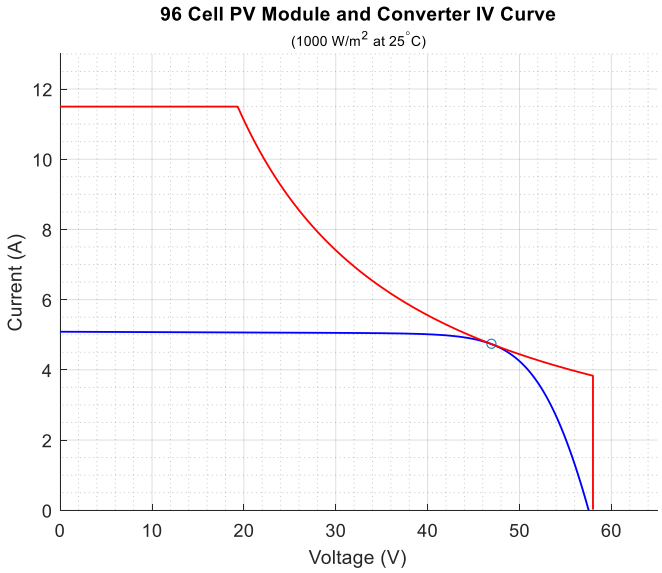

Figure 75: Simulated Buck Converter Output I-V Curve

Also by sweeping the output voltage from 45.0 V to 15.0 V and varying the duty cycle and load accordingly to maintain a constant power on the output, Table 25 can be generated.

Table 25: Simulated Data for Buck Converter Using NL5

D	$Load\ (\Omega)$	$P_{in\ (W)}$	$V_{out\ (V)}$	$I_{out\ (A)}$	$P_{diss\ (W)}$	$P_{out\ (W)}$	$\Delta I_{rip\ (A)}$	$\Delta V_{rip\ (mV)}$	%
0.999	9.228	238.409	46.817	5.073	1.953	235.549	0.011	3.243	98.800
0.956	8.460	238.380	44.817	5.298	1.996	235.425	0.329	98.687	98.760
0.850	6.684	238.426	39.827	5.958	2.255	235.046	1.003	299.373	98.582
0.744	5.118	238.462	34.834	6.807	2.640	234.461	1.503	446.565	98.322
0.637	3.760	238.339	29.827	7.933	3.025	233.604	1.824	539.878	98.013
0.531	2.611	237.907	24.804	9.500	3.335	232.305	1.967	578.293	97.645
0.500	2.313	237.687	23.325	10.083	3.407	231.785	1.974	578.830	97.517
0.425	1.671	236.893	19.759	11.824	3.559	230.087	1.928	558.994	97.127
0.319	0.940	234.637	14.683	15.620	3.798	225.590	1.709	472.709	96.144

Plotting the output voltage vs. the efficiency using the data in Table 25 shows that as the duty cycle decreases, the efficiency of the converter also decreases (Figure 76). This is like the calculated results (Figure 52) for the buck converter using the design specifications thus

confirming that the simulated results match the calculated results. In this mode of operation, the maximum efficiency of the boost-buck converter in buck mode is 98.80 %.

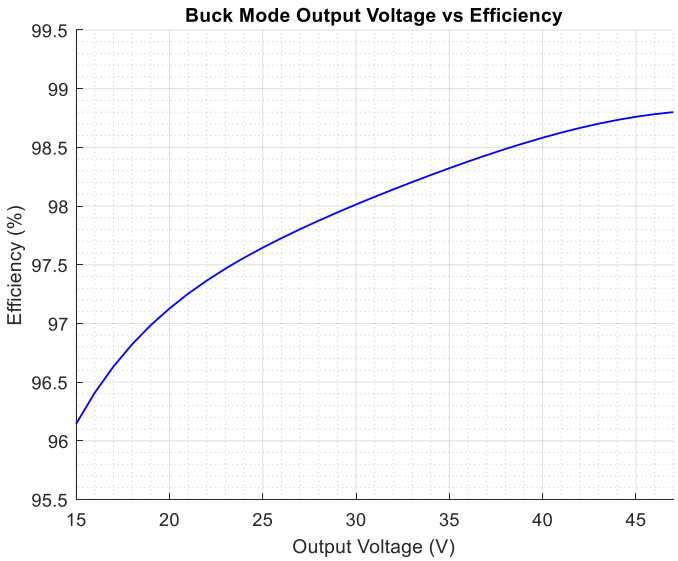

Figure 76: Simulated Buck Converter Output Voltage vs. Efficiency

Taking a looking at the worst-case scenario when the current and voltage ripple on the output will be at their maximum at a duty cycle of 50.0 %, the simulation shows the following waveform in Figure 77.

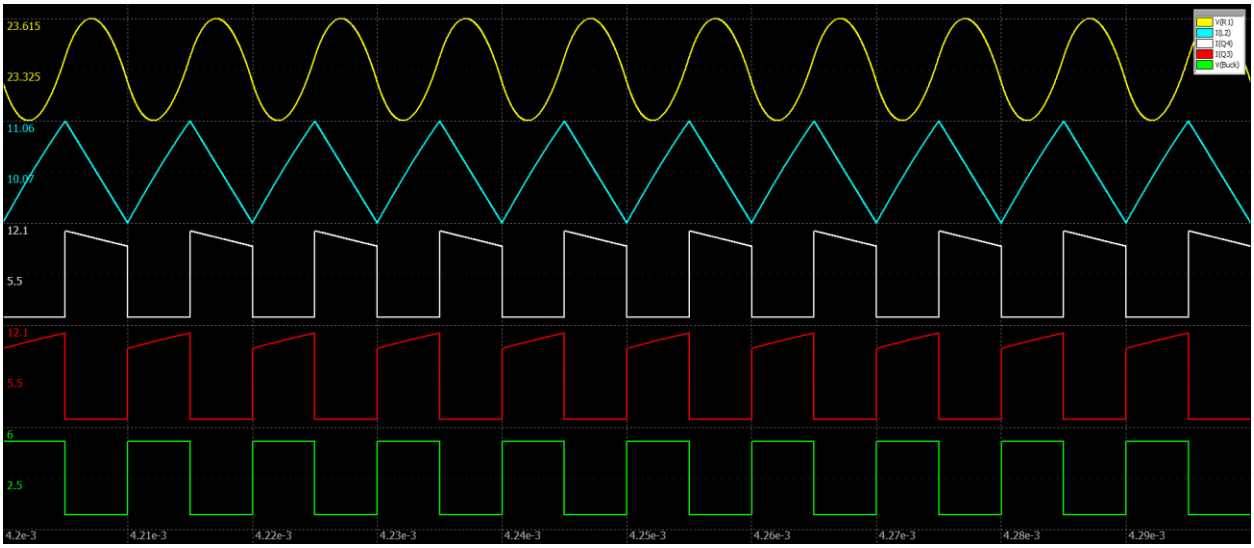

Figure 77: Simulated Buck Converter Output Waveforms at 50.0 % Duty Cycle

Using equations developed earlier in the paper, the simulated results (Table 25) where the duty cycle is at 50.0 % and output voltage and current ripple are at their maximum values can be confirmed.

$$D_{buck} = \frac{V_{out}}{V_{in(\min)}} = \frac{23.532\ V}{47.064\ V} = 0.50$$

$$P_{in} = P_{out} = \left(V_{mp} * I_{mp}\right) = (47.064\ V * 5.086\ A) = 239.368\ W$$

$$P_{out} = V_{out} * I_{out} = 239.368\ W = 47.064\ V *\ I_{out} = 10.172\ A$$

$$R_{load} = \frac{V_{out}}{I_{out}} = \frac{23.532\ V}{10.172\ A} = 2.313\ \Omega$$

$$\Delta I_L = \frac{(V_{in(\max)} - V_{out}) * D}{f_{sw} * L} = \frac{(47.064\ V - 23.532\ V) * 0.50}{100.0\ kHz * 60.0\ \mu H} = 1.961\ A$$

$$\Delta V_{out} = \frac{\Delta I_L}{8 * f_{sw} * C_3} = \frac{1.961\ A}{8 * 100.0\ kHz * 4.22\ \mu F} = 580.865\ mV$$

$$P_{loss}\ @\ 23.532\ V = 5885.112\ mW$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} * 100.0 = \frac{239.368\ W - 5885.112\ mW}{239.368\ W} * 100.0 = 97.541\ \%$$

5.2.3 Boost-Buck Maximum Power (72-Cell PV Module)

The 72-cell module is the highest power PV module that will stress the power capabilities of the converter. This module will put the boost-buck converter in the buck mode or boost mode depending on the characteristics of the PV module and output load conditions. This PV module has the absolute maximum power the converter can handle and will stress all components in the power engine for both the boost converter and buck converter. The PV modules input specifications to the converter are:

Table 26: 72-Cell PV Module Input Parameters for NL5 Simulation

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
72	15.6 cm²	44.3381	35.3362	7.9299	8.5176	280.2136

The equivalent circuit to simulate the boost-buck converter with all associated losses is shown in Figure 78. This equivalent circuit shows only the components active when the converter is in this mode of operation.

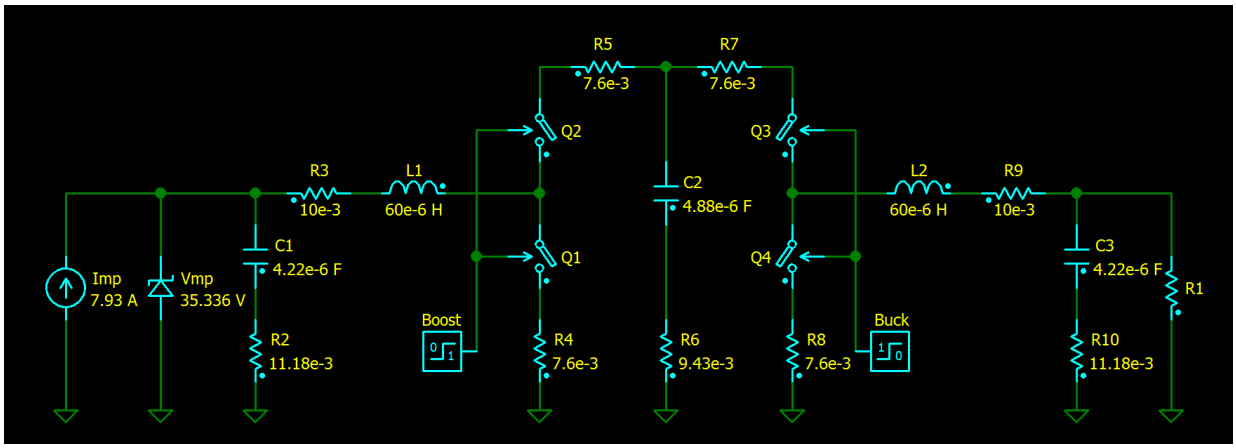

Figure 78: Simulated Boost-Buck Converter with Losses

By varying the duty cycle and the load $R1$, assuming the converter is working at the modules maximum power point, the I-V curve of the module and the output I-V curve of the converter can be simulated (Figure 79).

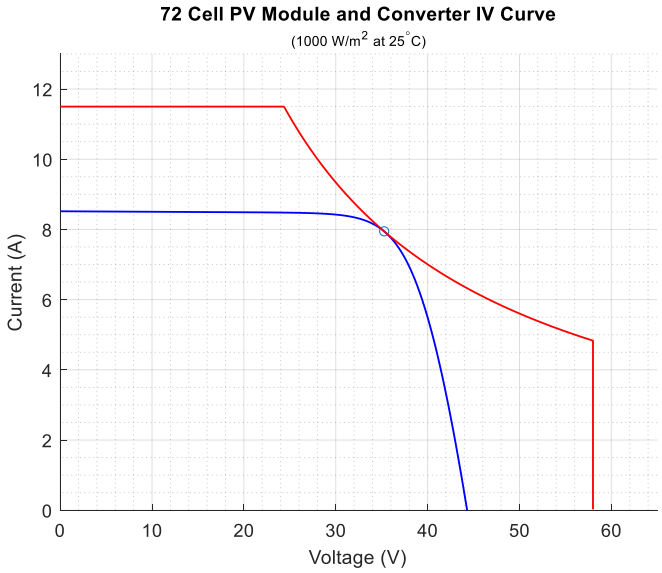

Figure 79: Simulated Boost-Buck Converter Output I-V Curve

Also by sweeping the output voltage from 52.0 V to 17.0 V and varying the duty cycle and load accordingly to maintain a constant power on the output, Table 27 can be generated.

Table 27: Simulated Data for Boost-Buck Converter Using NL5

D	$Load\ (\Omega)$	$P_{in\ (W)}$	$V_{out\ (V)}$	$I_{out\ (A)}$	$P_{diss\ (W)}$	$P_{out\ (W)}$	$\Delta I_{rip\ (A)}$	$\Delta V_{rip\ (mV)}$	%
0.320	9.650	274.346	51.292	5.315	2.901	269.736	1.902	28.998	98.322
0.293	8.922	274.664	49.345	5.531	2.746	270.174	1.745	27.374	98.367
0.215	7.227	275.650	44.482	6.155	2.388	271.411	1.290	21.645	98.463
0.117	5.710	276.968	39.624	6.940	2.115	272.858	0.719	12.755	98.513
0.990	4.372	277.867	34.715	7.941	2.013	273.648	0.101	30.165	98.456
0.849	3.212	277.639	29.716	9.252	2.233	272.705	0.789	234.269	98.194
0.707	2.230	277.271	24.711	11.079	2.594	271.184	1.244	366.000	97.770
0.566	1.427	276.143	19.678	13.785	2.970	268.298	1.459	421.533	97.113
0.500	1.114	275.107	17.317	15.545	3.141	266.058	1.476	418.681	96.657

Plotting the output voltage vs. the efficiency using the data in Table 27 shows that as the duty cycle increases in boost mode or decreases in buck mode, the efficiency of the converter

also decreases (Figure 80) which follows the calculated results presented earlier. In this mode of operation, the maximum efficiency of the boost-buck converter in buck mode is 98.52 %.

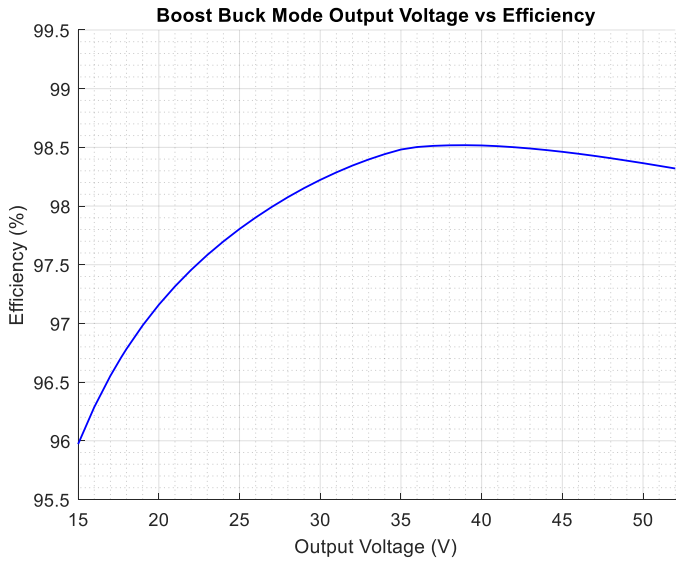

Figure 80: Simulated Boost-Buck Converter Output Voltage vs. Efficiency

Using equations developed earlier in the paper, the simulated results (Table 27) where the duty cycle and output voltage are operating at their maximum conditions for boost mode and the duty cycle is operating at 50.0 % for the buck mode can be confirmed.

For the boost converter:

$$\Delta I_L = \frac{V_{in(\min)} * D}{f_{sw} * L} = \frac{35.336\ V * 0.320}{100\ kHz * 60.0\ \mu H} = 1.887\ A$$

$$\Delta V_{out} = \frac{I_{out} * D}{f_{sw} * C_2} * \frac{X_c}{X_c + L_c} = \frac{1.887\ A * 0.320}{100.0\ kHz * 4.88\ \mu F} * \frac{0.3771}{0.3771 + 37.699} = 35.04\ mV$$

$$P_{loss}\ @\ 52.0\ V = 4605.005\ mW$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} * 100.0 = \frac{280.214\ W - 4605.005\ mW}{280.214\ W} * 100.0 = 98.357\ \%$$

For the buck converter:

$$\Delta I_L = \frac{(V_{in(\max)} - V_{out}) * D}{f_{sw} * L} = \frac{(35.336\ V - 17.668\ V) * 0.50}{100.0\ kHz * 60.0\ \mu H} = 1.472\ A$$

$$\Delta V_{out} = \frac{\Delta I_L}{8 * f_{sw} * C_3} = \frac{1.472\ A}{8 * 100.0\ kHz * 4.22\ \mu F} = 436.118\ mV$$

$$P_{loss}\ @\ 17.668\ V = 9222.302\ mW$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} * 100.0 = \frac{280.214\ W - 9222.302\ mW}{280.214\ W} * 100.0 = 96.709\ \%$$

5.3 Experimental

The boost-buck converter has been manufactured and will be tested to characterize its performance and confirm the calculated and simulated results presented earlier in the paper. Figure 81 shows the completed design. The top of the PCB is where most of the power components are for both the boost and buck engine of the converter while the bottom portion of the PCB houses all the control and logic circuitry for MPP tracking and radio communications.

Figure 81: Manufactured Boost-Buck PCBA

The boost-buck converter will be connected to an array of instruments (Figure 82) that will control the input and output power going to and from the device for it to be characterized.

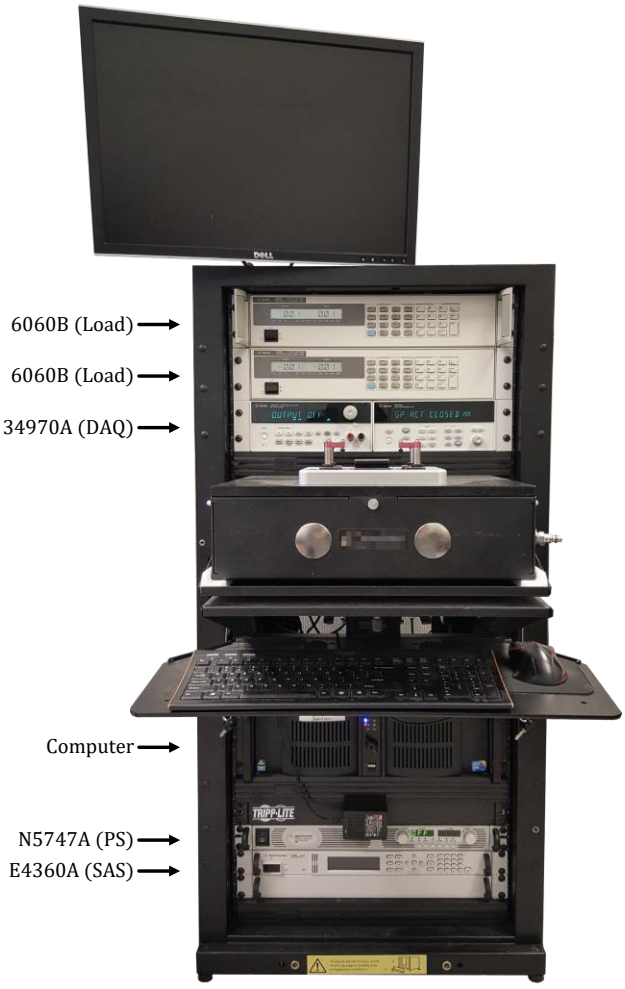

Figure 82: Test Station Used for Characterizing the Converter

The following is a list of the equipment inside of the test station that is used to characterize the converter and test the all of its functionality:

- Agilent E4360A (65.0 V/8.5 A Solar Array Simulator (SAS))
- Agilent N5737A (60.0 V/12.5 A DC Power Supply (PS))
- Agilent 6060B (60.0 V/60.0 A DC Electronic Load (Load))
- Agilent 34970A (Data Acquisition System (DAQ))
- OWON DS7102V (Digital Oscilloscope)

- Current sense shunts (20.0 mΩ) used for accurate input and output current measurements
- Custom built computer with GPIB control interface
- Custom designed software to control all the equipment in the test station and to receive and process all measurements used to characterize the boost-buck converter.

The input of the converter will be connected to the Agilent E4360A (SAS) and the Agilent N5737A (PS). These instruments will control the power going to the device and act as if a PV module is connected directly to the input of the boost-buck converter. The SAS essentially simulates the I-V curve of a PV module and allows the converters MPPT algorithm to function. The output of the device will be connected to two Agilent 6060B (loads) that will simulate varying load conditions and be able to exercise the converters different modes of operation (boost mode and buck mode). An Agilent 34970 (DAQ) will be connected to several points in the system to capture and record the input and output power conditions used to characterize the boost-buck converter. These connections and a general block diagram can be seen in Figure 83 when the converter is connected to the test station.

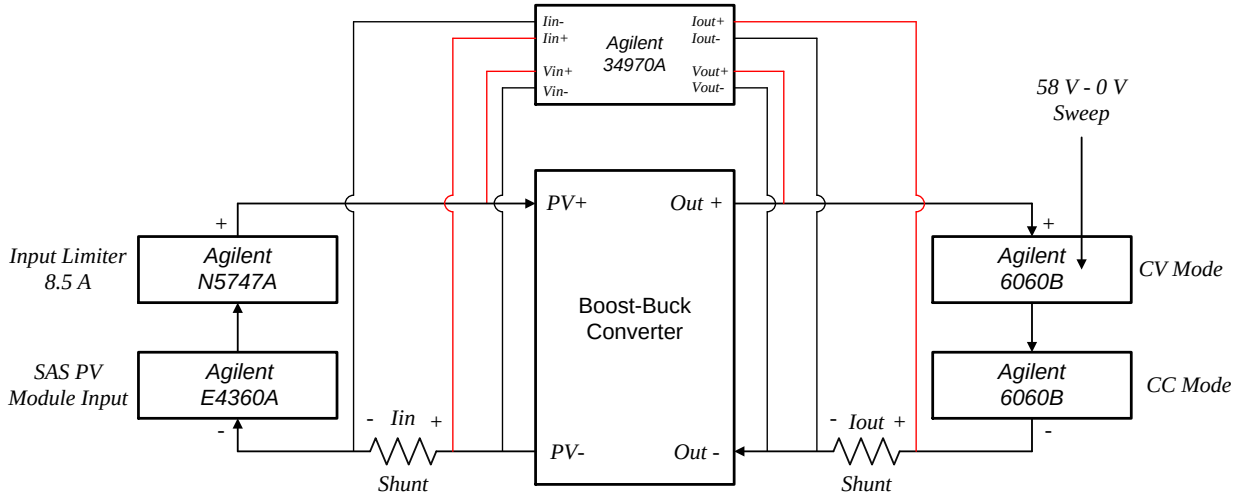

Figure 83: Hook-up Diagram for Boost-Buck Converter Testing

The purpose of this experiment is to simulate real world situations the boost-buck converter may see and characterize its performance during these different scenarios to understand its behavior in the field. The testing procedure for all the experiments will be as follows:

Step 1: Set the SAS to the desired PV module specifications

Step 2: Set the PS to 1.0 V and the current to the I_{sc} of the selected PV module

Step 3: Set one load to constant current mode with the current set to 11.5 A

Step 4: Set the other load to constant voltage mode with the starting voltage set to 58.0 V

Step 5: Set the DAQ channels 1 to 4 to measure the input and output voltage and current

Step 6: Turn on the SAS and PS

Step 7: Measure the DAQ channels and store the values in a data file

Step 8: Decrement the voltage of the constant voltage load by 0.2 V

Step 9: Repeat steps 7 and 8 until the constant voltage load becomes 0.2 V

Step 10: Turn off the SAS and PS

5.3.1 Boost Mode Minimum Voltage (36-Cell PV Module)

For this experiment, to test the boost functionality of the boost-buck converter, the SAS and PS are connected directly to the input of the converter. The settings for the SAS and the PS are programmed to have the same specifications as the 36-cell module used in the simulations. The PV modules input specifications to the converter are shown in Table 28:

Table 28: 36-Cell PV Module Input Parameters for Experiment

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
36	15.6 cm^2	22.1691	17.6681	7.9299	8.5176	140.1068

Power is then applied to the converter and the output voltage of the constant voltage load is varied from 58.0 V down to 0.2 V in 0.2 V decrements. During each output voltage step, data was captured and stored in a file. From this data, a plot of the output voltage vs. the output current is generated showing the output characteristics of the boost-buck converter in boost mode (Figure 84). This plot closely resembles the simulated plot (Figure 71) in the previous sections.

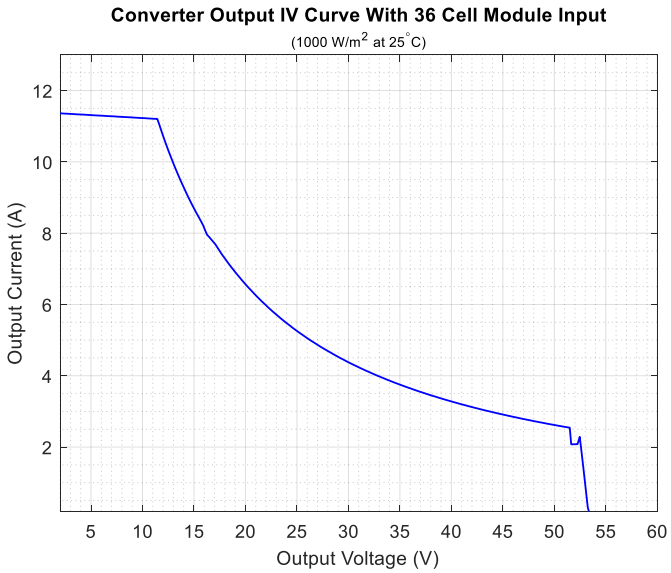

Figure 84: Boost-Buck Converter (Boost Mode) Output Voltage vs. Output Current

Taking the same data obtained from the experiment and plotting the output voltage vs. the efficiency, a new plot is generated (Figure 85) showing the efficiency curve of the boost-buck converter in boost mode over its entire duty cycle range.

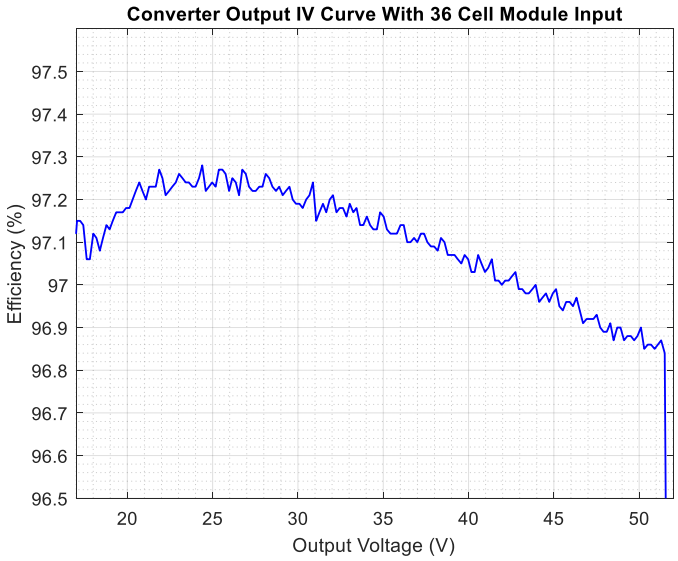

Figure 85: Boost-Buck Converter (Boost Mode) Output Voltage vs. Efficiency

Comparing this plot with the calculated results in Figure 51 and the simulated results in Figure 72, shows that the calculated and simulated results are very similar to the actual experimental results. The calculated and simulated results show a maximum efficiency of 97.48 % and 97.42 % respectively, while the actual results show a maximum efficiency of 97.28 %. The discrepancy lies with additional losses not accounted for on the PCB such as the losses of the other DC/DC converters on the PCB used to create auxiliary power supplies for all the logic circuitry. Also, many of the losses were neglected due to the low switching frequency even though they may have played a role in the overall efficiency losses. A summary of the efficiencies for the calculated, simulated and experimental results are listed in Table 29 and the output voltage vs. efficiency plot is shown in Figure 86.

Table 29: Boost Converter Efficiency Comparisons

D	$V_{out\ (V)}$	$Calculated$	$Simulated$	$Experimental$
0.6602	52.0	97.166	97.086	96.077
0.6466	50.0	97.189	97.113	96.846
0.6074	45.0	97.249	97.182	96.949
0.5583	40.0	97.313	97.256	97.031
0.4952	35.0	97.378	97.329	97.117
0.4111	30.0	97.441	97.397	97.202
0.2933	25.0	97.483	97.433	97.267
0.1166	20.0	97.431	97.374	97.237

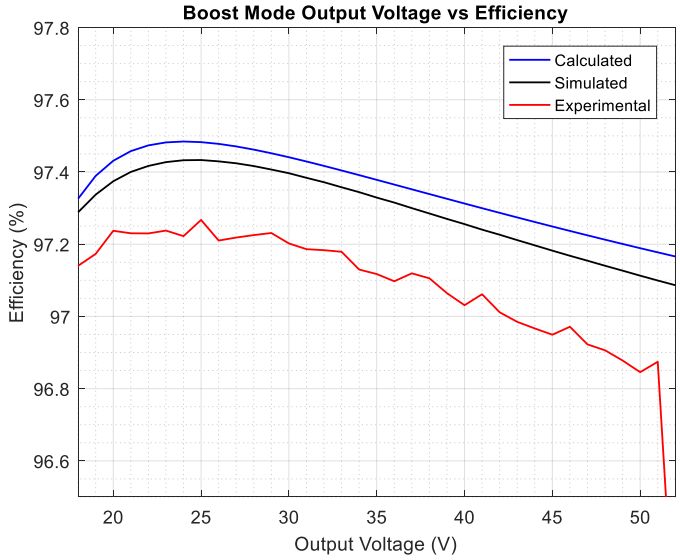

Figure 86: Boost Efficiencies for Calculated, Simulated and Measured Results

Taking a looking at the worst-case scenario when the duty cycle and output voltage is at its maximum operating condition, a snapshot can be made of the PWM waveform and duty cycle being delivered to the boost engine MOSFETs for the converter to be operating in this condition (Figure 87).

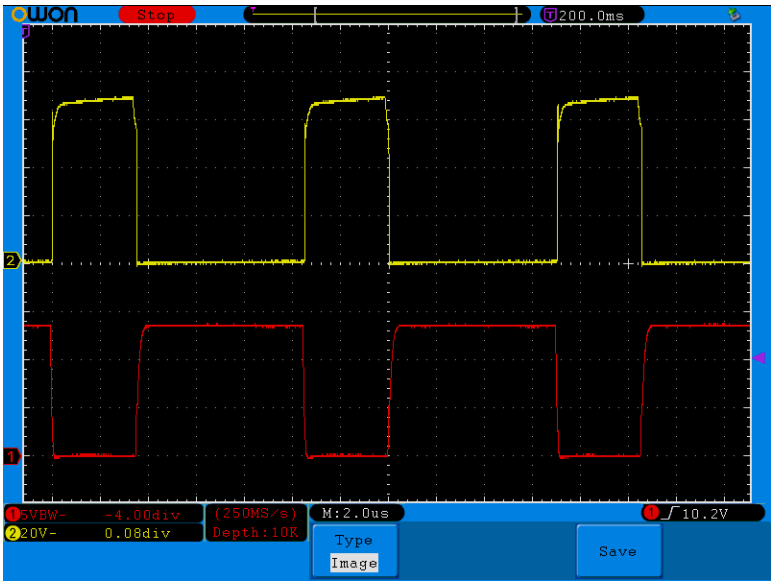

Figure 87: PWM Measurement for Q1 and Q2 at Maximum Duty Cycle

In this scenario when the output voltage is 52.0 V, the duty cycle is measured to be 0.650 which is very close to the calculated result of 0.660. The output ripple voltage was calculated to be 36.1 mV while the simulation showed a result of 29.1 mV. The experimental result, however, shows an output voltage ripple to be around 72.0 mV (Figure 88) which is much greater than the other two results due to other elements in the circuit that were not previously accounted for.

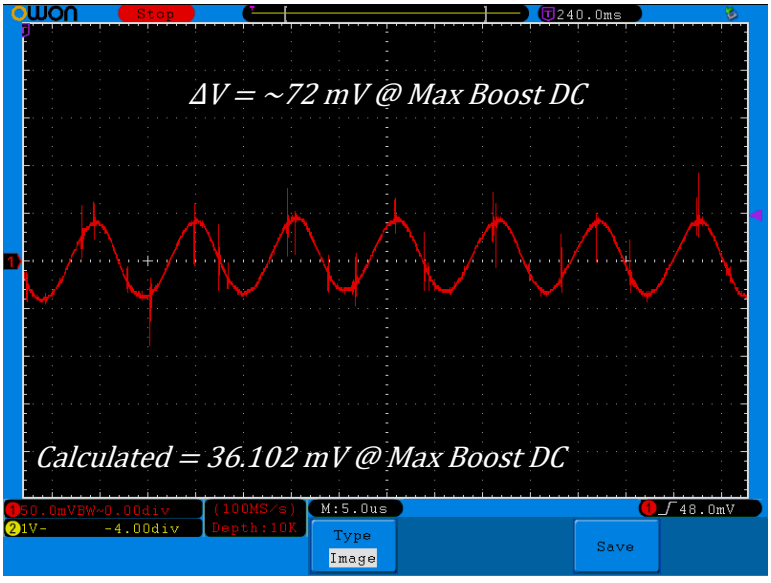

Figure 88: Boost Converter Output Voltage Ripple at Maximum Duty Cycle

5.3.2 Buck Mode Maximum Voltage (96-Cell PV Module)

For this experiment, to test the buck functionality of the boost-buck converter, the SAS and PS are connected directly to the input of the converter. The settings for the SAS and the PS are programmed to have the same specifications as the 96-cell module used in the simulations. The PV modules input specifications to the converter are shown in Table 30:

Table 30: 96-Cell PV Module Input Parameters for Experiment

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
96	15.6 cm²	57.8060	47.0639	5.0860	5.4688	239.3658

Power is then applied to the converter and the output voltage of the constant voltage load is varied from 58.0 V down to 0.2 V in 0.2 V decrements. During each output voltage step, data was captured and stored in a file. From this data, a plot of the output voltage vs. the output current is generated showing the output characteristics of the boost-buck converter in buck mode (Figure 89). This plot closely resembles the simulated plot (Figure 75) in the previous sections.

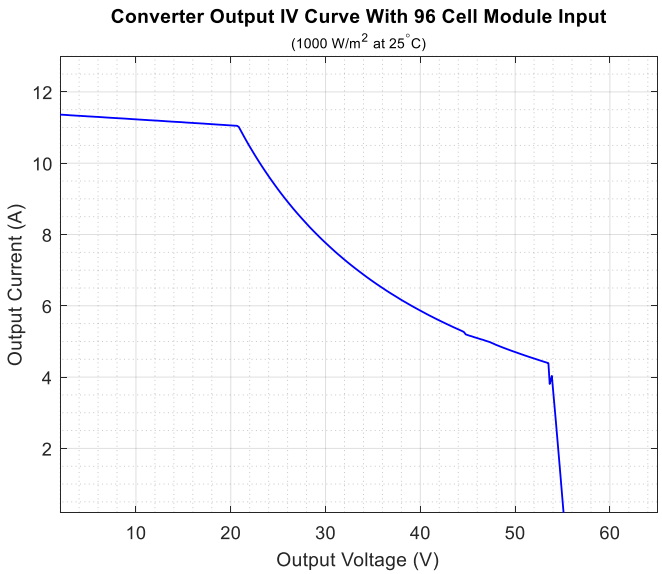

Figure 89: Boost-Buck Converter (Buck Mode) Output Voltage vs. Output Current

Taking the same data obtained from the experiment and plotting the output voltage vs. the efficiency, a new plot is generated (Figure 90) showing the efficiency curve of the boost-buck converter in boost mode over its entire duty cycle range.

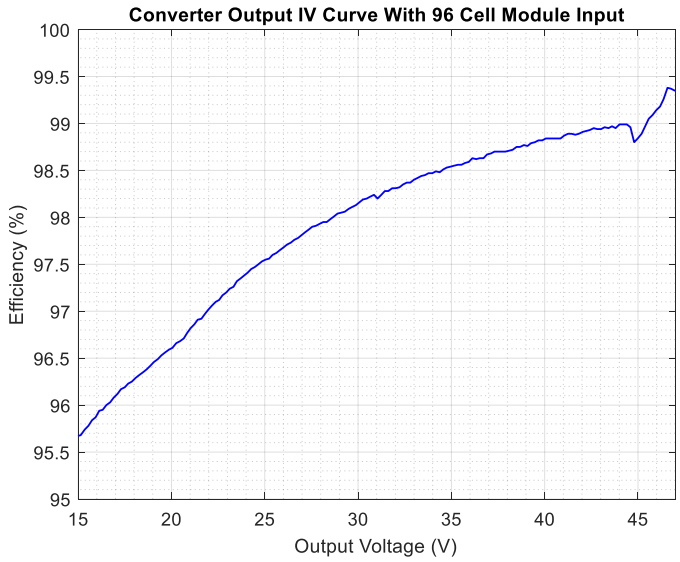

Figure 90: Boost-Buck Converter (Buck Mode) Output Voltage vs. Efficiency

Comparing this plot with the calculated results in Figure 52 and the simulated results in Figure 76, shows that the calculated and simulated results are very similar to the actual experimental results. The calculated and simulated results show a maximum efficiency of 98.82 % and 98.80 % respectively, while the actual results show a maximum efficiency of 99.38 %. There is a higher maximum efficiency for the experimental results due to the converter being a mode called the 'sweet spot'. In this mode of operation, when the converter is slightly bucking, the only losses are the DCR losses in the inductors and the R_{dson} losses in the MOSFETs. This mode is not reflected in the calculations or simulations therefore the losses are higher. A summary of the efficiencies for the calculated, simulated and experimental results are listed in Table 31 and the output voltage vs. efficiency plot is shown in Figure 91.

Table 31: Buck Converter Efficiency Comparisons

D	$V_{out\ (V)}$	$Calculated$	$Simulated$	$Experimental$
0.956	45.0	98.784	98.760	99.046
0.850	40.0	98.606	98.582	98.839
0.744	35.0	98.347	98.322	98.581
0.637	30.0	98.038	98.013	98.239
0.531	25.0	97.671	97.645	97.678
0.500	23.5	97.538	97.517	97.503
0.425	20.0	97.150	97.127	96.857
0.319	15.0	96.151	96.144	95.952

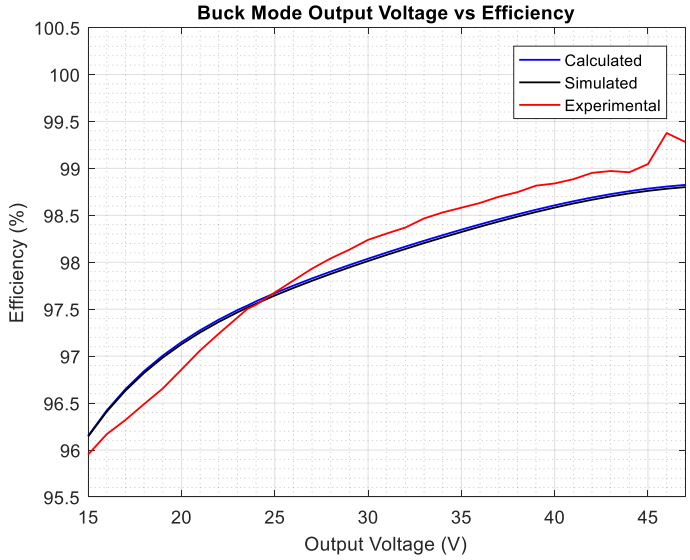

Figure 91: Buck Efficiencies for Calculated, Simulated and Measured Results

Taking a looking at the worst-case scenario when the duty cycle is at 50.0 % and the output voltage and current ripple are at their largest value, a snapshot can be made of the PWM waveform and duty cycle being delivered to the buck engine MOSFETs for the converter to be operating in this condition (Figure 92).

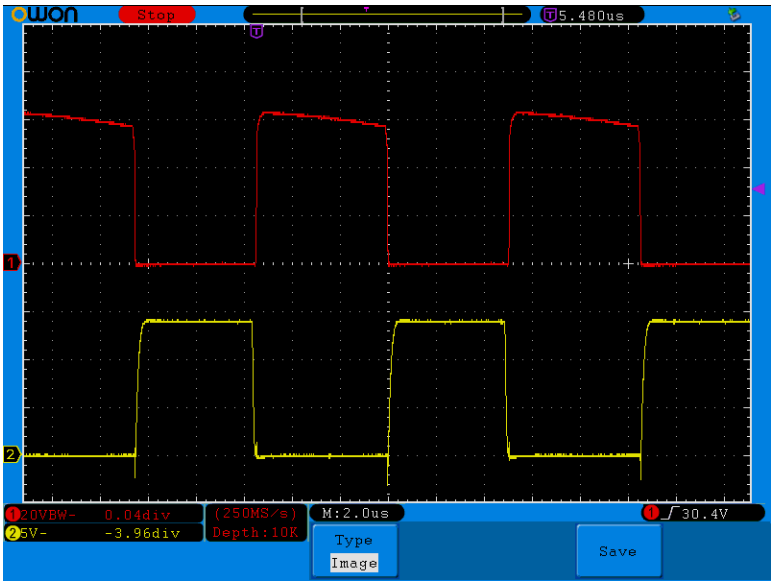

Figure 92: PWM Measurement for Q3 and Q4 at 50.0 % Duty Cycle

In this scenario when the output voltage is 23.53 V, the duty cycle is measured to be 0.50 which is the same as the calculated result of 0.50. The output ripple voltage was calculated to be 580.87 mV while the simulation showed a result of 578.83 mV. The experimental result, however, shows an output voltage ripple to be around 760.0 mV (Figure 93) which once again is much greater than the other two results due to other elements in the circuit.

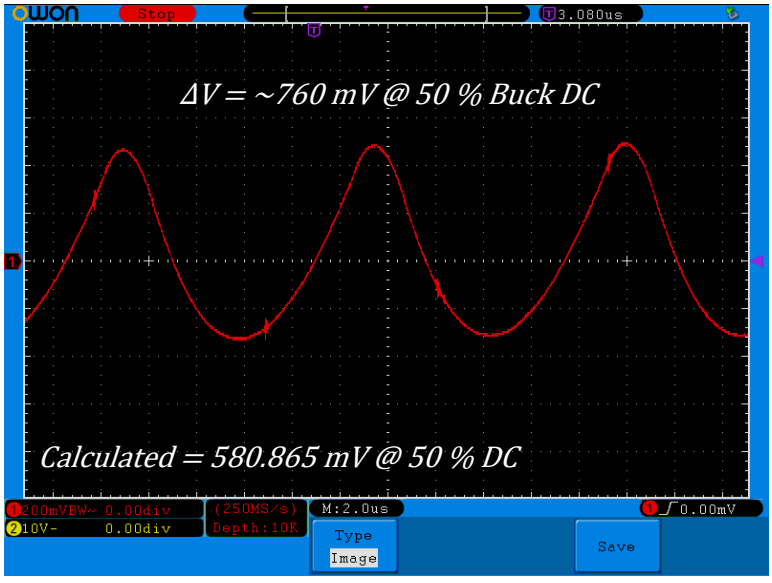

Figure 93: Buck Converter Output Voltage Ripple at 50.0 % Duty Cycle

5.3.3 Boost-Buck Maximum Power (72-Cell PV Module)

For this experiment, to test the full functionality of the boost-buck converter, the SAS and PS are connected directly to the input of the converter. The settings for the SAS and the PS are programmed to have the same specifications as the 72-cell module used in the simulations. The PV modules input specifications to the converter are shown in Table 32:

Table 32: 72-Cell PV Module Input Parameters for Experiment

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
72	15.6 cm²	44.3381	35.3362	7.9299	8.5176	280.2136

Power is then applied to the converter and the output voltage of the constant voltage load is varied from 58.0 V down to 0.2 V in 0.2 V decrements. During each output voltage step, data was captured and stored in a file. From this data, a plot of the output voltage vs. the output current is generated showing the output characteristics of the boost-buck converter in (Figure 94). This plot closely resembles the simulated plot (Figure 79) in the previous sections.

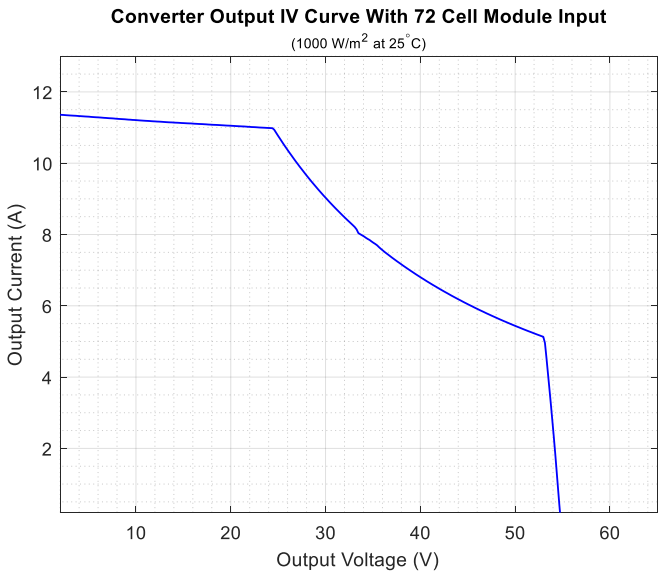

Figure 94: Boost-Buck Converter Output Voltage vs. Output Current

Taking the same data obtained from the experiment and plotting the output voltage vs. the efficiency, a new plot is generated (Figure 95) showing the efficiency curve of the boost-buck converter over its entire duty cycle range.

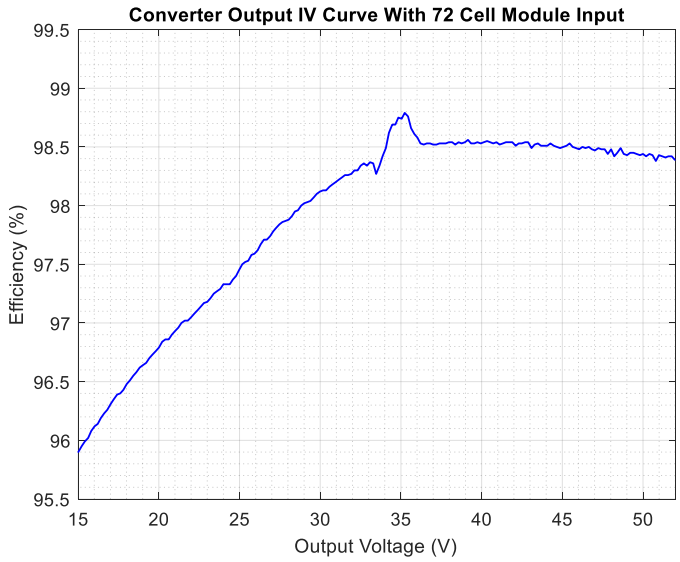

Figure 95: Boost-Buck Converter Output Voltage vs. Efficiency

Comparing this plot with the calculated results and the simulated results in Figure 80, shows that the calculated and simulated results are very similar to the actual experimental results. The calculated and simulated results show a maximum efficiency of 98.55 % and 98.52 % respectively, while the actual results show a maximum efficiency of 98.79 %. Again, there is a higher maximum efficiency for the experimental results due to the converter operating at the 'sweet spot'. In this mode of operation, when the converter is slightly bucking, the only losses are the DCR losses in the inductors and the R_{dson} losses in the MOSFETs. This mode is not reflected in the calculations or simulations therefore the losses are higher. A summary of the efficiencies for the calculated, simulated and experimental results are listed in Table 33 and the output voltage vs. efficiency plot is shown in Figure 96.

Table 33: Boost-Buck Converter Efficiency Comparisons

D	$V_{out\ (V)}$	$Calculated$	$Simulated$	$Experimental$
0.320	52.0	98.357	98.320	98.407
0.293	50.0	98.402	98.365	98.431
0.215	45.0	98.498	98.462	98.502
0.117	40.0	98.549	98.516	98.525
0.990	35.0	98.500	98.482	98.613
0.849	30.0	98.240	98.223	98.198
0.707	25.0	97.820	97.805	97.624
0.566	20.0	97.166	97.159	96.962
0.481	17.0	96.548	96.554	96.514

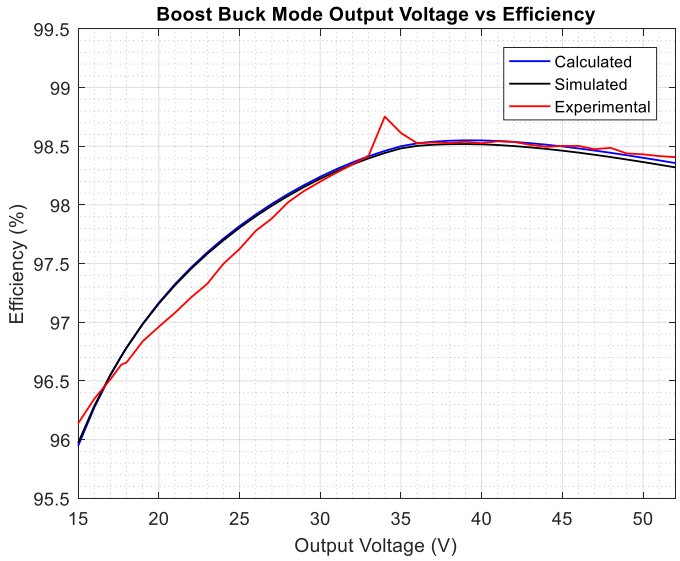

Figure 96: Boost-Buck Efficiencies for Calculated, Simulated and Measured Results

When the output voltage is 52.0 V, the duty cycle is measured to be 0.310 which is close to the calculated result of 0.30. The output ripple voltage was calculated to be 35.04 mV while the simulation showed a result of 29.0 mV. The experimental result, however, shows an output voltage ripple to be around 76.0 mV (Figure 97). Likewise, when the output voltage is 17.67 V, the duty cycle is measured to be 0.50 which is the same as the calculated result of 0.50. The output ripple voltage was calculated to be 436.12 mV while the simulation showed a result of

418.68 mV. The experimental result, however, shows an output voltage ripple to be around 650.0 mV (Figure 98) which once again is much greater than the other two results due to other elements in the circuit not accounted for that increase the voltage ripple on the output.

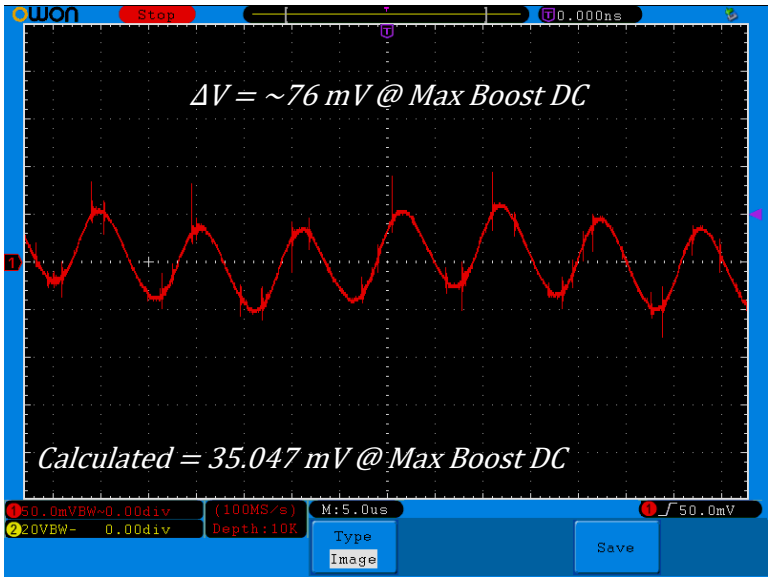

Figure 97: Boost Converter Output Voltage Ripple at Maximum Duty Cycle

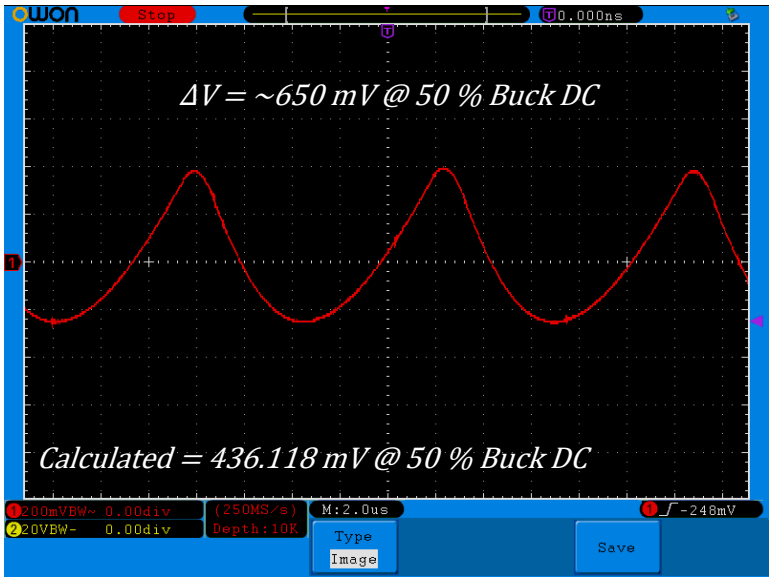

Figure 98: Buck Converter Output Voltage Ripple at 50.0 % Duty Cycle

Sections 5.2.1, 5.2.2 and 5.2.3 characterized and confirmed the accuracy between the calculated, simulated and experimental results. Since the converter was characterized using input

parameters that stress the converters operation in each mode (boost and buck), all other modules connected to the boost-buck converter will fall under these test results.

5.3.4 Efficiency vs. Input Power

For this experiment, the highest power module (72-cell) is used to test the overall efficiency of the converter at varying input power levels to simulate different irradiance and varying load conditions. The 72-cell module is used as a base where the output current of the module will be varied by increments of 1.0 A to vary the input power to the boost-buck converter. At the same time, the output load will be varied by 1.0 V increments at this power level to test the overall efficiency of the converter.

Using the same equations and Matlab script used to calculate the PV module parameters for a 36, 72 and 96-cell module with an I_{sc} of 5.469 A and 8.518 A, new parameters can be calculated to simulate a 72-cell module with different levels of output power. These values will be used as the input parameters to the SAS shown in Table 34, and will be used to simulate several I-V curves of the 72-cell PV module with varying irradiance conditions (Figure 99).

Table 34: Input Power vs. Efficiency PV Module Parameters

$Cells$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
72	39.816	33.138	1.0	1.111	33.138
72	41.310	34.300	2.0	2.177	68.600
72	42.194	34.844	3.0	3.242	104.532
72	42.825	35.134	4.0	4.309	140.536
72	43.317	35.290	5.0	5.377	176.450
72	43.720	35.359	6.0	6.447	212.154
72	44.061	35.369	7.0	7.519	247.583
72	44.334	35.335	8.0	8.500	282.680

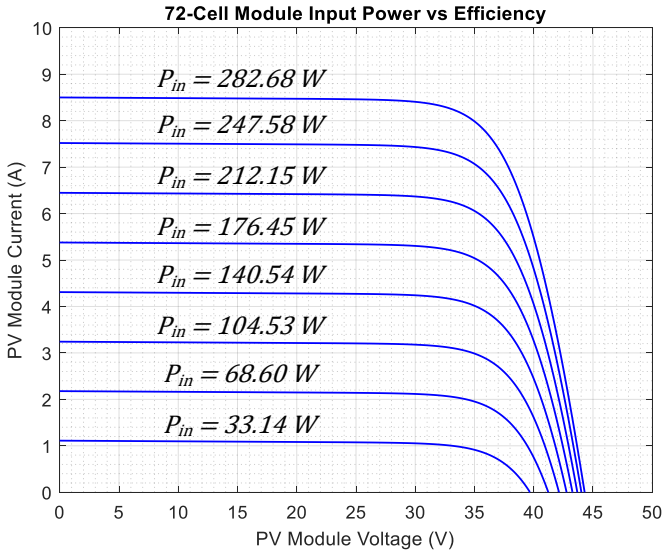

Figure 99: Varying Input Power on 72-Cell PV Module Due to Irradiance

With these SAS input parameters, the constant voltage load is once again decremented by 1.0 V steps from 58.0 V down to 1.0 V. Since the V_{mp} of the 72-cell PV module is around 34.0 V, three points are taken for analysis. The first point is 10.0 V above the V_{mp} of the module where the converter is operating in boost mode. The second point is just slightly below the V_{mp} of the module also known as the 'sweet spot' where the converter is just slightly bucking. Finally, a third point is taken 10.0 V below the V_{mp} of the module where the converter is operating in buck mode. These three points along with their associated efficiencies are presented in Appendix I at different power levels ranging from an I_{mp} of 1.0 A to 8.0 A.

Plotting the input power vs. the efficiency for these three modes of operation (boost, sweet spot and buck) yields the plot shown in Figure 100.

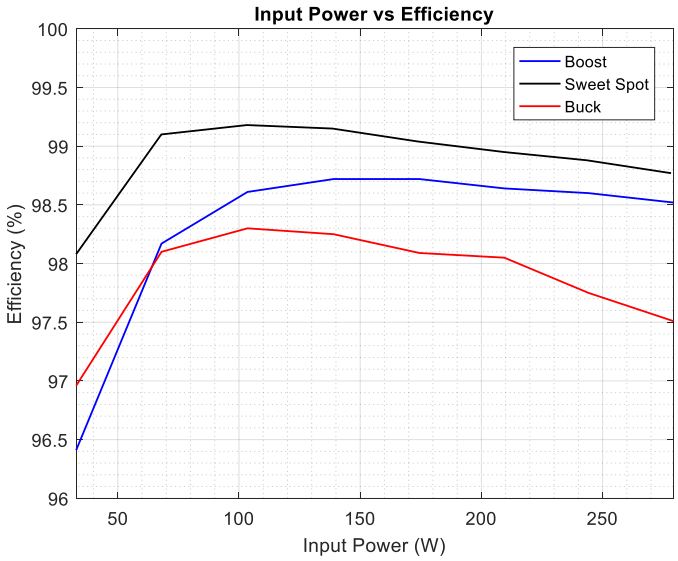

Figure 100: Boost-Buck Converter 72-Cell PV Module Input Power vs. Efficiency

From looking at Figure 100, a conclusion can be made that the designed boost-buck converter is most efficient when operating between 100.0 and 150.0 watts of input power from the PV module and is working at its peak efficiency when the converter is operating in its 'sweet spot'. No matter what input power is being delivered from the module, the converter will always be working at its peak efficiency when operating near the 'sweet spot'. Still, from all the data gathered, the boost-buck converter's efficiency will have a range of 95.0 % and 99.38 %, with an average efficiency of 98.30 %, no matter what PV module is connected to it.

5.3.5 Boost-Buck Control Loop

The boost-buck converters control loop is tested using the SAS with the 72-cell PV module input parameters and varying the constant voltage load in a way that would put the converter in either boost mode or buck mode. An oscilloscope is connected to measure the triangle waveform on one channel, while the second channel is connected to the output of the active comparator that generates the PWM waveform for the MOSFETs. In addition, the input to

the boost comparator and the buck comparator are measured using a different scope and superimposed on the original oscilloscopes image to show all generated control signals that are used to drive the MOSFETs. Once again, the PV module input parameters to the SAS are:

Table 35: 72-Cell PV Module Input Parameters for Control Loop Testing

$Cells$	$Cell\ Type$	$V_{oc\ (V)}$	$V_{mp\ (V)}$	$I_{mp\ (A)}$	$I_{sc\ (A)}$	$P_{mp\ (W)}$
72	15.6 cm²	44.3381	35.3362	7.9299	8.5176	280.2136

The constant voltage load is initially set to 52.0 V which puts the converter into boost mode. With the converter running in steady state, the signals are measured with the oscilloscope and the following images are generated (Figure 101).

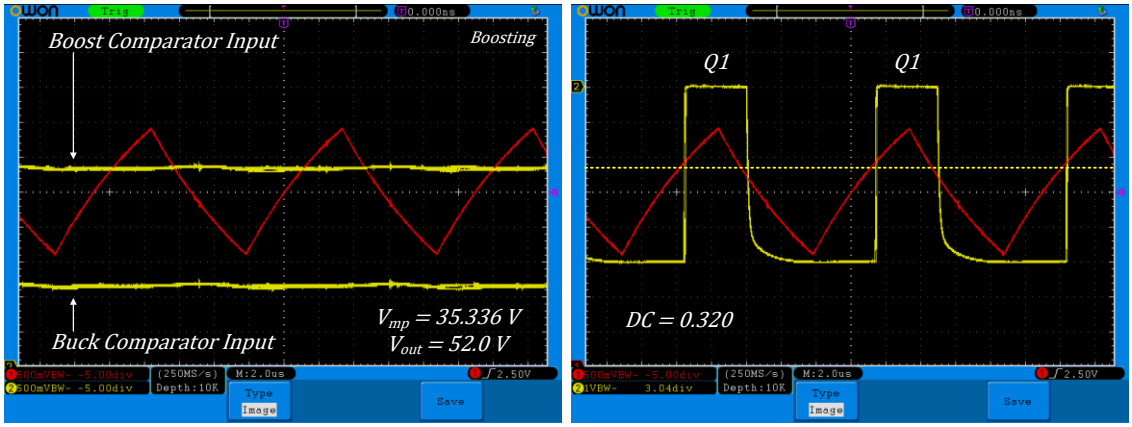

Figure 101: Boost Mode PWM Generated Waveform with a 52.0 V Load

The image on the left in Figure 101 shows the boost comparator input voltage signal slightly above the 2.5 V midpoint of the triangle waveform meaning the converter is boosting but nowhere near its maximum capability. The image also shows the buck comparator input voltage outside of the range of the triangle waveform meaning the buck engine of the converter is shut off completely and not switching at all. The image on the right shows the generated PWM signal on the output of the boost comparator circuit where the duty cycle is determined by the

interaction of the boost comparator input with the triangle waveform. This interaction generates the signal used to drive the boost engine MOSFETs. In this case the duty cycle is 0.320.

If the constant voltage load is changed from 52.0 V to 40.0 V so that the output voltage is now closer to the input voltage but still operating in boost mode, the following image is generated from the oscilloscope (Figure 102).

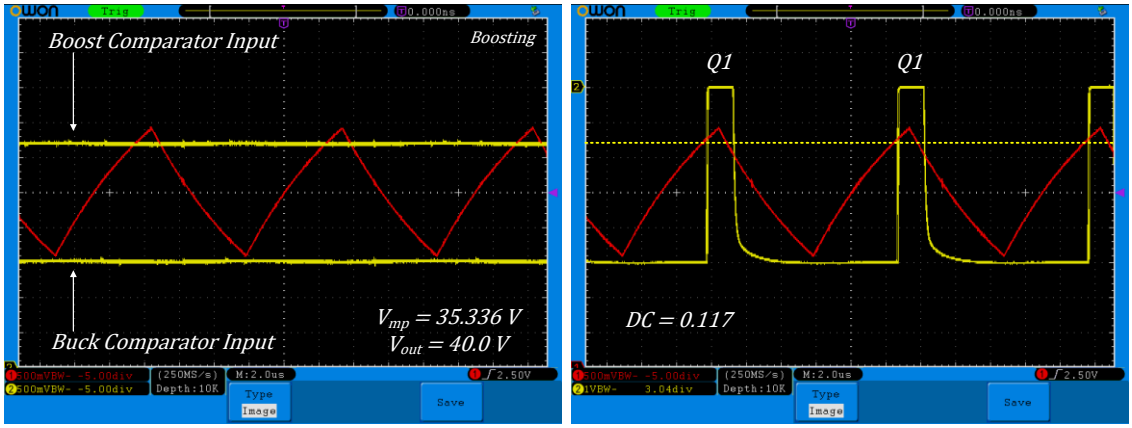

Figure 102: Boost Mode PWM Generated Waveform with a 40.0 V Load

Now the image on the left shows the boost comparator input voltage near the maximum voltage of the triangle waveform meaning the converter is now only slightly boosting its voltage. Also, the buck comparator input voltage is now getting closer to the minimum of the triangle waveform meaning the converter is nearing the point at which it will transition from boost mode to buck mode. The image on the right shows the new generated PWM signal and duty cycle being generated to drive the boost engine MOSFETs. In this case the new duty cycle is 0.117.

If the constant voltage load is decreased to from 40.0 V to 30.0 V so that the output voltage is less than then input voltage putting the converter into buck mode operation, the following image is generated from the oscilloscope (Figure 103).

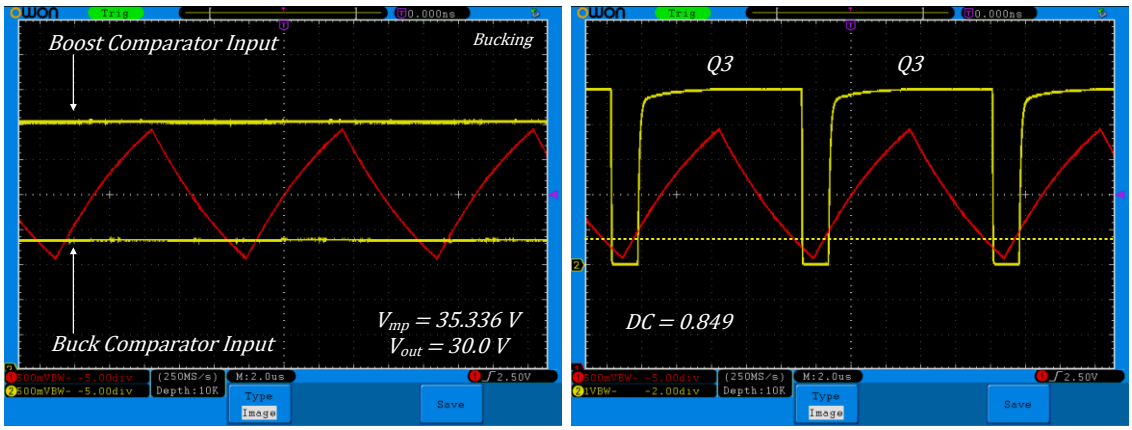

Figure 103: Buck Mode PWM Generated Waveform with a 30.0 V Load

This image shows the boost comparator input is now outside of the range of the triangle waveform meaning the boost engine is now turned off and only the buck engine is operational. The buck comparator input is near the minimum level of the triangle waveform near 1.66 V showing the buck converter is slightly bucking its voltage but nowhere near the maximum bucking capabilities the converter was designed for. The image on the right shows the generated PWM signal on the output of the buck comparator which is now used to drive the buck engine MOSFETs. In this case the duty cycle for the buck converter is 0.849.

If the output load voltage is now decreased to 17.668 V so that the output voltage is 50.0 % of the input voltage, the following image is generated from the oscilloscope (Figure 104).

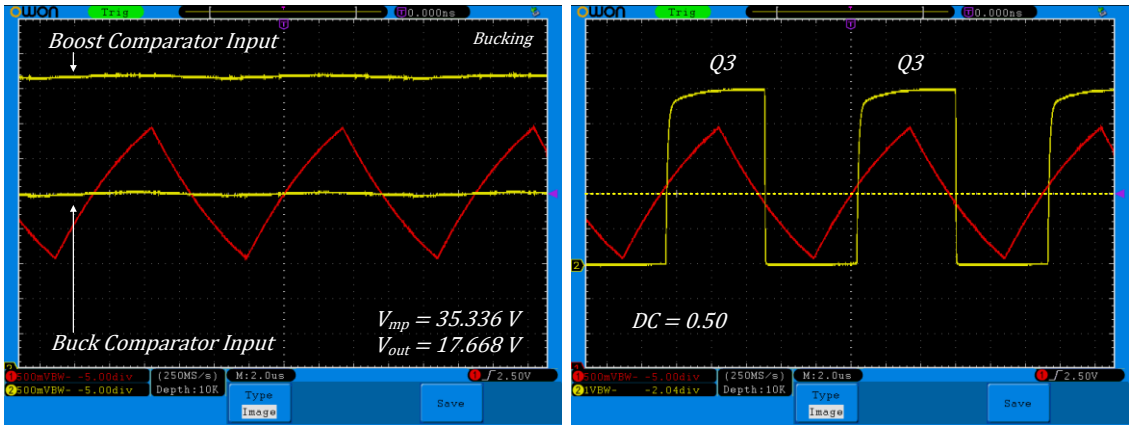

Figure 104: Buck Mode PWM Generated Waveform with a 17.668 V Load

The image shows again that the boost comparator input is still outside the triangle waveform so the boost engine is still turned off while the buck comparator input is right in the middle of the triangle waveform at 2.5 V. Having the buck comparator input in the middle of the waveform produces a 50.0 % duty cycle PWM waveform on the output of the comparator used to drive the buck engine MOSFETs as see in the image on the right in Figure 104.

5.3.6 Over Voltage and Over Current

The over voltage functionality is tested by connecting the input of the converter to a constant DC voltage supply and running it in open circuit mode all while changing its over voltage register values through the wireless radio. The register value starts at 255 and is decremented by steps of 10 until a value of 0 is reached. During each step value, the voltage is measured and recorded shown in Appendix J. By plotting the over voltage register value with the output voltage, a plot can be generated (Figure 105) showing a linear relationship.

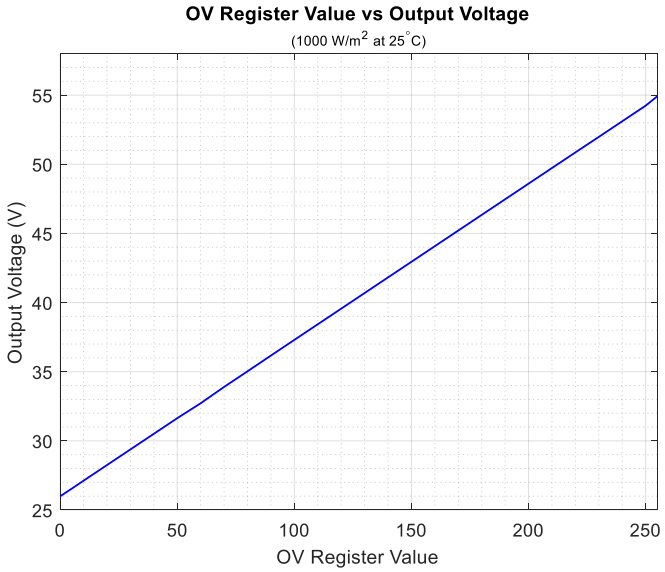

Figure 105: Over Voltage Register Value vs. Output Voltage

From this plot, an equation can be made to express the relationship between the over voltage register value and the output voltage given by.

$$V_{out} = (0.1131 * OV) + 25.981$$

The over current functionality is tested in a very similar manner with the exception that the output is connected to an electronic load with a resistance of 0.0 Ω to simulate a short. Again, the over current register value starts at 255 and is decremented by steps of 10 until a value of 0 is reached. During each step value, the voltage is measured and recorded shown in Appendix J. By plotting the over current register value with the output current, a plot can be generated (Figure 106) showing a linear relationship.

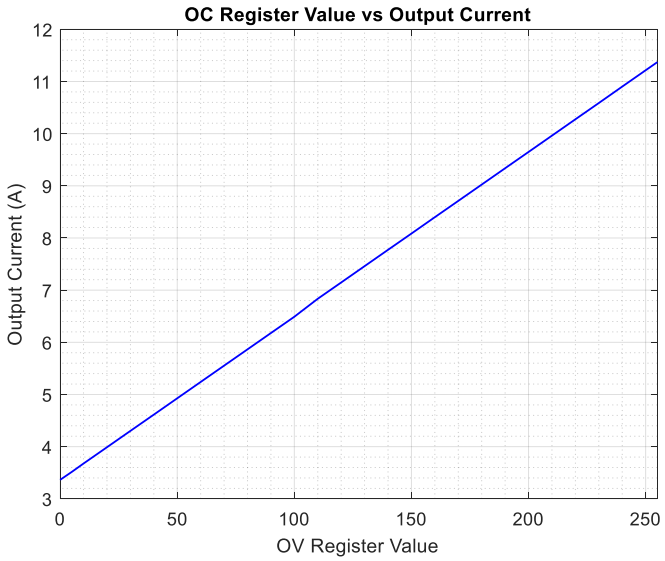

Figure 106: Over Current Register Value vs. Output Current

From this plot, an equation can be made to express the relationship between the over current register value and the output current given by:

$$I_{out} = (0.0314 * OC) + 3.599$$

5.3.7 Module On/Off and MPPT On/Off

The module on and off functionality is simply tested by sending a command over the wireless radio instructing the microprocessor to bypass the PWM signal to the MOSFETs and latch them in either an on or off state. To validate this, the gates of all the MOSFETs are measured with an oscilloscope to show they are in their proper state.

When the module off command is sent, the gates of the boost and buck engine MOSFETs are measured with an oscilloscope and shown in Figure 107 and Figure 108 respectively. From these figures, $Q2$ is in the on state while $Q1$, $Q3$ and $Q4$ are all in the off state. This configuration disables any power from reaching the output since the MOSFETs are not switching. MOSFET $Q2$ is still latched in the on position since the boost-buck converter still needs the input voltage from the PV module to run the other circuitry on the PCB including the microprocessor. If $Q2$ was latched off, no power would ever reach the PCB and the boost-buck converter would be rendered useless. Once in this state, only a module on command will enable the unit to produce power and behave as normal.

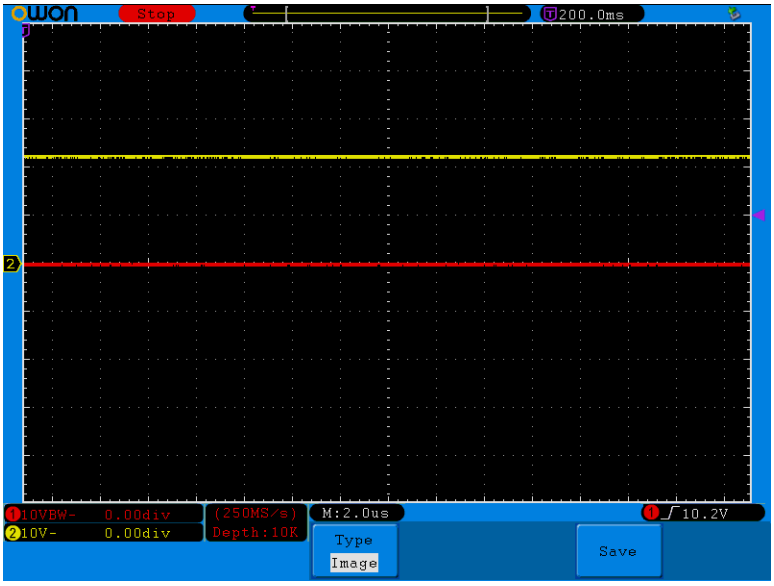

Figure 107: Q1 and Q2 MOSFET Gate Signal (Module Off)

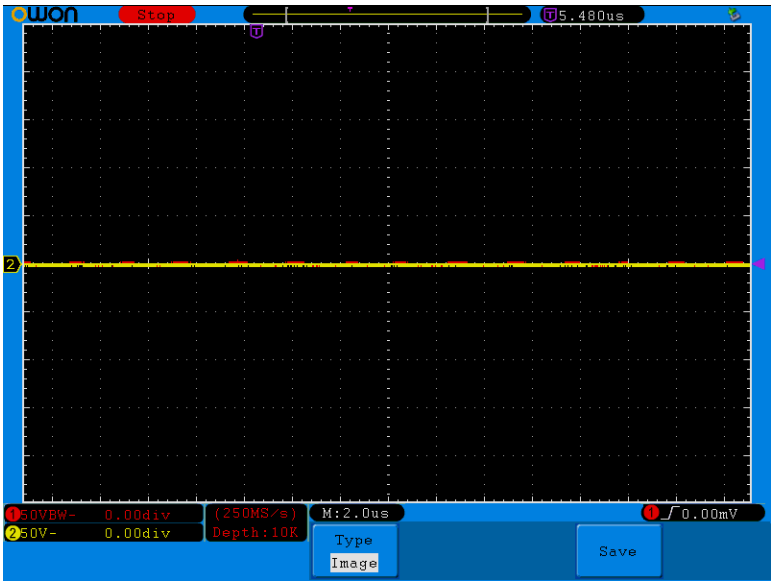

Figure 108: Q3 and Q4 MOSFET Gate Signal (Module Off)

The MPPT on and off functionality is tested the same way as the module on and off functionality. A command is sent over the radio instructing the microprocessor to bypass the PWM signal to the MOSFETs and latch them in either an on or off state. Again, to validate this, the gates of all the MOSFETs are measured with an oscilloscope to show they are in their proper state.

When the MPPT off command is sent, the gates of the boost and buck engine MOSFETs are measured with an oscilloscope and shown in Figure 109 and Figure 110 respectively. From these figures, $Q2$ and $Q3$ are in the on state while $Q1$ and $Q4$ are in the off state. This configuration allows for the output of the PV module to pass through the converter and on to the load directly, as if the converter does not exist. At this point, the only losses in the system due to the converter when the MPPT is turned off, is from the DCR losses in the inductor and the conduction losses from MOSFETs $Q2$ and $Q3$ due to their R_{dson}. These losses are very low and therefore the converters efficiency during this mode of operation is very high.

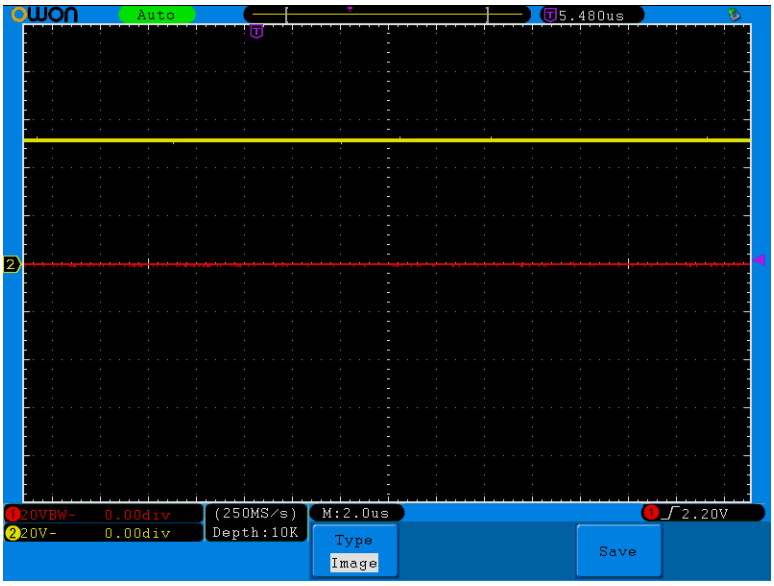

Figure 109: Q1 and Q2 MOSFET Gate Signal (MPPT Off)

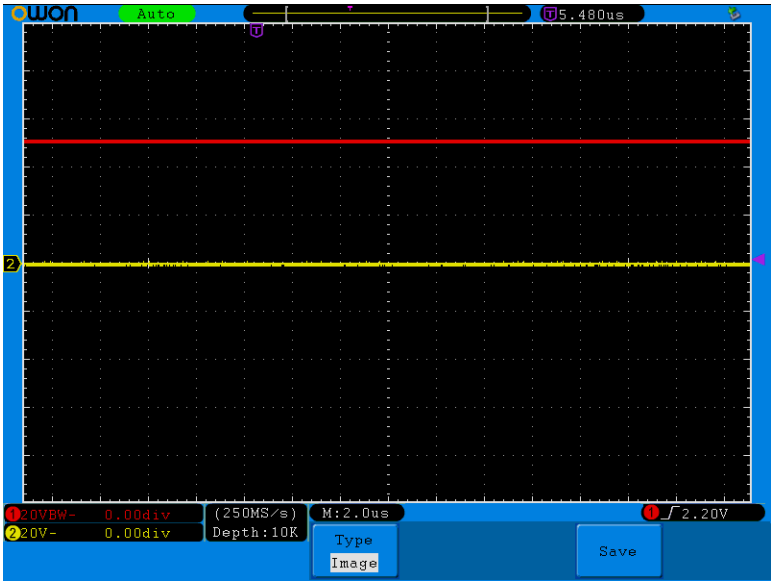

Figure 110: Q3 and Q4 MOSFET Gate Signal (MPPT Off)

CHAPTER 6. CONCLUSION

6.1 Conclusion

The PV system as it exists today has many flaws associated with it. Under certain conditions, the output power of a conventional PV array can be severely crippled with no way to recover the lost energy. Integrating module level DC/DC electronics, specifically boost-buck converters, into the PV array will dramatically improve the performance of the system and eliminate many of the issues seen today. In fact, the use of module level power electronics can potentially recover between 10.0 to 30.0 % of annual performance loss or more, depending on the system configuration and type of devices used.

Of the three converter topologies overviewed in this thesis, the synchronous boost-buck converter makes the most sense as it can be used with a wide variety of PV modules and configurations. Not only this, but the efficiency of this topology is much higher than any other topology as seen from the calculations, simulations and experiments performed. Even though the designed boost-buck converter can reach efficiencies upwards of 99.4 %, the chosen topology makes it difficult to control and has several added components that add to the overall cost.

As this paper explained, proper component selection is critical especially when trying to reach these higher efficiencies. In fact, these components are so critical, that even a one percent loss in efficiency on a PV module can lead to megawatts lost to the grid. When selecting these components, there are many tradeoffs to consider between price, size and efficiency. If the price is too high, or the efficiency too low, then integrating the device into a PV module would not make any sense especially if grid parity could not be met. Yet, as PV module efficiencies increase and newer technology come to pass, DC/DC converters with an MPPT algorithm will become invaluable in the implantation of PV modules as an alternative source of energy.

6.2 Future Work

There are several areas that need to be studied further when it comes to integrating DC/DC converters into PV modules, specifically the boost-buck converter. One such area that needs further study is to connect several PV modules with integrated DC/DC converters in series to see how they operate with each other. This would mean analyzing the loop stability of each converter and how it interacts with the other converters connected in the string.

PV modules are also becoming more efficient with higher output power so the converter will need to be redesigned to handle the higher voltage and current requirements. This means the new converter will need larger inductors, capacitors and MOSFETs. To do this without increasing the price will be a challenge.

Another area that is getting a lot of attention and needs to be looked at is more safety features, especially when it comes to arc faults and fire prevention. Animals can chew through wires or other situations can arise causing arcs to form in the system. These arcs can ultimately burn down buildings or seriously injure anyone who is exposed to them. Firefighters are especially hesitant to put out a fire if PV modules are installed on the roof due to the live voltage that can be present. An arc fault detection circuit with rapid shut down capabilities will have to be implemented for someone to safely work on a PV system if such a problem were to occur. To do this, extra circuity will need to be added to first, detect an arc fault and second, to safely turn the modules off within seconds, thus, extinguishing the arc and making the system safe to work on. However, this would also mean smarter diagnostics and more reliable radio communications to sense and alert the customer when and where the fault occurred, ultimately increasing the overall cost of the converter.

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APPENDIX A: MATLAB SCRIPT FOR PV CELL I-V CURVE

```
% PV Cell I-V Model
clc;
TNOM = 273.15;              % 0 Degrees C in Kelvin
T = 298.15;                 % Nominal Cell Temperature @ STC
K = 1.38065e-23;            % Boltzmann's Constant
Q = 1.602e-19;              % Electron Charge Constant
n = 1.2;                    % Diode Ideality Factor (1.2 = monosilicon)
VT = ((n*K*T)/Q);           % Thermal Voltage
IS = 5e-10;                 % Diode Reverse Satration Current
RS = 0.005;                 % Series Resistance
RSH = 10;                   % Shunt Resistnace
Eg = 1.12;                  % Bandgap of Silicone
IS = IS*((T/TNOM)^3)*exp(((Q*Eg/(n*K))*((1/TNOM)-(1/T))));
user_entry = input('Enter Number of Cells in PV Module? = ');
Cells = user_entry;         % Number of Cells in Solar Module
user_entry = input('Enter ISC @ STC = ');
ISCMAX = user_entry;
ISC = ISCMAX;               % Short Circuit Module Current (A)
IOUT = 0:0.001:ISC;
ID = ISC-IOUT;              % Diode Current
VD = VT*log(ID/IS+1);       % Diode Voltage
VOUT = VD-IOUT*RS;
IOUT = IOUT-VOUT/RSH;       % Output Current from PV Module
VOUT = VOUT*Cells;          % Output Voltage from PV Module
POUT = times(VOUT, IOUT);   % Output Power from PV Module
VOC = max(VOUT);            % Find Maximum Output Voltage
[Pmpp, col] = max(POUT);    % Find Location of Maximum Power
Vmpp = VOUT(col);           % Find Location of Maximum Voltage
Impp = IOUT(col);           % Find Location of Maximum Current

plot(VOUT, IOUT, 'b', 'linewidth', 1)
xlim([0.0 1.0]);
ylim([0.0 8.0]);
title({...
    '\fontsize{11pt}\bf{PV Cell I-V Curve}'
    '\fontsize{8pt}\rm{(1000 W/m^2 at 25^{\circ}C)}'
})
xlabel('PV Cell Voltage (V)')    % x-axis label
ylabel('PV Cell Current (A)')    % y-axis label
grid on
grid minor
hold all
plot(Vmpp, Impp, '-o', 'MarkerSize', 5)    % Plot Marker of Maximum Power
hold off
```

APPENDIX B: TYPES OF PV MODULES

Module	*Cells*	$V_{oc\,(V)}$	$V_{mp\,(V)}$	$I_{mp\,(A)}$	$I_{sc\,(A)}$	$P_{mp\,(W)}$
SLP085-12U	36	21.60	17.20	4.94	5.50	85.00
485J	36	22.20	17.80	4.78	5.35	85.00
SLP090-12	36	21.80	17.60	5.11	5.51	90.00
SPM090P-BP	36	22.20	17.90	5.03	5.58	90.00
Average		21.95	17.625	4.965	5.485	87.50

Module	*Cells*	$V_{oc\,(V)}$	$V_{mp\,(V)}$	$I_{mp\,(A)}$	$I_{sc\,(A)}$	$P_{mp\,(W)}$
SPM140P-BP	36	22.00	17.50	8.00	8.60	140.00
KD145 SX-UFU	36	22.30	17.90	8.11	8.78	145.00
SLP150-12	36	22.20	18.50	8.11	8.68	150.00
SP150P	36	21.17	17.64	8.51	9.51	150.00
Average		21.92	17.89	8.18	8.89	146.25

Module	*Cells*	$V_{oc\,(V)}$	$V_{mp\,(V)}$	$I_{mp\,(A)}$	$I_{sc\,(A)}$	$P_{mp\,(W)}$
BP 4180T	72	43.60	35.80	5.03	5.58	180.00
4190J	72	45.30	38.00	5.00	5.50	190.00
TSM-195DA01A	72	45.60	37.40	5.22	5.56	195.00
TP200	72	44.40	36.60	5.46	5.79	200.00
Average		44.73	36.95	5.18	5.61	191.25

Module	*Cells*	$V_{oc\,(V)}$	$V_{mp\,(V)}$	$I_{mp\,(A)}$	$I_{sc\,(A)}$	$P_{mp\,(W)}$
UP-M300P	72	45.60	35.90	8.360	8.66	300.00
310P	72	44.90	36.40	8.520	9.08	310.00
UP-M310P	72	46.00	36.30	8.540	8.82	310.00
YL315P-35b	72	45.70	36.80	8.560	9.12	315.00
Average		45.55	36.35	8.50	8.92	308.75

Module	*Cells*	$V_{oc\,(V)}$	$V_{mp\,(V)}$	$I_{mp\,(A)}$	$I_{sc\,(A)}$	$P_{mp\,(W)}$
RDM-215/96	96	57.00	47.50	4.47	5.00	215.00
BEST235MI-96	96	57.70	48.30	4.86	5.28	235.00
JTM250-96M	96	59.23	49.38	4.86	5.44	240.00
ZXM5-96-250	96	59.60	48.70	5.14	5.55	250.00
Average		58.38	48.47	4.83	5.32	235.00

APPENDIX C: BOOST CONVERTER INPUT AND OUTPUT CHARACTERISTICS

$V_{in\,(V)}$	$I_{in\,(A)}$	$P_{in\,(W)}$	$V_{out\,(V)}$	$I_{out\,(A)}$	$P_{out\,(W)}$	D	$Load\ (\Omega)$	$\Delta I_{L\,(A)}$	$\Delta V_{out\,(mV)}$
17.0	9.912	168.504	52.0	3.240	168.504	0.673	16.047	1.907	44.265
17.0	9.912	168.504	51.0	3.304	168.504	0.667	15.436	1.889	44.703
17.0	9.912	168.504	50.0	3.370	168.504	0.660	14.836	1.870	45.141
17.0	9.912	168.504	49.0	3.439	168.504	0.653	14.249	1.850	45.578
17.0	9.912	168.504	48.0	3.511	168.504	0.646	13.673	1.830	46.012
17.0	9.912	168.504	47.0	3.585	168.504	0.638	13.109	1.809	46.443
17.0	9.912	168.504	46.0	3.663	168.504	0.630	12.558	1.786	46.868
17.0	9.912	168.504	45.0	3.745	168.504	0.622	12.018	1.763	47.285
17.0	9.912	168.504	44.0	3.830	168.504	0.614	11.489	1.739	47.693
17.0	9.912	168.504	43.0	3.919	168.504	0.605	10.973	1.713	48.087
17.0	9.912	168.504	42.0	4.012	168.504	0.595	10.469	1.687	48.466
17.0	9.912	168.504	41.0	4.110	168.504	0.585	9.976	1.659	48.825
17.0	9.912	168.504	40.0	4.213	168.504	0.575	9.495	1.629	49.159
17.0	9.912	168.504	39.0	4.321	168.504	0.564	9.026	1.598	49.464
17.0	9.912	168.504	38.0	4.434	168.504	0.553	8.570	1.566	49.733
17.0	9.912	168.504	37.0	4.554	168.504	0.541	8.124	1.532	49.960
17.0	9.912	168.504	36.0	4.681	168.504	0.528	7.691	1.495	50.135
17.0	9.912	168.504	35.0	4.814	168.504	0.514	7.270	1.457	50.249
17.0	9.912	168.504	34.0	4.956	168.504	0.500	6.860	1.417	50.290
17.0	9.912	168.504	33.0	5.106	168.504	0.485	6.463	1.374	50.244
17.0	9.912	168.504	32.0	5.266	168.504	0.469	6.077	1.328	50.094
17.0	9.912	168.504	31.0	5.436	168.504	0.452	5.703	1.280	49.819
17.0	9.912	168.504	30.0	5.617	168.504	0.433	5.341	1.228	49.396
17.0	9.912	168.504	29.0	5.810	168.504	0.414	4.991	1.172	48.795
17.0	9.912	168.504	28.0	6.018	168.504	0.393	4.653	1.113	47.981
17.0	9.912	168.504	27.0	6.241	168.504	0.370	4.326	1.049	46.910
17.0	9.912	168.504	26.0	6.481	168.504	0.346	4.012	0.981	45.529
17.0	9.912	168.504	25.0	6.740	168.504	0.320	3.709	0.907	43.773
17.0	9.912	168.504	24.0	7.021	168.504	0.292	3.418	0.826	41.559
17.0	9.912	168.504	23.0	7.326	168.504	0.261	3.139	0.739	38.787
17.0	9.912	168.504	22.0	7.659	168.504	0.227	2.872	0.644	35.328
17.0	9.912	168.504	21.0	8.024	168.504	0.190	2.617	0.540	31.018
17.0	9.912	168.504	20.0	8.425	168.504	0.150	2.374	0.425	25.648
17.0	9.912	168.504	19.0	8.869	168.504	0.105	2.142	0.298	18.946
17.0	9.912	168.504	18.0	9.361	168.504	0.056	1.923	0.157	10.555
17.0	9.912	168.504	17.0	9.912	168.504	0.000	1.715	0.000	0.000

APPENDIX D: BUCK CONVERTER INPUT AND OUTPUT CHARACTERISTICS

$V_{in\,(V)}$	$I_{in\,(A)}$	$P_{in\,(W)}$	$V_{out\,(V)}$	$I_{out\,(A)}$	$P_{out\,(W)}$	D	$Load\ (\Omega)$	$\Delta I_{L\,(A)}$	$\Delta V_{out\,(mV)}$
52.0	3.240	168.48	52.0	3.240	168.48	1.000	16.049	0.000	0.000
52.0	3.240	168.48	51.0	3.304	168.48	0.981	15.438	0.163	48.419
52.0	3.240	168.48	50.0	3.370	168.48	0.962	14.839	0.321	94.939
52.0	3.240	168.48	49.0	3.438	168.48	0.942	14.251	0.471	139.560
52.0	3.240	168.48	48.0	3.510	168.48	0.923	13.675	0.615	182.282
52.0	3.240	168.48	47.0	3.585	168.48	0.904	13.111	0.753	223.106
52.0	3.240	168.48	46.0	3.663	168.48	0.885	12.559	0.885	262.031
52.0	3.240	168.48	45.0	3.744	168.48	0.865	12.019	1.010	299.057
52.0	3.240	168.48	44.0	3.829	168.48	0.846	11.491	1.128	334.184
52.0	3.240	168.48	43.0	3.918	168.48	0.827	10.975	1.240	367.413
52.0	3.240	168.48	42.0	4.011	168.48	0.808	10.470	1.346	398.742
52.0	3.240	168.48	41.0	4.109	168.48	0.788	9.977	1.446	428.173
52.0	3.240	168.48	40.0	4.212	168.48	0.769	9.497	1.538	455.705
52.0	3.240	168.48	39.0	4.320	168.48	0.750	9.028	1.625	481.339
52.0	3.240	168.48	38.0	4.434	168.48	0.731	8.571	1.705	505.074
52.0	3.240	168.48	37.0	4.554	168.48	0.712	8.126	1.779	526.909
52.0	3.240	168.48	36.0	4.680	168.48	0.692	7.692	1.846	546.847
52.0	3.240	168.48	35.0	4.814	168.48	0.673	7.271	1.907	564.885
52.0	3.240	168.48	34.0	4.955	168.48	0.654	6.861	1.962	581.024
52.0	3.240	168.48	33.0	5.105	168.48	0.635	6.464	2.010	595.265
52.0	3.240	168.48	32.0	5.265	168.48	0.615	6.078	2.051	607.607
52.0	3.240	168.48	31.0	5.435	168.48	0.596	5.704	2.087	618.050
52.0	3.240	168.48	30.0	5.616	168.48	0.577	5.342	2.115	626.595
52.0	3.240	168.48	29.0	5.810	168.48	0.558	4.992	2.138	633.241
52.0	3.240	168.48	28.0	6.017	168.48	0.538	4.653	2.154	637.988
52.0	3.240	168.48	27.0	6.240	168.48	0.519	4.327	2.163	640.836
52.0	3.240	168.48	26.0	6.480	168.48	0.500	4.012	2.167	641.785
52.0	3.240	168.48	25.0	6.739	168.48	0.481	3.710	2.163	640.836
52.0	3.240	168.48	24.0	7.020	168.48	0.462	3.419	2.154	637.988
52.0	3.240	168.48	23.0	7.325	168.48	0.442	3.140	2.138	633.241
52.0	3.240	168.48	22.0	7.658	168.48	0.423	2.873	2.115	626.595
52.0	3.240	168.48	21.0	8.023	168.48	0.404	2.618	2.087	618.050
52.0	3.240	168.48	20.0	8.424	168.48	0.385	2.374	2.051	607.607
52.0	3.240	168.48	19.0	8.867	168.48	0.365	2.143	2.010	595.265
52.0	3.240	168.48	18.0	9.360	168.48	0.346	1.923	1.962	581.024
52.0	3.240	168.48	17.0	9.911	168.48	0.327	1.715	1.907	564.885
52.0	3.240	168.48	16.0	10.530	168.48	0.308	1.519	1.846	546.847
52.0	3.240	168.48	15.0	11.232	168.48	0.288	1.335	1.779	526.909
52.0	3.240	168.48	14.0	12.034	168.48	0.269	1.163	1.705	505.074

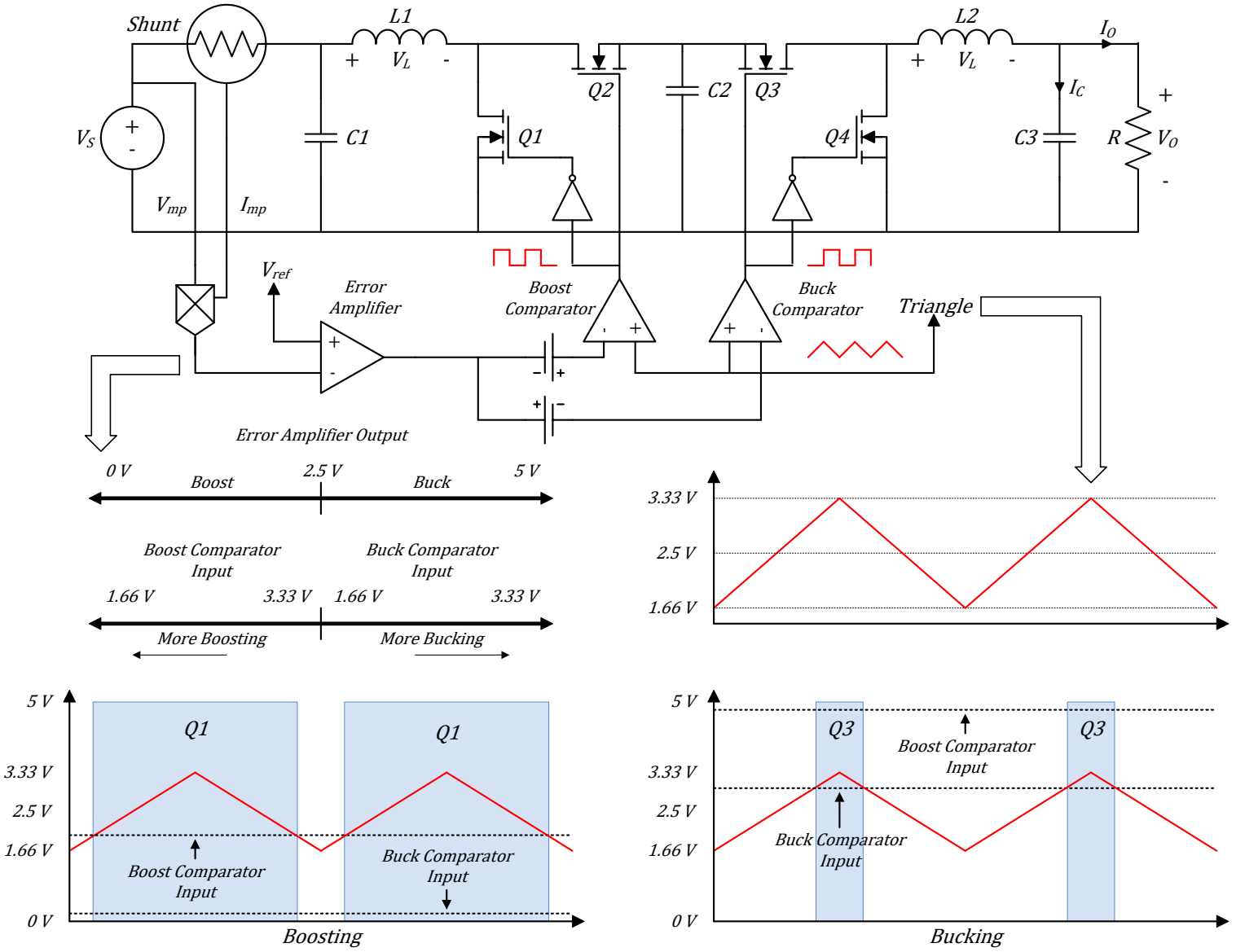
APPENDIX E: BOOST CONVERTER LOSS CALCULATIONS (IN MILLIWATTS)

D	V_{out}	$L_{1(DCR)}$	$L_{2(DCR)}$	$L_{1(core)}$	$C_{1(ESR)}$	$C_{2(ESR)}$	$Q_{1(con)}$	$Q_{2(con)}$	$Q_{3(con)}$	$Q_{1(sw)}$	$Q_{2(bd)}$	$Q_{1(g)}$	$Q_{2(g)}$	$Q_{2(rr)}$	P_{soc}	P_{ext}	P_{tot}	%
0.673	52.0	985.58	105.01	846.52	3.39	207.79	502.61	244.13	79.81	379.15	31.22	37.0	37.0	208.0	85.8	1000.0	4753.02	97.18
0.667	51.0	985.53	109.17	828.88	3.32	211.93	497.83	248.91	82.97	379.15	31.22	37.0	37.0	204.0	85.8	1000.0	4742.71	97.19
0.660	50.0	985.47	113.58	810.75	3.26	216.10	492.85	253.89	86.32	379.15	31.22	37.0	37.0	200.0	85.8	1000.0	4732.40	97.19
0.653	49.0	985.41	118.27	792.12	3.19	220.31	487.67	259.07	89.88	379.15	31.22	37.0	37.0	196.0	85.8	1000.0	4722.08	97.20
0.646	48.0	985.34	123.25	772.96	3.12	224.53	482.27	264.47	93.67	379.15	31.22	37.0	37.0	192.0	85.8	1000.0	4711.78	97.20
0.638	47.0	985.28	128.55	753.26	3.05	228.75	476.64	270.10	97.69	379.15	31.22	37.0	37.0	188.0	85.8	1000.0	4701.49	97.21
0.630	46.0	985.21	134.20	733.00	2.97	232.96	470.77	275.97	101.99	379.15	31.22	37.0	37.0	184.0	85.8	1000.0	4691.23	97.22
0.622	45.0	985.14	140.23	712.15	2.90	237.12	464.64	282.10	106.57	379.15	31.22	37.0	37.0	180.0	85.8	1000.0	4681.03	97.22
0.614	44.0	985.07	146.67	690.71	2.82	241.23	458.23	288.51	111.47	379.15	31.22	37.0	37.0	176.0	85.8	1000.0	4670.88	97.23
0.605	43.0	985.00	153.57	668.66	2.73	245.24	451.52	295.22	116.72	379.15	31.22	37.0	37.0	172.0	85.8	1000.0	4660.83	97.23
0.595	42.0	984.92	160.97	645.97	2.65	249.11	444.49	302.25	122.34	379.15	31.22	37.0	37.0	168.0	85.8	1000.0	4650.88	97.24
0.585	41.0	984.85	168.92	622.63	2.56	252.81	437.12	309.62	128.38	379.15	31.22	37.0	37.0	164.0	85.8	1000.0	4641.07	97.25
0.575	40.0	984.76	177.47	598.64	2.47	256.29	429.38	317.36	134.88	379.15	31.22	37.0	37.0	160.0	85.8	1000.0	4631.43	97.25
0.564	39.0	984.68	186.69	573.96	2.38	259.48	421.24	325.50	141.89	379.15	31.22	37.0	37.0	156.0	85.8	1000.0	4621.99	97.26
0.553	38.0	984.60	196.65	548.59	2.28	262.31	412.67	334.07	149.45	379.15	31.22	37.0	37.0	152.0	85.8	1000.0	4612.80	97.26
0.541	37.0	984.51	207.42	522.53	2.19	264.71	403.64	343.10	157.64	379.15	31.22	37.0	37.0	148.0	85.8	1000.0	4603.90	97.27
0.528	36.0	984.42	219.10	495.78	2.08	266.57	394.11	352.63	166.52	379.15	31.22	37.0	37.0	144.0	85.8	1000.0	4595.38	97.27
0.514	35.0	984.32	231.80	468.32	1.98	267.78	384.04	362.70	176.17	379.15	31.22	37.0	37.0	140.0	85.8	1000.0	4587.29	97.28
0.500	34.0	984.23	245.64	440.18	1.87	268.22	373.37	373.37	186.69	379.15	31.22	37.0	37.0	136.0	85.8	1000.0	4579.73	97.28
0.485	33.0	984.13	260.75	411.36	1.76	267.73	362.06	384.68	198.17	379.15	31.22	37.0	37.0	132.0	85.8	1000.0	4572.81	97.29
0.469	32.0	984.02	277.30	381.91	1.64	266.13	350.03	396.71	210.75	379.15	31.22	37.0	37.0	128.0	85.8	1000.0	4566.67	97.29
0.452	31.0	983.92	295.48	351.87	1.53	263.22	337.24	409.50	224.57	379.15	31.22	37.0	37.0	124.0	85.8	1000.0	4561.49	97.29
0.433	30.0	983.81	315.51	321.29	1.40	258.77	323.59	423.15	239.79	379.15	31.22	37.0	37.0	120.0	85.8	1000.0	4557.48	97.30
0.414	29.0	983.70	337.64	290.28	1.28	252.51	309.00	437.74	256.61	379.15	31.22	37.0	37.0	116.0	85.8	1000.0	4554.93	97.30
0.393	28.0	983.59	362.19	258.95	1.15	244.15	293.36	453.38	275.27	379.15	31.22	37.0	37.0	112.0	85.8	1000.0	4554.21	97.30
0.370	27.0	983.47	389.52	227.45	1.03	233.38	276.57	470.17	296.03	379.15	31.22	37.0	37.0	108.0	85.8	1000.0	4555.79	97.30
0.346	26.0	983.35	420.06	196.01	0.90	219.84	258.49	488.25	319.24	379.15	31.22	37.0	37.0	104.0	85.8	1000.0	4560.31	97.29
0.320	25.0	983.24	454.33	164.90	0.77	203.20	238.96	507.78	345.29	379.15	31.22	37.0	37.0	100.0	85.8	1000.0	4568.65	97.29
0.292	24.0	983.12	492.98	134.48	0.64	183.17	217.80	528.94	374.67	379.15	31.22	37.0	37.0	96.0	85.8	1000.0	4581.97	97.28
0.261	23.0	983.01	536.78	105.20	0.51	159.55	194.80	551.94	407.95	379.15	31.22	37.0	37.0	92.0	85.8	1000.0	4601.92	97.27
0.227	22.0	982.90	586.69	77.68	0.39	132.36	169.71	577.03	445.88	379.15	31.22	37.0	37.0	88.0	85.8	1000.0	4630.81	97.25
0.190	21.0	982.80	643.90	52.67	0.27	102.04	142.24	604.50	489.36	379.15	31.22	37.0	37.0	84.0	85.8	1000.0	4671.94	97.23
0.150	20.0	982.70	709.89	31.14	0.17	69.76	112.01	634.73	539.52	379.15	31.22	37.0	37.0	80.0	85.8	1000.0	4730.10	97.19
0.105	19.0	982.63	786.59	14.29	0.08	38.07	78.60	668.14	597.81	379.15	31.22	37.0	37.0	76.0	85.8	1000.0	4812.37	97.14
0.056	18.0	982.57	876.41	3.50	0.02	11.81	41.49	705.25	666.07	379.15	31.22	37.0	37.0	72.0	85.8	1000.0	4929.31	97.07
0.000	17.0	982.55	982.55	0.00	0.00	0.00	0.00	746.74	746.74	379.15	31.22	37.0	37.0	68.0	85.8	1000.0	5096.76	96.98

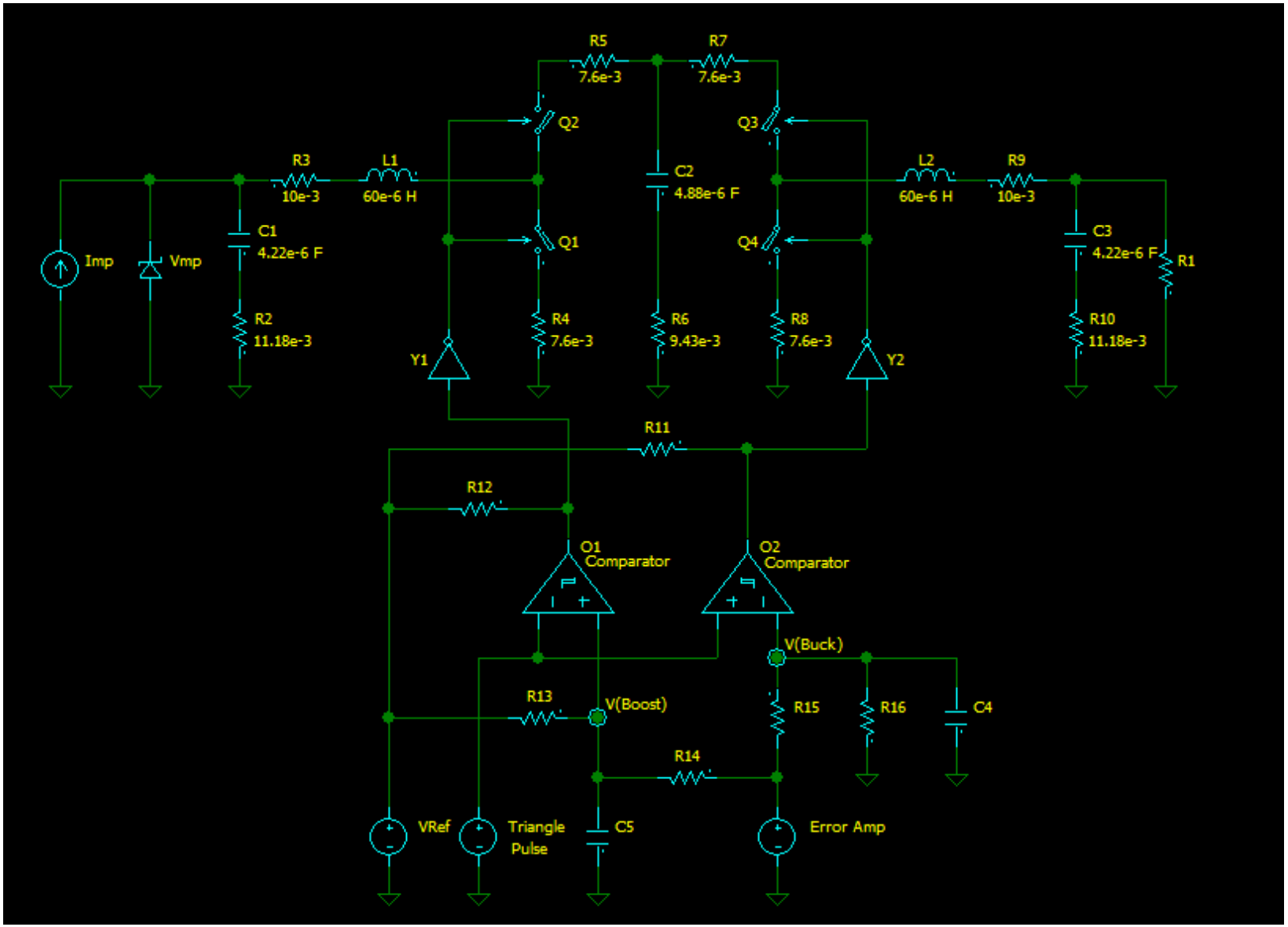
APPENDIX F: BUCK CONVERTER LOSS CALCULATIONS (IN MILLIWATTS)

D	V_{out}	$L_{1(DCR)}$	$L_{2(DCR)}$	$L_{2(core)}$	$C_{2(ESR)}$	$C_{3(ESR)}$	$Q_{2(con)}$	$Q_{3(con)}$	$Q_{4(con)}$	$Q_{3(sw)}$	$Q_{4(bd)}$	$Q_{3(g)}$	$Q_{4(g)}$	$Q_{1(rr)}$	P_{soc}	P_{ext}	P_{tot}	%
1.000	52.0	103.30	103.30	0.00	0.00	0.00	78.51	78.51	0.00	376.04	10.12	37.0	37.0	208.0	85.8	1000.0	2117.57	98.73
0.981	51.0	103.30	107.41	3.80	1.91	0.03	78.51	80.05	1.57	383.41	10.32	37.0	37.0	208.0	85.8	1000.0	2138.11	98.72
0.962	50.0	103.30	111.81	16.74	3.90	0.11	78.51	81.65	3.27	391.08	10.53	37.0	37.0	208.0	85.8	1000.0	2168.69	98.70
0.942	49.0	103.30	116.52	39.07	5.96	0.25	78.51	83.31	5.10	399.06	10.74	37.0	37.0	208.0	85.8	1000.0	2209.62	98.68
0.923	48.0	103.30	121.55	70.30	8.12	0.42	78.51	85.05	7.09	407.37	10.97	37.0	37.0	208.0	85.8	1000.0	2260.47	98.65
0.904	47.0	103.30	126.92	109.66	10.36	0.63	78.51	86.86	9.24	416.04	11.20	37.0	37.0	208.0	85.8	1000.0	2320.52	98.61
0.885	46.0	103.30	132.65	156.21	12.71	0.87	78.51	88.75	11.58	425.09	11.44	37.0	37.0	208.0	85.8	1000.0	2388.90	98.57
0.865	45.0	103.30	138.78	208.92	15.15	1.14	78.51	90.72	14.11	434.53	11.70	37.0	37.0	208.0	85.8	1000.0	2464.66	98.53
0.846	44.0	103.30	145.34	266.74	17.71	1.42	78.51	92.78	16.87	444.41	11.96	37.0	37.0	208.0	85.8	1000.0	2546.84	98.48
0.827	43.0	103.30	152.35	328.60	20.39	1.72	78.51	94.94	19.87	454.74	12.24	37.0	37.0	208.0	85.8	1000.0	2634.45	98.42
0.808	42.0	103.30	159.85	393.41	23.19	2.03	78.51	97.20	23.14	465.57	12.53	37.0	37.0	208.0	85.8	1000.0	2726.53	98.37
0.788	41.0	103.30	167.90	460.14	26.13	2.34	78.51	99.57	26.71	476.93	12.84	37.0	37.0	208.0	85.8	1000.0	2822.16	98.31
0.769	40.0	103.30	176.55	527.75	29.22	2.65	78.51	102.06	30.62	488.85	13.16	37.0	37.0	208.0	85.8	1000.0	2920.46	98.25
0.750	39.0	103.30	185.84	595.27	32.47	2.95	78.51	104.68	34.89	501.38	13.50	37.0	37.0	208.0	85.8	1000.0	3020.59	98.19
0.731	38.0	103.30	195.86	661.76	35.89	3.25	78.51	107.43	39.58	514.58	13.85	37.0	37.0	208.0	85.8	1000.0	3121.81	98.13
0.712	37.0	103.30	206.67	726.34	39.49	3.54	78.51	110.33	44.73	528.49	14.23	37.0	37.0	208.0	85.8	1000.0	3223.42	98.07
0.692	36.0	103.30	218.36	788.18	43.29	3.81	78.51	113.40	50.40	543.17	14.62	37.0	37.0	208.0	85.8	1000.0	3324.84	98.01
0.673	35.0	103.30	231.05	846.52	47.31	4.07	78.51	116.64	56.65	558.69	15.04	37.0	37.0	208.0	85.8	1000.0	3425.56	97.95
0.654	34.0	103.30	244.83	900.64	51.57	4.30	78.51	120.07	63.57	575.12	15.48	37.0	37.0	208.0	85.8	1000.0	3525.18	97.89
0.635	33.0	103.30	259.86	949.92	56.08	4.52	78.51	123.71	71.23	592.54	15.95	37.0	37.0	208.0	85.8	1000.0	3623.41	97.83
0.615	32.0	103.30	276.28	993.79	60.88	4.70	78.51	127.57	79.73	611.06	16.45	37.0	37.0	208.0	85.8	1000.0	3720.08	97.77
0.596	31.0	103.30	294.28	1031.75	65.99	4.87	78.51	131.69	89.21	630.77	16.98	37.0	37.0	208.0	85.8	1000.0	3815.15	97.72
0.577	30.0	103.30	314.08	1063.39	71.43	5.00	78.51	136.08	99.79	651.80	17.55	37.0	37.0	208.0	85.8	1000.0	3908.73	97.66
0.558	29.0	103.30	335.93	1088.37	77.26	5.11	78.51	140.77	111.65	674.28	18.15	37.0	37.0	208.0	85.8	1000.0	4001.11	97.61
0.538	28.0	103.30	360.14	1106.40	83.49	5.19	78.51	145.80	124.97	698.36	18.80	37.0	37.0	208.0	85.8	1000.0	4092.74	97.55
0.519	27.0	103.30	387.05	1117.29	90.19	5.23	78.51	151.20	140.00	724.22	19.50	37.0	37.0	208.0	85.8	1000.0	4184.29	97.50
0.500	26.0	103.30	417.10	1120.94	97.41	5.25	78.51	157.01	157.01	752.08	20.25	37.0	37.0	208.0	85.8	1000.0	4276.65	97.44
0.481	25.0	103.30	450.81	1117.29	105.20	5.23	78.51	163.29	176.36	782.16	21.06	37.0	37.0	208.0	85.8	1000.0	4371.01	97.38
0.462	24.0	103.30	488.79	1106.40	113.64	5.19	78.51	170.10	198.45	814.75	21.94	37.0	37.0	208.0	85.8	1000.0	4468.85	97.33
0.442	23.0	103.30	531.82	1088.37	122.82	5.11	78.51	177.49	223.80	850.17	22.89	37.0	37.0	208.0	85.8	1000.0	4572.07	97.26
0.423	22.0	103.30	580.83	1063.39	132.83	5.00	78.51	185.56	253.04	888.82	23.93	37.0	37.0	208.0	85.8	1000.0	4683.01	97.20
0.404	21.0	103.30	637.00	1031.75	143.80	4.87	78.51	194.40	286.97	931.14	25.07	37.0	37.0	208.0	85.8	1000.0	4804.60	97.13
0.385	20.0	103.30	701.80	993.79	155.86	4.70	78.51	204.12	326.59	977.70	26.32	37.0	37.0	208.0	85.8	1000.0	4940.48	97.04
0.365	19.0	103.30	777.10	949.92	169.19	4.52	78.51	214.86	373.18	1029.16	27.71	37.0	37.0	208.0	85.8	1000.0	5095.22	96.95
0.346	18.0	103.30	865.30	900.64	184.00	4.30	78.51	226.80	428.39	1086.33	29.25	37.0	37.0	208.0	85.8	1000.0	5274.61	96.84
0.327	17.0	103.30	969.53	846.52	200.55	4.07	78.51	240.14	494.40	1150.23	30.97	37.0	37.0	208.0	85.8	1000.0	5486.00	96.72

APPENDIX G: CONTROL BLOCK DIAGRAM



APPENDIX H: SIMULATED BOOST-BUCK SCHEMATIC



APPENDIX I: 72-CELL MODULE EFFICIENCY MEASUREMENTS

$V_{oc} = 39.816\ V$	$V_{mp} = 33.138\ V$	$I_{mp} = 1.0\ A$	$I_{sc} = 1.111\ A$				
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	1.001637	32.78006	32.83372	0.734493	43.09813	31.65527	43.0	96.41
Sweet	1.000127	32.82336	32.82751	0.972017	33.12262	32.19575	33.0	98.08
Buck	0.999232	32.87851	32.85327	1.375065	23.16618	31.85501	23.0	96.96

$V_{oc} = 41.310\ V$	$V_{mp} = 34.300\ V$	$I_{mp} = 2.0\ A$	$I_{sc} = 2.177\ A$				
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	1.982059	34.3285	68.04109	1.512028	44.17861	66.79928	44.0	98.17
Sweet	1.986017	34.2249	67.97124	1.968186	34.22358	67.35837	34.0	99.10
Buck	1.979332	34.37713	68.04376	2.744836	24.31845	66.75015	24.0	98.10

$V_{oc} = 42.194\ V$	$V_{mp} = 34.844\ V$	$I_{mp} = 3.0\ A$	$I_{sc} = 3.242\ A$				
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	2.956959	35.00541	103.5096	2.305961	44.26216	102.0668	44.0	98.61
Sweet	2.970216	34.7764	103.2934	2.984097	34.33086	102.4466	34.0	99.18
Buck	2.954676	35.03577	103.5193	4.158689	24.4685	101.7569	24.0	98.30

$V_{oc} = 42.825\ V$	$V_{mp} = 35.134\ V$	$I_{mp} = 4.0\ A$	$I_{sc} = 4.309\ A$				
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	3.931747	35.3628	139.0376	3.09531	44.34579	137.264	44.0	98.72
Sweet	3.950707	35.07563	138.5735	3.989616	34.43807	137.3947	34.0	99.15
Buck	3.931912	35.36088	139.0359	5.548653	24.61809	136.5972	24.0	98.25

$V_{oc} = 43.317\ V$	$V_{mp} = 35.290\ V$	$I_{mp} = 5.0\ A$	$I_{sc} = 5.377\ A$				
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	4.904642	35.55733	174.396	3.874825	44.42984	172.1579	44.0	98.72
Sweet	4.920373	35.30032	173.6907	4.979604	34.54503	172.0206	34.0	99.04
Buck	4.904869	35.5583	174.4088	6.908017	24.76569	171.0818	24.0	98.09

$V_{oc} = 43.720\ V$		$V_{mp} = 35.359\ V$		$I_{mp} = 6.0\ A$		$I_{sc} = 6.447\ A$	
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	5.875412	35.65224	209.4716	4.541441	45.49869	206.6296	45.0	98.64
Sweet	5.882217	35.59591	209.3829	5.811709	35.65015	207.1883	35.0	98.95
Buck	5.874196	35.65571	209.4486	7.936237	25.87718	205.3674	25.0	98.05

$V_{oc} = 44.061\ V$		$V_{mp} = 35.369\ V$		$I_{mp} = 7.0\ A$		$I_{sc} = 7.519\ A$	
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	6.844965	35.67625	244.2027	5.39873	44.59995	240.7831	44.0	98.60
Sweet	6.900047	35.28077	243.439	6.924441	34.76249	240.7108	34.0	98.88
Buck	6.84164	35.69056	244.182	9.52571	25.05784	238.6937	24.0	97.75

$V_{oc} = 44.334\ V$		$V_{mp} = 35.335\ V$		$I_{mp} = 8.0\ A$		$I_{sc} = 8.500\ A$	
$Mode$	$V_{in\ (V)}$	$I_{in\ (A)}$	$P_{in\ (W)}$	$I_{out\ (A)}$	$V_{out\ (V)}$	$P_{out\ (W)}$	$V_{Load\ (V)}$	%
Boost	7.804786	35.76974	279.1751	6.155343	44.68213	275.0338	44.0	98.52
Sweet	7.857715	35.40772	278.2238	7.881538	34.86772	274.8113	34.0	98.77
Buck	7.803805	35.77047	279.1458	10.80021	25.20199	272.1867	24.0	97.51

APPENDIX J: OVER VOLTAGE AND OVER CURRENT MEASUREMENTS

OV	$V_{out\ (V)}$	OC	$I_{out\ (A)}$
0	25.99	0	3.364
5	26.55	5	3.517
10	27.12	10	3.677
20	28.25	20	3.989
30	29.38	30	4.302
40	30.51	40	4.614
50	31.64	50	4.927
60	32.72	60	5.24
70	33.9	70	5.553
80	35.03	80	5.865
90	36.17	90	6.178
100	37.3	100	6.49
110	38.43	110	6.835
120	39.56	120	7.147
130	40.69	130	7.46
140	41.82	140	7.773
150	42.95	150	8.085
160	44.08	160	8.399
170	45.21	170	8.711
180	46.34	180	9.024
190	47.47	190	9.337
200	48.6	200	9.649
210	49.73	210	9.962
220	50.86	220	10.275
230	51.98	230	10.587
240	53.11	240	10.902
250	54.24	250	11.215
255	54.92	255	11.371