THESIS

CHARACTERIZATION OF TELLURIUM BACK CONTACT LAYER FOR CDTE THIN FILM DEVICES

Submitted by

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ABSTRACT

CHARACTERIZATION OF TELLURIUM BACK CONTACT LAYER FOR CDTE THIN FILM DEVICES

Cadmium Telluride (CdTe) thin film photovoltaic technology has shown favorable progress due to inexpensive and efficient processing techniques. However, efficiencies have yet to reach the overall projected CdTe device efficiency, with the back contact being a main source of CdTe performance limitations. Tellurium (Te) applied as a back contact has led to significant increases in fill factor and an overall progress in device efficiency. Devices deposited with Te show significant improvement in uniformity, even without intentional Cu doping, when compared to devices without Te. In current - density measurements, Te shows stability even at low temperatures, which is indicative of a low barrier developed at the CdTe/Te interface. X-ray and ultra-violet photoelectron spectroscopy were carried out to examine the valence band offset at the CdTe/Te back contact interface. The valence band offset was shown to be highly dependent on the Te thickness and was largely affected by oxidation and contamination at the surface. Capacitance measurements were carried out to study the effect Te has on the absorber depletion width. Data indicate a decreased depletion width with Te applied at the back of thin film CdTe devices, which agrees with increased device performance. Te thickness was varied in all studies to understand the effect of application thickness on device performance and material characteristics. With a thicker Te layer leading to overall improvement in device performance and favorable device characteristics.

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1 INTRODUCTION

1.1 Energy Demand

Global energy consumption is predicted to increase nearly 30% from 575 quadrillion BTUs (quads) in 2015 to 736 quads in 2040 [1]. Renewable technologies have gained worldwide support over the last decade in order to cut dependence on energy sources that not only have finite reserves but also contribute significantly to the increase in CO_2 emissions. Global CO_2 emissions are expected to increase at a rate smaller than that seen in previous years. Between 2015 and 2040, the average rate is projected to be 0.6% per year, slightly decreased from 1.3% per year between the years 1990-2015 (Figure 1) [1]. This decrease in emission rate is a direct result of the surge in renewable energy use over the last decade.

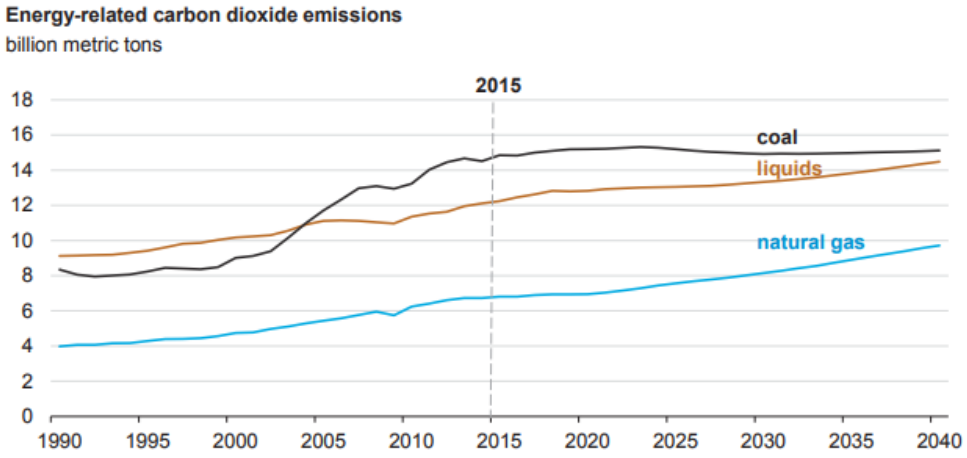

Figure 1: Carbon dioxide emissions [1]

1.2 Renewable Energy

Renewable energy continues to get cheaper due to increased funding and support from the public. Consistent increases in the efficiencies of renewable energy technologies has led to a significant rise in electricity generation of these technologies compared to that of traditional sources. Renewable energy is predicted to contribute 30% of the global power generation by 2022 (Figure 2)[2].

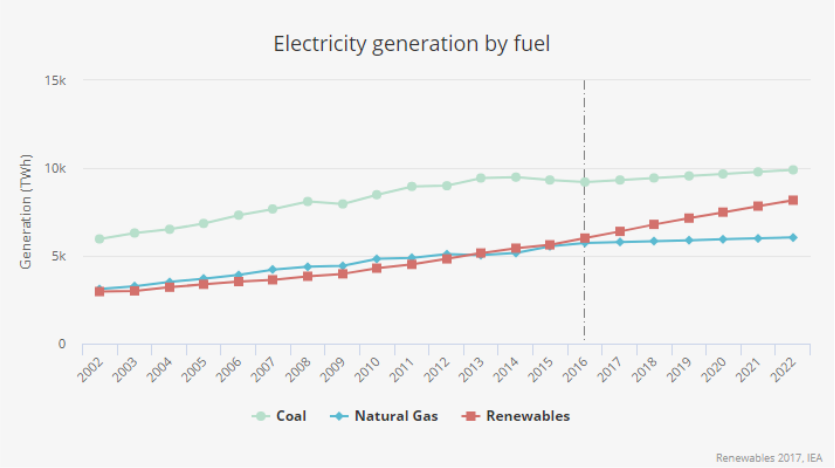

Figure 2: Electricity generation of different energy sources from 2002-2022 [2]

In 2016, solar energy saw the largest rise in capacity among not only renewable technologies but also traditional fuel sources. Renewable energy growth is expected to continually rise, with an increase of 43% expected by 2022, driven for the most part by solar growth [2]. Solar prices have also significantly dropped over the last several years (Figure 3), with average module prices at $0.32/W [3].

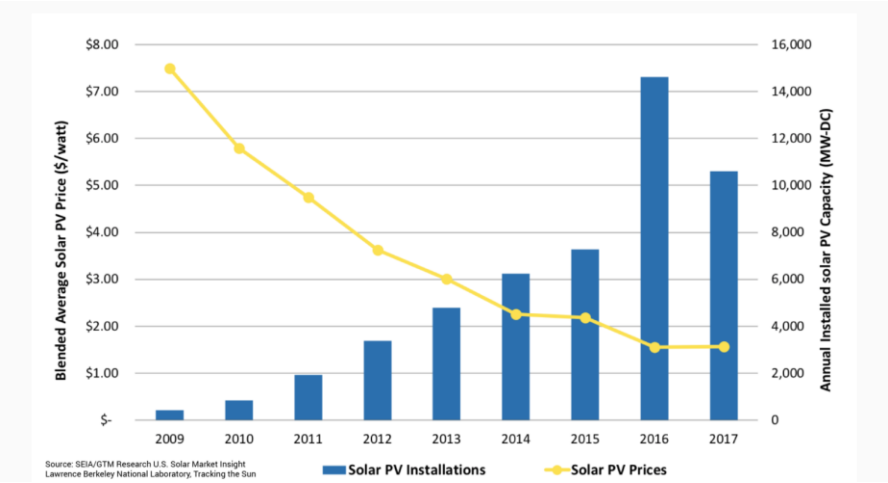

Figure 3: Trend of increasing solar installations with decreasing solar prices from 2009-2017 [4]

Thin film CdTe photovoltaics have not only the smallest carbon footprint of all solar technologies, but also the fastest energy payback time (Figure 4). For these reasons, CdTe has become an increasingly attractive solar technology.

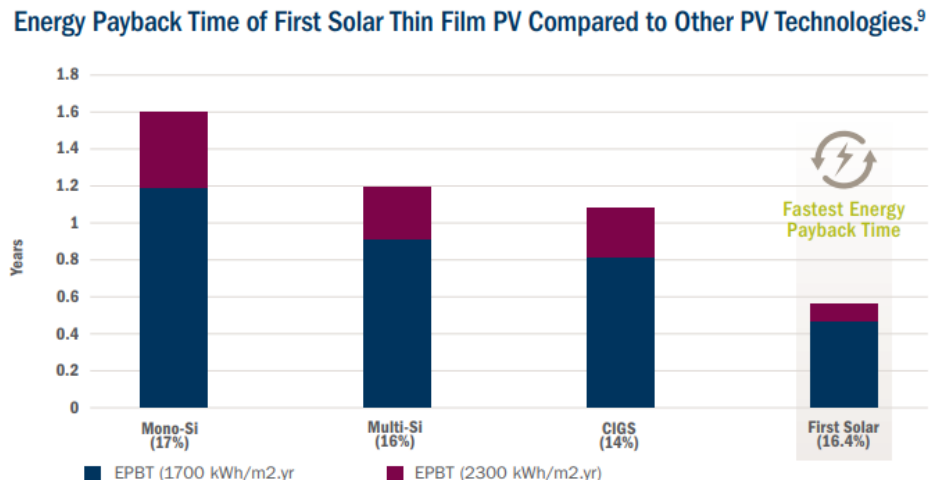

Figure 4: Energy payback time of different photovoltaic technologies [5]

First Solar Inc. is a leading CdTe photovoltaic module manufacturer, with demonstrated module efficiencies as high as 18.6% [6] . They have demonstrated record device efficiencies at 22.1% [7], with continued research efforts on further improving device performance.

1.3 PV Fundamentals

A semiconductor is often defined by its band gap (E_g), or the amount of energy required to create mobile charge carriers. The band gap defines the distance between the conduction (E_C) and valence (E_v) bands and in this region no charge carriers can exist. The valence band is the highest energy level that electrons occupy. If enough energy is absorbed, electrons can move from the valence band to the conduction band, leaving behind a hole. The Fermi level (E_F) lies between the two bands and its position depends on the concentration of charge carriers. The Fermi level has a 50% chance of being occupied by carriers at any temperature. Energy levels existing below the valence band are considered core levels (E_{CL}) and each material has its own well-defined core levels. The electron affinity (χ) of a semiconductor defines the amount of energy required to remove an electron from the conduction band to the vacuum level [8](Figure 5).

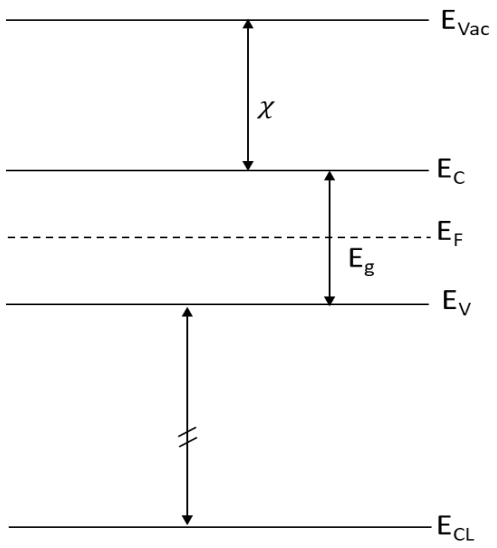

Figure 5: Energy band diagram of an intrinsic semiconductor

In a direct band gap semiconductor, the maximum valence band energy level and minimum conduction band energy levels are aligned with respect to momentum. An electron-hole pair is made easily in a direct band gap semiconductor, because the electron requires little momentum. However, radiative recombination is much more likely in these semiconductors. Common direct band gap semiconductors include GaAs and CdTe. In an indirect band gap semiconductor, the maximum valence band energy level and the minimum conduction band energy levels are misaligned with respect to momentum. These semiconductors require interaction with not only a photon but also a phonon, to conserve energy and momentum within the bands (Figure 6). Common indirect band gap semiconductors include Si and Ge [9].

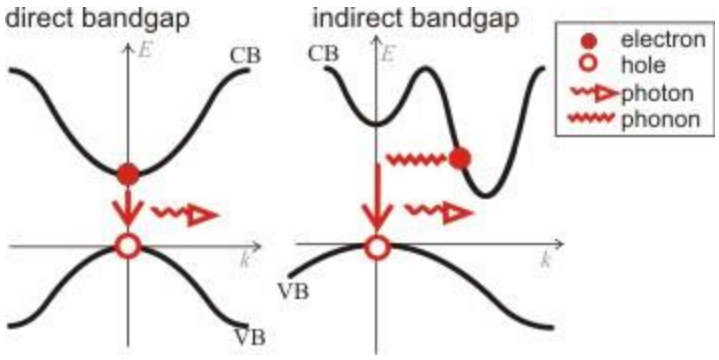

Figure 6: Direct vs. indirect band gap semiconductors [10]

The electrical conductivity of a semiconductor is controlled by the number of electrons and holes in their respective bands. In intrinsic semiconductors, the number of holes in the conduction band is equal to the number of electrons in the valence band and the Fermi level lies directly in between the bands (Figure 5). Intrinsic semiconductors are not useful for generating electricity due to the equal distribution of carriers, which causes the semiconductor to act like an insulator. In extrinsic semiconductors, impurities, or dopants, are introduced into the material. Impurities are either referred to as donors or acceptors depending on the charge of the impurity. Acceptors dopants "accept" an electron from the valence band, leaving behind a hole. This type of semiconductor is referred to as p-type and the majority carrier is holes. In n-type semiconductors, the donor dopants "donate" an electron to the conduction band, therefore the majority carrier of electrical conduction is electrons [9]. In p-type semiconductors, the Fermi level lies close to the valence band. The concentration of holes in the valence band is greater than the concentration of electrons in the conduction band, thus the Fermi has a greater chance of being occupied near the valence band. Similarly, in n-type semiconductors, the Fermi will lie closer to the conduction band due to the higher concentration of electrons (Figure 7). Higher dopant concentration will lead to the Fermi level shifting closer to the corresponding band.

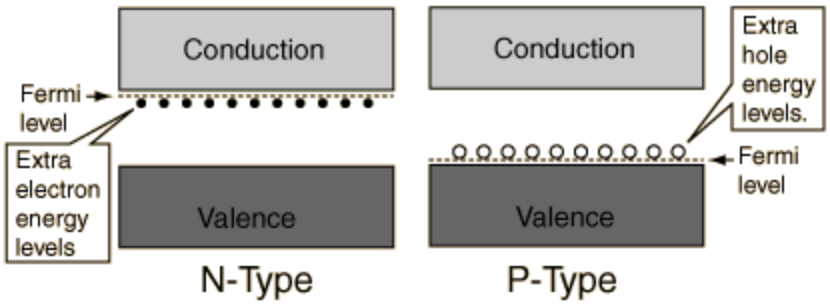

Figure 7: N-type vs. p-type semiconductor [11]

A p-n junction semiconductor is formed by bringing together an n-type and p-type semiconductor. When the junction is formed, electrons will diffuse to the p-type region and holes will diffuse to the n-type region. As the carriers diffuse across the junction, charge impurities are uncovered, and an electric field is produced in the transition region between the two semiconductors. This region limits carrier diffusion and is referred to as the depletion region, as it is depleted of any free charge carriers. A built-in voltage ($q\phi$), forms at the junction due to the electrostatic difference between the depletion region and the regions existing on either side of the depletion region, often called the quasi-neutral regions [9].

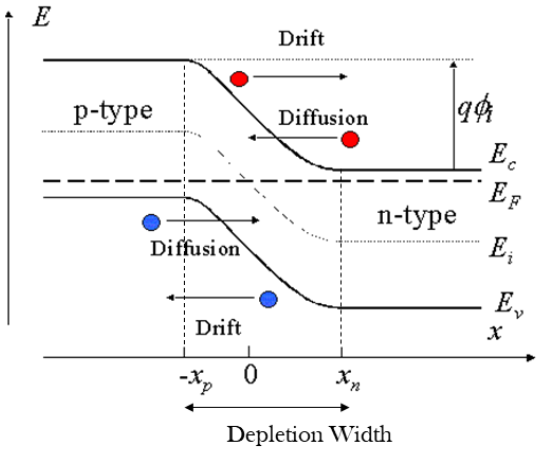

Figure 8: Band Diagram of p-n Junction [12]

For a p-n semiconductor in equilibrium, the carrier drift and diffusion balance out and the net current for the semiconductor is zero (Figure 8). When a voltage bias is applied across a uniformly doped semiconductor, the bands will bend in the direction of the applied voltage. In the conduction band,

electrons will move opposite the direction of the applied voltage, while holes in the valence band will move in the direction of the applied voltage. When a forward bias is applied to a p-n junction, an electric field is formed with opposing polarity to that of the depletion region. In forward bias, the depletion region decreases, which eases carrier diffusion across the junction and results in an increased diffusion current. In reverse bias, the electric field is in the same direction as the depletion region, thus the depletion region increases and diffusion current decreases.

A solar cell is a simply a p-n semiconductor diode that directly converts sunlight, or photons, into electrical energy. For a photon to be absorbed, the photon must have energy equal to or greater than that of the band gap of the semiconductor. When a photon is absorbed within the semiconductor it will excite an electron from the valence band to the conduction band, creating an electron-hole pair. Photovoltaic devices are fabricated from a wide variety of semiconductor materials. All photovoltaic semiconductor materials have absorption characteristics that match well with the solar spectrum [9]. The most common solar devices are made from Silicon (Si), which is an indirect band gap semiconductor. Si based solar devices requires a relatively thick absorber layer to effectively absorb photons. Thin film photovoltaic technology has become popular due to the limited amount of material required for effective absorption. GaAs and CdTe are two common thin film semiconductor materials used in photovoltaics, both are direct band gap semiconductors.

The Shockley-Queisser limit defines the maximum efficiency achievable in a single p-n junction semiconductor as a function of its band gap [13]. The limit assumes the standard global spectrum of AM1.5 (Figure 9a), which is the standard for measuring solar devices. The AM1.5 spectrum is normalized to a power density of 1000 W/m^2 and takes in to account light that is scattered and reflected in the earth's atmosphere. The Shockley-Queisser limit also accounts for other loses, including recombination and spectrum loses. The maximum achievable efficiency of single junction photovoltaic devices is

estimated at 33.7% [13] (Figure 9b). The limit assumes a single junction and one sun; therefore, these efficiencies can be exceeded when multiple junctions or solar concentrators are used.

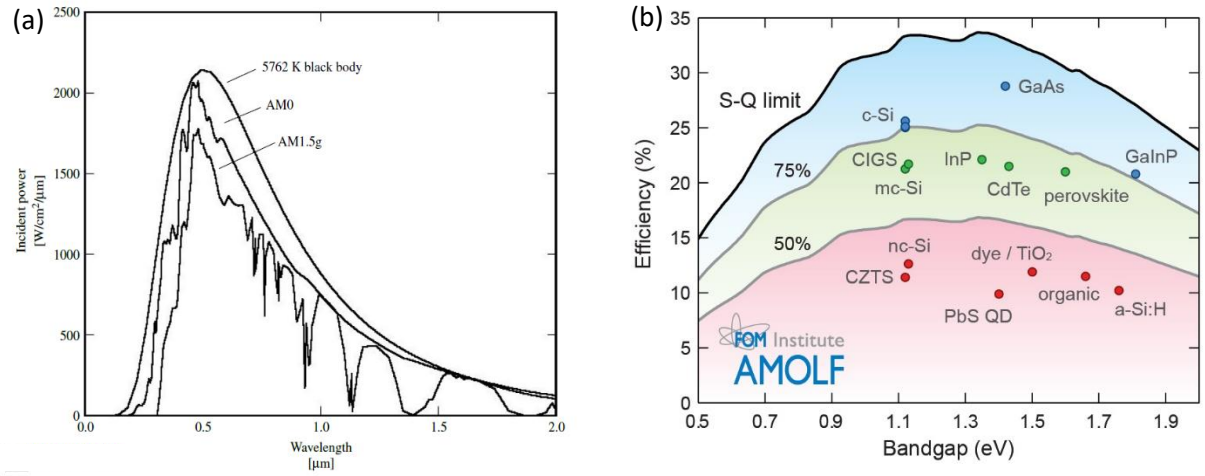

Figure 9: (a) Earth's radiation spectrum [9] *and (b) Shockley-Quessier limit with record efficiencies for common photovoltaic materials* [14]

1.4 CdTe PV

Cadmium Telluride (CdTe) has been largely successful in the thin film photovoltaic market. CdTe is a direct band gap (E_g= 1.5 eV) [15] semiconductor with a high absorption coefficient, therefore minimal material (~1 µm) is required for near complete absorption of incident photons. CdTe is used as a p-type absorber in photovoltaic devices, with either CdS or MgZnO (MZO) as the n-type emitter. Record efficiencies have yet to approach the CdTe theoretical limit (~30%)[16], with current research efforts focused on improving the back contact, incorporation of an electron reflector and increasing hole density.

1.5 Motivation

The development of high quality back contacts is essential to improve thin film CdTe device performance. The back contact has been a source of poor cell performance, largely due to the high electron affinity of CdTe (4.3 eV) [17]. An ideal back contact would form an ohmic contact with the p-n

diode, which eases carrier flow through the device. For an ohmic contact to form, it's necessary for the work functions between the two to closely match. A mismatch in work function leads to bending in the conduction and valence bands, for Fermi alignment (Figure 10). Since CdTe has a work function typically much greater than most materials used as back contacts, the valence and conduction band will bend downward to align the Fermi levels. This creates an energy barrier, often referred to as the valence band offset, which impedes carrier flow.

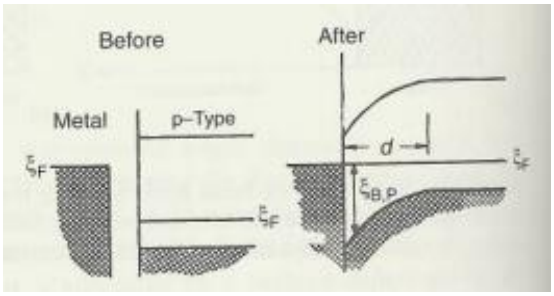

Figure 10: Schottky Barrier of p-type semiconductor and metal

Carbon is typically applied as the back contact in CSU fabricated devices. The carbon back contact is applied through a spray application with a thickness ~5μm. Carbon back contacted devices exhibit particularly poor device performance, which is apparent in a low fill factor. The carbon contact forms a valence band offset with CdTe, which limits overall current output. In J-V-T analysis of an MZO(100 nm)/CdTe(2.5 μm)/CdCl2/Cu/C/Ni device (Figure 11) the onset of rollover occurs at fairly high temperatures, with the contact barrier having a significantly greater negative effect on the fill factor of devices at low temperatures. Roll-over occurring below V_{OC} indicates a barrier formed at the junction that impedes reverse current. A barrier to reverse current limits the device's ability to collect current as well as ultimately lowers the V_{OC} of the device due to enhancement of forward current [18].

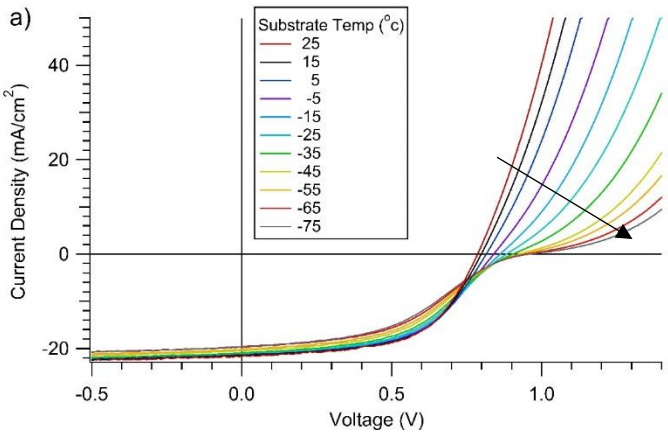

Figure 11: J-V-T of Cu doped baseline device with carbon back contact (arrow in the direction of decreasing temperature) [19]

The incorporation of a Tellurium (Te) back contact layer has shown significant improvement in device quality, most notably, an increase in fill factor of devices, which suggests a lower barrier formed at the back contact junction. The impact Tellurium presents on device performance will be explored in Sect. 2.

2 EXPERIMENTAL DETAILS

2.1 Device Fabrication

Many technologies, such as closed space sublimation (CSS), vapor transport, sputtering and physical vapor deposition, are compatible for CdTe deposition due to its' chemical stability and high formation enthalpy [15]. The Next Generation Photovoltaic Center at Colorado State University develops thin film devices with continuous in-line fabrication utilizing CSS (Figure 12)[20]. The system allows for versatility in the substrate deposition process.

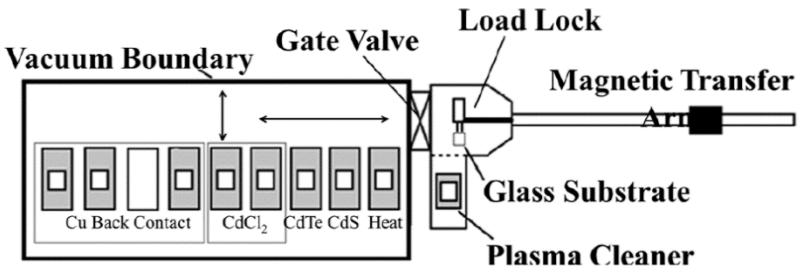

Figure 12: Schematic of single vacuum closed space sublimation Chamber [20]

CdTe devices are deposited in a superstrate structure, with light entering through the glass side. Devices are fabricated on commercially available 3.6" x 3.1" TEC10 soda-lime glass, coated with SnO_2:F. The device structure can be seen in Figure 13, where, MgZnO (MZO), the emitter layer, is deposited by RF sputtering at 100 nm. This is followed by a 2.2-2.6 μm CdTe absorber layer, and subsequent post-treatments with $CdCl_2$ and Cu doping. A 50 nm Te back contact layer is deposited by evaporation in an argon rich environment that is held at 10^{-5} Torr. The thickness is monitored by an R.D. Mathis quartz crystal and can be varied with deposition time. This is followed by Carbon and Nickel paint, which are deposited through a spray application and make up the remaining back contact of the device.

At Colorado State University record efficiencies have reached 18.7% [21], through the use of higher deposition temperatures and a thicker absorber layer.

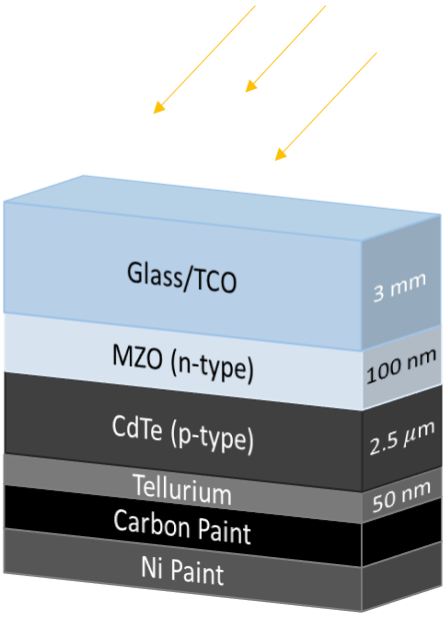

Figure 13: Baseline CdTe device fabricated at CSU

2.2 Device Characterization

Solar device quality is characterized by several electrical and material characterization techniques. For the purposes of understanding the CdTe and back contact interface the techniques used were as follow; Current Density vs. Voltage (J-V), Capacitance (C-F and C-V), Electroluminescence (EL), Current Density vs. Voltage with temperature bias (J-V-T), X-ray and Ultra-violet Photoelectron Spectroscopy (XPS and UPS).

2.2.1 Current Density vs. Voltage (J-V)

In J-V measurements, a solar device at 25°C is illuminated by a light source at standard AM1.5 conditions [22]. A DC voltage is incrementally applied at a range of biases while current output is measured. The current is normalized to a current-density value, which removes the dependence of solar cell area and allows for more accurate comparison among devices. Essential devices parameters found from J-V measurement include: short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), fill factor (FF) and efficiency (η) [22]. J_{SC} is current measured through the device when the voltage bias is zero. V_{OC}

is the voltage bias when no current flows through the device. Fill factor (FF) is the ratio of the maximum power output at V_{MP} and J_{MP} to the theoretical power output at V_{OC} and J_{SC} (Equation 1). Fill factor is essentially the "squareness" of the J-V curve and describes the quality of the solar device (Figure 14) [23].

$$FF = \frac{J_{MP}V_{MP}}{J_{SC}V_{OC}} \quad (1)$$

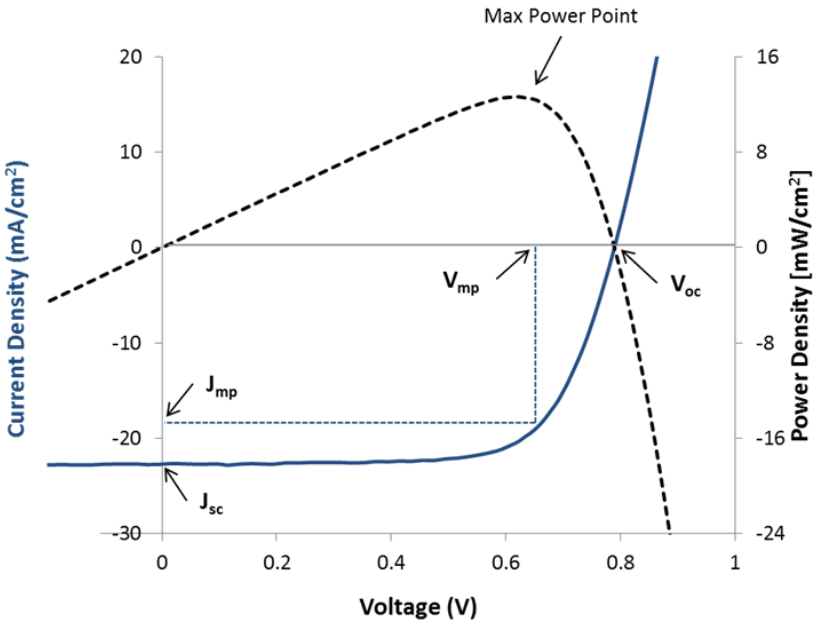

Figure 14: Current Density vs. Voltage Curve [19]

Efficiency (η) is a commonly used parameter to compare device performance and it is directly related to the V_{OC}, J_{SC}, and fill factor. Efficiency is simply the ratio of the power output of the device to the power input (Equation 2).

$$\eta = \frac{FFV_{OC}J_{SC}}{P_{in}} \quad (2)$$

2.2.2 Temperature Dependent Current Density vs. Voltage (J-V)

J-V-T measurements utilize the same concepts presented in Sect. 2.2.1. Measurement are taken at interval temperatures, typically 10°C intervals, while measuring the current output of the device. A Peltier device is used to control temperature, while a fan is used for forced cooling. At relatively low temperatures, liquid nitrogen and nitrogen gas are utilized. This allows measurements to be obtained at temperatures as low as -65°C. As temperature decrease, barriers become much more apparent in the device and make them easier to identify.

In J-V-T analysis, the turning current, J_T, is the inflection point of the curve and if it occurs in forward bias, it is often a result of a barrier at the back contact of the device and is referred to as the rollover effect [24]. The turning current, which in this case can also be referred to as the saturation current at the back contact, $J_{O,bc}$, can be found by applying a linear fit, above and below the inflection point and finding the intersection of the two lines (Figure 15).

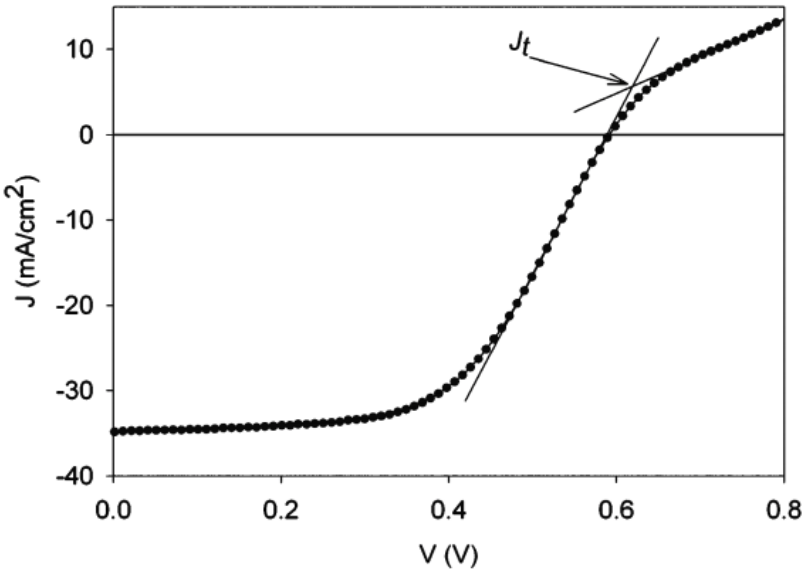

Figure 15: Fit of the turning current density [24]

The back barrier height can be solved using Equation 3, assuming rollover is prominent at low temperatures and J_t is greater than zero [25].

$$J_{0,bc} = J_t = A^* T^2 e^{\frac{-q\phi_b}{kT}} \quad (3)$$

where A* is the effective Richardson constant, for CdTe, $A^* = 12\ \frac{A}{cm^2K^2}$, T is the applied temperature bias, ϕ_b is the back barrier height, k is the Boltzman's constant, and q is the elementary charge.

2.2.3 Capacitance Measurements

In capacitance measurements, a diode is modeled as a parallel plate capacitor, and from this information about the bulk and interface properties within the device can be obtained [26]. Capacitance-voltage (C-V) profiling is useful for characterizing carrier density, depletion width of the absorber and barriers present in the semiconductor [27]. The absorber depth over the free carrier density profile can be obtained from Equation 4 [27].

$$N_{CV}(W_{CV}) = \frac{2}{q\varepsilon}\left[\frac{dC(V)^{-2}}{dV}\right]^{-1} \quad (4)$$

where q is the elemental charge, ε is permittivity, V is the voltage bias, and C(V) is the capacitance per unit area. W_{CV} is the depletion width of the absorber and is defined by Equation 5 [27].

$$W_{CV} = \frac{\varepsilon}{C(V)} \quad (5)$$

The capacitance model accurately models the carrier density profile assuming; the depletion width is less than the absorber thickness, the back contact junction is ohmic, and only shallow level defects exist in the semiconductor [27]. In the case where all assumptions are met, the $C(V)^{-2}$ vs. voltage plot, or Mott-Schottky plot, is given by the solid linear line (Figure 16). However, for polycrystalline thin films, such as CdTe, most or all of these assumptions are violated. Most relevant to understanding the effect on the depletion width, is that CdTe is deposited at a finite thickness and that there is a non-ohmic contact at the back junction, which introduces an additional junction, often referred to as the Schottky diode. At zero bias, it is possible for CdTe devices to be fully depleted due to finite thickness, which

presents itself as the “punch through” feature (Figure 16). The additional junction manifests as the voltage sharing feature (Figure 16).

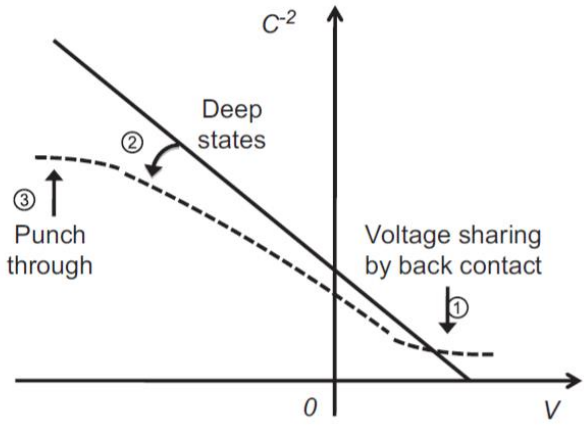

Figure 16: Mott Schottky plot of ideal (solid line) solar device and thin film (dotted line) solar device [27]

2.2.4 Electroluminescence

In electroluminescence (EL) measurements, a forward electrical bias is applied to the solar device and the emission response is imaged. EL simply operates the solar device in the reverse operation of the photovoltaic effect. EL provides visual representation of microscopic defects in the solar device. EL is performed in an enclosed space, to eliminate ambient light, and under constant current at 40 mA/cm^2[28]. The devices are imaged using a Silicon charge-coupled device (CCD) camera which is cooled to 25°C (Figure 17).

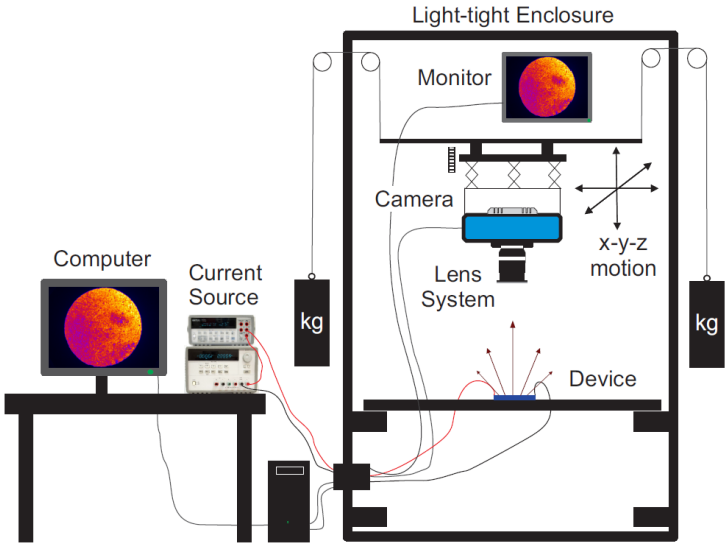

Figure 17: EL setup at Colorado State University [28]

2.2.5 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy is a useful analysis technique for determining important material characteristics within a device. XPS probes only the surface (~5-10nm) of a sample and therefore is a highly surface sensitive measurement. Contamination and oxidation can greatly affect results, therefore careful sample preparation is necessary to obtain meaningful data. In XPS analysis, the surface of the sample is irradiated with x-rays (1486.6 eV for Al Kα anode) which are absorbed by atoms from the core levels of the material present in the sample. This results in the ejection of electrons at these core levels, which are detected, and their kinetic energies measured by an electron energy analyzer (Figure 18). Binding energies of the electrons are determined utilizing the known energy of the x-ray and the measured kinetic energy of the emitted electron.

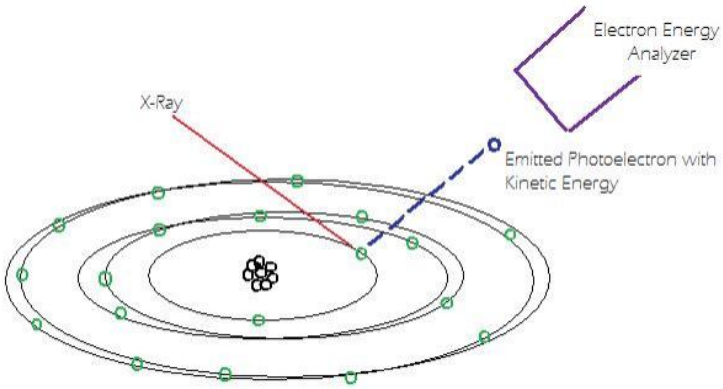

Figure 18: X-ray Photoelectron Spectroscopy Schematic [29]

Binding energies are measured with respect to the Fermi level (E_F=0). XPS data is provided by a graph of binding energies vs. counts per second, or relative intensity. Binding energies define the inherent elements and elemental bonding present in the sample. Each element is described by a set of peaks occurring at specified binding energies.

2.2.6 Ultra-violet Photoelectron Spectroscopy

Ultra-violet photoelectron spectroscopy (UPS) operates in a fairly similar way to that of XPS. Ultra-violet rays are utilized to bombard the surface of the sample and the probed electronic states are occupied valence levels. Typically, a Helium (He) discharge lamp emits radiation as its UV source. UPS has a much smaller energy range (~10-45 eV), allowing for a much higher resolution. From UPS spectra, the work function as well as the difference between the Fermi level and the valence band maximum can be determined.

In UPS, the valence band is typically the energy level of interest. The valence band is fit by linearly extrapolating the leading edge of the valence band. The valence band offset can be determined using Equation 6 [30].

$$E_{VBO} = (E_{CL}^{x} - E_{VBM}^{x}) - \left(E_{CL}^{y} - E_{VBM}^{y}\right) - \Delta E_{CL} \quad (6)$$

where E_{CL} is the core level binding energy of material and E_{VBM} is the valence band maxima of both species *x* and *y*. ΔE_{CL} is described in Eqn. # and is the difference in core levels of *x* and *y*, measured from the interface [30].

$$\Delta E_{CL} = E_{CL}^{x} - E_{CL}^{y} \quad (7)$$

3 TELLURIUM BACK CONTACT LAYER

A tellurium back contact layer incorporated in CdTe devices shows an increase in the device quality. Te is characterized as degenerate p-type semiconductor with a band gap of 0.33 eV. Te can be prepared either through evaporation or chemical etching. At fairly low thickness (<8 nm) Te exhibits n-type behavior due to the defect levels in CdTe dominating the conductivity type at the surface. For favorable electrical characteristics the Te thickness must be sufficient enough to exhibit bulk properties. The threshold for p-type characteristics is suggested as >8 nm [31].

The Te back contact displays a noticeable improvement in the fill factor compared to that over other metal back contacts. J-V-T measurements indicate that Te is stable at varying temperatures, with little variation in fill factor, even at low temperatures (Figure 19). The evidence provided proposes that a relatively low barrier is formed.

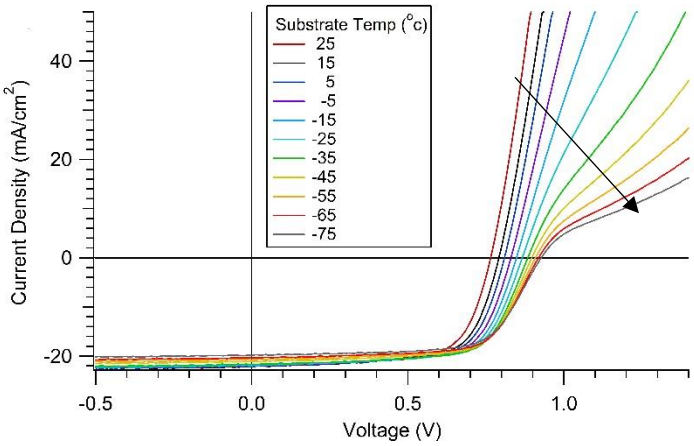

Figure 19: J-V-T of CSU baseline CdTe device with arrow in direction of decreasing temperature [19]

In previous work, the CdTe/Te valence band offset has been studied and reported by a variety of groups. For devices fabricated in situ, a valence band offset as low as 0.26 eV has been found [31]. A modeled energy band diagram of the interface shows that the Te bends the valence and conduction bands down [17], which likely attributes to the favorable device performance observed.

In this study, the Te thickness was varied and the effect studied with baseline CdTe devices both with and without intentional Cu doping. The Te buffer layer was deposited at 50 nm, 25 nm, 10 nm, 5 nm and 0 nm.

3.1 Effects of Cu Doping on Devices with Variation in Te Thickness

Cu is introduced into thin film CdTe devices with the intent to increase hole concentration in CdTe, however even with Cu doping, CdTe's bulk carrier concentration is low. Cu can exist as both a deep level acceptor, in the form of a substitutional impurity, Cu_{Cd}, and a shallow donor, in the form of an interstitial impurity, Cu_i. Cu_i diffuses quickly in the CdTe, which leads to stability issues and likely is the source of lower bulk doping concentrations seen in CdTe.

Despite low doping density, Cu shows improvement in the performance of devices fabricated at CSU. Doping with Cu reduces the effect of the back barrier and leads to significantly increased fill factor.

This section discusses devices with the traditional device configuration with and without the introduction of Cu dopant. The Te buffer layer is deposited at varying thicknesses. The semiconductor was made up of the standard 100 nm MZO (n-type) and 2.6 µm of CdTe (p-type). All devices were passivated with $CdCl_2$. The back contact was made up of a Te back contact layer and C/Ni paint.

3.1.1 Device Performance

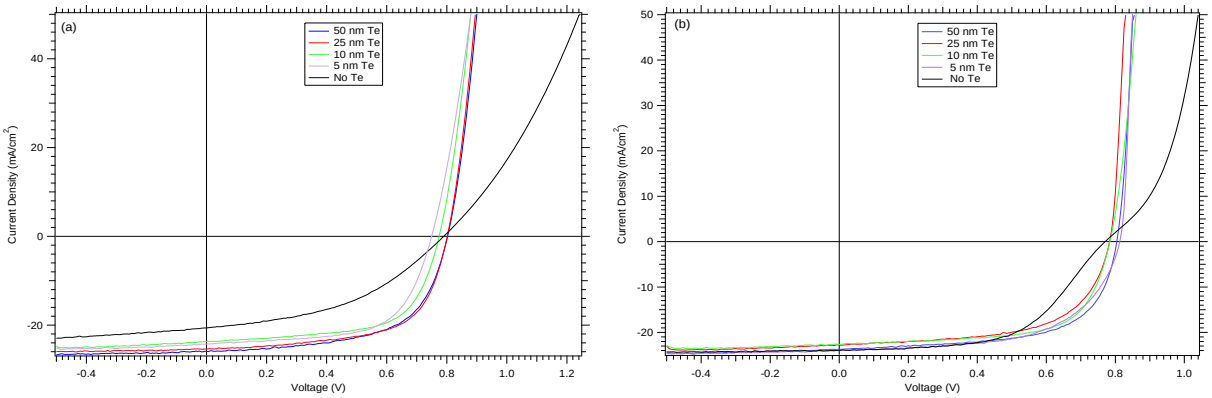

Figure 20: J-V of CdTe devices (a) with intentional Cu doping and (b) without intentional Cu doping with varying Te thickness

For devices treated with Cu, there is little difference in the J-V characteristics of the 50 nm and 25 nm devices. A decrease in efficiency is seen with a decreasing Te thickness. The devices show little difference among the fill factor and J_{SC}, with major losses only apparent in the V_{OC}. Low V_{OC} is indicative of large contact barrier that impedes carrier flow. As indicated in Table 1, this barrier becomes significantly larger as the Te thickness decreases. The device with no Te shows poor device performance, however a kink in not visible, likely due to the presence of Cu in the device (Figure 20a).

Table 1: Cell Performance Parameters of Cu Doped Devices

Te Thickness	V_{OC} (mV)	J_{sc} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
50 nm	816	26.4	62.5	13.4
25 nm	814	26.2	63.2	13.4
10 nm	797	24.7	64.5	12.6
5 nm	776	25.1	63.7	12.3
No Te	795	20.9	43.5	8.0

For devices with no intentional Cu doping, there is a larger difference in the J-V parameters among all the devices. The 50 nm Te device has the greatest efficiency at 12.3%, as well as the highest V_{OC} of 800mV. There seems to be a general trend between the Te thickness and device performance, with efficiency decreasing with Te thickness.

Table 2: Cell Performance Parameters of Devices w/o Cu

Te Thickness	V_{OC} (mV)	J_{sc} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
50 nm	800	23.0	65.3	12.3
25 nm	778	21.2	66.6	11.5
10 nm	770	21.0	64.0	10.8
5 nm	773	20.5	63.3	10.5
No Te	753	22.6	52.6	9.0

3.1.2 EL Characteristics

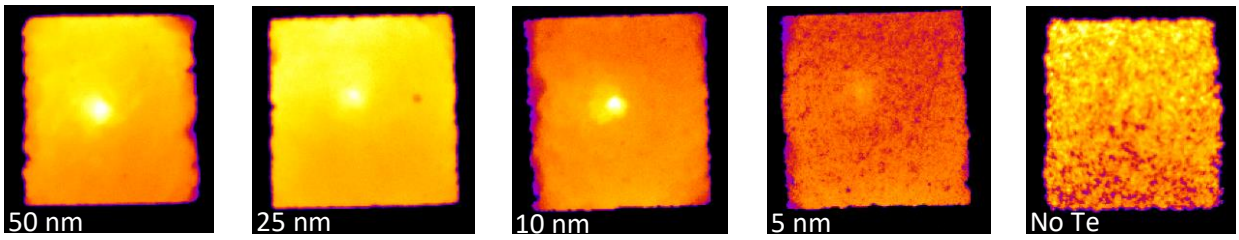

Figure 21: EL of devices w/ intentional Cu doping

The EL provides a visual representation of device performance and uniformity of the back contact layer. The device with no Te back contact layer, is non-uniform, with areas of low signal and high signal dispersed throughout the device (Figure 21). This indicates that the C paint is not in complete contact with the CdTe. The Te mitigates the grainy appearance and device quality improves as the layer gets thicker. Devices with the Te layer appear much more uniform and the Te makes complete contact with the CdTe. The bright spot, near the center, corresponds to the probe that contacts the back contact of the device in the EL setup. It is a result of not having a thick enough layer of Ni paint at the back, rather than non-uniform device performance.

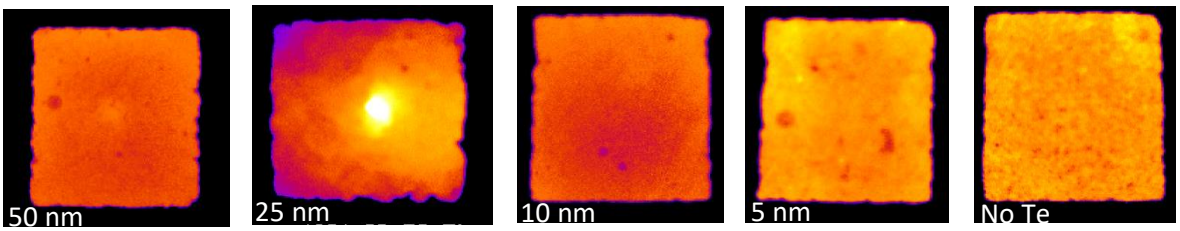

Figure 22: El of devices w/o intentional Cu doping

The EL shows significantly decreased device quality in the devices deposited without Cu (Figure 22) compared to those with Cu doping (Figure 21). The devices share similar uniformity issues with decreasing Te thickness. The devices with thinner Te exhibit a grainy appearance which is consistent with poor contact between the back contact and the CdTe.

3.1.3 J-V-T Analysis

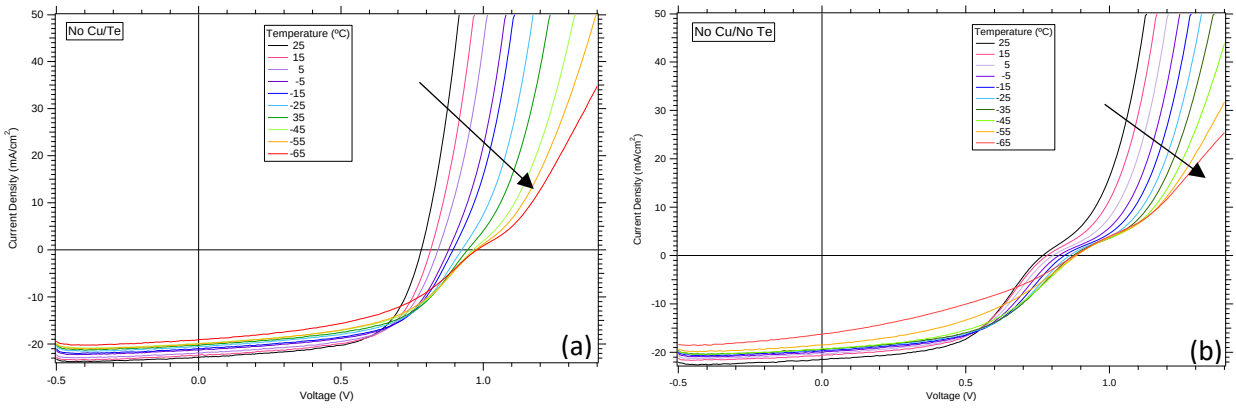

Figure 23: J-V-T of devices with no intentional Cu doping (a) with 50 nm Te back contact and (b) no Te back contact. Arrows in the direction of decreasing temperature bias.

Rollover in the J-V-T of devices with no intentional Cu doping is not apparent until -25°C in the device with the Te back contact (Figure 23a). Rollover is significantly worse in device with no Cu doping and no Te back contact as the temperature decreases (Figure 23b). At lower temperatures, it becomes more difficult for carrier diffusion. Carriers will require more energy to overcome barriers present in the device. At low temperatures, both devices show rollover, likely caused from the back barrier.

3.1.4 Depletion Width Analysis

In the C-F curves for Figure 25a, the device without Te, show increased dispersion at different voltage biases, which is indicative increased defects in the device. The C-F curves for the device with Te (50 nm) all lie flat with one another which indicate good contact between the back contact and CdTe.

Similarly, the device without Cu shows far more dispersion than the device with Cu doping as seen in Figure 24b.

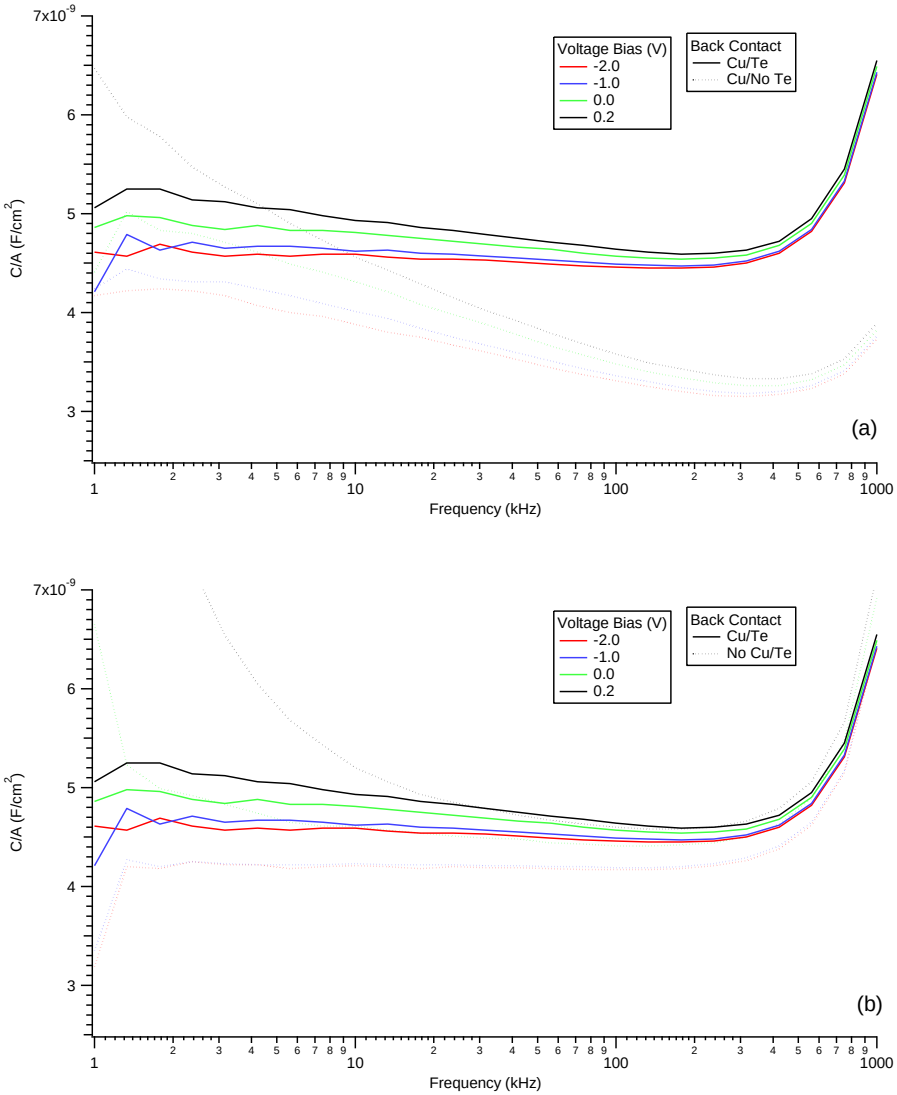

Figure 24: C-F curves at voltage biases 0f -2V, -1V, 0V and 0.2V for (a) Cu doped devices w/ and w/o Te back contact and (b) Te back contacted devices w/ and w/o Cu

In general, for thin film CdTe devices, the C-V curve is represented by a general U-shape, where the left branch correlates to the forward bias and the right branch correlates to the reverse bias. The depletion width directly affects the onset of the right branch. The larger the back contact barrier height, Φ_{bc}, the earlier punch through occurs. This suggests the depletion width is smaller with a greater back contact barrier [27], which is not consistent with results found in this research. The left branch of the curve is affected by the saturation current density of the Schottky diode at the back, $J_{o,bc,}$. A smaller

saturation current equates to a sharper upturn in the curve. Figure 25a and b displays the C-V curves for devices with and without Cu doping.

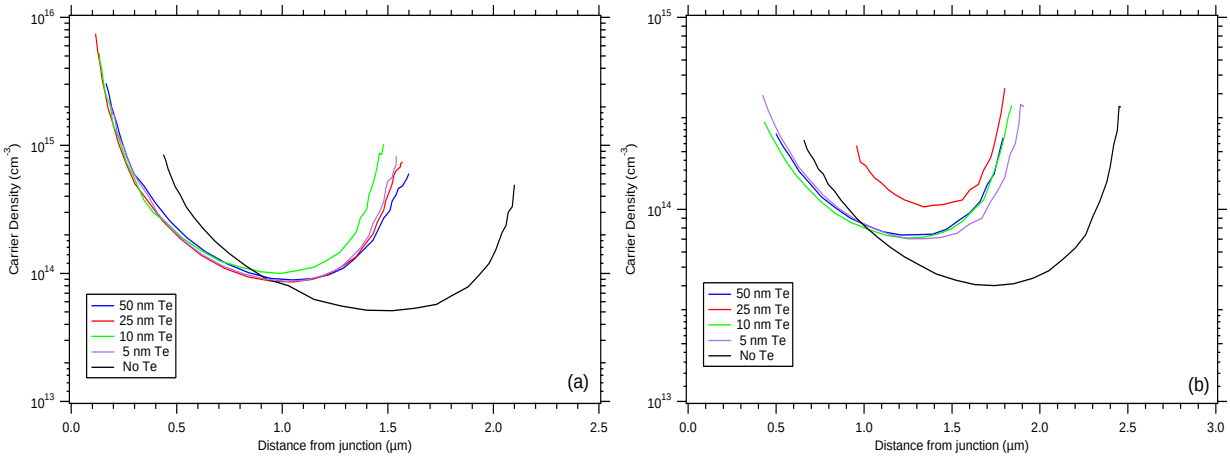

Figure 25: C-V curves of devices (a) with intentional Cu doping and (b) without intentional Cu doping

Despite tellurium having a much smaller back barrier than carbon, the depletion width in devices with Te, show a significantly decreased depletion width. Depletion width in the No Te device is significantly larger than those with the buffer layer. The belly also sits lower, with the carrier concentration decreased.

The devices deposited with Te all exhibit very similar depletion widths and carrier concentrations, with only small, negligible differences. Even with a very thin layer of Te, a dramatic decrease in the depletion width is noticeable. This is ideal, as it creates a smaller barrier for the carriers to cross.

In the device with no intentional Cu doping, the spread of the depletion width between the Te devices is less negligible than in the Cu doped devices. A significant difference in carrier concentration of no Te device and Te deposited devices.

When directly comparing the No Cu and Cu doped devices, an increase in depletion width is seen for the devices non-intentionally doped with Cu. As mentioned previously, Cu increases hole concentration in CdTe, while also reducing the back contact barrier. This is evident in Figure 20a and b, for the devices without Te, a kink is clearly visible in the device without Cu doping, while the Cu doped device has no

apparent kink. In Figure 26, the belly of the Cu/No Te curve sits higher than that of the No Cu/No Te curve, indicating a higher hole concentration.

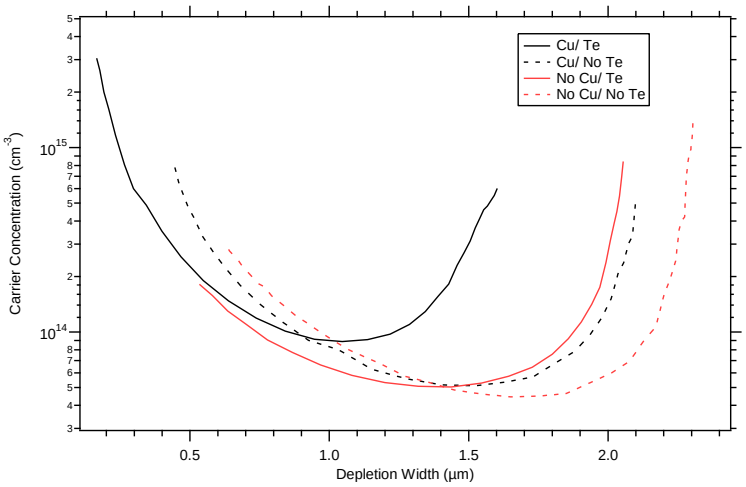

Figure 26: C-V Comparison of devices w/ and w/o intentional Cu doping and w/ and w/o Te back contact (50 nm).

For Te contact devices, a very similar result is apparent. There is a significant decrease in the depletion width of devices contacted with Te. The belly of the curve in these devices also sits higher, once again indicating a higher carrier concentration. This suggests that the Te back contact layer is raising the valence band of the CdTe at the back contact interface.

In the Mott Schottky plot of devices with and without Cu doping, the onset of the constant region in the plot occurs earlier in devices with intentional Cu doping versus the device without Cu doping [32]. The following is a possible explanation for this device behavior. In CdTe devices, two diodes exist within the device, the main p-n diode, MZO/CdTe, and back Schottky diode, CdTe/metal. The depletion region of the main diode and the back diode are separated by a region of high hole concentration associated with the CdTe. The depletion region of the p-n diode can only increase until it reaches this region. The introduction of dopants at the back of the CdTe, will increase the region of high hole concentration in the direction of both the main and back diode, therefore, decreasing the depletion region of both diodes. The main diode depletion width is limited by the back diode and therefore can show full depletion in reverse bias before reaching the absorber thickness.

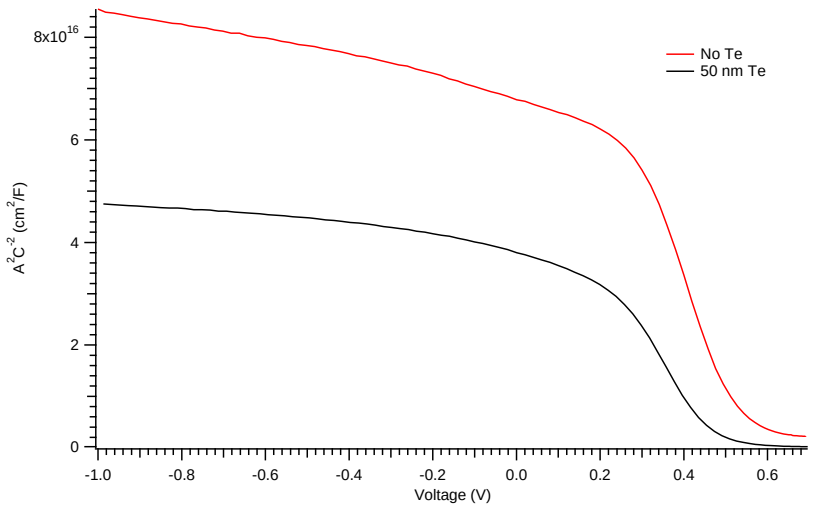

Figure 27: Mott Schottky plot of devices with intentional Cu doping w/ and w/o Te

Adding the Te back contact layer, shows an even earlier onset of the linear region (Figure 27) in the Mott-Schottky plot. This means CdTe depletion region is reaching full depletion at a much smaller voltage bias. This indicates that Te raises the CdTe valence band at the back junction and overall decrease the depletion width.

3.2 CdTe/Te Interface Properties with Variations in Te Thickness

The band offsets at the CdTe/Te interface were approximated by measuring the binding energy of the core levels (CL) of Te and Cd and valence band maxima (VBM) of Te and CdTe separately. Figure 28 shows three separate film stacks used for characterizing the Te and CdTe films. The CdTe film stacks were not passivated with $CdCl_2$ and did not receive any intentional copper doping. The structure shown in Figure 28a was used to approximate the CL binding energy and the VBM of Te; Figure 28b to measure the CL binding energy of Cd and the VBM of CdTe; and Figure 28c to measure the CL binding energies of Cd and Te at the interface. Several Te thicknesses were investigated to determine the properties of the CdTe/Te interface samples and to discern if bulk properties were affected by Te thickness. The Te layer was kept thin enough to measure the Cd CL emission. Using software packages Fityk and Multipak, the XPS data were analyzed to fit CL peaks and extrapolate the valence band edge.

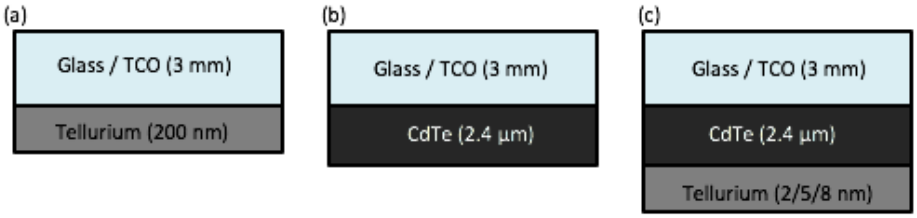

Figure 28: Schematics of sample structures utilized for XPS/UPS measurement. (a) bulk Te, (b) bulk CdTe and (c) CdTe/Te interface sample with varying Te thickness

3.2.1 Examination of Core Levels

Core level peaks were fit with Voigt functions, which are commonly used for peak fit in XPS[]. The XPS measured $Te3d_{5/2}$ and $Cd3d_{5/2}$ CL peaks exhibited well-defined behavior and were used for

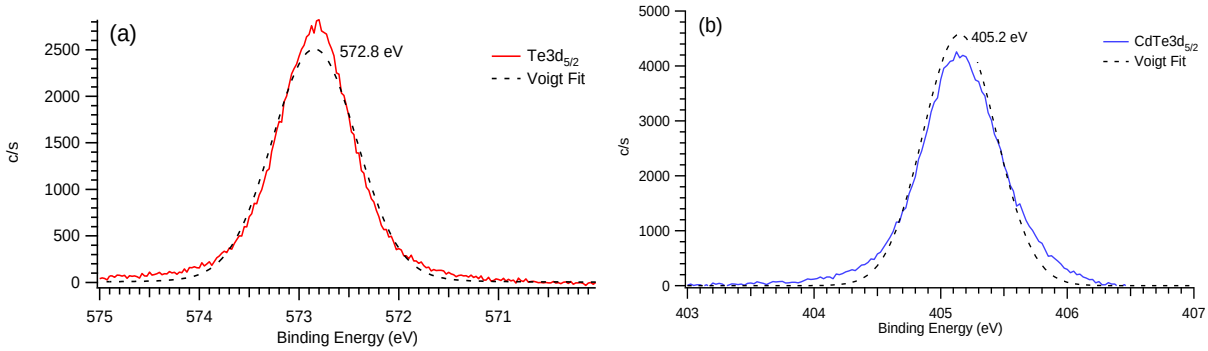

Figure 29: (a) XPS HRES scan of Te3d5/2 core level peak and (b) XPS HRES scan of CdTe3d5/2 core level peak with the data fits shown in the dotted lines

measurement of E_{CL}^{Te} and E_{CL}^{Cd} values, respectively. Figure 29a displays the $Te3d_{5/2}$ peak analyzed from the 200 nm bulk Te sample (Figure 28). Figure 29b displays the $CdTe3d_{5/2}$ peak analyzed from the 2.5 µm bulk CdTe sample shown in Figure 28. The average of several measured CL binding energy values with associated tool error are summarized in Table 3.

Table 3: Core levels from structures shown in Figure 28

Energy Levels	Binding Energy (eV)
E_{CL}^{Te}	572.8 ± 0.1
E_{CL}^{Cd}	405.2 ± 0.1

The XPS measured $Te3d_{5/2}$ and $Cd3d_{5/2}$ CL peaks determined from the structures shown in Figure 28c (2.4 µm CdTe/ 2-8 nm Te) are shown in Figure 30. A decreasing intensity of the $Te3d_{5/2}$ emission with

decreasing Te thickness is observed in Figure 30a. A similar effect was observed with the $Cd3d_{5/2}$ emission peak as Te thickness increased (Figure 30b). The CL values were determined and the averages of several peaks are summarized in Table 4. A slight shift among the binding energies with the varying thicknesses is apparent. ΔE_{CL} was calculated using Eqn # and used for calculation of VBO values for the varying CdTe/Te interface samples.

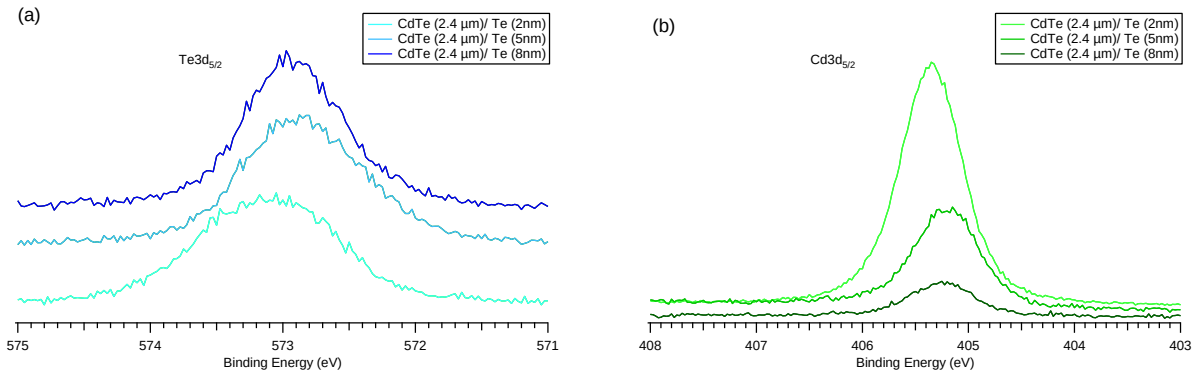

Figure 30: HRES scans of (a) $Te3d_{5/2}$ (b) $CdTe3d_{5/2}$, with 2, 5, 8 nm of Te at the back

Table 4: Core Levels of $Cd3d_{3/2}$ and $Te3d_{5/2}$ of the structures shown in Figure 28c

Cell Structure	E_{CL}^{Te} (eV)	E_{CL}^{Cd} (eV)
2.4 µm CdTe/ 2 nm Te	573.1±0.1	405.4±0.1
2.4 µm CdTe/ 5 nm Te	572.8±0.1	405.1± 0.1
2.4 µm CdTe/ 8 nm Te	573.0±0.1	405.1±0.1

3.2.2 Ultra-violet Photoelectron Spectroscopy Hardware

The purpose of setting up the ultra-violet photoelectron spectroscopy tool was for studying the valence band edge of the CdTe absorber layer and the tellrium buffer layer. X-ray photoelectron spectroscopy can be utilized for analyzing the valence band, however, the precision of such measurements is questionable. XPS utilizes an x-ray source with an energy of 1486.6 eV (Al Kα) and has an error of around ±0.5 eV. When reporting core level binding energies, this error is often negligible,

however for the valence band edge this error can be significant. Ultra-violet photoelectron spectroscopy uses a UV source with an energy of 21.1 eV (He I) and an error of only around ±0.05 eV and is better suited for such analyses.

The ultra-violet photoelectron spectroscopy tool was set-up in the same ultrahigh vacuum chamber as the current XPS system (Figure 31). For XPS operation an ion pump is utilized for maintaining base pressure in the chamber, however pumping He limits the speed and stability of the ion pump. A turbomolecular pump was installed for UPS operation and can maintain pressure at ~10^{-8} Torr, which is in the acceptable range for operation.

The UPS system utilizes a gas discharge lamp with an adjustable He I (21.2 eV)/ He II (40.8 eV) radiation ratio. The UV source is connected directly to the ultrahigh vacuum chamber and pumped down through two differential pumping stages. A molecular sieve trap and safety trap are attached to the two-stage rotary vane pump to avoid oil back streaming to the secondary turbomolecular pump. The UV source maintains pressures ~10^{-3} Torr, which is the acceptable range required for the UV source. The UV source is cooled by a thermoelectric chiller, which provides a constant temperature (15°C) coolant to the source.

A He tank is connected to the UV source and the flow of He is carefully controlled, allowing pressure to increase in the UV source for ignition of the lamp. The required pressure for the UV source to ignite is ~$1.3*10^{-2}$ Torr. Larger pressures can be used; however this will result in an overall increase in the chamber pressure. For ideal operation, the ultrahigh vacuum chamber must be maintained at pressures >10^{-6}.

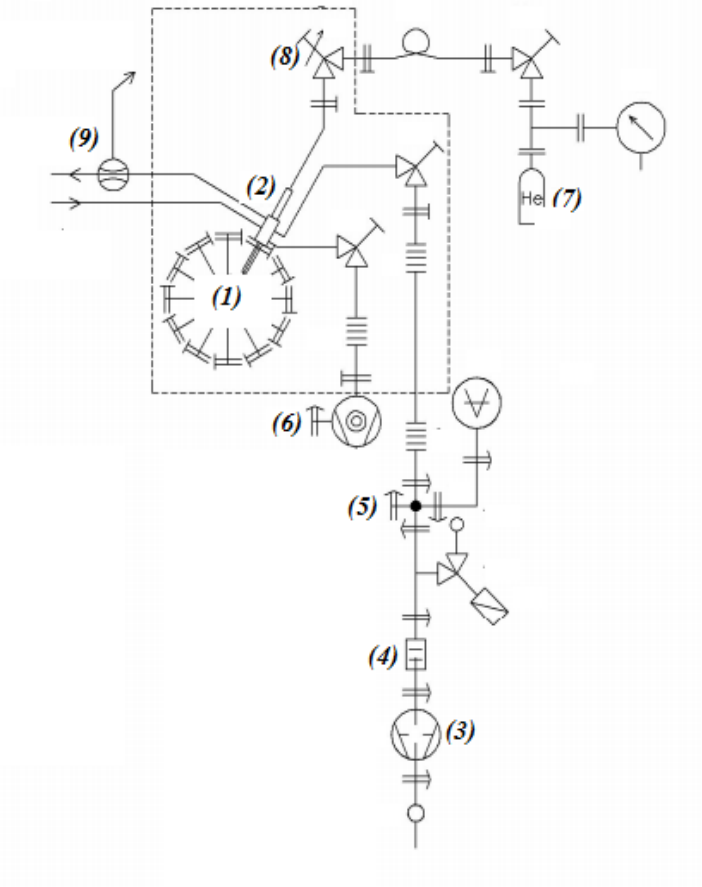

Figure 31: Schematic of ultra-violet photoelectron spectroscopy tool [33]. *(1) UHV, (2) UVS 40A2 Source, (3) 2-Stage Rotary Vane Pump, (4) Molecular Sieve Trap, (5) Safety Valve, (6) Turbomolecular Pump, (7) He Gas Tank, (8) Leak Valve, (9) Thermoelectric Chiller*

The intensity and nature of the discharge are dependent upon the gas pressure inside the source and discharge current. The ignition potential of the lamp is a magnitude higher than the operation potential necessary for continuous discharge. For ignition, the voltage is set to 0.7 kV and the current limited to 80 mA. The voltage is then brought down accordingly to maintain continuous discharge. A peach-colored plasma is visible with source ignited.

The beam size of the UPS source is 2 mm, much larger than the XPS source. The sample must be sized accordingly for accurate results. The sample is oriented at 90° for maximum irradiation. A pass energy of 2.95 eV at 0.025 eV per step obtains accurate results with good resolution.

3.2.3 Examination of Valence Band

E_{VBM}^{Te} and E_{VBM}^{CdTe} were determined from UPS analysis of the valence band edge. UPS data was used for analysis of the valence band edge due to a much smaller energy range, allowing for a higher resolution. An Au sample was measured and the Fermi level determined and used as a reference. The VBM of structures shown in Figure 28a and b were determined by linearly extrapolating the leading edge of the valence band [30]. The valence band offset can be determined using Equation 6 in Sect. 2.2.6. The average of several measured VBM binding energy values with associated tool error are summarized in

Table 5.

Table 5: Valence band maxima from structures shown in Figure 28

Energy Levels	Binding Energy (eV)
E_{VBM}^{Te}	0.25 ± 0.05
E_{VBM}^{CdTe}	0.81 ± 0.05

Niles *et al.* [31], who performed similar experiments studying the CdTe/Te interface and reported a valence band maximum value of 0.03 eV for Te. This is significantly less than the value listed in Table 5. Niles fabricated devices in-situ, which means the devices were not exposed to contamination and oxidation, which can largely effect the valence band edge position.

The 0.81 eV calculated VBM of CdTe suggests that CdTe exhibits slightly n-type behavior as this would put the approximate Fermi level slightly above the middle of the gap. This is inconsistent with hot probe tests, which probe bulk properties and indicate a slightly p-type doping under typical CSS CdTe deposition conditions. It has been suggested that the surface material characteristics of CdTe vary from those found in bulk CdTe [34]. Passivation and doping used in finished devices appear to have significant effects on the VBO.

3.2.4 Valence Band Offset Calculations

XPS and UPS analysis was performed to investigate the barrier at the CdTe/ Te interface and determine the VBO. The VBO values at the interface were calculated and listed in Table 6. Below a certain thickness it has been shown the bulk Te properties are not fully developed [34]. The VBO value decreases as the Te thickness increases from 2 to 8 nm. When compared to the previous J-V-T analysis, the VBO value further decreases as the CdTe device is $CdCl_2$ passivated, copper doped, and 50 nm Te is used.

Table 6: Calculated valence band offset of CdTe/Te interface for 2nm, 5nm and 8nm Te samples

Cell Structure	E_{VBO} (eV)
2.4 µm CdTe/ 2 nm Te	0.46 ± 0.2
2.4 µm CdTe/ 8 nm Te	0.26 ± 0.2

4 CONCLUSIONS AND FUTURE WORK

The use of a Tellurium back contact has led to increased device performance and uniformity, even without the use of intentional Cu doping at the back of CdTe. In J-V-T analysis, rollover is significantly reduced with the use of Te, suggesting low barrier formation at the back contact interface.

To study the back contact barrier at the CdTe/Te interface with precision, it was necessary to use ultra-violet photoelectron spectroscopy. For this study, an existing UPS system with an adjustable He I (21.1 eV) and He II (40.8 eV) UV source was rebuilt and incorporated into the ultrahigh vacuum system utilized for x-ray photoelectron spectroscopy. The system was then used to for probing the valence band edge of bulk CdTe and Te.

From XPS and UPS analysis, the valence band offset at the CdTe/Te interface was 0.26 ± 0.05 eV. The valence band position of the Te was found to be highly dependent on the state of the surface and therefore samples fabricated ex-situ had valence band edges far from what would be expected. The thickness of the Te layer affected the overall valence band offset, with a threshold of ~5nm before variation was negligible. CdTe was not treated with $CdCl_2$ or doped with Cu for this study.

Capacitance measurements of devices treated with and without Cu, show significant improvement in the carrier concentration when a thicker Te layer is deposited at the back. Devices without a Te back contact show poor carrier concentration and larger depletion widths, which approach the thickness of the absorber layer. Decreased depletion widths with application of Te at the back, suggest that Te raises the valence band of CdTe at the back contact interface. This would ease carrier flow at the back and lead to improved device performance, which is supported by the J-V and J-V-T carried out in this research.

Future Work

Future work should include studying the valence band edge of CdTe devices with $CdCl_2$ treatment and Cu doping and with and without Te. In photovoltaic application, CdTe is typically p-type doped before applying a back contact. Studying p-type doped CdTe should give insight into the CdTe/Te interface of fabricated and measured thin film CdTe devices at CSU.

The use of alternative back electrode materials to Carbon and Nickel paint should be explored for further improvement in device performance. Carbon and Nickel paint are deposited in a fairly non uniform spray application and therefore thickness cannot be controlled easily. Photovoltaic measurement techniques described in Sect. 2.2 would be useful for characterization of these back electrodes.

Research aimed towards developing devices with p-type dopants other than Cu is a major focus in CdTe technology. Cu leads to low lifetime and stability issues in CdTe devices and overall does not significantly increase carrier concentration in these devices. Increasing the carrier concertation of CdTe would lead to further reductions in the valence band offset and decreases in the depletion width, which would ultimately lead to a higher performing device.

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