DISSERTATION

HIGH-SPEED VERTICAL-CAVITY SURFACE-EMITTING LASERS WITH REDUCED ELECTRICAL AND THERMAL CONSTRAINTS ON MODULATION BANDWIDTH

Submitted by

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WE HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER OUR SUPERVISION BY AHMAD NASSER AL-OMARI ENTITLED HIGH-SPEED VERTICAL-CAVITY SURFACE-EMITTING LASERS WITH REDUCED ELECTRICAL AND THERMAL CONSTRAINTS ON MODULATION BANDWIDTH BE ACCEPTED AS FULFILLING IN PART REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY.

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ABSTRACT OF DISSERTATION

HIGH-SPEED VERTICAL-CAVITY SURFACE-EMITTING LASERS WITH REDUCED ELECTRICAL AND THERMAL CONSTRAINTS ON MODULATION BANDWIDTH

The need for communication network services has increased the need for high-speed communication systems with greater bandwidth. One of the approaches to greater local area network (LAN) link bandwidth is faster single-channel modulation rates. Because vertical-cavity surface-emitting lasers (VCSELs) are widely used in short wave length LAN transmitters, it is important to reduce the electrical and thermal constraints on their modulation bandwidth.

In this study high-speed oxide-confined VCSELs were fabricated and characterized. Complete fabrication processes for top-emitting self-aligned and non-self-aligned 850nm and 980nm high-speed VCSELs were developed. A complete fabrication process for bottom-emitting, non-self-aligned, flip-chip bonded 980nm high-speed VCSELs was developed. Some of the critical fabrication steps that affect the VCSEL's speed were examined. The effect of a heat-sinking layer on the performance of high-speed VCSELs was demonstrated for 850nm and 980nm devices.

Two generations of 850 and 980nm devices were designed, fabricated and characterized in this research; the second generation incorporated modifications based on the first generation fabrication and characterization results. In the first generation, self-aligned top-emitting 850nm high-speed VCSELs were fabricated and characterized. The self-aligned process allowed smaller mesa diameters for a given aperture size, thus

decreasing the distance for heat flow to the sidewall as well as mesa capacitance. VCSEL mesa capacitance was reduced by 49% compared to values reported before. The effect of a heat-sinking layer on the 850nm VCSELs' performance was demonstrated. Au-wrapped and Cu-plated heat- spreading layers reduced the thermal resistance by 25% and 44%, respectively, and the output power was increased by 17% and 38%, respectively, compared to similar VCSELs without the Cu-plated heatsink. The fabricated devices exhibited a 3dB modulation frequency bandwidth up to 16.3 GHz at 8.9kA/cm^2. Using the second generation design and fabrication process, an improved heat-sinking effect on the performance of high-speed non-self-aligned 850nm VCSELs was demonstrated. A 10μm active diameter Cu-plated device exhibited a reduced thermal resistance of 57%, 52%, and 45% compared to polyimide wrapped, Au-wrapped, and Cu-plated first generation devices, respectively. The lasers exhibited modulation bandwidths up to approximately 18 GHz at only 8kA/cm^2 and a modulation current efficiency factor (MCEF) as high as 15GHz/mA$^{1/2}$.

The effect of a heat-sinking layer on the performance of high-speed, non-self-aligned top-emitting 980 nm VCSELs was also demonstrated. Increasing Cu-plated heatsink radii from 0μm to 4μm greater than the mesa in 980nm VCSELs reduced the measured thermal resistance for a range of device sizes to values 50% lower than previously reported for top-emitting VCSELs over a range of device sizes. For a 9μm diameter oxide aperture, the 4μm heatsink increased output power and modulation bandwidth by 131% and 40%, respectively. The functional dependence of thermal resistance on oxide aperture diameter indicates the importance of lateral heat flow to

mesa sidewalls. The measured 3-dB modulation frequency bandwidth was 9.8 GHz at 10.5 kA/cm^2.

Bottom-emitting non-self-aligned flip-chip bonded 980nm devices were also fabricated and characterized. VCSELs with 10μm active area have a threshold current and a slope efficiency of 0.6mA and 80%, respectively. The flip-chip bonding increased the maximum output power for VCSELs by up to 25%. Based on the relative power increase for different device sizes, as the devices active diameter gets smaller the vertical heat sinking provided by the flip-chip bonding is less efficient and a lateral heat sinking mechanism needs to be introduced.

To further improve the understanding of current high-speed VCSEL performance restrictions, the effect of external heating on the VCSEL's resonance frequency and damping factor was examined for top-emitting, self-aligned 980nm VCSELs. Increasing the stage temperature reduced both the resonance frequency and the damping factor, hence limiting the modulation bandwidth of VCSELs. The relationship between the damping and the resonance frequency squared revealed a maximum intrinsic 3dB bandwidth of 24.7GHz. Furthermore, as the contacts of the self-aligned VCSELs go through annealing, etching, and oxidation, experiments using Ti-Pd-Ti-Au-Ti-Pd and Ti-Ni-Ti-Ni metal systems were performed on samples with different treatments to investigate the effect of these processes on the specific contact resistance. The later metal system exhibited a lower specific contact resistance compared to the former one.

To better model the high-speed devices and learn how to lower the parasitic capacitance associated with the high-speed VCSEL metal pads, the dielectric properties of four different spin-on dielectrics were investigated. Thicker dielectrics result in lower

parasitic pad capacitance but also higher losses. A circuit model for the pad capacitance is obtained based on geometrical and physical considerations. It is concluded that the remaining un-etched mirror stack under the VCSEL pad has no significant contribution to the loss and that the physical origin of most of this equivalent resistance is in fact dielectric loss in the pad capacitor.

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Chapter 1

INTRODUCTION AND MOTIVATION

1.1 Introduction

Over the last two decades, the semiconductor laser diode has emerged as a device that complements transistor technology to form the twin columns of modern information technology. Similar to the transistor's role in integrated circuits that process information, the laser is at the heart of fiber-optic networks that form the basis of the modern Internet. There are predominantly two forms of semiconductor lasers, the edge emitting laser (EEL) and the vertical-cavity surface-emitting laser (VCSEL). A vertical-cavity surface-emitting laser is a semiconductor laser diode in which the two mirrors as well as the intervening gain region are grown epitaxially on a semiconductor substrate. Light generated at the gain region bounces back and forth vertically between the mirrors, and some leaks through the top surface mirror to form the emitted beam [1].

Before discussing the difference between the VCSEL and EEL, I want to summarize some work that had an important impact on the development of the VCSEL. Beginning in the early 1980s, several researchers, mainly at Bell Laboratories and The Optical Sciences Center of the University of Arizona, began looking into the use of lasers as a nonlinear optical phenomenon in micro cavities for potential applications in optical switching, signal processing and optical computing [2].

Two-dimensional (2-D) arrays of light modulators were used in some of the system architectures that have been inspected for optical computing. These architectures are known to allow the performance of specific mathematical operations such as the

inversion of matrices in a simple and efficient approach [2]. While researchers were searching for technologies that could be used in these applications, they began investigating simple Fabry–Perot resonators that include nonlinear optical media. David Miller and his group at Bell Laboratories studied resonators with GaAs–AlGaAs multiple quantum wells as the nonlinear absorber [2]. The structures they investigated had a low threshold; because of this, they subsequently became the basis of the quantum-confined Stark-effect optical modulator. Dr. D. J. Goodwill and his group were able to fabricate modulators into large-size arrays and use them in switching applications [3]. These researchers implemented an optical hyper plane-based ATM switching fabric. They also designed the electronic interface and optical interconnects that are currently being fabricated using today's technology.

The performance of these devices as optical switches was improved by increasing the quality factor of the composite resonator structures by reducing the residual cavity losses and by increasing the reflectivity of the mirrors. Independent of any attempt to develop a laser, these improvements were essential for some of the main features of the practical VCSEL.

1.2 Vertical-cavity surface-emitting laser (VCSEL) vs. edge-emitting laser (EEL)

A VCSEL, or vertical-cavity surface-emitting laser, is a semiconductor micro laser diode that emits a cylindrical beam of light vertically from the surface of a fabricated wafer. It consists of a gain region placed between two distributed Bragg reflectors (DBRs), all parallel to the wafer plane. The feedback in edge-emitting lasers (EELs) is achieved by cleaving the devices and thus creating optical mirrors due to the difference in

refractive indices between the EEL's material and its surroundings (typically air). As a result, the EEL's emitted beams are parallel to the wafer plane. The VCSEL's special characteristic of emitting a light beam vertically from the surface of a fabricated wafer enables it to offer significant advantages over the EEL. Figure 1.1 below illustrates some of the advantages of VCSELs over EELs. In the EEL, the beam comes out of the edge while in the VCSEL the beam comes out of the wafer surface, which makes it possible to carry out on-wafer testing before the wafer is cut into individual laser dies that are then packaged. Further, the EEL produces an astigmatic diverging beam of an elliptical cross-section, whereas the beam of the VCSEL has a much smaller divergence angle and circular beam cross-section, which results in simpler optics and better performance [4].

In addition, VCSELs do not need corrective optics and over 50% of their light can be coupled into a fiber. VCSELs have lower current requirements than EELs, which makes them good for battery-driven applications and improves power budget efficiencies for low-power applications. For high-power applications, EELs are more efficient. VCSELs also have higher data rates (>10.0 GHz) than the simplest type of EELs, known as Fabry-Perot laser diodes (~2.0GHz). Other EELs, specifically distributed feedback (DFB) lasers, can operate at speeds of 20 GHz or higher, but are much more expensive than VCSELs. The large bandwidth of VCSELs makes them attractive for low-cost, high-speed communications applications. Moreover, VCSELs can easily be fabricated into high-density 2-D arrays [4], while this is much more complicated using EELs. Easier fiber alignment and reduced packaging costs are additional advantages of the VCSEL [5].

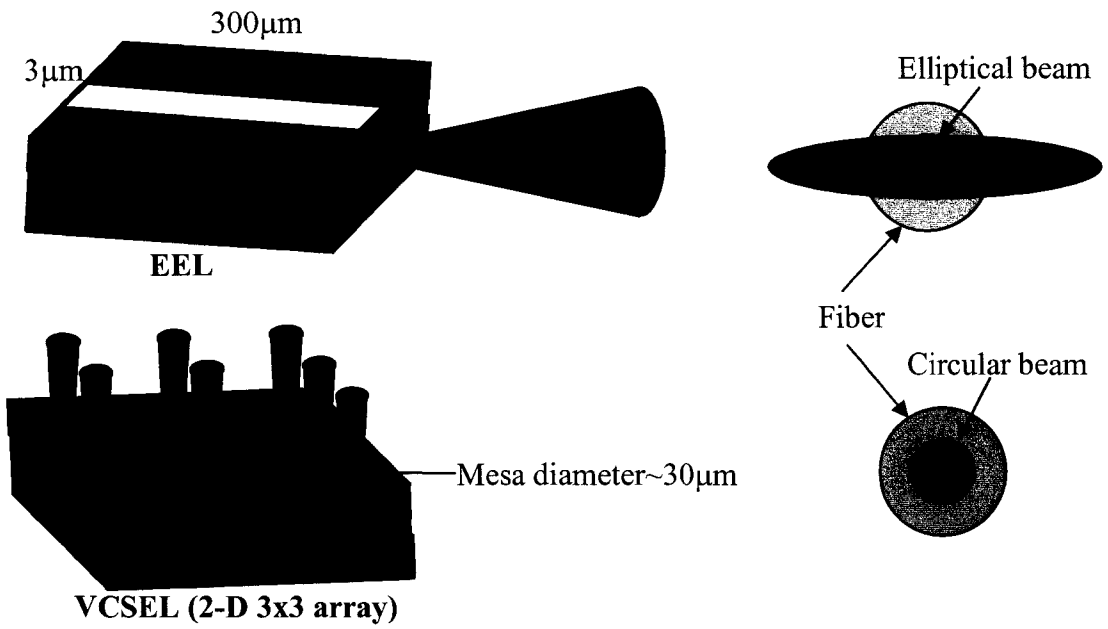

Figure 1.1 Vertical-cavity surface-emitting laser vs. edge-emitting laser.

1.3 Motivation

Telecommunication networks based on optical fiber communication have become major information transmission systems around the world. Local Area Networks (LAN) as a part of the telecommunication networks have become the norm for many workplaces and educational settings, as users move from an isolated desktop computing model to a more distributed computing model in which they gain access to shared and unlimited sources of information. As the demand for communication-network services such as database queries, remote education, telemedicine and videoconferencing increases, the need for high-speed communication systems with greater bandwidth also grows.

There are three approaches to greater link bandwidth: parallel fiber ribbons, wave division multiplexing, and faster single-channel systems. Because the optical beam is

emitted perpendicular to the wafer surface, VCSEL arrays can be fabricated with photolithographic tolerances, making them ideal sources to mate with ribbon fiber interconnects. To date, most of the market has centered on either four elements operating up to 3.125GBd per channel or 12 elements operating up to 1.25GBd per channel. The operating reach of a parallel interconnect is more than 100 meters, and is limited by the skew in the optical fiber. In other systems, serial data communication is more advantageous, and VCSELs have been operated at speeds in excess of 10GBd by direct modulation. Achievable link lengths are on the order of 75 meters over installed multimode optical fiber, with distances of 500 meters on 850nm optimized fiber such as Lucent's Lazer Speed ™ [6]. Faster single-channel systems require faster VCSELs, and thus it is important to develop high-speed VCSELs. VCSELs are suited for LAN applications in a number of ways [7,8].

Vertical-cavity surface-emitting lasers (VCSELs) are already the optical transmitter component of choice for single- and parallel-fiber links for LANs (~100 m) and rack-to-rack connections (~10 m). VCSEL based, parallel fiber transceivers will soon be used in commercially produced optical "backplanes" for board-to-board connections (~1 m). It is clear that the inherent advantages of VCSEL technology, including economical manufacturing, adequate direct modulation bandwidth, and scalable 1-D and 2-D array sizes will insure that they play a leading role in high data rate chip-to-chip optical interconnects (~0.1 m).

As discussed in [9], While optical interconnects offer a number of well known benefits in comparison to electrical connections at each length scale, history has indicated complex optics will only replace copper when optics has an overwhelming data rate

benefit at that length scale. Currently, PCB technology offers up to approximately 2-3 Gb/s electrical connections with 5 Gb/s in the near future. One high performance PCB manufacturer, Sanmina-SCI, believes that the incumbent technology, copper, will be pushed to 10 Gb/s, and that its superior bit error rates and reduced design time will yield to optical interconnects only at 20 to 40 Gb/s and beyond as illustrated in Figure 1.2. Thus technology demonstrations of chip-to-chip optical interconnects in the 20 to 40 Gb/s range are central to advancing the adoption of optical technology at the PCB level.

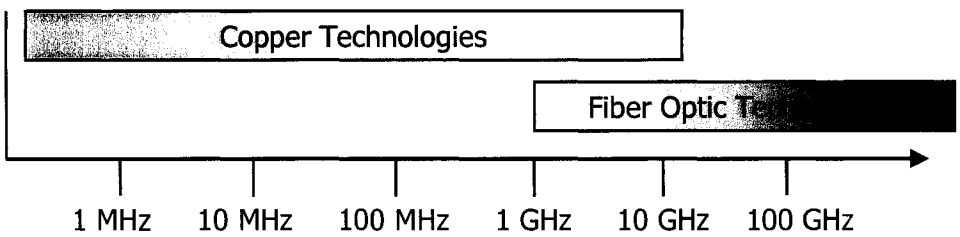

Figure 1.2 Applicable frequency ranges of copper and optical technology for boards according to technology assessment slides by Bob Whitehouse of Sanmina-SCI.

In contemplating economically viable 40 Gb/s chip-to-chip optical interconnects, the modulated source technology appears to be a key weak link. The short distances minimize the modal dispersion of multi-mode fiber or single-mode polymer waveguides so that 100 cm long channels should have sufficient bandwidth for 40 Gb/s data transmission. Detector technology with 40 GHz or higher bandwidths has been commercially available for a decade and research has demonstrated p-i-n detectors in excess of 100 GHz [10]. Externally modulated sources can operate at 40 Gb/s, but they are not compatible with the power, array form factor, or cost requirements of optical interconnects. Directly modulated edge-emitting laser diodes have been demonstrated

with bandwidths up to 40 GHz [11], but require large drive currents on the order of 100 mA. As already mentioned, VCSELs are extremely well suited for parallel optical interconnects, but the maximum demonstrated data rate for VCSELs is 12 Gb/s[12,13]. A 15.6Gb/s data transmission rate has been previously reported [14] using conventional VCSELs. This data rate was achieved by fabricating a high-speed VCSEL SiGe driver and the use of an experimental fiber whose properties were almost ideal at 850nm, but there was no attempt in [14] to investigate the limitations of the VCSELs bandwidth. Recently, a 20Gb/s data rate at 980nm was demonstrated [15] using sub-monolayer quantum dots based VCSELs at a current density of 969.7 kA/cm^2 which is almost a 100 times higher than the industrial benchmark for reliability that is 10 kA/cm^2. It is the primary aim of the proposed research to explore the limitations and approaches to further extending the direct modulation bandwidth of VCSELs.

There are a number of factors limiting the modulation bandwidth of current VCSEL technology, including:

- High junction temperatures that decrease gain at large current drives necessary for high speed operation
- Restricted single-mode operation range that determines the maximum photon density per mode
- Parasitic circuit effects, including contact and pad capacitances and peripheral charge storage
- Epitaxial structures that are not optimized for high differential gain

It is important to note that, while the intrinsic dynamics of the laser can be improved, prior studies have shown that VCSELs have the intrinsic capability to reach

modulation bandwidths greater than 50 GHz as will be discussed in more detail in Chapter 2.

In order to address the limitations just listed, a new VCSEL structure specifically designed for high-speed operation was fabricated that simultaneously diminished the source of each limitation. With its special structural considerations, the new VCSEL structure improved heat-sinking, moderated current density non-uniformity and reduced unnecessary device areas. These improvements benefited junction temperature and parasitic circuit element issues. Additionally, the effects of external heating on the VCSELs resonance frequency and damping factor were explored.

1.4 Research objective and outline

The overall objective of this research is to fabricate high-speed oxide-confined vertical-cavity surface-emitting laser based on new VCSEL structures specifically designed for high-speed operation. The structures to be developed are top-emitting and bottom-emitting flip-chipped VCSEL with special structural considerations designed to improve heat-sinking, moderate current density non-uniformity, and reduce unnecessary device areas. To achieve this objective, the parameters that affect VCSEL speed as well as the fabrication steps required to fabricate high-speed VCSELs were investigated.

Chapter 2 details the background information about the physics and fabrication of VCSELs. It includes the present technical status of high-speed VCSELs by highlighting the intrinsic and extrinsic parameters that affect VCSEL switching speed. Chapter 2 also reviews the previously published work in fabrication and characterization of high-speed

VCSELs. And finally, it will conclude with a summary of the new design, concept, and technical approach of the present work.

Chapter 3 discusses the detailed fabrication steps of high-speed top-emitting and bottom-emitting flip-chip bonded VCSELs. It incorporates an overview of VCSEL fabrication steps for both top- and bottom-emitting devices as well as detailed description of the actual fabrication steps and their setups, illustrated by SEM images and schematic drawings.

Chapter 4 presents the testing and characterization results of the fabricated high-speed VCSELs. It describes the measurements of electrical and optical characteristics of these VCSELs. The DC, AC, and RIN characterization setups are described and presented as schematic diagrams. Various measured parameters for different devices are presented, compared where applicable, and discussed.

In Chapter 5, dielectric properties of four different spin-on dielectrics that are typical options for planarization are investigated using the parasitic capacitance of high-speed VCSEL metal pads as test geometry for the samples. Achievements, conclusions, and suggestions for future work are given in Chapter 6.

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Chapter 2

BACKGROUND, PRESENT TECHNICAL STATUS AND NEW DESIGN AND CONCEPT OF HIGH–SPEED VCSELS

2.1 Introduction

Modern high-speed, short wavelength communication systems use the Vertical Cavity Surface Emitting Laser as their light source. Great progress has been achieved in the development of VCSELs for high-speed optical interconnects in high bit-rate data transmission systems [1]–[11].

To develop more understanding of VCSEL's limitations, this chapter will present and discuss the four common means used to achieve optical and current confinement in VCSELs which are post etched, regrown, proton implanted, and oxidized VCSEL structures. The advantages and disadvantages of these structures will be discussed in Section 2.3.

In order to enhance the VCSELs' performance, the factors affecting VCSEL speed need to be explored. In Section 2.4 the intrinsic and extrinsic limitations, which include parasitic circuit effects, junction heating, and mode control, will be discussed. Following the discussion of the intrinsic bandwidth from experimental results in Section 2.4.1, this chapter will discuss in detail the parasitic circuit elements, including series resistance and shunt capacitances, significant heating at high current density, and the effect of the number of modes on the bandwidth of VCSELs in Section 2.4.2.

Section 2.5 will present the different ways many research groups have reported on fabricating high-speed VCSELs and reducing their modulation bandwidth-related parasitics. A summary of the new design and concept and technical approach of the present work will be presented in Sections 2.6 and 2.7, respectively.

2.2 VCSEL structure

In the 1970s, the Iga group at the Tokyo Institute of Technology, Tokyo, Japan, presented the first proposed concept of a vertical-cavity surface-emitting laser. They achieved pulsed operation and continuous wave (CW) operation in 1984 and 1988, respectively [12,13]. State-of-the-art fabrication developed through the years as more advances were achieved in the design and growth of mirrors in addition to the progress accomplished in fabrication techniques for electrical and optical confinement. Various companies are presently manufacturing VCSELs.

Numerous means are used to achieve optical and current confinement in VCSEL fabrication. The four common ones are: etching a post, regrowth, proton implantation, and oxidation. Figure 2.1 below illustrates cross-sections of these fabrication methods where most of the alterations focus on the method of defining the injected current path. All structures will be discussed in more detail in the next section.

2.3 Etched-post, regrown, proton implanted, and oxidized VCSEL structures

An air-post structure is a simple approach to defining the lateral extent of a VCSEL cavity. It is done by etching a pillar or post, as shown in Figure 2.1. The first

demonstration of a monolithic VCSEL was achieved with an etched air-post structure by the Jewell group at AT&T Bell Laboratories [14].

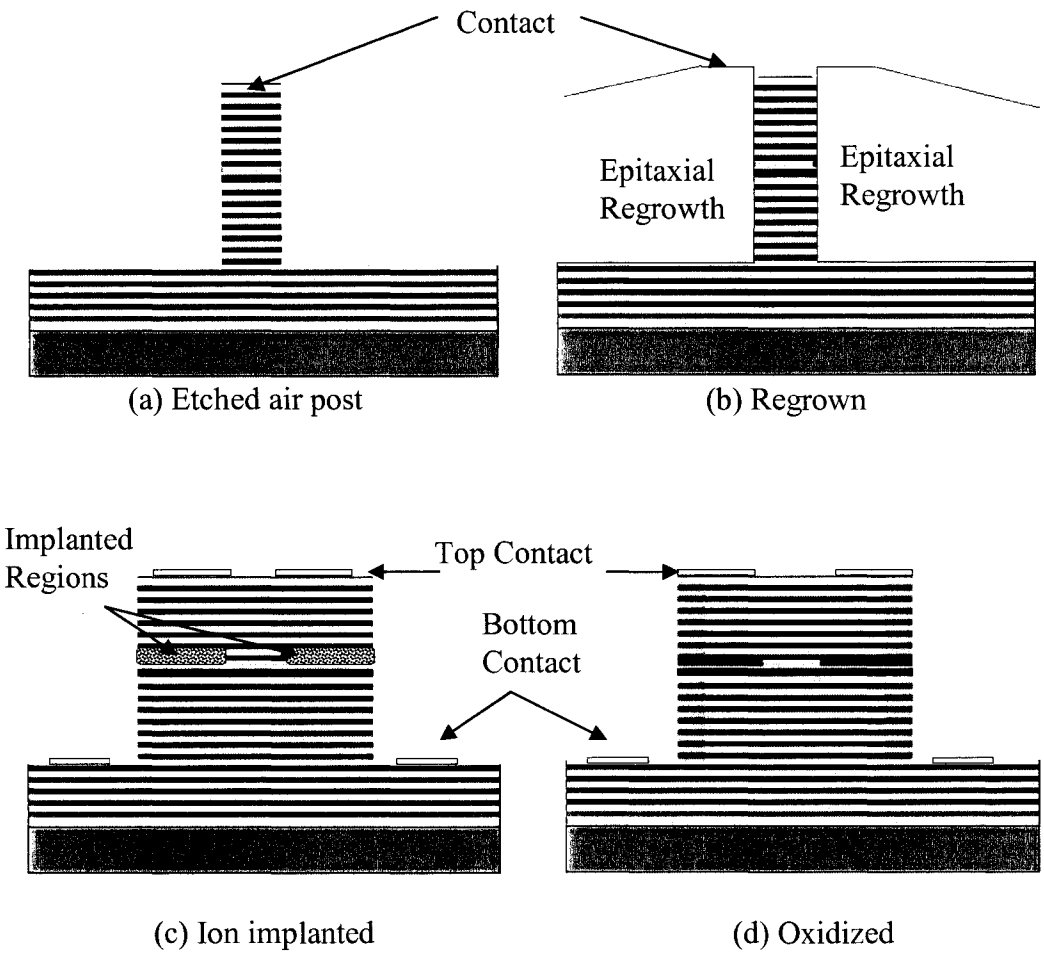

Figure 2.1 Various VCSEL structures (reproduced after [16]).

The disadvantage of the air-post VCSEL structure is carrier loss due to surface recombination at the sidewalls. Furthermore, there is a limit to how small the air-post diameter can be due to optical loss. Also, defects in the sidewalls will result in diffraction and scattering [15]. An additional concern is that these types of structures do not have an effective heat sink, which results in high thermal impedance. Moreover, in air-post VCSELs, the top contact overlaps at least part if not all of the active area, so the structure

is not well suited to short-wavelength VCSELs operating at wavelengths where the substrate is absorbing since top emission will be required.

The regrown structure is a method that gives index guiding in a planar geometry using a buried heterostructure, as shown in Figure 2.1. Etching the materials around the intended cavity isolates the active region. After that, the etched regions are filled with materials that have higher bandgap energies. Because of their wider bandgaps and lower refractive indices [17], the regrown regions are used to define the lateral margins of the active region and to play a part in electrical as well as optical confinement.

To date, three regrowth methods have been successfully demonstrated. These are: vacuum-integrated dry etching and molecular beam epitaxy (MBE) [18]; dry etching followed by chemical pretreatments before metalorganic vapor phase epitaxy (MOVPE) [19]; and etching followed by liquid phase epitaxy (LPE) utilizing melt-back cleaning [20].

To form implanted VCSELs, ion implantation is used to damage a certain part of the top mirror material and make it insulating, with the undamaged center acting as a conduit for the current. As a result, the current will flow from the top contact and channel through the undamaged region, which is the central region of the distributed Bragg reflector (DBR), and into the underlying active region [21]. Figure 2.2 represents a schematic cross-section of the ion implanted VCSEL.

Using a proton implantation structure has several disadvantages. It is possible that the active layer will be damaged by the implanted ions. Also, the lateral scattering of ion species (straggle) is indistinct, which limits the precision with which small apertures can be defined [17]. Another drawback of proton implantation is that it does not provide

inherent index-guiding. Moreover, the implanted geometry does not provide inherent polarization discrimination or control [22]. Furthermore, the presence of some residual surface damage from the implanted protons increases the contact resistance over the implanted material.

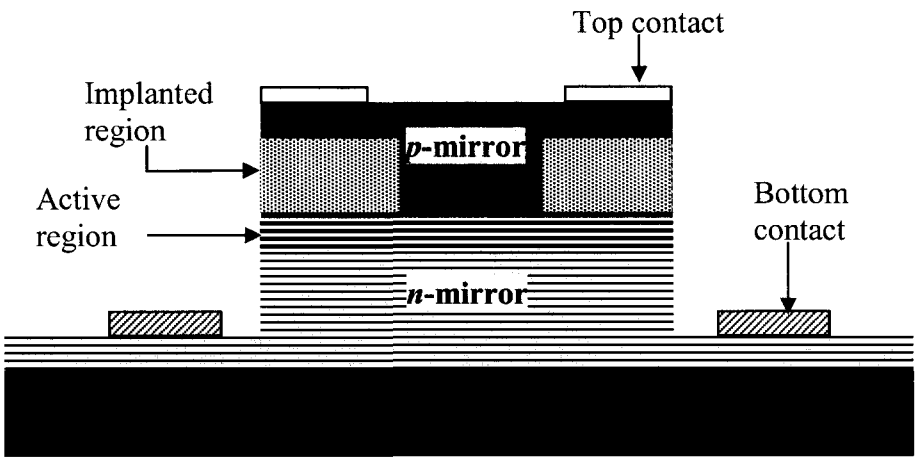

Figure 2.2 Schematic of an ion implanted VCSEL.

Oxide-confined VCSELs involve the introduction of an oxide aperture close to the active region. This is achieved by growing layers with the highest aluminum (Al) mole fraction adjacent to the active region. Etching the mesa will expose the edges of these layers, and then they will be oxidized at high temperatures in a water-steam environment using an oxidation furnace [23]. Details of the oxidation process will be discussed in Chapter 3. As a consequence, the layers with the highest Al mole fraction are converted from $Al_xGa_{1-x}As$ into Al-oxide, which is an insulator with a low refractive index (n~1.55) [21]. As illustrated in Figure 2.3 below, this insulating layer above the active region acts to confine the current to be injected into the preferred active area. Since this layer has a low refractive index, it also provides index-guiding.

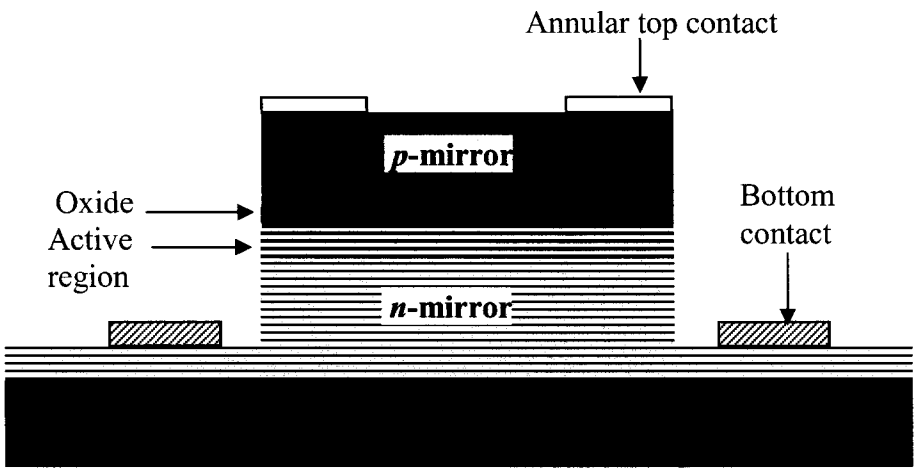

Figure 2.3 Schematic of an oxide-confined VCSEL.

A comparison between the proton-implanted and oxidized VCSEL structures (shown in Figures 2.2 and 2.3) indicates that the oxidized VCSEL provides excellent performance in terms of lower threshold current density and voltage [17]. Furthermore, while the best proton-implanted VCSELs provide about 20% power conversion efficiencies, oxidized VCSELs with efficiencies of 50% and 57% have been reported [24, 25].

Most of the recent reports on the progress of VCSEL device operation have mainly been for oxide-confined VCSEL designs, which provide low threshold current and high power efficiency as a result of their good optical beam and current confinement. In these various designs, the aperture has a different refractive index than the oxide isolation layer and thus acts as an index guide, as well as providing the current confinement for current injection into the active region.

2.4 Factors affecting VCSEL speed

As the bit rates of high-speed data transmission increase, the dynamic properties of the VCSELs are becoming more significant. Enhancing the VCSEL's speed to the 20 to 40 Gb/s range will extend its potential applications into future high-speed data transmission systems, parallel supercomputer interfaces, and multi-channel optical computing systems. For all these potential applications, it would be highly desirable to make high-speed VCSELs [26].

2.4.1 Intrinsic bandwidth of VCSELs

The maximum modulated VCSEL bandwidth of 21.5 GHz, obtained several years ago [27], is an indication of the potential of VCSELs, but is far from the ultimate limit of the devices. Two experiments have indicated intrinsic bandwidths of 58GHz and 71GHz [27,28]. By fitting the VCSEL modulation response with the traditional damped oscillator model the resonance frequency and equivalent damping frequency were obtained. Next, fitting the damping factor's parabolic dependence on the resonant frequency prior to saturation resulted in a factor of K=0.159 ns and zero current damping constant intercept of γ_o=18.8/ns leads to a calculation of the intrinsic 3dB bandwidth of 58 GHz [27]. In [28] a maximum resonance frequency of 71GHz was obtained by directly observing the intensity oscillations when the laser was pulsed (gain switched) at a I ~$60I_{th}$ using a ~20 ps electrical pulse. The high intrinsic resonance frequencies of VCSELs derive from their short cavity length and high transverse confinement factor, resulting in strong carrier-photon interactions. The ability to create large photon densities inside the high finesse cavity is also beneficial. These properties may lead to ultimate

modulation bandwidths for VCSELs that exceed the 40 GHz demonstrated for edge-emitting lasers [29].

2.4.2 Extrinsic limitations to intrinsic VCSEL bandwidth

The primary extrinsic factors that limit the VCSEL bandwidth are junction heating, multimode operation, and parasitic circuit effects. These topics are addressed in the following paragraphs.

2.4.2.1 Parasitic circuit effects

Regardless of the optical performance and resonance frequency that can be achieved, a physical device cannot be electrically driven with a signal frequency near the anticipated 3dB frequency if the junction current is not effectively modulated. Parasitic circuit elements, including series inductance or resistance and shunt capacitances, can limit the effective current modulation of the junction necessary to affect the light output. Parasitic inductance is usually contributed by the packaging rather than the laser diode die. However, there can be shunt capacitances due to VCSEL bond pads and oxide layers that limit VCSEL bandwidth to less than 20 GHz if not addressed. Figure 2.4 shows a cross-sectional diagram of a conventional high-speed VCSEL with a superimposed equivalent circuit schematic representing the pad capacitance, C_p, series contact and annular spreading resistance, R_s, and active area oxide capacitance, C_a, which shunt or otherwise restrict high-frequency current from flowing through the active aperture represented by R_a.

Calculations associated with the high-speed VCSELs reported in [27] indicated that the purely electrical circuit effects would allow a maximum 3dB modulation bandwidth of 18.8 GHz unless the oxide capacitance, C_a, was reduced using an ion implant.

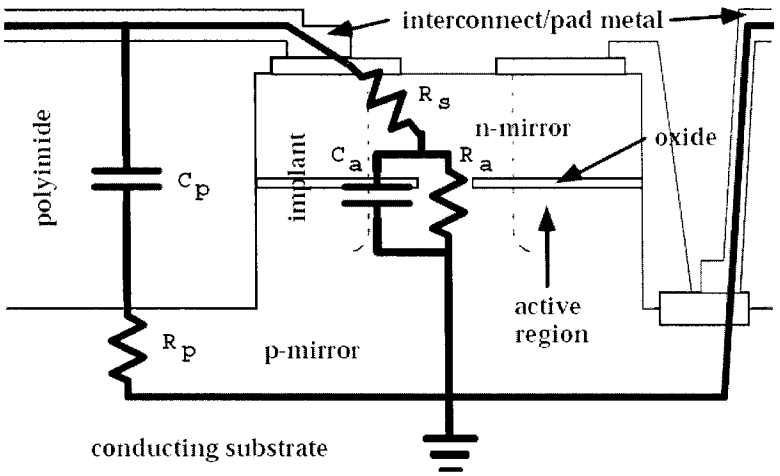

Figure 2.4 Schematic cross-section of conventional, top-emitting, high-speed VCSEL structure with superposed equivalent circuit [27].

2.4.2.2 Junction heating

Because laser diode bandwidth varies as $(I-I_{th})^{1/2}$, the laser must be biased at a current several times the threshold current, I_{th}, in order to reach high frequencies. A VCSEL with a threshold current of I_{th}=0.5mA was biased with I=2.4mA to reach approximately 18 GHz [27]. At the correspondingly high current density of 15kA/cm^2, there is significant heating and the estimated junction temperature is 50°C based on the thermal resistance of this 4μm device being about 5°C/mW. Such a temperature rise diminishes both the gain and differential gain, leading to lower resonance frequencies. This is believed to be a significant contribution to resonance frequency saturation.

To experimentally demonstrate the effect of junction temperature on resonance frequency saturation and the ultimate modulation bandwidth observed for VCSELs, a

comparable device was measured with stage (effectively the case) temperatures of T_{case}= -50°C, 25°C, and 100°C [27]. At T_{case}=25°C, a maximum bandwidth of 21.5GHz was observed at a bias current of 4 mA. However, when the case temperature was adjusted to T_{case}=-50°C, the bandwidth peaked at a maximum of 26 GHz at a much higher bias current of approximately 6.5mA. Based on the estimated thermal resistance of the device, the junction temperatures in both cases were believed to be 50°C. In order to allow operation to the large current levels necessary for higher speed operation, lower thermal resistances need to be achieved.

To reduce the VCSELs' thermal resistances, heat-sinking elements were incorporated within the VCSELs' structures. Different approaches have been reported to sink the VCSELs' junction heat and thus lower the thermal resistances and improve the performance, such as the electroplating of 8.5μm of gold on a (120x120) μm^2 pad around 8μm pillars [30], which resulted in about 60% improvement in the VCSELs' maximum output power. Another, more complex, approach was reported by attaching 20μm-diameter VCSELs to a Cu substrate after GaAs substrate removal, resulting in a 107% improvement of the device's maximum output power [31]. Another possible approach to reduce the junction temperature is the modification of the epitaxial structure design with more tolerance to temperature rises. For example, structures with higher confinement barriers should also permit higher junction temperature operation. Figure 2.5 shows R_{th} as a function of the active diameter for a range of device sizes for different generations of the fabricated VCSELs of the presented work. For active diameters greater than 7μm, the Cu plated heatsinks gave a 50% reduction in R_{th} for top-emitting VCSELs compared to the best known previously published results. More details about R_{th} reduction are

presented in Chapter 4, Sections 4.3.1 and 4.4.1 and 4.4.2. Figure 2.5 also summarizes previously published results of R_{th} as a function of the active diameter of VCSELs [6,7,27,30-33,35,36] that were fabricated using the various techniques listed in Table 2.1.

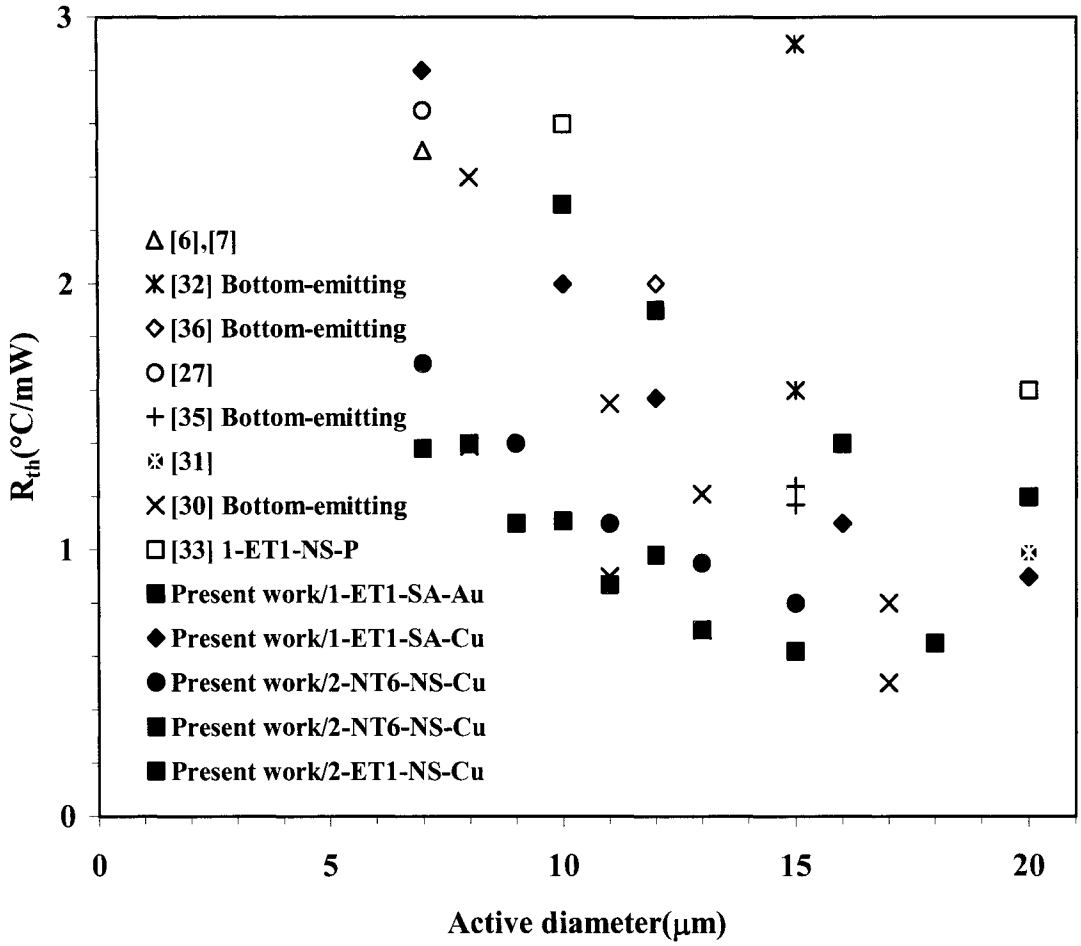

Figure 2.5 VCSEL thermal resistance as a function of the active diameter.

Table 2.1 Summary of the various techniques used to heatsink VCSELs.

Reference #	Fabrication technique
[24]	Polyimide planarized
[7]	SiN_x
[32]	Polyimide-bonded
[33]	Polyimide-wrapped
[34]	Air pillar
[31]	Attaching devices to a Cu substrate after GaAs substrate removal
[35]	Coplanar flip-chip and top contact with epoxy
[30], [36]	8.5μm Au electroplating
Present work	2-3μm Cu electroplating

2.4.2.3 Mode control

Another factor that was observed to limit the maximum bandwidth of VCSELs is the number of transverse modes. Higher modulation bandwidth was obtained from devices that operated in a single mode for an extended range above threshold. A maximum observed VCSEL bandwidth of 21.5 GHz was obtained using small (4x4) μm^2 aperture lasers that emitted only a single, fundamental transverse mode. Multimode devices achieved a maximum bandwidth of approximately 15 GHz or lower for larger devices [27]. Single-mode operation enhances the resonance frequency because all of the photons interact with the carrier population in the same way, and the resonance frequency is proportional to the square root of the number of photons in the mode. A number of interrelated factors contribute to single-mode operation, including the current distribution, gain-mode overlap, spatial hole-burning, and the relative loss of the higher-order modes. Top-emitting VCSELs rely on annular, peripheral contacts that lead to current crowding, which produces gain profiles peaked near the perimeter of the device. Such profiles favor high-order modes. Note that since the light must pass out of the device to one side, one of the contacts will always be annular. The various ways that have

been reported to promote the VCSELs' single-mode operation will be discussed in the end of the following section.

2.5 Review of previous work in high-speed VCSEL fabrication and reduction of related parasitics

As mentioned in the previous section, since VCSEL speed is often determined by circuit parasitics, many research groups have tried different ways of reducing these parasitics.

Mirror resistance can be reduced to some extent by using means such as delta doping, which Dr. Kojima and his group did in 1993 [37]; changing the VCSEL structure itself, as Dr. M. K. Hibbs's and Dr. R. A. Morgan's group did in 1994 [38,39]; or by using the metal organic vapor phase epitaxy (MOVPE) method, which was illustrated by Dr. K. L. Lear and his group in 1994 [40]. Using delta doping in VCSEL mirrors, it was reported that the differential resistance was reduced almost by half and the peak output power was increased by 40%. MOVPE was used to implement a new mirror scheme. Mirrors with low vertical resistance can be achieved by grading mirror interface and decreasing alloy composition. As a result, low lateral resistance, high reflectivity, and high thermal conductivity were obtained [40]. To date, much work has been done to achieve low resistance.

On the other hand, parasitic capacitances in oxide-confined VCSELs are pad [26,41] and oxide capacitance [41]. To reduce pad capacitance, three parameters can be changed: pad area [26], dielectric material, and the dielectric material thickness. Equation 2.1 illustrates the relationship between these three parameters.

$$C_{pad} = \frac{\varepsilon_o \varepsilon_r A}{d} \tag{2.1}$$

where ε_o is the permitivity of free space, ε_r is the relative dielectric constant, A is the pad area, and d is the dielectric material thickness.

Clearly, reducing the pad area, increasing the thickness of the dielectric material, or using a dielectric material that has a low dielectric constant will decrease the pad capacitance and thus increase the 3dB frequency response of the VCSEL:

As reported in [26], the PSPICE program was used to simulate the VCSEL equivalent circuit using different pad areas. As a result, reducing the pad area to one fourth (25x25)μm^2 of its normal area, which is (50x50)μm^2 [26], improved the VCSEL dynamic response to more than 7.9 GHz (at 3dB). Two VCSELs with pad areas (20x20)μm^2 and (50x50) μm^2 were also fabricated. Results show that VCSELs with the smaller pad area exhibit a 3dB modulation frequency of 6.5GHz while VCSELs with the larger pad area exhibit a 3dB modulation frequency of only 3.2GHz.

Changing the dielectric material used to planarize the VCSEL, as well as increasing its thickness, will increase the modulation frequency. In other words, a low dielectric constant material, as well as keeping the thickness of this material at a maximum, will result in lower pad capacitance. A study of four spin-on dielectric materials will be presented in Chapter 5.

Reducing the oxide capacitance will also result in increasing the modulation response of the VCSEL. Several values of the VCSELs' modulation frequencies were reported by different research groups, but the fastest-ever realized VCSEL of 850nm was demonstrated by the Sandia National Laboratories group [27]. The modulation frequency for this device was reported to be in excess of 20GHz at room temperature. To achieve

this, the group reduced the oxide capacitance by using an ion implantation process, as shown in Figure 2.6.

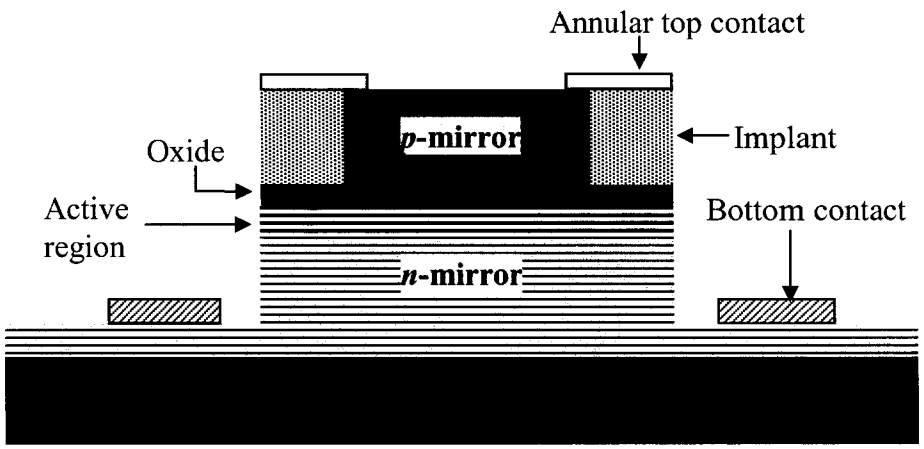

Figure 2.6 Implanted and oxidized VCSEL cross- section (reproduced after [27]).

Low-capacitance VCSELs with modulation bandwidths of 17.0 GHz based on a simplified, robust process incorporating photosensitive polyimide were reported by the author [33]. The process does not require ion implantation [27], deep field etches to semi-insulating substrates and subsequent metal step coverage, or very small pad areas [26]. Figure 2.7 shows a scanning electron microscope (SEM) photo for a completed high-speed VCSEL ready for testing. As shown in Figure 2.8, the 7 μm diameter aperture laser exhibits a very flat modulation response with a 17.0 GHz bandwidth when biased at I_{bias}=4.5 mA at room temperature [33].

As shown in Figure 2.9, measured 3dB frequencies at different bias currents follows the theoretical expectations for $I_{bias}<10I_{th}$. After that, the measured 3dB modulation frequency tends to saturate with further increase in the bias current. Reference [33] reported that this saturation is due to junction heating although data

presented at the end of Section 4.4.2 indicates that similar saturation can be caused due to multimode operation.

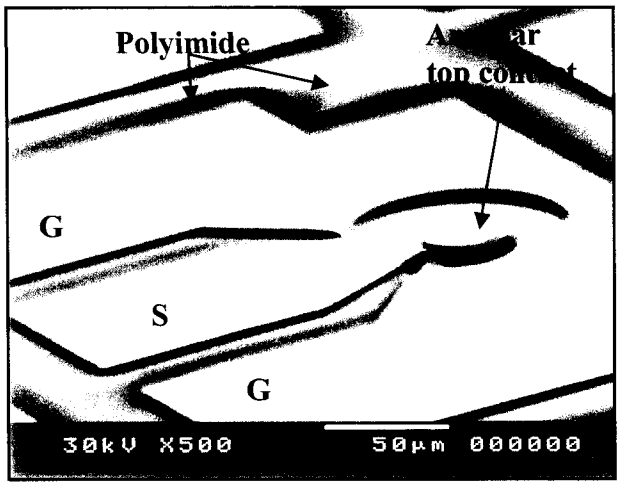

Figure 2.7 An SEM photo for a completed high-speed VCSEL ready for testing [33].

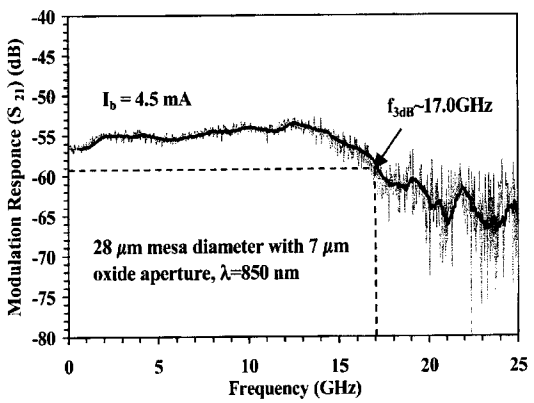

Figure 2.8. VCSEL modulation response [35].

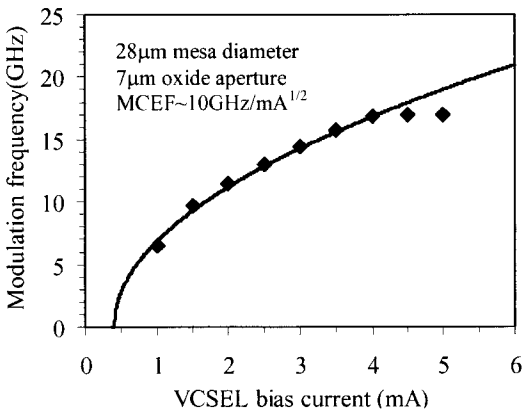

Figure 2.9 VCSEL bandwidth vs. oxide aperture [35].

In addition to polyimide, BCB, which has a relative dielectric constant (ε_r ~2.5) lower than that of polyimide (ε_r ~3.4), was used to fabricate high speed 850nm VCSELs [42]. A 19GHz bandwidth at a current density of 30kA/cm^2 was calculated for these devices based on a measured relaxation oscillation frequency (f_r) of 12GHz and the assumption of a low damping condition using $f_{3dB}=1.55f_r$ [42]. Based on the data

provided in [42], I believe that the assumption of low damping (<<1), which leads to an ideal case where the f_{3dB} is about 1.55 times higher than f_r, is not valid.

While VCSELs show single-mode operation under continuous wave (CW) conditions, it has been demonstrated that this might change into multimode operation when the bias current is modulated [43]. For example, the 780nm VCSELs with 4μm active diameter reported in [43] exhibit a single-mode operation with about 30dB side mode suppression ratio (SMSR) when operated under CW conditions, and the same devices exhibited only 15dB SMSR under large signal modulation with Vpp=0.5V at the same bias current. To obtain a consistent single-mode operation under CW and small signal modulation conditions and thus promote the VCSELs' modulation bandwidth, various techniques have been used, such as the use of a multi-oxide layer and a micro-machined surface relieved structure, which Dr. Iga and his group reported in 2000 and 2001, respectively [44,45], or the incorporation of a photonic crystal pattern with oxide-confined VCSEL structure, as Dr. Choquette's group did in 2004 [46].

Using a multi-oxide layer structure [44], it was reported that an 8μm oxide aperture structure maintained single-mode operation with bias currents up to four times the threshold current at about 960nm wavelength. The reported multi-oxide layer structure devices were not tested for mode stability under small signal modulation conditions. The micro-machined surface relieved devices reported in [45] have a 9μm oxide aperture and 14μmx0.5μm trenches, which were fabricated using a focused ion beam. These devices reported to have a stable single-mode operation (SMSR~30dB) under both CW and small-signal modulation at a bias current of 2 times the threshold current (I_{th}~2mA) and V_{pp} of 0.25V and 0.5V with data transmission rate of 2.5Gp/s.

On the other hand, the incorporation of photonic crystal patterns with oxide-confined VCSEL structures [46] reported by Dr. Choquette and his group were able to operate at a single-mode operation under both CW and small-signal modulation with SMSR values of about 40dB and 30dB, respectively, even though the reported devices have relatively large oxide apertures of $(6x6)\mu m^2$ and $(10x10)\mu m^2$. Furthermore, the reported VCSELs exhibit a 3dB bandwidth of 9GHz.

Figure 2.10 below summarizes the presented and other reported current densities for various VCSELs bandwidths [26,27,33,42,47-53] fabricated using various techniques. The x-axis arrow (yellow), the y-axis arrow (green), and the diagonal arrow (yellow and green) point to the preferred direction for J_{bias}, f_{3dB}, and the combination of both J_{bias} and f_{3dB}. Present work results will be discussed in greater detail in Chapter 4.

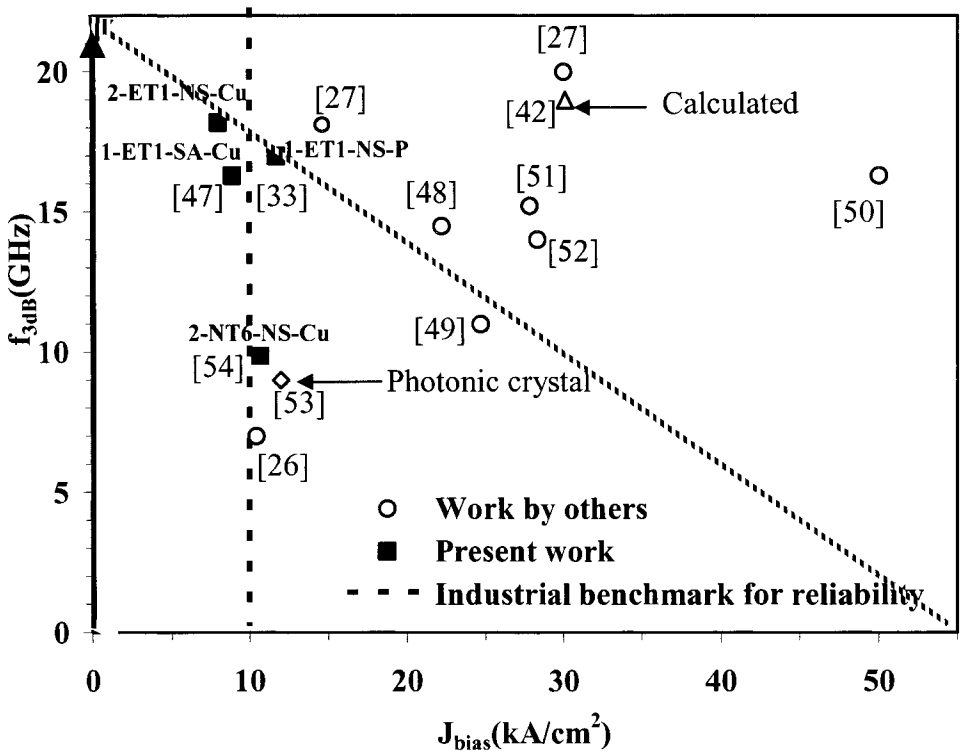

Figure 2.10 VCSELs' bandwidths vs. current densities.

2.6 New design and concept

In this section, new VCSEL structures specifically designed for high-speed operation will be presented. The structures to be developed are top- and bottom-(substrate-side) emitting structures that incorporate special structural considerations to improve heat-sinking, moderate current density non-uniformity, and reduce unnecessary device areas. The new VCSEL structures and a summary of the relative advantages accruing to them are presented in Section 2.6.1. Summaries of the planned fabrication steps sequence for both top- and bottom-emitting structures are described in Section 2.6.2.

As explained in Section 2.6.1.1, a considerably lower thermal resistance can be achieved due to the proximity of the plated Cu heatsink layer to the active junction of the laser, which reduces the junction temperature at the high drive current densities needed for high-speed operation. The reduced mesa size minimizes the oxide area, which in turn reduces the parasitic RC time constant of the VCSEL, as explained in Section 2.6.1.2. The nominal mesa diameter also allows the more efficient heat extraction through the mesa sidewall. More uniform current injection due to the directly aligned contact with the active region promotes single-mode operation, as described in Section 2.6.1.3.

2.6.1 New designs

In order to address the limitations listed in Section 2.4, new VCSEL structures specifically designed to reduce constraints on modulation bandwidth were fabricated that simultaneously diminish the source of each limitation. The structures to be developed are top- and bottom-emitting VCSELs with special structural considerations to improve heat-

sinking, current density uniformity, and reduce unnecessary device areas. These improvements benefit junction temperature, single-mode operation, and parasitic circuit element issues, respectively.

Figures 11 and 12 (a) and (b) show cross-sections of a conventional top-emitting oxide-confined VCSEL of the type that has demonstrated the highest modulation speeds to date [27] and the new top- and bottom-emitting copper-plated VCSELs, respectively. Following are a number of relative advantages that accrue to the top- and bottom-emitting structures:

2.6.1.1 Lower thermal resistance

A key benefit of both structures is their reduced thermal resistance due to the proximity of the plated copper heatsink to the active junction of the laser. This reduces

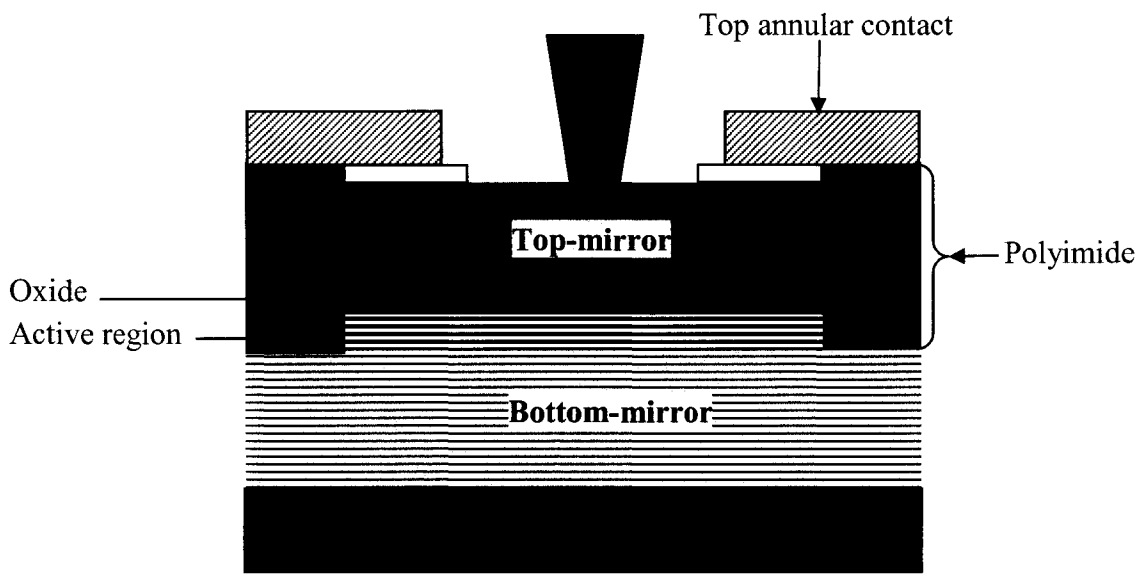

Figure 11 Conventional oxide VCSEL of the type used for prior high-speed designs.

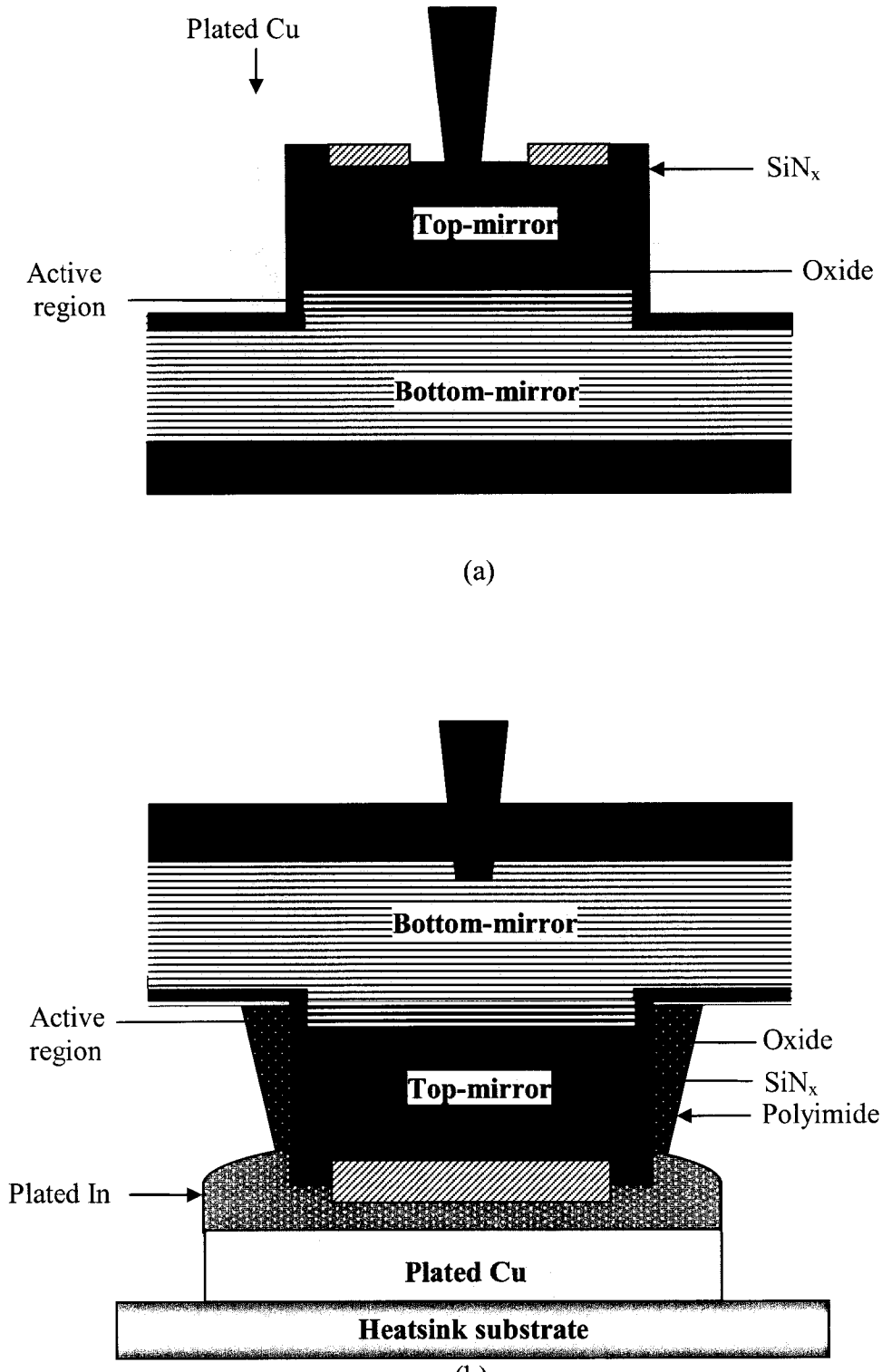

Figure 12 Proposed (a) top-emitting and (b) bottom-emitting devices with reduced mesa and oxide dimensions and wrap-around plated copper heat spreader.

the junction temperature at the high drive currents required for high-speed operation. The thermal resistance is lowered not only because of heat flow perpendicular to the mirror and directly into the heatsink without an intervening substrate, but the wrap-around heat sink structure also allows heat flow in the lateral direction. Another benefit of the reduced junction temperature is that it will offer higher reliability since degradation mechanisms are thermally activated.

2.6.1.2 Reduced parasitic circuit elements

The proposed structures substantially reduce the area of the parasitic capacitor elements that can limit external electrical bandwidth. The reduced mesa size minimizes oxide area, thus reducing the high capacitance associated with the thin oxide layer, which reduces the parasitic RC time constant of the VCSEL, resulting in faster devices. The minimal mesa diameter also allows more efficient heat extraction through the mesa sidewall, which also promotes high-speed operation.

A bond wire pad is no longer required for the bottom-emitting structure, and although metal traces on the submount (heatsink) will run out from under the VCSEL die, they will be separated from the die by air with a relative dielectric constant lower than either polyimide or semiconductor. The oxide area has also been reduced from a typical value of ~1800 μm^2 for the conventional top-emitting structure to as little as 75 μm^2 in the small mesa top- and bottom-emitting structures. The reason that the oxide is not completely eliminated from the mesa is that it is useful for mode control, reduced scattering compared to the mesa sidewall, as well as control of diffusion currents reaching the sidewall. The diffusion currents can be an important contribution to the

overall current for small devices. The flip-chip structure also reduces spreading current resistance present in annularly contacted top emitting structures [2].

2.6.1.3 Enhanced single mode operation

While top-emitting VCSEL design might suffer from multimode operation due to its annular top contact, which causes current crowding that modifies the gain profile, the more uniform current injection provided by the flip-chip structure due to the directly aligned top ohmic contact to the active area is expected to promote single, fundamental-mode operation with maximum photon density. Other design parameters to be considered for laser mode control in top- and bottom-emitting VCSELs are discussed in the future work section, Chapter 6.

Although epitaxial improvements have not been incorporated in the presented work, it is worth mentioning that such improvements can be utilized to maximize the modulation rate of the VCSELs as discussed in the future work section Chapter 6.

2.6.2 High-speed, top- and bottom-emitting VCSEL fabrication summary

Using the structures illustrated in Figure 12 (a) and (b), the extrinsic limitations will be reduced in comparison to the conventional structure shown in Figure 11. Following are summaries of the planned process sequence for both structures.

2.6.2.1 Top emitting VCSEL process sequence summary

1. Etch small-diameter mesas approximately 2 to 8μm larger in diameter than the intended aperture size.

2. Oxidize the sample the limited amount required.
3. Form the contacts on top of the mesa.
4. Form the bottom contacts.
5. Protect the mesa side walls with a nitride layer.
6. Planarization using photosensitive polyimide.
7. Plate up a copper heatsink around the mesa and the coplanar waveguide probe pads.

2.6.2.2 Bottom-emitting VCSEL process sequence summary

1. Etch small-diameter mesas approximately 2 to 8μm larger than the intended aperture size.
2. Form the contacts on top of the mesa.
3. Oxidize the sample the limited amount required.
4. Form the bottom contacts.
5. Protect the lower portion of the mesa with photosensitive polyimide.
6. Plate up a copper heatsink around the mesa and at the same time, copper posts on the top-mirror contact.
7. Dice the sample and flip-chip solder the die onto an appropriately patterned copper/indium electroplated submount heatsink.

The detailed process sequence for both top- and bottom-emitting structures will be discussed in more detail in Chapter 4.

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Chapter 3

FABRICATION AND PROCESS DEVELOPMENT

3.1 Introduction

Oxide-confined vertical-cavity surface-emitting lasers are VCSELs with an oxide aperture formed by wet oxidation of $Al_xGa_{1-x}As$ to form aluminum oxide Al_2O_3 where x is close to 1.

Fabricating VCSELs requires a number of processing steps carried out in the proper sequence. VCSELs designed for high-speed operation require additional processing steps designed to reduce electrical parasitics that would otherwise limit their speed. This chapter discusses in detail the steps used in producing high-speed top- and bottom-emitting VCSELs. Sections 3.2 and 3.4 will summarize the overall process for top- and bottom- emitting devices respectively, and then Sections 3.3, 3.5, and 3.6 will detail steps used for contact formation, mesa etching, oxidation, planarization, interconnect metal deposition, and finally, copper electroplating.

3.2 Overall process for oxide confined top-emitting VCSEL fabrication

3.2.1 Epitaxial growth

Epitaxy is a process whereby the required types and compositions of semiconductor alloys are grown on top of each other in a certain order with a certain thickness on a compound semiconductor substrate [1]. In this case, the compound semiconductor substrate is GaAs. Epitaxial growth requires that the grown material and the substrate material have the same crystal structure. The lattice constants (space between 2 atoms) of

the grown material and the substrate material should be as close as possible, and the difference between them, called the lattice mismatch, should be in the range of a few percent or less. There are three commonly used compound semiconductor growth techniques. These are Metal Organic Chemical Vapor Deposition (MOCVD) [2], Liquid Phase Epitaxy (LPE), and Molecular Beam Epitaxy (MBE) [3].

The wafers with epitaxial material used for the devices fabricated as part of this research were supplied by Emcore via Mission Research Corporation (λ=850nm), Novalux Inc. (λ=980nm) and Opticomp Inc. (λ=980nm). There are two major differences between the 850nm and 980nm structures used. The first obvious one is the emitting wavelength [4]. The second is that the 980nm structures were grown on an *n*-type substrate, which will end with *p*-side-up VCSELs. On the other hand, the 850nm structure was grown on a *p*-type substrate. This will result in *n*-side up VCSELs that offer a compatible electrical polarity with the *npn* bipolar-junction transistors used in driving circuits for VCSELs [5]. Figure 3.1 represents the general structure of the grown wafer that was used in this process. More details about the various structures will be presented later in this chapter.

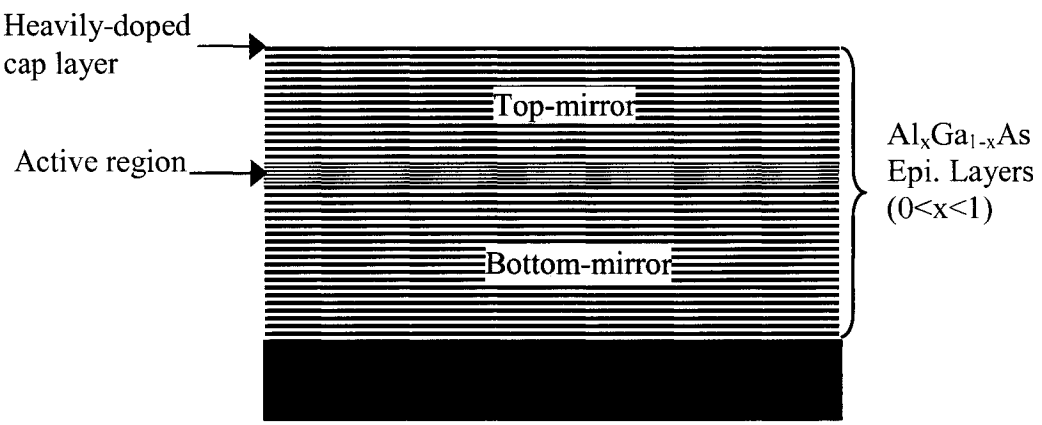


Figure 3.1 General structure of Epi. layers grown on a GaAs substrate.

The wafer is now ready to proceed to the next step of VCSEL fabrication. Two different approaches have been used to begin the device fabrication. One involves non-self-aligned devices in which the mesas were formed first, and then the top annular contacts were deposited. The other approach was to deposit the top annular contact first and then the mesas were formed after protecting the annular contact aperture with photoresist. In this approach, the top contact will be self-aligned with the device mesa and the oxide aperture. These devices are referred to as self-aligned devices.

3.2.2 Top-emitting non-self-aligned VCSEL fabrication

This section will summarize the overall fabrication process for top-emitting non-self-aligned devices.

3.2.2.1 Mesa etching

Mesa etching for vertically stacked layers has to be done in such a way as to electrically isolate a working VCSEL to restrict undesirable leakage currents, make contact to underlying layers, and expose the $Al_xGa_{1-x}As$ layer with high Al composition for subsequent oxidation. It is important to expose the high Al composition layer to water vapor since our VCSELs are oxide-confined VCSELs, which means that water vapor is necessary as an oxygen source to oxidize the high Al composition layer to form the required aperture [6]. Wet oxidation will be discussed later in this chapter.

The patterned photoresist served as an etch mask for cylindrical mesas formed by etching to a certain depth into the bottom mirror using a load-locked, ICP dry-etching

system, for which further information will be provided later in this chapter. The sample cross-section, including the resist, the etched areas and the mesa, are shown in Figure 3.2.

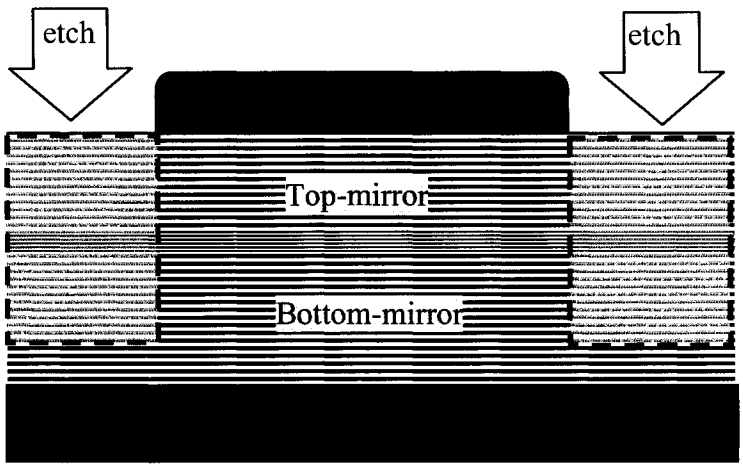


Figure 3.2 Device cross-section showing the resist and areas to be etched.

3.2.2.2 Wet oxidation

Due to its advantages in forming the current aperture and providing a lateral index guiding to the lasing mode [7], wet oxidation is used to fabricate high-speed VCSELs. The high Al composition layer, which we discussed in the epitaxial growth and the mesa etching sections, has a higher oxidation rate than the rest of the mirror stacks under the same conditions [6,8]. Wet oxidation is carried out by exposing the sample to a high temperature (>350°C) steam environment [6]. The equipment setup and schematic diagram of the oxidation furnace will be discussed in detail in Section 3.3. Figure 3.3 represents the mesa after oxidation. Note that the layer with the highest Al percent oxidized further than the other layers. After the oxidation step, our mesa now has an oxide aperture with a certain diameter, depending on many variables in the oxidation process [6].

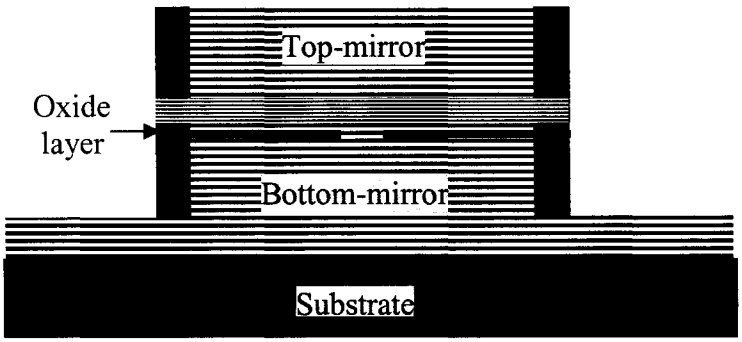


Figure 3.3 Mesa after oxidation. AlGaAs layers with different Al percent, which are converted to Al-oxide, are shown in orange.

3.2.2.3 Ohmic contacts (top contacts)

An ohmic contact should have a low contact resistance compared to the bulk resistance of the semiconductor [6]. Top contacts are applied by evaporating the required types of metals onto the sample after the sample passes through the photolithography process, as shown in Figure 3.4, for top contact ready for metal deposition.

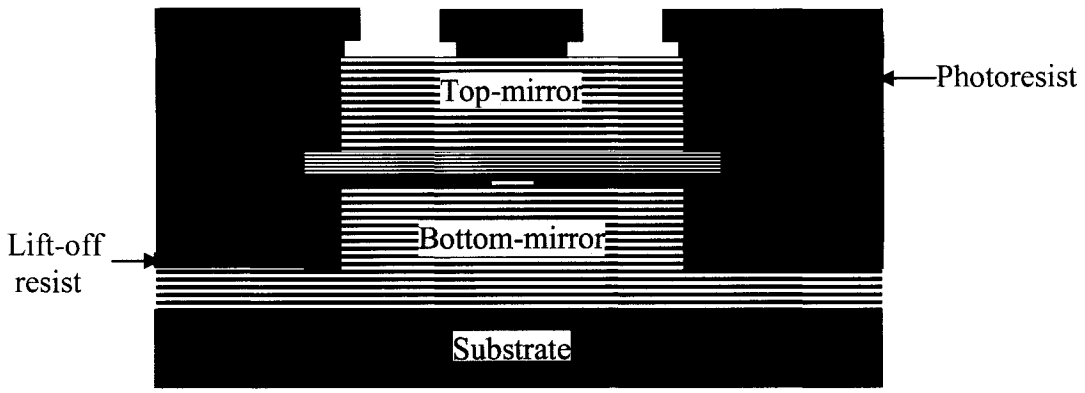


Figure 3.4 Sample covered with lift-off resist and photoresist after developing is ready for metal deposition.

As shown in Figure 3.4, it is important to get an overhanging photoresist profile by the edges since this will result in an easy, clean metal lift-off step. After checking the

profile using the microscope, the sample is ready to proceed to the next step, which is loading the sample into the evaporator.

After loading the sample into the evaporator, the pressure needs to be pumped down to a low level. The required combination of metals can then be evaporated by melting each metal in sequence, using an electron-beam. After unloading the sample, its entire surface will be covered with the evaporated metals.

Lift-off is a simple, uncomplicated method for patterning metal films that are deposited. Lift-off processing can be done with acetone, whereby the photoresist will be stripped away, removing with it all the unwanted metals that lie on top of the photoresist surface, while the metals in the photoresist openings adhere directly to the substrate and remain [3] as shown in Figure 3.5.

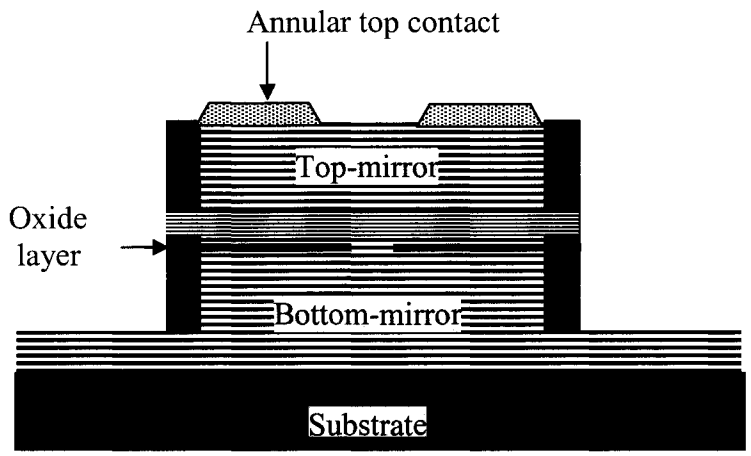


Figure 3.5 VCSEL mesa after metal evaporation and lift-off.

After contact-metal evaporation and lift-off, the sample will go through the high temperature alloying step. The sample temperature is increased until the contact metals alloy onto the surface of the semiconductor. For the top contacts, the metals are alloyed

into the thin GaAs cap layer, shown in Figure 3.1. The sample is now ready to proceed to the bottom contact process.

3.2.2.4 Ohmic contacts (bottom contacts)

For bottom contacts, the sample will go through the same process as for the top contact except that the types of metals that needs to be evaporated, as well as the photomask, will be different, as will be discussed in a later section. Figure 3.6 below shows the mesa after applying the bottom contacts.

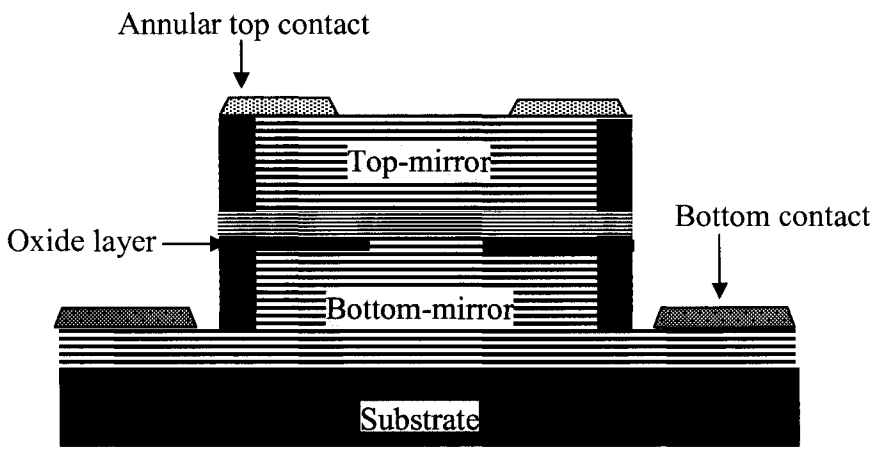


Figure 3.6 Mesa after bottom contacts deposition.

3.2.2.5 Mesa sidewall insulation (SiN_x)

After contact formation, a thin layer of silicon nitride, SiN_x, needs to be deposited and partially etched to electrically insulate the mesa sidewall from later metal deposition. After the silicon nitride deposition, the sample passes through the photolithography process, and then the nitride is etched using tetrafluoromethane gas (CF_4), as will be discussed in more detail later in this chapter. Figure 3.7 represents the VCSEL mesa after opening vias through the deposited nitride and photoresist striping.

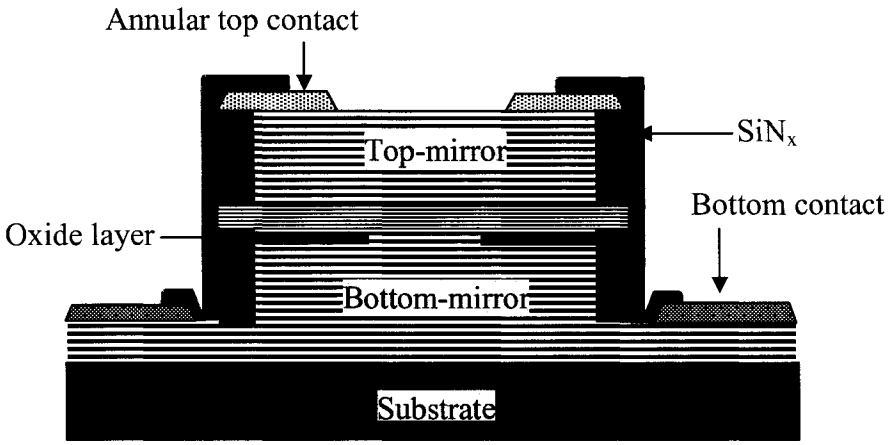
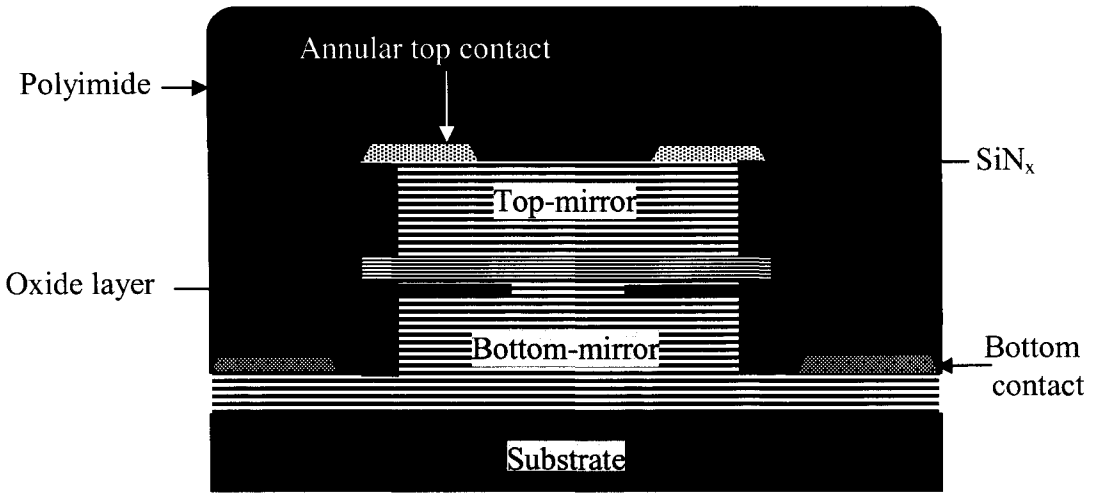


Figure 3.7 VCSEL mesa after opening vias through the deposited nitride and striping the photoresist.

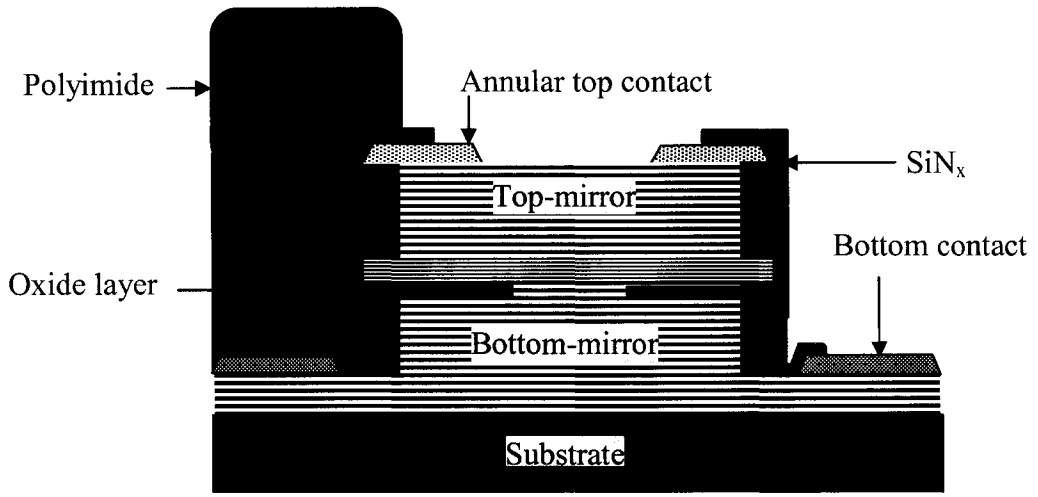
3.2.2.6 Planarization

The surface of the mesa must be planarized for several reasons. A smooth surface is needed for metal interconnects and metal bonding pads to be patterned and deposited and planarization material creates an isolation layer between the n and p contacts. Planarization is also used in fabricating many high-speed electronic devices, including VCSELs, for reduction of parasitic circuit elements that may limit device speed (as discussed in greater detail in Chapter 5). The use of photo-definable polyimide is one of the common approaches for planarization.

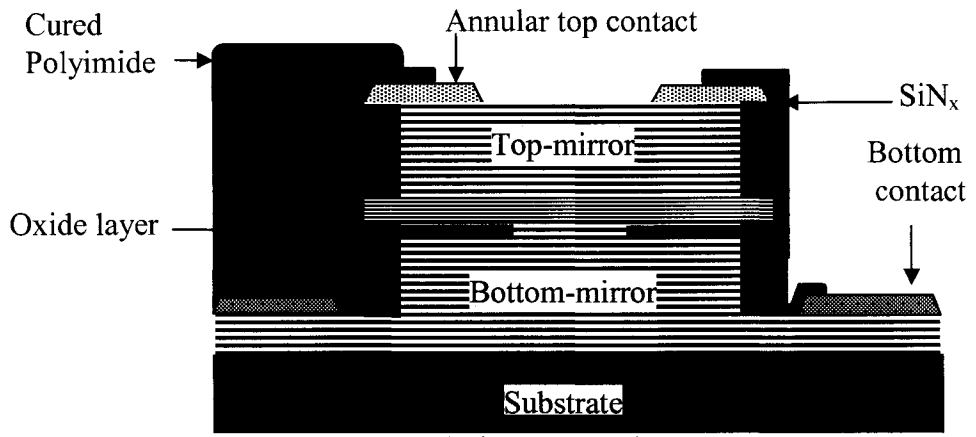
The polyimide is applied to the sample. It then has to go through a lithography process similar to the lithography process for the photoresist described earlier in this chapter. After developing, the polyimide has to be cured. A more detailed discussion of curing polyimide will be presented later in this chapter. Figure 3.8 illustrates the three main steps in mesa planarization.



(a) Polyimide all over the mesa.



(b) Polyimide after developing.



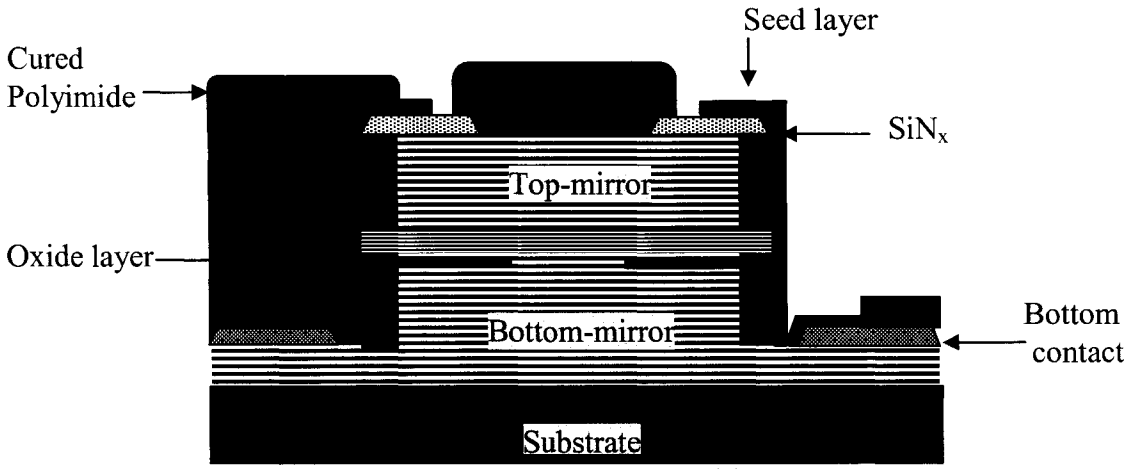
(c) Polyimide after curing.

Figure 3.8 Different stages of mesa planarization.

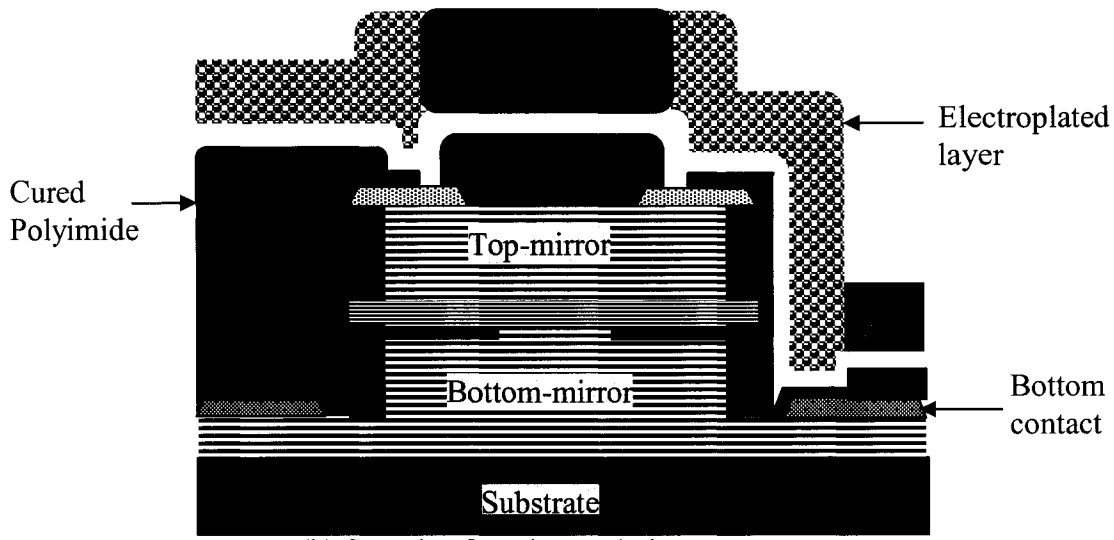
3.2.2.7 Electroplated metal interconnects

In order to test the sample, we now need metal interconnects so that we can place the probe station tips on metal pads to electrically contact the VCSEL. Based on the new design presented in Chapter 2, the mesa needs to be wrapped with metal for heat sinking. The electroplating process uses an ionic solution to deposit metal atoms onto a pre-existing conducting surface. Current passing through the solution is carried to the surface by metal ions, which then remain. Consequently, the deposited metal thickness at a point on the surface will depend on the current density flowing through the surface at that point. This can lead to geometrical dependencies of the deposited metal thickness, such as edge enhancement.

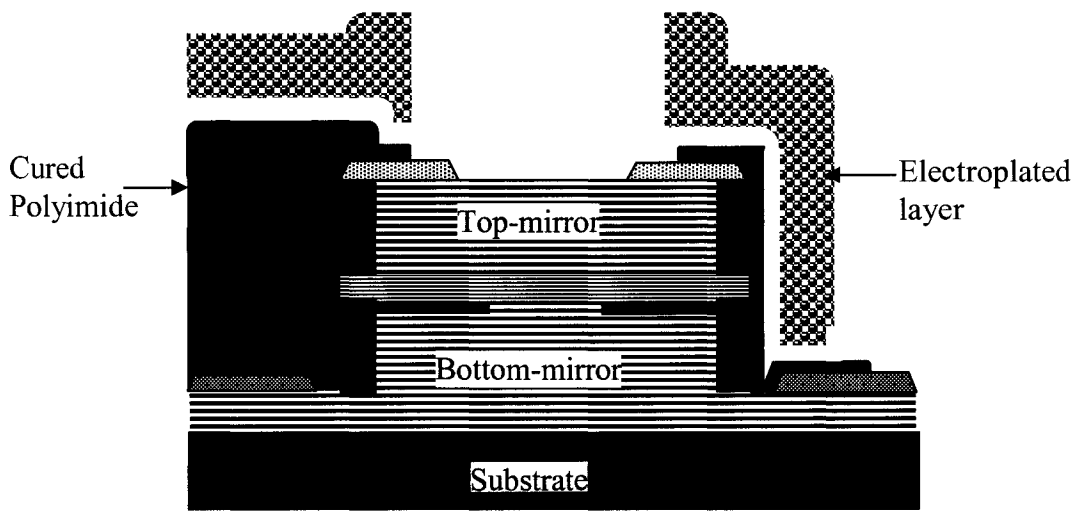
The sample needs to go through the photolithography process to protect the VCSEL aperture where a seed layer (~800Å) will be deposited. After deposition, a second photolithography process is needed to pattern the areas for electroplating. More details on electroplating will be presented later in this chapter. After electroplating to the required metal thickness, the second layer of photoresist is stripped, the seed layer is etched, and finally, the first photoresist layer is stripped. Figure 3.9 illustrates the three main steps in mesa electroplating.



(a) Sample after seed layer deposition.



(b) Sample after electroplating.



(c) Sample after seed layer etching and resist 1 stripping.

Figure 3.9 Different stages of mesa electroplating.

3.2.3 Top-emitting self-aligned VCSEL fabrication

This section will summarize the overall fabrication process for top-emitting self-aligned devices.

3.2.3.1 Ohmic contacts (top contacts)

This step is carried out using the procedure described in Section 3.2.2.3, including the alloying step. Figure 3.10 (a) and (b) shows the sample before metal deposition and after lift-off, respectively. The sample is now ready to proceed to the mesa etching step.

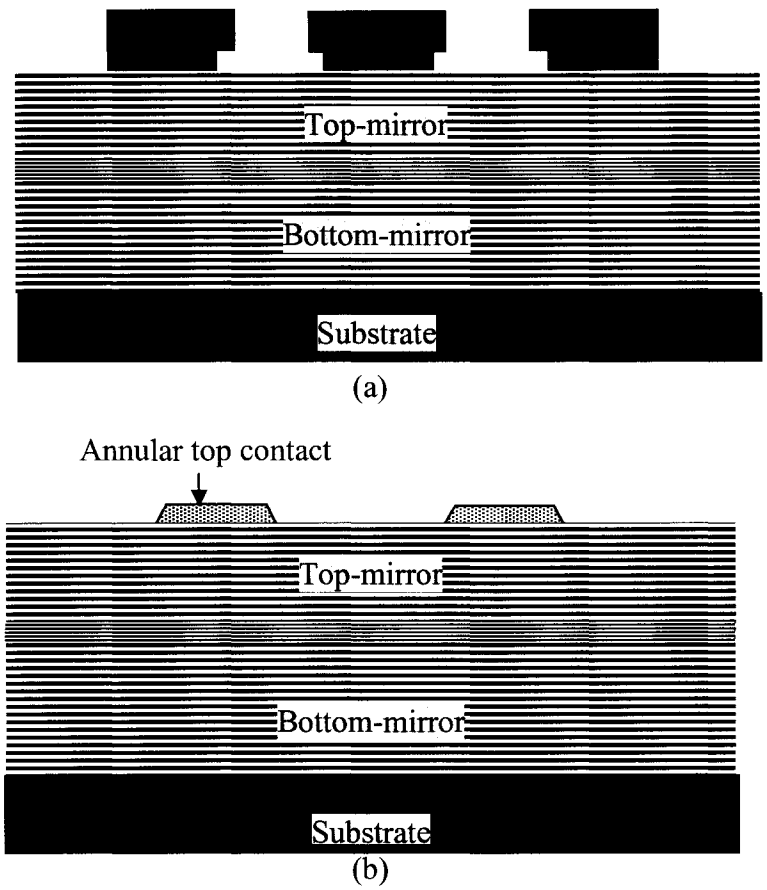


Figure 3.10 (a) Sample covered with lift-off resist and photoresist, after developing. (b) Sample after metal evaporation and lift-off.

3.2.3.2 Mesa etching

The contact and a smaller diameter photoresist feature protecting the aperture served as an etch mask for cylindrical mesas formed by etching to a certain depth into the bottom mirror using a load-locked, ICP dry-etching system. As shown in Figure 3.11, the use of the contact to define the outer perimeter of the mesa etch mask results in a device mesa that is self-aligned to the contact. The sample cross-section after etching and photoresist stripping is shown in Figure 3.12.

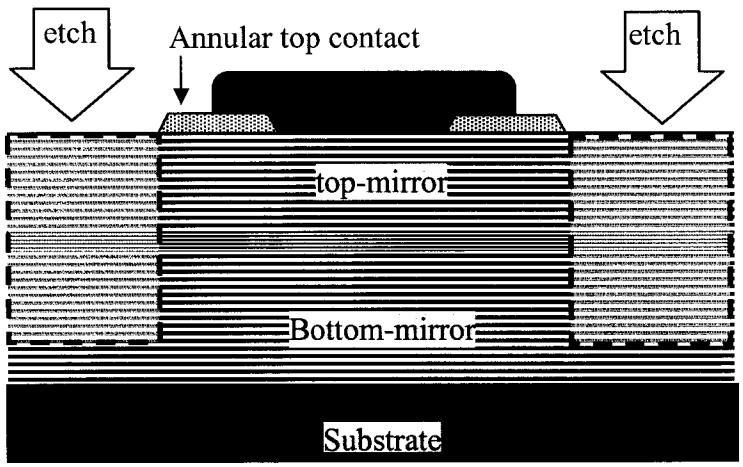


Figure 3.11 The top contact and a smaller diameter photoresist feature protecting the aperture served as an etch mask for cylindrical mesas.

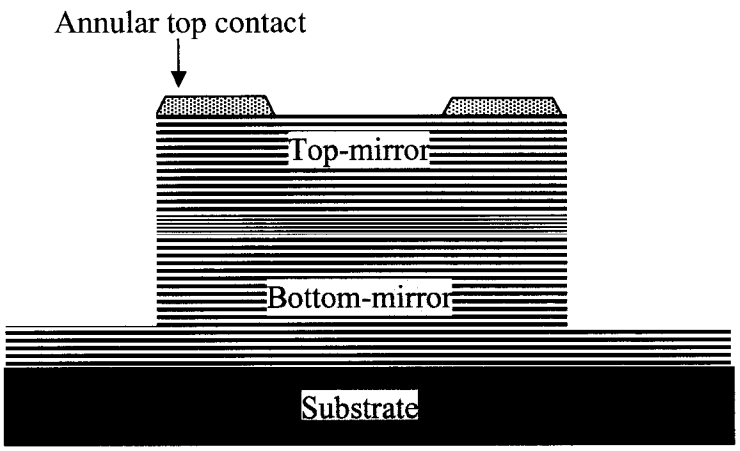


Figure 3.12 VCSEL mesa after etching and stripping the photoresist.

After stripping the photoresist, the sample is now ready to proceed to the next step, which is wet oxidation. From this step on, the self-aligned devices are processed using the same fabrication steps used for fabricating the non-self-aligned devices described in Sections 3.2.2.4 through 3.2.2.7.

3.3 Top-emitting high-speed VCSEL fabrication

3.3.1 Non-self-aligned 850nm VCSELs

In this section the detailed fabrication process for top-emitting non-self-aligned VCSELs will be presented.

3.3.1.1 Epitaxial growth

Top-emitting, non-self-aligned high-speed 850 nm VCSELs were fabricated from an AlGaAs structure on a *p*-type substrate as shown in Figure 3.1 [5]. The active region contains five GaAs (80Å)/$Al_{0.2}Ga_{0.8}As$ (80Å) quantum wells with calculated refractive indices of 3.66 and 3.49, respectively, using equation 3.1[9]. The n-mirrors have 25 periods of $Al_{0.92}Ga_{0.08}As$ (701.1Å)/$Al_{0.16}Ga_{0.84}As$ (605.4Å) *n*-DBRs with calculated refractive indices of 3.05 and 3.52 [9]. The p-mirrors have 35 periods of $Al_{0.92}Ga_{0.08}As$ (701.1Å)/$Al_{0.16}Ga_{0.84}As$ (605.4 Å) *p*-DBRs with corresponding refractive indices of 3.03 and 3.51. The layer that has the highest composition, x=0.98, ($Al_{0.98}Ga_{0.02}As$), is buried inside the *p*-DBRs with a thickness of 707.7Å and a 700Å barrier from the quantum wells. The cap layer is an *n*-GaAs layer with an 116.8Å thickness and a doping concentration of (1-2)x10^{19} cm^{-3}. The doping of both *n*-DBRs and *p*-DBRs are in the range of (1-2)x10^{18} cm^{-3}.

$$n(\lambda,x)=\left(A_o\left[\left(\frac{2-\sqrt{1+A_1(\lambda,x)}-\sqrt{1-A_1(\lambda,x)}}{(A_1(\lambda,x))^2}\right)+\frac{A_2(\lambda,x)}{2}\left(\frac{A_2(\lambda,x)}{A_1(\lambda,x)}\right)^{\frac{3}{2}}\right]+A_3(x)\right)^{\frac{1}{2}} \quad (3.1)$$

where :

n : refractive index

λ : wavelength in the vacuum

x : Al fraction in the $Al_XGa_{1-X}As$ alloy

$h = 6.626 \times 10^{-34}$ Js

$c = 2.998 \times 10^{8}$ m/s

$$A_o(x) = 6.3 + 19x$$

$$A_1(x) = \frac{hc}{\lambda(1.425 + 1.155x + 0.37x^2)}$$

$$A_2(x) = \frac{hc}{\lambda(1.765 + 1.155x + 0.37x^2)}$$

$$A_3(x) = 9.4 - 10.2x$$

3.3.1.2 Mesa etch

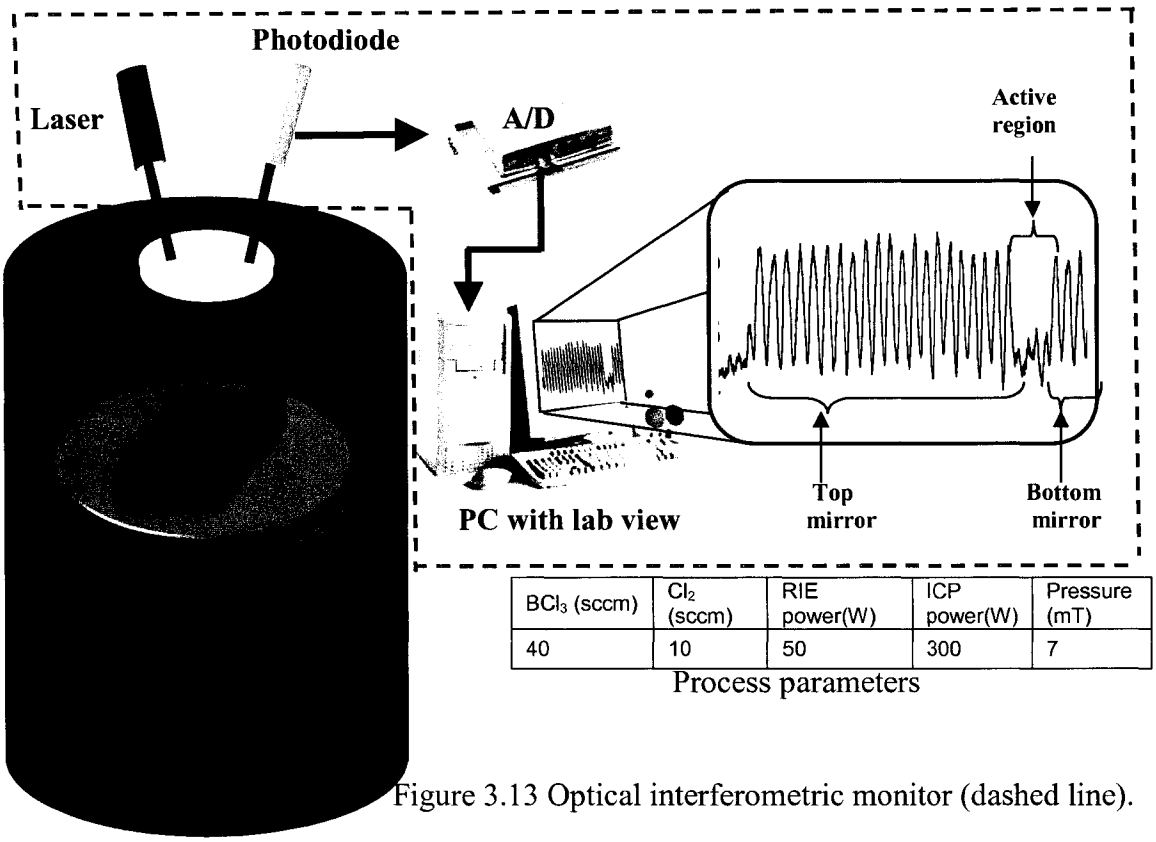
Dry etching has several advantages over wet etching. It offers considerable directionality and etches more rapidly in the vertical direction than the horizontal direction. Some cases can result in a lateral etch rate close to zero, and hence undercutting of masked patterns can be significantly reduced. Moreover, dry etching is

capable of patterning smaller geometric features (on the order of one micron) than wet etching. Furthermore, there is less contamination and higher purity compared to wet etching. Also, dry etching provides steeper sidewalls that will result in a larger mesa surface area [3, 10].

After cleaning with solvents, the sample was blown dry with N_2 to remove any residual fluid from the sample surface. The sample was then baked at 120°C to remove any moisture from the surface, since the photoresist properties depend on the amount of moisture in it. Liquid photoresist (Shipley 1818) was then applied. The photoresist was deposited in a puddle on the sample, which had been previously positioned on a spinner. Next, the sample was spun at approximately 5000 rpm for 30 seconds to evenly distribute the photoresist across the sample and to make the photoresist adhere to the sample [3]. The thickness of the photoresist after spinning is a function of photoresist viscosity and spin speed, but usually ranges from about 1μm to 10μm. The thickness of the photoresist can be tested by scratching away part of the photoresist (optionally prepared on a dummy sample) and using a surface profilometer, e.g., Alpha Step 100, to measure its thickness. (For more information about how to operate the Alpha Step 100 profilometer refer to [11]). Next, using the mask aligner, the mesa photomask was aligned with the sample and the sample UV-exposed for 11 sec. at 15mW/cm^2. The 11 seconds exposure time was determined based on the exposure dose decided by the manufacturer. Next, the sample was developed for 45 seconds using AZ400K:DI H_2O (1:4). The developing time is determined when all the exposed photoresist is developed away. The sample was then rinsed with DI water and blown dry. Our measured photoresist thickness for Shipley 1818 spun at 5000 rpm was ~2.5μm.

The 2μm high cylindrical photoresist mesas served as an etch mask for cylindrical mesas 20μm to 36 μm in diameter formed by etching to a depth of 4.5μm into the bottom, *p*-type mirror using a load-locked, Trion Minilock II ICP dry-etching system. To control the etching depth, an optical interferometric monitor was designed and installed as shown in Figure 3.13 (dashed line). More information about how to operate the optical interferometric and the Trion Minilock II can be found at [11] and in Appendix A.

The optical interferometric monitor was designed based on the difference in reflectivity between the high and low aluminum layers of the epitaxial material. The laser beam hits the sample and is reflected to hit the photodiode surface, which in turn generates a photodiode current proportional to the reflected light, which is changing as the mirror layers are being etched. Using an analog-to-digital converter with a computer, the resulting changes in current are plotted with time. By counting peaks or valleys, the number of mirror periods etched can be known. Figure 3.14 (a) below shows the temporal in situ reflectance obtained during the etching of the VCSEL sample. Each period of reflectance oscillation corresponds to one pair of DBR mirrors. Different components of the VCSEL structure, such as the layers of the DBR mirrors and the optical cavity, can be identified in real time. Figure 3.14 (b) shows an SEM image for etched mesa after stripping the photoresist.



BCl_3 (sccm)	Cl_2 (sccm)	RIE power(W)	ICP power(W)	Pressure (mT)
40	10	50	300	7

Process parameters

Figure 3.13 Optical interferometric monitor (dashed line).

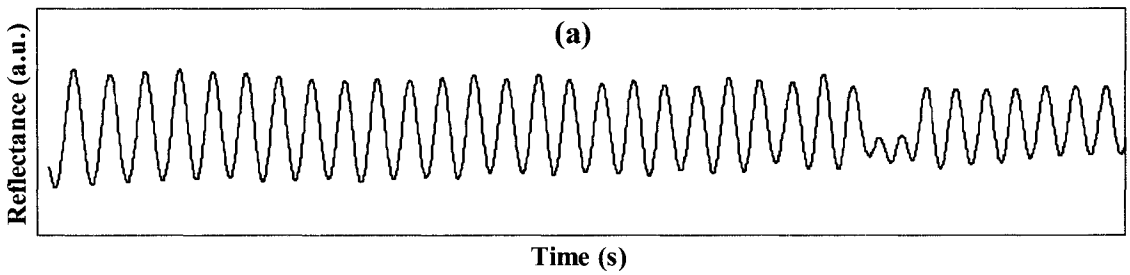


Figure 3.14 (a) Temporal in situ reflectance obtained during the etching of the VCSEL sample. (b) SEM image for an etched mesa after stripping the photoresist.

3.3.1.3 Wet oxidation

Wet oxidation was used to form the current aperture and provide lateral index guiding to the lasing mode.

Oxidation is used to convert high aluminum content $Al_{0.98}Ga_{0.02}As$ to aluminum oxide. It is carried out in a furnace using water vapor. The oxidation furnace is set up using a 6 cm diameter quartz tube inside a CARBOLITE tube furnace with electrical heating elements. Water vapor is provided by heating water, and the resulting vapor is carried through the furnace tube using N_2 with 30 sccm. The amount of water vapor that can be transferred in the N_2 stream is proportional to the water temperature. To achieve maximum water vapor into the N_2 stream, the water temperature is kept just below the boiling temperature (85-90)°C. N_2 will bubble through the water to bring the vapor into the furnace. The inlet tubing has to be heated using heat tape to prevent the condensation of vapor before entering the furnace [6]. The oxidation furnace apparatus is shown in Figure 3.15 below.

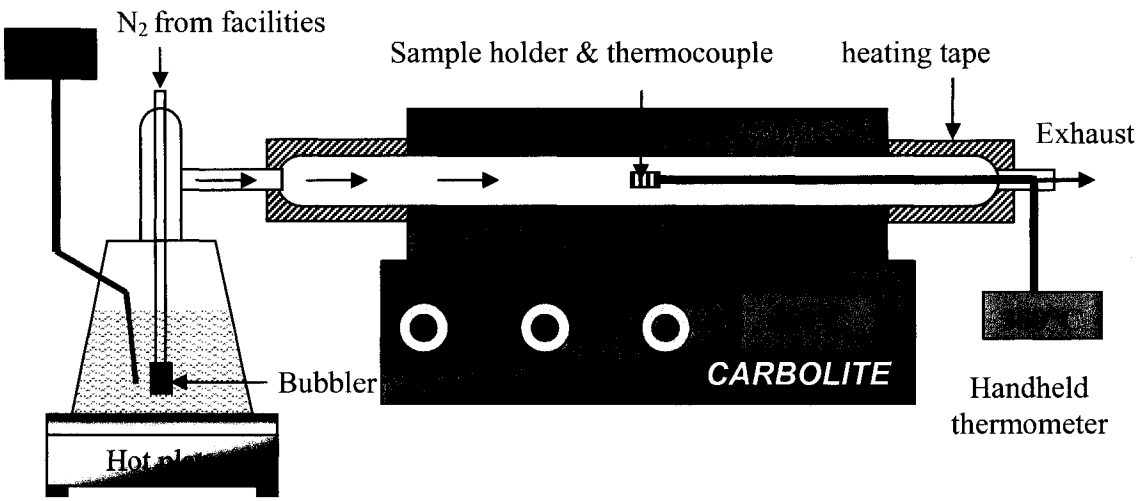
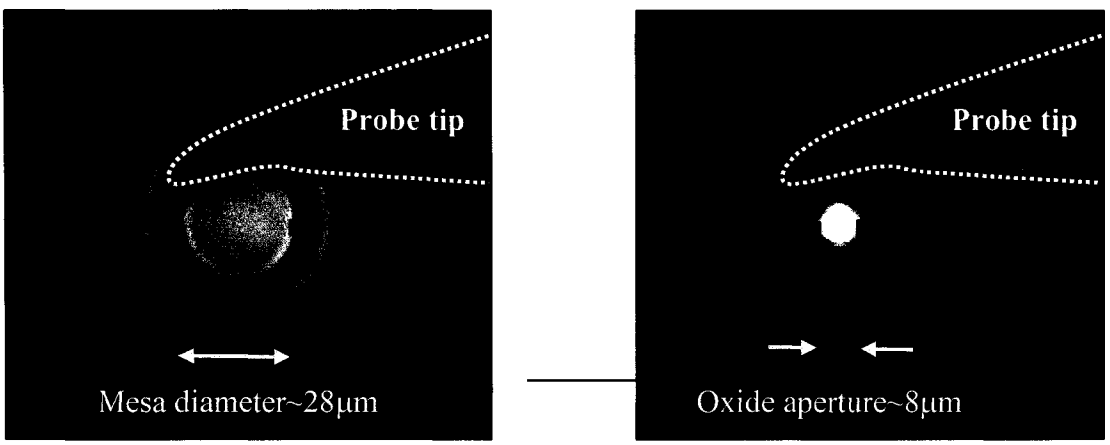


Figure 3.15 Wet oxidation setup using CARBOLITE tube furnace.

To investigate the oxidation rate, a calibration sample (usually from the same epitaxial material) was loaded into the furnace after letting the system stabilize for about 90 minutes. The calibration sample was oxidized in a 380°C steam environment for 10 minutes and then the sample was unloaded. Since the oxide aperture is not directly visible in the optical microscope, a 28μm mesa diameter from the test sample was probed, as shown in Figure 3.16 (a) and biased below threshold, as shown in Figure 3.16 (b) where the oxide aperture was estimated from the glowing area shown. (For more information about how to operate the CARBOLITE tube furnace, refer to [11].)



(a) (b)

Figure 3.16 An oxidized 28μm mesa diameter test sample (a) at zero bias. (b) Biased below threshold showing an oxide aperture of 10μm.

Another, and more accurate, way to estimate the oxidation length is to cleave the calibration sample and use a scanning electron microscope (SEM) to measure the oxidation length, as shown in Figure 3.17. This resulted in about 10μm oxidation length at a rate of 1μm/minute. The real sample went through the same process and resulted in a 9μm oxidation length extending from the edge of the mesas.

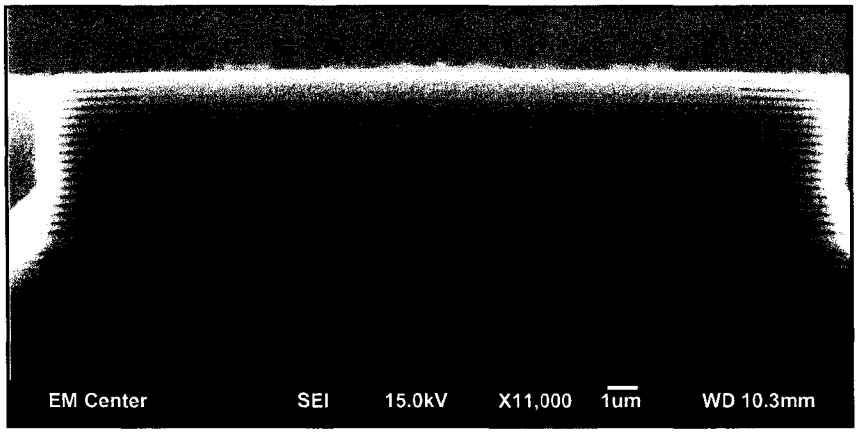


Figure 3.17 SEM image of a cleaved mesa showing the DBRs and the oxidized layers.

3.3.1.4 Top Contact

The specific contact resistance is defined as the contact resistance of a unit area for current flow perpendicular to the contact and is typically stated in units of Ω-cm^2. Ideally, the contact resistance should be very small, in the range of (10^{-5}-10^{-7}) Ω-cm^2, and the contact should have a linear I-V curve. Two different types of contacts present in the VCSEL structure are *n*-contacts and *p*-contacts. Whether one uses one or the other depends on whether the semiconductor surface is an *n*-type or a *p*-type.

Ohmic contacts are fabricated by evaporating different types of metals of certain thicknesses on the semiconductor surface. Before the contact can be used as an ohmic contact, the wafer (GaAs) must be heated until the deposited metal alloys into the semiconductor layer underneath the contact. During this process, a component of the metal enters the GaAs and highly dopes the surface. Nominal metal types for this doping function are Zn, Be, Cd and Mg for *p*-type GaAs and Ge, Se, Sn, and Si for *n*-type GaAs [10].

To get the over hanging resist profile for the small aperture sizes and to avoid the use of chlorobenzene [3], lift off resist (LOR-10B) which is based on the PMGI

(polydimethylglutarimide) platform was used. LOR-10B is suited for lift-off processes, as finely tuned undercuts can be obtained by changing the baking temperature.

The sample was cleaned using acetone, methanol, and de-ionized (DI) water and blown-dry with N_2. Next, the sample was baked at 120°C for two minutes and left to cool down for about three minutes.

After cleaning the sample, LOR-10B was spun at 3600rpm for 30 seconds and baked for 5 minutes at 180°C, following the data provided by the manufacturer [12]. Next, the LOR-10B edge-bead was removed using a sharp blade. Photoresist (Shipley 1818) was then applied. Next, the sample was spun at approximately 5000 rpm for 30 seconds. Next, using the mask aligner, the top contact photomask was aligned and UV-exposed for 11 sec. at 15mW/cm^2. Next, the sample was developed for 45 seconds using AZ400K: DI H_2O (1:4). After the sample was inspected, it was soaked for 15 seconds in an HCl: H_2O solution with a 1:1 ratio to remove any oxide layer formed on the contact region during the oxidation process since the presence of oxide underneath the contacts will result in high-resistance ohmic contacts, which will affect the VCSEL performance. After that, the sample was blown dry with N_2 and immediately loaded into the E-beam evaporator. After closing the bell jar, the pressure inside the evaporator was pumped down to ~$2x10^{-6}$ Torr.

Gold-germanium is usually used for *n*-type GaAs ohmic contacts with an overlay of another metal such as nickel or silver [3]. The nickel is introduced as a wetting agent and to prevent AuGe metal from "balling up". The germanium is used for doping the GaAs during alloying.

An Au-Ge-Ni-Au sequence of metals was chosen for the top n-type contact. The ratio of the lower Au and Ge layer thickness was chosen as 88% Au and 12% Ge percent by weight to make it a eutectic mixture. The total AuGe thickness was chosen to be 1000Å since ohmic contact resistance will suffer if the contact thickness is less than 1000Å [3]. As a result, the Au thickness was 670Å, while the Ge thickness was 330Å. The nickel layer thickness to be evaporated is approximately 200Å for each 1000Å of AuGe.

Au-Ge-Ni-Au was evaporated with thicknesses of (670:330:200:500)Å, respectively. The last layer of 500 Å Au was added to enhance the sheet resistance and make it easier to probe the device [3]. (For more information about how to operate the e-beam evaporator, refer to the standard online clean room operation manual [11] or [13: Appendix A].) After lift-off, the LOR-10B layer was removed using MICROPOSIT REMOVER 1165, which is a mixture of pure organic solvents specifically formulated for use in applications where the photoresist has seen high temperatures, strong etchants, or other harsh processing conditions. Figure 3.18 below is an SEM image of the mesa after lift-off showing the annular *n*-type contact on top of the mesa.

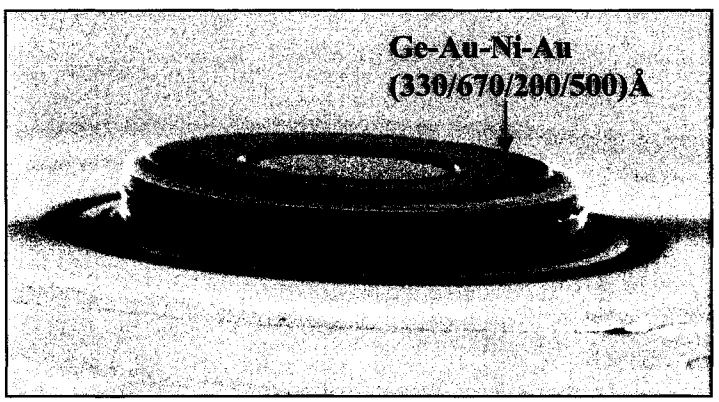


Figure 3.18 SEM image of the mesa with the annular n-type contact on top of the mesa.

3.3.1.5 Bottom contact

The process for applying the bottom contact is very similar to that used for applying the top contact with few modifications. After cleaning the sample, LOR-10B was spun at 2500rpm for 30 seconds and baked for 5 minutes at 180°C. Next, the LOR-10B edge-bead was removed using a sharp blade. Photoresist (AZ4400) was then applied. After the photoresist was put on the sample, the sample was spun at approximately 4000 rpm for 30 seconds. The measured photoresist thickness for AZ4400 spun at 4000 rpm was 4μm. Next, using the mask aligner, the bottom contact photomask, which is shown in Figure 3.19 (blue), was aligned with the sample and the sample was UV-exposed for 25 sec. at 10mW/cm^2. Next, the sample was developed using AZ400K: DI H_2O (1:4). The sample was then rinsed with DI water and blown dry. After inspection, the sample was prepared for metal evaporation through the same steps used for the top contact.

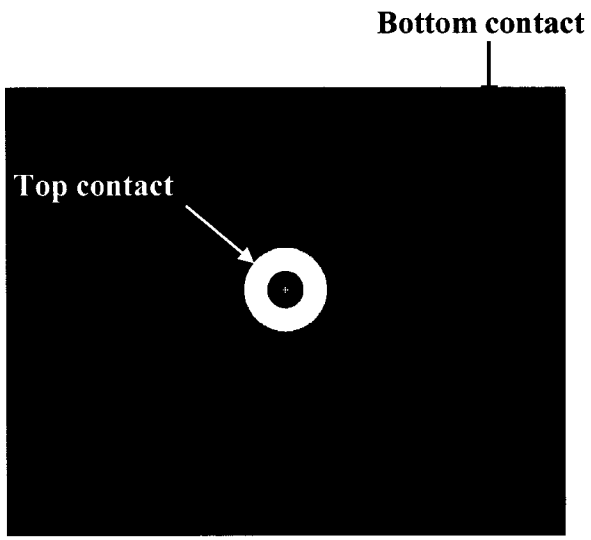


Figure 3.19 Bottom contact photomask (blue) imposed on the top contact mask (yellow).

Different types of metalizations can be used for *p*-type contact including BeAu-Ti-Au, Ti-Pt-Au and ZnAu-Ti-Au. For the VCSEL polarity presented here, Ti-Pt-Au metalization system cannot be used since the *p*-type layer that our contact will be deposited on is not highly-doped. Consequently, Be or Zn must be used. Using Zn is not recommended since it will contaminate the evaporation system. BeAu-Ti-Au was chosen as our bottom-contact metalization. BeAu was applied as a pre-alloyed metal with (1% Be by weight) [3]. Be was used to highly dope the surface layer.

BeAu-Ti-Au was evaporated with corresponding thicknesses of (500:200:700) Å after the sample was soaked for 15 seconds in an HCl: H_2O solution with a 1:1 ratio to remove any oxide layer formed on the contact region. Next, the sample went through the lift-off process using the same recipe used for top contact lift-off. The sample was alloyed at 420 °C for 30 seconds. Figure 3.20 shows a microscopic top view image of a mesa with alloyed top and bottom contacts.

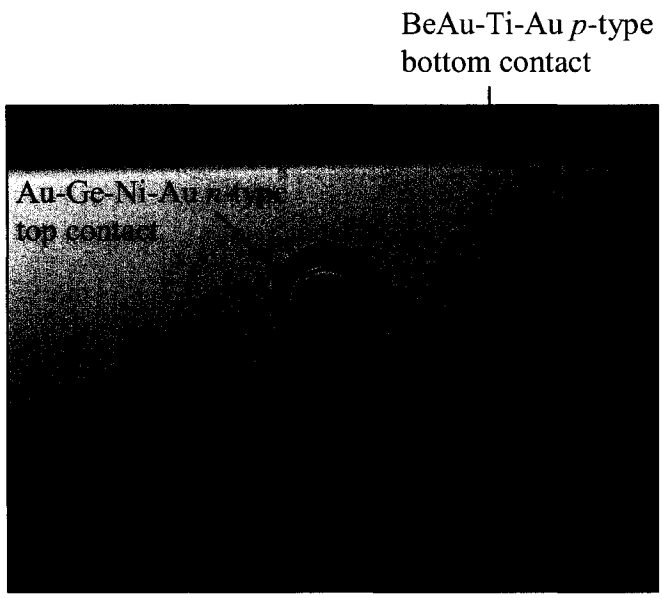


Figure 3.20 Microscopic top view image of a mesa with alloyed top and bottom contacts.

3.3.1.6 Mesa sidewall insulation (SiN_x)

After contact formation, a thin layer of silicon nitride (SiN_x) needs to be deposited and partially etched to electrically insulate the mesa sidewall from later metallic. 1000 Å of SiN_x was deposited all over the sample. Photoresist (Shipley 1818) was then applied. The sample was spun at approximately 5000 rpm for 30 seconds. Next, using the mask aligner, the silicon nitride photomask, which is shown in Figure 3.21 (green) and superimposed on the top and bottom contact photomasks (yellow and blue), was aligned with the sample and the sample was UV-exposed for about 11 sec. at 15mW/cm^2. Next, the sample was developed for 45 seconds using AZ400K. After rinsing with DI water and being blown-dry, the sample was baked for 2 minutes at 95°C to reduce the resist etching rate. The nitride was etched in the Technics Micro-RIE System using CF_4:O_2 with (30: 6) sccm flow for 45 seconds at 100W power. Next, the photoresist was striped. Figure 3.22 shows a SEM image of the device at this stage after nitride etching and photoresist stripping. (For more information about how to operate the Technics Micro-RIE System, refer to [11].)

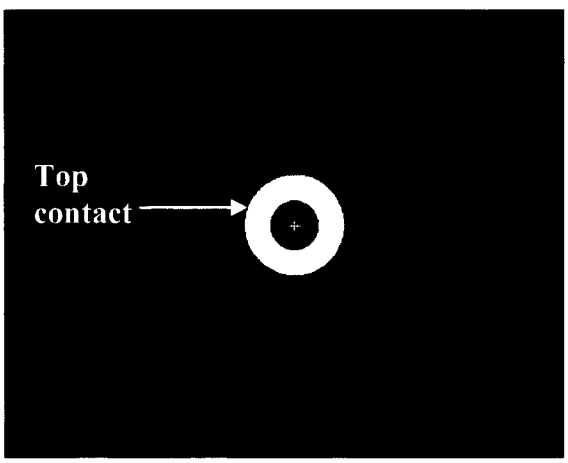


Figure 3.21 Silicon nitride (SiN_x) photomask (green) imposed on the top and bottom contacts masks (yellow and blue). Dummy mesas are not shown.

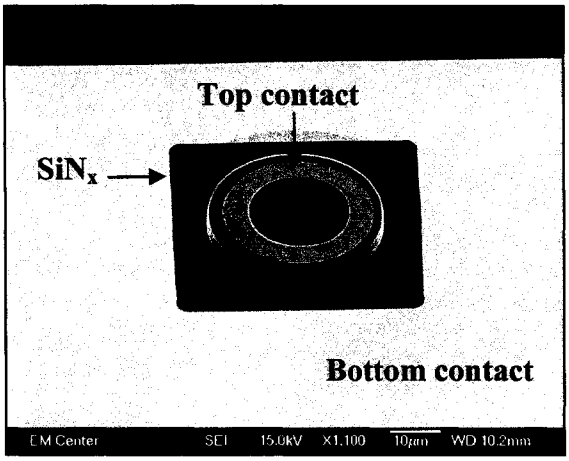


Figure 3.22 SEM image of the VCSEL mesa after nitride etching and photoresist striping.

3.3.1.7 Planarization

Polyimides are typically applied in semiconductor micro-fabrication for use as stress buffers, for surface planarization, or as dielectric isolation layers [14,15]. Many factors should be considered in the combination of polymers and metals. The dielectric constant is an important factor in choosing the polymer since a low dielectric constant will result in a smaller RC time constant and, consequently, faster devices. Also, the polymer should have low moisture absorption so that it has stable properties. In addition, low curing temperature is important if the sample is sensitive to high temperatures. Good adhesion properties to metals such as gold are important factors that also need to be considered [14, 15].

Polyimide is used to planarize the VCSEL before depositing metal interconnects and bonding pads. An HD-8000 positive tone photosensitive polyimide was chosen. The key advantages of HD-8000 polyimides are: HD-8000 is a positive tone polyimide that is compatible with our photomask; it contains a built-in adhesion promoter; it can be directly exposed without needing an additional photoresist layer for patterning; it is

developed with positive photoresist developer; it is cured in only 90 minutes and provides a cured film thickness in the range of (5-12) μm; and it offers high resolution, good room temperature viscosity stability, and a low dielectric constant (~3.4 at 1 kHz) after curing.

Before incorporating the HD-8000 polyimide directly in VCSEL fabrication, its profile on a dummy GaAs sample was investigated. The real VCSEL sample was processed as follows: First, the sample was cleaned. Next, HD-8000 was applied and spun at approximately 5000 rpm for 30 seconds and then the sample was baked for 100 seconds at 115°C. Next, using the mask aligner, the polyimide photomask illustrated in Figure 3.23 (pink), was aligned with the sample and the sample was UV-exposed for about 25 sec. at 10mW/cm^2. The sample was then developed using the AZ400K: DI H_2O (1:4). Next, the sample was rinsed by squirting it with DI water while it was spun at 1000 rpm for ten seconds. Immediately after the rinse, while the sample was still on the spinner, it was spin-dried at 3500rpm for ten seconds to make sure that the developed polyimide was cleaned.

After developing, the sample was inspected using both the microscope camera and the Alpha-Step surface profilometer. Next, the sample must pass through the curing process, in which the sample temperature is raised to a certain value for a specific time. The objectives of the curing process are to remove the residual solvents, to remove all cross-links, and to complete the imidization and the adhesion processes. Since all four events occur together at a given temperature, the cure schedule is a very important step that impacts the cured film quality and associated mechanical properties. Many variables need to be considered in curing polyimide films, such as the curing furnace, atmosphere,

loading temperature, ramp rate, soaks (holding temperatures), final cure temperature, and ramp-down [16]. Curing should be carried out in a nitrogen atmosphere.

The real VCSEL sample was loaded with the following curing schedule: the sample was loaded into furnace at 20°C, and the temperature was ramped from 20°C to 350°C over a 60-minute period. After that, the temperature was held at 350°C for 30 minutes. Finally, the sample was unloaded immediately or allowed to cool down in the furnace. Figure 3.24 below shows an SEM photo of the mesa after curing the polyimide. Measured cured polyimide thickness was about 5μm. (More information about how to operate the Polyimide curing furnace is available at [11].)

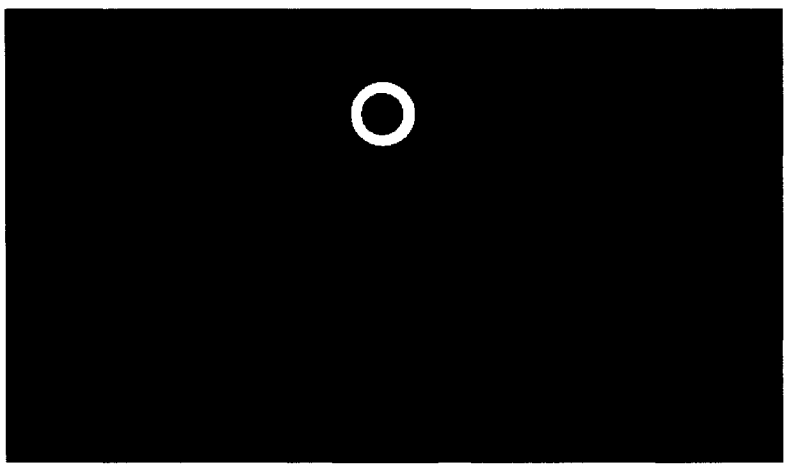


Figure 3.23 Polyimide (pink), SiN_x (green), top contact (yellow), and bottom contact (blue) photomasks. Dummy mesas are not shown.

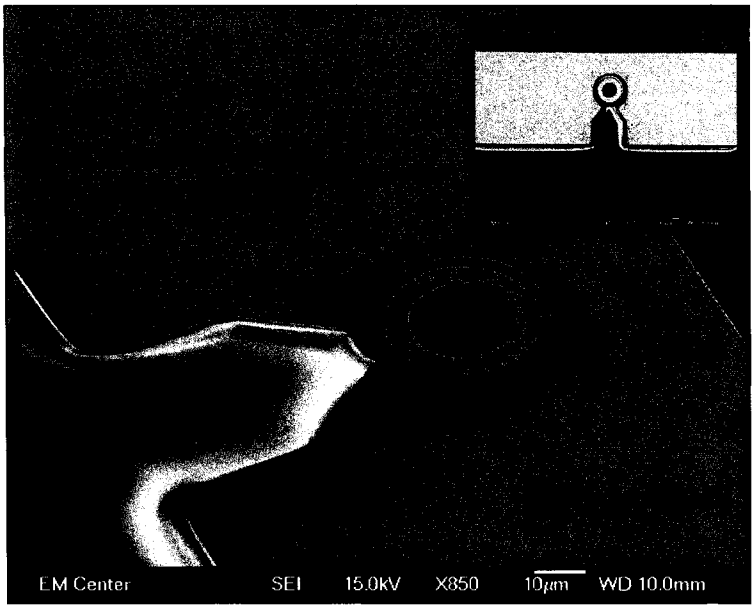


Figure 3.24 SEM image of the sample after polyimide curing.

3.3.1.8 Electroplated metal interconnects

Metal interconnects and bonding pads are probing pads that allow for electrical connection to the VCSEL. For example, probe station tips can be placed on probe pads so that current can pass through the VCSEL. Copper was used as the electroplated metal due to its higher thermal conductivity (4.01W/cm-K) and lower cost (~$100) compared to gold (3.17W/cm-K, ~$1000). The copper electroplating process uses an ionic solution of copper to deposit copper atoms onto a pre-existing conducting surface. Since the plating process depends on passing current through the surface to be plated, the sample must have some electrical contact to an external current source. This is accomplished using a probe that contacts the seed layer on the sample, which is then suspended in the Cu plating solution and forms the primary electrode. The other electrode is a platinized niobium mesh that encloses the primary electrode while it is in the plating solution. Current is then forced from one electrode to the other through the solution to accomplish the copper deposition.

Depositing pad and interconnect metal proceeds with the following steps: After cleaning the sample, Lift-off resist LOR-10B and positive tone Shipley 1818 photoresist were spun on the sample as described in Section 3.3.1.4. The sample was then aligned and UV-exposed using the interconnect photomask shown in Figure 3.25 (orange). Next, the sample was developed and the 1818 photoresist was stripped, leaving the LOR-10B to protect the lasers' facets from being exposed to chemical etchant used later in the process to etch back the seed layer and from possible argon gas sputtering. Figure 3.26 shows the device under fabrication at this point of the process. Ti-Cu with thicknesses of (200:800) Å was evaporated on the sample using a planetary stage with tilting angles range from 50 to -50 degrees in 2 degree steps to ensure good step coverage. Next, the sample went through a second photolithography process using AZ4400 photoresist, as described earlier in preparation for the copper electroplating step.

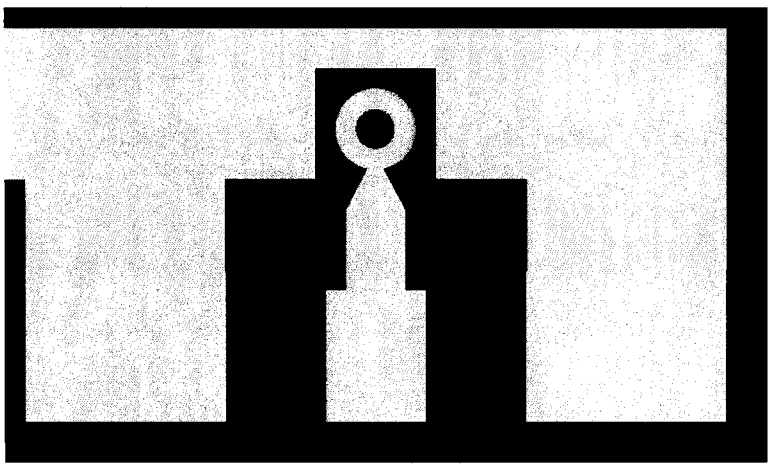


Figure 3.25 Cu-electroplating mask (orange).

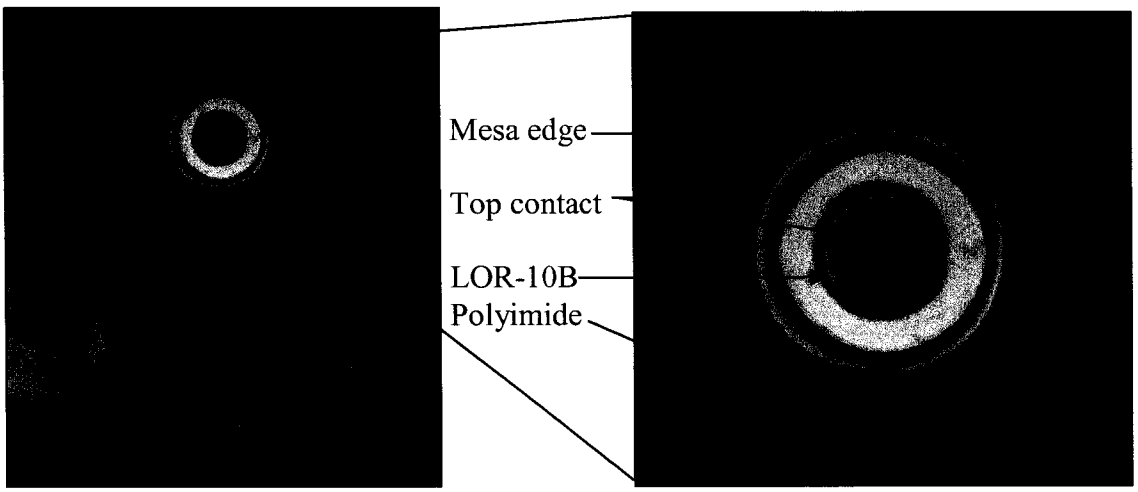


Figure 3.26 Microscope top view image of the device under fabrication with the aperture covered with LOR-10B.

The sample was then aligned and UV-exposed a second time using AZ4400 photoresist and the interconnect photomask shown in Figure 3.25 (orange). Next, the sample was developed. The first electroplating setup used is shown in Figure 3.27. It consists of a temperature controller and a water pump unit to warm up the Cu P RTU electroplating solution supplied by Technic Inc. to about 52°C. A four-point probe apparatus probed the sample at the exposed corners of the seed layer area, a slab of copper was used as the anode, and a pulse current source (DYNATRONIX). (For more information about how to operate the DYNATRONIX current source refer to [11].)

The current density and duty cycle were set to about 56kA/cm^2 (plated area) and 10%, respectively. The sample was electroplated for 10 minutes at 0.2μm/minutes. After unloading the sample, the photoresist was stripped using acetone. The seed layer was removed by wet etching in the Cu etchant and in the HF etchant (this removes the Ti) for 5 seconds. Figure 3.28 shows a SEM photo of a VCSEL ready for testing where the mesa and the metal pad are electroplated with copper.

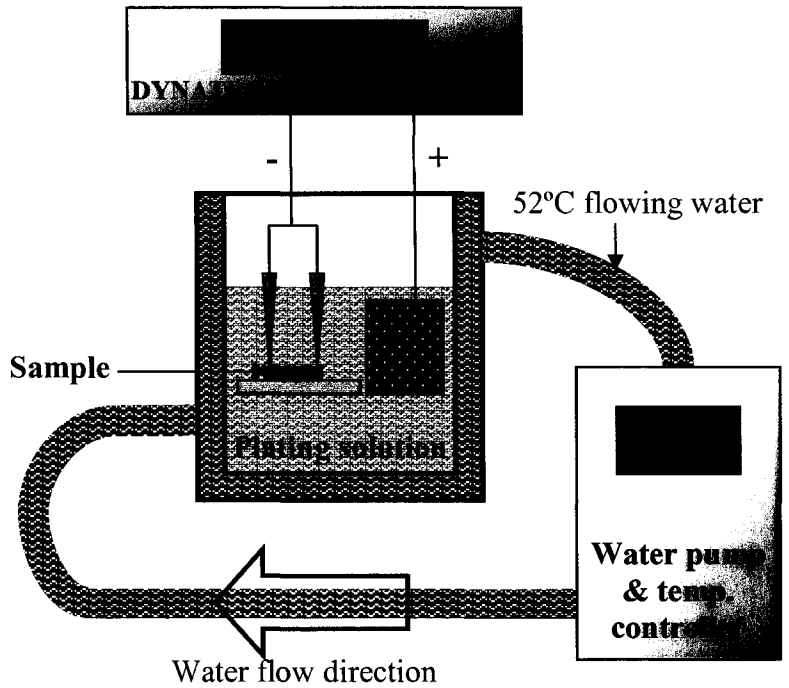


Figure 3.27 Copper electroplating setup.

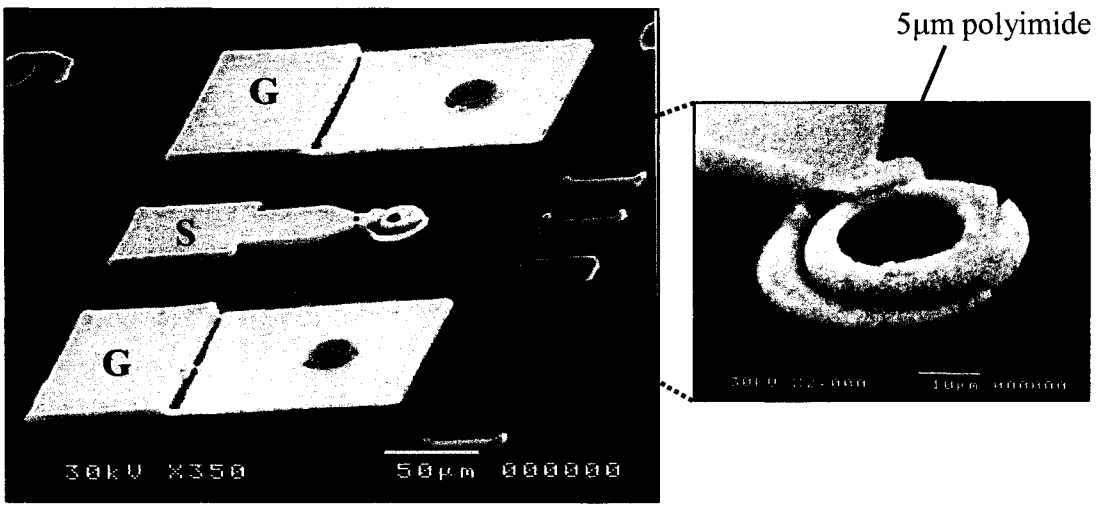


Figure 3.28 SEM image of a VCSEL where the mesa and the metal pad are electroplated with copper.

From the SEM images, the quality of the electroplated copper needs to be investigated in terms of the plated Cu density and plated Cu adhesion to the seed layer as shown in Figures 3.28 and 3.29, respectively.

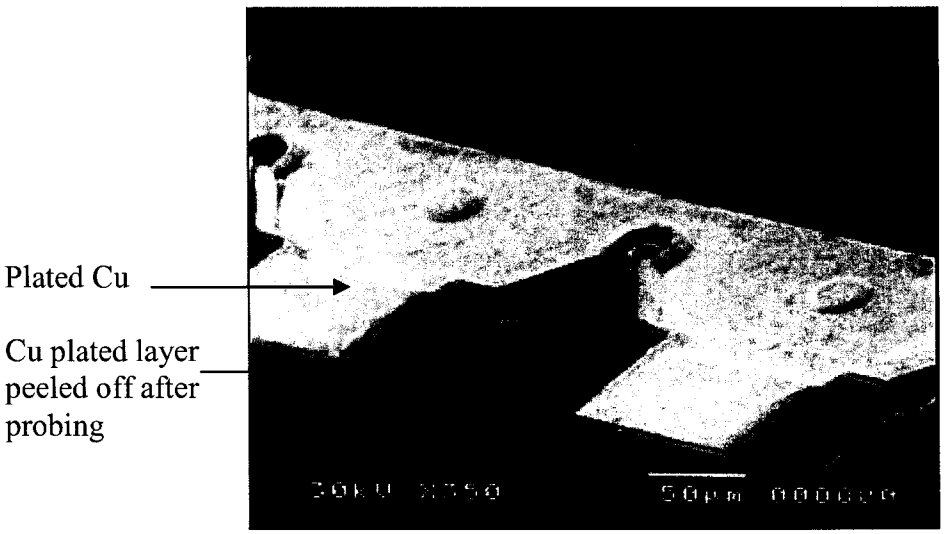


Figure 3.29 SEM image showing a device after testing, where Cu plated layer peeled off the signal pad after probing.

A closer look to the quality of the current Cu electroplated layer shown in the inset of Figure 3.28 shows a low-density Cu-plated layer, which will not be as good a heat sink as a higher-density Cu-plated layer. Furthermore, during device testing, it was noticed that the plated Cu does not stick to the seed layer in some places, as illustrated in Figure 3.29.

The plated layer roughness and density might be due to the current density values used. As for the seed layer, it might have an oxide layer that results in weak adhesion. To solve those two problems, a different electroplating setup with a different plating bath that worked at room temperature was used.

After protecting the aperture with LOR-10B, depositing the Ti-Au seed layer, and patterning the AZ4400 photoresist using the interconnect photo mask, the sample was loaded into the new electroplating setup shown in Figure 3.31. The current density was set at about 18kA/cm^2 based on the plated area of the sample and the duty cycle was set to 20%. The sample was electroplated using Cu FB RTU electroplating solution supplied by Technic Inc. at room temperature for 20 minutes at 0.15μm/minutes. After unloading the sample, the photoresist was stripped using acetone. Although the Ti and Au parts of the seed layer can be etched easily using Au etchant and HF, respectively, this step will also etch and degrade the electroplated Cu. So the seed layer was sputtered off the sample using the ICP and argon gas (ICP=50W, RIE=100W, pressure=7mTorr, Ar flow=15sccm). Next, the LOR-10B, which was used to protect the devices apertures, is stripped using the resist remover 1165. Figure 3.32 shows an SEM photo of a VCSEL ready for testing where the mesa and the metal pad are electroplated with copper.

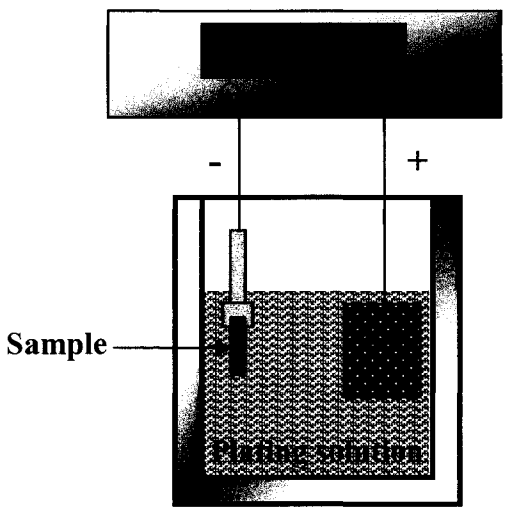


Figure 3.31 Copper electroplating setup.

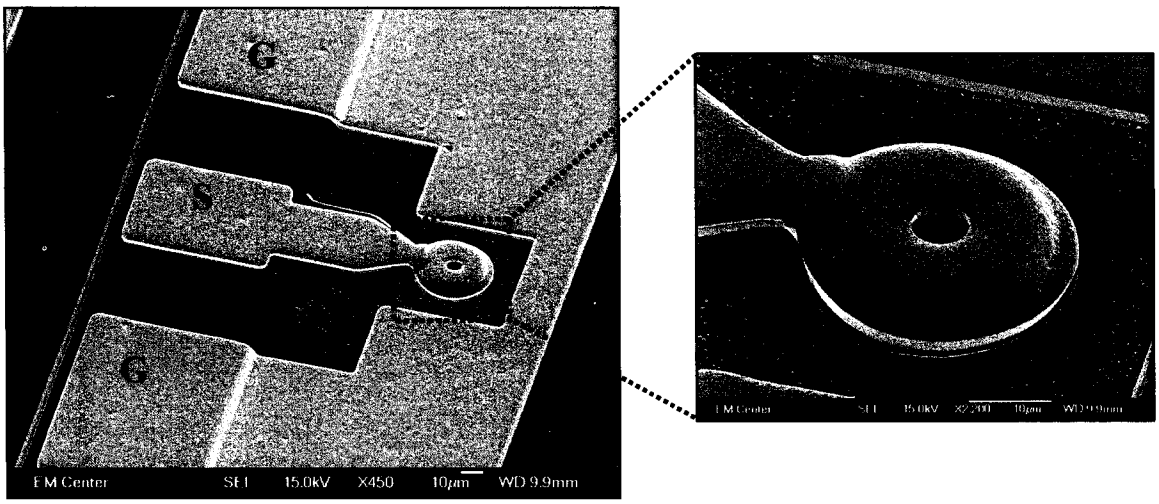


Figure 3.32 SEM image of Cu-plated VCSEL at the completion of fabrication.

3.3.2 Fabrication of top-emitting high-speed self aligned 850nm VCSELs

The top-emitting high-speed self-aligned 850nm VCSELs were fabricated using the same epitaxial structure described in Section 3.3.1.1.

3.3.2.1 Self-aligned top contact

To apply the top contacts, the sample went through the same general fabrication steps and mask described in Section 3.3.1.4 Figure 3.33 below shows the photoresist mask ready for the top contact metal deposition.

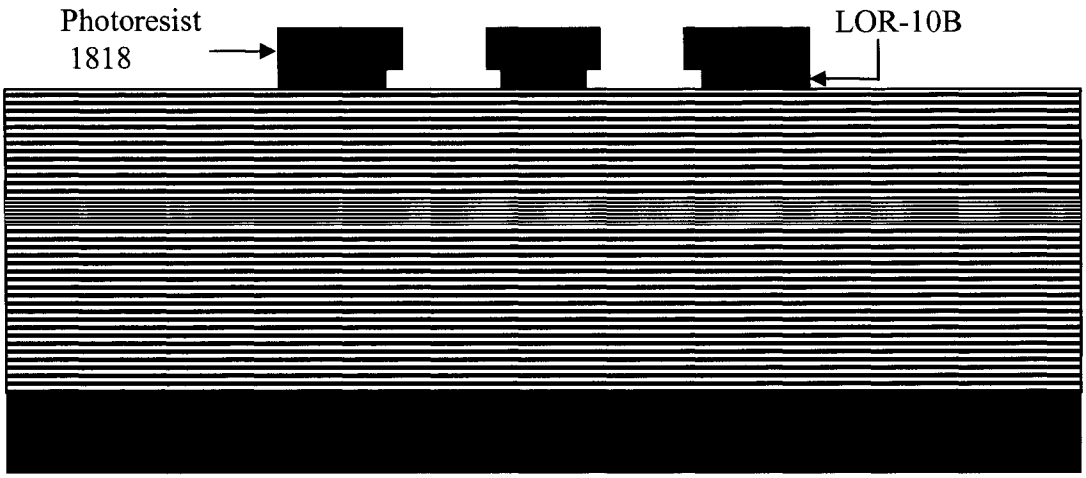


Figure 3.33 Photoresist mask for top contact.

Since the top contact needs to pass through the etching and oxidation processes described in Sections 3.3.1.2 and 3.3.1.3 respectively, it is important to use a metal contact system that is dry etching resistant, thermally stable, and wet oxidation resistant. Due to its thermal stability [17] and dry etching and wet oxidation resistance, Pd-Ge-Ti-Pt was evaporated with thicknesses of (500/1000/250/300)Å, respectively, to form the annular *n*-type top contact. After lift-off, contact was alloyed for 30 seconds at 450°C. Figure 3.34 below illustrates a top view of the sample after lift-off ready for mesa etching.

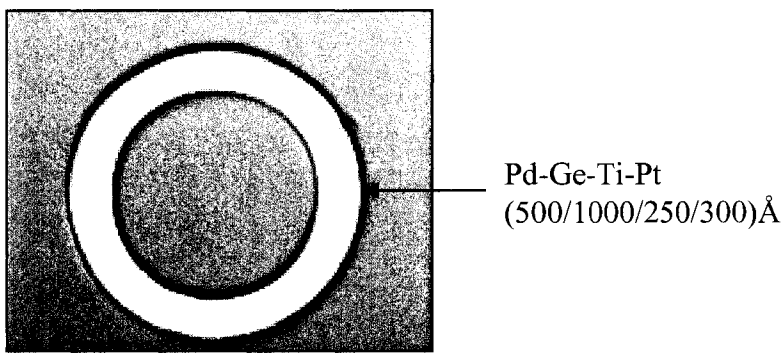


Figure 3.34 Top view of the sample after lift-off showing the annular top contact.

3.3.2.2 Mesa etch

After contact formation, the contact and a smaller diameter 1818 photoresist feature protecting the aperture served as an etch mask for cylindrical mesas 18 to 28 μm in diameter formed by etching to a depth of 5μm into the bottom, *p*-type mirror using the load-locked, TRION ICP dry-etching system. As shown in Figure 3.35, the use of the contact to define the outer perimeter of the mesa etch mask results in a device mesa that is self-aligned to the contact. The self-aligned process allowed smaller mesa diameters for a given aperture size, thus decreasing the distance for heat flow to the sidewall as well as mesa capacitance. The self-aligned process also increased the alignment tolerance to about 4μm, as illustrated in Figure 3.36. The sample was etched using the same setup and parameters described in Section 3.3.1.2. Figure 3.37 shows an SEM image for etched mesa after stripping the photoresist protecting the aperture shown in Figures 3.35 and 3.36.

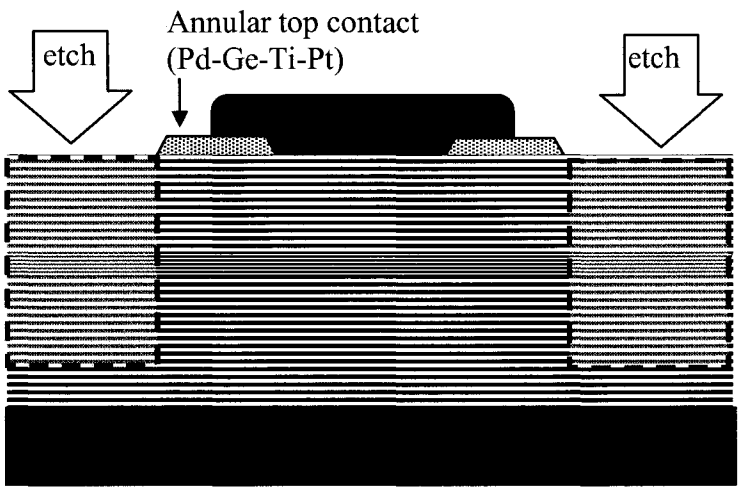


Figure 3.35 The Pd-Ge-Ti-Pt top contact and a smaller diameter 1818 photoresist feature protecting the aperture served as an etch mask for cylindrical mesas.

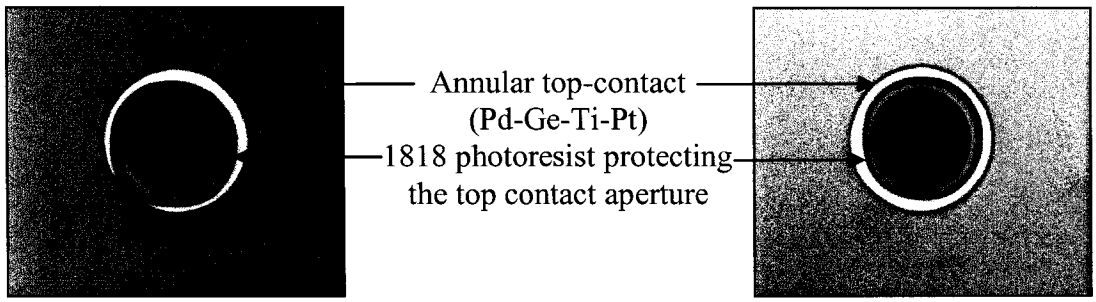


Figure 3.36 Top views of the top contact and a smaller-diameter photoresist protecting the aperture ready for mesa etching.

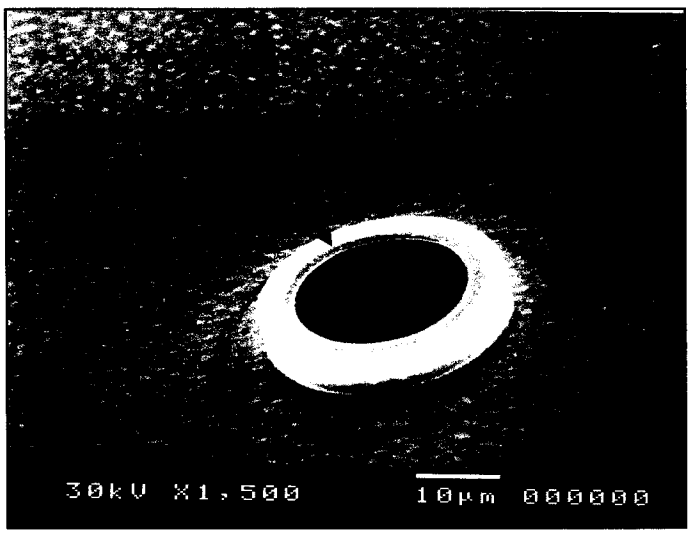


Figure 3.37 SEM image for etched mesa after stripping the photoresist protecting the aperture shown in Figure 3.36.

3.3.2.3 Wet oxidation

Using the same setup described in Section 3.3.1.3 and shown in Figure 3.15, the sample was oxidized at 380°C for 10 minutes resulting in a 4µm oxide extending from the edges of the different mesas sizes.

3.3.2.4 Bottom contact, nitride, polyimide and plating

After oxidation the sample went through the same processes, types of chemicals, and metals described in Sections 3.3.1.5, 3.3.1.6, 3.3.1.7, and 3.3.1.8, respectively.

3.3.3 Fabrication of 980nm high-speed top-emitting non self aligned VCSELs

Top-emitting, non-self-aligned 980nm VCSELs were fabricated on an *n*-type substrate. The sample was fabricated using the same procedure used to fabricate the 850nm non-self-aligned VCSELs described in Section 3.3.1 and its subsections. The only change was the types of metals used to form the top and bottom contact since the 850nm samples were grown on a *p*-type substrate while the 980nm sample was grown on an *n*-type substrate. Ti-Au was evaporated with thicknesses of (200/1500) Å, respectively, to form the annular *p*-type top contact. For the bottom *n*-type contact, Ge-Au-Ni-Au was evaporated with thicknesses of (330/670/200/1000) Å, respectively.

3.3.4 Fabrication of 980nm high-speed top-emitting self-aligned VCSELs

A sample was fabricated using the same procedure used to fabricate the 850nm self-aligned VCSELs described in Section 3.3.2 and its subsections. Ti-Pd-Ti-Au-Ti-Pd was evaporated with thicknesses of (200/500//200/1000/200/1000) Å, respectively, to form the annular *p*-type top contact. For the bottom *n*-type contact, Ge-Au-Ni-Au was evaporated with thicknesses of (330/670/200/1000) Å, respectively.

3.4 Process overview for oxide confined bottom-emitting flip-chip bonded VCSEL fabrication

This section summarizes the fabrication process for bottom-emitting flip-chip bonded VCSELs.

3.4.1 Epitaxial growth

The wafers with epitaxial material used for fabricating 980nm bottom emitting devices were supplied by Novalux Inc. Figure 3.1 represents the general structure of the grown wafer that was used in this process. More details about the various structures will be presented later in this chapter. Only the non-self-aligned approach was used to fabricate the bottom-emitting devices since the self-aligned process for bottom-emitting devices was not developed yet.

3.4.2 Bottom-emitting non-self-aligned flip-chip bonded 980nm VCSEL fabrication

Initially, the bottom-emitting VCSELs fabrication process went through the same fabrication steps used to fabricate the top-emitting VCSELs described in Sections 3.2.2.1 through Section 3.2.2.4, except the mask layouts used are different from those used for the top-emitting devices. Figure 3.38 represents the bottom-emitting VCSEL after bottom contact deposition. As illustrated in the figure, the device mesa has a solid circular top contact. In other words, the top contact has no aperture for the emitted light to be transmitted through compared to the top-emitting structure. Besides, it is very important to have good metal step coverage between the dummy mesas top side and the bottom (substrate) contact to planarize the device signal and ground contacts. Furthermore, the device at this point has no coplanar waveguide for high-speed testing and no heat sinking. To overcome these issues, a heat-spreading substrate with coplanar waveguide probe pads must be fabricated, and the structure shown in Figure 3.38 will be flipped and bonded to the VCSEL chip as will be discussed later.

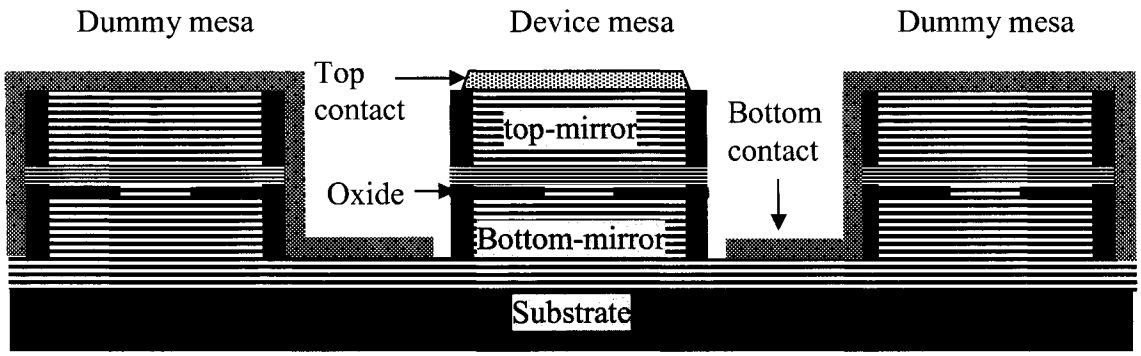


Figure 3.38 Mesa after applying the bottom contacts.

3.4.3 Heat spreader

The heat spreaders should be designed to allow devices to be individually DC and AC tested. The spreader's material should have a coefficientt of thermal expansion (CTE) as close as possible to the device chip, in order to minimize the strain on the solder joint. Plated copper was used for its good thermal conductivity and CTE match between the VCSEL die and the heat spreader substrate while plated indium was utilized for the bonding process.

To fabricate the heat spreaders, a seed layer of metal (~1000Å) was deposited on the entire sample. After deposition, a photolithography process is needed to pattern the areas for electroplating. Next, the sample was electroplated using the same setup described in Section 3.3.1.8. After electroplating the required metal thicknesses, the photoresist layer was stripped, the seed layer was etched or sputtered and finally, the sample went through a reflow process to improve the plated layers uniformity and smoothness. Figure 3.39 illustrates a heat spreader after seed layer removal ready for flip-chip bonding.

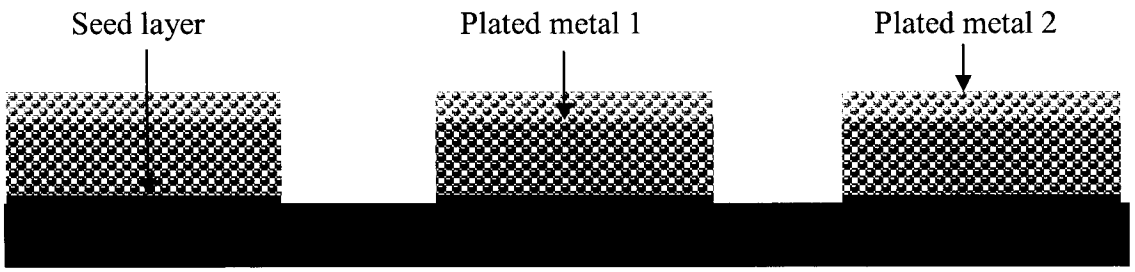


Figure 3.39 Heat spreader ready for flip-chip bonding.

3.4.4 Flip-chip bonding

At this point, the VCSEL die shown in Figure 3.38 needs to be flipped, aligned, and placed to be bonded to the heat spreader shown in Figure 3.39 by melting the In layer. This step was carried out using the PICO flip-chip bonder, which enables picking up a VCSEL die, aligning it with the heat spreader, and placing it on top of the heat spreader while applying a specific force. The alignment mechanism of the flip-chip bonder is based on the principle of imaging two orthogonal images simultaneously into one common image plane, using a stationary beam splitter and a single beam deflection. A more detailed discussion of the flip-chip bonder setup and the bonding process will be presented later in this chapter. Figure 3.40 below shows the VCSEL die flipped and bonded on top of the heat spreader substrate. The final step of the process is to ensure good wetting and bonding between the In layer and the top contact metals. This is done by reflowing the In layer according to a certain temperature profile in N_2.

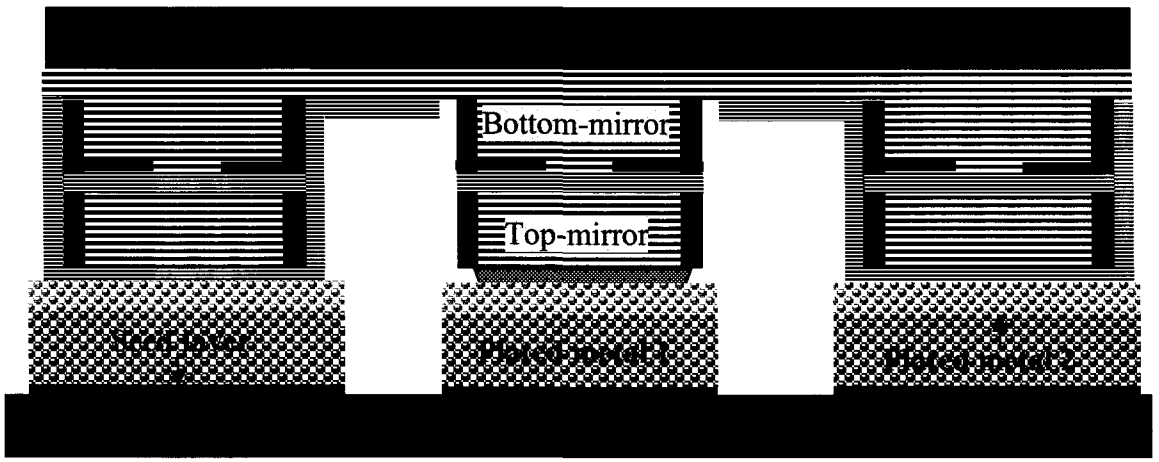


Figure 3.40 Devices chip flipped and bonded on top of the heat spreader substrate.

3.5 Bottom-emitting flip-chip bonded VCSEL fabrication (1st generation)

3.5.1 Epitaxial growth

Three 980nm bottom-emitting wafers were supplied by Novalux Inc.: 8.53, 8.54 and 8.55. All three of the structures have 32 top mirrors and 6 quantum wells and 19, 20, and 15 bottom mirrors, respectively. After initial testing, it was determined that none of the structures provided have a single high Al contents layer. So, only one structure was chosen to proceed with and that was structure number 8.54.

3.5.2 Bottom-emitting non-self -aligned flip-chip bonded 980nm VCSEL fabrication

The bottom-emitting VCSELs fabrication process began with mesa etching (see Sec. 3.2.2.1). Next, the sample was wet-oxidized for 4 minutes at 380°C with water vapor temperature of 90°C and N_2 flow of 30sccm using the CARBOLITE tube furnace. The oxidation rate was 0.75um/minute, resulting in 3μm of oxide extending from the mesa sidewalls (see Sec. 3.2.2.2). To form the top *p*-type contact, Ti-Au was evaporated with thicknesses of (200:1500)Å (see Section 3.2.2.3). Au-Ge-Ni-Au was evaporated with

thicknesses of (330/670/200/500)Å for the bottom *n*-type contact (see Section 3.2.2.4). Figure 3.41 shows an SEM image of the bottom-emitting VCSEL die after bottom-contact deposition.

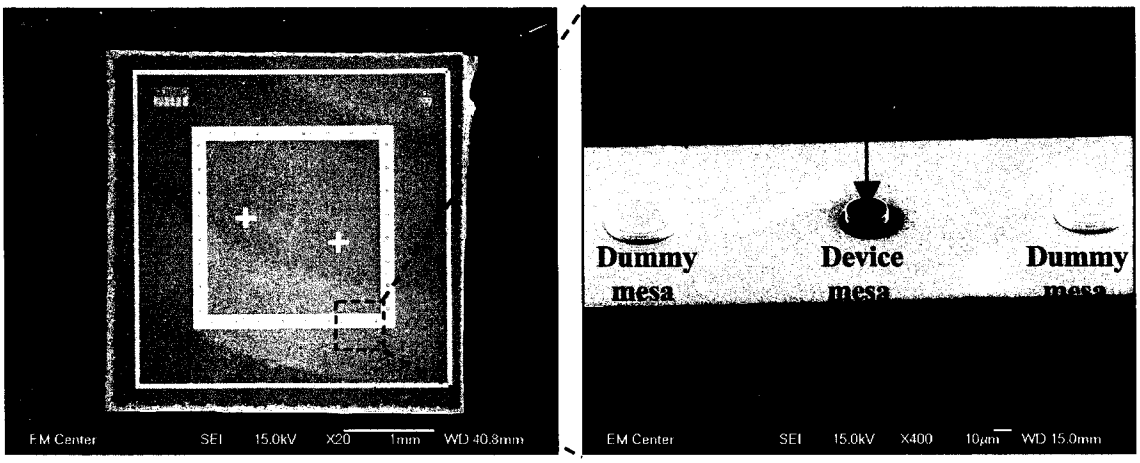


Figure 3.41 SEM image of the VCSEL die before flipping and bonding to the heat spreader.

3.5.3 Heat spreader

To minimize the strain on the solder joint, a semi-insulating GaAs wafer was used for the heat spreader due to the CTE match between the VCSEL die and the heat spreader substrate.

After cleaning with solvents, a semi-insulating GaAs sample was blown dry with N_2. The sample was then soaked for 1 minute in HCl / H_2O = 1:1 solution for removal of oxide layer formed on the GaAs surface. Next, the sample was rinsed and blown-dry with N_2, loaded into the E-beam evaporator. Next a seed layer of Ti-Au with thicknesses of (200:1000)Å was evaporated on the entire sample. After that, photoresist (AZ4400) was applied, spun at 2000 rpm for 30 seconds and baked at 95°C for 2 minutes. Next, using the mask aligner, the heat spreader photomask was aligned with the sample and the

sample was UV-exposed for 25 sec. at 10mW/cm^2. Next, the sample was developed using AZ400K:DI H_2O (1:4). The sample was then rinsed and dried. Our measured photoresist thickness was ~7μm.

Due to its good thermal conductivity, copper was used as our first plated layer while plated indium was utilized for the bonding process. The sample was first electroplated with Cu using the plating setup described in Section 3.3.1.8 at a current density of 13kA/cm^2 and a 20% duty cycle. Total electroplating time was 40 minutes. To improve plating thickness uniformity, the sample was rotated 180 degrees after 20 minutes of electroplating. Next, the sample was rinsed and the plating thickness was measured. Plated Cu thickness was about 4 μm.

Indium plating was done using the same setup used for Cu plating. Duty cycle and current density were also the same. The only difference was the plating chemical and electrode. The sample was plated with about 4μm of In. After stripping the resist, the Ti-Au seed layer was sputtered with Argon using the ICP (flow= 15sccm, ICP=50W, RIE=100W, pressure=7mTorr). The approximate sputtering time is 400sec. Since the exact time might vary, the ICP top view port was used to visually decide the exact time. Finally, to reduce the indium surface roughness and improve the thickness uniformity, the heat spreaders were annealed for 30 sec. at 160°C in N_2 using the Bio-Rad repaid thermal annealer. Furthermore, the annealing process makes the Indium layer denser, which should result in better thermal conductivity. Figure 3.42 shows an SEM image of the heat spreader. The insets show a bonding pad (a) before annealing, and (b) after annealing.

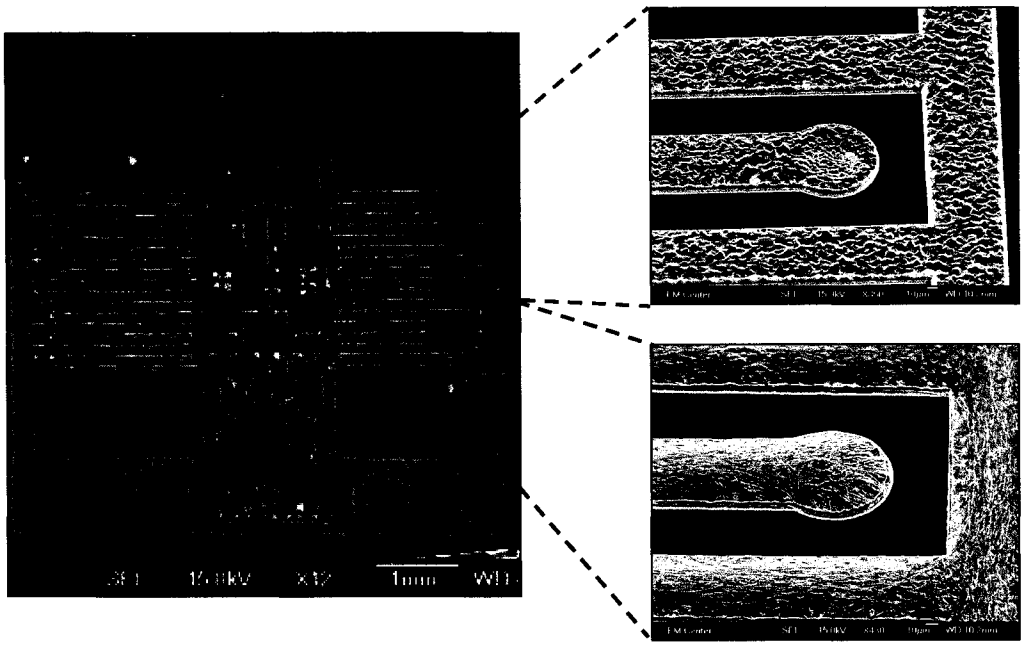


Figure 3.42 SEM image of the heat spreader. The insets show a bonding pad (a) before annealing, (b) after annealing.

At this point of the process, the VCSEL die is ready to be flipped and bonded to the heat spreader as shown in Figure 3.43.

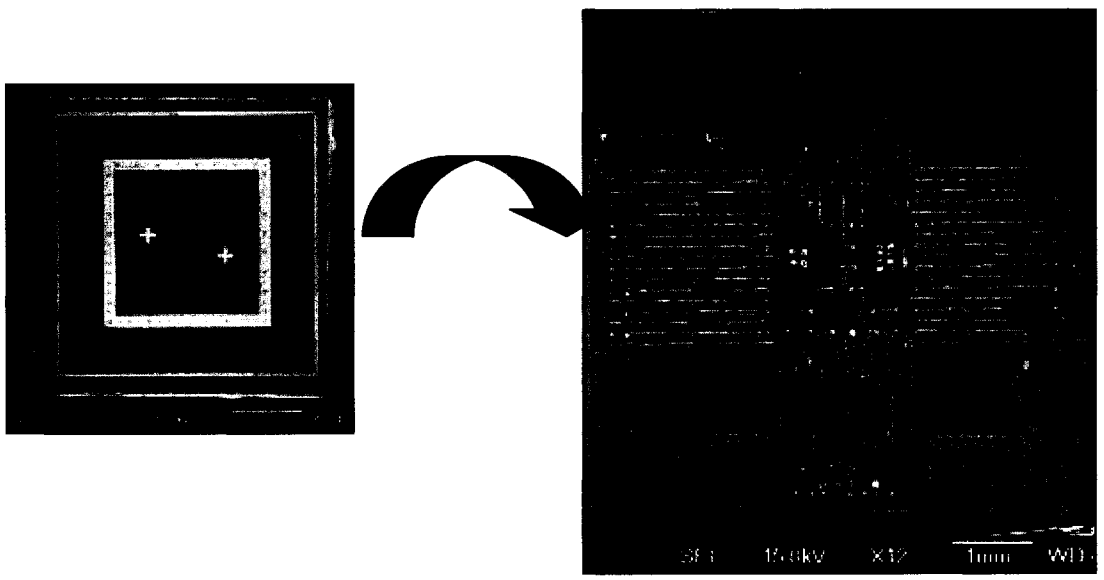


Figure 3.43 SEM image of the VCSEL die ready for flip-chip bonding to the heat spreader.

3.5.4 Flip-chip bonding

The bonding process began by placing the VCSEL die upside down on the sample holder. Next, the VCSEL die with the vacuum port was aligned on the placer arm and picked up by the vacuum. After that, the heat spreader was placed at the center of the resistively heated bonding chuck. To improve the bonding, a thin layer of indium flux (The Superior Flux and Mfg. Co. /Flux#30) was applied on the heat spreader. Next, the heat spreader was aligned with the VCSEL die by moving the stage holder (heat spreader holder) and then the VCSEL die was lowered slowly and placed on top of the heat spreader after setting a bonding force of 10N (1Kg). Figure 3.44 below illustrates the bonding setup at this point.

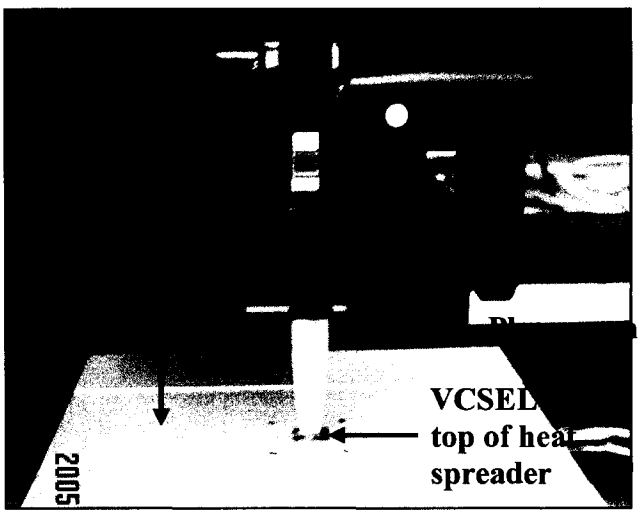


Figure 3.44 Flip-chip bonding setup.

Next, the heat spreader holder temperature was ramped to 130°C in 10 minutes and held at 130°C for 4 minutes using the resistively heated chuck, which replaced the original gas-heated chuck. Then the heater was switched off and the sample was allowed

to cool down for 10-15 minutes. An extra hour is allowed before the flux was rinsed with DI-water and blown dry with N_2. (Refer to [11] for complete detailed instructions on how to use the PICO flip-chip bonder.) It is important to tightly hold both the substrate and VCSEL die together during the rinsing. The reflow process was carried out using the Bio-Rad rapid thermal annealer in N_2, where the following heating profile was performed. The process began by loading the sample into the Bio-Rad rapid thermal annealer at 20°C, then gradually ramping the temperature from 20°C to 120°C over a 2-minute period and held at 120°C for 5 minutes to dry off the water. After that, the temperature was ramped again, from 120°C to 200°C over a 2-minute period, and held for 15 minutes, sufficient for wetting and bonding. Finally, the heater was turned off until the temperature dropped down to 50°C. (For more information on how to use the Bio-Rad rapid thermal annealer, refer to [11].) Even after reflow, it was easy to break the solder bonds by gently pushing on the laser die with tweezers. Figure 3.45 below shows the VCSEL die-bonded to the heat spreader and ready for characterization.

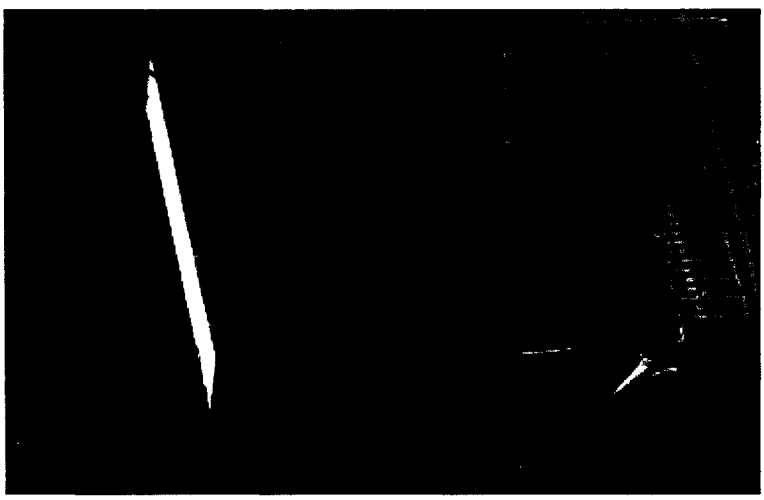


Figure 3.45 SEM of the flip-chip bonded VCSEL die ready for characterization.

Initial characterization of the fabricated devices raised several issues regarding the current design, which prevented the realization of operational flip-chip bottom-emitting VCSELs. The dummy mesa side walls were too steep for good step coverage, which resulted in a discontinuity of the ground contact (substrate contact). Another issue was the fact that the device mesa sidewalls were not insulated, which caused the junction to short out when the device mesa was pressed into the melted In during the bonding process. Figure 3.46 below shows a device mesa before and after bonding.

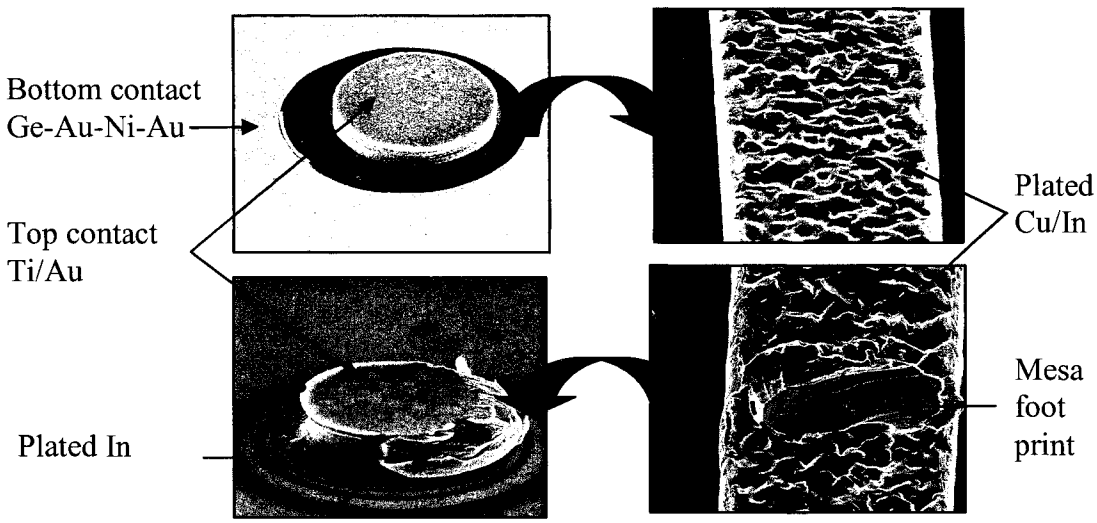


Figure 3.46 SEM images of the device mesas before and after bonding.

To overcome those two problems, the ground (Dummy) mesa sidewalls profile needs to be modified for better step coverage and the device mesa sidewalls need to be protected from the plated metals with an insulating material. The incorporation of photosensitive polyimide with the VCSEL die fabrication not only solved both problems, but also resulted in a process that is less sensitive to parameters such as the plating thickness and the bonding force. Since use of polyimide on the side wall provides poor lateral thermal conductivity compared to using SiN_x with plated metals on the sidewalls

as in the top-emitting devices, the current process will also work with the substitution of nitride for polyimide.

3.6 Bottom-emitting flip-chip bonded VCSEL fabrication (2nd generation)

For the second generation of the bottom-emitting VCSEL die fabrication, mesa etching and top and bottom contacts deposition were carried out using the same procedure described in Section 3.5.2. After that, the VCSEL die went through the polyimide photolithography and curing processes described in Section 3.3.1.7 using the mask aligner and the polyimide photomask, which is shown in Figure 3.47 (pink), imposed on the top and bottom contact masks (yellow and blue). This step formed annular polyimide around the device and ground mesas as shown in Figure 3.48 below, where the device mesa junction sidewalls are protected from the plated layers and the ground mesa sidewalls have a sloping profile that will solve the problem of step coverage. Next, the VCSEL die went through a final photolithography process using a mask to allow a layer of metal to be deposited everywhere except the device mesa. The goal of this step is to connect the bottom (substrate) contact to the top of the dummy mesas; in other words, to make both the signal and ground contacts on the same level. Figure 3.49 below shows a cross-section of the VCSEL die after the deposition of the Ti-Au layer with thicknesses of (200/1500) Å. A SEM image of the second generation of the VCSEL die, where the device and ground mesas are wrapped with polyimide and covered with Ti/Au, is show in Figure 3.50.

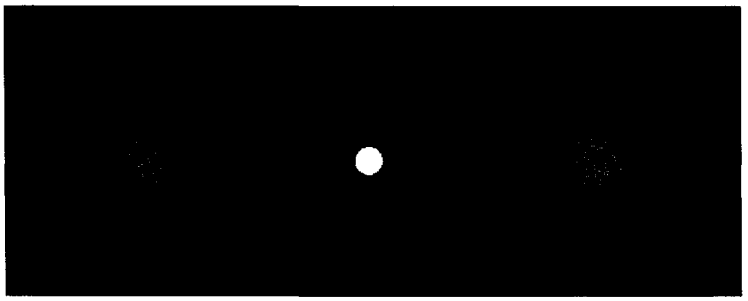


Figure 3.47 Polyimide (pink), top contact (yellow), and bottom contact (blue) photomasks.

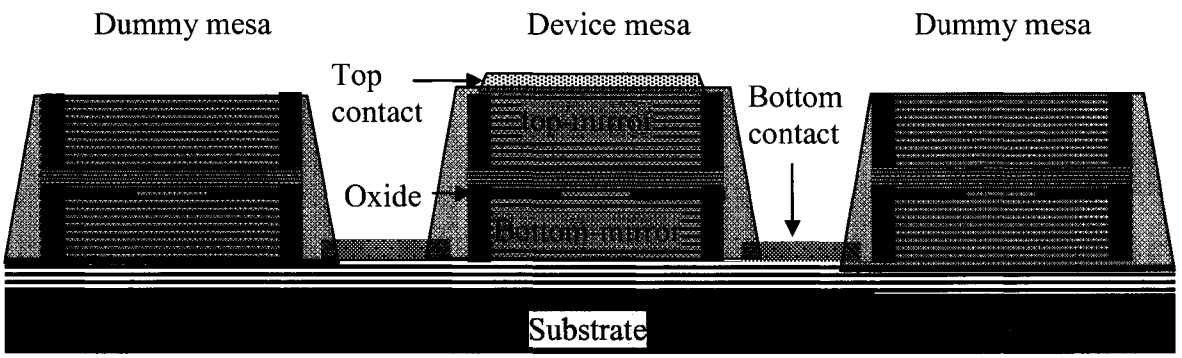


Figure 3.48 Device and dummy mesas after polyimide curing.

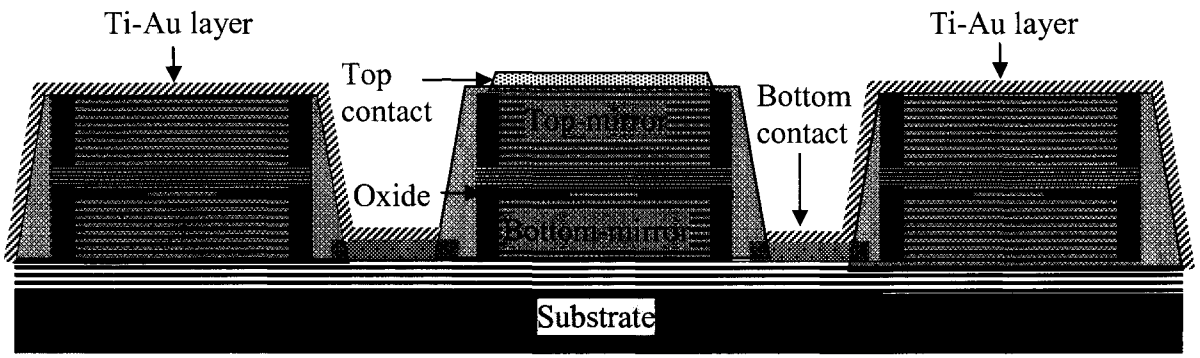


Figure 3.49 Cross- section of the VCSEL die after the deposition of Ti-Au.

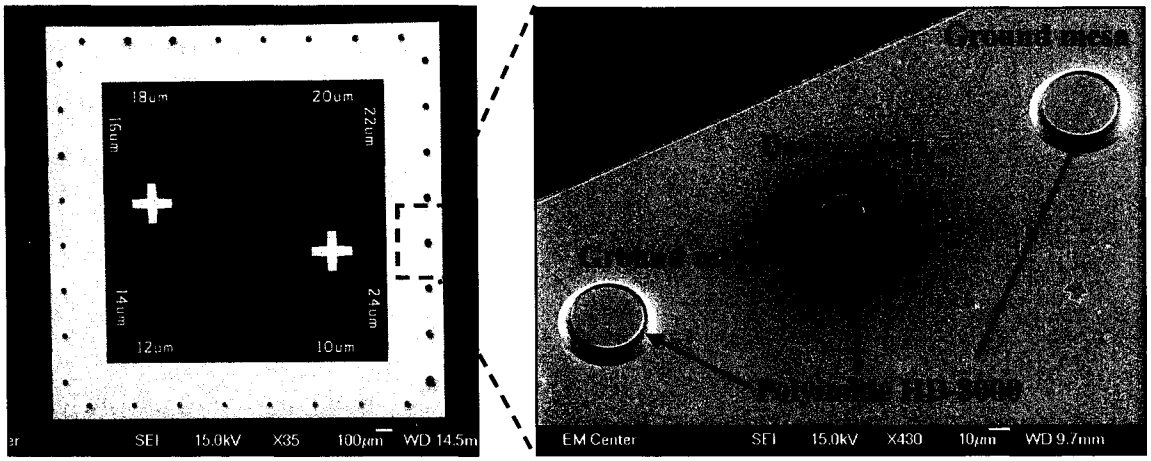


Figure 3.50 SEM image of the second generation of the VCSEL die. Device and ground mesas are wrapped with polyimide and covered with Ti/Au.

The heat spreaders for the bottom-emitting VCSELs were fabricated using the same procedure used for the first generation and described in Section 3.5.3 using the heat spreader mask shown in Figure 3.51. At this point, the VCSEL die is ready to be flipped and bonded to the heat spreader, as shown in Figure 3.52. The bonding process was also performed, as described in Section 3.5.4. Figure 3.53 below shows the VCSEL die bonded to the heat spreader and ready for testing.

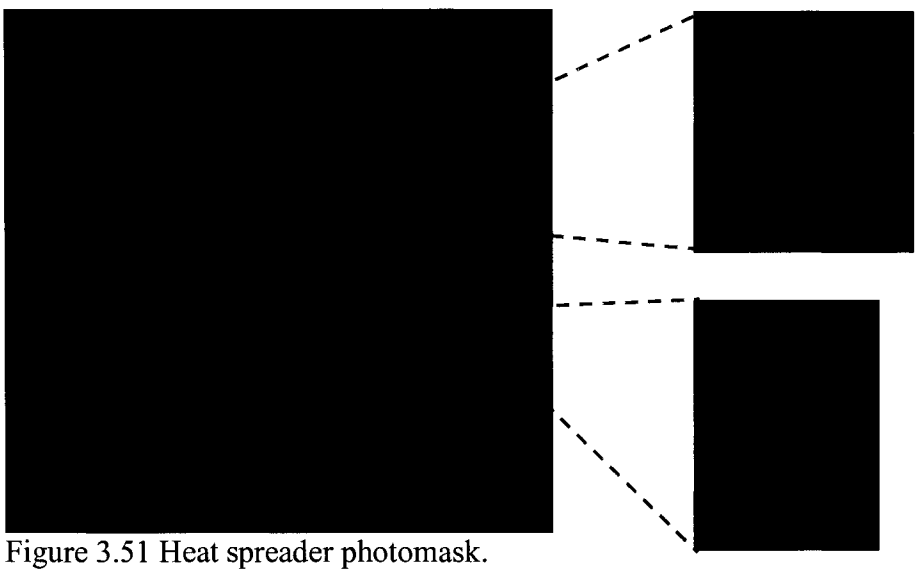


Figure 3.51 Heat spreader photomask.

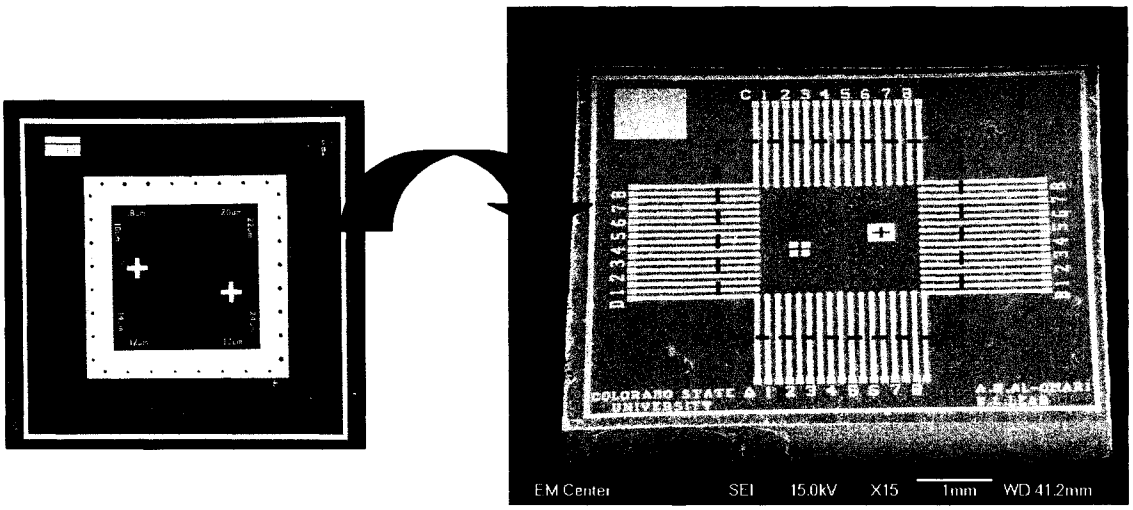


Figure 3.52 SEM image of the VCSEL die ready for flip chip bonding to the heat spreader.

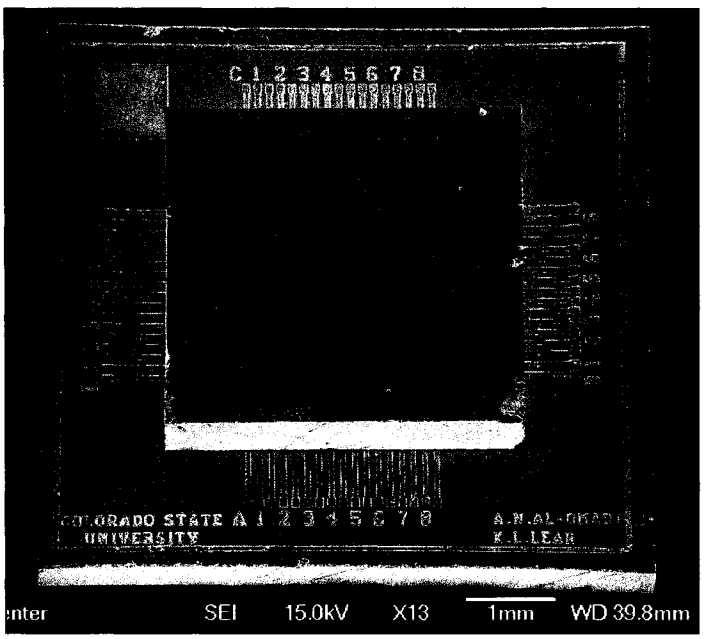


Figure 3.53 SEM image of the flip chip bonded VCSEL die ready for testing.

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Chapter 4

TESTING AND CHARACTERIZATION OF HIGH-SPEED VERTICAL-CAVITY SURFACE-EMITTING LASERS

4.1 Introduction

In this chapter, testing and characterization of high speed VCSELs will be discussed. Two phases of testing will be presented. The first phase is the DC characterization of VCSELs, which is done by changing the VCSEL bias current and measuring the voltage across the device as well as the output power in order to generate the continuous wave (CW) L-I-V plots. All the plots were obtained at room temperature. Included in this DC testing phase also is the measurement of the thermal resistance (R_{th}), which were determined by measuring the wavelength dependence of the laser spectra as a function of the electrical input power. Both setups used for the L-I-V and R_{th} measurements are presented in Section 4.2.1. The second phase is the AC characterization of VCSELs, where the modulation response (S_{21}) of VCSELs with different diameters was measured for various bias currents using the AC testing setup and procedure described in Section 4.2.2.

As two different generations of VCSELs were fabricated from the various epitaxial materials (see Table 4.1), the rest of the chapter will be divided into two main sections. The first is Section 4.3.1, which will present the testing and characterization results for the first generation of VCSELs, followed by case studies for related results. Section 4.3.2

will present the testing results for the second generation of VCSELs, in which various modifications on the mask layout design and fabrication process have been adopted.

4.2 Testing and characterization setup

4.2.1 DC testing setup

The DC characteristics of VCSELs, which includes I-V plots as well as photodiode current vs. VCSEL current plots for different VCSEL sizes, were measured. In addition, plots for thermal resistance and threshold current density for different mesa sizes were obtained.

4.2.1.1 CW *L-I-V* testing setup

To carry out the DC measurements, an equipment setup consisting of a Micromanipulator probe station with a constant temperature chuck, an HP 4145A semiconductor parameter analyzer, and a silicon photodiode with a 10x10mm^2 active area and ~0.5A/W and 0.68A/W responsivity for 850nm and 980nm wavelengths, respectively, were used.

Figure 4.1 shows the DC testing setup. Channel 1 from the HP 4145A was connected to the VCSEL pads to provide bias current and measure voltage. Channel 2 was connected to the photodiode to provide the DC reverse bias voltage and to enable the HP 4145A to measure the photodiode current. The VCSEL voltage and photodiode current were plotted as a function of the VCSEL bias current. The photodiode was aligned on top of the VCSEL with a 1cm clearance so that most of the light from the VCSEL would hit the photodiode surface, while providing enough working space to

make sure that the photodiode would not be damaged by hitting the probes. A similar setup was used to carry out the L-I-V plots for the bottom-emitting devices with minor changes, shown in Figure 4.2, where a transparent (glass) chuck was used and the photodiode was placed to collect the output light from the devices at the bottom since the devices at this point have not been flip-chip bonded and, as a result the light is emitted downward. All the plots that were obtained on the HP 4145A screen were captured using a PC, GPIB card, and a Labview code. Both I-V curves and photodiode current vs. VCSEL current curves were measured at room temperature.

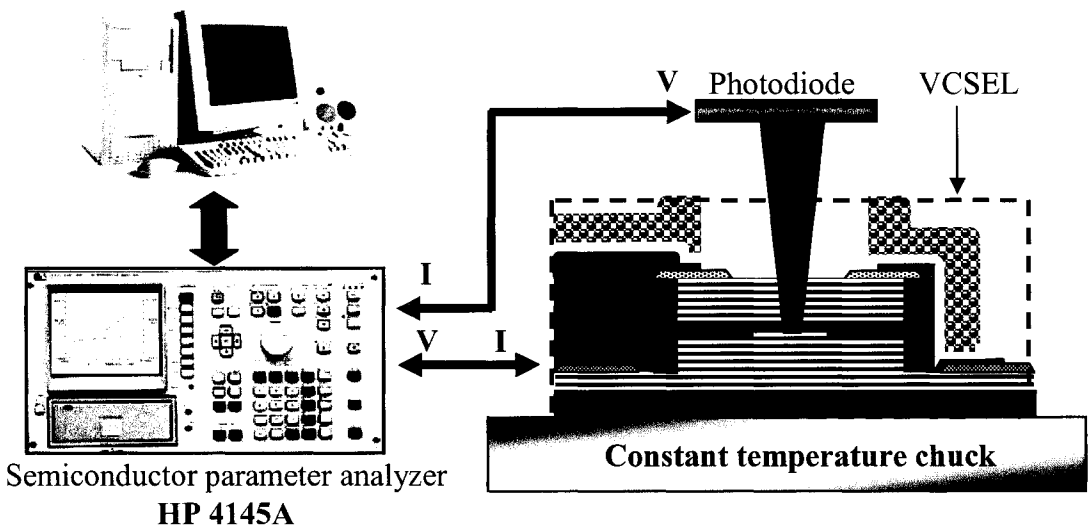


Figure 4.1 Top-emitting CW L-I-V testing setup.

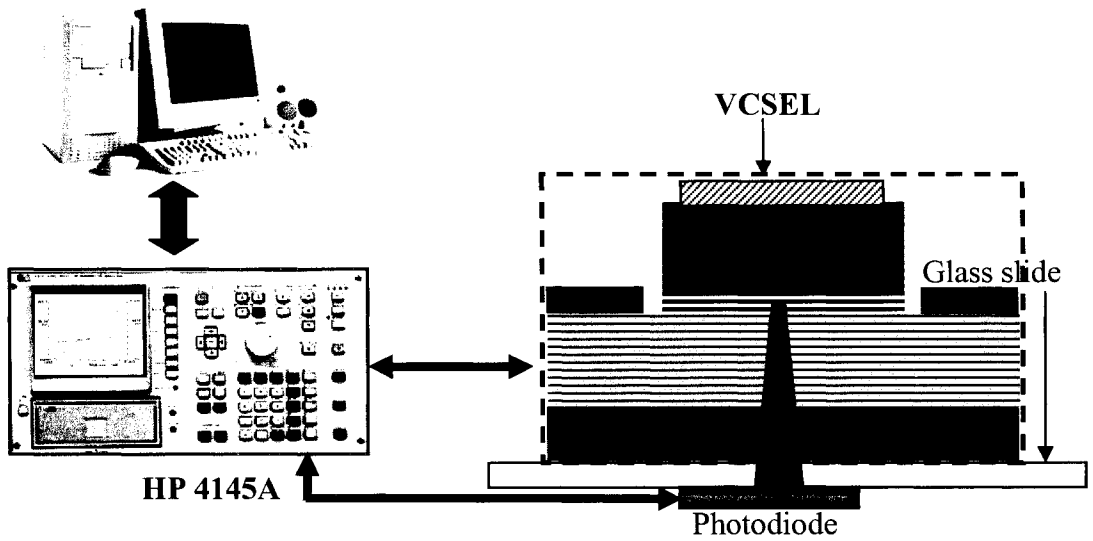


Figure 4.2 Bottom-emitting CW L-I-V testing setup before flip-chip bonding.

The HP 4145A was programmed to provide the VCSEL under test with the required DC voltage and to sweep the current up to ~$10I_{th}$. In fact, pushing the current significantly above $10I_{th}$ could result in damaging the VCSEL under test. It is therefore recommended to program the parameter analyzer to sweep the current in a small range first to get a feeling for the VCSEL I_{th}, and then the maximum limit for the applied bias current can be decided.

The VCSEL first worked as an LED when the applied current was less than I_{th}. Since there is only spontaneous emission in this current range, only a small photodiode current was measured (~ μA). As soon as the applied current reached the VCSEL I_{th}, the VCSEL began operating as a laser and the output light intensity was enough to produce a current in the photodiode in the range of ~0.1 to 10 mA, depending on the VCSEL output light intensity. An example of an L-I-V curve is seen in Figure 4.7.

4.2.1.2 Thermal impedance (R_{th}) measurements setup

VCSEL self-heating is an important issue that is worth discussion. Heat in a VCSEL will cause what is called thermal wavelength shift, due to the change in the refractive index of the resonator and the thermal expansion of the semiconductor mirrors. Also, VCSEL heating will cause the optical gain peak to decrease as the VCSEL heats up. Heating in the VCSEL can be described by the VCSEL thermal resistance, R_{th}, which is used to quantify how easily heat power flows out of the VCSEL toward the heat sink. Thermal resistance is defined as the ratio of VCSEL temperature rise ΔT and dissipated electrical power P_d ($R_{th}= \Delta T/ P_d$). Assuming that heat flows from a uniform temperature disc with a diameter $2a$ on a homogenous, isotropic, semi-infinite substrate of thermal conductivity ξ, the measured size dependence of thermal resistance approximately follows the simple analytical estimation for heat spreading [1,2],

$$R_{th} = \frac{1}{4\xi \cdot a} \tag{4.1}$$

For VCSELs in the 800 to 1000nm emission wavelength range, the mode shift is typically found to be $\partial\lambda/\partial T \approx 0.07 nm/^{o}C$ [1,2]. With this ratio, the thermal resistance (R_{th}) was determined by measuring the wavelength dependence of the laser spectra as a function of the electrical input power using the setup shown in Figure 4.3. The Keithley Source Meter 2400 series provided bias current to the VCSEL under test and measured voltage. Using a multimode fiber, the output light of the VCSEL was coupled into the optical spectrum analyzer, which measured the wavelength spectrum. In devices where

multiple modes exist, individual modes need to be tracked. A more detailed explanation for this technique is presented in Section 4.3.1.2.

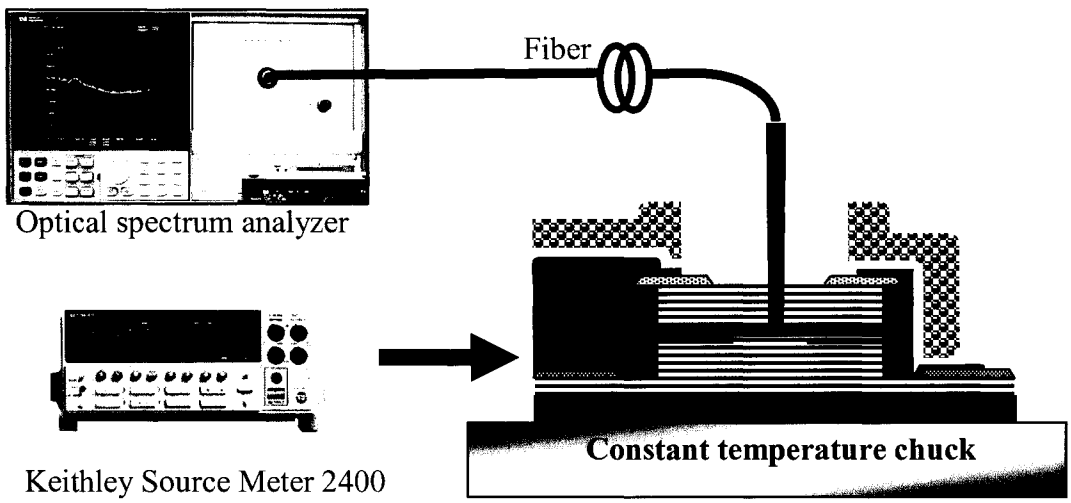


Figure 4.3 Thermal resistance (R_{th}) measurement setup.

4.2.2 AC testing and characterization setup

The frequency modulation response (S_{21}) of VCSELs with different diameters was measured for varying bias currents. The AC measurements test apparatus consisted of an Agilent 8722ET vector network analyzer (VNA) with 40GHz bandwidth, a computer with a GPIB card to load the calibration kit into the VNA, a high-speed 22GHz Discovery Semiconductor DSC30S photodiode attached to a 20GHz MITEQ JSTD-02K200-40-10P amplifier, an HP 4145A semiconductor parameter analyzer, a high precision Cascade Microtech impedance standard substrate (ISS-101-190), a probe station equipped with a 20°C constant temperature vacuum chuck, an LED illuminator to reduce sample temperature variations, ~2 meters of graded index multimode 50μm core diameter fiber, a JAVELIN CCD camera, a SONY 12" monitor, a 40GHz Anritsu K251

bias tee, 40GHz Insulated Wire KPS-1501-360-KPS electrical cables with 2.92mm(k) type connectors, and Cascade Microtech air co-planar probes (ACP40) with GSG configuration, a 125μm pitch, and Be-Cu tips that provide repeatable contact on gold pads. The use of ACP with GSG configuration helps deliver the RF signals with minimal attenuation and good impedance control, which results in accurate measurements [3]. Figure 4.4 gives an illustration of the AC testing setup. The HP 4145A operation is similar to that described in Section 4.2.1. The sample was mounted on the constant temperature chuck at room temperature and was aligned so that the output light would be collected by the fiber. The active alignment was done by biasing the VCSEL above threshold and adjusting the position of the fiber tip using an x-y-z positioning stage until the DC optical power in the fiber was maximized based on the reading of a hand-held RIFOCS 555B optical power meter. The fiber was probably within 0.1mm or less of the sample.

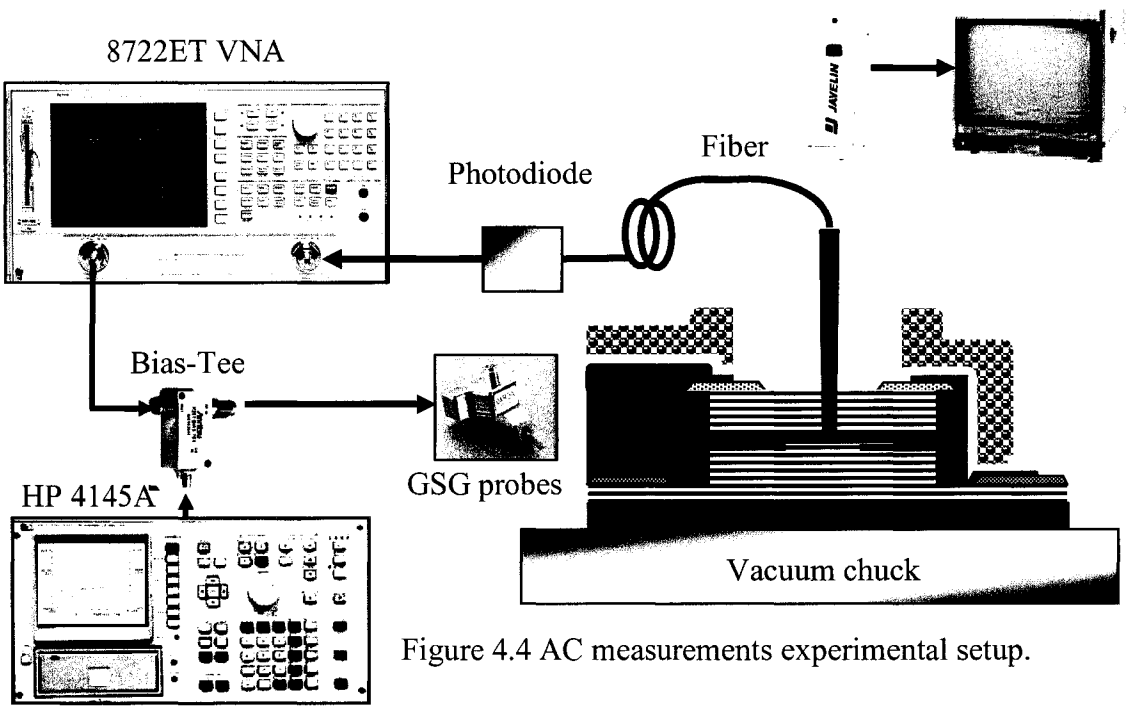
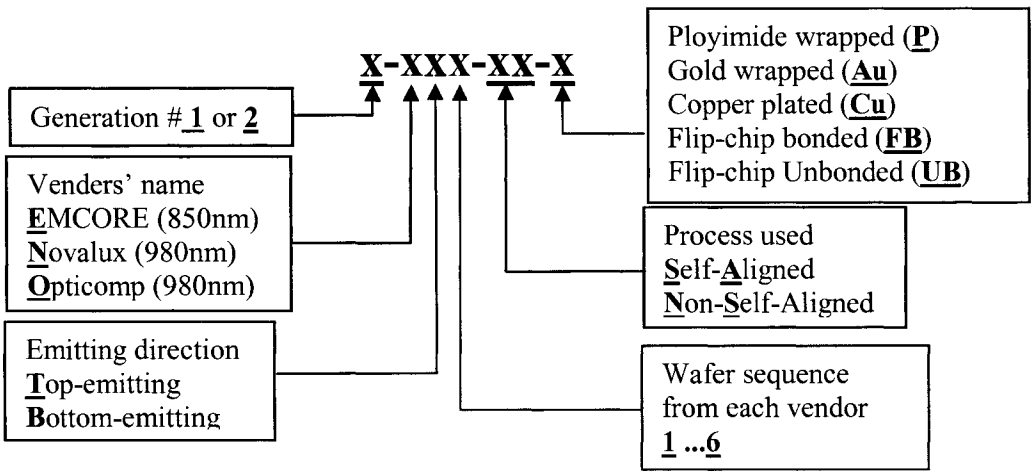


Figure 4.4 AC measurements experimental setup.

The output light was collected by the fiber and guided to the optical high-speed Discovery photodiode. The electrical AC signal from the photodiode was amplified and input to the 8722ET network analyzer. The modulation response of VCSELs for various bias currents was measured at microwave frequencies over a range of 50MHz to 40 GHz.

4.3 First generation VCSELs DC and AC testing and characterization results

Table 4.1 summarizes the various epitaxial material structures that were used to fabricate VCSELs. In the following sections, each fabricated sample will be identified by a unique identification number, x-yyy-zz-w, where its' legend is shown below.



T able 4.1 Epitaxial structures summary.

Vendor	Wafer label	Wafer number	Emitting direction/ λ(nm)	Top mirror	# of QW	Bottom Mirror	Oxidation layer location	Comments
EMCORE	EMCORE	ET1	top/850	25n	3	34p	bottom mirror[a]	Inverted polarity
Novalux	8.50/5	NT1	top/980	32p	3	37n	top mirror[a]	Need λ/4 SiN_x see Sec. 4.3.2 for more details
	8.50/6	NT2	top/980	20p	3	37n	top mirror[a]	
	8.51/9	NT3	top/980	22p	6	37n	top mirror[a]	
	8.53	NB1	bottom/980	32p	6	19n	none	
	8.54	NB2	bottom/980	32p	6	20n	none	
	8.55	NB3	bottom/980	32p	6	15n	none	
	8.57	NT4	top/980	16p	3	37n	none	
	8.58	NT5	top/980	16p	6	37n	none	
	8.59	NT6	top/980	17p	3	37n	top mirror[a]	
Opticomp	137	OT1	top/980	17p	3	30n	top mirror[a]	

a: close to the active region

4.3.1 Top-emitting 850nm VCSELs with a self-aligned contact and copper-plated heatsink (1-ET1-SA-Au and 1-ET1-SA-Cu)

Top-emitting, 850nm VCSELs with a self-aligned top contact and evaporated gold or plated copper heatsink were fabricated and characterized using the EMCORE structure. Thermal resistance was reduced by 44%, and output power and bandwidth were increased by 38% and 12%, respectively, compared to polyimide wrapped devices fabricated from the same epitaxial wafer [4]. The fabricated devices exhibit a 3dB modulation frequency bandwidth up to 16.3GHz at 10kA/cm^2. The results presented in this section were published in [5].

4.3.1.1 Fabrication summary

Top-emitting, self-aligned, high-speed, 850 nm VCSELs were fabricated using ET1 epitaxial material structure described in Section 3.3.1.1. Device fabrication began with the formation of an annular *n*-type contact by evaporating Pd-Ge-Ti-Pt with thicknesses of (500/1000/250/300) Å. The contact and a smaller diameter photoresist feature protecting the aperture served as an etch mask for cylindrical mesas. The contact outer diameter, and thus the mesa diameter is 18 to 28μm. The contact has a 4μm width, giving contact aperture sizes of 10 to 20μm. Mesas were etched to a depth of 5μm, stopping in the bottom mirror, using a load-locked, Trion ICP dry-etching system (see Section 3.3.1.2 for more details). To form the current aperture and provide lateral index guiding to the lasing mode, the sample was wet-oxidized in a 380°C steam environment for 20 minutes using the oxidation setup shown in Figure 3.15, resulting in the oxide extending in 4μm from the mesa sidewall. The bottom *p*-type contact of BeAu (pre-alloyed 1% Be by weight)-Ti-Au with thicknesses of (500/300/700)Å was evaporated onto the partially etched bottom mirror as described in Section 3.3.1.5. After contact formation, 1000Å layer of PECVD silicon nitride (SiN_x) was deposited to electrically insulate the mesa sidewall from later metallic coatings. Vias in the SiN_x were etched for the top and bottom metal contacts. The HD-8000 positive tone polyimide used for VCSEL planarization, as described in Section 3.3.1.7, resulted in a polyimide thickness of 5.5μm.

The final processing steps were varied to compare the thermal impact of three different structures. Ti-Au with thicknesses of (200/3000) Å were evaporated on the first sample, including the mesa sidewall for a heatsink, metal interconnects, and coplanar

waveguide probe/bond pads. A second sample was electroplated with ~2μm of Cu using the process and setup described in Section 3.3.1.8. Cu rather than Au plating was chosen due to copper's higher thermal conductivity (4.01W/cm-K) and lower cost (~$24/m^2-μm) compared to gold (3.17W/cm-K, ~$3520/ m^2-μm). Figures 4.5 and 4.6 show SEM photos of high-speed Au-wrapped and Cu-plated VCSELs, respectively, at the completion of fabrication, with a magnified view of the mesas.

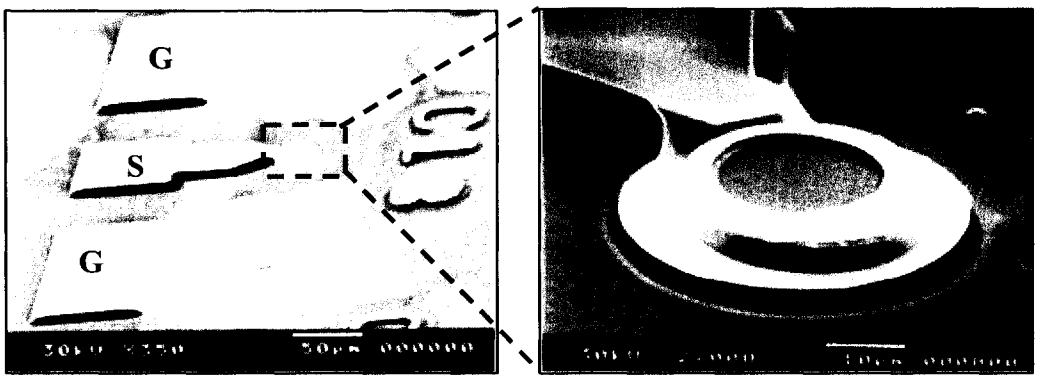


Figure 4.5 SEM photo for a completed Au-wrapped high-speed VCSEL with 18μm diameter and 10μm oxide aperture (1-ET1-SA-Au).

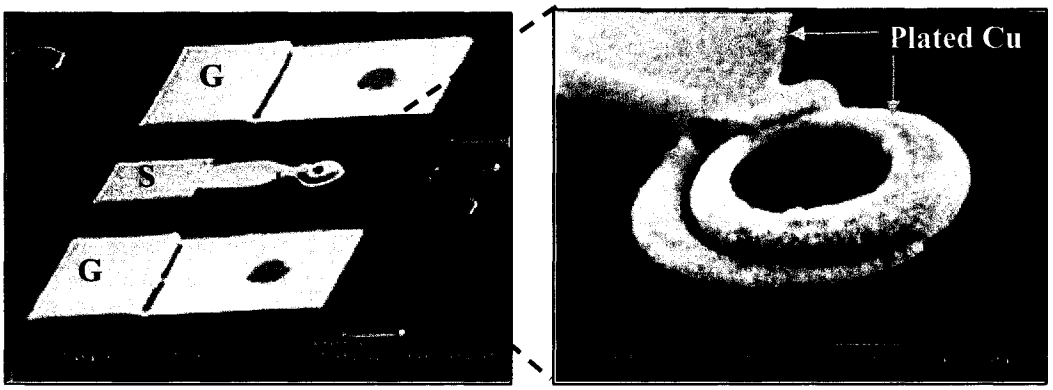


Figure 4.6 SEM photo for a completed Cu-electroplated high-speed VCSEL with 18μm diameter and 10μm oxide aperture (1-ET1-SA-Cu).

4.3.1.2 Measurements and discussion

Using the DC testing setup described in Section 4.2.1.1, the CW L-I and I-V characteristics of Au-wrapped (1-ET1-SA-Au) and Cu-plated (1-ET1-SA-Cu) VCSELs with 18 and 28μm mesa diameter with 10 and 18μm oxide apertures, respectively, were measured at room temperature. Figures 4.7 and 4.8 show the L-I-V characteristics of Au-wrapped and Cu-plated VCSELs with 10μm and 18μm oxide apertures. A third sample had been fabricated earlier with polyimide, which has a thermal conductivity of 0.002W/cm-K [6], rather than metal covering the mesa sidewall [4]. All of the devices were fabricated from material within 20mm of the center of a single 75mm diameter, epitaxial wafer.

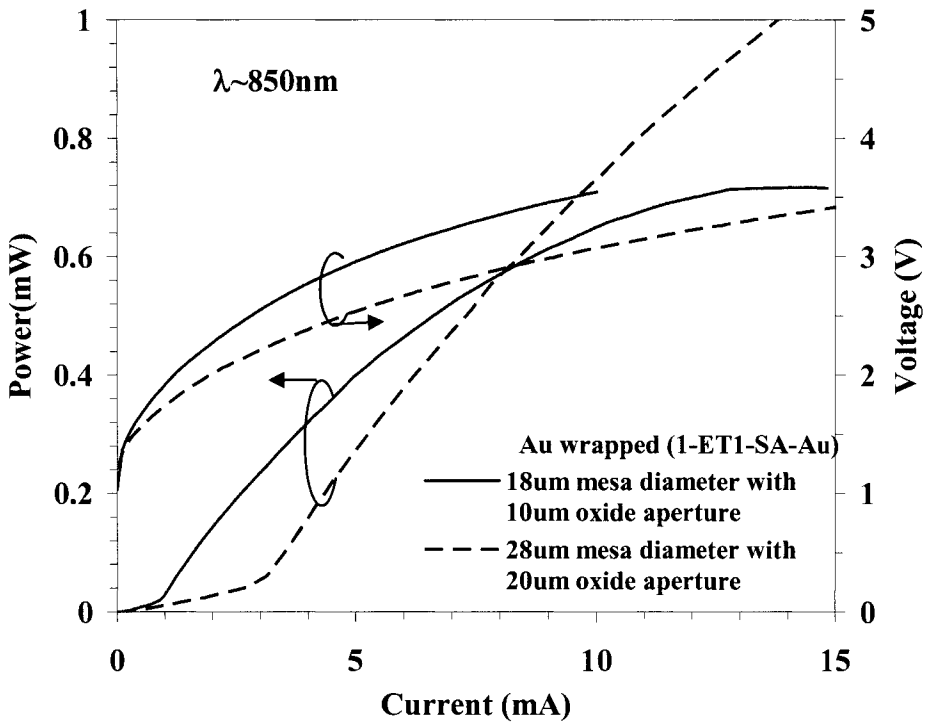


Figure 4.7 CW L-I-V for a top-emitting 850nm VCSELs with a self-aligned contact and Au-wrapped heatsink.

Figure 4.9 shows the CW L-I characteristics of polyimide wrapped [4], Au-wrapped, and Cu-plated VCSELs with 10μm oxide apertures. The Au-wrapped and the Cu-plated heat-spreading layers increase the output power at 10mA=~$13I_{th}$ from 0.66mW to 0.76 mW and 0.91 mW, respectively. VCSELs were all chosen to have the same size, 10μm diameter, oxide apertures. Minimal device heating occurs at threshold, so the average threshold current densities of the samples are assumed to be the same. The observed ±14% variation in threshold current corresponds to a variation of ±0.7μm in diameter due to oxide aperture non-uniformity. For easier comparison, Table 4.2 lists the threshold current, output power at bias current 13 times the threshold current, and the slope efficiency close to threshold for the polyimide-wrapped [4], Au-wrapped, and Cu-plated VCSELs.

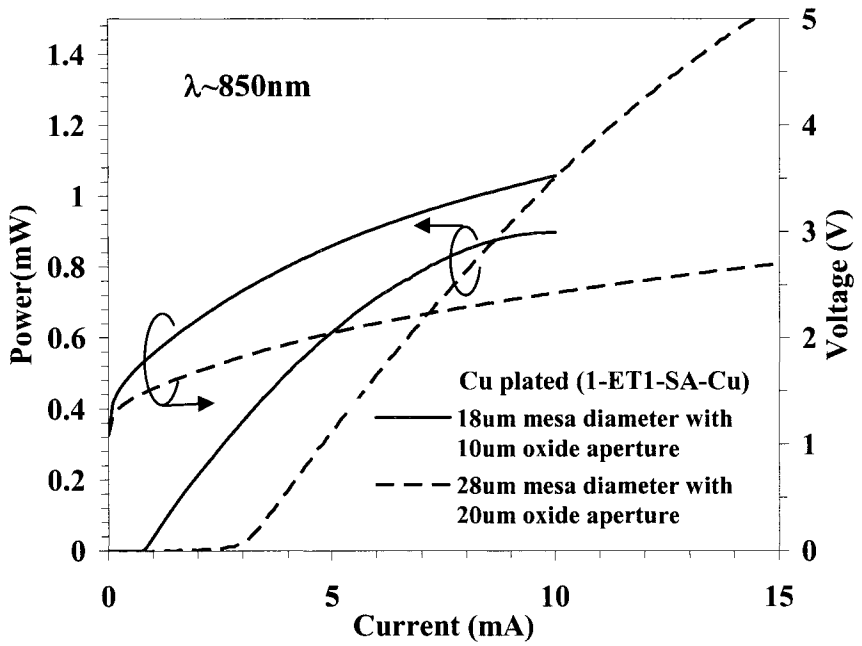


Figure 4.8 CW L-I-V for a top-emitting 850nm VCSELs with a self-aligned contact and Cu- plated heatsink.

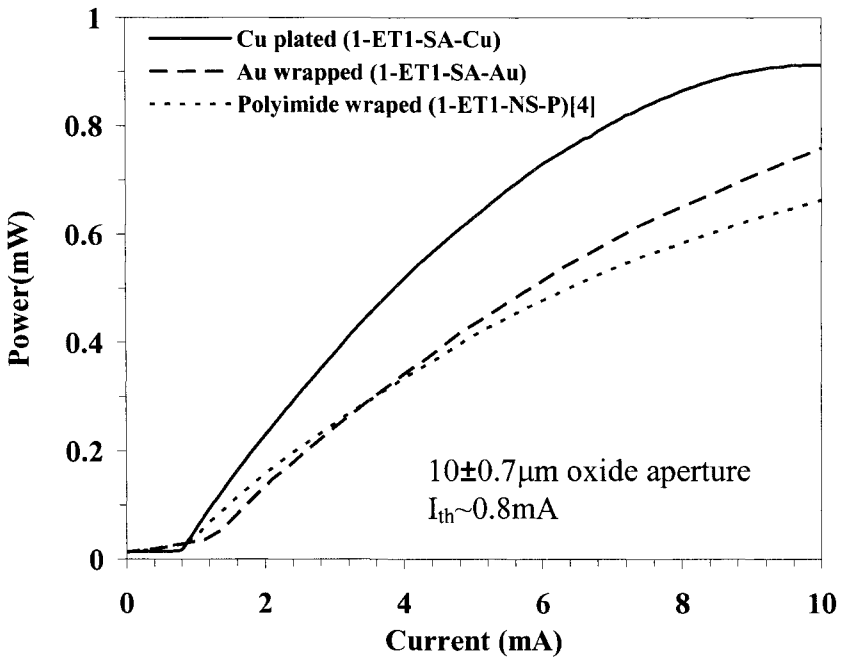


Figure 4.9 CW L-I characteristics of polyimide wrapped [4], Au-wrapped, and Cu-plated VCSELs with 10μm oxide apertures.

Table 4.2 I_{th}, output power at $I_{bias}= 13I_{th}$, slope efficiency, and R_{th} for polyimide-wrapped [4], Au-wrapped, and Cu-plated VCSELs.

	Polyimide wrapped [4] (1-ET1-NS-P)	Au wrapped (1-ET1-SA-Au)	Cu plated (1-ET1-SA-Cu)
Oxide aperture (μm)		10±0.7	
I_{th} (mA)	0.90	0.65	0.70
P at $I_{bias}= 13I_{th}$ (mW)	0.66	0.76	0.91
η_{slope} (%)	6	7	10
R_{th} (°C/mW)	2.6	2.3	2

The thermal resistance (R_{th}) of the devices was determined as described in Section 4.2.1.2 using the setup shown in Figure 4.3. As an example, let us discuss in detail how the measured R_{th} for a Au-wrapped (1-ET1-SA-Au) 10μm device ended up to be 2.5°C/mW. The Keithley multimeter was programmed to provide the bias current (I_{bias}) and measure the bias voltage (V_{bias}) for the VCSEL under test. Next, the multimode fiber was aligned on top of the VCSEL to pick up the emitted light and feed it to the spectrum

analyzer, which measured the wavelength spectrum (power vs. wavelength). The measured wavelength light intensity peaks and their corresponding dissipated electrical power (P_d=$P_{in\ electrical}$-$P_{out\ optical}$) were recorded and tabulated, as shown in Table 4.3. Next, the light intensity peaks at λ_1, λ_2, λ_3, λ_4, and λ_5 (nm) were plotted as a function of P_d, as shown in Figure 4.10. After that, the data were fitted to a straight line with a slope of $\delta\lambda/\delta P_d$. To obtain R_{th}, $\delta\lambda/\delta P_d$ is divided by the wavelength change as a function of temperature that is $\delta\lambda/\delta T$~0.07(nm/°C) [1,2]. For our example, the slope of the fitted straight line was $\delta\lambda/\delta P_d$~0.175 (nm/mW), thus R_{th}= 0.175 (nm/mW)/ 0.07(nm/°C) = 2.5°C/mW.

Table 4.3 Dissipated electrical power (P_d), and light intensity peaks at λ_1, λ_2, λ_3, λ_4, and λ_5

P_d (mW) =$P_{in\ electrical}$-$P_{out\ optical}$	λ_1(nm)	λ_2(nm)	λ_3(nm)	λ_4(nm)	λ_5(nm)
3.09	839.47	none	none	none	none
4.40	839.67	none	none	none	none
5.75	839.88	840.49	840.96	none	none
7.2	840.12	840.73	841.21	841.58	none
8.71	840.37	840.97	841.48	841.84	842.24
10.28	840.62	841.23	841.73	842.2	842.51
11.83	840.98	841.52	842.02	842.47	842.81
13.4	841.16	841.79	842.3	842.72	843.1

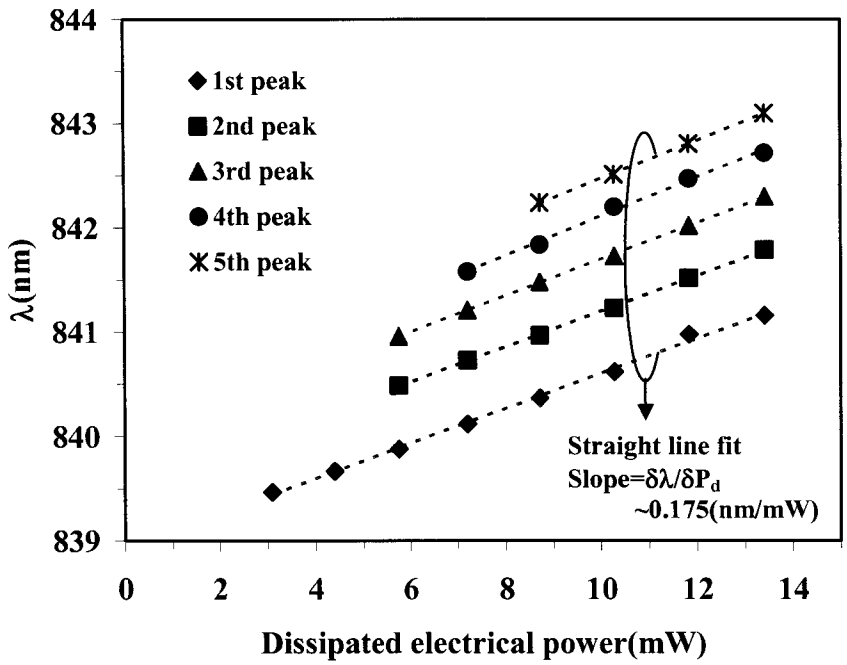


Figure 4.10 Light intensity peaks at λ_1, λ_2, λ_3, λ_4, and λ_5 (nm) as a function of the dissipated electrical power.

The samples with metal near the sidewalls showed reduced thermal resistance for a range of device diameters. Figure 4.11 shows the thermal resistance as a function of the active diameter (red). Au-wrapped and Cu-plated heat-spreading layers reduce R_{th} by 25% and 44%, respectively, for a range of device sizes compared to devices reported in [4]. The measured size dependence of thermal resistance approximately follows the simple analytical estimation presented in Equation 4.1. Although the sample structure is more complicated than the idealized disc geometry, the good fit motivates parameterization using ξ to allow comparison of various sized devices. Using a best fit to our data, we obtain ξ =0.22 W/cm-K, 0.27 W/cm-K, and ~0.17 W/cm-K for Au-wrapped, Cu-plated, and polyimide wrapped devices, respectively. As predicted, the DBR alloy scattering reduces ξ [1] compared to GaAs and AlAs, which have ξ =0.45 W/cm-K and 0.9 W/cm-K. Figure 4.11 summarizes other reported thermal resistances of

VCSELs that were fabricated using various techniques [7-14]. While reported R_{th} values for the present devices are lower than some of the values reported by others [4,10,11,13], there are previously reported values for R_{th} [9] that are much lower than the rest of the previous reports. For example, devices from [9] with an 8μm oxide aperture diameter exhibited R_{th} values of 1.4°C/mW. These devices are bottom-emitting VCSELs, which have the advantage of allowing the plated metal heatsink to cover not only the mesa sidewalls, but also the top side of the mesa without the need of having an aperture within the plating on top of the mesa for the light to escape since these devices emit light through the substrate. Furthermore, the reported VCSELs [9] were plated with 8.5μm of Au compared to only 2μm of Cu in our case.

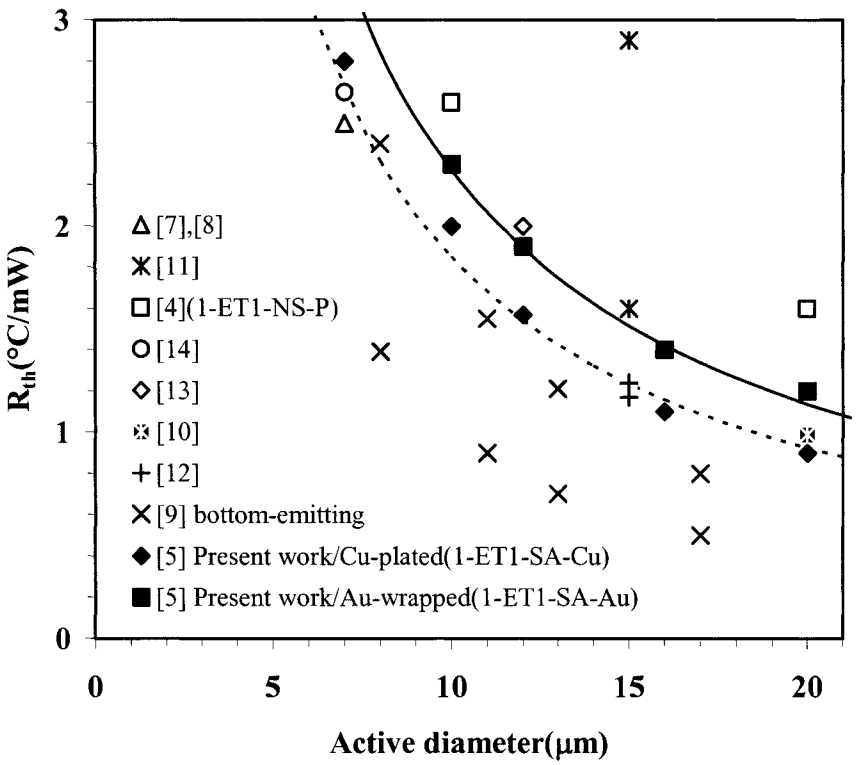


Figure 4.11 VCSELs thermal resistance as a function of the active diameter. Au wrapped and Cu-plated heat spreading layers reduce R_{th} by 25% and 44%, respectively, compared to [4].

The AC measurement apparatus used is described in Section 4.2.2. The system modulation response, S_{21} was measured for VCSELs at various bias currents over a frequency range of 50 MHz to 40 GHz from which the 3dB frequencies were obtained. As shown in Figure 4.12, polyimide wrapped and Cu-plated 10μm diameter aperture lasers exhibit maximum 14.6GHz and 16.3GHz 3dB bandwidths when biased at 4.5mA and 8 mA, respectively. Larger devices exhibit smaller 3dB frequencies. The moderate bias current densities, such as the 9.5±1.3kA/cm^2 necessary for the 16.3GHz bandwidth in the 10μm diameter device, should improve reliability [15]. Previously published VCSEL modulation bandwidths of 16.3GHz [16] and 15.2GHz [8] for oxide-confined devices, 14.5 GHz for an implanted device [17], and 21 GHz for an oxide and implant confined device [14] required bias current densities of 50kA/cm^2, 27.8kA/cm^2, 22.2kA/cm^2, and 30kA/cm^2, respectively. The history of published results on VCSEL modulation bandwidth as a function of the current density is summarized in Figure 4.13. It is apparent from Figure 4.12 that as the bias current increases, the -3dB modulation frequency also increases until a certain limit, and then the modulation frequency saturates. The solid line is a theoretical fit using

$$f_{3dB}=MCEF.(I-I_{th})^{1/2} \tag{4.2}$$

where MCEF is the modulation current efficiency factor. The 3dB bandwidth for polyimide-wrapped and Cu-plated devices saturates at $6I_{th}$ and $11I_{th}$, respectively. The best fit results in a MCEF of 8.2GHz/mA$^{1/2}$ and 7.0GHz/mA$^{1/2}$ for polyimide-wrapped and Cu-plated devices, respectively. The lower MCEF of the Cu-plated device was

unexpected. An even higher thermally limited 3dB bandwidth would be expected from the lower thermal resistance Cu-plated device if its MCEF were increased and capacitance reduced.

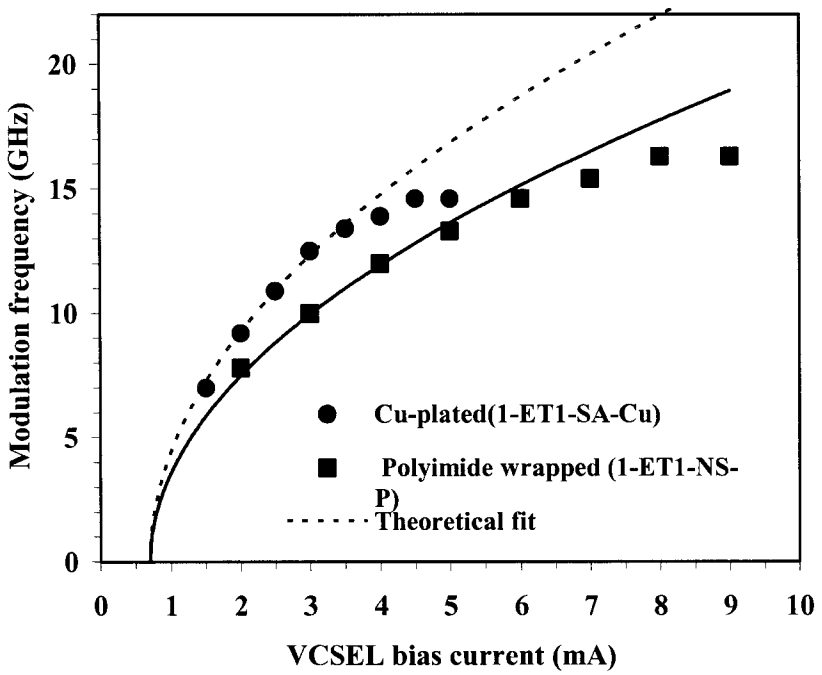


Figure 4.12 Polyimide-wrapped and Cu-plated 10μm diameter aperture VCSELs modulation response at various bias currents.

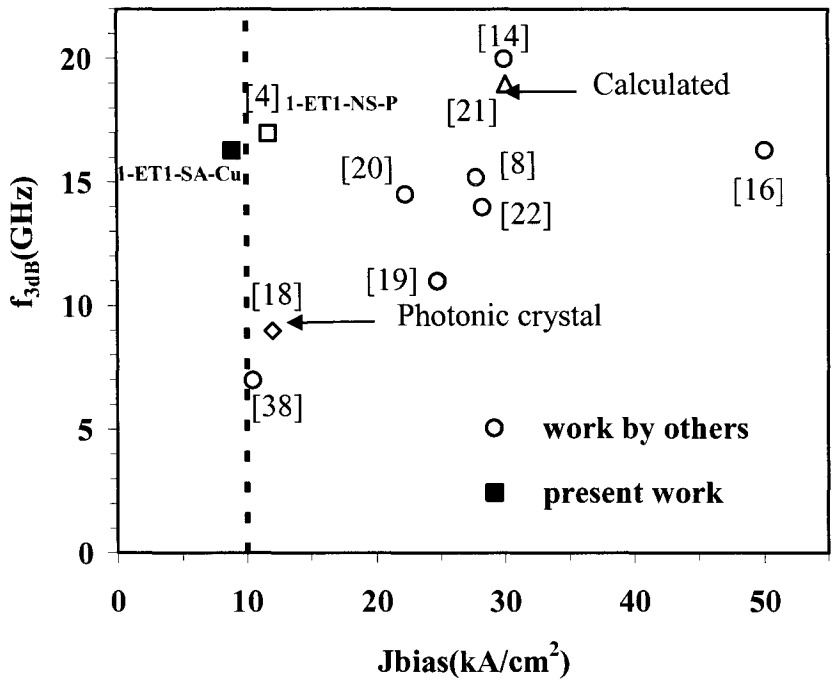


Figure 4.13 VCSEL modulation bandwidth vs. bias current density.

4.3.2 Top-emitting 980nm VCSELs with a self-aligned contact and copper-plated heatsink (1-NT1-SA-Cu, 1-NT2-SA-Cu, and 1-NT3-SA-Cu)

In the previous section, VCSELs with ~850nm wavelength were investigated. Devices with ~980nm wavelength are also of interest due to the higher differential gain ($\delta g/\delta N$) of the quantum wells and the transparency of the GaAs substrate at this wavelength. Undoped InGaAs 980nm quantum wells have a $\delta g/\delta N$ of $1.13 \times 10^{-15} cm^{-2}$ [23] compared to $0.77 \times 10^{-15} cm^{-2}$ for undoped 848nm GaAs quantum wells [24]. Furthermore, since the energy of the 980nm photons is less than the GaAs substrate energy gap, VCSELs emitting at ~980nm enables the fabrication of flip-chip geometries without the need for substrate removal.

Due to an epitaxial growth error, the Novalux 980nm VCSEL structures 8.50/5, 6 and 9 have two sequential, high-index $\lambda/4$ layers (a $\lambda/4$ of $Al_{0.08}Ga_{0.92}As$ followed by a

λ/4 of GaAs) as the final layers. The two layers act as a λ/2 absentee layer, which means that the p-DBR mistakenly ends on a low index layer. The p-DBR reflectance is only 97.80% instead of 99.0%. Although this problem could have been fixed by depositing an additional λ /4 layer of SiN_x on top of the current layer stack, this approach has not been used since the mask and process are not compatible. In designing the second generation mask, this issue was taken into consideration to fabricate working high-speed VCSELs out of these wafers, as will be explained later in this chapter.

4.3.2.1 Fabrication summary and testing

Despite the explained growth problem, one of the Novalux structures (NT3) was processed using the first generation mask design and fabrication process to fabricate the 980nm top-emitting VCSELs up to the point after depositing the bottom contact.

The fabrication process began by depositing a 2500 Å of SiN_x before patterning the top contact resist and etching it back completely after applying the top contact resist. After the formation of an annular *p*-type contact by evaporating Ti-Au-Ni-Au with thicknesses of (200-1000/500/1000)Å, mesas were etched to a depth of about 5μm using the *p*-contact as a self-aligned etch mask. Next, the sample was wet-oxidized, resulting in the oxide extending in 9μm from the mesa sidewall. The bottom *n*-type contact of Ge-Au-Ni-Au with thicknesses of (330/670/200/500)Å were evaporated onto the partially etched bottom mirror. No further processing for the sample was possible.

The VCSELs L-I-V plots for a 24μm and 28μm mesa diameter with a 6μm and 10μm oxide aperture are presented in Figure 4.14. The threshold current, threshold voltage, series resistance, and slope efficiency for the 6μm oxide aperture device were

0.75mA, 1.4V, 96Ω, and 25%, respectively, and for the 10μm oxide aperture device were 1.1mA, 1.7V, 78Ω, and about 25%, respectively. Based on these DC characteristics, the devices seemed to work fairly well without the need of a SiN_x layer to increase the top *p*-DBR mirror reflectivity from 97.8% to ~99% as mentioned in Table 4.1. One of the conditions for reaching the lasing threshold is to have $g_{th}=\alpha_{i+}\alpha_m$, where g_{th} is the optical gain, α_m is the mirror loss, and α_i is the internal (distributed) loss, which represents mainly the diffraction losses and the free carrier absorption losses due to the DBRs doping [1,25]. Since the growth error resulted in a higher value for α_m than the one originally designed for a given g_{th}, either α_i for these devices is lower than estimated or the quantum wells were heavily pumped to reach a higher g_{th} due to a higher α_m.

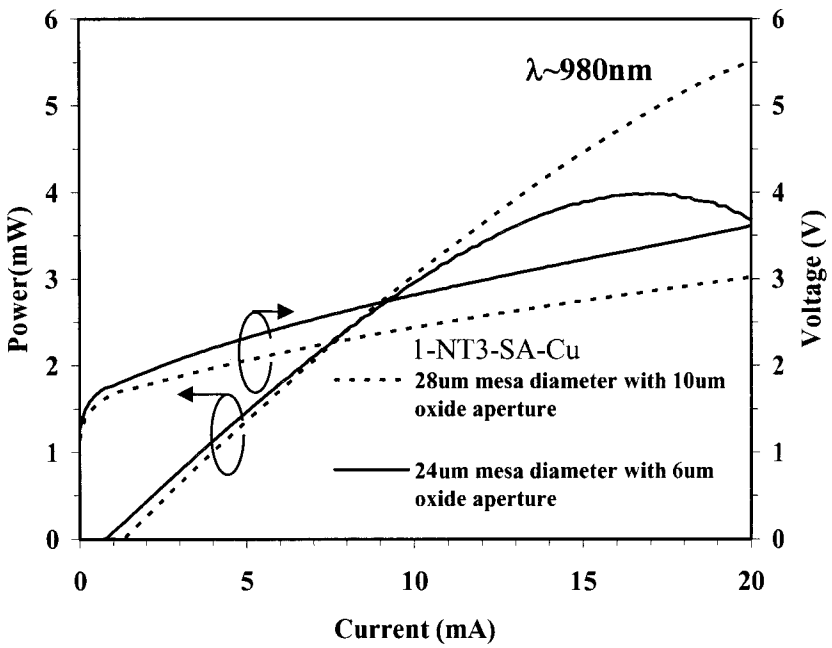


Figure 4.14 CW L-I-V for a top-emitting 980nm VCSELs with a self-aligned contact (1-NT3-SA-Cu).

4.3.3 Top-emitting 980nm VCSELs with a self-aligned contact and copper-plated heatsink (1-NT4-SA-Cu, 1-NT5-SA-Cu, and 1-NT6-SA-Cu)

During the preliminary investigation of the three wafers, using the SEM, no high Al layer (oxidation layer) was observed in samples NT4 and NT5. So a decision was made to only fabricate and test the NT6 sample 1-NT6-SA-Cu.

4.3.3.1 Fabrication summary

Device fabrication began with the formation of an annular *p*-type contact by depositing 1000Å of Cr. Although Ti-Au-Ni-Au was used as a top contact for the devices fabricated in Section 4.3.2, Cr was used this time due to its good performance as a mask for dry etching processes. It is easier to evaporate than Ni and Au, less time-consuming since it is only one layer compared to four layers used in the previous section, and much cheaper than Au. Next, mesas were etched to a depth of about 4.5μm using the *p*-contact as a self-aligned etch mask. After that, the sample was wet-oxidized in a 400°C steam environment resulting in an oxidation length of 6μm extending in from the mesa sidewall. AuGe-Ni-Au with thicknesses of (500/200/1000)Å was evaporated to form the bottom *n*-type contact. After contact formation, 1000 Å of PECVD SiN_x was deposited and vias were etched for the metal contacts. Next, the VCSEL was planarized. Finally, the sample was electroplated with ~2μm of Cu.

4.3.3.2 Measurements and discussion

The DC and AC measurements were carried out using the setups described in Sections 4.2.1 and 4.2.2, respectively. Figure 4.15 below shows the CW L-I-V

characteristics of a 30μm mesa diameter with a 18μm active diameter and a 22μm mesa diameter with a 10μm active diameter.

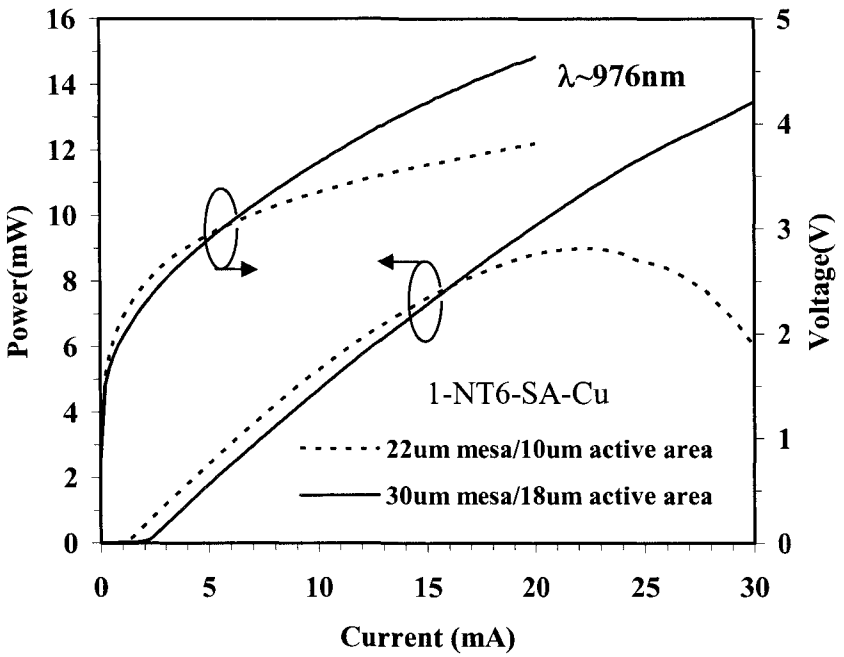


Figure 4.15 CW L-I-V for top-emitting self-aligned Cu-plated 980nm VCSELs (1-NT6-SA-Cu).

The threshold voltages of the devices reported in this section are higher than those for the devices reported in Section 4.3.2. To shed some light on possible causes for such an increase, Table 4.4 below summarizes some of the fabrication steps and DC characteristics for devices with a 10μm active area diameter.

Table 4.4 Summary of some of the fabrication steps and DC characteristics.

	VCSELs from Section 4.3.2 1-NT3-SA-Cu	VCSELs from current section 1-NT6-SA-Cu
Etching depth (μm)	4.5	5
Top contact	Ti-Au-Ni-Au	Cr
Bottom contact	Ge-Au-Ni-Au	$AuGe_{pre\text{-}alloyed}$-Ni-Au
Mesa diameter (μm)	28	22
Active diameter (μm)	10	10
I_{th} (mA)	~1	~1
V_{th}(V) at I_{th}	1.75	2.30

From the data listed in Table 4.4, the increase in the threshold voltage might be due to one or more of the following reasons:-

1. It is possible that the adhesion properties of Cr to the mesa top surface were not as good as those for the Ti. Also, Cr oxide might have been formed during the wet-oxidation process.
2. As for bottom contacts, devices with the lower V_{th} have the AuGe alloy formed by depositing Ge and Au separately and then have the annealing process form the alloy, while the devices with the higher V_{th} have a pre-alloyed AuGe deposited for the bottom contact. Furthermore, there might have been a metal contamination or metal crucible miss labeling as both pre- alloyed AuGe and BeAu which are used for *n*-type and *p*-type contacts respectively look visually similar.
3. The VCSELs with the higher V_{th} have a mesa diameter that is less than that for the lower V_{th} device by 4μm. Given that both VCSELs have the same active area diameter of 10μm, it is possible that the higher V_{th} is due to the smaller area available for the current to begin with before funneling into the 10μm active area diameter.

The modulation response of VCSELs with a range of diameters was measured for varying bias currents. Figure 4.16 shows the maximum frequency modulation response for 30μm, 22μm, and 16μm mesa diameter VCSELs with 18μm, 10μm, and 4μm oxide apertures, respectively. More of the devices' characteristics are listed in Table 4.5.
The smaller device exhibits lower threshold current and higher series resistance, which is expected. The observed maximum 3dB frequencies are relatively independent of aperture

size, which is an unexpected trend in contrast to previously reported results [4,26] and on results demonstrated later in this chapter using other epitaxial structures. Despite the fact that smaller devices suffer more from self-heating, still they are expected to exhibit higher modulation bandwidths compared to larger active area diameter devices since they have less parasitics to limit the bandwidth. It is possible that the unexpected AC results of this epitaxial structure are due to growth quality and design issues. This case is a good demonstration that a good mask design and fabrication process are not enough to demonstrate high-speed VCSELs; they need to be combined with good epitaxial structure optimized for high-speed operation.

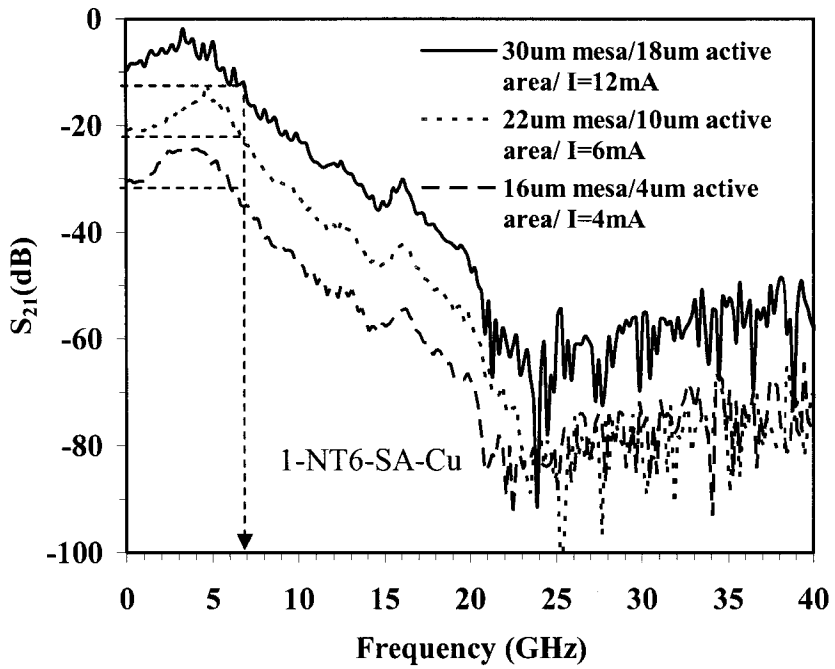


Figure 4.16 Modulation responses of different VCSELs sizes at bias current for maximum f_{3dB}.

Table 4.5 List of various VCSEL characteristics values.

Sample number	1-NT6-SA-Cu		
Mesa diameter(μm)	30	22	16
Aperture size(μm)	18	10	4
I_{th} (mA)	2	1.1	0.6
η_{slope} (%)	44	42	47
I_{bias}(mA) at f_{3dB} max	12	6	4
I_{bias}/I_{th} at f_{3dB} max	6	5.6	6.6
J_{bias} (kA/cm^2) at f_{3dB} max	4.72	7.64	31.85
$f_{3dB\ max}$(GHz)	7	7	6.6

4.3.4 Bottom-emitting flip-chip bonded 980nm VCSELs (1-NB1-NS-FB, 1-NB2-NS-FB, and 1-NB3-NS-FB)

Based on the calibration samples taken from the Novalux NB1, NB2 and NB3 wafers, it turns out that there was no high Al content layer. More details about the wafers, epitaxial structures are listed in Table 4.1. Only devices from wafer number NB2 were fabricated.

4.3.4.1 Fabrication summary

Bottom-emitting VCSEL fabrication began with the formation of cylindrical mesas with 6μm depth and different diameters. Next, the sample was wet-oxidized for 4 minutes at 380°C with water vapor temperature of 90°C and N_2 flow of 30sccm. The oxidation rate was a 0.75μm/minutes resulting in 3μm of oxide extending from the mesa sidewalls. Ti-Au with thicknesses of (200:1500)Å was deposited for the top *p*-type contact and Au-Ge-Ni-Au was evaporated with thicknesses of (330/670/200/500)Å for

the bottom *n*-type contact. Figure 3.41 represent an SEM image of the bottom-emitting VCSEL die after bottom contact deposition.

Heat spreaders were fabricated according to the process described in Section 3.5.3 to allow flip-chip bonding of the bottom-emitting VCSELs for heat-sinking and testing. To improve the adhesion of the seed layer and thus the plated metals to the GaAs substrate, the heat spreader fabrication process began with the removal of any oxide layer formed on the GaAs surface. Next, a Ti-Au seed layer with thicknesses of (200:1000)Å was deposited on the entire sample. After that, photoresist (AZ4400) with a thickness of ~7μm was patterned. Finally, the sample was electroplated with Cu and In with thicknesses of 3μm and 4μm, respectively, and the seed layer was sputtered. Figure 3.42 shows SEM image of the heat spreader. The insets show a bonding pad (a) before annealing, (b) after annealing. At this point of the process, the VCSEL die is ready to be flipped and bonded to the heat spreader, as shown in Figure 3.43. The flip-chip bonding process was done as described in Section 3.5.4 and the VCSEL die bonded to the heat spreader ready for characterization, as shown in Figure 3.45.

4.3.4.2 Measurements and discussion

As described in detail in Section 3.5.4, the initial characterization of the fabricated devices raised several issues regarding the current design that prevented the realization of operational flip-chip bottom-emitting VCSELs. As a result only DC testing was performed on the VCSEL die without flip-chip bonding, using the DC testing setup described earlier in this chapter.

Figures 4.17 and 4.18 show the CW L-I and I-V characteristics, respectively for 14, 16, 18, 20, 22, 24, 26, and 28μm mesa diameter VCSELs with 8, 10, 12, 14, 16, 18, and

20μm oxide apertures. The device with an 8μm oxide aperture exhibits a threshold current of 0.5mA, a series resistance of 228Ω, and a slope and wall plug efficiencies of 71% and 47%, respectively. The 71% is considered to be a good slope efficiency value as it means that 71% of the photons generated per radiative electron-hole recombination above threshold are emitted. As for the 47% wall plug efficiency, it is also considered a good value compared to a previously reported value of 50% [27]. Is should be noted that these efficiency values were obtained using responsivity values that were provided by the vendor for this model of photodiode but not for this specific photodiode, which might raise some concern about the accuracy for these numbers (i.e., the reported values might be higher or lower). Values for other device sizes are shown in Figures 4.17 and 4.18. Although there was no antireflection coating applied to the emitting side (substrate side), the L-I plots seem to be clean from the typical ripples (peaks/valleys) that usually appear in bottom-emitting VCSELs due to the substrate-air interface, which causes addition or subtraction from the field in the device cavity [1].

The VCSELs' series resistance values for the various device sizes are relatively high. This increase in device resistance is believed to be due to the fact that the processed epitaxial structure had no high Al content layer (oxidation layer), which resulted in a narrower path for the current. This promotes the devices' higher resistance, which follows the expression $R=\rho l/A$, where ρ is the combined top mirror resistivity, l is

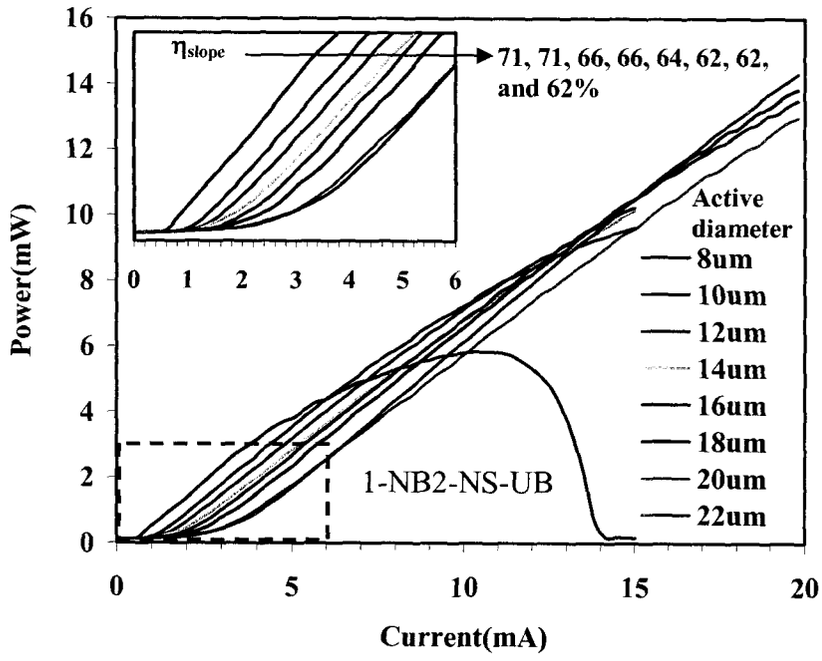


Figure 4.17 CW L-I characteristics for 980nm bottom-emitting unbonded VCSELs (1-NB2-NS-UB).

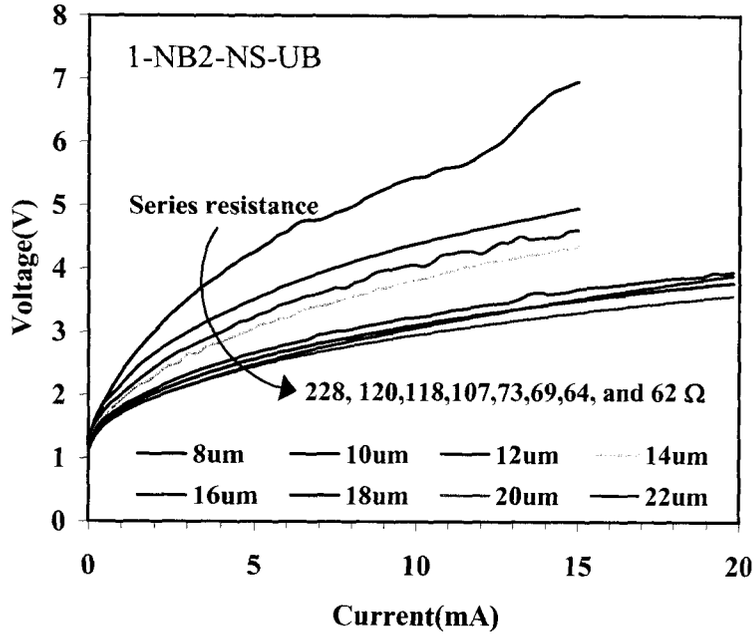


Figure 4.18 I-V characteristics for 980nm bottom-emitting unbonded VCSELs (1-NB2-NS-UB).

the current path length, and A is the cross-sectional area. This effect is illustrated in Figure 4.19, below showing the current case (left) and the typical case (right) where the arrows (red) show the current flow path. On the other hand, the fact that the current flows through a constant cross-sectional area path might help reduce the current crowding.

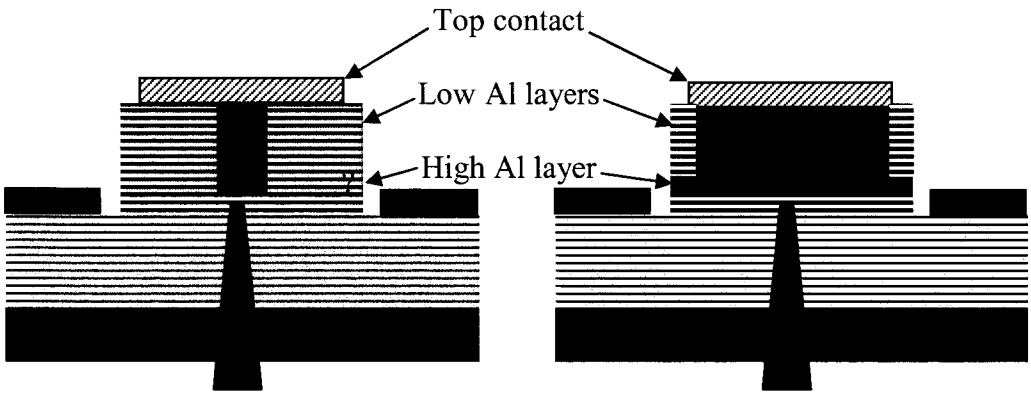


Figure 4.19 Novalux 8.54 structure with no oxidation layer (left) and typical VCSEL structure with an oxidation layer (right).

4.3.5 Equivalent circuit analysis: A case study for devices in Section 4.3.1

An equivalent circuit for the VCSEL impedance is useful for analysis of both bandwidth limitations of the laser and matching to driver circuits. The circuit model, shown in Figure 4.20, consists of elements corresponding to physical features of the VCSEL die. C_a is the aperture's junction capacitance; C_{o1} and C_{o2} represent the mesa regions with single and multiple oxidized layers, respectively, and C_p denotes the pad capacitance between the metal interconnect on the polyimide and the bottom *p*-mirror stack.

The pad and combined mesa capacitance values estimated from simple geometrical considerations are illustrated in Figure 4.20. C_{o1} and C_{o2} contain contributions from the series capacitance of the junction or other intervening depletion regions. The estimated

values of C_a, C_{o1} and C_{o2}, result in a combined total mesa capacitance of C_m=70 fF for an 18μm mesa diameter with a 10μm oxide aperture, which represents a 49% reduction in total mesa capacitance compared to the total mesa capacitance C_m=142.4 fF for VCSELs fabricated using a part of the same epitaxial wafer with a 28μm mesa diameter and a 7μm oxide aperture [4].

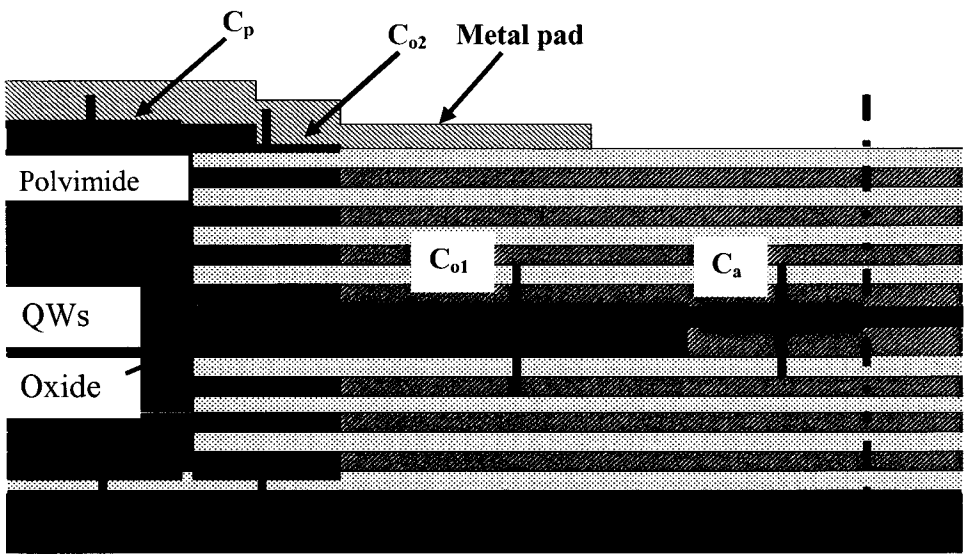


Figure 4.20 High-speed VCSEL cross-section.

The physical dimensions of the pad, as well as the polyimide thickness, were measured to calculate the pad capacitance C_p. The dimensions were measured using a scaled microscope and the polyimide thickness was measured using the α-step surface profilometer. The polyimide thickness (d) was measured to be about 5.5μm. The pad is shown in Figure 4.21 below.

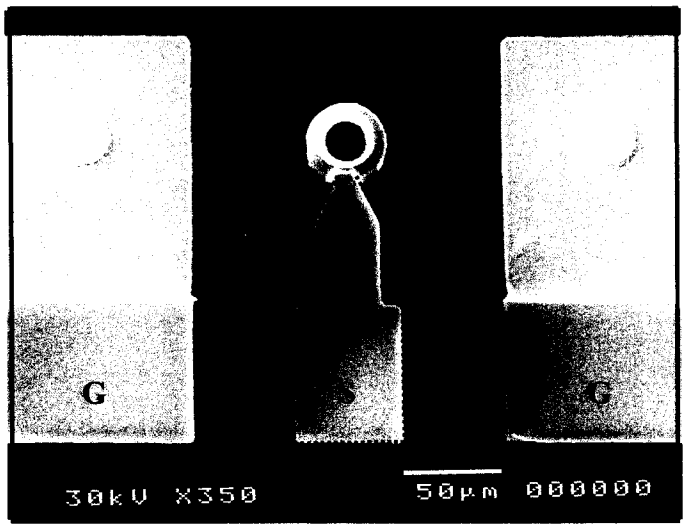


Figure 4.21 SEM photo of a VCSEL top view.

The pad capacitance can then be calculated using equation 4.3 shown below,

$$C_p = \frac{\varepsilon_o \varepsilon_r A_T}{d} \tag{4.3}$$

where ε_o is the free space permittivity (8.85×10^{-14} F/cm), ε_r is the relative dielectric constant (3.4 for HD-8000 polyimide at 1 kHz), A_T is the pad area (47.5×10^{-6}cm^2), and d is the polyimide thickness (5.5µm).

Substituting the corresponding values in equation 4.3, we get $C_p \sim 25$fF, which is 56% less than the pad capacitance value previously reported [4], where the use of the same polyimide with about 5.5µm thickness resulted in a pad capacitance value of C_p~56.9 fF [4]. Clearly, the reduction of the unnecessary pad area has its advantage in reducing the parasitic pad capacitance, but there is a limit on how small the pads can be.

The goal of their presence is to probe the devices under test easily and ultimately to wire-bond them for packaging.

Due to the overlap of the wrapped Au and plated Cu with the bottom (substrate) contact, which extends to about 5μm around the mesa and sandwiches a 1000 Å of SiN_x in between, a new parasitic capacitance that adds to the total pad capacitance exists. The horizontal and vertical parasitic capacitances (C_{wrap} h, C_{wrap} v), shown in Figure 4.22, were estimated using equation 4.3, where, ε_r=7.5 for SiN_x, A_T equals the horizontal overlap area of $3.9x10^{-6}cm^2$ for C_{wrap} h and the vertical overlap area of $3.1x10^{-7}cm^2$ for C_{wrap} v, and d is the SiN_x of 1000Å. As shown below, the combined C_{wrap} h, C_{wrap} v were found to be ~232fF for Au-wrapped and Cu-plated devices.

$$C_{wraph} = \frac{8.85 \cdot 10^{-14} \cdot 7.5 \cdot 3.9 \cdot 10^{-6}}{1000 \cdot 10^{-8}} \sim 222 fF$$

$$C_{wrapv} = \frac{8.85 \cdot 10^{-14} \cdot 7.5 \cdot 3.1 \cdot 10^{-7}}{1000 \cdot 10^{-8}} \sim 10 fF$$

As shown in Figure 4.23, PSpice simulation indicated that the purely electrical circuit effects would allow a maximum f_{3dB} of ~15.6GHz, which is very close to the measured value of the VCSELs' modulation bandwidth. It is believed that the Au-wrapped and the Cu-plated VCSELs are limited by electrical parasitics rather than thermal effects. A modified design that allows Au and Cu to extend only 2μm around the mesa is expected to have a modulation frequency of 63GHz while maintaining significantly reduced thermal resistance, as predicted by the PSpice simulation.

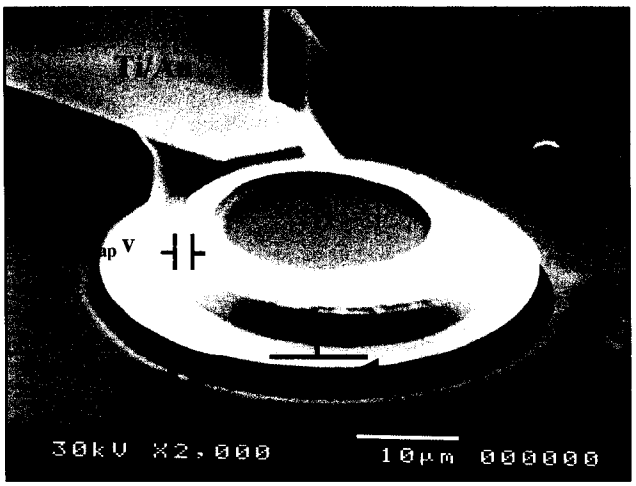


Figure 4.22 Au-wrapped VCSEL showing the horizontal and vertical parasitic.

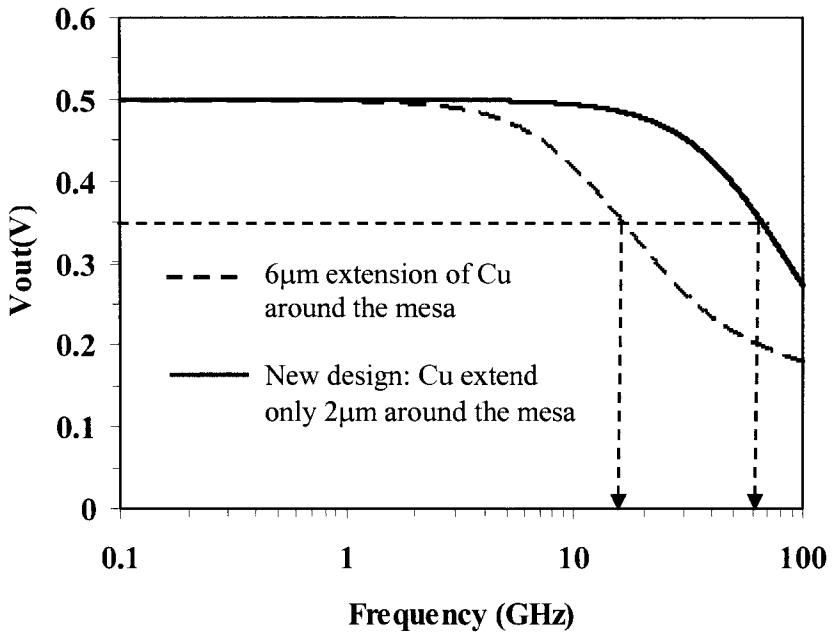


Figure 4.23 PSpice simulations for 6µm and 2µm of Cu extension.

4.3.6 Summary and conclusions

In summary, VCSELs with a self-aligned top contact and copper-plated heatsink were fabricated and characterized. We have demonstrated the effect of a heat-sinking layer on the performance of high-speed VCSELs. Au-wrapped and Cu-plated heat-

spreading layers reduced the thermal resistance by 25% and 44%, respectively, and output power was increased by 17% and 38%, respectively.

To further reduce the VCSELs' thermal resistance and thus improve their bandwidth, the quality of the electroplated copper was investigated in terms of the plated Cu adhesion to the seed layer and plated Cu density. During device testing, it was noticed that the plated Cu does not stick to the seed layer as illustrated in Figure 4.24 (left). Furthermore, a closer look at the quality of the initial Cu electroplated layer shown in Figure 4.24 (right) shows a low density Cu-plated layer that will not be a good heat sink as the higher-density Cu-plated layer. It is possible that the seed layer has an oxide layer that results in weak adhesion. As for the plated layer's roughness and density, it might be due to the current density values used. To improve the quality of the plated Cu, a different electroplating setup with a different electroplating chemical was used, as described in detail in Section 3.3.1.8. Improvements in the adhesion, quality, and density, of the electroplated copper resulted in further reduction in thermal resistance, as demonstrated by the second generation of the mask layout and fabrication process described later in this chapter.

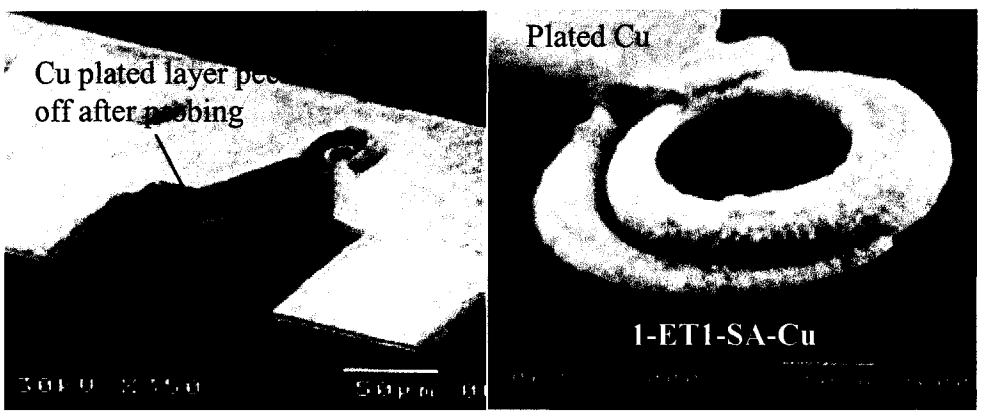


Figure 4.24 An SEM photo showing an 18μm device after testing, where the Cu-plated layer peeled off the signal pad after probing.

A closer look at the I-V data for VCSELs fabricated from different epitaxial material showed high voltage values whether at the threshold current or at the extrapolated zero current intercept on the voltage axis. Furthermore, values of the series resistance (I-V slope) also exhibited high resistance values. This issue motivated a contact resistance study, which will be discussed next before presenting the results of the second generation devices.

4.3.7 Ohmic contact resistance: A case study for Ti-Pd-Ti-Au-Ti-Pd and Ti-Ni-Ti-Ni metal systems

The contact resistance is defined as the resistance associated with an ohmic metal to the semiconductor junction. More detailed discussion of the ohmic contact resistance and its physics are discussed elsewhere [28]. In cases where the surface of the semiconductor, in this case GaAs, is heavily doped ($1x10^{19}cm^{-3}$), most metals will result in an ohmic contact when deposited on the GaAs surface. Ideally, the specific contact resistance should be in the range of $(10^{-5}\text{-}10^{-7})\Omega\text{-cm}^2$ and the contact should have a linear I-V curve.

Different test structures (models) such as the linear transmission line model (TLM), the circular transmission line model (CTLM), and the cross-bridge Kelvin model (CBKM) have been used to measure the specific contact resistance [28]. In the present study, the TLM structure shown in Figure 4.25, which consists of differently spaced rectangular-shaped contacts with $(50x100)\mu m^2$ area, have been used. The numbers shown in Figure 4.25 (2, 4, 8, 10, and 20) represent the spacing between the adjacent contacts in microns. Typically, the TLM or any other model of choice is incorporated within the

mask design. In other words, the model will be fabricated at the same time the devices are.

The resistance between the two contacts A and B shown in Figure 4.25 consists of the contact resistances of contacts A and B and the resistance of the GaAs in between. The total resistance between contact A and B is [28],

$$R = 2R_{contact} + \left(\frac{R_{sheet}}{W}\right) \cdot L \tag{4.4}$$

where $R_{contact}$ is the total resistance of contact A or the identical contact B, R_{sheet} is the GaAs sheet resistance, L is the spacing between contacts, and W is the contact width. A plot of the measured resistance vs. L will result in a straight line that has a slope of (R_{sheet}/W) and intercepts the R axis (y-axis) at $2R_{contact}$. The intercept of equation 4.4 with the L axis (x-axis), $-L_x$, is related to the transfer length L_t [28] by,

$$L_x = \frac{2R_{contact}W}{R_{sheet}} = \frac{2R_{sheet}L_t}{R_{sheet\perp}} \tag{4.5}$$

where $R_{sheet\perp}$ is the sheet resistance of the GaAs right underneath the contacts. Assuming $R_{sheet\perp} = R_{sheet}$, we get $L_t = 0.5L_x$. Given $(R_{sheet}/W) = slope$ of R vs. L equation 4.4, for the TLM model the specific contact resistance (r_c) can be calculated using

$$r_c = R_{sheet}L_t^2 = slope \cdot W \cdot \left(\frac{L_x}{2}\right)^2 \tag{4.6}$$

Figure 4.25 TLM model with a (50x100) μm^2 contact area and 2, 4, 8, 10, and 20μm spacing.

Two different contact systems have been used in this study. After photoresist patterning, Ti-Pd-Ti-Au-Ti-Pd with thicknesses of (200/500/200/1000/200/1000)Å and Ti-Ni-Ti-Ni ($TiNi^2$) with thicknesses of (100/700/100/700)Å were evaporated on two samples from a 2" heavily doped *p*-type wafer. Next, each sample was cleaved into smaller pieces and each piece went though different treatments (annealing, etching using a photoresist mask that covers all of the contacts such as those shown in Figure 4.25, and oxidation) and then its contact resistance was measured using the 4-probe measurement setup shown in Figure 4.26 below. Table 4.6 below shows the combination of the different treatments the samples went through. The column order reflects the treatment order. Although more different treatment combinations are possible, only the treatment combinations that resemble the actual process of VCSEL fabrication have been adopted.

Using the setup shown in Figure 4.26, Channel 1 of the HP 4145A provided current that flowed between the two probed contacts while Channel 2 measured the voltage drop caused by the current flow. From the measured I and V values, the measured resistance values for different contact spacing were calculated ($R_{Lx}=I_{Lx}/V_{Lx}$). The next step was to plot the measured resistance versus the corresponding contact spacing and fit that with a

straight line that yields R_{sheet}, $R_{contact}$, and L_t, as shown in Figure 4.27, which represents the data for the $TiNi^2$ metal system that was annealed and etched.

Table 4.6 The combination of the different treatments the samples went through.

Contact	As deposited [a]	Annealed [b]	Etched [c]	Oxidized [d]
	✓			
Ti-Pd-Ti-Au-Ti-Pd	✓		✓	
	✓		✓	✓
(200/500/200/1000/200/1000) Å		✓		
		✓	✓	
		✓	✓	✓
	✓			
	✓		✓	
Ti-Ni-Ti-Ni	✓		✓	✓
		✓		
(100/700/100/700) Å		✓	✓	
		✓	✓	✓

a: after lift-off
b: annealed at 420°C for 30 seconds in N_2
c: etched for 2 minutes using the setup and process parameters shown in Figure 3.13. visually, both contacts showed good resistance to dry etching.
d: oxidized for 20 minutes at 400°C the setup and process parameters shown in Figure 3.15.

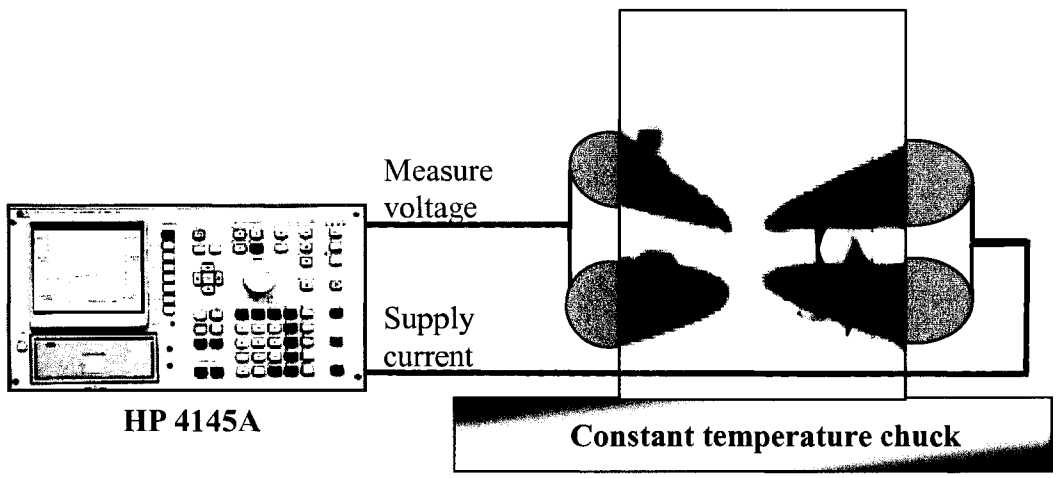


Figure 4.26 TLM 4-probe contact resistance measurements setup.

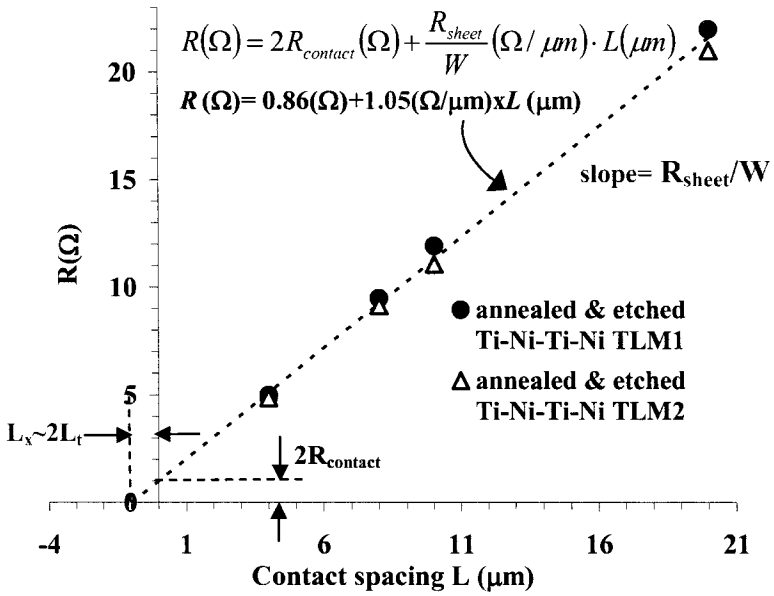


Figure 4.27 Measured resistances as a function of the contact spacing for the TLM pattern shown in Figure 4.25.

The specific contact resistance was calculated using equation 4.6. From the plot above $2R_{contact}$=0.86Ω, *slope*=1.05Ω/μm, and L_x= 1.1μm. Substituting these values in equation 4.6 resulted in a specific contact resistance of r_c~2x10^{-7}Ω-cm^2, which is within the typical values previously reported [28]. Figures 4.28 and 4.29 below show the specific contact resistances using different treatments for the Ti-Pd-Ti-Au-Ti-Pd and TiNi^2 metal systems, respectively. Figure 4.30 shows the specific contact resistances for annealed Ti-Pd-Ti-Au-Ti-Pd and TiNi^2 ohmic contacts.

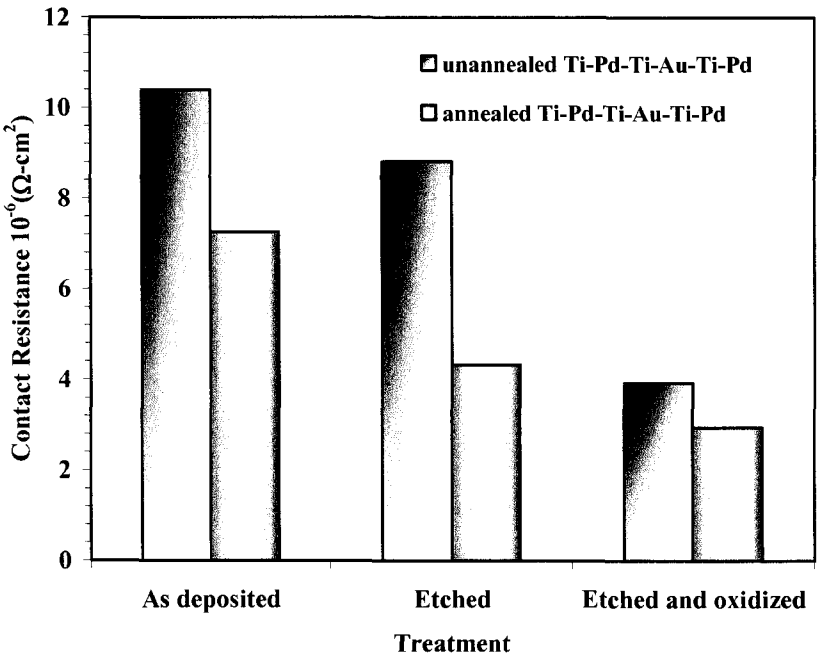


Figure 4.28 Specific contact resistances for Ti-Pd-Ti-Au-Ti-Pd.

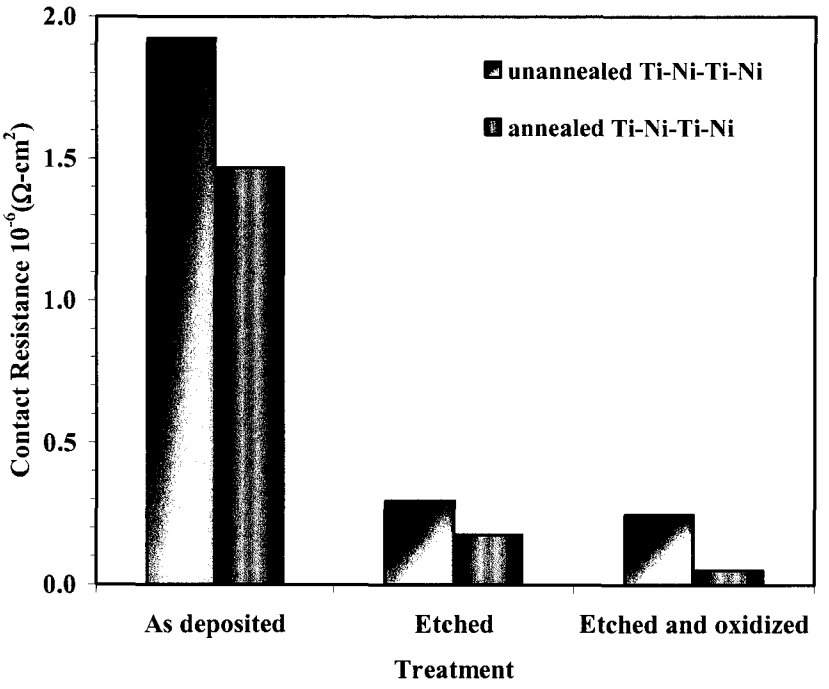


Figure 4.29 Specific contact resistances for $TiNi^2$.

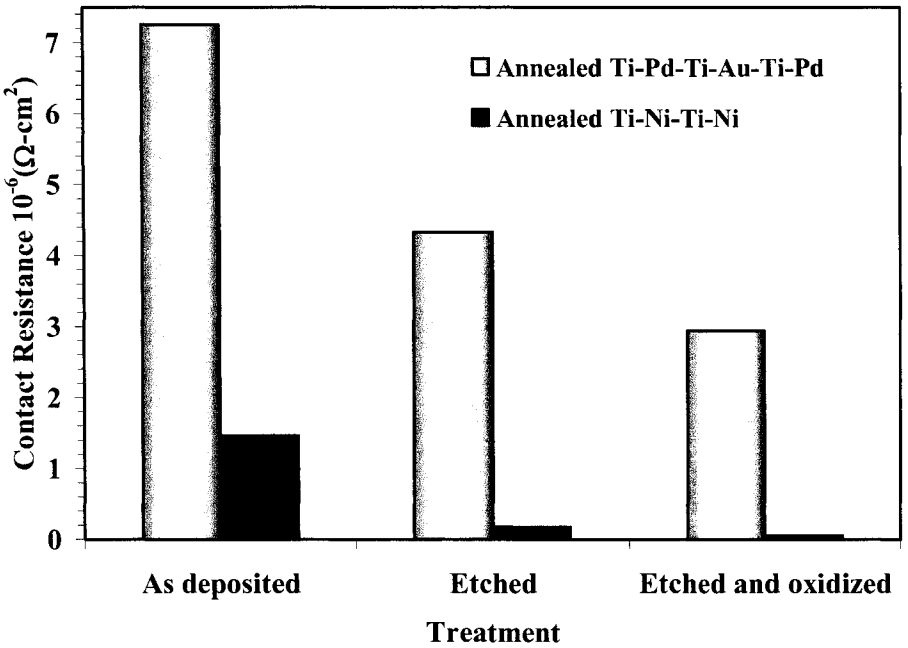


Figure 4.30 Specific contact resistances for the annealed metal systems $TiNi^2$ and Ti-Pd-Ti-Au-Ti-Pd.

Etched contacts resulted in a lower specific contact resistance compared to unetched contacts, which is not expected since etching made the TLM structure sits on a rectangular island of semiconductor material, which reduced any possible paths for current to flow between the two adjacent pads other than the horizontal path. One possible explanation for this decrease in resistance is that during the dry etching process sample temperature increases which might have annealed the contacts. While the $TiNi^2$ metal system demonstrated a lower specific contact resistance compared to the Ti-Pd-Ti-Au-Ti-Pd metal system, both systems are good candidates to be used. Based on the measurements made and the characterization equipment used, the fact that the specific contact resistance for one system is lower than the other can not be definitively explained, but reasonable explanations can be made. For example, minor variations in the TLM pad spacing, irregular edges, and defects can affect the accuracy. This being said, in

the present study the spacing between the pads was not measured and the pads edges were not investigated. The spacing values used previously were taken from the mask gds file assuming that the same dimensions were printed on the photomask and reproduced on the testing wafer. Furthermore, the measured resistance values depend on the testing probe tips' placement and the applied pressure, which is very difficult to reproduce. Also, the 4- probe testing setup shown in Figure 4.26 has two grounds and current is free to choose to flow though affects the measurements.

The goal of this case study was to investigate whether the high threshold voltages measured for the fabricated VCSELs were caused by the use of bad metal contact systems. Based on this study, both metal systems are eliminated as a possible source for the VCSELs' threshold voltage increase. There are some differences between the VCSELs' contacts and the pads used to estimate the specific contact resistance that might result in high threshold voltages for VCSELs while still demonstrating low specific contact resistance for the TLM structure. The average VCSEL's top contact area represents only 3 to 5% of the $5x10^{-5}cm^2$ TLM pad area, which means that if 3 to 5% of the TLM pad is damaged during etching or oxidation, it is very likely to still result in good specific contact resistance. On the other hand, the damaged 3 to 5% of the TLM pad area represents a 100% damage of the VCSEL top contact. Furthermore, the annular VCSELs' top contact shape might play a role compared to the rectangular TLM pad shape.

Another possible source for such an increase in the VCSELs, threshold voltage is the type of doping used. For example, the use of proper modulation doping significantly

reduces the threshold voltage at 1kA/cm^2 of current density from 2.7V down to 1.5V, which is about 44% reduction in threshold voltage [25].

4.3.8 Effect of external heating on VCSELs resonance frequency and damping factor: A case study for top-emitting, self-aligned 980nm VCSELs (1-NT4-SA)

In an effort to develop more understanding of the factors affecting or limiting the VCSEL's modulation response, this section presents a preliminary study of the effect of external heating (stage heating) on VCSELs' resonance frequency (f_r) and damping factor (Γ). Due to the coupling between the small signal electron and photon densities, a resonance frequency exists because electrons and photons try to relax to their steady state values [1]. VCSELs exhibit large thermal impedances due to their small sizes and poor thermal conductivity of the Distributed Bragg Reflectors (DBR). The resultant high junction temperature is one of the factors that currently limit the frequency response of VCSEL technology. Such a temperature rise leads to lower f_r, which is believed to be a considerable contribution to the modulation bandwidth saturation. There have been a number of studies on the VCSELs f_r using the VCSELs' relative intensity noise (RIN) measurement [29-31], which is the noise spectrum of the device under DC bias conditions. Most have reported on the effect of the bias current on f_r. In this section of the present work, the impact of external heating source on the VCSELs' f_r and damping factor are examined by measuring the RIN spectrum at a fixed bias current and different stage temperatures.

4.3.8.1 Fabrication summary

Using a sample from wafer NT4, top-emitting, self aligned, oxide-confined, 980nm VCSEL fabrication began with the formation of an annular *p*-type contact by depositing Pd-Ti-Au-Ti-Pd with thicknesses of (500/200/1000/200/1000)Å. Next, mesas with 18 to 28μm diameter were dry-etched to a depth of about 5μm. After that, the sample was wet-oxidized in a 400°C steam environment using the Lindberg tube furnace (subsequently replaced with a CARBOLITE tube furnace) resulting in mesas with oxide aperture diameters ranging from 8 to 18μm. AuGe(12%)-Ni-Au with thicknesses of (500/250/1500) Å was evaporated to form the bottom *n*-type contact. Contacts were alloyed for 30 seconds at 440°C in N_2. Figure 4.31 shows an SEM photo for a VCSEL ready for testing.

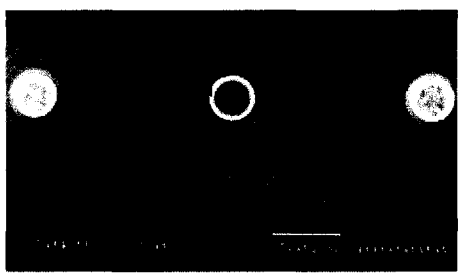


Figure 4.31 SEM image for a 1-NT4-SA VCSEL ready for testing.

4.3.8.2 Measurements and discussion

The L-I measurements were carried out using the setup described in Section 4.2.1. Figure 4.32 below shows the CW L-I characteristics of an 18μm mesa diameter with an 8μm aperture. The inset shows the wavelength spectrum at 2mA at which the RIN measurements were taken. The device exhibits a threshold current of 0.4mA, a maximum output power of 1.6mW at bias current 13 times I_{th}, and a slope efficiency of about 36%.

The relative intensity noise (RIN) of VCSELs at different stage temperatures was measured using the setup shown in Figure 4.33. The RIN measurement apparatus consisted of an Hp 8569B spectrum analyzer with 22GHz bandwidth, a high-speed Discovery Semiconductor DSC30S photodiode attached to a JSTD-02K200-40-10P amplifier with a 23dB gain and a 3.5dB noise figure amplifier followed by a JSMF4-02K190-35-10P amplifier with a 34dB gain and a 2.6dB noise figure MITEQ amplifier, a Keithley Source Meter model 2400, a probe station equipped with a temperature controlled (ILX-LDT-5910B) vacuum chuck and an LED illuminator, a JAVELIN CCD camera, a SONY 12" monitor, and Cascade Microtech air co-planar probes (ACP40) with GSG configuration, a 125μm pitch, and Be-Cu tips. The sample was mounted on the temperature controller chuck at 20°C and was aligned as described in Section 4.2.2.

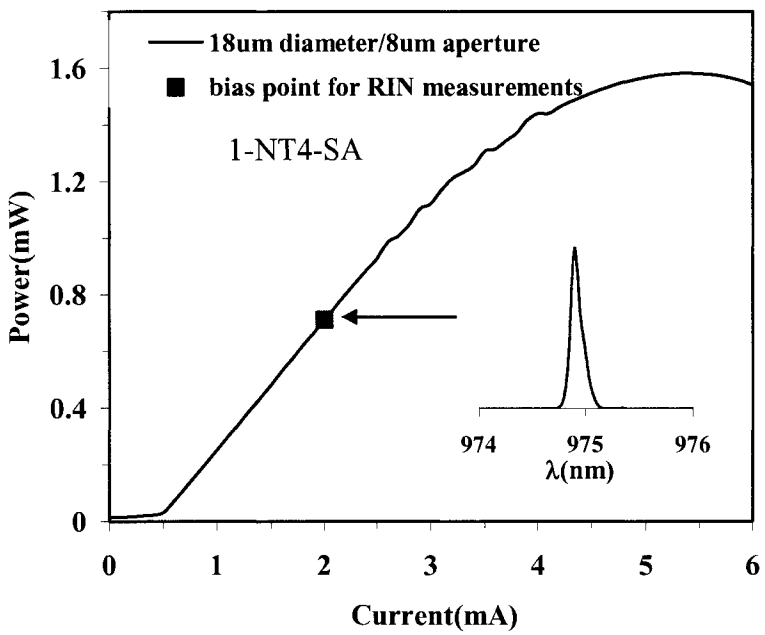


Figure 4.32 CW L-I characteristics of an 18μm mesa diameter with an 8μm active diameter. The inset shows the wavelength spectrum at 2mA of bias at which the RIN was measured.

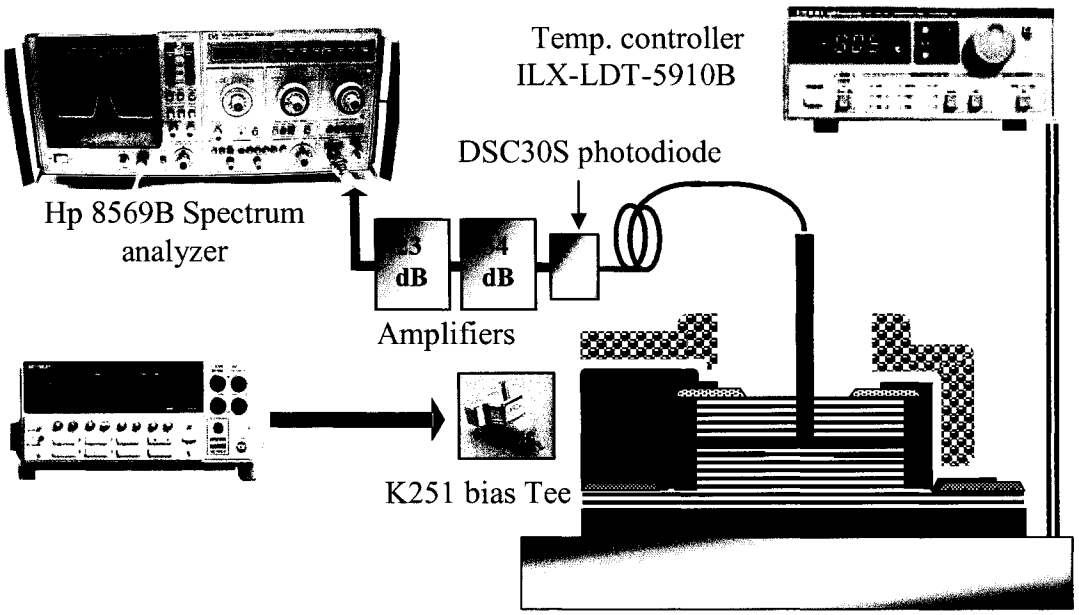


Figure 4.33 RIN measurement setup.

The RIN was measured for an 18μm mesa diameter VCSEL with an 8 μm oxide aperture at a bias current of 2mA at stage temperatures from 10°C to 60°C with a 10°C step. Figure 4.34 shows the measured RIN spectra at different stage temperatures, where the resonance peaks represent the resonance frequencies. Due to the Labview code null function, the y-axis of Figure 4.34 was not captured properly, but still the relative y-axis values between different curves are correct. Figure 4.35 shows the variation in f_r as a function of the stage temperature. As the stage temperature increases, the resonance frequency decreases. Decrease in resonance frequency due to internal heating is a possible mechanism for modulation bandwidth saturation. To further understand what might have caused f_r to decrease, we consider the following simple approximated expression for the resonance frequency [1,25],

$$f_r \approx \left(\frac{v_g a N_p}{4\pi^2 \tau_p} \right)^{\frac{1}{2}} \tag{4.7}$$

where v_g is the group velocity, a is the differential gain, τ_p is the photon lifetime, and N_p is the photon density. To cause f_r to decrease, external heating resulted in decreased N_p and possibly decreased a or increased τ_p, which is a function of the internal (cavity) loss (α_i) and mirror loss (α_m). To further investigate the reason(s) behind the decrease in N_p, the following equation, which is used to calculate N_p, is considered [1],

$$N_p = \frac{\eta_i (I - I_{th})}{q v_g g_{th} V} \tag{4.8}$$

where η_i is the internal efficiency, I is the bias current, I_{th} is the threshold current, q is the electron charge, g_{th} is the threshold gain, and V is the active region volume (volume occupied by electrons). Based on Equation 4.8, and since I is a constant bias current, to cause N_p to decrease, the external heating might have decreased η_i, increased I_{th}, or both.

The VCSEL's threshold current value is related to both the radiative and nonradiative recombination by the following equation for a single quantum well VCSEL [1],

$$I_{th} \cong \frac{qVBN_{tr}^2}{\eta_i} e^{\frac{2(\alpha_i + \alpha_m)}{\chi g_o}} + \frac{qVCN_{tr}^3}{\eta_i} e^{\frac{3(\alpha_i + \alpha_m)}{\chi g_o}} \tag{4.9}$$

where N_{tr} is the transparency value of electron density, χ is the confinement factor, B is the recombination coefficient, and C is the Auger coefficient. For Equation 4.9, the factors that have significant dependence on temperature are $N_{tr} \propto T$, $g_o \propto 1/T$, and $\alpha_i \propto T$. Going back to the resonance frequency experiment, as the stage temperature increased, N_{tr} increased and thus g_o decreased since the injected carriers are distributed over a wider energy range with temperature. The internal loss also increased due to the need of more carriers to reach threshold as the stage temperature increased. As a result, the increase in threshold current reduced the carriers available for recombination above threshold (i.e., the value of $I-I_{th}$ gets smaller), which reduced N_p, which decreased f_r.

According to [29], the damping factor can be extracted by fitting the measured RIN spectra with the theoretical form [29,30],

$$RIN(\omega) = \frac{A + B\omega^2}{(\omega^2 - \omega_r^2)^2 + \omega^2\Gamma^2} \tag{4.10}$$

where A and B are fitting parameters, ω_r is the resonance frequency ($\omega_r = 2\pi f_r$) and Γ is the damping factor. Figure 4.35 also shows the change in Γ as a function of the stage temperature. As the stage temperature increases Γ increases, which reduces the VCSELs' modulation bandwidth. The damping factor can be written as, $\Gamma = Kf_r^2 + \Gamma_o$, where K describes the damping of the response and Γ_o is the damping factor offset. Thus, the damping factor is proportional to the resonance frequency squared. So the decrease in Γ is related to the factors that caused the resonance frequency to decrease with increased

stage temperature, as discussed earlier. Further experiments related to the effect of heating on VCSELs' f_r and Γ are suggested in Chapter 6.

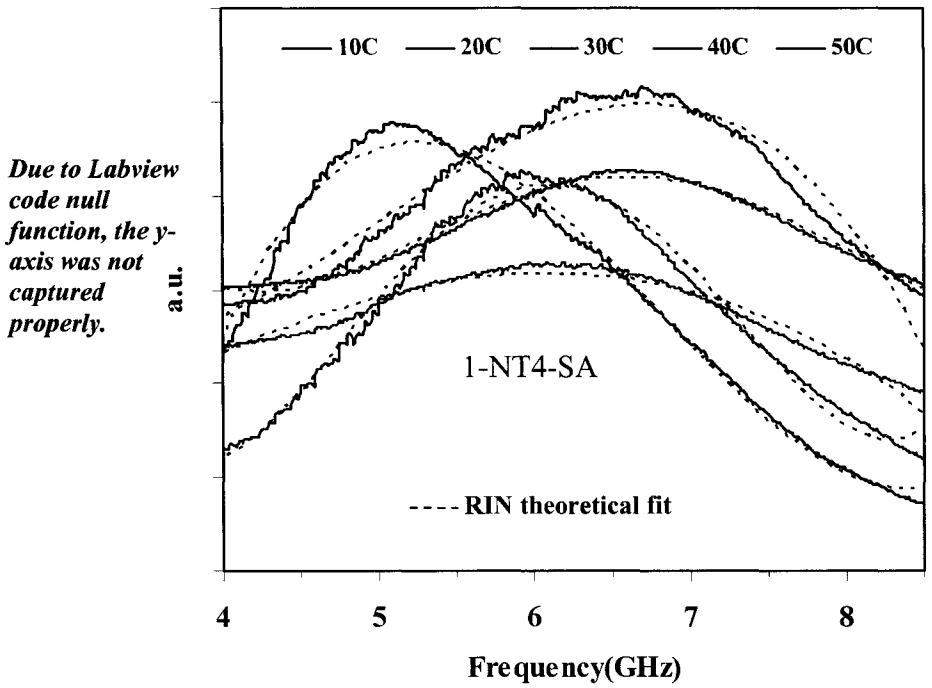


Figure 4.34 RIN spectra of the investigated 1-NT4-SA VCSEL under different stage temperatures.

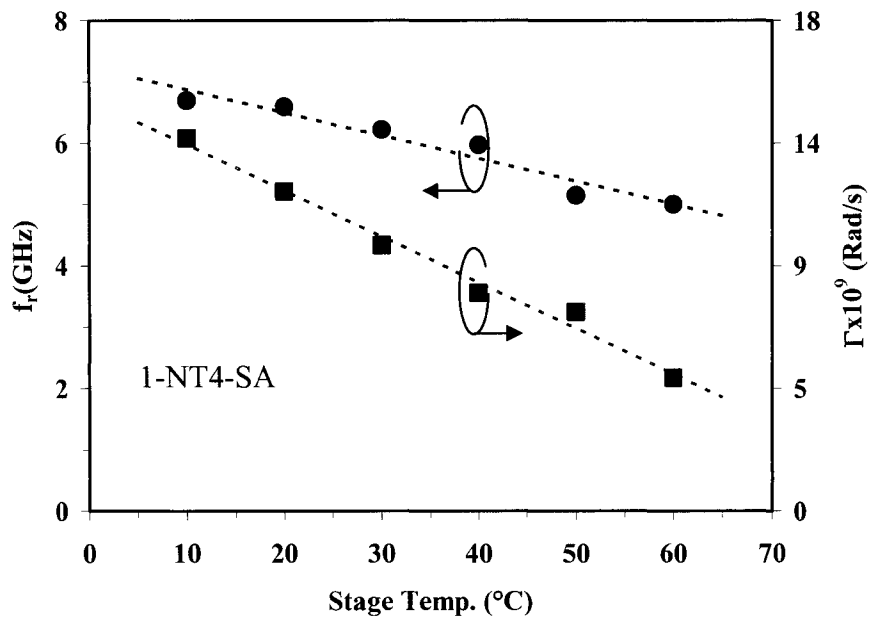


Figure 4.35 Relaxation oscillation frequency and damping as a function of the stage temperature.

Figure 4.36 below shows the damping as a function of the relaxation oscillation frequency squared at different stage temperatures. With $\Gamma = Kf_r^2 + \Gamma_o$ and ignoring Γ_o, we get $\Gamma \sim Kf_r^2$, which represents a straight line equation that can be fitted to the data points in Figure 4.36 with a slope of K. Best fitting yielded a K of 0.36ns. The maximum intrinsic 3dB frequency bandwidth can be estimated using $f_{3dB} = (2\pi\sqrt{2})/K$ [1,25,30], yielding an f_{3dB} of 24.7GHz. It should be noted that the expression $\Gamma \sim Kf_r^2$ has been developed and used previously to represent a straight line that can be fitted to the damping as a function of the relaxation oscillation frequency squared at different bias currents not at different stage temperatures as in this case. Further experiments that validate the use of $\Gamma \sim Kf_r^2$ to fit the data at different stage temperatures are suggested in Chapter 6.

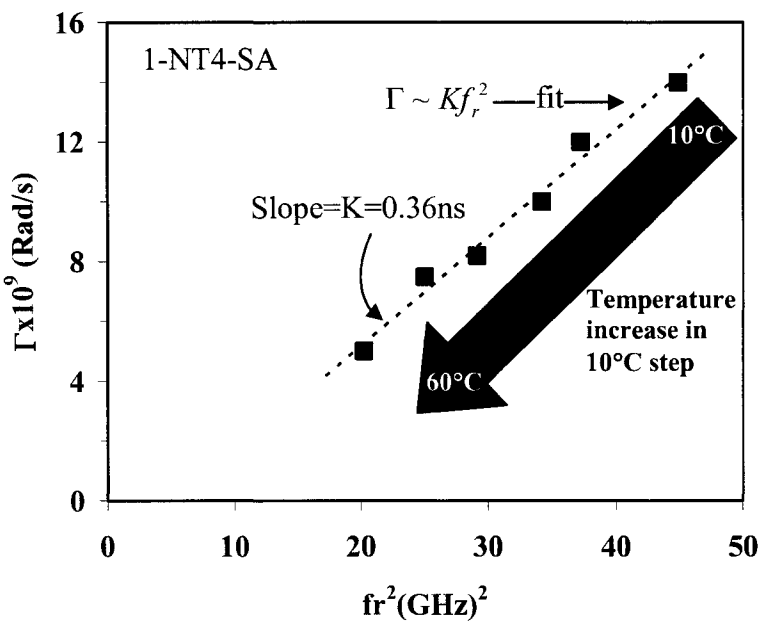


Figure 4.36 Damping versus the relaxation oscillation frequency squared at different stage temperatures.

4.4 Second generation VCSELs DC and AC testing and characterization results

Before presenting the DC and AC testing and characterization results for the second generation of VCSELs, below is a summary of the changes made to the mask layout design and fabrication process that were incorporated in the second generation of VCSEL fabrication.

- **Top-emitting VCSELs**
  1. The relief of device dimensions resulted in an easier fabrication process and working devices. For example, the width of the annular top contact in the first generation was 4μm. In the second generation, this width was increased to 7μm.
  2. The shrinkage of the polyimide during the curing process extended the gap between the mesa and the pads, which caused an open circuit break in interconnect metal during the lift-off between the testing pads and the mesa top contact. The second generation extended the polyimide to touch the mesa sidewalls and even hang at the edge of the mesa.
  3. Increasing the area of the annular top contact improved the IV characteristics of the devices. The old design had a 4μm difference between the outer and inner diameters of the contact. The new mask has a 7μm difference.
  4. The use of a new setup and chemicals (described in Chapter 3) for the Cu-electroplating process improved the plating density and adhesion.
- **Bottom-emitting VCSELs**
  1. Modify the ground mesa sidewalls for a better step coverage by incorporating polyimide in the process.

2. Protect the device junction from shorting due to the exposed device mesa sidewall to the plated In/Cu used for flip-chip bonding. This can be done using either polyimide or SiN_x.
3. The incorporation of polyimide as mentioned in 1 and 2 resulted in an easier bonding process that is less sensitive to the bonding parameters such as the plating thickness and the bonding force.
4. Due to the symmetry of the new design layout, errors due to the wrong orientation of the VCSEL die with respect to the heat spreader are easily avoided.

4.4.1 Low-thermal resistance, high-speed, non–self-aligned, top-emitting 980nm VCSELs (2-NT6-NS-Cu)

In the results in Section 4.3.1 (and published in [5]), evaporated Au and plated Cu heatsinks were used to reduce R_{th} of a 10μm diameter oxide aperture, top-emitting, 850nm devices to 2.0°C/mW and accordingly increase the bandwidth by up to 12% compared to separately fabricated samples without metal heatsinks [4]. This section reports a better controlled experiment using varying sizes of plated Cu heatsinks yielding much lower R_{th} to values 50% lower than those previously reported for top-emittng VCSELs over a range of device sizes. For example, R_{th} of a 9μm diameter oxide aperture, top-emitting, 980nm VCSEL was reduced to 1.0°C/mW, resulting in a 131% and 40% increase in output power and bandwidth, respectively. The lasers exhibit a 3dB modulation frequency bandwidth up to 9.8GHz at 10.5kA/cm^2. The functional

dependence of thermal resistance on oxide aperture diameter indicates the importance of lateral heat flow to mesa sidewalls. The results of this section were published in [32].

4.4.1.1 Fabrication summary

Top-emitting, high-speed, 980nm VCSELs were fabricated from the Novalux 8.59 wafer, whose structure is summarized in Table 4.1 and detailed below.

The active region contains three 80 Å InGaAs quantum wells centered on the anti-node of the 1-λ cavity with $GaAs_{0.955}P_{0.045}$ used for strain-balancing as 100 Å barriers between the wells and for the spacer material before and after the wells. The *p*-mirror above the active region employs a 17 period, C-doped $Al_{0.08}Ga_{0.92}As/Al_{0.95}Ga_{0.05}As$ DBR except for a single low index ~λ/4 layer adjacent to the cavity with 98% Al content. The *p*-DBR was terminated with a phase matching GaAs p^{++} ($2x10^{20}cm^{-3}$) contact layer. The 37 period *n*-mirror below the active region is Si-doped.

Non-self-aligned 980nm VCSELs were fabricated using a six photomask process sequence. First, 4μm deep cylindrical mesas 20μm to 36μm were formed by dry etching. Etching was terminated at the fourth mirror pair below the active region. To form oxide apertures, the sample was wet-oxidized for 8 minutes, resulting in the oxide extending in 8.5μm from the mesa sidewall, yielding oxide aperture diameters from 3μm to 19μm depending on mesa size. After oxidation, annular *p*-type contacts of Ti-Au with thicknesses of (200 /1500)Å were evaporated on top of the mesas after deoxidizing the surface. Immediately before depositing the bottom *n*-type contact, the contact region was deoxidized. AuGe (pre-alloyed 12% Ge by weight)-Ni-Au with thicknesses of (1000/300/500)Å were evaporated to form the *n*-type contact, which is electrically

connected to the substrate. Contacts were alloyed for 30 seconds at 440 °C in N_2.

A 1000Å of PECVD SiN_x was deposited and vias were etched for mesa sidewall isolation. HD-8000 positive tone polyimide was used for planarization [33]. The final processing step was to form electroplated Cu heatsinks of varying outer diameters over the mesas along with probe pads on the neighboring polyimide-covered regions. The use of Cu rather than Au was motivated by cost and thermal conductivity [5]. After depositing a seed layer of Ti-Au with thicknesses of (200/800)Å, approximately 2μm of Cu was plated directly on the seed layer in a Cu bath at room temperature and a current density of J~18 kA/cm^2. After stripping the photoresist, the seed layer was removed by etching back the Au and Ti using a commercial Au-etchant and buffered HF, respectively. Annular plated heatsinks with an outer radii of 0μm, 2μm, and 4μm greater than the mesa diameter, referred to as the heatsink overlap, were plated in adjacent positions (separated by 250μm) on the sample. Figure 4.37 (a) shows as SEM image for the devices ready for testing. Heatsinks with zero overlap did not cover the mesa sidewalls, as shown in Figure 4.37 (b), while ones with 2 and 4μm overlap covering the sidewall and a portion of the lower mirror surrounding the mesas are shown in Figure 4.37 (c) and (d). Figure 4.38 shows a cross-section of the device along AA' of Figure 4.37 (d).

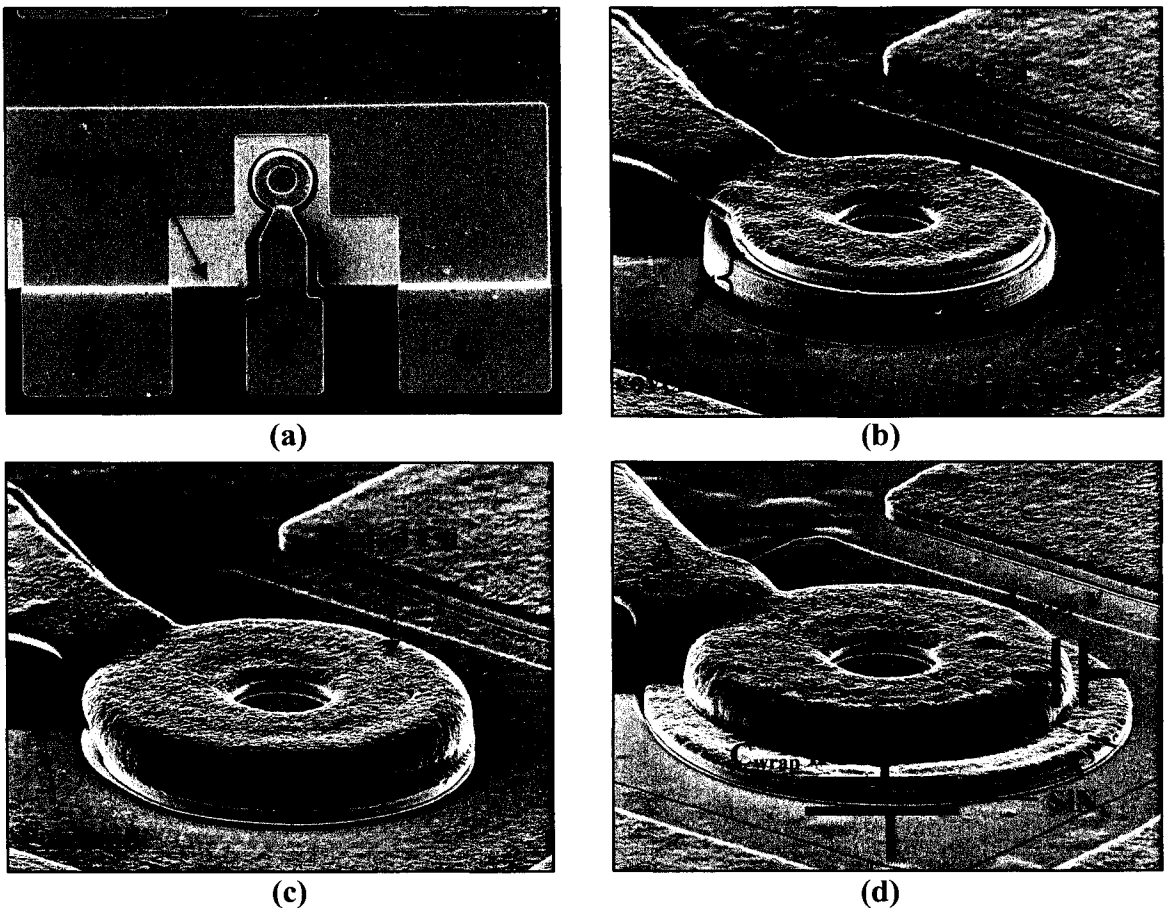


Figure 4.37 SEM images for (a) 2-NT6-NS-Cu VCSEL ready for testing, VCSEL mesas with (b) 0μm *(did not cover the mesa sidewalls)*, (c) 2μm, and (d) 4μm heatsink overlap.

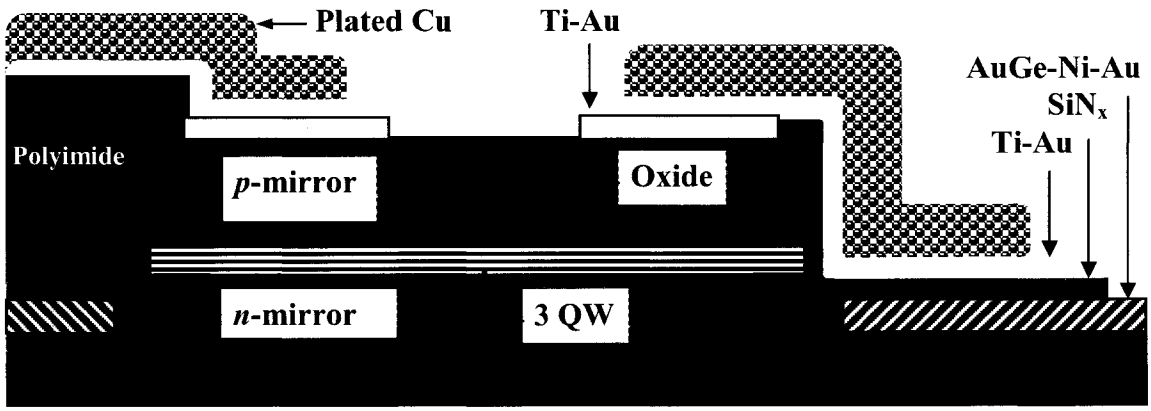


Figure 4.38 A cross-section of the 2-NT6-NS-Cu device along AA' of Figure 3.37 (d).

4.4.1.2 Measurements and discussion

Room temperature DC characterization of completed VCSELs with varying heatsink overlaps for oxide aperture diameters from 7μm to 5μm showed that increased heatsink overlap significantly reduces R_{th} and increases maximum output power for all sizes. Figure 4.39 compares the CW *L-I*-V characteristics of two VCSELs with heatsink overlaps of 0μm and 4μm, where both had identical mesas diameters of 26μm and oxide aperture diameters of 9μm. The I-V characteristics of the two devices are essentially identical, indicating a minimal thermal impact on the 72Ω series resistance. To our knowledge, the 131% increase in the maximum power output is the highest ever reported as a result of improved heatsinking. Previous publications presented improvements in VCSEL maximum output power of 60%, accomplished by plating 8.5μm of Au on the 120x120μm^2 pads around 8μm pillars [9]; and of 107% by attaching 20μm diameter

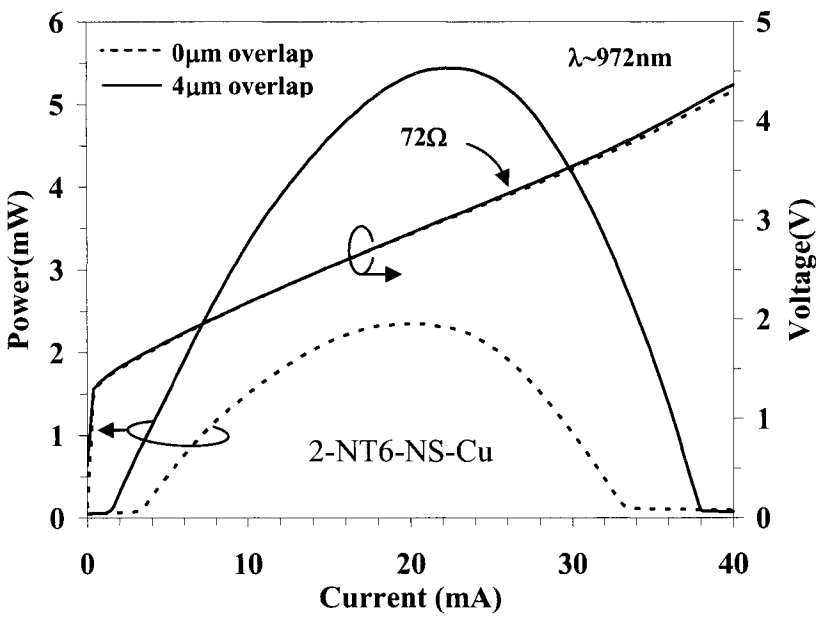


Figure 4.39 CW *L-I-V* characteristics for a 2-NT6-NS-Cu 26μm mesa diameter VCSEL with a 9μm oxide-aperture diameter.

VCSELs to a Cu substrate after GaAs substrate removal, resulting in a 20% reduction in R_{th} [10]. VCSELs with 0μm and 4μm overlap exhibited slope efficiencies of 0.26W/A and 0.44W/A, respectively, which is about a 69% improvement. Since the structure used in this section is the same structure used to fabricate devices in Section 4.3.3, it will be of benefit to summarize some of the fabrication steps and DC characteristics for comparison, as shown in Table 4.7.

Table 4.7 Summary of some of the fabrication steps and DC characteristics results for samples from Sections 4.3.3 and 4.4.1.

	VCSELs from current section 2-NT6-NS-Cu	VCSELs from Section 4.3.3 1-NT6-SA-Cu
Etching depth (μm)	4	5
Top contact	Ti-Au	Cr
Bottom contact	$AuGe_{pre\text{-}alloyed}$-Ni-Au	$AuGe_{pre\text{-}alloyed}$-Ni-Au
Plating setup: Section 3.3.1.8	Figure 3.27	Figure 3.31
Mesa diameter (μm)	26	24
Active diameter (μm)	9	10
I_{th} (mA)	~1	~1
V_{th}(V) at I_{th}	1.45	2.30
I-V shape	Linear with a constant slope of 72Ω	Curved with a continuously changing slope (i.e. resistance).

The observed dependence of R_{th} on device size with and without sidewall heatsinking further illuminates the role of lateral heat flow in VCSELs. Using $\delta N/\delta T \sim 0.07 nm/K$ [1,7], R_{th} of the devices was determined for a range of device diameters. Figure 4.40 shows R_{th} as a function of the active diameter (blue). Extension of the heatsink over the mesa sidewalls reduces R_{th} by approximately 20% for a range of device sizes, comparable to the more complex process in [10]. For active diameters greater than 7μm, the Cu-plated heatsinks with 2μm overlap gave a 50% reduction in R_{th} compared to the best known previously published results. Figure 4.40 also summarizes other reported

R_{th} of VCSELs that were fabricated using various techniques [4, 7-14] and shows the amount of improvement achieved in lowering the devices' R_{th}. The measured size dependence of R_{th} with and without overlap approximately follows the simple analytical estimation shown in Equation 4.1. Although the sample structure is significantly more complicated than the idealized disc geometry, the good fit motivates parameterization using ξ to allow comparison of various sized devices. Using a best fit to our data, we obtain ξ =0.41W/cm.K and 0.53W/cm.K for 0μm and 2μm of Cu-plated overlap, respectively. The difference in the effective thermal conductivities indicates sidewall heatsinks increase lateral heat flow since the thermal resistance of the VCSEL mirror stacks is anisotropic [34]. Thus, with sufficient heatsink overlap on the substrate and sidewall

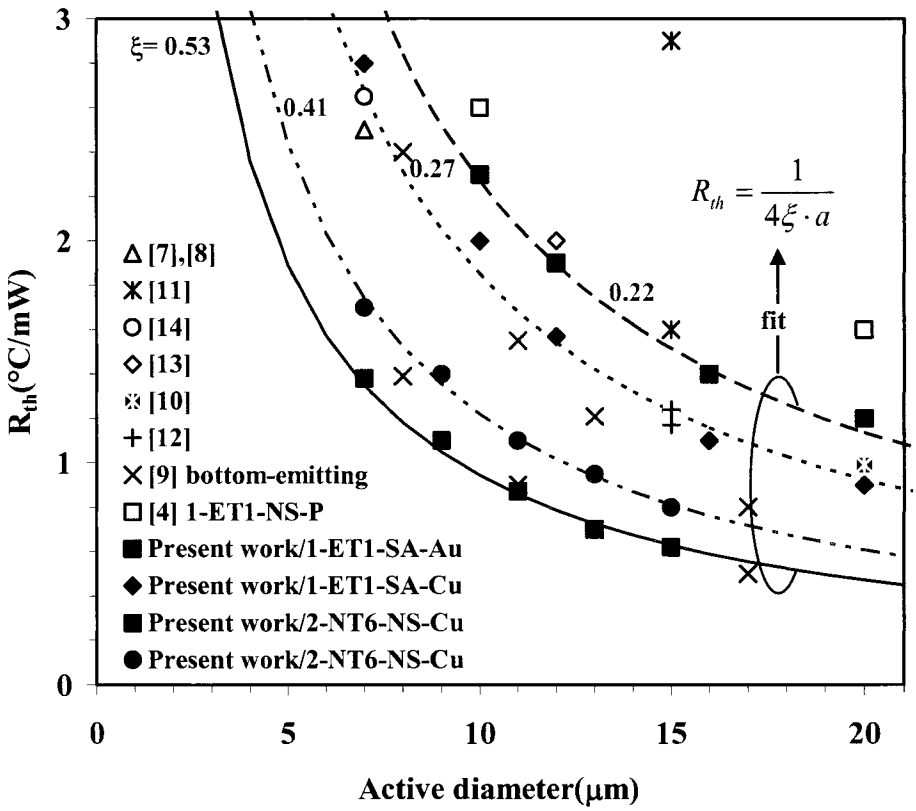


Figure 4.40 VCSELs' thermal resistance as a function of the active diameter.

heatsinking, more heat flows laterally through the mirrors to the Cu-plated sidewalls and from there into the substrate via the heatsink overlap rather than going through the bottom mirror to the substrate.

In addition to the improvement in DC and thermal properties, the increased heatsink overlap also significantly improves VCSEL bandwidth. Frequency response was measured on wafers using the same apparatus described in Section 4.2.2 [5]. The modulation response for a 9μmVCSEL with 4μm heatsink at different bias currents is shown in Figure 4.41 below. When biased at I_b=6.7mA, the VCSEL exhibits a maximum 3dB bandwidth of 9.8GHz. Figure 4.42 below shows the VCSEL 3dB bandwidth as a function of the square root of the current above threshold. As shown in Figure 4.42, the 4μm overlap increased the 3dB bandwidths by 40% in comparison to zero overlap heatsinks.

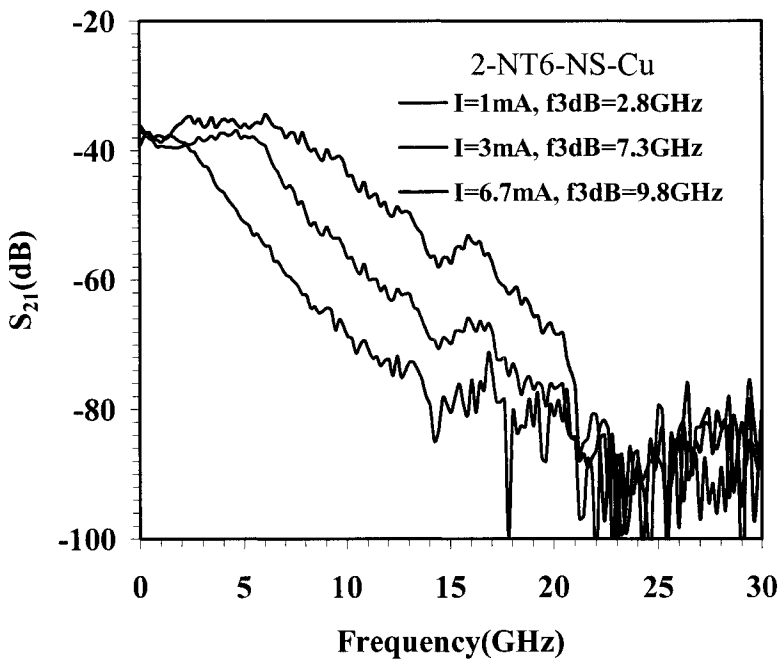


Figure 4.41 Modulation response for a 2-NT6-NS-Cu 9μmVCSEL with 4μm heatsink at different bias currents.

The increase in bandwidth due to sidewall heatsinking for the 980nm lasers reported here is much larger than the previously reported 12% increase in the 3dB bandwidths for similar λ=850nm devices with and without Cu heatsinks presented in Section 4.3.1 and published in [5]. The Cu-plating in that case is believed to have suffered from quality, density, and adhesion issues. Since higher current densities increase the internal temperature of the devices and otherwise accelerate device degradation independent of junction temperature, the low bias current densities, such as 10.5kA/cm^2 necessary for the 9.8GHz bandwidth in the 9μm diameter device, is expected to improve device reliability [15]. Previously published VCSEL modulation bandwidths of 8.5 [35] and 9.75GHz [22] required bias current densities of 10.5kA/cm^2 and 20kA/cm^2, respectively.

In Figure 4.42, the bandwidth increases as expected with bias current up to a limit where it saturates. The solid and dashed lines are theoretical fits using Equation 4.2. The trend of higher MCEF with larger overlap was expected due to the increased photon density, gain, and differential gain at lower junction temperatures, but the factors affecting the saturated bandwidth are less clear. Non-zero heatsink overlaps result in an additional parasitic capacitance between the heatsink and lower mirror that adds to the total pad capacitance. The horizontal and vertical parasitic capacitance ($C_{\text{wrap }h}$, $C_{\text{wrap }v}$) for the 9μm active diameter Cu-plated device as shown in Figure 4.37(d) were estimated to be ~224fF and ~16fF based on geometrical calculations with a 1000Å of SiN_x layer serving as the dielectric. PSpice simulations, which also include a ~22fF parasitic pad capacitance, indicate purely electrical circuit effects would allow a maximum f_{3dB} of 12.4 GHz for the 4μm overlap. Smaller overlaps and corresponding lower capacitance would

give higher electrical bandwidths in a trend opposite to the measured bandwidth, indicating the devices are not electrical bandwidth limited. Thus, the bandwidth saturation is attributed to thermal effects, perhaps combined with gain partitioning between modes, to be examined in further detail in the future. The optimum overlap will balance the tradeoff in capacitance and thermal impact on overall bandwidth.

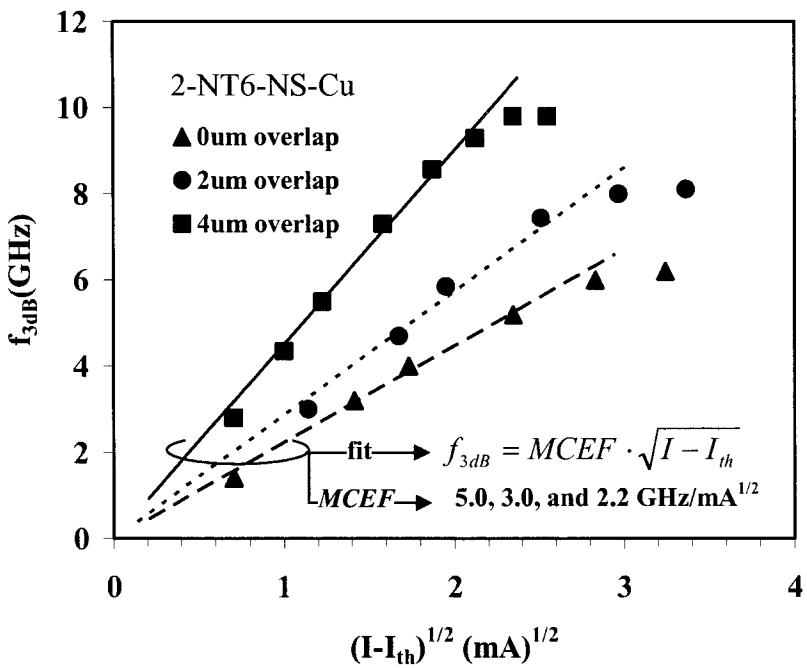


Figure 4.42 2-NT6-NS-Cu VCSEL 3dB modulation frequency as a function of the square root of the current above threshold.

Variation in the outer diameter of Cu-plated heatsinks is seen to have a major effect on thermal impedance and, thus, temperature-dependent DC and AC properties of top-emitting VCSELs. The second generation of VCSELs presented in this work with the lowest published thermal resistances to date have been developed using wafer-scalable processes that do not require soldering to external heatsinks or other hybrid processes. It appears that the application of these Cu-plated heatsinks to epitaxial structures designed

to provide higher MCEF and prolonged single-mode operation should enable significantly higher bandwidths than those demonstrated in this section and potentially higher than any previously demonstrated in VCSELs.

4.4.2 Non-self-aligned low-current density, inverted-polarity, 850nm VCSELs (2-ET1-NS-Cu)

While driving VCSELs at higher currents can give higher speed, this also negatively impacts reliability [15]. Thus, it is important to explore devices that can operate at high data rates while maintaining low current densities. Furthermore, most VCSELs are fabricated using *n*-type substrates with *n*-type and *p*-type DBRs below and above the quantum wells, respectively. On the other hand, circuit and device performance considerations for arrays of VCSELs motivate inverting this polarity so that the substrate and lower DBR layers are *p*-type and the upper DBR layers are *n*-type. The second configuration allows fabrication of common anode VCSEL arrays that can be driven with *npn* transistors which, typically perform better than *pnp* transistors [36].

This section presents low current density, inverted polarity, oxide-confined, polyimide-planarized, Cu-plated 850nm VCSELs with a record bandwidth and one of the highest reported MCEFs. The lasers exhibit modulation bandwidths up to 18GHz at current densities of only 8kA/cm^2 and a MCEF as high as 15.6GHz/mA$^{1/2}$. The process does not require ion implantation [14], deep field etches to semi-insulating substrates [37], or very small pad areas [38].

4.4.2.1 Fabrication summary

Low current density, inverted polarity, top-emitting, Cu-plated 850nm VCSELs were fabricated from an AlGaAs structure on a *p*-type substrate, which is described in [4,26].

Devices were fabricated by etching 4.5μm deep cylindrical mesas 20μm to 36μm in diameter. Next, the sample was wet-oxidized, resulting in the oxide extending about 9μm from the mesa sidewall, yielding oxide aperture diameters from 3μm to19 μm depending on mesa size. After oxidation, Ge-Au-Ni-Au and BeAu(1%)-Ti-Au were evaporated with thicknesses of (330/670/200/500)Å and (500/300/500)Å to form the *n*-type top and *p*-type bottom contacts. A 1000Å of PECVD SiN_x was used to insulate the mesas sidewalls. Next, 5μm of cured HD-8000 polyimide was used for planarization and pad capacitance reduction [33]. Finally Cu heatsinks over the mesas along with probe pads on the neighboring polyimide covered regions were electroplated. Before depositing a seed layer of Ti-Au with thicknesses of (100/1000)Å on the entire sample, LOR-10B, which is based on a polydimethylglutarimide platform, was lithographically patterned to protect the VCSELs' facets from being exposed to the chemical etchants used to etch back the seed layer later in the process. About 3μm of Cu was plated. After removing the seed layer, the LOR-10B was stripped using AZ400K. VCSELs with different diameters were plated with annular heatsinks with an outer radius of 2μm larger than the mesa diameter, except for adjacent 26μm mesa diameter VCSELs, which were plated with 0μm and 2μm overlap. Figure 4.43 (a) shows an SEM photograph of a VCSEL with a 26μm mesa diameter, including coplanar waveguide probe pads plated with ~3μm of Cu ready for testing and a magnified view of the device structure in Figure 4.43 (b) and (c).

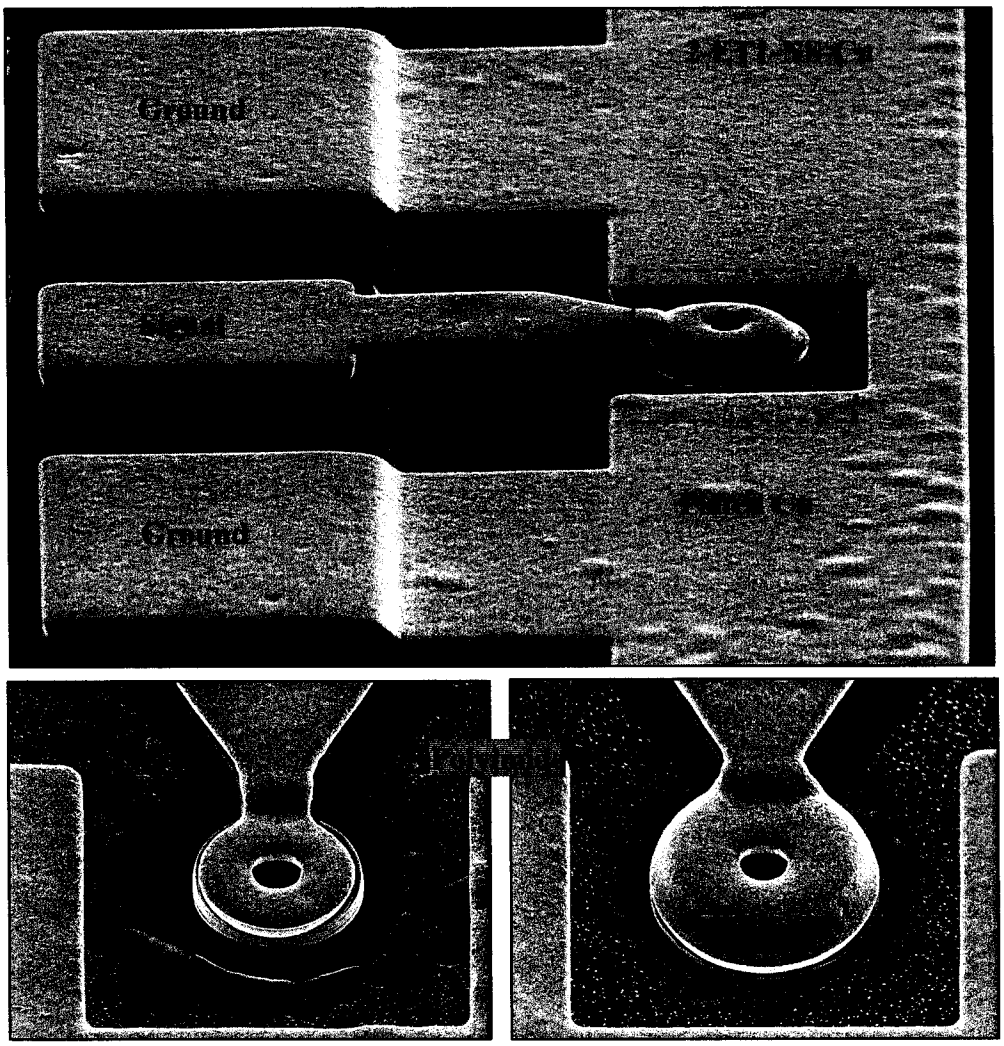


Figure 4.43 SEM images of (a) a 2-ET1-NS-Cu 26μm mesa diameter including coplanar waveguide probe pads plated with ~3μm of Cu. A magnified view of the device structure with (b) 0μm and (c) 2μm overlap.

4.4.2.2 Measurements and discussion

DC characteristics of completed VCSELs were measured using the same apparatus described earlier in this chapter. Figures 4.44 and 4.45 show the CW *L-I* and *I-V* characteristics for 26, 28, 30, and 36μm mesas diameters devices with 8, 10, 12, and 18μm diameter oxide apertures, respectively.

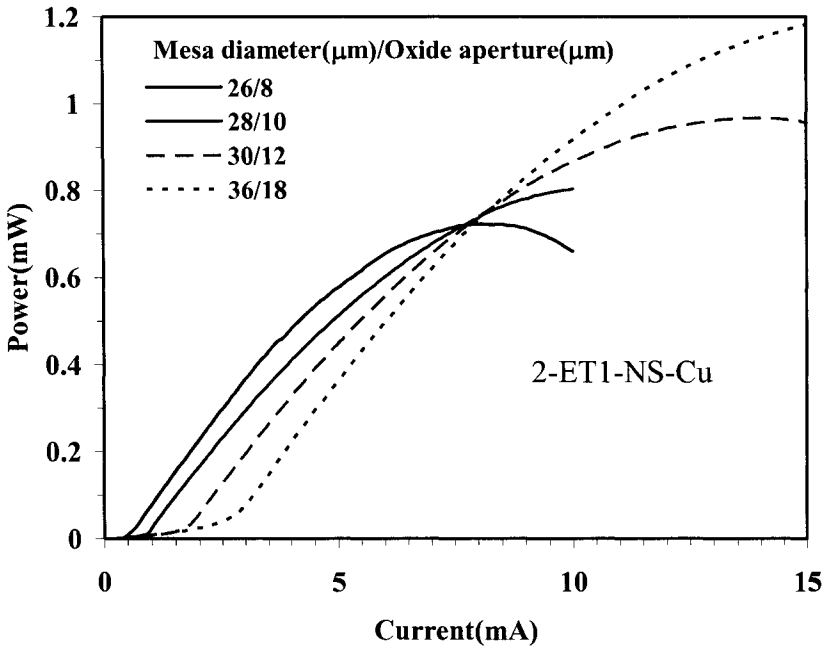


Figure 4.44 CW *L-I* characteristics for 2-ET1-NS-Cu VCSELs.

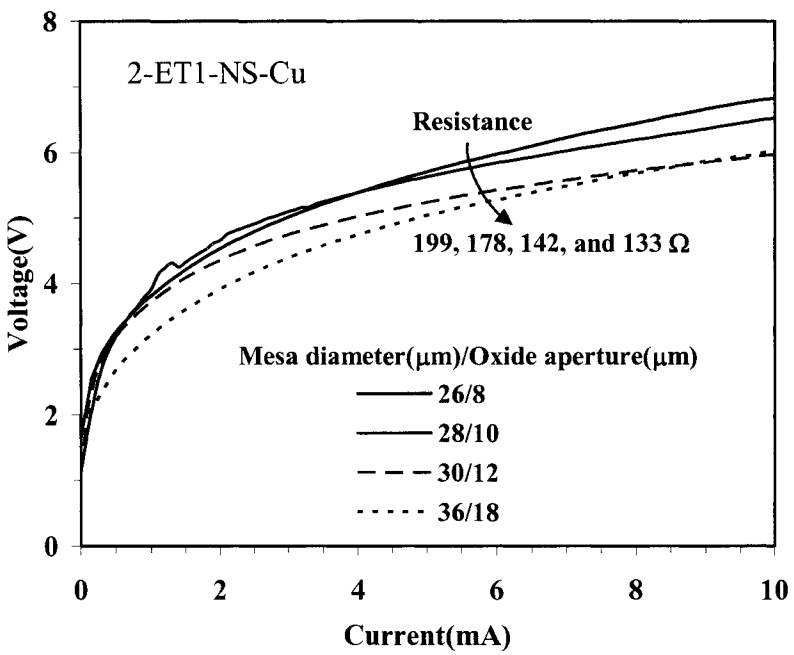


Figure 4.45 *I-V* characteristics for 2-ET1-NS-Cu VCSELs.

VCSELs with different oxide apertures exhibit a uniform threshold current density of 1kA/cm^2. Devices with a 26μm mesa diameter and an 8μm oxide aperture exhibit a

threshold current of only 0.5mA. The measured threshold voltages were considered to be high and the V-I curves are non-linear. Non-linear V-I curves might be due to either a non-ohmic (rectifying) contacts or thermionic mirrors in the VCSEL mirrors.

R_{th} of the devices was determined as described earlier in this chapter for a range of device diameters. Figure 4.46 shows R_{th} as a function of the active diameter (pink). The measured size dependence of R_{th} approximately follows the analytical estimation in Equation 4.1 for heat spreading from a uniform temperature disc on a homogenous, isotropic, semi-infinite substrate. Using a best fit to our data, we obtained a thermal conductivity of ξ =0.45 W/cm.K. For devices with a 10μm active diameter, the second generation of 850nm Cu-plated devices exhibited a reduced thermal resistance of 57%, 52%, and 45% compared to polyimide-wrapped [4], Au-wrapped, and Cu-plated first generation devices [5], respectively.

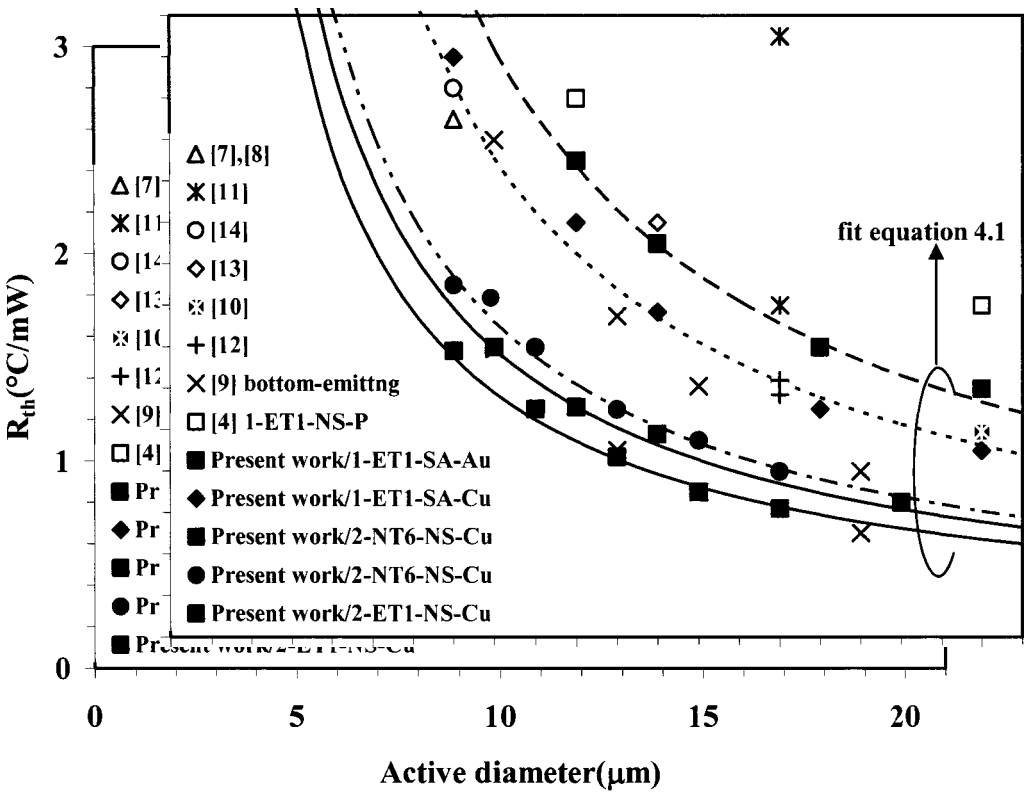


Figure 4.46 VCSELs' thermal resistance as a function of the active diameter.

Frequency response was measured on wafers using the same apparatus described earlier in this chapter. Figure 4.47 shows the modulation frequency response for a 26μm mesa diameter VCSEL with an 8μm oxide aperture at different bias currents. As shown in Figure 4.47, 8μm lasers exhibit 18 GHz maximum 3dB bandwidths when biased at I_{bias}=4.0mA. Due to calibration uncertainty and amplifier response issues, there is some uncertainty related to the reported bandwidth (i.e., the reported 18 GHz bandwidth might be more or less by 1-2GHz). Larger devices demonstrate smaller 3dB frequencies. Mesa diameters of 28μm and 30μm corresponding to 10μm and 12μm oxide aperture diameters yielded maximum bandwidths of 12.22GHz and 10.2GHz when biased at 6.0mA and 7.0mA, respectively.

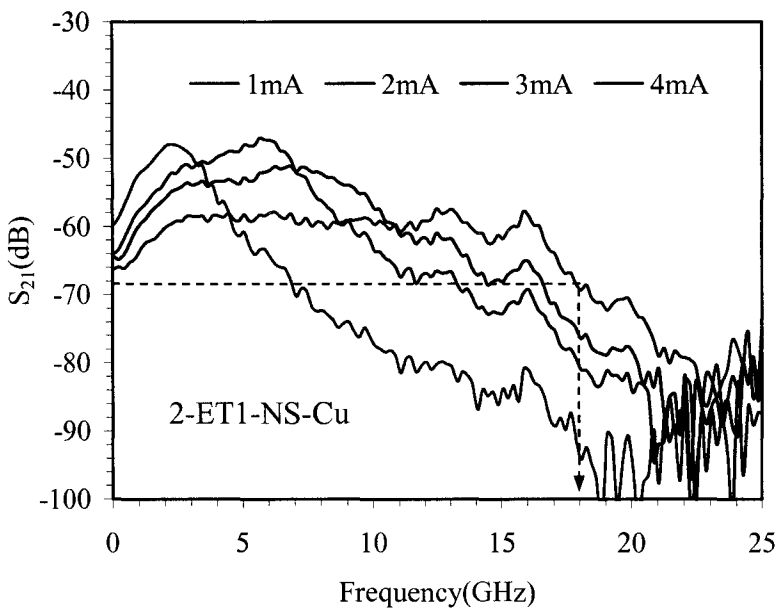


Figure 4.47 Modulation frequency response for a 2-ET1-NS-Cu 26μm mesa diameter VCSEL with an 8μm oxide aperture at a bias current of 4mA.

Based on the industrial current density benchmark for reliability, which is 10kA/cm^2 or less for VCSELs, the moderate bias current densities, such as 8kA/cm^2

necessary for the 18 GHz bandwidth in the 8 μm diameter device, should improve reliability and make it one step closer to commercialization. Figure 4.48 summarizes other reported current densities for various VCSELs bandwidths [4, 5, 8, 9, 14, 16, 18-21, 32]. To our knowledge, the 18 GHz bandwidth is the highest ever reported for directly modulated oxide-confined VCSELs. Although, a 19GHz bandwidth at a current density of 30kA/cm^2 for a similar device structure was calculated based on the measured relaxation oscillation frequency and the assumption of a low damping condition, which is an invalid assumption based on the data provided [40]. On the other hand, the highest measured VCSEL modulation bandwidth previously reported was 17.0 GHz [4], although a bandwidth in excess of 21.0 GHz using a combined implanted/oxidized device has been

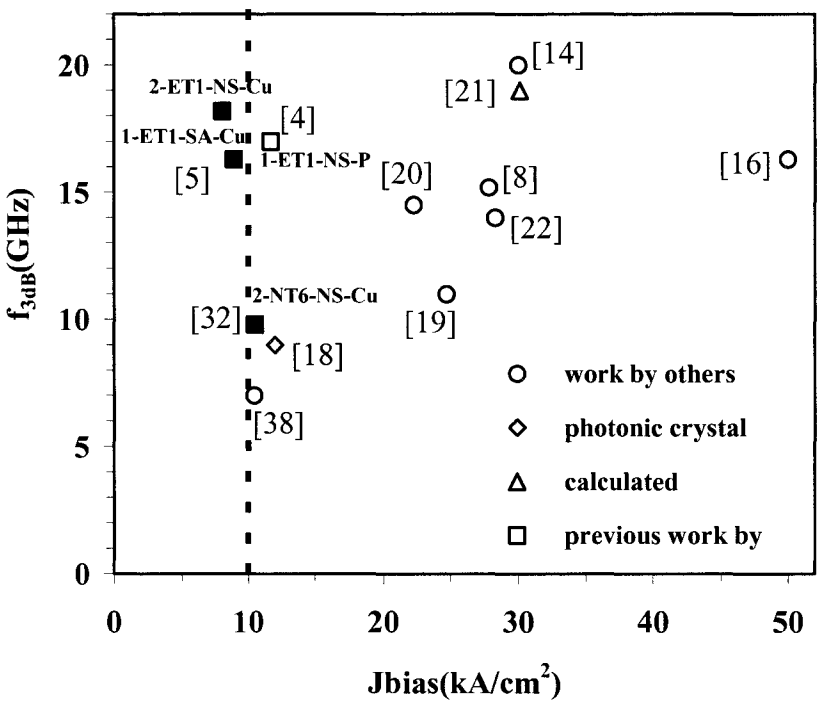


Figure 4.48 VCSELs bandwidths vs. current densities.

reported [14]. The bias current densities required to achieve these two bandwidths were about 12kA/cm^2 and 30kA/cm^2, respectively. Figure 4.48 shows the VCSELs' 3dB modulation frequencies as a function of the square root of the current above threshold for different device sizes at different bias currents. In Figure 4.49, the bandwidth increases as expected, with bias current up to a limit where it saturates. The solid lines are theoretical fits using $f_{3dB}=(MCEF)(I-I_{th})^{1/2}$. VCSELs with an 8μm diameter oxide aperture exhibited a MCEF of 15.6GHz/mA$^{1/2}$, which is slightly lower than the highest ever reported MCEF of 16.8GHz/mA$^{1/2}$ for oxide-confined 980nm VCSELs [16]. The measured wavelength spectrum for a device with an 8μm active diameter and 3μm of plated Cu at different bias currents is shown in Figure 4.50 (a) below. As the bias current increases, higher order modes are excited and the device exhibits multimode operation. Figure 4.50 (b) shows the VCSEL 3dB modulation frequencies as a function of the

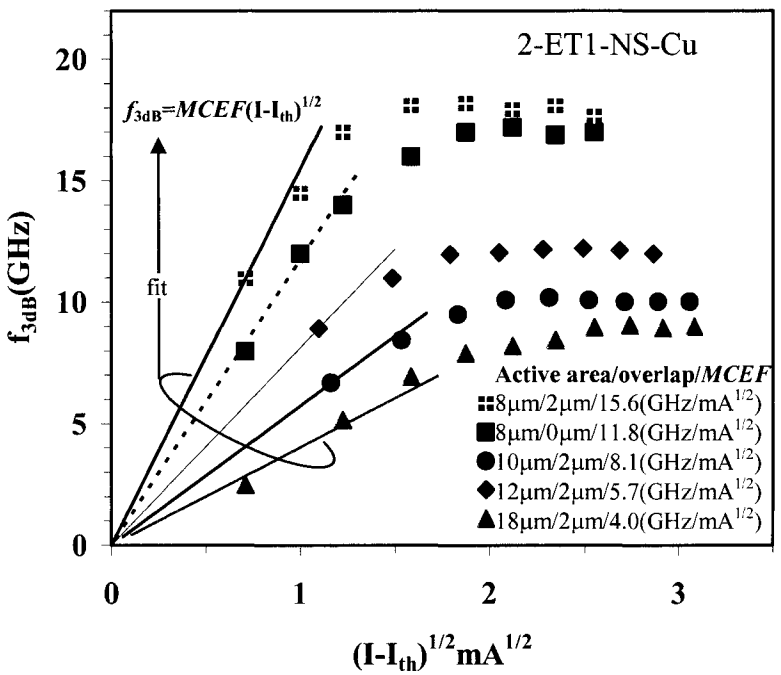


Figure 4.49 2-ET1-NS-Cu VCSEL 3dB modulation frequencies as a function of the square root of the current above threshold.

square root of the current above threshold, where the 3dB frequency increases as the bias current increases in a linear fashion and then begins to deviate from the linear relation between the 3dB frequency and $(I_{bias}-I_{th})^{1/2}$ more and more until it saturates completely when biased at currents greater than or equal to 4mA. Tying this phenomenon to the number of modes at each bias point shown in Figure 4.50 (a), one can see that as soon as the second mode appears, the 3dB frequency begins to saturate. Further increase in the bias current increases the number of modes and their corresponding intensity, which increases the rate at which the 3dB modulation response saturates.

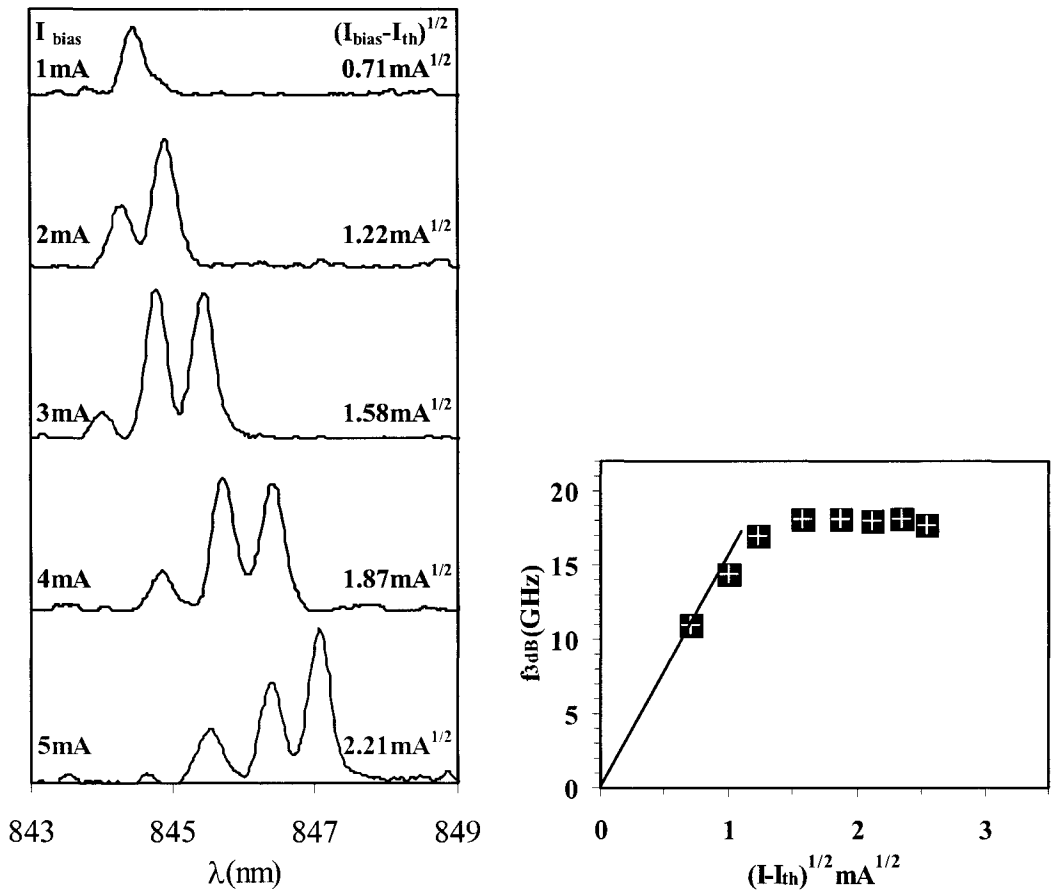


Figure 4.50 (a) Wavelength spectrum for an 8μm active diameter 2-ET1-NS-Cu VCSEL with a 3μm of plated Cu at different bias currents. (b) VCSEL 3dB modulation frequencies as a function of the square root of the current above threshold.

We have fabricated and characterized high-speed oxide-confined polyimide-planarized Cu-plated VCSELs with excellent performance using a process without implantation or semi-insulating substrates. The modulation bandwidth of VCSELs with conventionally sized pads is as high as 18GHz at only 8kA/cm^2 and a modulation current efficiency factor as high as 15.6GHz/mA$^{1/2}$.

4.4.3 Bottom-emitting flip-chip bonded 980nm VCSELs (2-NB1-NS-FB, 2-NB2-NS-FB, and 2-NB3-NS-FB)

Due to the reasons given in Section 4.3.4, only devices from wafer number NB1 were fabricated.

4.4.3.1 Fabrication summary

The second generation of the bottom-emitting VCSELs fabrication began with etching 6μm tall cylindrical mesas. Next, the sample was wet-oxidized, resulting in 4μm of oxide extending from the mesa sidewalls. Ti-Au and Au-Ge-Ni-Au with thicknesses of (200:1500)Å and (330/670/200/500)Å were evaporated to form the top *p*-type and bottom *n*-type contacts, respectively. Finally, HD-8000 polyimide was used for the reasons listed in Section 4.4. Figure 3.41 represent an SEM image of the bottom-emitting VCSEL die after bottom contact deposition. The heat spreaders were fabricated as described in Section 4.3.4.1. Figure 3.42 shows an SEM image of the heat spreader. The insets show a bonding pad (a) before annealing, (b) after annealing. At this point of the process, the VCSEL die is ready to be flipped and bonded to the heat spreader as shown in Figure 3.43. The flip-chip bonding process was done as described in Section

3.5.4, and the VCSEL die-bonded to the heat spreader ready for characterization is shown in Figure 3.45.

4.4.3.2 Measurements and discussion

The DC testing was performed on the VCSEL die before and after the flip-chip bonding using the DC testing setup described earlier in this chapter.

The CW L-I and I-V characteristics for VCSELs with mesa diameters of 18, 22, 24, and 28μm and oxide apertures of 10, 14, 16, and 20μm, respectively, are shown in Figures 4.51 and 4.52. Devices with a 10μm active area have a threshold current and a slope efficiency of 0.6mA and 80%, respectively. The flip-chip bonding increased the maximum output power for VCSELs with active diameters of 10, 14, 16, and 20μm by 10, 11, 19, and 25%, respectively. Based on the relative power increase, it seems that as the devices' active diameter gets smaller the vertical heat sinking provided by the flip-chip bonding is less efficient and a lateral heat sinking mechanism needs to be introduced, as discussed in Chapter 6. Even with no antireflection coating, the L-I plots seem to be clean of the typical ripples associated with bottom-emitting VCSELs' output light intensity [1]. Being able to measure and compare the L-I data for devices with different sizes before and after flip-chip bonding side by side highlights the importance of the modification made to both the mask design and the fabrication process compared to those used to fabricate the first generation of bottom-emitting flip-chip devices where none of the flip-chip bonded device worked, as discussed in Section 4.3.4.2.

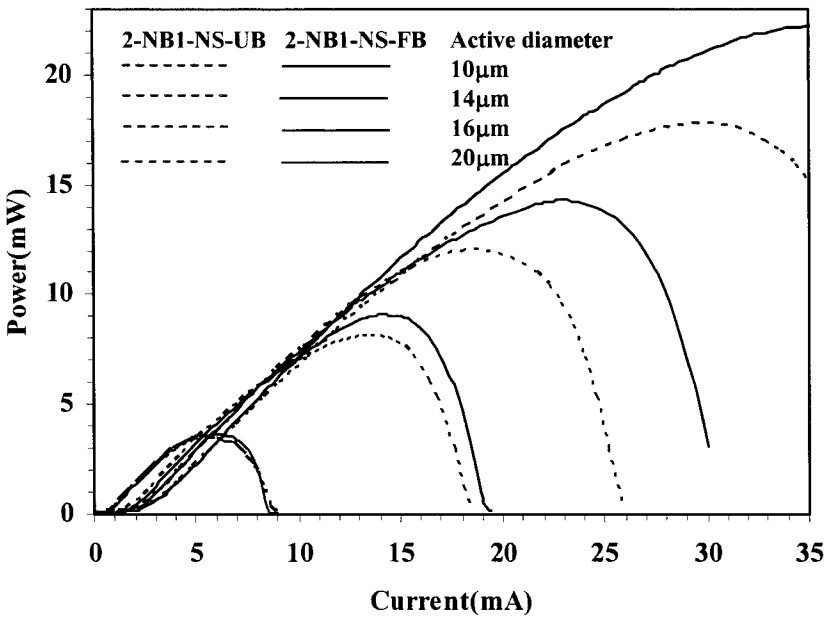


Figure 4.51 CW L-I characteristics for 980nm bottom-emitting VCSELs before and after flip chip bonding.

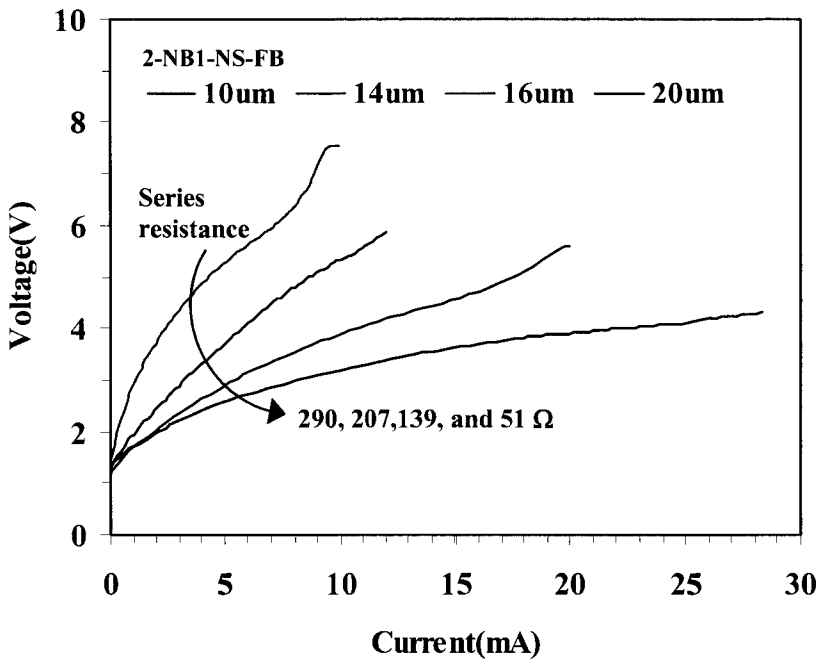


Figure 4.52 I-V characteristics for 980nm bottom-emitting unbonded VCSELs.

4.5 Conclusions

High-speed oxide-confined VCSELs with excellent performance have been tested and characterized. Measurements demonstrated the effect of heat-sinking on the performance of high-speed VCSELs operating at 850nm and 980nm wavelengths. In addition to the electroplating technique for top-emitting VCSELs' heat-sinking, the flip-chip bonding of bottom-emitting devices also demonstrated its effect on the VCSELs' performance. Furthermore, the effect of external heating on the VCSELs' resonance frequency and damping factor was examined. Following is a summary of the conclusions made based on the measurements.

The first generation of self-aligned top-emitting 850nm high-speed VCSELs (1-ET1-SA-Au, 1-ET1-SA-Cu) were tested and characterized. VCSELs' mesa capacitance was reduced by 49% compared to values reported earlier [4]. Measurements show a considerable effect of heat sinking on the performance of the 850nm VCSELs. Au-wrapped and Cu-plated heat-spreading layers reduced the thermal resistance by 25% and 44%, respectively [5], and the output power was increased by 17% and 38%, respectively, compared to similar VCSELs (1-ET1-NS-P) [4] without the Cu-plated heatsink. The fabricated lasers exhibited a 3dB modulation frequency bandwidth up to 16.3 GHz at about 8.9kA/cm^2 current density [5], which is 12% higher than that reported in [4] compared to 50kA/cm^2 required to achieve this bandwidth before [16]. The lower operating current density improves device reliability [15]. Modulation bandwidth limitations due to parasitic capacitance for the 850nm fabricated devices (1-ET1-SA-Au) were investigated. Due to the overlap of the plated Cu that extends to about 6μm around the mesa, PSpice simulation indicated that the purely electrical circuit effects would

allow a maximum 3dB bandwidth of ~15.6GHz, which is very close to the measured value of 16.3GHz. By limiting the plated Cu extension to 2μm, a simulation pointed out that the purely electrical circuit effects would allow a maximum 3dB bandwidth of about 63GHz [5]. It is believed that the Cu-plated VCSELs with 6μm overlap are limited by electrical parasitics rather than thermal effects.

The testing also revealed the effect of heat sinking on the performance of the second generation of high-speed, non-self-aligned top-emitting 980nm VCSELs (2-NT6-NS-Cu). Increasing Cu-plated heatsink radii from 0μm to 4μm greater than the mesa in 980nm VCSELs reduced the measured thermal resistance for a range of device sizes to values 50% [32] lower than previously reported over a range of device sizes. For a 9μm diameter oxide aperture, the 4μm heatsink increases output power and modulation bandwidth by 131% and 40%, respectively [32]. The functional dependence of thermal resistance versus the large change with and without sidewall coating indicates the importance of lateral heat flow to mesa sidewalls. The measured 3dB modulation frequency bandwidth was up to 9.8GHz at 10.5kA/cm^2 compared to 20kA/cm^2 required to achieve similar bandwidth [22]. Although the second generation devices (2-NT6-NS-Cu) increased output power and modulation bandwidth by 131% and 40% [32], respectively, compared to only 38% and 12% [5] for the first generation devices (1-ET1-NS-P), still the first generation VCSELs (1-ET1-NS-P) exhibited 16.3GHz of modulation bandwidth compared to 9.8GHz bandwidth for the second generation devices (2-NT6-NS-Cu). This case is a good example of the importance of epitaxial material optimization for high speed operation.

Using the second generation process, measurements showed an improved heat-sinking effect on the performance of high-speed non-self-aligned 850nm VCSELs. For the 2-ET1-NS-Cu devices with a 10μm active diameter, the second generation of 850nm Cu-plated devices exhibited a reduced thermal resistance by 57%, 52%, and 45% compared to polyimide- wrapped (1-ET1-NS-P) [4], Au-wrapped (1-ET1-SA-Au) and Cu-plated (1-ET1-SA-Cu) first generation devices [5], respectively. The lasers exhibit modulation bandwidths up to 18GHz at current densities of only 8kA/cm^2 and a MCEF of 15.6GHz/mA$^{1/2}$.

The effect of external heating on the 1-NT4-SA VCSELs' resonance frequency and damping factor was also demonstrated. Measurements showed that increasing the stage temperature reduces both the resonance frequency and the damping factor, hence limiting the modulation bandwidth of VCSELs. Based on the relationship between the damping and the resonance frequency squared, the maximum intrinsic 3dB frequency bandwidth was estimated to be 24.7GHz. Finally, as the contacts of the self-aligned VCSELs go through annealing, etching, and oxidation, specific contact resistance measurements for Ti-Pd-Ti-Au-Ti-Pd and Ti-Ni-Ti-Ni metal systems revealed the effect of different treatments on their specific contact resistance. The latter metal system exhibited a lower specific contact resistance compared to the former one.

Bottom-emitting non-self-aligned 980nm devices that were fabricated using the first generation of mask layout and fabrication process (1-NB2-NS-UB) were tested and characterized. VCSELs with an 8μm oxide aperture exhibited a threshold current of 0.5mA, a threshold voltage of 2V, a series resistance of 228Ω, and slope and wall plug efficiencies of 71% and 47%, respectively. The relatively high value of the device

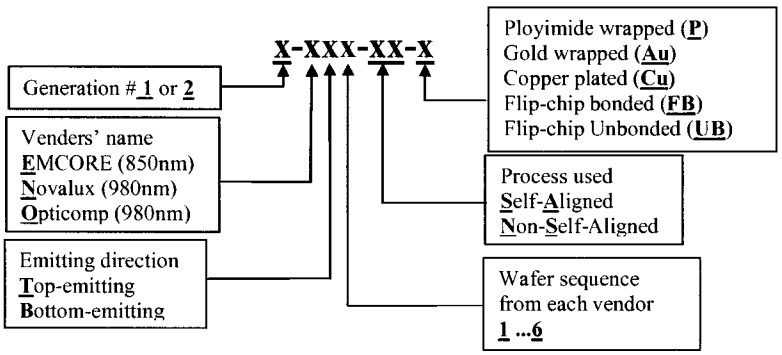
resistance might be due to the fact that the oxidation layer was missing, while the high threshold voltage might be due to the type of doping used. Measurements for bottom-emitting non-self-aligned flip-chip bonded 980nm devices fabricated using the second generation of mask layout and process parameters (1-NB2-NS-FB) showed that VCSELs with 10μm active area have a threshold current and a slope efficiency of 0.6mA and 80%, respectively. Furthermore, the flip-chip bonding increased the maximum output power for VCSELs with active diameters of 10, 14, 16, and 20μm by 10, 11, 19, and 25%, respectively.

Table 4.8 summarizes some of the fabrication steps and testing results for the samples reported in this chapter.

Table 4.8 Summary of some of the fabrication steps and testing results.

Sample number [a]	Top contact	Bottom contact	Active diameter (μm)	I_{th} (mA)	V_{th}(V) at I_{th}	$P_{out\ max}$ (mW)	η^{b}_{slope} (%)	R_{th} (°C/mW)	$f_{3dB\ max}$ (GHz)	J_{bias} (kA/cm^2) at $f_{3dB\ max}$
1-ET1-NS-P	Ge/Au/Ni/Au	BeAu[c]/Ti/Au	10	0.90		0.66	6	2.6	14.6	5.7
1-ET1-SA-Au	Pd/Ge/Ti/Pt	BeAu[c]/Ti/Au	10	0.65	1.8	0.76	7	2.3		
1-ET1-SA-Cu	Pd/Ge/Ti/Pt	BeAu[c]/Ti/Au	10	0.70	1.8	0.91	10	2.0	16.3	9.5
1-NT3-SA-Cu	Ti/Au/Ni/Au	Ge/Au/Ni/Au	6	0.75	1.4	4	25	--	--	--
			10	1.1	1.7	>5.5	25	--	--	--
1-NT6-SA-Cu	Cr	AuGe[d]/Ni/Au	10	1.1	2.3	9	47	--	7.0	7.64
			18	2.0	2.2	>13.5	45	--	7.0	4.72
1-NB2-NS-UB	Ti/Au	Ge/Au/Ni/Au	8	0.5	1.9	6	71	--	--	--
			10	0.9	2.2	>9	71	--	--	--
			12	1.3	2.2	>9	66	--	--	--
			14	1.5	2.2	>9	66	--	--	--
			16	1.8	2.1	>12	64	--	--	--
			18	2.1	2.1	>12	62	--	--	--
			20	2.5	2.1	>12	62	--	--	--
			22	2.9	2.1	>12	62	--	--	--
2-NT6-NS-Cu	Ti/Au	AuGe[d]/Ni/Au	9[f]	2.8	1.6	2.4	20	1.4	6.2	19.7
			9[h]	1.0	1.45	5.5	35	1.1	9.8	10.5
2-ET1-NS-Cu	Ge/Au/Ni/Au	BeAu[c]/Ti/Au	8[f]	0.5	--	--	--	1.62	17	14
			8[g]	0.5	3.25	0.73	10	1.4	18	8
			10[g]	0.75	3.6	0.8	9	1.11	12	16
			12[g]	1.5	4.1	0.97	10	0.98	10	18
			18[g]	2.5	4.0	1.2	10	0.65	9	24
2-NB1-NS-UB/FB	Ti/Au	Ge/Au/Ni/Au	10	0.6	--/2.4	3.5/3.6	80	--	--	--
			12	1.5	--/2.2	8.1/9.0	80	--	--	--
			14	1.8	--/2.0	12/14.3	80	--	--	--
			20	2.4	--/2.1	18/22	67/73	--	--	--

a: Sample number legend
Wet-oxidized
Dry etched



b: Close to threshold
Un-calibrated photodiode
c: 1% pre-alloyed
d: 12% pre-alloyed
f: 0μm overlap
g: 2μm overlap
h: 4μm overlap
--: N/A

References:

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Chapter 5

STUDY OF SPIN-COATED DIELECTRIC INSULATORS SUITABLE FOR HIGH-SPEED VCSELS AT MICROWAVE FREQUENCIES

5.1 Introduction and background

In order to reduce the metal pad VCSEL parasitic capacitance, this chapter presents a dielectric study of spin-coated dielectric insulators properties suitable for high-speed device fabrication (Table 5.1). Section 5.2 details the fabrication steps used to fabricate the test capacitors to evaluate the parasitic capacitance of high speed VCSEL using the metal pads. The microwave reflection coefficient, S_{11}, measurements and experimental setup are presented in Section 5.3. Details on complex dielectric permittivity and tangential loss extraction are discussed in Section 5.4. The circuit model for the pad capacitance which is obtained based on geometrical and physical considerations will be considered in Section 5.5.

As devices become smaller, faster and more powerful, the demands on both materials and processes used by the manufacturers of microelectronic devices become more critical. Dielectrics play a significant role in achieving the current state-of-the art in microelectronics [1-3]. They are typically applied in semiconductor micro-fabrication for a number of applications such as stress buffers to accommodate built-in strains as well as strain induced by forced bending [4,5], surface planarization and passivation [6], dielectric isolation layers [7,8], die bonding [9], and buried channel waveguides [10].

Spin-on dielectrics are used in fabricating many high speed electronic devices for reduction of parasitic circuit elements that may limit device speed. In heterojunction

bipolar transistors (HBTs), parasitics were reduced by collector implantation [11] or by double polymer planarization [12]. A multilayer polymer structure was used to reduce parasitic capacitance of permeable base transistors (PBTs) (vertical MESFETs) [13]. In vertical-cavity surface emitting lasers (VCSELs), polymer was used for planarization, passivation and metal pad parasitic capacitance reduction [14]. Spin-on glass (SOG) has been actively investigated [15-17] for similar applications. SOG have been used in multilevel metal interconnect processes [15,16].

When a dielectric material is subjected to an electric field, the bound positive and negative charge constituents are displaced from their average equilibrium positions by the Lorentz electric field forces. The charge adjustment results in several polarization mechanisms including dipolar polarization, ionic polarization, and electronic polarization [18]. Dipolar or orientational polarization occurs when permanent dipoles in asymmetric molecules respond to the applied electric field. Ionic polarization arises when adjacent positive and negative ions are displaced in the presence of an applied electric field. Electronic polarization occurs in neutral atoms when an electric field displaces the negative electron cloud with respect to the positive nucleus. Each polarization mechanism has an associated response time and therefore will not contribute to the dielectric constant beyond some corresponding frequency [19]. The maximum effective response frequency of dipolar, ionic, and electronic mechanisms are on the order of 10^{10} GHz, 10^{12} GHz and 10^{15} GHz respectively [19].

Table 5.1 Families, specific verities and general properties of the investigated dielectrics.

Specific variety	HD-8000	PI-2723	BCB-4024	SOG IC1-200
Manufacturer	HD Microsystems™	HD Microsystems™	Dow Chemical Cyclotene™	Futurrex, Inc.
Dielectric material	Organic polymer	Organic polymer	Organic polymer	Spin On Glass
Family	Polyimide	Polyimide	Bisbenzo- cyclobutene	Polysiloxane
Tone	positive	positive	negative	non-photosensitive
Cured film thickness(μm)	5-11	1.8-8.5	3.5-7.5	0.5[a]
Tg[b] (°C)	300	>320	>350	-
CTE[c] (ppm/(°C)	47	57	52	-
Elongation (%)	11	12	8	-
Breakdown field (V/cm)	-	$>2x10^4$	$3x10^6$	$3x10^6$
Volume resistivity (Ω-cm)	-	$>10^{16}$	10^{19}	$5x10^{13}$
Tensile modulus (Gpa)	2.5	2.7	2.9	-
Tensile strength (Mpa)	122	160	87	20

a: Achieved by double spin coating.

b: Glass Transition Temperature.

c: Coefficient of Thermal Expansion.

5.2 Fabrication

In high speed VCSEL fabrication, dielectrics are used to planarize etched mesas before depositing metal interconnects and bonding pads [14]. A smooth surface is needed for metal interconnect and metal bonding pad lithography and deposition. Polymer coatings also protect the sidewalls of the mesa from the external environment, and it creates an isolation layer between n and p contacts. Although the thermal conductivity of most polymers is poor, it is better than the thermal conductivity of gases in hermetic packages or air. The dielectric properties of the materials used in this work were investigated by fabricating capacitors from the different dielectric materials with various thicknesses and measuring their microwave scattering parameters (S-parameters).

5.2.1 Fabrication overview

Capacitors corresponding to the probe pads of VCSELs were fabricated above conducting ground planes on undoped GaAs substrates as illustrated in Figure 5.1 which shows a cross-section along AA' of Figure 5.2. To form the ground plane, which serves as the lower plate of the capacitor, layers of Ti-Au-Ti with thicknesses of (100/170/100) nm were evaporated in sequence on top of the substrate. In addition to serving as the capacitor's bottom plate, these ground plane layers shield the capacitors from the properties of the substrate. The lower layer of Ti was applied to improve the adhesion of the Au layer to the substrate while the upper Ti layer improves the adhesion of the spin-on dielectric to the lower metal. Au and Ti layers were chosen to be thick enough to withstand the dielectric surface tension and contraction during the curing process. Next, each one of the four different types of dielectrics listed in Table 5.1 were spun on the

ground plane and appropriately patterned and cured. Details of the dielectric fabrication processes will be discussed individually. Table 5.1 also shows the general family of the dielectric materials along with their tones, manufacturers, and specific part numbers.

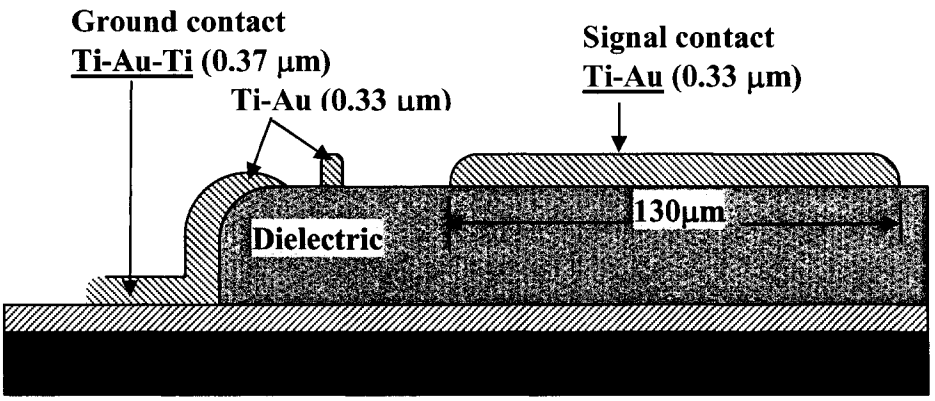


Figure 5.1 Capacitor cross-section at AA' in Figure 5.2.

The capacitor's top plate was fabricated with a metal pad mask suitable for on-wafer microwave testing. The co-planar pad configuration was originally designed for use in fabricating VCSELs including an annular contact region as seen in Figure 5.2. In the present work, the entire pad and annular contact region are insulated from the ground plane by a constant thickness dielectric layer. The pad design greatly reduces inaccuracies in microwave probing associated with parasitic coupling and unwanted mode excitation at the probing tips [20]. A ground-signal-ground (GSG) contact configuration was chosen as it terminates field lines at the interface effectively and excites the unwanted microstrip modes less than other contact configurations [20,21].

The metal probe pads and thus capacitor top plates were patterned using the same lift-off process on ten dielectric samples of varying thicknesses of the four materials (Table 5.2). The photolithography step used AZ4400 photoresist that was soaked in chlorobenzene for five minutes prior to developing to obtain a suitable profile for the lift-

off process [22]. Next, the samples were developed using AZ400K developer diluted with DI water (1:4). To reduce the resistance between the ground pads of the top plate and the lower Ti-Au-Ti ground plane, the titanium oxide layer TiO_2 that formed during

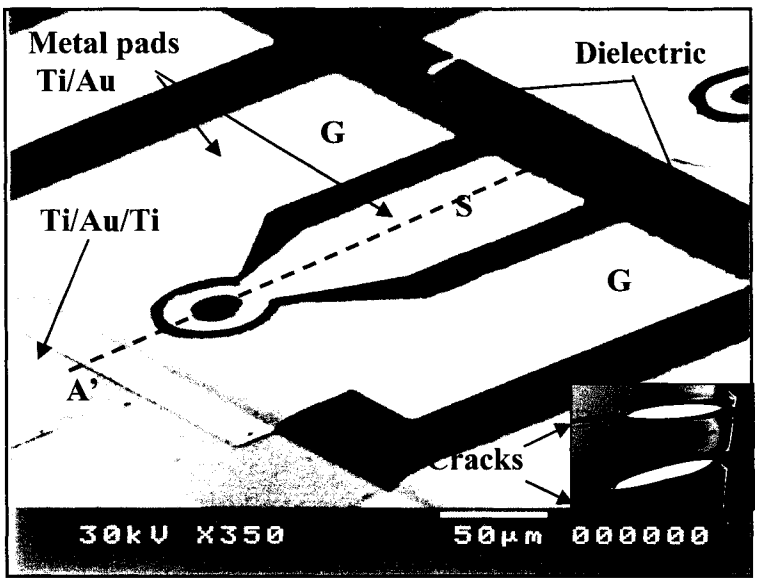


Figure 5.2 SEM photo for a completed capacitor ready for testing.

the curing process was wet etched in hydrofluoric acid (HF) diluted with DI water (5%:95%) for ~5s which is long enough to remove the TiO_2 layer and short enough to maintain the dielectrics surface smoothness. Then, Ti-Au was evaporated with thicknesses of (30/300) nm respectively [22]. Figure 5.2 shows an SEM photo of a completed capacitor structure using the high-speed VCSEL metal interconnect pad design.

5.2.2 Dielectrics Fabrication

5.2.2.1 Polyimides (HD-8000 and PI2723)

Polyimides have been identified as having excellent potential for use in high speed electronic devices, aerospace composites, and air craft wire and cable coating among

other applications due to their high inherent thermal stability, and excellent electrical and mechanical properties [23]. One potential disadvantage of polyimides is their moisture absorption [24]. Polyimides are cyclic-chain polymers which are mainly synthesized by a two-step technique. First, polyamic acid is formed by a condensation reaction of a tetracarboxylic acid dianhyride with a dysfunctional base (diamine). Polyamic acid is readily soluble in polar organic solvents. In the second step of the synthesis polyamic acid is cyclodehydrated to the corresponding polyimide by extended heating at an elevated temperature [25], by treating with chemical dehydrating agents [26], or by microwave energy [27]. A typical molecular structure for a photosensitive polyimide after curing is shown in Figure 5.3 (a) [28].

The dielectric for the first set of capacitors was HD-8000, a photosensitive, positive tone polyimide that can be imaged and processed as a positive tone photoresist. HD-8000 capacitors were fabricated as follows. First the standard photolithography process was carried out according to the manufacturer's data sheet. To obtain different dielectric thicknesses, different spinning speeds were used for this type of polyimide as well as all other types of dielectrics used in this study. After exposure, the sample was baked for 100s at 115°C. Then, it was left to cool down to ambient temperature for about 30 minutes prior to proceeding with the developing step. Developing polyimide while hot leads to severe cracks in the cured polyimide as shown in the inset of Figure 5.2. Dipping a hot sample in the developer will drop the cured polyimide surface temperature to 20°C while the temperature of the polyimide underneath the surface is about 120°C. As a result the surface of the polyimide contracts more than the polyimide underneath, with the resulting stress cracking the polyimide. The polyimide was developed in the commonly

used AZ400K aqueous developer diluted with deionized (DI) water (1:4). After developing, the sample was rinsed by squirting it with DI water while it was spun at 1000 rpm for 10 seconds. Immediately after the rinse, it was spin-dried at 3500rpm for 10 seconds. To cure the polyimide the sample was loaded into a curing furnace at 20°C in a nitrogen atmosphere, and the temperature was ramped from 20°C to 350°C over a 60-minute period. The temperature was held at 350°C for 30 minutes. Finally, the sample was allowed to cool down. The spinning speeds, developing times, and measured HD-8000 polyimide thicknesses after curing are listed in Table 5.2.

Table 5.2 Dielectrics fabrication process summary.

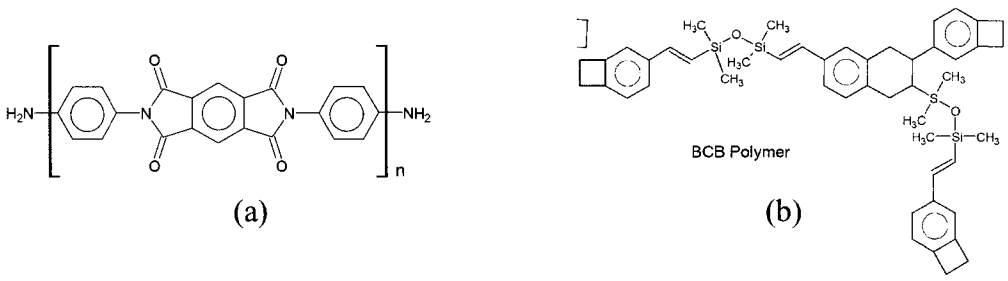
Specific variety	Sample number	Spin speed ($x10^3$rpm)	Developing time (s)	Cured thickness(μm)
HD-8000	1	10.0	40	1.36
	2	5.0	55	3.6
	3	3.5	80	5.5
PI-2723	4	5.5	25	1.35
	5	2.0	30	4.1
	6	1.3	46	6.0
BCB-4024	7	7.5	20	1.8
	8	3.5	30	4.3
	9	2.5	55	7.2
IC1-200	10	3.0	--	0.65

Pyralin® PI-2723 polyimide is a photosensitive negative tone organic polymer which was used to fabricate the second set of capacitors. After the photolithographic exposure, the polyimide was developed using DE-6018 solvent, then further developed in DE-6018 diluted with RI-9045 solvent (1:1), and finally rinsed using RI-9045. To cure the polyimide, the sample was loaded into furnace at 20°C, and the temperature was ramped from 20°C to 150°C at about 6.5°C /minute. Then the temperature was ramped

from 150°C to 300°C over a 60 minute period. The temperature was held at 300°C for 30 minutes. Table 5.2 lists the cured thicknesses of the PI-2723 polyimide as well as other process parameters.

5.2.2.2 Bisbenzocyclobutene (BCB-4024)

Bisbenzocyclobutene (BCB) has been traditionally used as a polymer dielectric for many multichip module (MCM) applications [29]. The thermal curing of Cyclotene™ polymers is a two step process. First the benzocyclobutene ring opens thermally to produce an *o*-quinodimethane intermediate. Next, the o-quinodimethane undergoes a Diels-Alder reaction with residual alkene groups in the prepolymer, forming a tri-substituted tetrahydronaphthalene [30]. One difference with respect to polyimide is that BCB does not evolve water during crosslinking. After curing, the crosslinked BCB polymer has low moisture uptake. The main disadvantage of BCB is the thermal stability of the cured film [31]. Figure 5.3 (b) shows standard cured photosensitive BCB polymer structure [32,33].



(a) (b)

Figure 5.3 Typical cured (a) photosensitive polyimide [28] and (b) BCB polymer [32,33] molecular structures.

BCB-4024 is a photosensitive, negative-tone polymer that was used for the third set of capacitors. Following the photolithographic exposure process, the polymer was developed using the DS-2100 solvent. To cure the polymer the sample was loaded into a furnace and the temperature was ramped from 20°C to 150°C at 4.5°C/minute. The temperature was held at 150°C for 15 minutes. Then, the temperature was ramped from 150°C to 250°C over a 10 minute period. The temperature was held at 250°C for 40 minutes. The measured BCB-4024 polymer thicknesses after curing are shown in Table 5.2 along with the corresponding developing times and spinning speeds.

5.2.2.3 Spin-on glass (IC1-200)

Intermediate coating IC1-200 is a high transparency polysiloxane-based spin-on dielectric material, which contains methyl and unspecified alkoxy groups bounded to silicon atoms with carbon contents in the range of 20-30% [34]. IC1-200 is used primarily in the planarization of topography on integrated circuits in multilevel metal techniques. SOG is applied as a dielectric in a permanent or a partial etchback mode. It can be utilized as an intermediate layer in the trilayer resist technique and as a protective layer for plastics and metals [34].

IC1-200 was spun at 3000rpm for 30 seconds. Then it was baked on a hot plate at 100°C for one minute and at 200°C for another one minute. Next, a second layer of SOG was spun and baked at same temperatures used for the first layer. After that, positive tone photoresist was patterned and developed to serve as a mask for a part of the SOG area. The exposed SOG was etched using reactive ion etching (RIE) system for ten minutes with chlorine and oxygen (2:1) at approximately 100mW power and 150 mTorr pressure.

Then the photoresist was striped and the SOG was cured at 400°C for 30 minutes in a nitrogen gas flow that prevents the SOG from oxidation, which can cause flakes to form. After curing the, SOG has an approximate thickness of ~0.65μm. Only this single thickness was used to fabricate SOG capacitors. The vendor recommended a maximum film thickness of ~0.5μm as thicker films can have excessive tensile stress that leads to the film cracking. Table 5.2 summarizes the cured dielectric thicknesses and their corresponding developing times and spinning speeds.

5.3 Measurements

The fundamental properties of dielectric materials can be measured either in the frequency domain or in the time domain using suitable transformation techniques to obtain the frequency dependence of the materials properties. One motivation for the development of time domain techniques was the necessity of different frequency domain methods and instruments to cover a frequency range of 1 Hz up to 10 GHz [35]. Frequency domain measurements were used in this study since time-domain techniques assume the system is linear and any unexpected non-linearity introduces complications in the transformation technique to be adapted [35,36]. Furthermore it is now possible to use a single instrument to cover a wide range of frequencies.

A variety of techniques can be used to measure the properties of dielectric materials in the frequency domain. The auto balancing bridge technique is accurate in the frequency range from a few Hz to 110MHz. The current-voltage (IV) and RF-IV techniques are also accurate and can be applied from 40 Hz to 3 GHz. The

Transmission/Reflection technique can be utilized for a frequency range from a few Hz to 110GHz [37].

Based on the frequency range of the available equipment, the Transmission/Reflection technique was applied. The S_{11} parameter measurement apparatus consisted of an Agilent 8722ET vector network analyzer (VNA) with 40GHz bandwidth, a computer with GPIB card to load the calibration kit into the VNA, a high precision Cascade Microtech impedance standard substrate (ISS-101-190), a probe station equipped with a 20°C constant temperature chuck, a fiber optic illuminator to reduce sample temperature variations, a CCD camera, and Cascade Microtech air co-planar probes (ACP40) with GSG configuration, a 125μm pitch, and Be-Cu tips which provide repeatable contact on gold pads. The use of ACP with GSG configuration helps deliver the RF signals with minimal attenuation and good impedance control, which results in accurate measurements [38].

The S_{11} parameter measurements proceeded as follows; Isopropyl alcohol diluted with DI water and lint-free wipes were used to clean the mating surfaces so that the measurements are not affected by dirt and impurities. RF cable reflection stability and connector repeatability were verified. The largest drift in the reflection coefficient for the cable terminated with an open circuit was -57dB which corresponds to a 0.0014 change in voltage amplitude. The VNA was calibrated at a power level of -10dBm (0.1mW) in order to maximize signal to noise ratio while not being so large as to require attenuation of the reflected signal. A low IF bandwidth of 100Hz was used to reduce noise. The measurement repeatability was improved by operating the VNA in stepped frequency mode, rather than with continuous sweep and by applying the VNA built in averaging

and smoothing functions. One-port calibration using a standard short-open-load (SOL) was carried out. Next the capacitor's microwave reflection coefficients were measured over a frequency range of 50 MHz to 40 GHz. Figure 5.4 and 5.5 show the real and imaginary parts of the measured reflection coefficients respectively for the dielectrics listed in Table 5.1. The raw data exhibited some ripples with magnitudes on the order of 10^{-3} that were filtered out using the VNA built-in smoothing and averaging functions. To maintain clarity, only the data for selected dielectric thicknesses are shown.

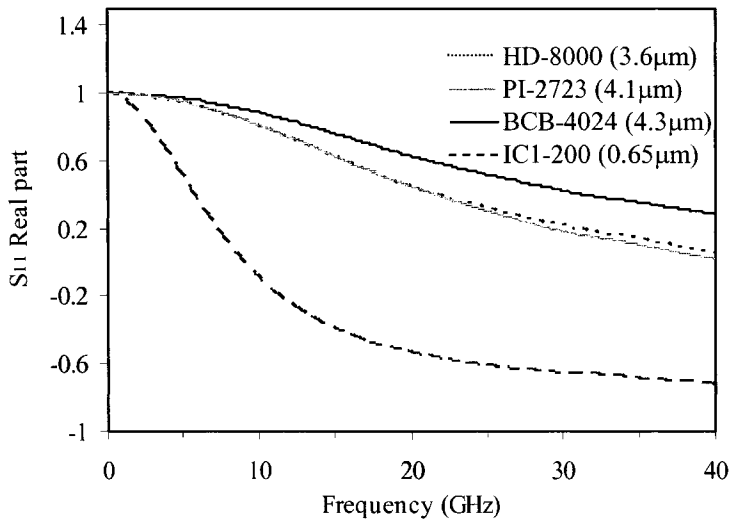


Figure 5.4 Real part of S_{11} parameter vs. frequency.

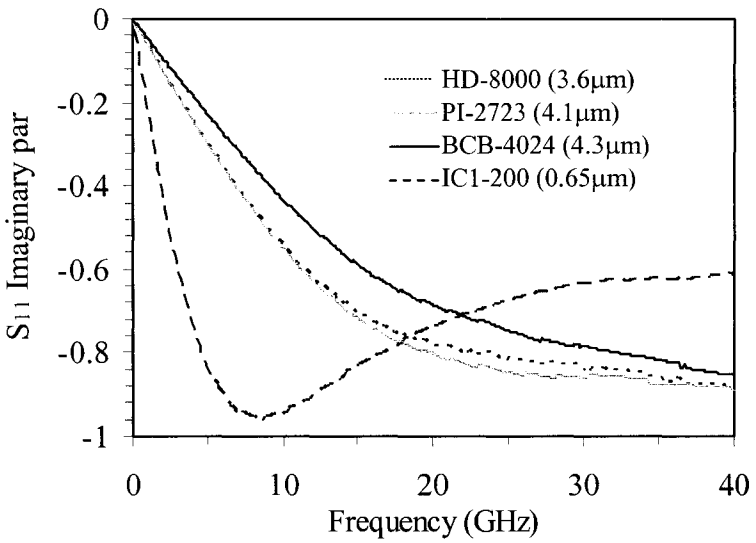


Figure 5.5 Imaginary part of S_{11} parameter vs. frequency.

5.4 Complex permitivity and tangential loss extraction

The complex permittivity and tangential loss are regarded as the most important parameters for describing dielectric properties [39]. The relative permittivity can be expressed in the complex form $\varepsilon^*=\varepsilon'-j\varepsilon''$, where ε' is the relative dielectric constant which characterizes a material's ability to store charges, and ε'' is the dielectric loss which is a measure of the dissipation in the material. The dielectric loss is typically quantified in terms of a material's dielectric loss tangent, $\tan|\delta_d| = \varepsilon''/\varepsilon'$, where δ_d is the dielectric loss angle [40,41].

The impedance of a capacitor with a lossy dielectric is given by $Z=d/(j\omega\varepsilon_o\varepsilon^*A)$[42], where ε_o is the free space permittivity $8.85\text{x}10^{-14}$ F/m, A is the capacitor area which is fixed for all capacitors in this study at 10400 μm^2, d is the thickness of the dielectric, and ω is the angular frequency. The measured impedances of the fabricated capacitors can be calculated from the measured reflection coefficients by $Z = Z_o(1+S_{11meas})/(1-S_{11meas})$, where S_{11meas} is the measured reflection coefficient and Z_o is the vector network analyzer impedance (50Ω). The relation between the measured and calculated capacitors' impedances is expressed as [42]

$$\frac{d}{j\omega\varepsilon_o(\varepsilon'-j\varepsilon'')A} = Z_o\left(\frac{1+S_{11meas}}{1-S_{11meas}}\right) \tag{5.1}$$

Solving equation (5.1) for the real and imaginary parts of $\varepsilon'-j\varepsilon''$ results in

$$\varepsilon'(\omega) = \left(\frac{d}{\omega\varepsilon_o A}\right)\frac{1}{Z_o}\mathrm{Im}\left(\frac{1-S_{11meas}}{1+S_{11meas}}\right) \tag{5.2}$$

$$\varepsilon''(\omega) = \left(\frac{d}{\omega\varepsilon_o A}\right)\frac{1}{Z_o}\mathrm{Re}\left(\frac{1-S_{11meas}}{1+S_{11meas}}\right) \tag{5.3}$$

Figure 5.6 and 5.7 illustrate ε'(ω) and ε"(ω) extracted from the measured data using equations (5.2) and (5.3) respectively. The tangential loss, $\tan|\delta_d|$, is shown in Figure 5.8 and was obtained by calculating the ratio ε"(ω)/ε'(ω) [41] using results from equations (5.2) and (5.3).

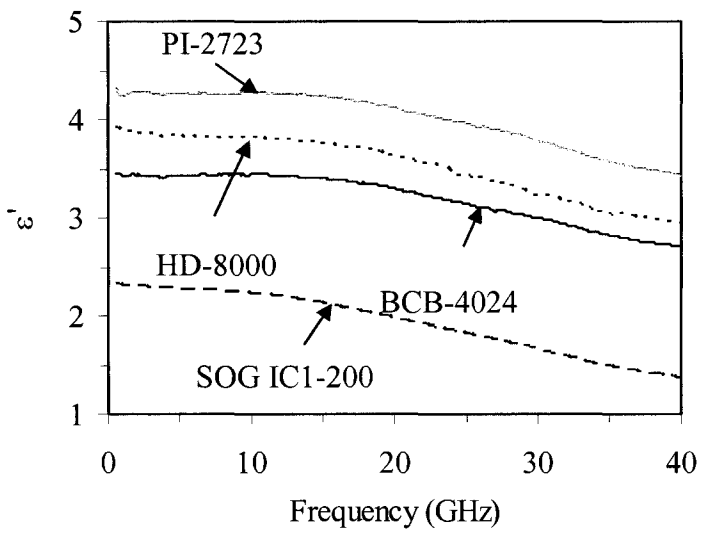


Figure 5.6 Measured real part of dielectric permittivity vs. frequency.

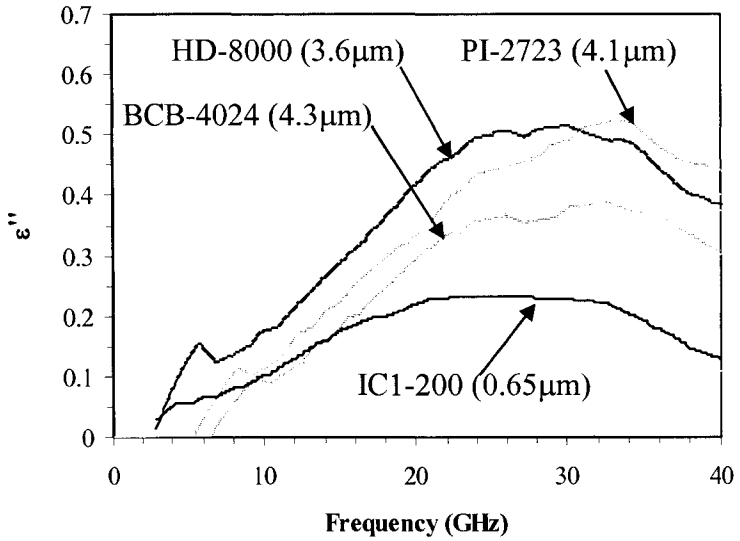


Figure 5.7 Measured dielectric loss vs. frequency.

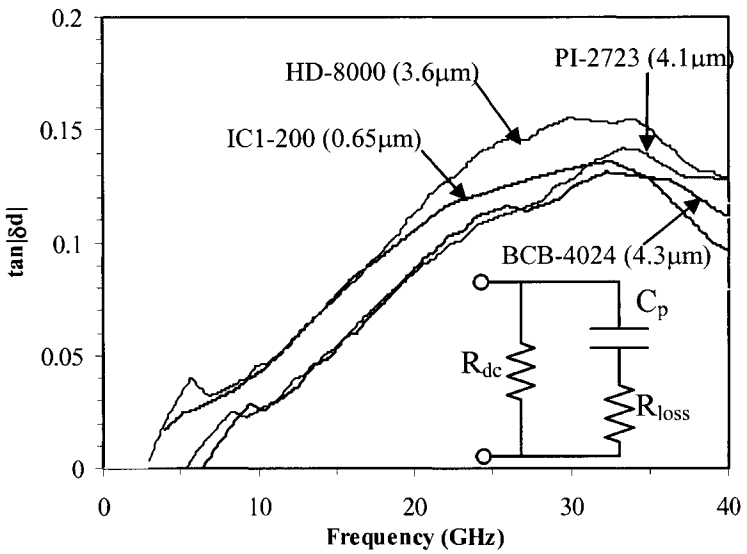


Figure 5.8 Measured dielectric tangential loss vs. frequency.

The data clearly show the frequency dependence of ε', ε", and tan $|\delta_d|$ for the studied dielectrics. The real part of the dielectric permittivity for all studied dielectrics monotonically decreases as frequency increases. The dielectric losses and thus loss tangents initially increase approximately linearly in frequency before reaching a broad peak and then decreasing. Such a response corresponds to the presence of one or more relaxation phenomena [36,41,43]. The maximum dielectric loss for HD-8000, PI-2723,

BCB-4024 and IC1-200 occurs at frequencies of 30GHz, 33GHz, 32GHz, and 25GHz respectively.

The dielectric parameters, ε', ε'', and tan $|\delta_d|$ vary in frequency as the different polarization mechanisms discussed in the introduction are selectively excited [18, 19]. As the frequency of the applied field is increased, a point is reached where the permanent electric dipoles (polar molecules) of the material can no longer rotate fast enough to remain in phase with the field. Therefore, contributions of the dipolar polarization mechanism to the net polarization declines, which subsequently causes a reduction in ε', ε'', and tan $|\delta_d|$.

5.5 Modeling and data fitting

Circuit models are useful for the analysis of high speed bandwidth limitations of electronic devices as well as matching driver circuits to device impedances. A circuit model for the capacitors was developed based on geometrical and physical considerations. The circuit model, shown in the inset of Figure 5.8, consists of elements corresponding to the physical features of the capacitor, where C_p denotes a lossless capacitor between the metal interconnect Ti-Au on top of the dielectric and the bottom plate Ti-Au-Ti. The fringing field at the sides of the top plate was neglected since the associated fringing capacitance was estimated to be less than 3fF [44]. A resistor, R_{loss}, in series with the capacitor models the resistance associated with the dielectric loss and the shunt resistor, R_{dc}, represents the resistance of the dielectric material at DC or low frequency due to the leakage current in the capacitor. R_{dc} is usually on the order of multi-gigaohms and was assumed to be so large that it has a negligible effect on the model.

Numerical calculations assumed a value of $R_{dc}= 10^{12}\ \Omega$ to improve convergence. The resistance in the leads and plates of the capacitor is relatively small. The DC plate resistance was estimated to be~0.15Ω. According to classical theory [45], the AC surface resistance of a conductor is $R_s(\omega)=(\mu_o\omega/2\sigma)^{1/2}$, where σ is the electrical conductivity which equals $4.1\text{x}10^7\ \Omega^{-1}\text{m}^{-1}$ and $2.3\text{x}10^6\ \Omega^{-1}\text{m}^{-1}$ for Au and Ti respectively, and μ_o is the material permeability that is $4\pi\text{x}10^{-7}$H/m for non-ferromagnets. The maximum surface resistance values for Au and Ti at 40GHz were approximately 0.06Ω and 0.26Ω respectively. The skin depth is given by $\delta_s(\omega)= (2/\ \omega\sigma\mu_o)^{1/2}$ for a good conductor assuming $\sigma/\omega\varepsilon'>>1$ [46-49]. At 40 GHz, the skin depths of Au and Ti were estimated to be 2.1μm and 0.39μm respectively which are larger than the capacitor's plate thickness of 0.33μm. Therefore the capacitor plates' DC resistance, AC resistance, and skin effect were neglected in the present model and subsequent analysis.

The circuit model impedance can be calculated as

$$Z_{model} = R_{loss} + \frac{1}{j\omega C_p} = \frac{d}{j\omega\varepsilon_o(\varepsilon'-j\varepsilon'')A} \tag{5.4}$$

Solving equation (5.4) for C_p results in

$$C_p = \left(1-\frac{\varepsilon''^2}{\varepsilon'^2}\right)\cdot\left(\frac{\varepsilon_o\varepsilon' A}{d}\right) \tag{5.5}$$

Since $\varepsilon''^2/\varepsilon'^2 << 1$, then equation (5.5) can be reduced to $C_p=\varepsilon_o\varepsilon' A/d$ so the frequency dependence of the capacitance is nearly proportional to the frequency dependence of ε'. Solving equation (5.4) for R_{loss} results in

$$R_{loss} = \frac{\varepsilon''}{\varepsilon'^2}\left(1-\frac{\varepsilon''^2}{\varepsilon'^2}\right)\cdot\left(\frac{d}{\omega\varepsilon_o A}\right) \tag{5.6}$$

Which can be simplified to $R_{loss}=(\varepsilon''/\varepsilon'^2)(d/\omega\varepsilon_o A)$.

Values for ε' and R_{loss} were found to be well approximated by second degree polynomials. The polynomial coefficients were allowed to vary until the minimum squared error was less than 10^{-4}. Figure 5.9 and 5.10 illustrate the extracted and fitted data for C_p and R_{loss} respectively, for the four dielectric materials investigated. The polynomial coefficients that result in the best fit are listed in Table 5.3. The constant term for the real dielectric permittivity, a_o, was found to be in reasonable agreement with the low.

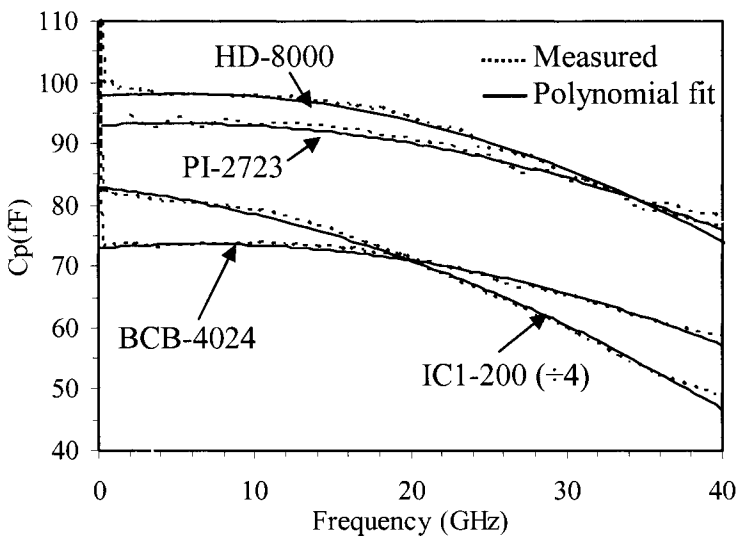


Figure 5.9 Capacitance vs. frequency.

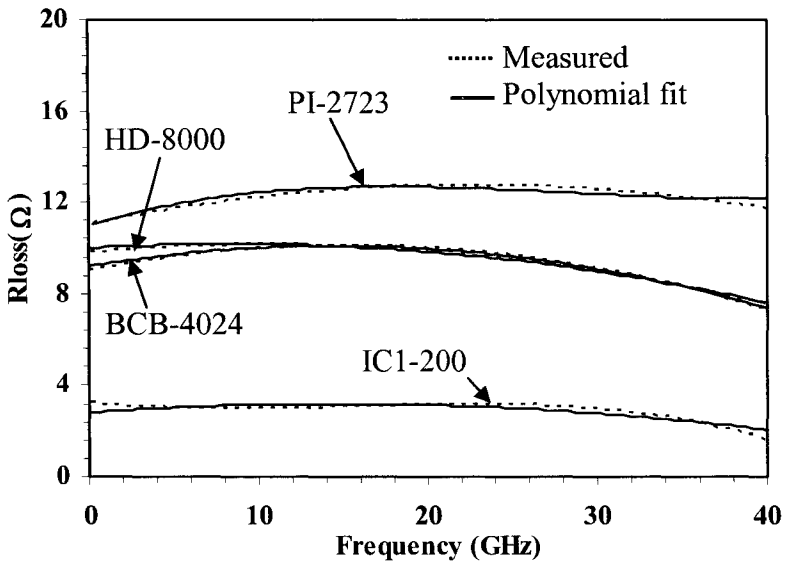


Figure 5.10 Dielectric loss equivalent resistance vs. frequency.

frequency dielectric permittivity values, ε_{LF}, provided by the vendors and reported by others [34,50] which are also listed in Table 5.3. As seen in Figure 5.10, the extracted values for R_{loss} are moderately constant across the frequency range studied, justifying the series resistance model. Average values of R_{loss} are listed in the table as well, and these constant resistances may suffice in simplified circuit models.

Table 5.3 Polynomials coefficients values for ε' as well as R_{loss}.

Specific variety	ε_{LF}			Thickness (μm)	$\varepsilon'(f)=a_o+a_1 f+a_2 f^2$			$C_p(f)$	$R_{loss}(\Omega)$	$R_{loss}(f)=b_o+b_1 f+b_2 f^2$		
	§	♦	‡		a_o	$a_1 x10^{-3}$	$a_2 x10^{-4}$			b_o	$b_1 x10^{-3}$	$b_2 x10^{-4}$
HD-8000	3.4	3.9	-	3.6	3.9	-2	-6	$\frac{\varepsilon_o \varepsilon'(f) A}{d}$	10	10	44	-26
PI-2723	3.3	4.3	-	4.1	4.3	7	-7		11	11	155	-34
BCB-4024	3.3	3.5	2.6[50]	4.3	3.5	20	-8		11	9.2	124	-43
SOG IC1-200	2.65	2.35	2.3[34]	0.65	2.35	-10	-4		2.8	2.8	52	-18

C_p : pad capacitance

R_{loss} : resistance associated with the dielectric loss

f : operating frequency(GHz)

§: vendor

♦: present work

‡: others

To further investigate the properties of the dielectrics under test, capacitors were fabricated using three different thicknesses of each of the organic polymers available. S_{11} parameters were measured and fitted to the circuit model as discussed earlier for each thickness. Figure 5.11 illustrates R_{loss} as a function of the polymer thickness. Results show a linear, approximately proportional dependence on thickness as expected from equation (5.6). Because R_{loss} is roughly proportional to the dielectric thickness, d, while the capacitance is inversely proportional to d, the RC time constant of these capacitors is relatively independent of dielectric thickness. In the case of a 50Ω load shunted by a lossy capacitor driven by a 50Ω source as shown in the inset of Figure 5.12 the 3dB bandwidth due to the capacitance is neither constant nor proportional to d. The actual 3dB bandwidth in this case is smaller than what would be expected if the capacitors were lossless for large dielectric thicknesses as illustrated in Figure 5.12 for HD-8000. The other dielectrics have the same trend.

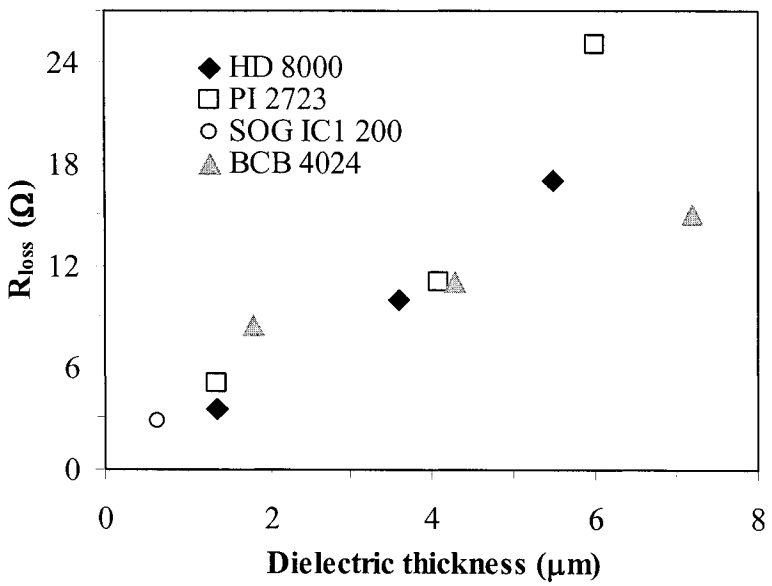


Figure 5.11 Dielectric loss equivalent resistance vs. dielectric thickness.

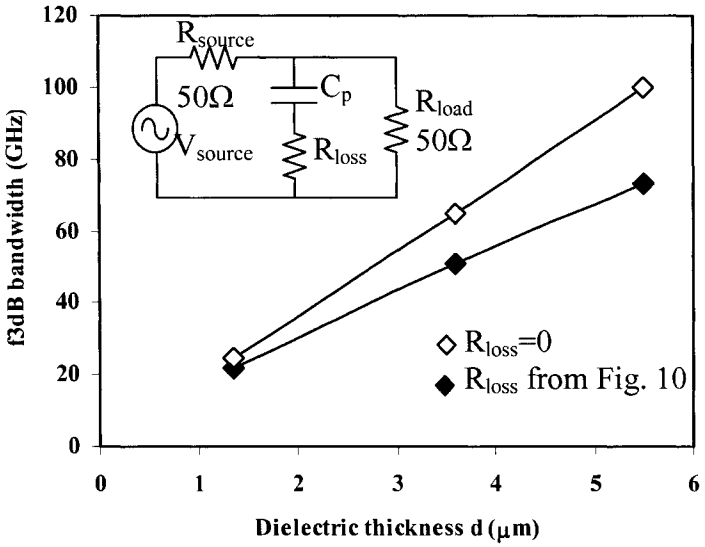


Figure 5.12 3dB bandwidth vs dielectric thickness.

Our previous work [14] modeled the pad capacitor circuit for a VCSEL with a series resistance, R_p, in order to fit the measured data. In that work, the bottom plate of the parasitic pad capacitor consisted of p-type semiconductor mirror stack, and the observed series resistance was attributed to the moderate resistivity of the semiconductor material. The present work indicates that the physical origin of most of this equivalent resistance is in fact dielectric loss.

5.6 Debye and Cole-Cole Models

A commonly used model of the complex relative permittivity at microwave and lower frequencies is the Debye model [41,43] given by

$$\varepsilon^*(\omega) = \varepsilon_\infty + \frac{\varepsilon_{dc} - \varepsilon_\infty}{1 + (jf / f_{peak})} \tag{5.7}$$

where f is the frequency, f_{peak} is the relaxation frequency at which the dielectric loss peaks, ε_{dc} is the dielectric constant at dc, and ε_{∞} is the dielectric constant at $f>>f_{peak}$. A key advantage of the Debye model is that its inverse Fourier transform is an exponential function which permitted the development of numerous computationally effective algorithms to incorporate Debye materials into finite difference time domain simulations (FDTD) [43,49]. Conversely, the Debye model is often a poor predictor of the dielectric performance of most physical materials since the original Debye treatment for polar molecules assumes that the molecules are spherical in shape and as a result the axis of rotation has no effect on the value of $\varepsilon^*(\omega)$. Furthermore, it neglects the interactions between the molecules in the dielectric material [43] that in practicality are not negligible [51]. Accordingly, the Debye model incorporates only one relaxation frequency f_{peak} [49].

More accurate models account for molecular interactions [52,53] and for asymmetric molecular shapes [52]. An example of such an improved model is that of Cole-Cole [43,54],

$$\varepsilon^*(\omega) = \varepsilon_{\infty} + \frac{\varepsilon_{dc} - \varepsilon_{\infty}}{1 + (jf / f_{peak})^{1-\alpha}} \tag{5.8}$$

where α is an experimental fitting parameter in the range $0 \le \alpha \le 1$. The Debye model is a special case of the Cole-Cole model when $\alpha=0$. It should be noted that the Cole-Cole model's non-integer value of α hinders its inclusion in FDTD computations [49].

To investigate the applicability of the two models mentioned above, approximate values of ε_{∞} for all four dielectrics were estimated utilizing the Cole-Cole plot (ε' on the

x-axis and ε'' on the y-axis) and extrapolating the values of ε for $f \to \infty$ using equation (5.8). A best fit for each dielectric material was achieved by allowing the values for f_{peak}, ε_∞, and α to vary. Values of f_{peak} for HD-8000, PI-2723, BCB-4024, and IC1-200 were 30GHz, 32GHz, 33GHz, and 25GHz respectively. Table 5.4 lists the dielectric relaxation times ($\tau_o=1/2\pi f_{peak}$), α, ε_∞ and 95% confidence limit for HD-8000, PI-2723, BCB-4024, and IC1-200. By applying values of f_{peak} and ε_∞ in equation (5.7) plots for the Debye model were also obtained. Figure 5.13 below illustrates the Cole-Cole plots obtained from experimental measurements, the Debye model, and the Cole-Cole model. The measured curves are very close to a circular arc in conformity with the Cole-Cole model [52,54].

Table 5.4 Values of τ_o, α, ε_∞ and 95% confidence limits.

Specific variety	τ_0 **(ps)**	α	ε_∞	**95% Log(τ/τ_0) C.I.**
HD-8000	5.31	0.10	2.7	± 0.22
PI-2723	4.97	0.11	3.1	± 0.23
BCB-4024	4.82	0.20	2.4	± 0.40
SOG IC1-200	6.36	0.48	1.2	± 0.62

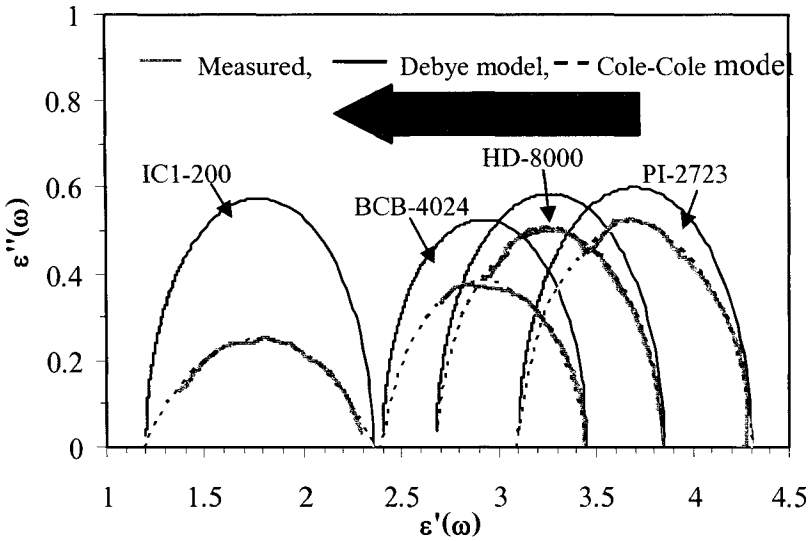


Figure 5.13 Cole-Cole complex plane plots obtained from experimental measurements, Debye model and Cole-Cole model.

Based on the plots presented in Figure 5.13 it is concluded that there are considerable inter-molecular interactions in organic polymers and SOG [53,54]. Furthermore, the results presented here support the claim in [53] which states that the simple Debye model cannot adequately describe the relaxation process in these materials. However, the Cole-Cole model well describes the experimental data.

Most materials require a finite time for polarization to occur. This time dependence results in a relaxation time τ that is defined as the time interval characterizing the restoration of distributed molecules to their equilibrium state under the effect of an electric field. For dielectrics which cannot be described by the Debye model (one relaxation time), several analytical relations that give a relatively good agreement with the experimental data reported here have been proposed to describe the relaxation time distribution function $G(\tau)$ [35,36,54,55]. The Cole-Cole relaxation relation corresponds to a superposition of a group of Debye processes with a range of relaxation times distributed around τ_o.

5.7 Conclusions

In this chapter, on-wafer, parallel-plate capacitors were fabricated from four different spin-on dielectrics. Multiple dielectric thicknesses were used for the three organic dielectrics. Microwave reflection coefficients, S_{11}, were measured up to 40GHz. Dielectric permitivity and losses as a function of frequency were extracted from measured microwave reflection coefficients, S_{11}, of the capacitors. The dielectric permittivity is well approximated by a second degree polynomial, while the dielectric loss and tangential loss peak in the 25GHz to 34GHz range. A circuit model for the fabricated capacitor was obtained with a minimum square error of less than 10^{-4} between measured and modeled reflection coefficients. Measurements of organic polymer losses at different thicknesses show a linear trend proportional to thicknesses with different slopes. The Cole-Cole model, which accounts for molecular shapes and interactions in organic polymers and SOG, provides a good fit to the measured data.

For applications to high speed devices, thicker dielectrics result in lower pad capacitance but also higher losses. Accordingly, devices with capacitive pads in 50Ω invireomants have 3dB bandwidths that increase with increasing dielectric thickness, but not as rapidly as simple lossless models would predict. Obtaining models that describe the complex dielectric behavior for high speed devices will improve device simulation and provide more accurate performance predictions. With respect to developing an equivalent circuit model for high speed VCSELs, it is concluded that the remaining un-etched mirror stack under the VCSEL pad has no considerable loss and the dielectric provides the majority of loss in the pad capacitor.

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Chapter 6

ACHIEVEMENTS, CONCLUSIONS AND FUTURE WORK

This chapter summarizes the achievements of the research discussed in this dissertation. Conclusions and suggestions for future work are given based on these achievements.

Section 6.1 will summarize achievements related to the fabrication process development of top- and bottom-emitting devices. It will also discuss the results achieved using the fabricated top- and bottom-emitting flip-chip bonded VCSELs based on various epitaxial structures, and it will conclude with the modeling results. Conclusions are presented in Section 6.2 and suggestions for future work in the quest of high-speed VCSELs are presented in Section 6.3.

6.1 Achievements

The overall objective of this research is to fabricate high-speed oxide-confined vertical-cavity surface-emitting lasers based on new VCSEL structures specifically designed to reduce the electrical and thermal constraints on modulation bandwidth. The developed structures are top- and bottom-emitting, copper-plated VCSELs with special structural considerations. To achieve this objective, the parameters that affect VCSEL speed as well as the fabrication steps required to fabricate high-speed VCSEL structures have been investigated. Below is a summary of the achievements. Much of this work has been published in journals, conference presentations, and poster sessions [1-6].

6.1.1 Process development

1) New mask sets were designed with a flexibility that enables the investigation of various VCSEL structures that include top-emitting, bottom-emitting, self-aligned, and non-self-aligned structures. The new design also allows intermediate DC testing for the devices, which saves time in the event of bad wafers and/or process errors. Furthermore, the self-aligned process relieves the alignment resolution requirements by up to 3-4μm, as explained in detail in Section 3.3.2.2.
2) Complete fabrication processes for top-emitting, self- and non-self-aligned 850nm and 980nm high-speed VCSELs were developed [1,3,5,6].
3) A complete fabrication process for bottom-emitting, non-self-aligned, flip-chip bonded 980nm high-speed VCSELs was developed.
4) Some of the critical fabrication steps that affect the high-speed oxide-confined VCSEL's speed were determined and controlled. For example: Accurate control of the mesa etching to stop within a few layers after the layer with highest aluminum content (oxidation layer) reduces the bottom mirror series resistance. Also, accurate control of the oxidation process parameters such as the control of the sample real temperature rather than the furnace reading by installing a thermocouple inside the oxidation tube is important for repeatable and identical oxide-confined VCSEL fabrication. Finally, modification to the Cu electroplating setup combined with the proper plating chemicals and conditions improved the plated Cu density and adhesion properties.

6.1.2 Top-emitting VCSELs

1) Self-aligned top-emitting 850nm high-speed VCSELs were fabricated and characterized using the first generation of the photomask layout and the fabrication processes presented in Chapter 3. The self-aligned process allows smaller mesa diameters for a given aperture size, thus decreasing the distance for heat flow to the sidewall as well as mesa capacitance. VCSEL mesa capacitance was reduced by 49% compared to values reported before [7,8]. The effect of a heat-sinking layer on the performance of the 850nm VCSELs was demonstrated in a preliminary experiment. Au-wrapped and Cu-plated heat-spreading layers reduced the thermal resistance by 25% and 44%, respectively [1,6], and the output power was increased by 17% and 38%, respectively, compared to similar VCSELs [7] without the Cu plated heatsink. The fabricated lasers exhibited a 3dB modulation frequency bandwidth up to 16.3 GHz [1,6], which is 12% higher than that reported in [7] at about 8.9kA/cm^2 current density compared to 50kA/cm^2 required to achieve this bandwidth before [9]. The lower operating current density improves the device reliability [10].

   Modulation bandwidth limitations due to parasitic capacitance for the 850nm fabricated devices were investigated. Due to the overlap of the plated Cu that extends to about 6μm around the mesa, PSpice simulation indicated that the purely electrical circuit effects would allow a maximum 3dB bandwidth of ~15.6GHz, which is very close to the measured value of 16.3GHz. By limiting the plated Cu extension to 2μm, a simulation pointed out that the purely electrical circuit effects would allow a maximum 3dB bandwidth of about 63GHz [1]. It is believed that the Cu-plated VCSELs are limited by electrical parasitics rather than thermal effects.

2) The effect of a heat sinking layer on the performance of high-speed, non-self-aligned top-emitting 980 nm VCSELs was demonstrated in an improved design and controlled process using the second generation of the photomask layout and the fabrication processes discussed in Chapter 3. Increasing Cu-plated heatsink radii from 0μm to 4 μm greater than the mesa in 980nm VCSELs reduced the measured thermal resistance for a range of device sizes to values 50% [3] lower than previously reported over a range of device sizes (see Figure 4.46). For a 9μm diameter oxide aperture, the 4 μm heatsink increases output power and modulation bandwidth by 131% and 40%, respectively [3]. The functional dependence of thermal resistance on oxide aperture diameter indicates the importance of lateral heat flow to mesa sidewalls. The measured 3dB modulation frequency bandwidth was up to 9.8 GHz at 10.5 kA/cm^2 compared to 20 kA/cm^2 [11] required to achieve similar bandwidth. Although the second generation devices (Novalux 8.59) increased output power and modulation bandwidth by 131% and 40% [3], respectively, compared to only 38% and 12% [1] for the first generation devices (EMCORE), still the first generation VCSELs exhibited 16.3GHz of modulation bandwidth compared to 9.8GHz bandwidth for the second generation devices. This case is a good example of the importance of the epitaxial material optimization for high speed operation. (See Table 4.1 for epitaxial material comparison.)

3) Using the modified and more controlled process used in fabricating the devices reported in achievement 2, an improved heat-sinking effect on the performance of high-speed non-self-aligned 850nm VCSELs was demonstrated. For devices with a 10μm active diameter, the second generation of 850nm Cu plated devices exhibited a

reduced thermal resistance by 57%, 52%, and 45% compared to polyimide-wrapped [7], Au-wrapped and Cu-plated first generation devices [1], respectively (see Figure 4.46). The lasers exhibit modulation bandwidths up to 18 GHz at current densities of only 8kA/cm^2 (see Figure 4.49) and an MCEF as high as 15.6GHz/mA$^{1/2}$. Due to calibration uncertainty and amplifier response issues, there is some uncertainty related to the reported bandwidth (i.e., the reported 18 GHz bandwidth might be more or less).

4) The effect of external heating on the VCSELs' resonance frequency and damping factor was demonstrated in a preliminary experiment. Increasing the stage temperature tends to reduce both the resonance frequency and the damping factor, hence limiting the modulation bandwidth of the VCSEL (see Figure 4.35). Based on the relationship between the damping and the resonance frequency squared, the maximum intrinsic 3dB frequency bandwidth was estimated to be 24.7GHz (see Figure 4.36).

5) As the contacts of the self-aligned VCSELs go through annealing, etching, and oxidation, experiments using Ti-Pd-Ti-Au-Ti-Pd and Ti-Ni-Ti-Ni metal systems were performed on samples with different treatments to investigate the effect of these processes on the specific contact resistance. The later metal system exhibited a lower specific contact resistance relative to the former one.

6.1.3 Bottom-emitting 980nm VCSELs

1) Bottom-emitting non-self-aligned 980nm devices were fabricated using the first generation of mask layout and fabrication process. As discussed in detail in Chapter

3, only results from devices before flip-chip bonding were obtained. VCSELs with an 8μm oxide aperture exhibited a threshold current of 0.5mA, a threshold voltage of 2V, a series resistance of 228Ω, and slope and wall plug efficiencies of 71% and 47%, respectively. The relatively high value of the device resistance might be due to the fact that the oxidation layer was missing, while the high threshold voltage might be due to the type of doping used.

2) Using the second generation of mask layout and process parameters, bottom-emitting non-self-aligned flip-chip bonded 980nm devices were fabricated and characterized. VCSELs with 10μm active area have a threshold current and a slope efficiency of 0.6mA and 80%, respectively. The flip-chip bonding increased the maximum output power for VCSELs with active diameters of 10, 14, 16, and 20μm by 10, 11, 19, and 25%, respectively (see Figure 4.51). Based on the relative power increase, it is concluded that as the device's active diameter gets smaller, the vertical heat-sinking provide by the flip-chip bonding is less efficient and a lateral heat-sinking mechanism needs to be introduced, as discussed later in this chapter. Even with no antireflection coating, the output light intensity seems to be clean from the typical ripples associated with bottom-emitting (substrate side) VCSELs' output light intensity.

6.1.4 Modeling

1) To better model the high-speed devices and get better ideas about how to lower the parasitic capacitance associated with the high-speed VCSEL metal pads, the dielectric properties of four different spin-on dielectrics that can be used for planarization were

investigated [2]. Thicker dielectrics result in lower parasitic pad capacitance but also higher losses, as discussed in Section 5.7.

2) A circuit model for the pad capacitance is obtained based on geometrical and physical considerations [2]. Due to their small values, the capacitor plates' DC resistance, AC resistance, and skin effect were neglected in the model. It is concluded that the remaining un-etched mirror stack under the VCSEL pad has no considerable contribution to the loss as opposed to previous reports [7], and the physical origin of most of this equivalent resistance is in fact dielectric loss in the pad capacitor [2].

6.2 Conclusions

We have fabricated and characterized high-speed oxide-confined VCSELs with high-speed performance.

The effect of a heat-sinking layer on the performance of high-speed VCSELs was demonstrated for VCSELs operating at 850nm and 980nm wavelengths [1,3,6]. The presence of heat-spreading layers reduces the thermal impedance, increases the maximum output power, and increases the f_{3dB} modulation bandwidth. For top-emitting 850nm devices, plated Cu reduced their thermal resistance by up to 126% compared to other methods of heatsinking [7]. As for the maximum output power and the f_{3dB} bandwidth, top-emitting VCSELs with 4μm heatsink increase the output power and modulation bandwidth by 131% and 40%, respectively [3].

Other than the electroplating technique for top-emitting VCSELs, the flip-chip bonding of bottom-emitting 980nm devices presented also demonstrated its effect on the

VCSEL performance. The flip-chip bonding increased the maximum output power for a 20μm active diameter bottom-emitting VCSEL by up to 25%.

The flip-chip bonding effect on the bottom-emitting VCSELs' performance is less than that for top-emitting ones. The thermal resistance measurements for top-emitting devices with only the top of the mesa Cu plated compared to adjacent devices with the mesa top and sidewalls plated with Cu indicates the importance of lateral heat flow to the mesa sidewalls which is a mechanism that is missing from the flip-chip bonded VCSELs configuration.

Due to the overlap of the wrapped Au and plated Cu with silicon nitride, which extends around the mesa, there is a new parasitic capacitance that adds to the total pad capacitance [1]. As a result, there is a tradeoff between the heat-spreading layer thickness for thermal impedance reduction and the resulting parasitic capacitance for high-speed operation [1].

The reduction in the resonance frequency and damping factor due to the increase in stage temperature is believed to cause the VCSEL's modulation bandwidth to saturate, which further emphasizes the effect of the VCSEL's heating on its performance. Possible reasons for such a decrease in both the resonance frequency and damping factor might be related to the decrease in photon density and/or the decrease in differential gain and/or the increase in photon lifetime.

Although the specific contact resistances for both Ti-Ni-Ti-Ni and Ti-Pd-Ti-Au-Ti-Pd metal systems were within the range of typical values ($\sim 10^{-6}$ Ω-cm^2), the fabricated device's L-I characteristics still suffer from nonlinearity and high threshold voltages.

Since the oxidation length is short, precise control of the oxidation process parameters is important for repeatable and identical oxide-confined VCSEL fabrication. Moreover, scaling down both the mesa diameter and the active area will reduce the VCSEL self-heating since the threshold current will be reduced. The mesa parasitic capacitance will decrease as well since the oxide length is also reduced.

The use of photosensitive HD-8000 polyimide gave reliable and repeatable results [2,7]. The polyimide was incorporated in the fabrication process for both top- and bottom-emitting devices for different reasons. For top emitting devices, it was used for planarzation, passavation, and lower parasitic pad capacitance. For bottom emitting flip-chip devices, it was used as an insulator to prevent the device mesa *pn* junction from shorting during the flip-chip bonding process and to simultaneously modify the ground mesa sidewalls' profile for easier and guaranteed step coverage.

With proper wafer VCSEL design and electrical parasitic circuit element reduction, along with good thermal characteristics, we expect that it is possible to improve the current high-speed VCSELs' performance, which will open more application areas for VCSELs.

6.3 Future work

While much has been done to improve the VCSEL's performance, whether by our group or by other groups, many issues still need to be investigated and addressed to push the VCSEL's performance and applications further. Due to time limitations and other issues, in this section I discuss some issues and suggestions that may improve our

understanding of current high-speed VCSELs' performance limitations and help reduce those limitations.

Although the self-aligned process allowed fabrication of smaller mesa diameters for a given aperture size using the current fabrication process, more fabrication runs need to be done to optimize the high-speed oxide-confined VCSEL fabrication process to push the operating devices' mesa diameter to a smaller size, thus furthering heat flow improvement, mesa capacitance reduction, and mode control. One of the issues that the self-aligned process suffered from is the degradation of the ohmic contact resistance as the devices go through different fabrication processes such as etching and oxidation. To identify the cause of this degradation and develop a metal contact system that maintains a low contact resistance under these harsh fabrication conditions, it is recommended that the following be done:

1- Review literature for already developed metal contact systems.

2- Identify possible metal contact system candidates for the self-aligned process.

3- Design of experiment (DOE), fabrication of different metal contact systems, and exposing them to the different fabrication steps they are expected to go through during the real VCSEL fabrication process.

4- Using more advanced diagnostic techniques such as Auger depth and surface survey profiling.

Whether the VCSELs were self-aligned or non-self aligned the fabricated devices in this work suffered from high threshold voltage values and nonlinear I-V characteristics. This issue needs to be resolved as it causes impedance mismatch when the VCSELs are under large signal testing. It is recommended that the AuGe and BeAu evaporator

crucibles be checked for cross-contamination or mislabeling, which leads to using the wrong metal(s) type. I have used Energy Dispersive X-ray Spectroscopy (EDS) to check for contamination, but due to the small-cross section of the atoms of some of the metals involved such as Be, the EDS analysis was not conclusive. Thus, X-ray photoelectron spectroscopy (XPS) is recommended. Both EDS and XPS analysis are available through the Colorado State University/Central Instrument Facility [12].

The effect of the Cu-plated heat-sinking layer on the performance of high-speed VCSELs was demonstrated. But the tradeoff between the heat-spreading layer thickness and the overlap length for thermal impedance and parasitic capacitance reduction was not completely optimized. Experiments need to be done to answer the following question: At which thickness will further increase in the heat-sinking layer cease to have considerable effect on the VCSEL thermal resistance reduction?

While the present work was based on using plated Cu as a heat-sinking layer through a 1000 Å layer of SiN_x with a thermal conductivity from 0.08-0.3W/cm-K and a relative dielectric constant of ~7.5 [13], other materials with better characteristics can be used also. For example, CVD diamond is an interesting material as it is one of the hardest materials available, it has a wide optical transparency window [14], and very high thermal conductivities of ~15W/cm-K and ~20 W/cm-K [15] for in-plane and perpendicular, respectively, and lower relative dielectric contact of 5.6 compared to the corresponding values of SiN_x [13]. The use of CVD diamond will further improve the VCSELs' heat-sinking as well as reduce the parasitic capacitance associated with the overlap of the heat-sinking layer with the bottom contact, which was separated previously

by SiN_x. NASA has already investigated the effect of mounting VCSELs on CVD diamond substrates, as reported by H. C. Shaw and M. N. Ott [15].

It is important to develop a complete and repeatable fabrication process for bottom-emitting, self-aligned 980nm flip-chip bondable high-speed VCSELs. The current structure of the bottom-emitting flip-chip devices provided heat sinking through the top contact side to the substrate. To improve the heat sinking for theses devices, the device mesa sidewalls need to be plated with a heat sinking layer. While plating the sidewalls is expected to further improve the VCSELs performance, the use of HD-8000 polyimide to solve the bottom emitting flip-chip devices *pn* junction shortening in the current design is expected to limit the improvement due to the poor thermal conductivity of polyimide (0.002W/cm-K). It is suggested that the polyimide be replaced with SiN_x or even better with CVD diamond. S_{11}, S_{21}, and thermal impedance characterization of bottom-emitting devices including assessment of the limitations on bandwidth, should then be done.

The effect of external heating on the VCSELs' resonance frequency and damping factor was demonstrated in a preliminary experiment. In the present work, the relationship between the damping and the resonance frequency squared was fitted with the expression $\Gamma \sim Kf_r^2$ which has been used previously to be fitted to the damping as a function of the relaxation oscillation frequency squared at different bias currents but not different stage temperatures. To validate the use of $\Gamma \sim Kf_r^2$ for data at different stage temperatures the damping and the resonance frequency need to be measured for the same device under different bias currents with fixed stage temperature and under different stage temperatures at a fixed bias current. Next, the relationship between Γ and f_r^2

should be fitted with the expression $\Gamma \sim Kf_r^2$ for both cases and then the maximum intrinsic 3dB frequency bandwidth are estimated and compared.

Furthermore, the epitaxial structure design plays an important role in improving the VCSELs' performance since tradeoffs exist between different factors affecting high-speed operation. For example, the resonance frequency can be calculated using the following expression [16],

$$\omega_R = \left[\frac{\Gamma v_g a}{qV} \eta_i (I - I_{th}) \right]^{1/2}$$

where a is the differential gain, I_{th} is the threshold current, and I is the bias current. To obtain high ω_R, it is desirable to enhance the differential gain a, minimize the volume of the mode (Γ/V), and maximize the bias current I relative to the threshold current I_{th} for maximum bandwidth. But it turns out that the maximum differential gain occurs at a transparency that is far from ideal for minimizing the threshold current. As a result, a tradeoff exists between obtaining low threshold current and high differential gain. Thus, a reasonable compromise operating point needs to be achieved.

Another example is the tradeoff related to the amount of internal loss α_i and mirror doping. Low doping values results in low internal loss and thus a lower bias current is needed to achieve certain output power which result in less heating of the device. Lower doping values result in higher mirror series resistance, which the current has to pass through to reach the active region. This results in heating of the device, which in turn limits the maximum output power in the VCSEL. Consequently, a tradeoff exists between

obtaining low threshold current and low internal loss. Thus, a reasonable compromise operating point needs to be achieved.

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Appendix A: TRION Minilock II ICP etching system user manual (Ar, He, Cl_2, BCl_3, N_2, O_2)

This procedure is meant as a guide only. It is NOT a substitute for proper training. Users must exercise care while operating this machine and should be observant to any anomalies. If any problems are encountered with which the user is unfamiliar, immediately contact the ICP caretaker or other qualified person for assistance.

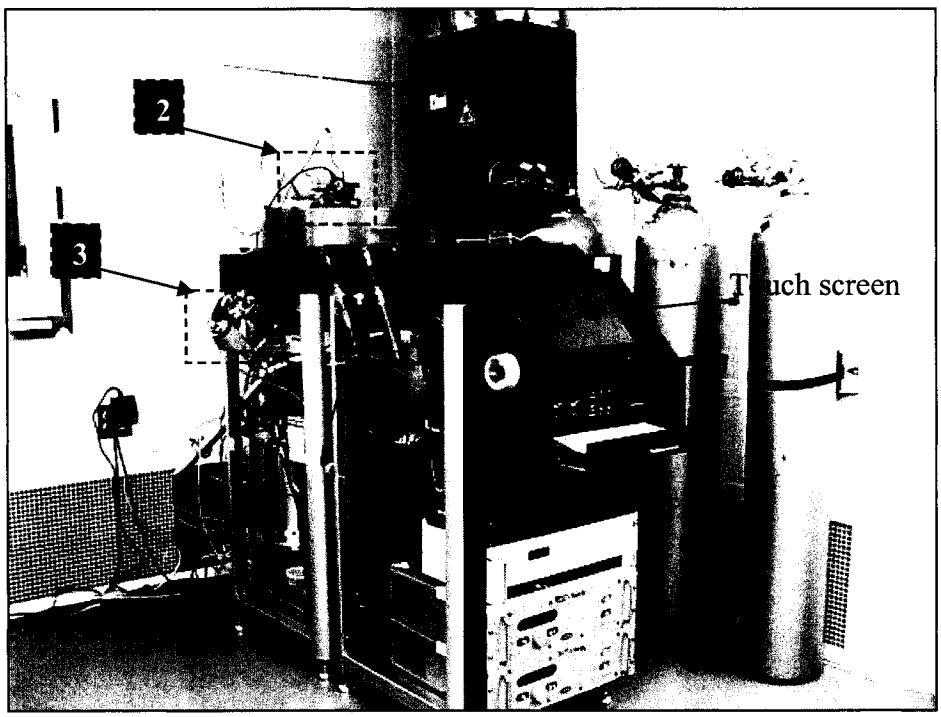

Figure 1 TRION Minilock III ICP etching system.


Figure 2 Baratron pressure gauge.


Figure 3 *In-situ* monitor.

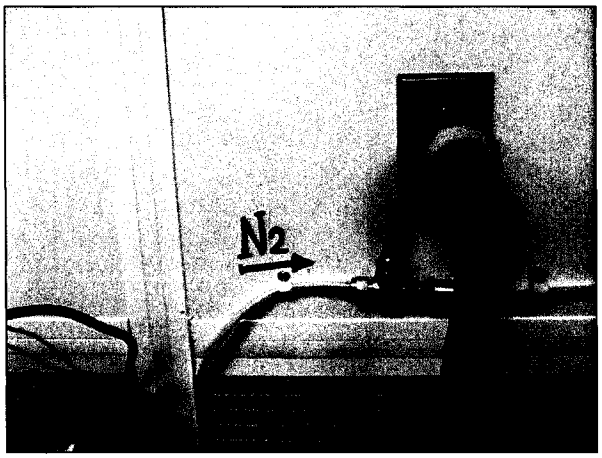

Figure 4 N_2 valve located under the transfer window.

Sample preparation:-

1- Take a fused silica wafer with a flat (WF3937X02031190) stored at the dry box located near the door between the white room and yellow room and clean it with acetone only. ***Handle with care as these wafers breaks easily.***

2- To get the sample to stick on the fused silica wafer, use the diffusion pump oil stored at the same place. Apply some at the back of the sample using the stick of a cotton swab.

3- Place the sample as close as possible to the center of the fused silica wafer. Don't place the sample elsewhere in the wafer and then slide it to the center as this will leave a trail of oil that later in the etching process might be deposited on the sample surface and damage it.

4- Due to the surface tension of the oil, the sample will stick to the fused silica wafer. The sample now is ready to be loaded into the ICP etching system.

Sample loading sequence:-

1- Make sure that the nitrogen gas valve shown in Figure 4 above, which is located under the transfer window, is opened. Typical N2 pressure is about 80psi. You can read this value from the gas pressure gauge located at the end of the service corridor. 2- Stand in

front of the ICP shown in Figure 1 and look to the touch screen, where you will see Figure 5 below displayed on the screen. ***Keep in mind that this is the state that you should leave the system at after you used it.*** Now, press **Cancel** and move to step 3.

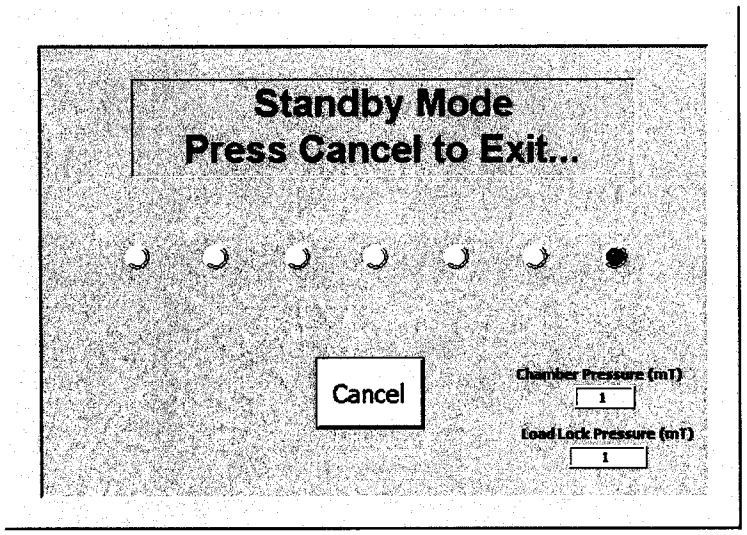

Figure 5

3- You will hear some valves closing and opening and the loading chamber will be vented through the valve shown in Figure 4 that you should have opened in step 1. When Figure 6 shown below is displayed on the screen, press **Load Wafer** and move to the next step.

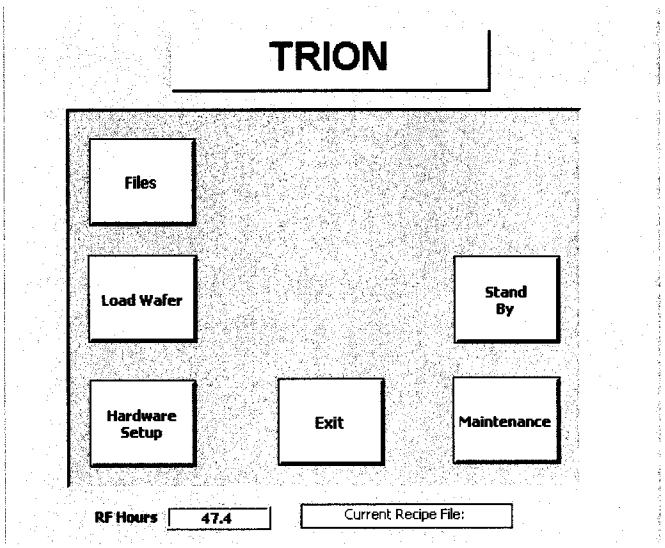

Figure 6

4- The loading chamber will open as shown in Figure 7 and Figure 8 will be displayed on the screen. In some rare cases when the compressed air pressure is less than 80psi, you need to push the door up with your finger tip just a little bit to help the door begin opening and then leave it. ***Do not force the door open.***

Figure 7

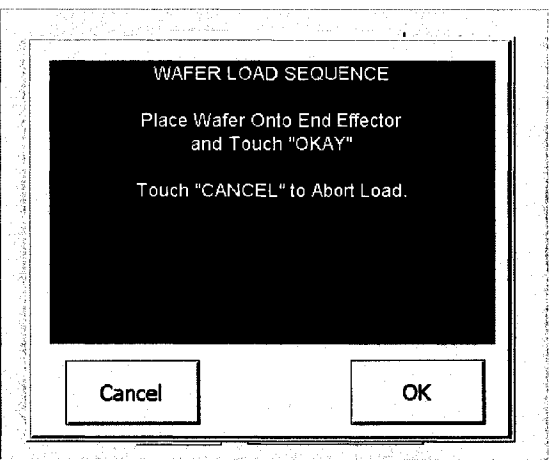

Figure 8

5- Follow the illustration shown in Figure 9 (a), (b), and (c) to load the wafer on the wafer holder (also called "End Effector") shown in Figure 7 above. Begin by placing the wafer on the wafer holder with the flat aligned to the angled corner edge as shown in Figure 9 (a) and (b). Then gently slide the wafer forward on the wafer holder tines until the edge of the wafer is even with the end of the tines as shown in Figure 9 (c). Next, press OK on the screen (Figure 8). The load lock door will close and the screen will display Figure 10 below and the system will begin to pump down the load lock chamber until the lock pressure (mT)=200, then you will hear the gate valve that separates the loading chamber from the etching chamber open and the robot arm will extend inside the etching chamber, load the sample, and retract. After this, the screen will display Figure

11 (a) or (b) below. If the screen displayed corresponds to Figure 11 (a), proceed to step 6; if it displays Figure 11 (b) skip step 6 and go to step 7.

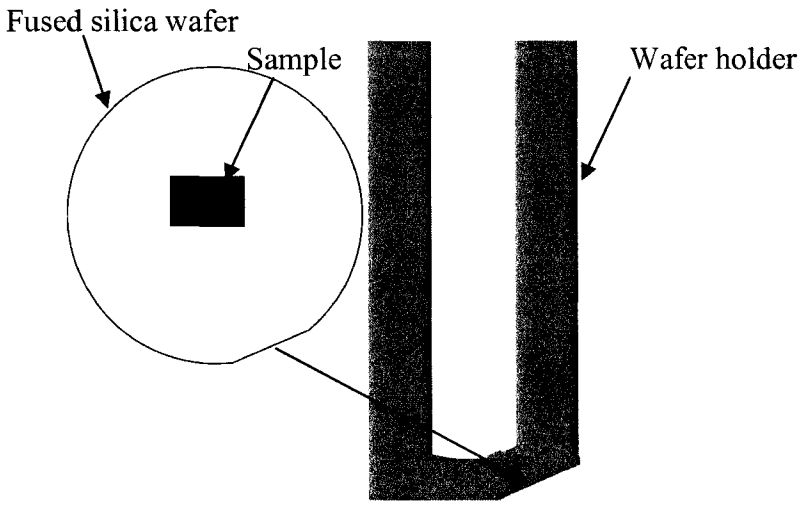

Figure 9 (a)

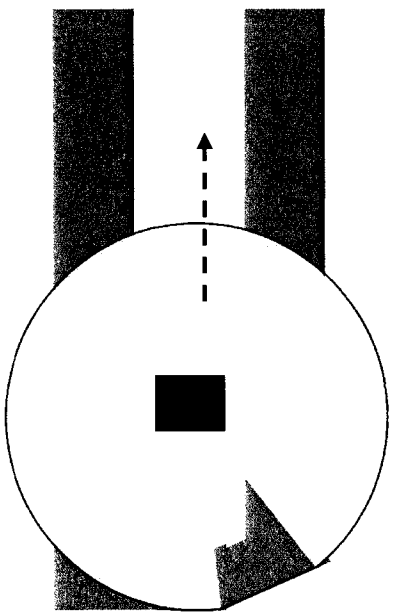

Figure 9 (b)

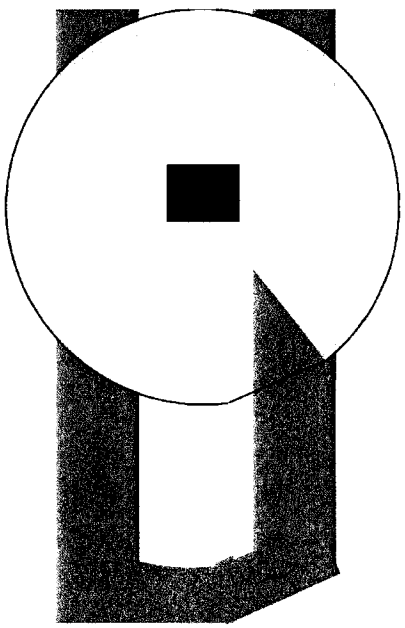

Figure 9 (c)

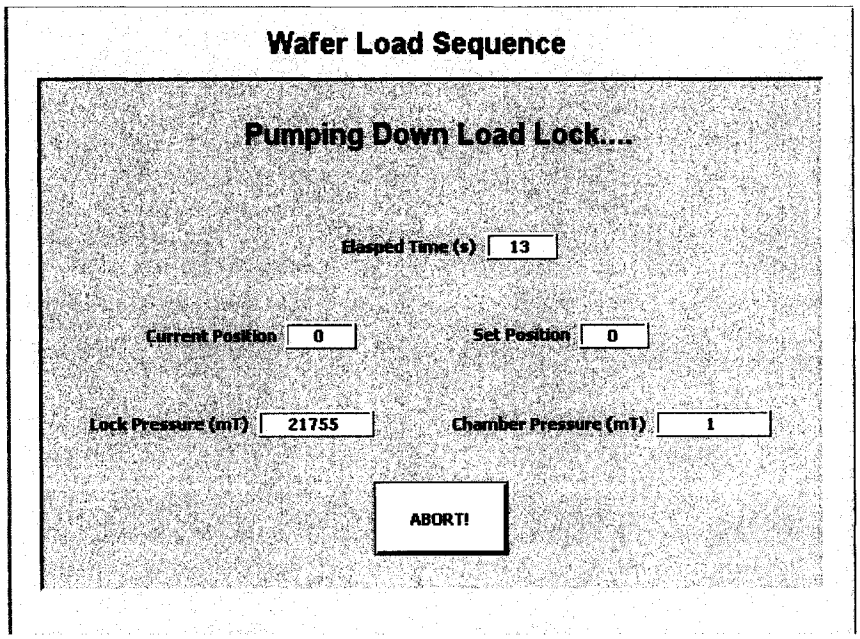

Figure 10

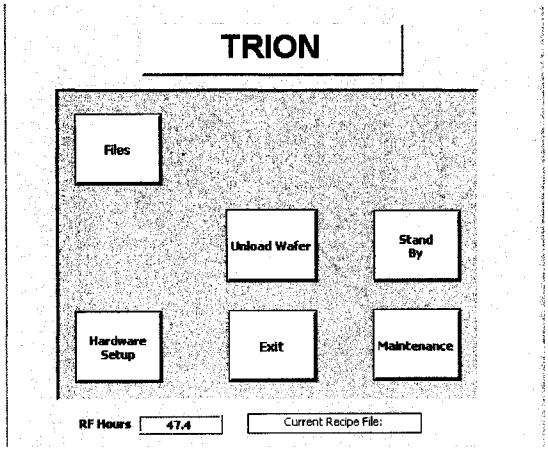

Figure 11(a)

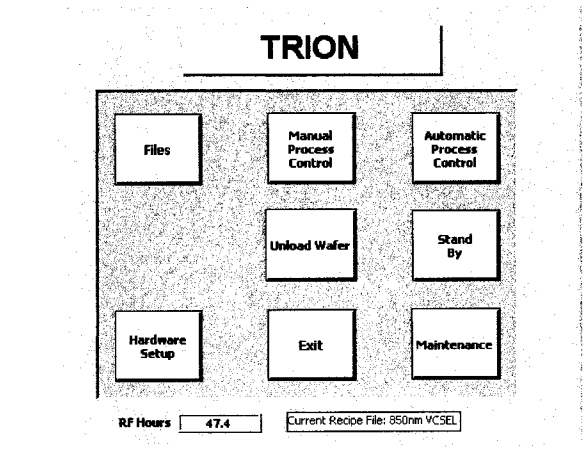

Figure 11(b)

6- At this point you need to choose a recipe file. Even if you think that none of the stored files fits your application, you need to choose one by pressing **Files** shown in Figure 11(a) above. After pressing **Files**, the screen will display a list of recipe files as shown in Figure 12 below. If you see a file that you know, used, or saved before, press on its name. Otherwise, press any file name and later you will be instructed on what to do if you

decided to load a different recipe file or modify the loaded recipe file. Next press **Exit** at the lower left corner of Figure 12 and move to the next step.

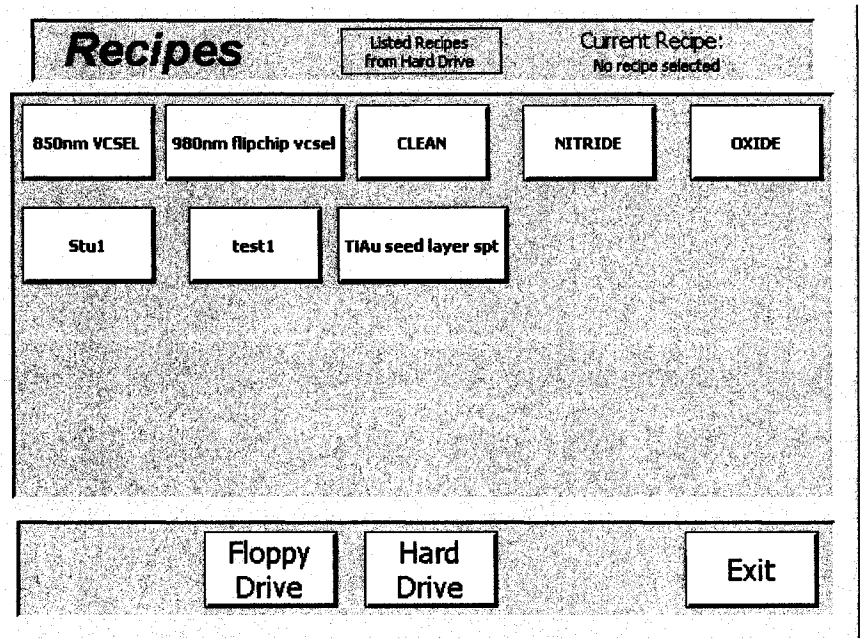

Figure 12

7- Now you see Figure 13 below on the screen. Press **Manual Process Control** and the screen will display Figure 14.

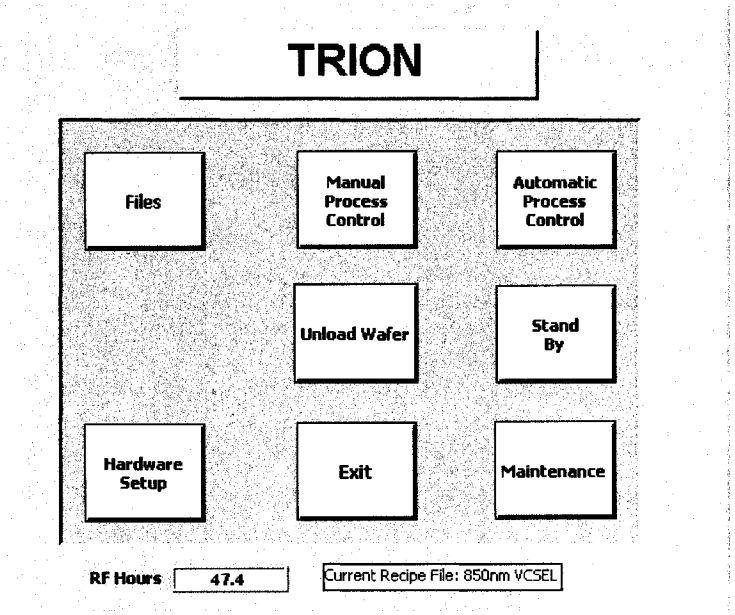

Figure 13

Figure 14 shows the different process parameters like pressure, ICP power, RIE power ...etc. Figure 14 below shows that the **Pressure Set** is **7.0**. If you want to change it, press the button that shows **7.0** and a keypad will appear. Type the pressure value you want and press ok and the **7.0** value will be changed to the new set value. You can change all the set values, using the same procedure to match your recipe. After setting all your process parameters to the required values you need to ***close the Baratron pressure gauge value shown in Figure 2 to protect the gauge from the process gases.*** To let the process gases flow into the chamber, press the gas toggle button, which initially reads **Gas Off** as shown in Figure 14 below. Pressing the button will cause it to turn green and display **Gas On** as shown in Figure 15.

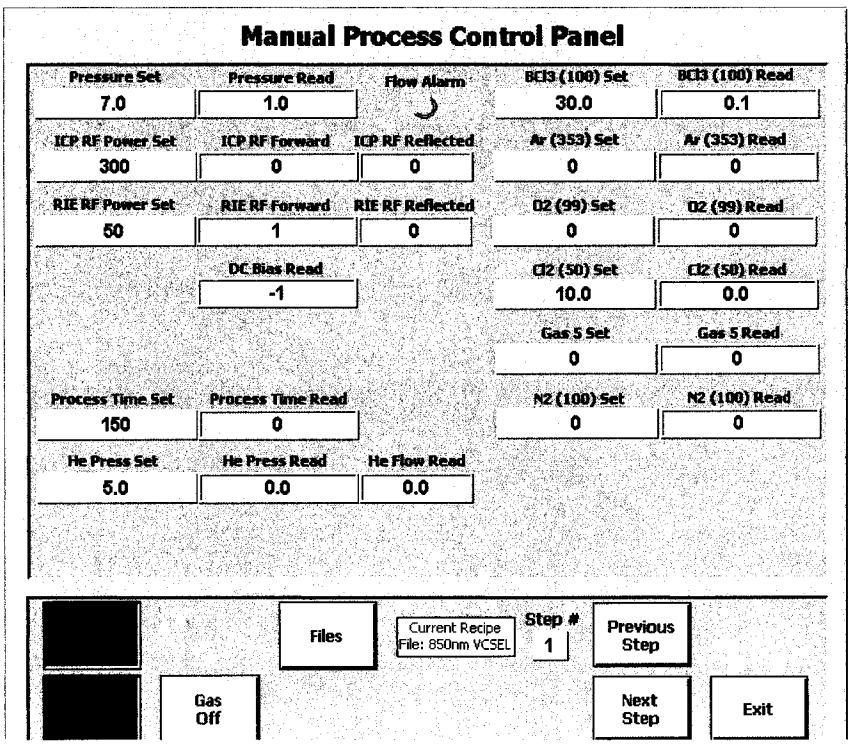

Figure 14

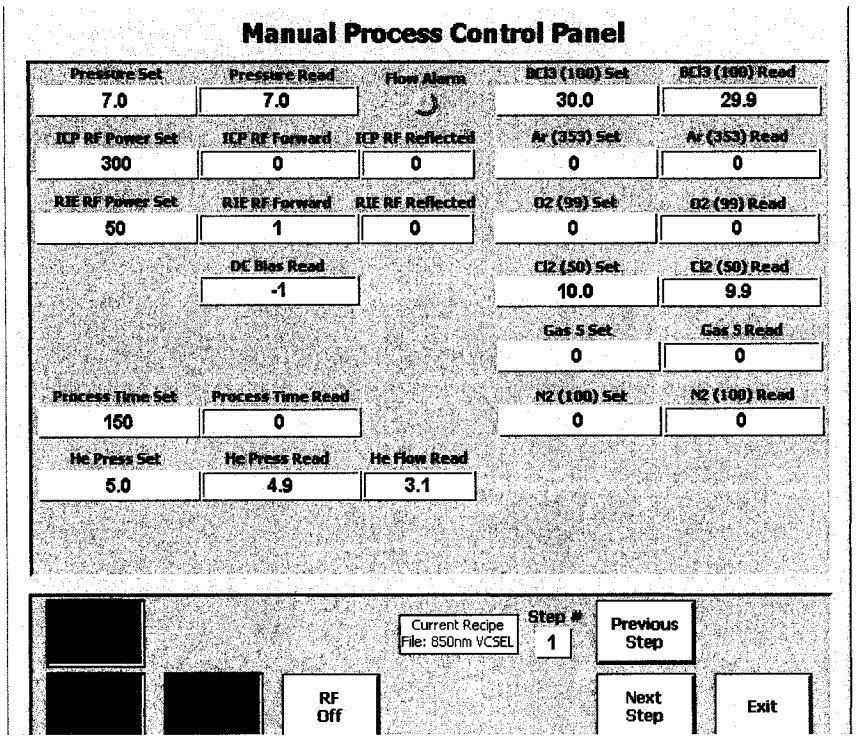

Figure 15

8- Allow the system to stabilize for 1 minute after turning on the process gas. At this point, you need to decide if you need to use the in-situ optical reflectance monitor shown in Figure 16 below. If not, skip this step; otherwise, proceed by logging into the computer located under the transfer window and double-click on the lab view icon "ICP". Next, turn on the laser power by connecting its power plug. Align the red laser beam to the center of the sample by looking through the edge of the top view port. **YOU NEED TO BE VERY CAREFUL TO KEEP YOUR EYE OUT OF THE DIRECT REFLECTION OF THE LASER BEAM FROM THE SAMPLE.** The aligned laser beam will be reflected from the sample and hit the photodiode shown in Figure 16 below. You might need to realign the photodiode so that most if not all the reflected laser beam hits the photodiode.

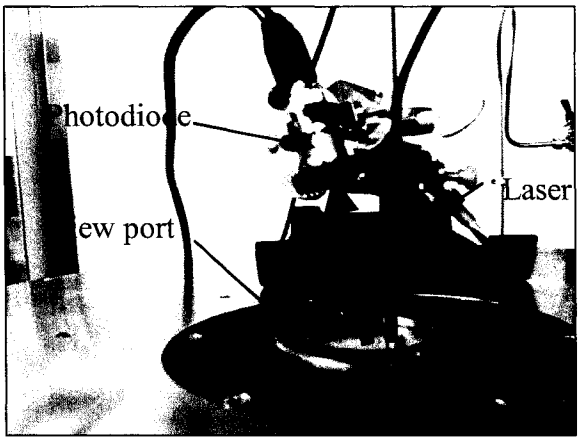

Figure 16 *In-situ* monitor.

9- Now you are ready to etch. If you are monitoring reflectance, start the LabView code you opened in step 8. Then press the RF toggle button, which initially reads **RF Off** as shown in Figure 15. You can use the **Process Time Read** shown in Figure 17 below to decide when to stop etching for a timed etch or you can use the real time reflectivity measurements displayed on the computer screen to determine when you have etched the appropriate number of layers. Since etch rates can vary some depending on the sample and other parameters, using the reflectance monitor is preferable. When you decide to stop etching, press the RF toggle button currently marked **RF On** as shown in Figure 17 below. It should then change to **RF Off**.

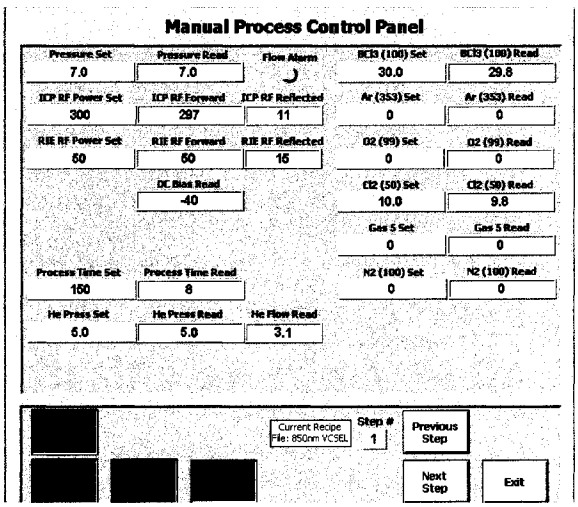

Figure 17

10 – Wait for about 30 seconds to allow the sample to cool down under gas flow, which helps to carry away heat from the sample. Now press the gas toggle button initially showing **Gas On** as shown in Figure 18 until it shows **Gas Off** and wait for 5 minutes to make sure that all the process gases are pumped out. Next, press **Exit** as shown in Figure 19 below.

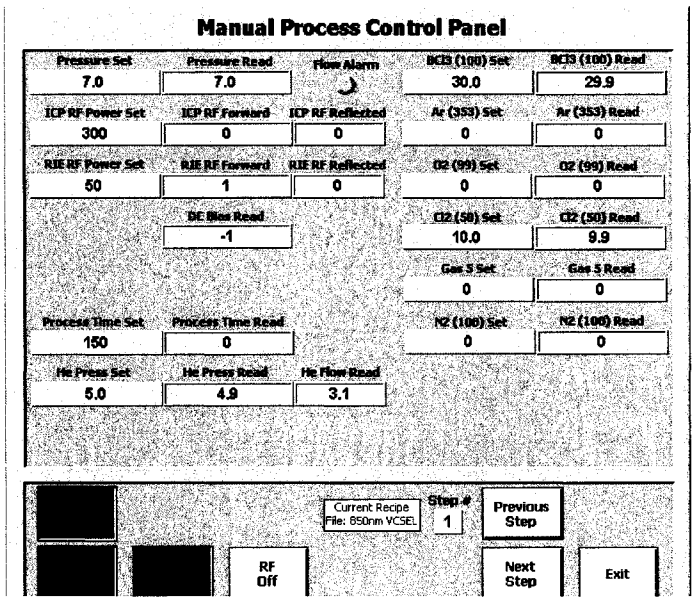

Figure 18

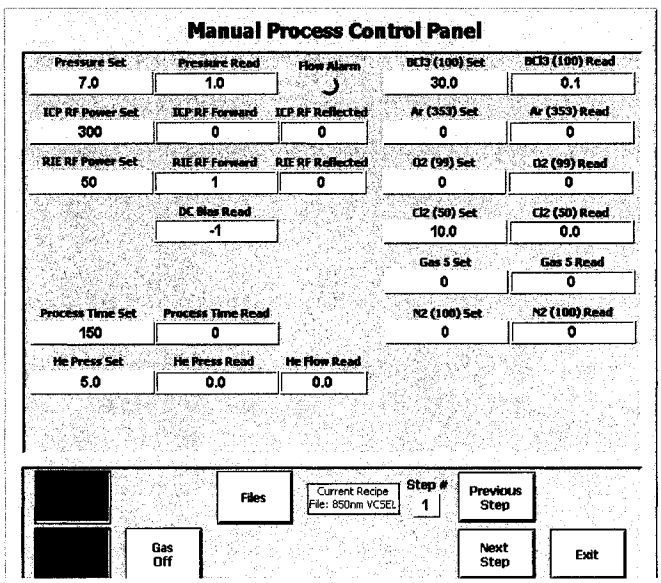

Figure 19

Sample unloading sequence:

11 – To unload your sample, press the **Unload Wafer** shown in Figure 20. The gate valve will open, the robot arm will extend inside the etching chamber and retract with the sample, the gate valve will close, and the loading chamber will be vented and its door will open as shown in Figure 7. The screen will display Figure 21 below. Remove your sample and press **OK** as shown in Figure 21. This will cause the load lock door to close and Figure 22 will be displayed.

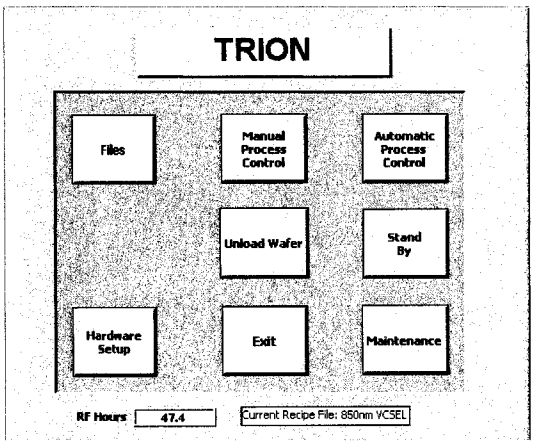

Figure 20

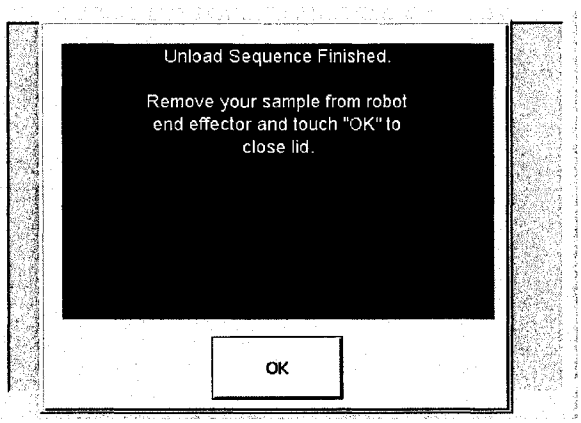

Figure 21

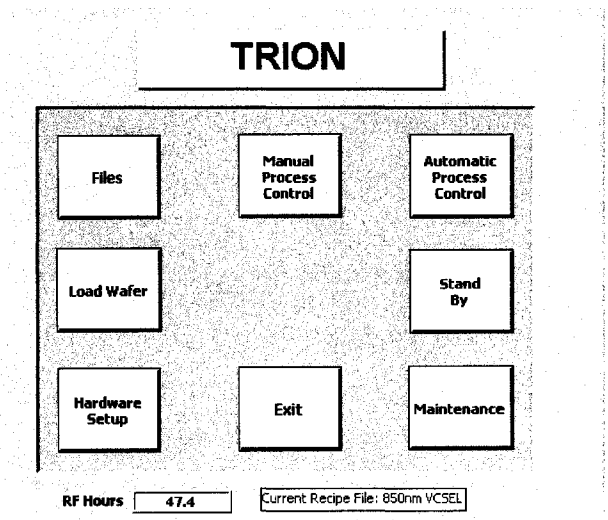

Figure 22

12- To load another sample, press the **Load Wafer** button as shown in Figure 22 above and go to step 3. If you are not immediately using the system for another etch, press the **Stand By** button also shown in Figure 22 and the screen will display Figure 23. Next, open the pressure gauge valve you closed in step 7 (shown in Figure 2), but remember to close it at the appropriate step for any later etches.