DISSERTATION

IMPACT OF BACK–CONTACT MATERIALS ON PERFORMANCE AND STABILITY OF CdS/CdTe SOLAR CELLS

Submitted by

Samuel H. Demtsu

Department of Physics

In partial fulfillment of the requirements

for the Degree of Doctor of Philosophy

Colorado State University

Fort Collins, Colorado

Summer 2006

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

UMI Number: 3233335

INFORMATION TO USERS

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleed-through, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

UMI®

UMI Microform 3233335

Copyright 2006 by ProQuest Information and Learning Company.

All rights reserved. This microform edition is protected against unauthorized copying under Title 17, United States Code.

ProQuest Information and Learning Company
300 North Zeeb Road
P.O. Box 1346
Ann Arbor, MI 48106-1346

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

COLORADO STATE UNIVERSITY

June 14, 2006

WE HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER OUR SUPERVISION BY SAMUEL H. DEMTSU ENTITLED IMPACT OF BACK–CONTACT MATERIALS ON PERFORMANCE AND STABILITY OF CDS/CDTE SOLAR CELLS BE ACCEPTED AS FULFILLING IN PART REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY.

Committee on Graduate Work

Advisor

Department Head

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

ABSTRACT OF DISSERTATION

Impact of Back-contact Materials on Performance and Stability of CdS/CdTe Solar Cells

Thin-film CdTe based solar cells are one of the leading contenders for providing low-cost and pollution-free energy. The formation of a stable, low resistance, non-rectifying contact to p-CdTe thin-film is one of the major and critical challenges associated with this technology in the fabrication of efficient and stable solar cells.

The premise of this thesis is a systematic study of the impact of back-contact materials on the initial performance and the degradation of CdS/CdTe solar cells. Two different back-contact structures that incorporate Cu as a key element are investigated in this study: (a) $Cu_{1.4}Te$:HgTe-doped graphite and (b) evaporated-Cu back contacts.

The effect of Cu inclusion is not limited to the back–contact layer where it is deposited. Cu is a known fast diffuser in p-CdTe, and therefore, a significant amount of Cu reaches both the CdTe and CdS layers. Hence, the effect of the presence of Cu on the individual layers: back-contact, the absorber (CdTe), and the window (CdS) layers is discussed respectively. The effect of different metals used to form the current-carrying electrode following the Cu layer is also evaluated.

Devices are studied through current-voltage (JV) measurements at different temperatures and intensities, quantum efficiency (QE) measurements under light and voltage bias, capacitance-voltage (CV), drive-level-capacitance-profiling (DLCP), and time-resolved photoluminescence (TRPL) measurements. Numerical simulation is also used to reproduce and explain some of the experimental results.

In devices made without Cu, a current-limiting effect, rollover (distortion) in the

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

current-voltage characteristic, was observed. With the inclusion of a small amount of Cu (5-nm), however, the distortion disappeared, and higher FF was obtained. The performance of these devices was comparable to devices made with the standard Cu-doped graphite paste contacts when the same CdTe absorber is used.

Small amount of Cu (5-20 nm) partially diffused into the CdTe absorber layer resulted in increased hole density, and improved V_{oc}. However, excess Cu (100 nm) created recombination centers that significantly reduced the FF and V_{oc}. The presence of Cu in the CdS window layer had minimal effect on device performance. It was found, however, to be responsible for anomalies such as dark/light crossover and distortions in apparent quantum efficiency, neither of which has a direct impact on the device performance.

Numerous metals: Au, Cr, Pd, Pt, and Ni were evaporated, following the Cu layer, and were found to form good current-carrying electrodes. Ag and Al, however, did not perform well in this role.

With exposure to elevated temperature (60–120°C) for extended period of time, diffusion of Cu from the back contact was found to cause back-contact degradation and additional increases in CdTe recombination. This degradation resulted in a reduced fill-factor, due to the formation of the Cu-depleted blocking contact and the consequent reduction in collection efficiency.

Samuel H. Demtsu
Department of Physics
Colorado State University
Fort Collins, CO 80523
Summer 2006

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Acknowledgements

I am very grateful to my research advisor, James Sites, for his guidance, stimulating suggestions and encouragement throughout my research for and writing of this thesis.

I thank the National Renewable Energy Laboratory (NREL) for funding my research and for giving me the opportunity to do research at the facility. I am deeply indebted to David Albin my mentor at NREL.

I express my sincere thanks to my committee members: Carl Patton, Robert Leisure and W.S. Sampath.

I gratefully appreciate the support of the following researchers of the National Renewable Energy Laboratory: Xuanzhi Wu, Wyatt Metzger, Tom McMahon, David Young, Anna Duda, Tom Moriarty, Joel Pankow, Sally Asher, and Steve Johnston.

I thank all the graduate students at the CSU's photovoltaic lab, Caroline Corwine, Ana Kanevce, Jun Pan, and especially Alan Davies and Tim Nagle for LBIC measurement, and for their critical review of this manuscript.

Finally, thanks to my wife Bizen, my daughter Saron, and my son Thomas for their patience and love during this time.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Contents

1 Introduction 1

1.1 Solar Energy and Solar Cells 1

1.2 Thin–film Cadmium Telluride (CdTe) solar cells 3

1.3 Fundamentals of Solar Cells 7

2 Back–Contact Barrier 18

2.1 CdTe/ Metal contact 18

2.2 Two–diode model 23

2.3 Barrier height determination 24

3 Device Fabrication and Data Analysis Techniques 34

3.1 Device Fabrication 34

3.1.1 Structure I (SnO_2/CdS/CdTe) 35

3.1.2 Structure II (Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe) 37

3.2 Data analysis techniques 39

3.2.1 Current – Voltage measurement 39

3.2.2 Quantum efficiency 41

3.2.3 Room-temperature Capacitance–Voltage measurement 43

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

3.2.4 Drive-level capacitance profiling (DLCP) 45

3.2.5 Time–resolved photoluminescence (TRPL) 48

3.2.6 Numerical Simulation 49

4 Role of Cu on performance of CdS/CdTe solar cells 51

4.1 Effect of Cu incorporation at the back-contact layer 52

4.2 Effect of Cu on the CdTe (absorber) layer 64

4.3 Effect of Cu on the CdS (window) layer 77

5 Stability of CdS/CdTe solar cells 87

5.1 Effect of stress temperature 87

5.2 Degradation of devices made with and without Cu at the back–contact . 91

5.3 Influence of a graphite layer at the CdTe/ back-contact interface on stability 93

6 Conclusions 100

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

List of Figures

1.1 A generic CdS/CdTe superstrate device structure (not to scale). 6

1.2 Energy band diagram of a n-CdTe/ p-CdTe homojunction. a) In the dark and b) under illumination, where the Fermi level E_F splits into separate levels for electrons and holes. 9

1.3 Energy band diagram of a n-CdS/ p-CdTe heterojunction. a) In the dark and b) under illumination. 9

1.4 Current–voltage characteristics of a generic solar cell with quadrants labeled according to standard convention. 12

1.5 Equivalent circuit model of a generic solar cell. 14

1.6 Effect of series and shunt resistances on the J–V curves: a) series resistance, b) shunt resistance, and c) series and shunt resistances. 15

1.7 Current–voltage analysis. 17

2.1 Ohmic and rectifying metal/p-semiconductor contacts. 19

2.2 J-V curve with rollover. 21

2.3 A two-diode equivalent circuit model. 23

2.4 Band-diagram of two non-interacting diodes in the light at zero bias (the two depletion regions, d_m and d_b, do not overlap). 24

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

2.5 Experimental and simulated J-V curve of a CdTe cell with a rollover. . . 28

2.6 The voltage drop across the main and the back diode as a function of the applied bias. 29

2.7 Effect of barrier height on CdTe current–voltage characteristics (simulated). 31

2.8 Reduction of fill-factor with increase in barrier height. Insert shows the diode saturation current J_{bo} as a function of the barrier height. 32

2.9 JVT-simulated 33

2.10 The effect of series resistance R_s on rollover 33

3.1 The SnO_2/CdS/CdTe structure: a) Cu-doped graphite contact, and b) evaporated-Cu contact. 37

3.2 The Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe device structure. 39

3.3 The global AM1.5 outdoors solar spectrum, and the spectrum of the solar simulator at CSU. 40

3.4 QE and current losses of a typical production cell. 42

3.5 (a) capacitance as a function of the applied bias, and (b) carrier density deduced from the C–V data as a function of the distance from the junction. 45

3.6 Trap energy level E_t with respect to the fermi energy level E_F. E_t crosses E_F at a distance X from the junction, and traps with energy above E_F are ionized. 46

3.7 Drive level carrier density as a function of distance from the junction. . . 47

3.8 A typical normalized time-resolved photoluminesence (TRPL) decay curve of a CdS/CdTe device. 49

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

4.1 The current-voltage curves of devices made with and without Cu in the graphite paste that forms the primary contact. 52

4.2 The effect of the graphite layer on the J–V curve. 53

4.3 J-V as a function of Cu thickness. 55

4.4 (a) Shunted dark and light J-V curves of the device with 170-nm Cu, (b) LBIC map and (c) infrared (IR) images of the device clearly showed the shunt location. 56

4.5 J–V characteristics of devices made with 5-nm Cu, and different metals as current-carrying electrodes. 58

4.6 Comparison of the J-V curves for devices made with different back-contact processes. 61

4.7 J-V curves as a function of Cu thickness for Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe devices. 62

4.8 FF and Barrier height as a function of Cu amounts for Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe devices. 63

4.9 SIMS profile of Cu in CdS/CdTe devices with Cu-doped graphite paste contacts. 64

4.10 (a) Room temperature capacitance-voltage measurement of devices with varying Cu amounts annealed at 280°C, and (b) hole density as a function of the distance from the junction. 66

4.11 Carrier density as a function of the distance from the junction estimated from DLCP measurement (a) no Cu and (b) 20–nm Cu. 67

4.12 Low-temperature (10 K) PL response as a function of Cu amounts 68

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

4.13 Normalized time-resolved photoluminescence (TRPL) decay curves as a function of Cu thickness. 69
4.14 (a) QE curves as a function of Cu thickness (no voltage bias), and (b) Evolution of QE curves with changes in lifetime (simulated). 70
4.15 QE curves as a function of voltage bias for devices with and without Cu. 71
4.16 (a) Curved J-V (b) the effect of lifetime on the current–voltage characteristics (simulated). 71
4.17 JV characteristics as a function of intensity of illumination for: (a) no Cu, and (b) 5-nm Cu devices 72
4.18 (a) Capacitance-voltage measurement, and (b) Carrier density as a function of the distance from the junction, estimated from C-V measurement, for the devices with different metal electrodes. 75
4.19 Capacitance-frequency measurements as a function of temperature for devices with Au, Ni, Ag and Al current-carrying electrodes. 76
4.20 LBIC photocurrent mapping of devices made with Au, Ni, Ag, and Al as a current-carrying electrode. 77
4.21 JV curves under white-and red-light illumination of comparable intensites of devices made (a) without Cu and (b) with 5-nm Cu at the back-contact. 79
4.22 Increase in the crossover of the dark/light curves with increase in defect concentration in CdS. The corresponding carrier densities in the dark and under illumination are also shown in the inset. 80

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

4.23 The CdS/CdTe energy band diagram in the presence of significant defect concentration in the CdS layer. (a) In the dark and at 0 V bias, (b) Under white light illumination and 0 V bias, (c) In the dark and 1.0 V bias, (d) Under white light illumination and 1.0 V bias. 81

4.24 Dark/light crossover before and after exposure to blue-light illumination and storage in the dark for a device made with Cu at the back-contact. . 83

4.25 QE measured as a function of Cu amounts under light bias: a) white light and b) red light. 84

4.26 AQE as a function of the defect concentration N_{AG} in CdS. 86

5.1 Evolution of JV curves with stress time as a function of stress temperature: (a) 60°C, (b) 80°C, (c) 100°C and (d) 120°C. 89

5.2 Changes in parameters with stress time as a function of the stress temperature: (a) J_{sc} (b) V_{oc} (c) FF and (d) efficiency. 90

5.3 The current-voltage curves before and after stress of devices made with and without Cu, with and without $CdCl_2$ treatment. 92

5.4 J-V curve (a) before stress and (b) after stress. 94

5.5 Performance parameters as a function of stress time. 95

5.6 (a) capacitance versus voltage measurements and (b) carrier density as function of depletion width for devices before and after 707 hours of stress. 97

5.7 The statistical distribution of absolute quantum efficiencies measured across devices, a) before and b) after 707 hours of stress, using a 100 μm sampling beam. Peak width correlates with non-uniform behavior. 98

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

List of Tables

2.1 Metal work-function ϕ_m and resulting hole barrier ϕ_b in CdTe 20

3.1 Input parameters used for numerical simulations 50

4.1 PV parameters of SnO_2/CdS/CdTe devices with evaporated–Cu/metal contacts 59

4.2 Heats of telluride formation 60

4.3 PV parameters of Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe devices with evaporated–Cu contacts 63

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Chapter 1

Introduction

1.1 Solar Energy and Solar Cells

Solar cells

A solar cell, or a photovoltaic (PV) cell, is a p–n junction semiconductor device that converts sunlight directly into electric current. An array of electrically connected and encapsulated solar cells make a PV module. Solar cells were first fabricated in the early 1950s, and were extensively studied at that time. In 1954, solar cells with 6% conversion efficiencies were made from crystalline silicon [1]. Early solar cells were primarily treated as laboratory curiosities, until the first significant application as a power supply for space satellites in the late 1950s. Historically, solar cells are used in situations where electrical power from the grid is unavailable, such as remote area power systems, satellites, handheld calculators, and water pumps. At present, the PV market is expanding from such niche applications and consumer products, to the utility market, through building-integrated and other distributed and centralized PV generation systems.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Solar Energy

Solar energy is a renewable, and a pollution–free source of energy that is ubiquitously available in sufficient quantity. At the present, the world uses about 12 TW of power, about 3.3 TW of which is consumed in the USA alone, and most of which comes from conventional sources of energy, which are mostly environmentally unfriendly. By 2050, the world is projected to need about 30 TW of power [2], and conventional fossil fuels may not have the potential to supply this demand. The continuous growth of mass consumption of the limited fossil fuels, and the severe global environmental issues associated with conventional sources of energy are of great concern to the present and future generations. Therefore, the development of alternative sources of energy is vital.

There is a wide variety of renewable energy sources: solar, wind, geo–thermal, biomass and hydro. Among these renewable energy sources, however, only solar energy has a large enough potential to meet the major fraction of the world's energy needs [3]. Of course, the other renewable sources can also generate a significant fraction of a TW of energy. Of the 125,000 TW of global incident solar energy that strikes the earth's surface, about 600 TW of solar-power potential is estimated to be practical. Thus with a 10% efficient solar modules, 60 TW power could be supplied [3], and this amounts to twice the projected world energy need by 2050.

Photovoltaic (PV) technology is one of the most promising ways of meeting the increasing energy demands of the future at a time when conventional sources of energy are being depleted. However, a major barrier impeding the development of large-scale power application of PV system is the high price of commercially available solar cell modules. Hence, the primary objective of worldwide PV research and development is lowering the

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

cost of PV modules to a level that will be competitive with conventional energy sources.

Currently silicon-based solar cells are the dominant commercial photovoltaic products. The PV market, dominated by crystalline silicon, has grown substantially, but, is not yet competitive with conventional sources of energy. It is doubtful that crystalline silicon technology can meet the cost reductions necessary. Therefore, materials that are less expensive than single crystal silicon and that are compatible with large-scale manufacturing are required. Thin-film materials and manufacturing processes are the leading contenders for lowering the cost. Thin-film materials use very thin layers of semiconductor material deposited on a low cost material such as glass, plastic or metal. Currently, thin–film technologies based on amorphous silicon (α–Si), cadmium telluride (CdTe), and copper–indium–gallium–diselenide (CIGS) are the promising technologies for large–scale production. The focus of this work is entirely on CdTe-based thin-film solar cells.

Thin-film CdTe-based solar cell devices are achieving a growing market share, and remarkable progress has been made in recent years in terms of conversion efficiency, long-term stability, and large-scale manufacturing capability. However, the reported efficiencies of the leading thin-film CdTe solar cells are lower than the efficiencies that should be achievable, and thus considerable work will likely be required to optimize the materials as well as the fabrication techniques.

1.2 Thin–film Cadmium Telluride (CdTe) solar cells

CdTe is a group II-IV compound semiconductor material, and is potentially a high–efficiency PV material. CdTe has also other applications: it can be alloyed with Hg to make HgCdTe, an infrared detector material, and it can be alloyed with zinc to make

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

X-ray detectors.

Thin–film polycrystaline CdTe-based solar cells are one of the leading contenders for thin-film solar energy conversion due to an optimal band gap of 1.5 eV that is a nearly ideal match to the solar spectrum, high optical absorbtion coefficient, and low cost fabrication processes. The maximum theoretical efficiency for its band gap and a standard solar spectrum is about 29% [4]. A few-micron thick CdTe film absorbs more than 99% of the radiation with photon energy above the band gap. Hence, the small thickness required for an absorbing layer makes the cost of material for CdTe solar cells relatively low. CdTe can be doped n- or p-type by varying the Cd–Te stoichiometry, and CdTe is the only II-VI compound that can be doped relatively easily p- or n-type [5]. Excess Cd yields n-type and excess Te yields p-type . However, conversion efficiencies of homojunction CdTe solar cells have not been encouraging. Thus, heterojunctions of a wide band-gap n-type semiconductor (commonly CdS) and p-CdTe are widely used. CdS has a wide band gap (2.4 eV), and hence it is transparent to most of the solar spectrum and is often refereed to as the "window" layer. The interdiffusion of hexagonal CdS and cubic CdTe, which can be enhanced by post-deposition heat treatment, is believed to mitigate the 10% lattice mismatch at the CdS/CdTe junction. Thin film n–CdS/p–CdTe research cells have reached 16.5% efficiency [6]. This is a little over half of the 29% theoretical limit, but it has been estimated that practical CdTe devices with 18–19% efficiencies should be feasible in the near future [7, 8]. Complete and stable CdTe modules are being produced at an industrial level (20 MW in 2005), with an efficiency of 7-10% [9].

Fundamental understanding of the CdTe-based solar cell properties is limited. Particularly as a result of the polycrystalline nature, many features of CdTe devices are still not sufficiently understood. Research effort, therefore, is focused on studies of the

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

fundamental electronic properties of the polycrystalline thin film CdTe and other constituents of the cell relevant to improvements in device performance. Properties such as electronic properties of impurities and defects, mechanisms of the dopant compensation, recombination centers, diffusion, electro–migration and transformation of defects, that limit the initial performance or allow device degradation, are active research topics.

The low-cost of fabrication and the wide range of viable fabrication methods make CdTe-based thin film solar cells very attractive. CdTe can be deposited by a wide variety of techniques such as close spaced sublimation (CSS), vapor transport deposition (VTD), physical vapor deposition (PVD), chemical vapor deposition (CVD), electrodeposition, sputtering, molecular beam epitaxy (MBE), or laser ablation. Several research groups in different countries make CdTe devices with reasonable conversion efficiencies using different fabrication approaches, and this diversity of approaches makes the technology very attractive. For example, the Colorado State University Materials Engineering Laboratory has demonstrated, a continuous in-line process with 2-min cycle time that is cost effective and suitable for large volume manufacturing of CdS/CdTe solar cells. This pilot scale system incorporates all device fabrication steps in one chamber operating at modest vacuum, and devices with efficiencies greater than 12% have been realized [10].

CdS/CdTe cells are usually fabricated in a superstrate structure where light is incident through the glass substrate. The basic CdS/CdTe structure consists of four main layers: a transparent conducting oxide (TCO), an n-type semiconductor window layer (CdS), a p-type semiconductor absorber layer (CdTe), and a back contact layer. A generic CdS/CdTe superstrate device structure is shown in figure 1.1. The TCO and back contact carry the current to the terminals of the solar cell.

The standard TCO, SnO_2, has a typically sheet resistance of $10\ \Omega/\square$ and an average

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

optical transmission of 80%. The window layer is a high bandgap material that is transparent to most of the incident light, so that the highest possible fraction of incident light reaches the absorber layer. Devices with 15.8% conversion efficiency are fabricated in the conventional glass/SnO_2/CdS/CdTe structure [11]. Researchers at the National Re-

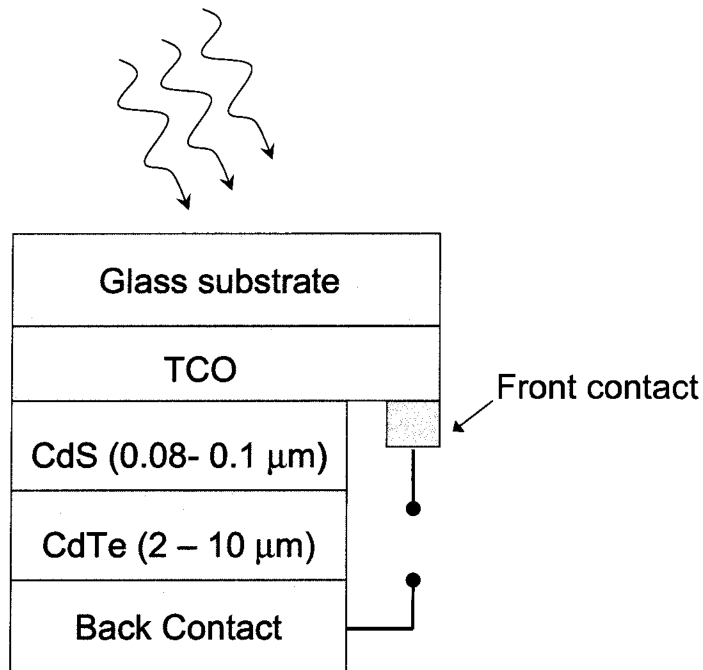

Figure 1.1: A generic CdS/CdTe superstrate device structure (not to scale).

newable Energy Laboratory (NREL) have used a modified device structure to fabricate devices with somewhat higher conversion efficiency (16.5%) [6], which is the record efficiency to date. In the modified structure, SnO_2 is replaced by Cd_2SnO_4 (CTO) that has superior electrical and optical properties, and a buffer layer of high-resistivity Zn_2SnO_4 (ZTO) is sputtered on the CTO layer. By integrating a ZTO buffer layer, the formation of localized TCO/CdTe junctions (partial shunts) can be minimized, particulary when a thin CdS layer is used to optimize the current. Generally, CdTe based solar cells are deposited on a glass substrate. However, in recent years, there has been an increased

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

interest on lightweight flexible substrates.

The CdTe back contact, which needs to be formed by a low-resistance, non–rectifying, and stable contact to p-type CdTe remains, as a challenge. The formation of today's back-contact layer involves a multi-step process, and there are wide variety of materials and techniques for depositing this contact. In the next chapter, the complexity associated with the formation of a back-contact to CdTe will be discussed. The main point of the result of this thesis will identify the impact of the back-contact on the device performance, and stability.

1.3 Fundamentals of Solar Cells

The p–n junction diode

The building block of a photovoltaic device is a p–n junction diode. When n–type semiconductor is brought into contact with p–type semiconductor, a p–n junction diode is formed. The hole concentration gradient on the p–side causes the majority carriers (holes) to diffuse across the junction to the n-side, leaving immobile negatively charged ions behind. Likewise, the electron concentration gradient on the n-side causes majority carriers (electrons) to diffuse into the p–side, leaving immobile positively charged ions. This separation of immobile ions on opposite sides of the junction develops a built-in electric field, and this field applies a force on carriers, refereed to as a drift force, in the opposite direction to the diffusion process. Ultimately, the diffusion and drift current for both carriers balance each other and a thermal equilibrium is attained. In thermal equilibrium, the Fermi-energy level is constant throughout the device, and thus

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

the conduction and valence bands are forced to bend at the junction. Electrons in the conduction band of the n-side see a potential barrier formed by this bending as they traverse to the p-side. This potential barrier is referred to as built-in voltage (V_{bi}). The region with the positively and negatively charged ions is called the space-charge-region (SCR), because it has a net charge, or the depletion region, because in thermal equilibrium it is depleted of mobile carriers.

A p-n junction can be a homojunciton or heterojunction, depending on the materials that form the junction. Homojunctions are formed when p- and n-type layers of the same material are in contact, and heterojunctions are formed when two different conductivity types of different materials and bandgaps are in contact. The energy–band diagrams in the dark and under illumination for homojunction and heterojunction CdTe based solar cells are shown in figures 1.2 and 1.3, respectively.

For a homojunction, the bangaps are equal $E_{g1} = E_{g2}$, hence no band offset where the layers meet, but for a heterojunction $E_{g1} \neq Eg_2$, conduction- and valence-band offsets, $\triangle E_c$ and $\triangle E_v$ respectively, are formed. In the dark the potential barrier at the p-n junction is the built–in voltage (V_{bi}), and under illumination the barrier will be reduced by the photogenerated voltage V_p. Homojunction n-CdTe/p-CdTe solar cells have not yielded acceptable conversion efficiencies. Satisfactory conversion efficiency, however, has often been achieved with a heterojunction n-CdS/p-CdTe devices, even though the existence of the band offsets, and interfacial states due to lattice mismatch at the junction could have a detrimental effect.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

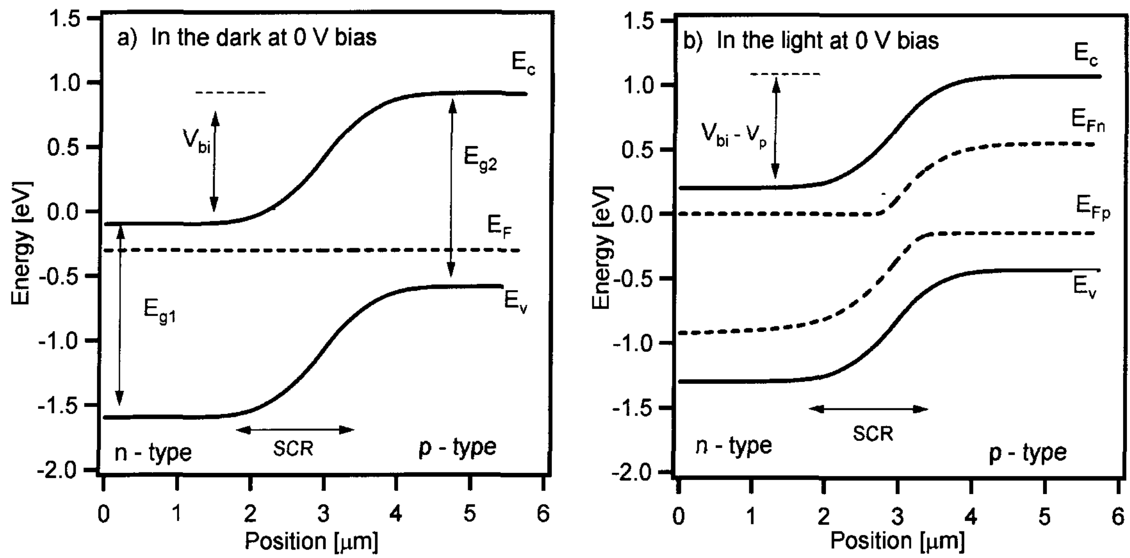

Figure 1.2: Energy band diagram of a n-CdTe/ p-CdTe homojunction. a) In the dark and b) under illumination, where the Fermi level E_F splits into separate levels for electrons and holes.

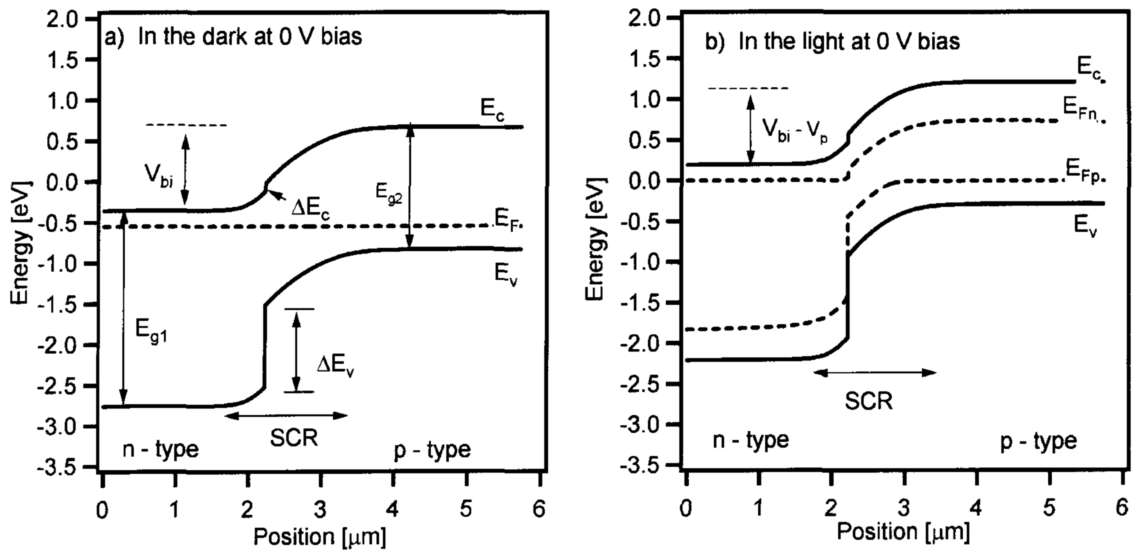

Figure 1.3: Energy band diagram of a n-CdS/ p-CdTe heterojunction. a) In the dark and b) under illumination.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

The operation of a p–n junction diode is governed by the Poisson's, the electron and hole continuity equations.

Poisson's equation:

$$\nabla \cdot \epsilon \nabla \phi = -q(p - n + N_D^+ - N_A^-) \tag{1.1}$$

Continuity equations:

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q} \nabla \cdot \overrightarrow{J_n} \tag{1.2}$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q} \nabla \cdot \overrightarrow{J_p} \tag{1.3}$$

where ϵ is dielectric constant, q is elementary charge, ϕ is the electrostatic potential, p and n are hole and electron carrier concentrations, N_D and N_A are density of ionized donors and acceptors, $\overrightarrow{J_p}$ and $\overrightarrow{J_n}$ are the hole and election current densities, G_p and G_n are hole and electron generation rates, and R_p and R_n are hole and electron recombination rates, respectively.

In general, when a forward bias is applied to the p–n junction, the potential will be reduced and more current will flow across the junction. When the junction is reverse biased, the potential is increased and small current flows through the junction. The current-voltage characteristics of a p–n junction diode is described by

$$J = J_o \left[\exp\left(\frac{qV}{AkT} \right) - 1 \right] \tag{1.4}$$

where J_0 is the saturation current density, A is the diode quality factor, k is Boltzman constant, and T is temperature.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Photovoltaic Parameters of a Solar Cell

A solar cell is a p–n junction diode placed under illumination. In the dark, the current-voltage characteristic of a solar cell is described by equation (1.4). Under illumination, the dark curve will be shifted by the photogenerated current density (J_L).

Typical current–voltage (J–V) curves of a solar cell in the dark and under illumination are shown in figure 1.4. The current-voltage characteristics of a solar cell in the absence of complications is described by

$$J = J_o \left[\exp\left(\frac{qV}{AkT} \right) - 1 \right] - J_L \tag{1.5}$$

In the first and third quadrants of the J–V plot, the product of the current and voltage is positive, and hence power is delivered to the device from the external load. Light–emitting diodes (LEDs) operate in the first quadrant, and photodetectors operate in the third quadrant where the current is independent of voltage but proportional to the optical generation rate. In the fourth quadrant, however, the product of the current and voltage is negative, and hence power is extracted from the device. Solar cells operate in the fourth quadrant, also known as the power quadrant.

The primary parameters that describe the performance of a photovoltaic device are the short-circuit current density, (J_{sc}), open-circuit voltage (V_{oc}), fill–factor (FF) and conversion efficiency (η).

J_{sc} is the current density that flows through the junction under illumination at zero applied bias. In the ideal case it equals the photogenerated current density (J_L) and is proportional to the incident number of photons, or alternatively the intensity of illumination.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

V_{oc} is the voltage across the junction when the current through the junction is zero, and can be expressed as

$$V_{oc} = \frac{AkT}{q} \ln \left(\frac{J_L}{J_0} + 1 \right) \tag{1.6}$$

by rearranging equation 1.5 with J = 0.

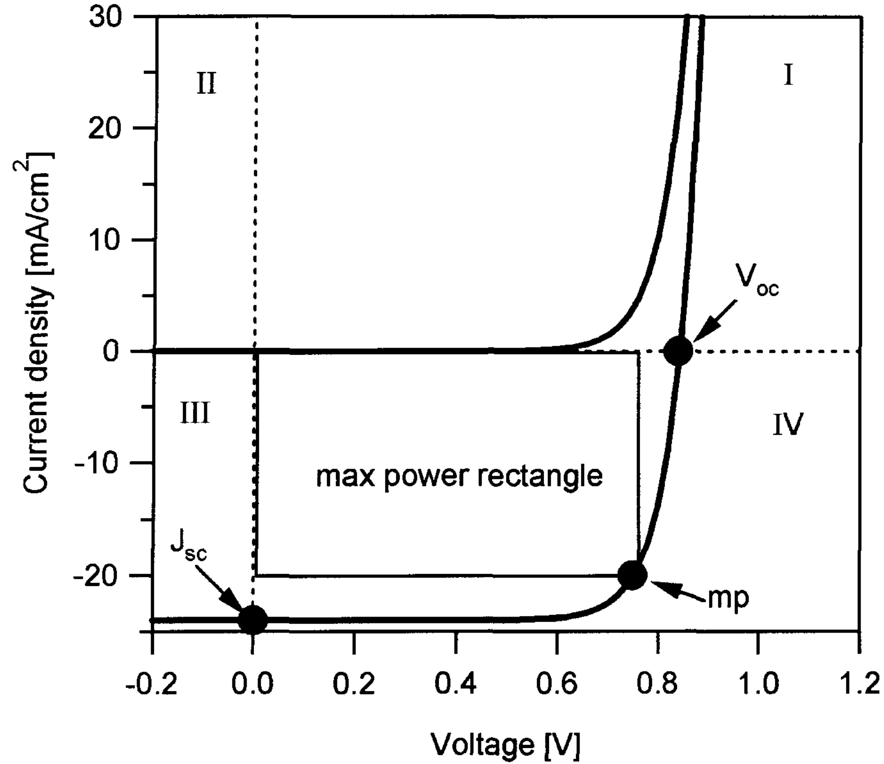

Figure 1.4: Current–voltage characteristics of a generic solar cell with quadrants labeled according to standard convention.

The point on the J–V curve that yields the maximum power is refereed to as the maximum power point (mp), the corresponding current density and voltage are J_{mp} and V_{mp}. The fill–factor (FF) is a measure of the squareness of the J–V curve, and is given by

$$FF = \frac{V_{mp} J_{mp}}{V_{oc} J_{sc}} \tag{1.7}$$

The efficiency of a solar cell is defined as the ratio of the maximum output power

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

P_{max} to the input power (incident power) $P_{incident}$, and can be expressed as

$$\eta = \frac{P_{max}}{P_{incident}} = \frac{V_{oc} J_{sc} FF}{P_{incident}} \tag{1.8}$$

A real solar cell has a parasitic series (R_s) and shunt resistance (R_{sh}). There are several physical mechanisms responsible for these resistances. Series resistance, R_s, is composed of the bulk resistance of the semiconductor materials and that of the front and back contacts. Shunt resistance, R_{sh}, is caused by leakage across the p–n junction and around the edge of the cell. An ideal cell will have high shunt resistance ($R_{sh} = \infty$) and low series resistance ($R_s = 0$). Modest R_s affects mostly the far–forward voltage region above V_{mp} but the open–circuit voltage is not affected by R_s, because no current flows at V_{oc}. The influence of R_{sh} is visible in the low voltage range (near zero voltage). Both, R_s and R_{sh} can reduce the FF by a predictable amount. High values of R_s and low values of R_{sh} can also reduce J_{sc} and V_{oc} respectively.

Under illumination, the J-V characteristics of a generic solar cell with parasitic resistance can be described by

$$J = J_o \left[\exp\left(\frac{q(V - R_s J)}{AkT} \right) - 1 \right] - J_L + (V - R_s J)G \tag{1.9}$$

where $G = 1/R_{sh}$ is the shunt conductance.

The electronic behavior of such a solar cell can be represented by an equivalent circuit model, shown in figure 1.5, based on discrete electrical components. The photo–generation mechanism is represented by the current generator, and the dark current is represented by the diode which is oriented opposite to the current generator. The resistor

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

parallel to the diode represents the shunt resistance R_{sh} and the resistor that is in series with the rest of the circuit represents the series resistance R_s. The effects of R_s and R_{sh} on the J–V characteristics are illustrated graphically in figure 1.6.

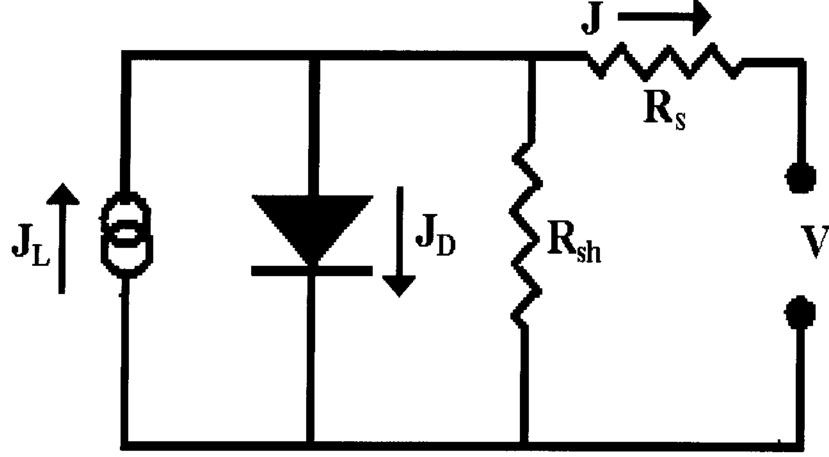

Figure 1.5: Equivalent circuit model of a generic solar cell.

Current–Voltage curve (J–V) analysis

Many of the parameters that describe a solar cell are extracted from the current-voltage curves. The following four steps and the corresponding graphs in figure 1.7 illustrate the techniques.

(a) The parameters J_{sc}, V_{oc}, J_{mp}, and V_{mp} are obtained from the fourth quadrant of the J-V plot, and then FF and efficiency are calculated using equation (1.7) and equation (1.8), respectively. Non–idealities such as light-to-dark crossover and the current limiting behavior in the far-forward bias are examined in the first quadrant.

(b) The shunt resistance R_{sh} is obtained from the plot of the derivative dJ/dV vs. the applied voltage V. Taking the derivative of equation (1.9) yields,

$$\frac{dJ}{dV} = J_0 \frac{d}{dV}\left[\exp\left(\frac{q(V - R_s J)}{AkT}\right) - 1\right] - \frac{dJ_L}{dV} + G \qquad (1.10)$$

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Near J_{sc} and in the reverse bias the first term in the above equation is negligible, and if the photocurrent J_L is voltage independent then equation (1.10) reduces to

$$\frac{dJ}{dV} \simeq G \tag{1.11}$$

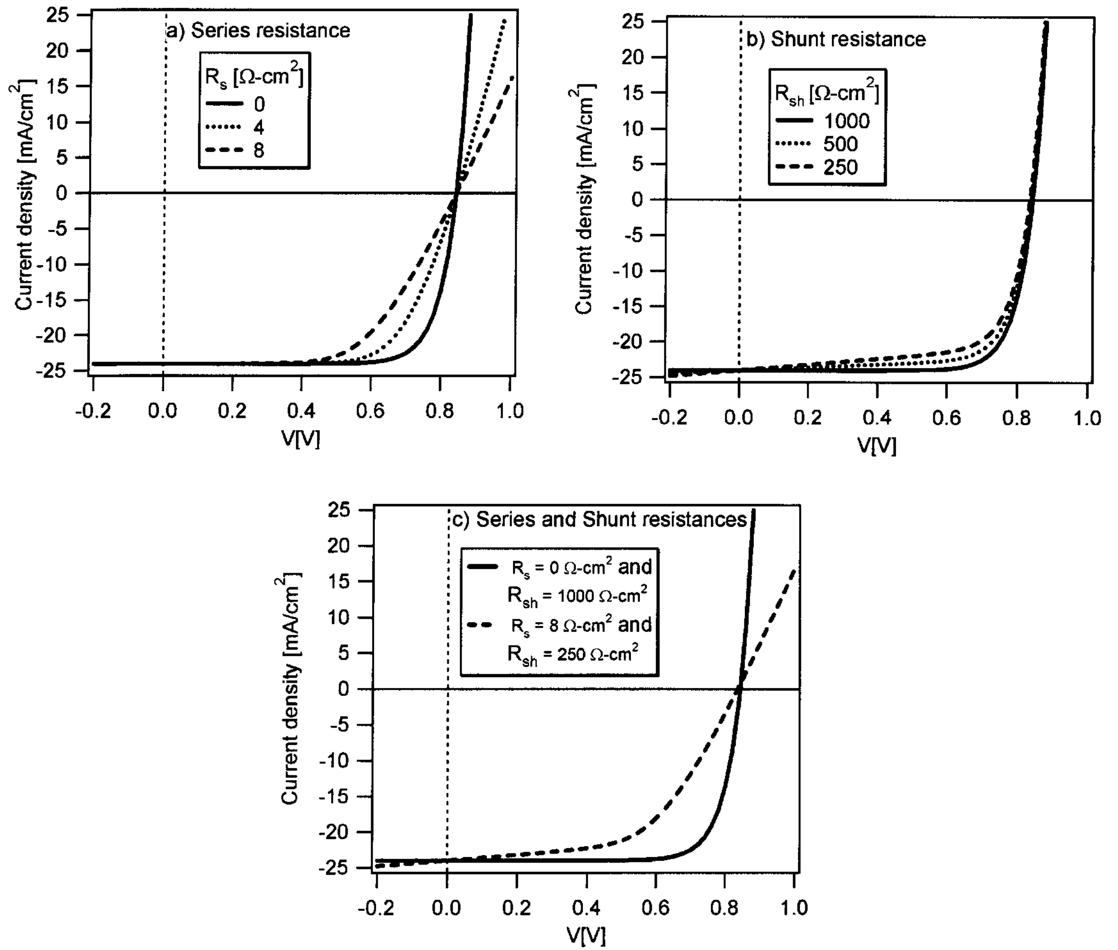

Figure 1.6: Effect of series and shunt resistances on the J–V curves: a) series resistance, b) shunt resistance, and c) series and shunt resistances.

Thus the dJ/dV plot near J_{sc} and in reverse bias will be constant and its value equal to the shunt conductance G [12]. Since the slope of the J–V curve in this range is often very small, measurement noise can have a significant impact on the analysis, so smoothing

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

techniques may need to be applied. Also, the analysis assumes a constant photocurrent, so if the photocurrent is voltage dependent, it becomes difficult to extract a credible shunt conductance value, and this difficulty may affect subsequent analysis.

(c) The series resistance R_s is determined from the plot of dV/dJ. Differentiation of equation (1.9) with respect to the current density gives,

$$\frac{dV}{dJ} = R_s + \frac{AkT}{q}\left(\frac{1 - GdV/dJ}{J + J_L - GV}\right) \tag{1.12}$$

A plot of dV/dJ vs. the factor in parenthesis will be linear for voltage ranges between V_{mp} and V_{oc}. The intercept yields R_s and the diode quality factor may be calculated from the slope, AkT/q [13].

d) A linear fit to the semi-logarithmic plot of the forward current, $J+J_{sc}$ - GV vs. V - JR_s in the voltage range between V_{mp} and V_{oc} gives an intercept J_0 and slope q/AkT from which the diode quality factor can also be calculated. Depending on the dominant current transport mechanism the diode quality factor for a well behaved curve, is expected to be in the range between 1 and 2. A diode quality factor of one is the ideal case, and the high end, A=2, occurs when recombination is the dominant current transport mechanism.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

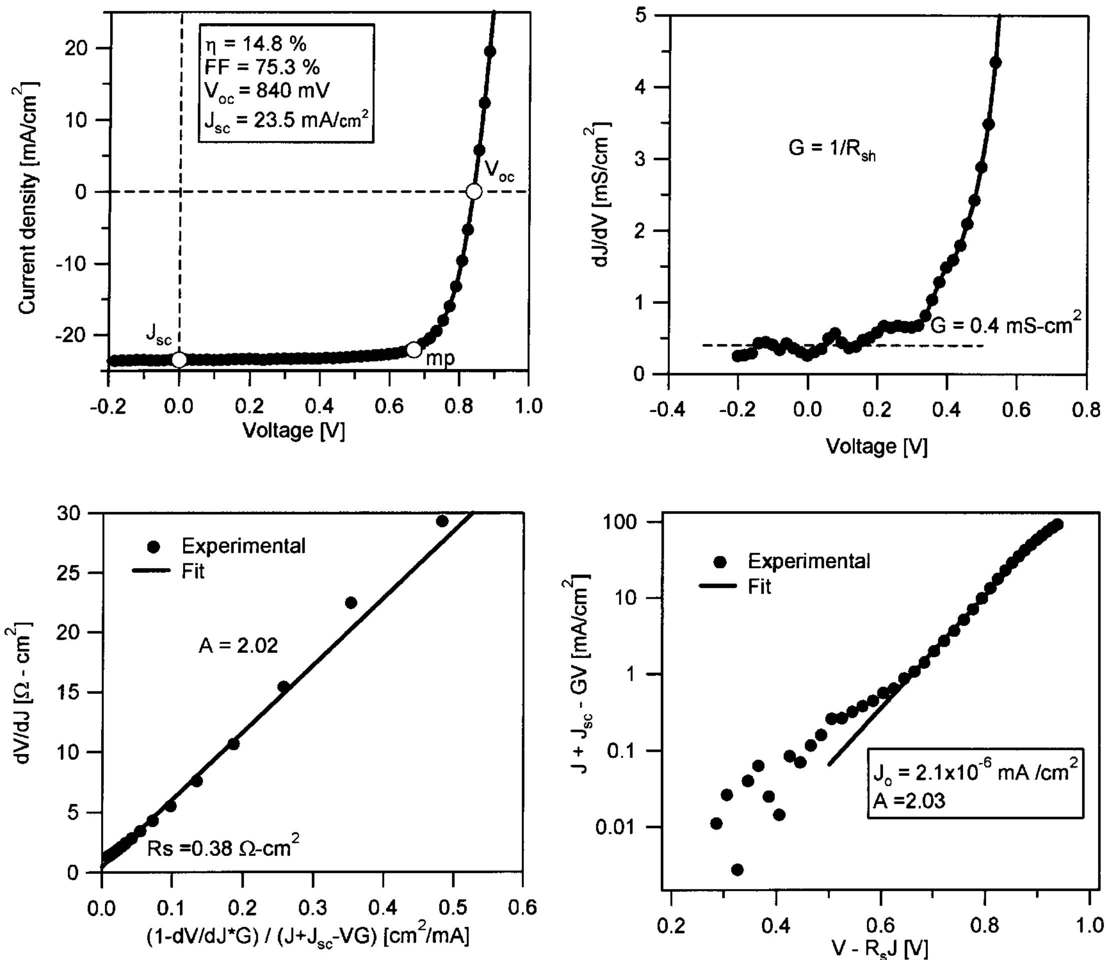

Figure 1.7: Current–voltage analysis.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Chapter 2

Back–Contact Barrier

2.1 CdTe/ Metal contact

A stable back-contact that is not significantly rectifying is essential for good performance and long-term stability of CdS/CdTe solar cells. The formation of a low resistance, low-barrier back-contact is one of the most challenging aspects in the fabrication of high performance CdTe based solar cells.

In general, metal-to-semiconductor contacts can behave either as a rectifying (Schottky) or as an ohmic contact depending on the characteristics of the interface. For a p-type semiconductor with band-gap E_g and electron affinity χ, and a metal with workfunction ϕ_m, an ohmic metal/semiconductor contact is formed when

$$\phi_m > E_g + \chi \tag{2.1}$$

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

and a rectifying contact is formed when

$$\phi_m < E_g + \chi \tag{2.2}$$

Both ohmic and Schottky metal/p-semiconductor interfaces are shown in figure 2.1. At the Schottky-contact interface, majority carriers (holes) see a barrier ϕ_b as they travel from the semiconductor towards the metal, but such a barrier is absent in the case of ohmic contact interface.

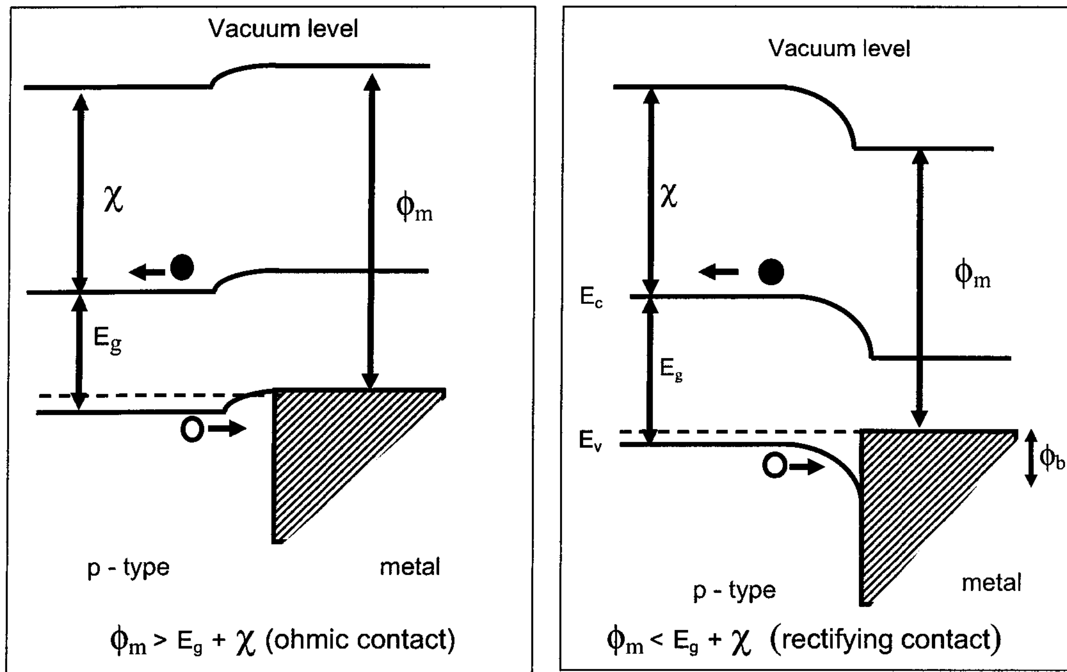

Figure 2.1: Ohmic and rectifying metal/p-semiconductor contacts.

A tunneling contact can in some cases be formed by heavily doping the semiconductor surface. Tunneling contacts, however, require high doping (10^{18} cm^{-3}) and a thin layer (< 3 nm). Since CdTe is heavily compensated, it is difficult to achieve a hole density near 10^{18}cm^{-3}, and hence tunneling mechanism is unlikely to happen. CdTe is a p-type

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

semiconductor with a high electron affinity ($\chi = 4.5$ eV) and high band gap (1.45 eV), and thus a metal with a high work–function ($\phi_m \geq 5.9$ eV) is required to make an ohmic contact to CdTe. Most metals, however, do not have sufficiently high work-functions and therefore form Schottky-barrier contacts to CdTe absorber layers. Table 2.1, tabulates the work–functions of typical metals that can be used to make contacts to p–type CdTe.

Table 2.1: Metal work-function ϕ_m and resulting hole barrier ϕ_b in CdTe

Metal	ϕ_m [eV]	ϕ_b [eV]
Ag	4.26	1.69
Al	4.28	1.67
Au	5.10	0.85
Cu	4.65	1.30
Cr	4.50	1.45
In	4.12	1.83
Mo	4.60	1.35
Ni	5.15	0.80
Pd	5.12	0.83
Pt	5.65	0.30
Sb	4.55	1.40
Te	4.95	1.00
Ti	4.33	1.62
V	4.30	1.65

If any of the metals in Table 2.1 is deposited directly on a p-CdTe surface, then a Schottky contact is formed at the junction, and the contact barrier height, ϕ_b, for holes at the interface (figure 2.1), in the absence of interface states, is given by the difference between the valence band edge and the Fermi energy in the metal.

$$\phi_b = \frac{E_g}{q} + (\chi - \phi_m) \tag{2.3}$$

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

where q is the elementary charge. The barrier heights at the metal/p-CdTe interface calculated using equation (2.3) are also shown in Table 2.1. A zero or negative value would be preferred, though in practice thermal effects make 0.3 eV or less sufficient.

The presence of a back-contact barrier can significantly affect the current-voltage characteristics of a CdTe based solar cells, primarily by impeding hole transport. This current limiting effect is commonly refereed to as "rollover". Figure 2.2, shows a typical J–V curve from a CdTe device with a rollover caused by a 0.52 eV barrier at the back–contact.

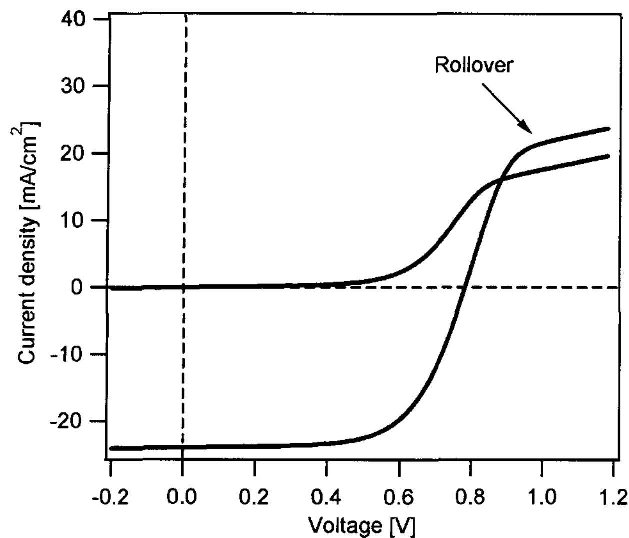

Figure 2.2: J-V curve with rollover.

Metal/p-CdTe contacts has been extensively studied by others. Humphreys et al. reported the formation of Schottky barriers by a range of metals on clean cleaved p-CdTe surface [14]. Similarly Werthen et al., reported Schottky contacts and showed that the barrier height formed on cleaved or heat-treated surface depends on the metal work–function [15]. Other groups have also reported Schottky contacts for Au(Cu)/p-CdTe [16, 17], Al/p-CdTe [18, 19] and In/p-CdTe [20] contacts.

Since no metal has a sufficiently high work–function to make an ohmic contact to p-

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

CdTe, numerous approaches to form low resistance ohmic contacts have been attempted. Most have been directed towards special etching treatments of the CdTe surface prior to metal deposition. The metal/semicondcutor contact depends strongly on the surface condition of the semiconductor, and some surface treatments have achieved improved contacts.

Often the CdTe surface is chemically etched to create a Te-rich surface, and then Cu is incorporated as a key element on the surface followed by anneal to form a Cu_xTe layer that improves the back-contact property. Cu can be incorporated as elemental Cu, followed by a metal or carbon paint to form the electrode [21–23]. Alternatively, Cu_xTe and HgTe doped graphite paste may be used as a Cu source [24] . Other compounds such as HgTe [25], ZnTe:Cu [26] and Sb_2Te_3 [27] have also been used as contacts to p-CdTe. High performance CdS/CdTe solar cells often utilize Cu_xTe and HgTe doped graphite paste, and this is the back-contact process for standard devices at the National Renewable Energy Laboratory (NREL). The use of a Cu-doped graphite paste offers a quick and simple process. It is difficult, however, to reproduce or control this process. Moreover, it may not be scalable to large volume production. Hence, an alternative approach that incorporates evaporated Cu as the primary route to a Cu_xTe contact layer and evaporated metals for a secondary contact is utilized on NREL devices in this study. Though Cu inclusion at the back contact layer insures a non–rectifying contact, its use has been also linked to stability problems in CdTe solar cells. The stability problem is apparently double edged; (1) Over time Cu diffuses away from the back contact leaving behind a Cu-depleted rectifying back contact, and (2) also over time Cu diffuses towards the CdS/CdTe junction and forms Cu-related recombination centers.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

2.2 Two–diode model

In earlier work, Stollwerck and Sites showed that a CdTe cell with a back contact barrier could be modeled by a series connection of two diodes with opposite polarities [28]: the CdS/CdTe main junction diode, and the CdTe/metal-contact back diode. Based on a similar two-diode model, Niemegeers and Burgelman developed a simple analytical theory that explained the observed rollover in thin-film CdTe solar cells [29]. Other groups have also studied the current limiting effect of the back contact on the performance of CdTe solar cells [30, 31]. However, the effects of series resistance and the leakage conductance at the main and back diodes were not included in the simplified model. McCandless et al have used a two-diode model to study the effect of back contact, and the barrier height was determined from the temperature dependence of the series resistance [32]. Recently, we have investigated the details of the CdTe/metal contact using a similar two-diode model (Fig.2.4), and a straightforward technique that extracts the barrier height from room temperature current-voltage characteristics was presented [33].

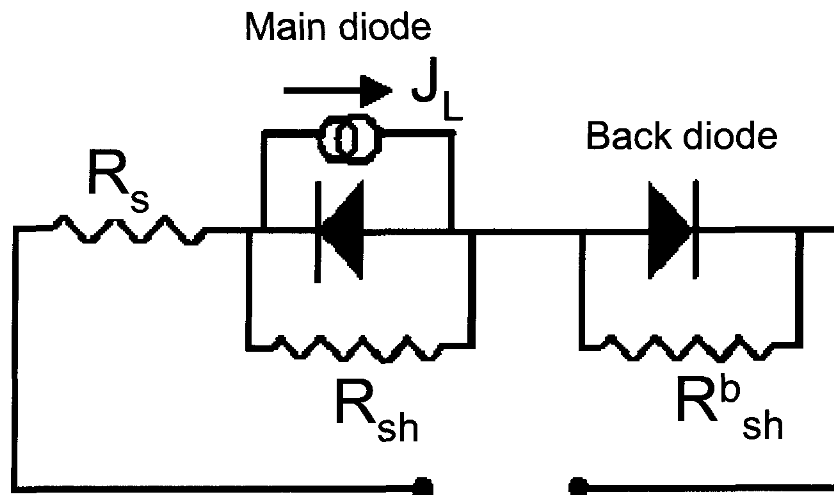

Figure 2.3: A two-diode equivalent circuit model.

To simulate the behavior of a real CdS/CdTe/metal device, the effects of a lumped

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

series resistance and the shunt resistances of the main and the back diodes were included. In the simulation, parameters were systematically changed to yield current-voltage characteristics that match the measured curves. With this approach, the corresponding back barrier height can be extracted. Moreover, the voltage distribution between the two diodes as a function of the applied bias for different conditions can be calculated.

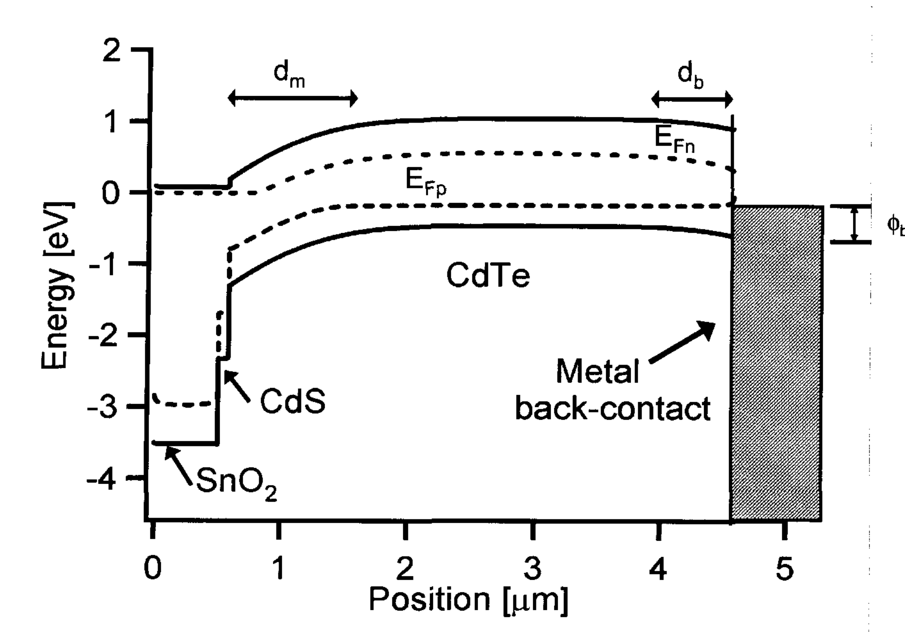

Figure 2.4: Band-diagram of two non-interacting diodes in the light at zero bias (the two depletion regions, d_m and d_b, do not overlap).

2.3 Barrier height determination

For devices with a thick CdTe layer, the main and the back diodes (figure 2.3) can be treated as independent circuit elements with no interaction between the two diodes. This implies that the CdTe thickness is larger than the sum of the depletion regions of the two diodes, and that the electron density in the middle part of the CdTe is low, as shown in figure (2.4). For a reasonably thick CdTe (> 3 μm) with a typical carrier density (2×10^{14}

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

cm^{-3}), the conduction and valence bands are flat over much of the CdTe thickness, and the two diodes can be treated as non-interacting elements. Assuming that thermionic emission current is the dominant transport mechanism at the CdTe/metal interface, and the electron current there is negligibly small, the hole current can be written as

$$J_b = -J_{bo}[\exp(qV_b/kT) - 1] \tag{2.4}$$

It should be noted that the polarity of the CdTe/metal junction is opposite that of the main junction, and hence the negative sign convention for its current. In equation ??EqnJb), q is electronic charge, k is Boltzmann constant, T is temperature, V_b is the voltage across back contact. The saturation current J_{bo} can be expressed as

$$J_{bo} = A^* T^2 \exp(-q\phi_b/kT) \tag{2.5}$$

where T is temperature, ϕ_b is the barrier height, and A^* is the effective Richardson constant given by,

$$A^* = 4\pi q m^* k^2/h^3 = qN_V(k/2\pi m^* T^3)^{1/2} \tag{2.6}$$

Here, h is Planck's constant, N_V is the effective density of states in the valence band, and m^* is effective mass. Equations (2.5) and (2.6) yield

$$J_{bo} = qv_R N_V \exp(-q\phi_b/kT) \tag{2.7}$$

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

The Richardson velocity v_R is thermal velocity given by

$$v_R = \frac{\int_0^\infty v \exp(-m^* v^2/2kT) dv}{\int_{-\infty}^\infty \exp(-m^* v^2/2kT) dv} = \frac{1}{\sqrt{2\pi}} \sqrt{\frac{kT}{m^*}} \tag{2.8}$$

and is proportional to $T^{1/2}$. For CdTe, the effective mass of holes is approximately 0.8 m_0, and hence the Richardson velocity is approximately 3×10^7 cm/s at room temperature.

The hole concentration of a p-type semiconductor is given by

$$p = N_V \exp[-(E_F - E_V)/kT] \tag{2.9}$$

where E_F and E_V are the Fermi and valence band energy respectively. Alternatively, the back contact saturation current J_{bo} given in equation (2.5) can be expressed in terms of the hole carrier density by solving for N_V from equation (2.9) and substituting it into equations (2.7).

$$J_{bo} = q v_R p \exp(-q\phi_d/kT) \tag{2.10}$$

where $\phi_b = \phi_d + (E_F - E_V)$ is the energy difference between the Fermi level and the valence band maximum in the semiconductor at the back interface, whereas ϕ_d is the energy difference between the valence band in the bulk and valence band edge of the semiconductor (figure 2.4). The current–limiting effect, rollover, is attributed to the back contact barrier height (ϕ_b) given by equation (2.3), and occurs because the total current saturates at a current equal to J_{bo}, given by equation (2.7).

When a forward bias V is applied to the two-diode equivalent circuit in figure 2.3, the voltage is divided between V_m across the main junction, V_b across the back contact junction, and JR_s over any resistive components:

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

$$V = V_m + V_b + JR_s \tag{2.11}$$

where J is the current density and R_s is the series resistance.

Under illumination, the voltage drop across the back contact (V_b) is less than zero when the applied voltage (V) is less than the open-circuit voltage (V_{oc}), zero at V = V_{oc}, and greater than zero for V > V_{oc}. Under illumination the current across the main junction can be expressed as,

$$J_m = J_{mo}[\exp(-qV_m/AkT) - 1] - J_L + V_m/R_{sh} \tag{2.12}$$

The current that flows through the back contact is,

$$J_b = -J_{bo}[\exp(-qV_b/kT) - 1] + V_b/R_{sh}^b \tag{2.13}$$

Equating equation (2.12) to equation (2.13), yields,

$$J_{mo}[\exp(-qV_m/AkT) - 1] - J_L + V_m/R_{sh} + J_{bo}[\exp(-qV_b/kT) - 1] - V_b/R_{sh}^b = 0 \tag{2.14}$$

Using the technique described by Sites and Mauk [13] the parameters J_{mo}, A, R_s and R_{sh} of the main diode are extracted from experimental data in the region where J_b is not significant. The value of J_{bo} is the limiting current of the J–V curve at large forward bias in the absence of shunting. Equation (2.14) can be solved analytically to generate the current-voltage characteristics, and the barrier height can be extracted. A very similar result to the analytic solution is also obtained using discrete circuit element modeling

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

with PSpice.

Here, for illustration purposes, the technique described above will be applied to experimental current-voltage (J–V) data of a typical CdTe cell with rollover as shown in figure 2.5. The parameters extracted from the experimental data are J_{mo}= 7×10^{-4} mA/cm^2, J_L= 24 mA/cm^2, A = 2.9, R_s= 1.4 Ω-cm^2, R_{sh}= 1500 Ω-cm^2. For this cell, rollover occurred when its total current saturated at 4 mA/cm^2 and from equation ??EqnJb3) this corresponds to a barrier height of 0.55 eV. Using these parameters and a back diode shunt resistance of R^b_{sh}= 75 Ω cm^2 (or G_b= 13 mS/cm^2), the current–voltage characteristic is simulated analytically.

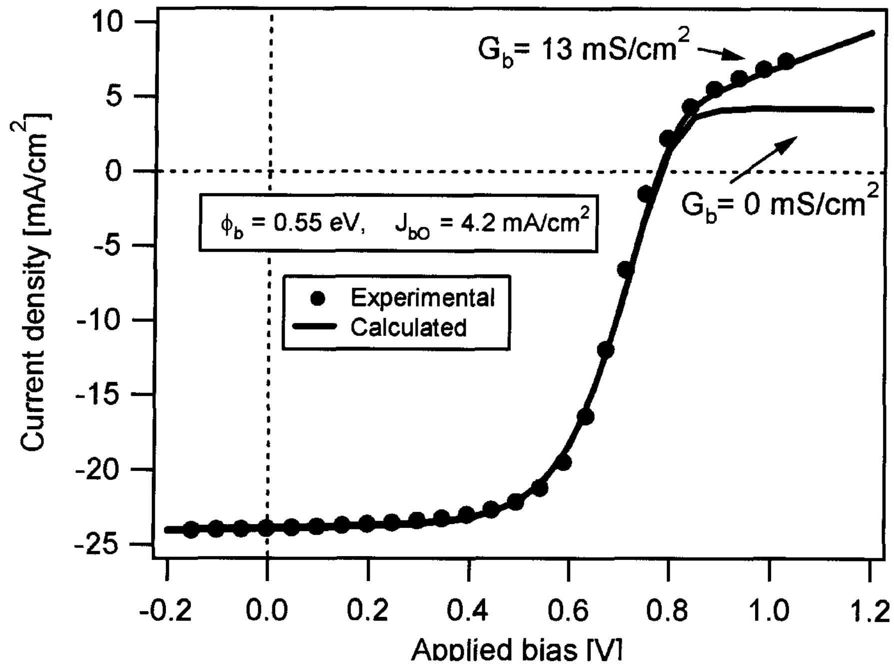

Figure 2.5: Experimental and simulated J-V curve of a CdTe cell with a rollover.

Figure 2.5, shows the simulated curve overlaid on the measured data, and Figure 2.6 shows the voltage drops across the main diode and across the back diode as a function of the applied bias. Under illumination and at low forward applied bias, the back diode is

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

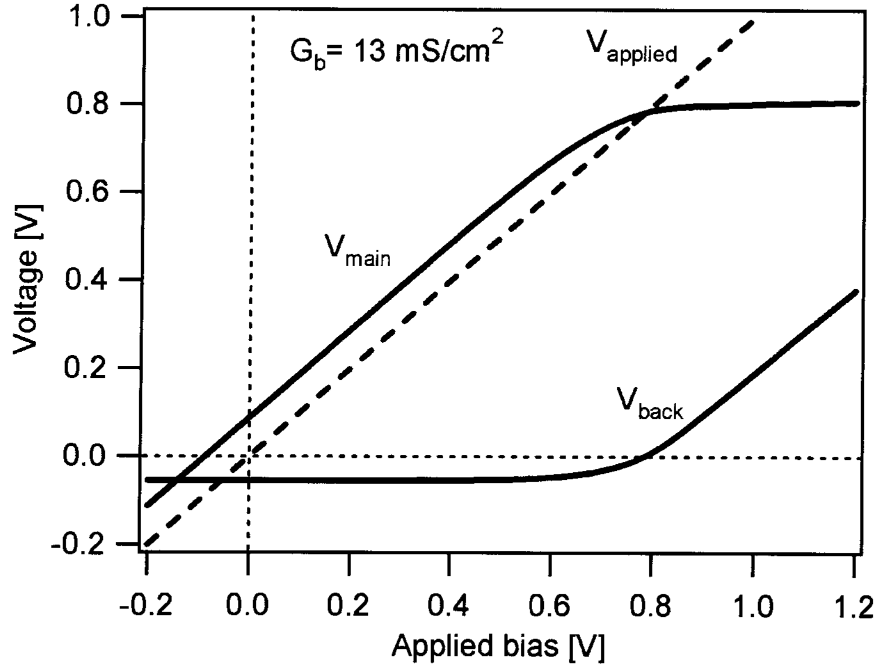

Figure 2.6: The voltage drop across the main and the back diode as a function of the applied bias.

under reverse bias, and the main diode is at slightly higher voltage than the applied bias. At open circuit voltage the current is zero. Zero current through the back diode, which receives no illumination, means there is no voltage across it, and hence the applied bias is entirely across the main diode. As the applied bias is further increased, the primary increase is across the back diode, and the current reaches the saturation value defined by the barrier height. Consequently, rollover occurs. The voltage across the main diode saturates at a voltage, V_s, given by

$$V_s = \frac{AkT}{q} \ln \left[\frac{1}{J_{mo}} \left(J_{bo} + J_L + \frac{V_s}{R_{sh}} \right) \right] \tag{2.15}$$

If J_{bo} is infinitely large ($J_{bo} >> J_L$), then V_s becomes large. This implies no rollover (ϕ_b= 0). If J_{bo} is small (large ϕ_b from equation 2.5) then the voltage saturates at

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

$$V_s = \frac{AkT}{q} \ln \left[\frac{1}{J_{mo}} \left(J_L + \frac{V_s}{R_{sh}} \right) \right] = V_{oc} \tag{2.16}$$

The voltage across the main diode saturates at V_{oc} hence any applied bias increment above V_{oc} will be entirely across the back diode.

The effect of shunt resistance at the back diode, R^b_{sh}, on rollover is also shown. The simulated result, Figure 2.5, showed that R^b_{sh} affects only the rollover part of the J–V curve, and the slope of the rollover curve is the leakage conductance G_b at the back contact ($G_b = 1/ R^b_{sh}$). For room-temperature barrier heights in the range 0.5-0.6 eV, significant rollover appears only in the first quadrant, and hence FF is not affected by the magnitude of the shunt resistance at the back diode. For a very large shunt resistance, $R^b_{sh} = \infty$, the rollover curve is very flat, but its slope will increase with decreasing R^b_{sh}. When the shunt resistance at the back contact equals the lumped series resistance of the device, the slope of the rollover matches the J-V curve slope, and hence rollover disappears despite a significant barrier height. In general, the magnitude of the barrier height determines the point where the current-voltage curve becomes current-limited, and the slope of the rollover curve is determined by the shunt conductance of the back diode. Although a fixed barrier height may result in rollover curves that appear different depending on the value of shunt conductance, such curves will show the onset rollover concurrently.

When the back-barrier height is varied in the calculation, keeping other parameters unchanged, the result is the series of curves shown figure 2.7. As the barrier height is increased, the current saturates at a lower value and hence rollover occurs at lower bias voltage. Note that the rollover changes dramatically over a relatively narrow range of

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

barrier heights. With increasing barrier height, solar-cell performance is affected by a reduction in fill–factor. In general, the open-circuit voltage at room temperature is not significantly affected by a barrier below 0.6 eV.

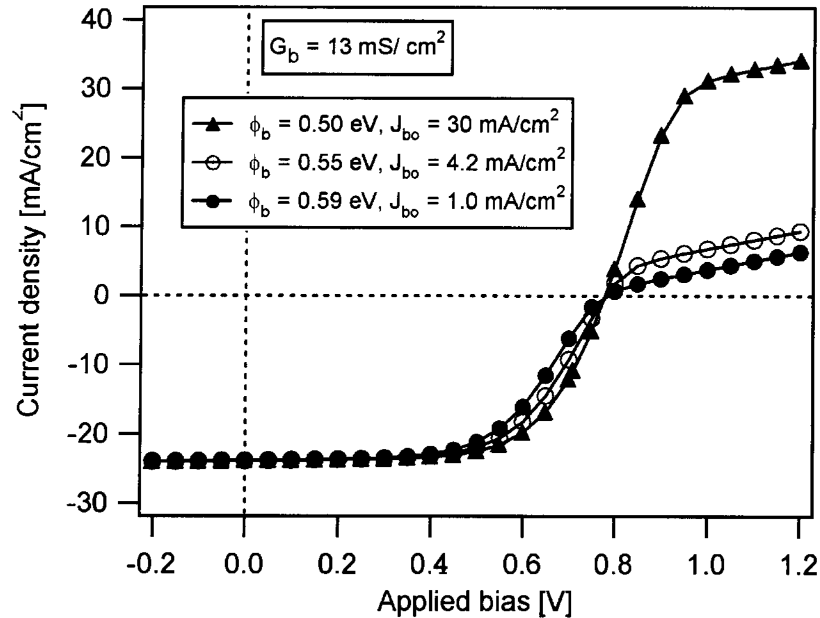

Figure 2.7: Effect of barrier height on CdTe current–voltage characteristics (simulated).

Figure (2.8) shows the effect of barrier height on fill–factor for two temperatures. The fill–factor difference for high and low temperature is smaller at higher barriers. The insert in figure (2.8) shows the saturation current J_{bo} as a function of the barrier height.

The effect of temperature on rollover was further investigated by keeping the barrier height unchanged and varying the temperature from -40 to +40°C. The simulated current-voltage curves are shown in figure (2.9), which shows that the contact barrier in fact has a larger impact as the temperature is lowered. Lower temperature has a similar effect to increased barrier height. As the temperature is lowered, rollover appears at a lower voltage, although the open-circuit voltage shows an increase very similar to that in the absence of the barrier.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

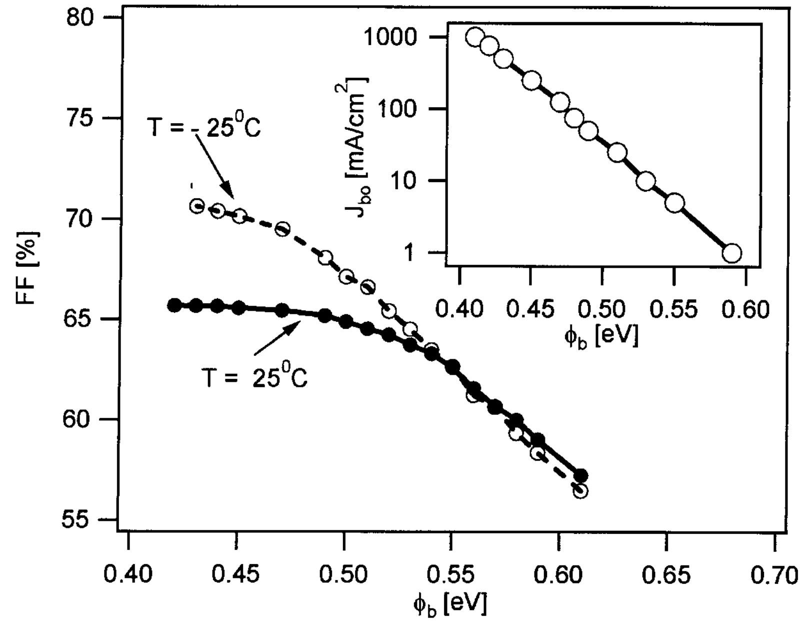

Figure 2.8: Reduction of fill-factor with increase in barrier height. Insert shows the diode saturation current J_{bo} as a function of the barrier height.

Finally, the effect of the series resistance on rollover was studied. Figure 2.10 shows the simulated J-V curves for devices with a fixed barrier height of 0.55 eV but variable series resistance. The simulated result shows that a large increase in series resistance can mask rollover even in the presence of a significant barrier. With zero series resistance, a modest rollover is observed in the first quadrant. As series resistance increases, the ability to discern rollover diminishes. At series resistance values exceeding 10 Ω–cm^2, rollover is no longer apparent.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

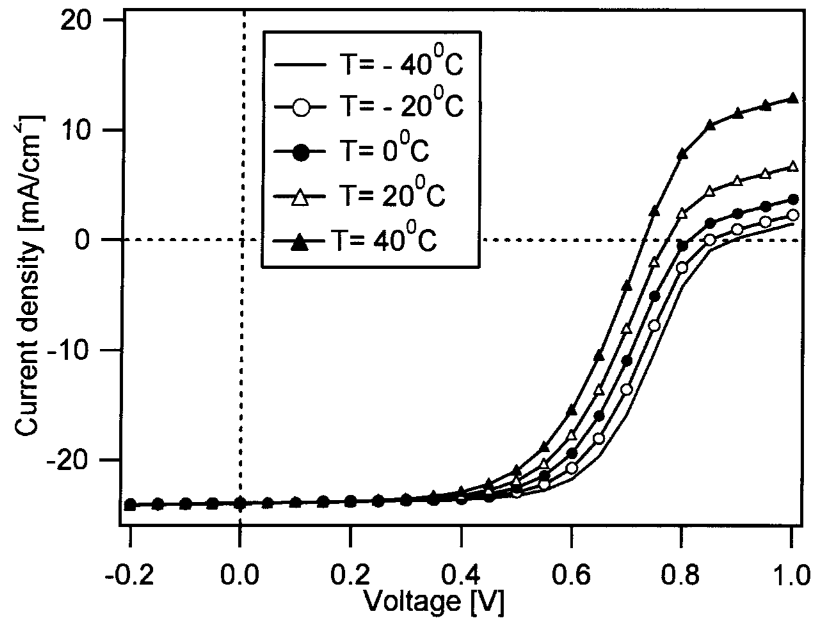

Figure 2.9: JVT-simulated

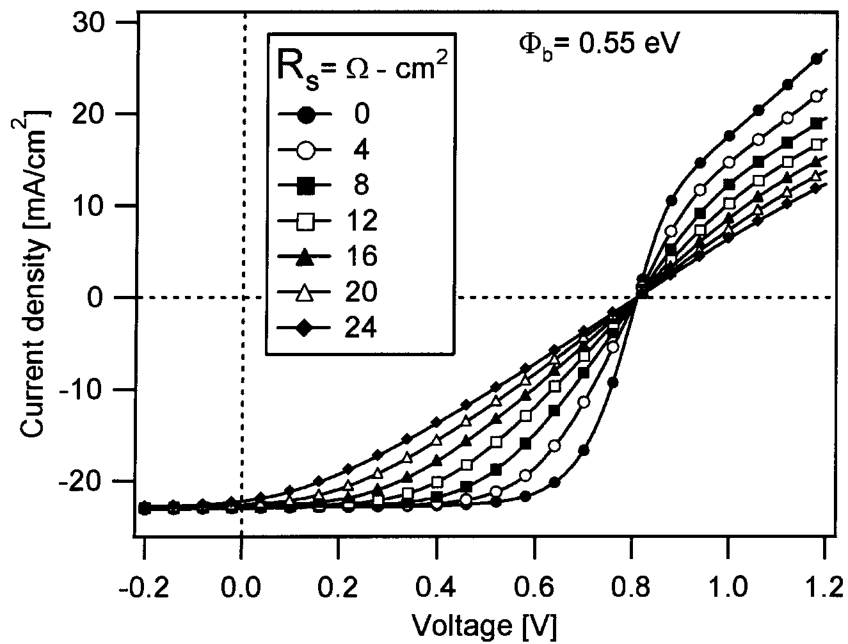

Figure 2.10: The effect of series resistance R_s on rollover

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Chapter 3

Device Fabrication and Data Analysis Techniques

3.1 Device Fabrication

All thin–film CdS/CdTe solar cells studied in this work were fabricated at NREL. Two structures were studied: Structure I is the conventional structure SnO_2/CdS/CdTe, and Structure II is the modified structure Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe, which is the structure used in the record efficiency CdTe cells. Most of the devices studied here had the first structure, but devices with the second structure were also studied to test whether the back–contact behavior is dependent on device structure. The film depositions and the subsequent back–contact process of both structures are described in the following sections.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

3.1.1 Structure I (SnO_2/CdS/CdTe)

a) Film depositions:

A fluorine-doped tin–oxide (SnO_2:F), which is conductive, was deposited by chemical vapor deposition (CVD) on to a Corning 7059 glass substrate, and then a thinner layer of undoped intrinsic $Sn0_2$, was deposited by CVD. The transparent–conductive–oxide (TCO) layer consisted of the bilayer tin oxide (SnO_2:F/SnO_2). The presence of the intrinsic tin oxide (no doping) is believed to be beneficial in maintaining a good junction over the entire area and hence high open–circuit voltage. The CdS layer was deposited onto the tin-oxide-coated glass by chemical-bath deposition (CBD), using cadmium acetate ($Cd(C_2H_3)_2$), ammonium acetate ($NH_4C_2H_3O_2$), ammonia hydroxide (NH_4OH), and thiourea ($CS(NH_2)_2$) in an aqueous solution. The CdTe films were deposited by the close-spaced-sublimation (CSS) technique, with the substrate held at 620°C and the CdTe source at 660°C in an O_2 and He mixture atmosphere for about 4–5 minutes. The thickness of the CdS and CdTe layers were about 80 nm and 10 μm, respectively. The resulting glass/SnO_2/CdS/CdTe structure was then exposed to vapor $CdCl_2$, also mixed with O_2, at approximately 400°C prior to the back contact formation [34]. The $CdCl_2$ treatment plays a vital role in improving the performance of CdTe based solar cells, at least in part by regrowth of crystallites with fewer defects and often a larger size.

b) Back–contact process:

Since direct application of metals on CdTe surface do not result in a good contact, formation of a satisfactory contact consist of multiple steps. After the $CdCl_2$ treatment, all devices were etched in a nitric-phosphoric acid solution that consists 1:88:35 parts of HNO_3:H_3PO_4:H_2O. The nitric-phosphoric (NP) etch removes surface oxides, and it is

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

well known to deplete Cd from the CdTe resulting in a thick, 100-300 nm, conductive Te layer on the CdTe the surface. The standard back–contact processes at NREL consists of brushing $Cu_{1.4}Te$ + HgTe doped graphite layer mixed in an organic-based paste on top of the chemically etched CdTe surface followed by annealing in helium ambient at 280°C for 30 min [34, 35]. The paste is made by mixing 0.24 g $Cu_{1.4}Te$, 5 g HgTe, and 10 g carbon powder (Acheson Electrodag 114). The paste is thinned by methylethylketone (MEK). During the annealing step, Cu is effectively incorporated within the CdTe layer and forms the beneficial Cu_xTe layer. Then, a silver paste is applied to form a current carrying electrode. The paste is cured at 100°C for 1 hr. The silver and graphite pastes are nominally 100-150 μm thick. Since the $Cu_{1.4}Te$ + HgTe doped graphite paste is composed of multiple compounds, carbon and the polymer solvent, it is difficult to reproduce and control. Nevertheless, most high efficiency devices during the past decade have used a Cu–doped graphite layer.

In this study a relatively simple and clean back-contact process has been used to systematically study the effect of Cu on the performance: After the NP etch, Cu metal of varying thickness was deposited by electron-beam evaporation technique at room temperature with a deposition rate of 0.01-0.05 nm/s. In one set of devices, varying amounts of Cu (0-170 nm) were evaporated on the NP-etched surface, and then the contact was annealed in a helium ambient at 280°C for 30 minutes to promote Cu diffusion and facilitate the formation of Cu_xTe. These devices were completed by evaporating 60–nm Pd and 300–nm Al layers to form a current carrying electrode. In another set of devices, 5 nm of Cu was evaporated on the NP etched surface, the contact was annealed in helium at 200°C or 240°C for 30 min., and then 300–500 nm of different metals: Ag, Al, Au, Cr, Ni, Pd, or Pt were evaporated to form an electrode. Schematics of the SnO_2/CdS/CdTe

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

structure with either a Cu-doped graphite paste or an evaporated Cu back–contact are shown in Figure 3.1. The above variations in the back-contact process are aimed at the device implications of the amount of Cu used, the annealing temperature, and the metal used as a current carrying electrode.

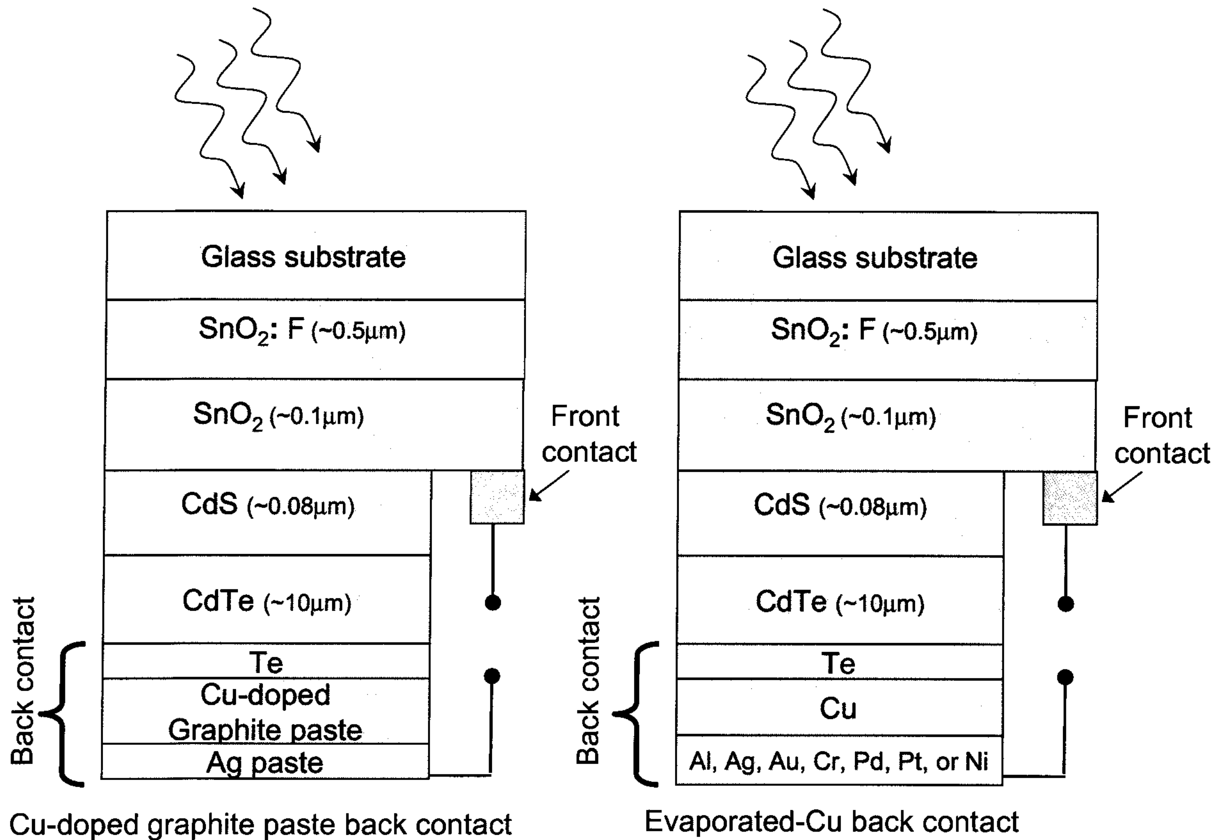

Figure 3.1: The SnO_2/CdS/CdTe structure: a) Cu-doped graphite contact, and b) evaporated-Cu contact.

3.1.2 Structure II (Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe)

a) Film depositions:

CTO (Cd_2SnO_4) and ZTO (Zn_2SnO_4) films were both deposited on a glass substrate by rf magnetron sputtering at room temperature in pure oxygen using hot-pressed oxide

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

targets. The CTO layer was heat treated in CdS/Ar atmosphere at 580-660°C for 10–20 minutes, prior to the deposition of ZTO layer. The thicknesses of both the CTO and ZTO films were in the range 100–300 nm. Next, an oxygenated nano–crystalline CdS film (nano-CdS:O) was deposited by rf-magnetron sputtering at room temperature using an oxygen/argon gas mixture. The CdTe films were deposited by the close-space-sublimation (CSS) technique at 570-625°C for 3-5 minutes in an O_2/He atmosphere. After CdTe deposition, samples received a vapor $CdCl_2$ treatment at 400-430°C for 15 minutes [6]. The temperature and duration of $CdCl_2$ treatment were optimized, since over-treatment may introduce stress at the TCO/CdS interface due to grain growth of CdS film, which can lead to blistering or peeling of the film. In the modified structure (structure II), the interdiffusion of CdS and ZTO layers appears to relieve the stress, thereby improving adhesion. This stress relief provides greater latitude in optimizing the $CdCl_2$ treatment, hence the overall device performance.

b) Back–contact process

The Cd_2SnO_4/Zn_2SO_4/CdS:O/CdTe devices were also NP etched after $CdCl_2$ treatment. Cu metal of varying thickness, 0–130 nm, was evaporated, the un-doped graphite layer (buffer) was applied, and the contact was then annealed in helium ambient at 250°C for 30 min to promote Cu diffusion. Devices were completed by applying a Ag paste as a secondary contact. The Ag paste was cured at 100°C for about one hour. The schematic of the structure Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe with a back–contact layer that consists of evaporated Cu, un-doped graphite buffer, and Ag-paste electrode is shown in Figure 3.2.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

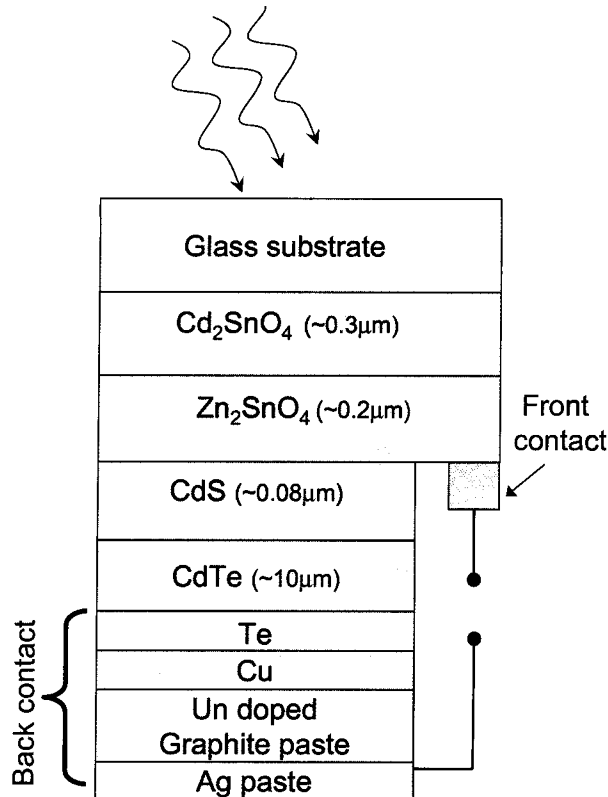

Figure 3.2: The Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe device structure.

3.2 Data analysis techniques

3.2.1 Current – Voltage measurement

Current–voltage (J–V) measurements were done at both CSU and NREL. The measurement setup and the procedures at both laboratories are similar, and here the description of the setup at CSU is presented. A Keithley, programable voltage source, is used to apply a predetermined voltage range and voltage increment. The actual voltage across the cell and the current flowing through the cell are measured with a Hewlett Packard multimeter, model 34401A. Measurement temperature is controlled by flowing cold nitrogen gas through a polymer box that encompasses the device and the mounting stage, and solar cell temperature is read from a thermocouple attached to the device. The

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

standard J–V measurement is done at 25±0.5°C. However, current-voltage measurement at different temperatures (J–V–T) could also be performed to investigate the effect of the back–barrier height, and to study the change in open-circuit voltage with temperature, which gives insight to the current transport mechanism. In a well-behaved solar cell, the extrapolation of V_{oc} to 0 K temperature gives an estimation of the absorber bandgap.

J–V measurement at different intensities and selected spectrum ranges were also done for detailed analysis by using neutral density (ND) filters and colored glass slides, respectively. The light source used for J–V measurements is a two-inch beam solar simulator (Model XPS 400). The output spectrum of the simulator is reasonably well matched to the standard global one-sun (100 mW/cm^2) solar spectrum as shown in figure 3.3.

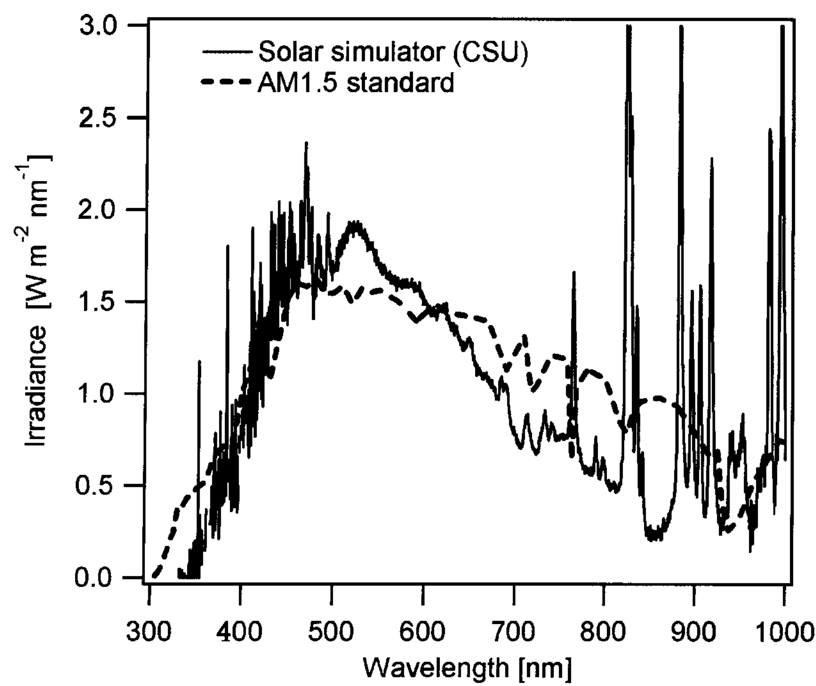

Figure 3.3: The global AM1.5 outdoors solar spectrum, and the spectrum of the solar simulator at CSU.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

3.2.2 Quantum efficiency

The quantum efficiency (QE) of a solar cell at a certain wavelength, λ, is defined as the ratio of the photogenerated current, $J_L(\lambda)$, to the incident photon flux, $\phi(\lambda)$.

$$QE(\lambda) = \frac{J_L(\lambda)}{q\Phi(\lambda)} \tag{3.1}$$

A standard quantum efficiency (QE) measurement is performed using a chopped monochromatic probe beam, with the sample is exposed to one sun white light illumination during the measurement. A halogen light bulb is used as a source of light. The chopped monochromatic beam is achieved by using a monochromator and a rotating wheel, or chopper. The output current is amplified and phase-sensitively detected by lock-in amplifier. The QE measurement uses a lock-in technique to detect the resulting ac current from the chopped probe beam, and any dc current response from light bias is rejected.

For more detailed analysis, QE measurements are also done under illumination with limited spectral content. In this study, QE measurements are done in the dark, as well as under white–light, blue–light and red–light illuminations. In addition to the light bias, electrical bias was also applied during QE measurements, to examine the effect of the change in the depletion width on the current collection. The QE measurements under voltage and light bias were performed at NREL.

QE measurements are valuable to characterize the photocurrent, and can also be used to determine the individual losses responsible for reducing the measured J_{sc} from its ideal value. In general, the short-circuit current J_{sc} equals the photocurrent J_L and can be calculated by integrating the QE spectrum multiplied by the photon current J_{solar} being

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

used, generally that of the standard AM1.5 spectrum.

$$J_{sc} = \int_{\lambda} QE(\lambda) * J_{solar}(\lambda) d\lambda \tag{3.2}$$

Using equation (3.2), an ideal CdTe cell with band gap 1.45 eV and QE of 100% will yield a photocurrent of 30.5 mA/cm^2. In practice the photocurrent will be less, often significantly less. Current losses can be optical, due to front reflection and absorption in the window, TCO and glass layers, or electronic losses due to recombination losses in the absorber. In figure 3.4, QE of a typical production CdS/CdTe solar cell and the current losses in each layer are shown.

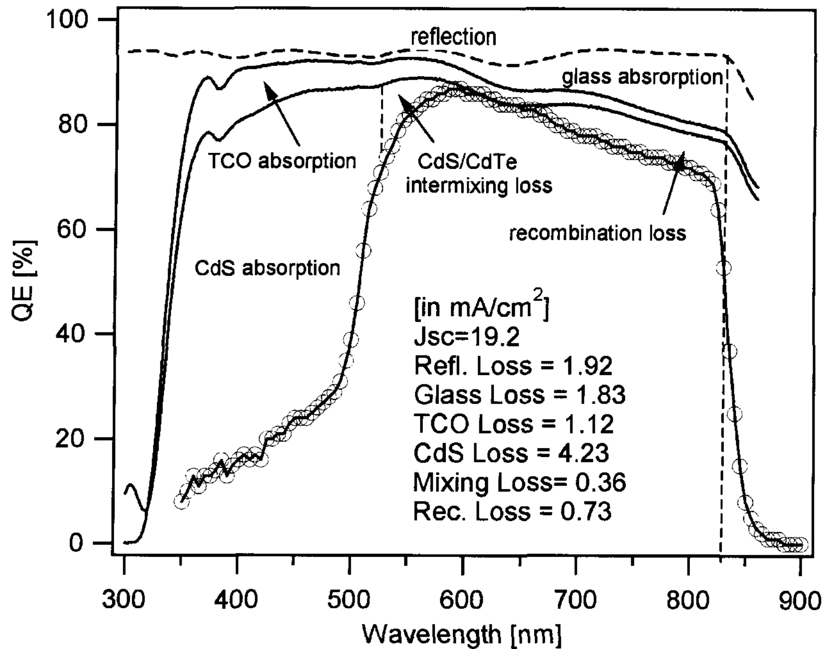

Figure 3.4: QE and current losses of a typical production cell.

Each individual current loss can be calculated using

$$J_{loss} = \int_{\lambda} F(\lambda) * J_{solar}(\lambda) d\lambda \tag{3.3}$$

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

F(λ) is the fractional reflection or absorption at each wavelength. The sum of the losses plus QE must equal unity at each wavelength.

3.2.3 Room-temperature Capacitance–Voltage measurement

The capacitance-voltage (C–V) technique is a useful tool to obtain information about the doping concentration profile of the lightly doped side of a p–n junction diode. In the case of n-CdS/p-CdTe solar cells, the free carrier electron concentration in illuminated n-CdS is at least two orders of magnitude higher than the free hole concentration in p-CdTe, and thus C–V technique primarily probes the carrier density of the CdTe layer. The capacitance measurement relies on the fact that the width (W) of the space-charge -region (SCR) of a semiconductor device junction changes with applied voltage. The CdS layer is very thin and generally fully depleted, and thus the change in the depletion due to applied voltage appears on the CdTe side.

The room-temperature capacitance–voltage measurements were performed at CSU using an impedance analyzer (HP 4192A LF). A modulation voltage of 20 mV was applied, and the dc bias was typically varied from 0.2 V to -2.0 V and the frequency from 1 kHz–1 MHz in a predetermined sequence. As a standard procedure, prior to a C-V measurement, capacitance vs frequency measurement (C–F) at different biases is done to choose a frequency at which the change in the capacitance with frequency is not significant. Such frequency is used for the subsequent C–V measurement. Routinely, prior to the actual C–V measurement, devices are prebiased at -2 V reverse bias for about 8 minutes to minimize any transient effect. The phase angle between the capacitive and conductive terms of the impedance signal should be kept above 20^0 for a credible C–V

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

measurement [36]. For all the C–V measurements performed in this study, however, the phase angles were well above 70^0.

The depletion region of the p–n junction solar cell can be approximated as a parallel plate capacitor, and the capacitance is given by

$$C = \epsilon \frac{A}{W} \tag{3.4}$$

where ϵ is the permittivity, A is the area, and W is the depletion width.

For a step junction the depletion width W given by

$$W = \left[\frac{2\epsilon}{q} (V_{bi} - V) \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \right]^{\frac{1}{2}} \tag{3.5}$$

where q is the fundamental charge, V_{bi} is the built-in voltage, N_A is the acceptor concentration in the n-layer, and N_D is the donor concentration in the p-layer. From the above two equations, the capacitance per unit area A, can be expressed as

$$\frac{A^2}{C^2} = \frac{2}{q\epsilon} (V_{bi} - V) \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \tag{3.6}$$

For a n^+–p junction, $N_D >> N_A$ thus

$$\frac{A^2}{C^2} = \frac{2}{q\epsilon N_A} (V_{bi} - V) \tag{3.7}$$

As the dc bias is changed, the charge density at the edge of the depletion width is changed, and in the absence of compensation N_A will correspond to the density of free carriers p. From the slope of A^2/C^2 as a function of the applied voltage, the hole density

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

p can be estimated. Figure 3.5(a) shows a typical plot of A^2/C^2 vs. V, and figure 3.5(b) shows the carrier density as a function of position deduced from the data. Although room-temperature C–V measurements are generally done at a frequency that minimizes any contribution from deep-gap traps, a room–temperature C–V measurement by itself may not adequately account for such traps. Hence, the drive-level capacitance-profiling (DLCP) technique described in the next section was also used for detailed analysis.

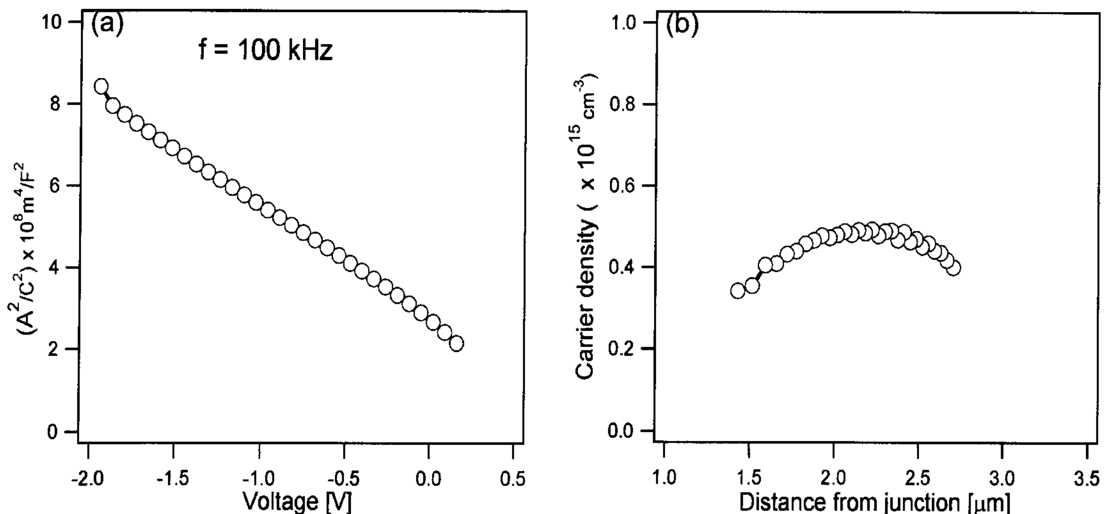

Figure 3.5: (a) capacitance as a function of the applied bias, and (b) carrier density deduced from the C–V data as a function of the distance from the junction.

3.2.4 Drive-level capacitance profiling (DLCP)

DLCP measurements provide a more accurate assessment of the free carrier density. In DLCP measurement, a dc bias is applied to the device, while the amplitude of the ac probe signal (drive level) is varied. In a standard CV measurement, a very small ac voltage is applied and the response is assumed to be linear with ac voltage. In DLCP, larger ac biases are used, and additional nonlinear terms becomes significant.

$$C = C_0 + C_1\delta V + C_2(\delta V)^2 + ..., \tag{3.8}$$

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

where C_0 is the capacitance in the limit of zero amplitude drive level, and C_1 and C_2 are the first and the second order corrections to the junction capacitance for finite drive levels. C_0 and C_1 can be extracted from the slope and intercept of a liner fit of C vs δV plot. The drive level defect density, N_{DL}, for p-type material is given by [37]

$$N_{DL} = -\frac{C_0^3}{2q\epsilon A^2 C_1} = p + \int_{E_F}^{E_v+E_e} g(E)dE, \tag{3.9}$$

where E_e is the activation of energy for thermal emission from a deep defect, E_F is the Fermi energy, E_v is the valence band energy, g(E) is the density of trap states, and p is the free carrier density.

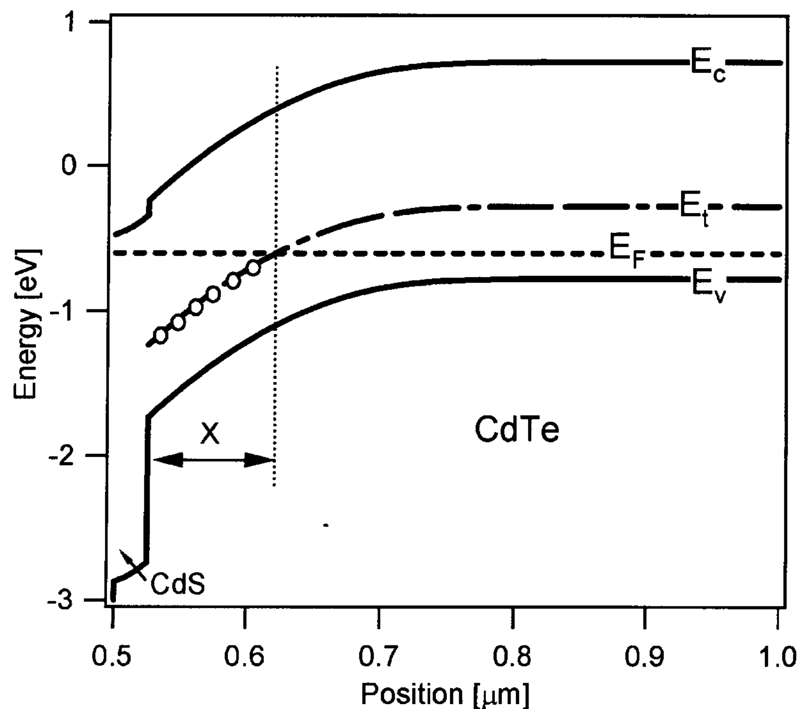

Figure 3.6: Trap energy level E_t with respect to the fermi energy level E_F. E_t crosses E_F at a distance X from the junction, and traps with energy above E_F are ionized.

Spatial and energy profiles of defect states are obtained by varying the dc bias, and E_e is determined by changing temperature or frequency, since the frequency and temper-

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

ature of the depth profile determines which gap states contributes to the capacitance. At relatively low temperature or high frequency, the response from deep trap states is minimal, and hence N_{DL} is very nearly the free-carrier density p. As temperature is increased or frequency is lowered, the value of N_{DL} increases because of the ionization of deep trap states. The difference between N_{DL} at high and low temperatures yields the density of the trap states. The drive level density is measured at a point, X, where the trap level E_t crosses the Fermi level (figure 3.6). In response to a periodic small change in bias, trap levels close to the Fermi level can cross the Fermi level (figure 3.6) and change their state. Near X the trap states can be filled or emptied by the applied oscillating (drive level) signal. It is difficult to accurately determine the position of X, and hence, N_{DL} is commonly plotted as a function of the depletion width (Figure 3.7).

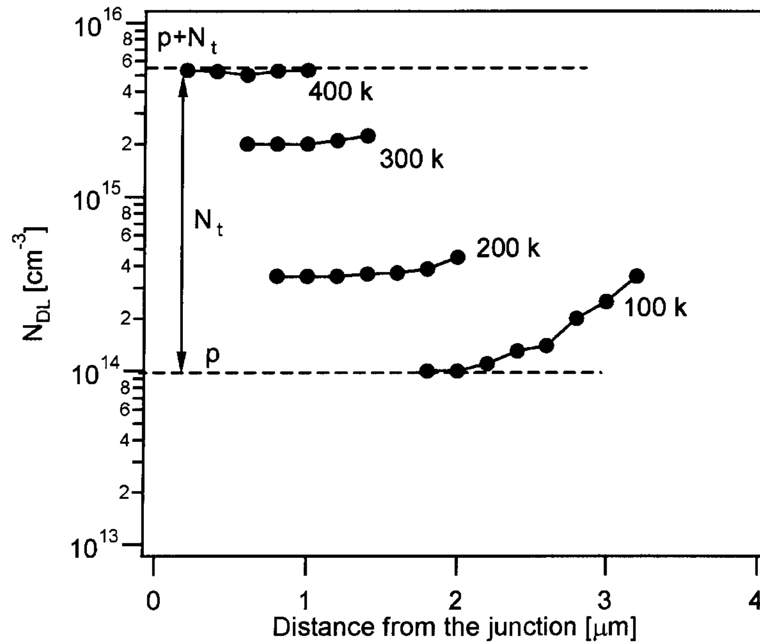

Figure 3.7: Drive level carrier density as a function of distance from the junction.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

3.2.5 Time–resolved photoluminescence (TRPL)

Room–temperature photoluminescence (PL) decay curves were measured through the glass side of CdTe structures using time–correlated single–photon counting. Photoexcitation at 633 nm was provided by an optical parametric amplifier pumped by the output of a titanium:sapphire laser system with a regenerative amplifier [38]. The final laser output consisted of a 250-kHz pulse train with an average power of 250 μW, a beam diameter of about 0.5 mm, and a pulse width of several hundred femtoseconds. This corresponds to peak photoexcited carrier density of about 10^{16}-10^{17} cm^{-3}. Lifetimes were determined by nonlinear least-squares iterative reconvolution of the system response with a model single exponential fit.

$$I_{PL}(t) = I_{PL}(0)\exp\left(-\frac{t}{\tau}\right) \tag{3.10}$$

where I_{PL} is the PL signal, t is decay time, and τ is the TRPL lifetime.

The penetration depth for 633 nm light in CdTe is 220 nm, so the technique primarily probes the CdTe near the junction. At these injection levels, charge separation by the junction is considerably reduced and PL decay is dominated by recombination. Varying the injection level by three orders of magnitude did not significantly affect the decay rates. For CdTe, the low radiative efficiency, short lifetimes, and small injection dependence indicate that the dominant recombination mechanisms are nonradiative, associated with Shockley-Read-Hall and interface recombination. Polycrystalline CdTe based solar cells contain a fairly high concentration of traps near the junction, thus it is difficult to separate the effects of capture and emission of carriers in traps from recombination processes. Hence, TRPL lifetime may not equal the minority-carrier lifetime, but should reliably

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

track it.

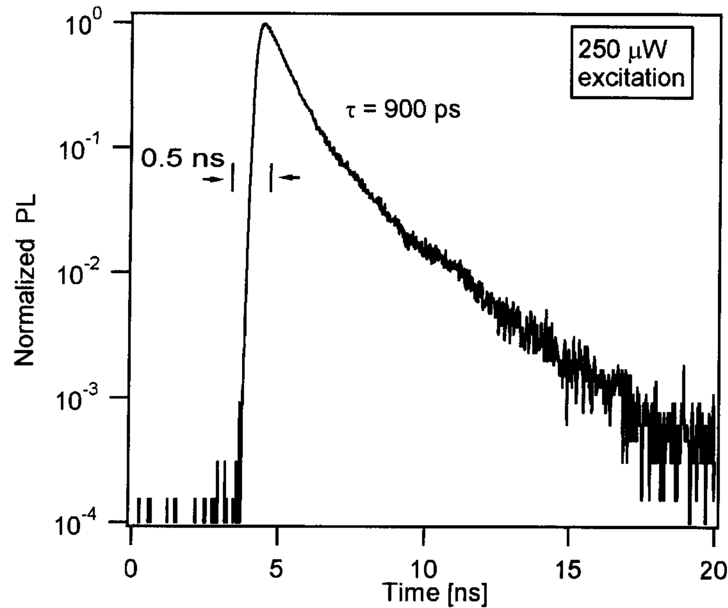

Figure 3.8: A typical normalized time-resolved photoluminesence (TRPL) decay curve of a CdS/CdTe device.

3.2.6 Numerical Simulation

Analytical solutions provide an intuitive understanding of solar cell performance, however, they are limited in their accuracy due to the simplifying assumptions that often must be made. For a more thorough investigation of the transport properties of solar cells the semiconductor equations that govern solar cells can be solved numerically. In general, the physics of solar cells devices is governed by the three equations: Poisson's equation (equation 1.1), the continuity equation of free electrons (equation 1.2), and the continuity equation of free holes (equation 1.3).

Numerical simulations of CdS/CdTe solar cells were performed using the one-dimensional simulation software "AMPS-1D" developed at Pennsylvania State University by S. Fonash

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

et al. with support from the Electric Power Research Institute. In AMPS (Analysis of Microelectronic and Photonic Structures), the three coupled differential equations, along with appropriate boundary conditions are solved numerically. Finite-element and Newton-Raphson methods are incorporated. Such numerical simulation allows analysis of solar cell designs and operating conditions for which simple analytic expressions are inadequate. The input parameters used for the numerical simulations, Table 3.1, are similar to the baseline parameters recently suggested by Gloeckler et al. [39]. In this work, numerical simulations are used to reproduce and explain experimental results.

Table 3.1: Input parameters used for numerical simulations

A. General device properties		Front	Back
ϕ_b(eV)		ϕ_{bn}= 0.1	ϕ_{bp}= 0.4
S_e (cm/s)		10^7	10^7
S_h (cm/s)		10^7	10^7
Reflectivity R_f		0.1	0.5
B. Layer properties	**SnO_2**	**CdS**	**CdTe**
W(nm)	500	80	9000
ϵ/ϵ_0	9	10	9.4
μ_e(cm^2/Vs)	100	100	320
μ_h(cm^2/Vs)	25	25	40
$N_{D(A)}$(cm^{-3})	N_D:10^{17}	N_D:1.1x10^{18}	N_A:2x10^{14}
E_g(eV)	3.6	2.4	1.4
N_C(cm^{-3})	2.2x10^{18}	2.2x10^{18}	7.8x10^{17}
N_V(cm^{-3})	1.8x10^{19}	1.8x10^{19}	1.8x10^{19}
χ(eV)	4.5	4.5(ΔE_C = 0)	4.4(ΔE_C = -0.1)
C. Gaussian defect states	**SnO_2**	**CdS**	**CdTe**
N_{DG},N_{AG}(cm^{-3}	D:10^{15}	A:10^{18}	D:2x10^{12}
E_A,E_D(eV)	1.8	1.2	0.75
W_G(eV)	0.1	0.1	0.1
σ_e(cm^2)	10^{-12}	10^{-17}	2.5x10^{-11}
σ_h(cm^2)	10^{-15}	10^{-12}	10^{-13}

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Chapter 4

Role of Cu on performance of CdS/CdTe solar cells

The performance of CdS/CdTe solar cells made with evaporated Cu as a primary back contact was studied through current-voltage (JV) at different temperatures and intensities, quantum efficiency (QE) under light and voltage bias, capacitance-voltage (CV), drive-level-capacitance-profiling (DLCP), and time-resolved photoluminescence (TRPL) measurements. Varying Cu amounts were evaporated on the chemically etched CdTe surface to form the primary back-contact layer. The effect of inclusion of Cu is not limited to the back–contact layer where it is deposited. Cu is well known to be a fast diffuser in p–CdTe, and hence, a significant amount of Cu could reach and affect both the CdTe and CdS layers. Hence, the effect of the presence of Cu on the individual layers: back-contact, the absorber (CdTe) and the window (CdS) layers will be discussed respectively.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

4.1 Effect of Cu incorporation at the back-contact layer

Satisfactory performance of CdTe based solar cells depends on the formation of a low-barrier, low-resistance back–contact, which is frequently accomplished by incorporating Cu at the back-contact. The two different back-contact structures that incorporate Cu as a key element, (a) $Cu_{1.4}Te$:HgTe doped graphite and (b) evaporated-Cu back-contacts, were described earlier.

(a) $Cu_{1.4}Te$:HgTe doped graphite back–contact

A $Cu_{1.4}Te$:HgTe-doped graphite paste, which is commonly used in back-contact formation, was applied on a chemically etched CdTe surface of SnO_2/CdS/CdTe devices to form the back–contact. The role of Cu at the back–contact layer was studied by compar-

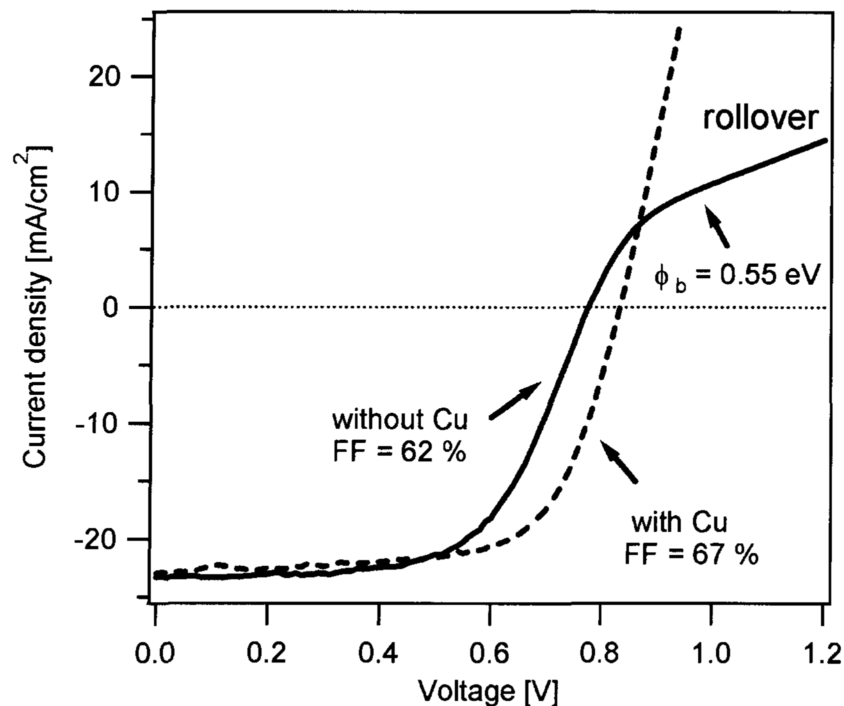

Figure 4.1: The current-voltage curves of devices made with and without Cu in the graphite paste that forms the primary contact.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

ing devices with and without the inclusion of the $Cu_{1.4}Te$:HgTe dopant in the graphite paste. The current–voltage curves of these devices with and without Cu are shown in figure 4.1. The fill-factor increased from 62% to 67% with the inclusion of Cu. In the absence of Cu, a current–limiting effect, rollover or distortion in the current-voltage curves, which is a characteristic of a rectifying contact, was observed. Using the technique described in Chapter 2, the back–contact barrier height of the device with rollover (distortion) was estimated to be 0.55 eV. In the presence of an optimal amount of Cu in the graphite layer, a quasi ohmic-contact was formed, hence, no rollover(distortion) was observed. As a result the fill-factor increased significantly, and the barrier height was smaller than 0.4 eV. This upper limit of the barrier can be inferred from the FF vs. barrier height relation shown in figure 2.8 (Chapter 2). The graphite layer is mainly used as a source of Cu, but

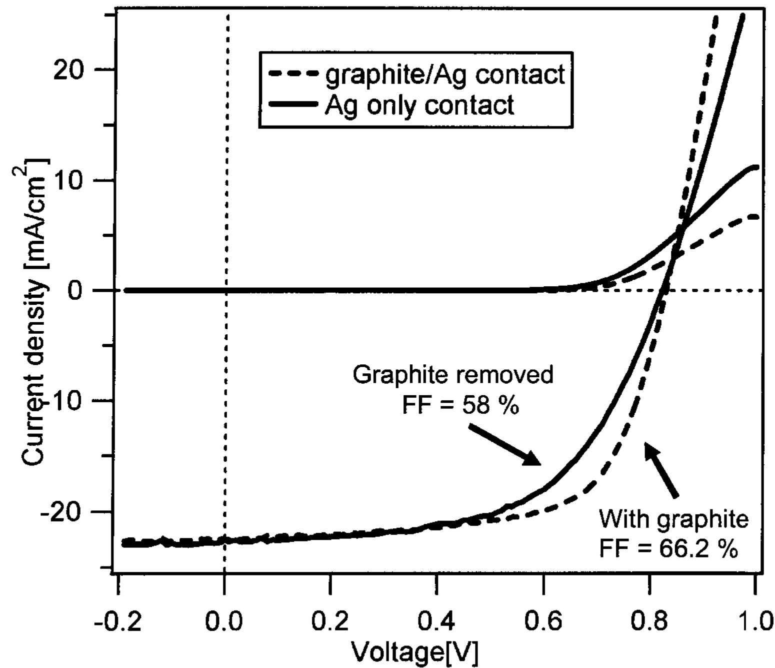

Figure 4.2: The effect of the graphite layer on the J–V curve.

it could also have additional functions. This possibility was investigated by removing the graphite paste after the annealing but prior to the application of the Ag-paste current

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

carrying electrode. The $Cu_{1.4}Te$:HgTe-doped graphite was applied on the CdTe surface followed by anneal at 280°C. In one set of devices the graphite paste was intentionally removed by ultrasonic rinsing in methylethylketone (MEK) solvent, prior to the application of the Ag paste current-carrying electrode. In a second set of devices, the graphite was left intact, and then Ag paste was applied. The two structures will be referred as graphite/Ag and Ag only contacts. The current–voltage curves of the resulting devices are shown in figure 4.2. Both, devices had similar V_{oc} and J_{sc}, but the fill-factor of the devices made with the graphite removed was smaller, due to higher series resistance. Thus, the presence of the graphite contributed to a lower contact resistance.

(b) Evaporated-Cu contacts

The back-contact using graphite paste consists of multiple compounds, carbon and a polymer binder. This complexity makes it difficult to study, control and reproduce the result. Moreover, it is not easily scalable to industrial size. Nevertheless, high efficiency CdTe based devices [40], including the record device to-date [6], utilize this Cu–doped graphite paste. In an alternative approach, the complex back–contact layer was replaced with a relatively simple one in which Cu metal of varying thickness was evaporated on the Te-rich CdTe surface to systematically study the effect of Cu on the performance. Cu metal of varying thickness, 0–170 nm, was evaporated on the Te-rich CdTe surface, followed by an anneal step at 280°C in flowing He atmosphere as described in section 3.1.1. During the heat treatment, Cu was reacted with Te to form a Cu_xTe layer and was also effectively incorporated in the CdTe layer. A control sample, which had no intentional Cu on the back–contact, underwent an identical anneal. All devices were completed by evaporating 60–nm Pd and 300–nm Al layers to form a current carrying electrode. All these devices had the conventional glass/SnO_2/CdS/CdTe/back–contact

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

structure, and the current–voltage curves with varying amounts of Cu are shown in figure 4.3.

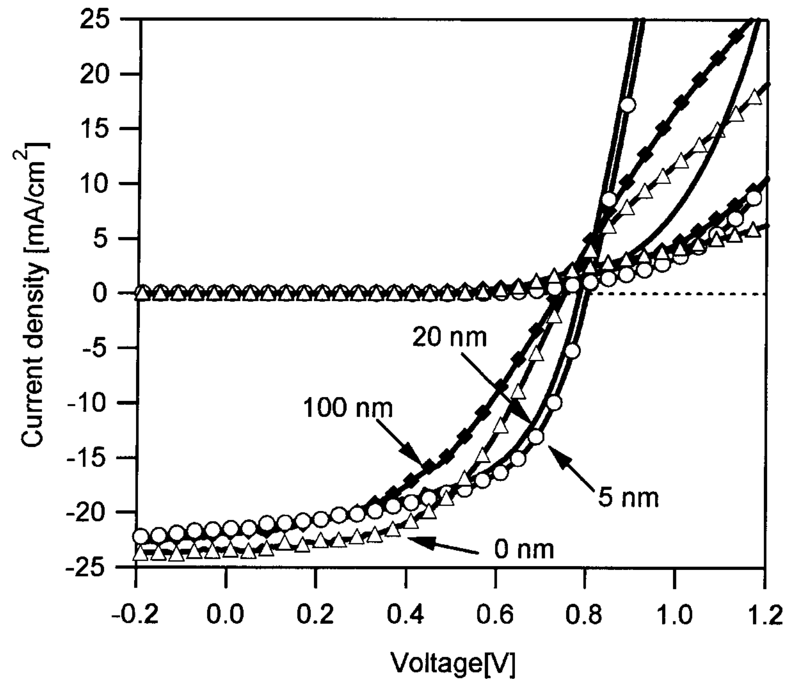

Figure 4.3: J-V as a function of Cu thickness.

The device made with no intentional Cu, and the device made with excess Cu (100–nm) have shown a current limiting effect, distortion (rollover), in the far–forward bias voltage, due to a relatively higher back–barrier. The device with 170-nm Cu was severely shunted, and a signature of the shunt was clearly seen in light-beam-induced-current (LBIC) and infrared or thermal heating (IR) images (figure 4.4). The shunt path has low response in the LBIC map, and the bright spot in the IR image is due to heat generated by the same shunt path. For devices made with a relative optimal amount of Cu, 5-20 nm, the back–contact behavior was significantly improved and no rollover was observed. In general, the effect of the amount of Cu used at the back-contact region primary affected the J-V slope. The lower fill-factor and lower efficiency observed in

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

this set of devices compared to the devices completed with a Cu–doped graphite paste contact could be due to excess diffusion of Cu as a result of a relatively high back–contact annealing temperature.

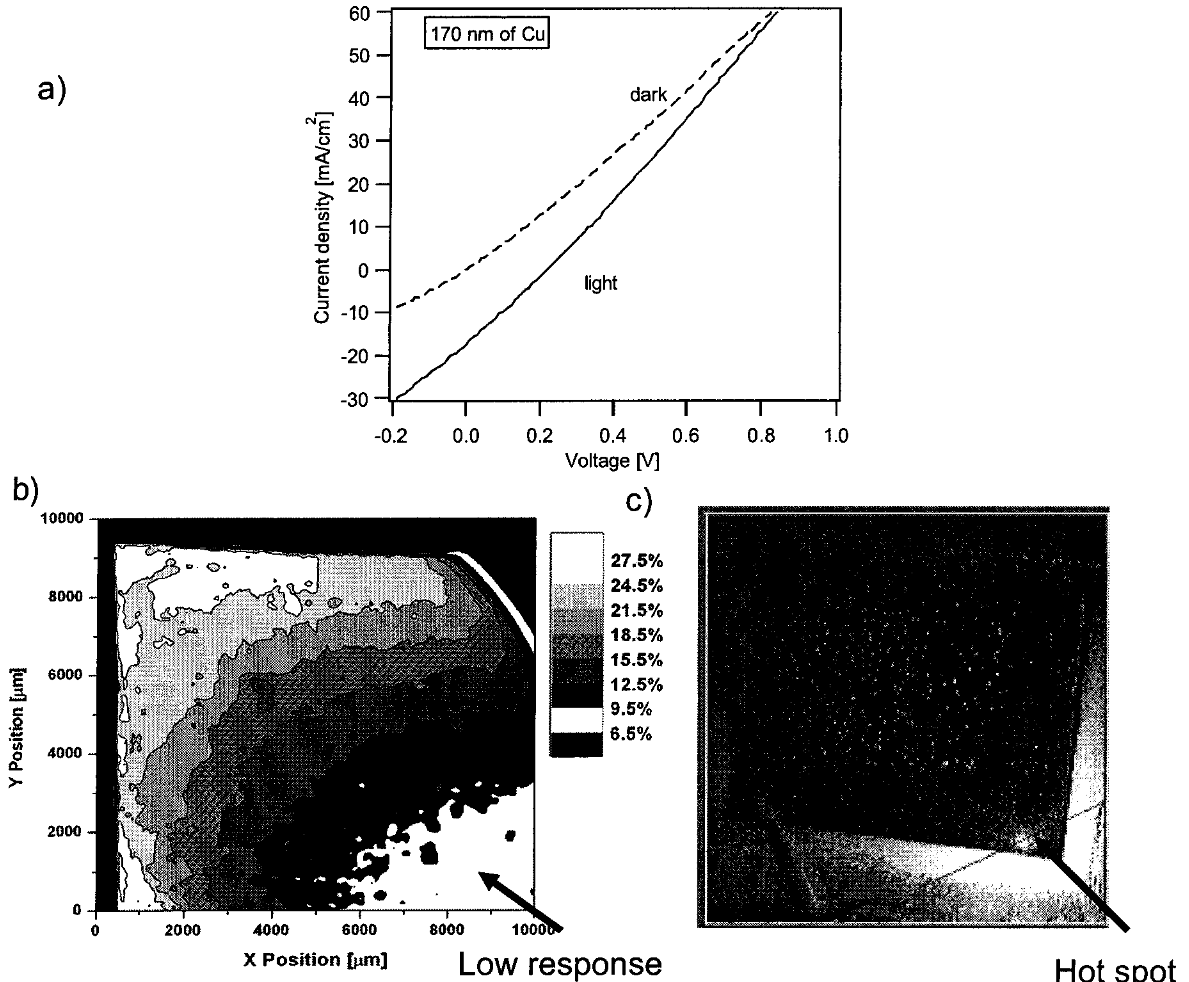

Figure 4.4: (a) Shunted dark and light J-V curves of the device with 170-nm Cu, (b) LBIC map and (c) infrared (IR) images of the device clearly showed the shunt location.

The optimum back–contact annealing temperature for Cu-doped graphite paste contact is about 280°C. However, this temperature could be somewhat higher than optimal for evaporated Cu contacts that use elemental Cu as a source, and could enhance the diffusion of Cu towards the main junction. Low fill–factors of similar magnitude are also observed in devices made with the standard Cu-doped graphite paste back–contact, after such devices were subjected to elevated temperature and illumination in long-term

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

stability study, and this will be discussed in Chapter 5.

Effect of back–contact annealing temperature:

The back–contact annealing temperature plays a major role in how Cu diffuses toward the main junction and also in the formation of Cu_xTe layer. In a subsequent separate study, a fixed amount of Cu (5 nm) was evaporated on the CdTe surface, and then the back-contact layer was annealed at lower temperatures, 200 and 240°C, to slow the diffusion of Cu and optimize the formation of Cu_xTe. A variety of metals was evaporated to form the electrode: Ag, Al, Au, Cr, Pd, Pt and Ni. Multiple devices with each electrode were measured. All other device processing steps, including the chemical etch step, were kept the same. The current-voltage curves for typical devices made with 5–nm Cu and different metals as electrode are shown in figure 4.5. In general, it was found that the devices that were annealed at lower temperature, 200°C, have higher fill-factors, higher efficiencies, but lower V_{oc} than the devices that were annealed at 280°C. There was no distortion (rollover) in the JV curve, and the series resistances were significantly smaller, and hence better FF than those devices annealed at 280°C. The photovoltaic parameters extracted using the techniques described in Chapter 1 are tabulated in Table 4.1. One striking feature observed with these devices, is that the dark J-V curves were well-behaved, and as a result no dark/light crossover was observed. This could be a strong evidence that by lowering the anneal-temperature, diffusion of Cu is minimized, and hence the formation of a Cu_xTe layer is optimized.

The devices in this set have variety of metals as a current-carrying electrode. Of all the devices, only those made with Al and Ag electrode, did not perform well. Two different reasons were responsible for their poor performance. The series resistance R_s of the devices with Ag electrode was higher than the rest of the devices with good performance,

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

and the diffusion of Ag toward the bulk layer probably resulted in significantly lower V_{oc} observed.

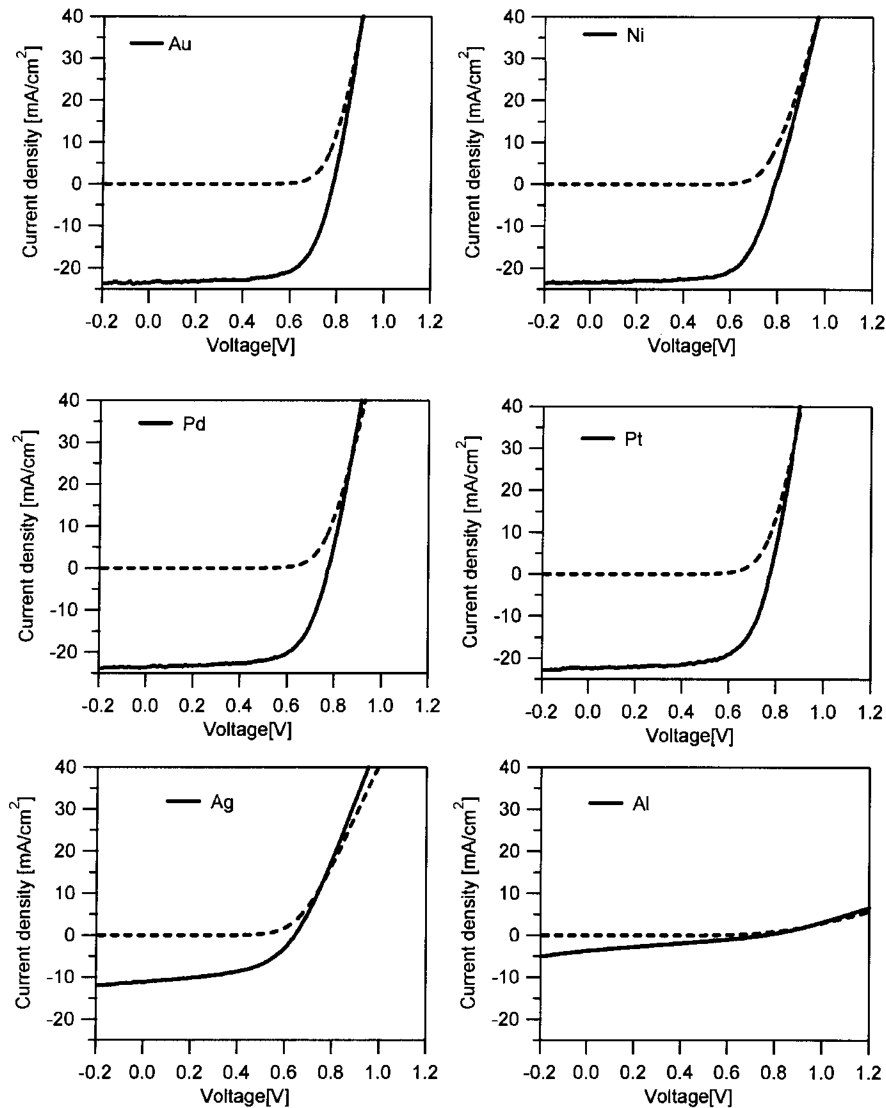

Figure 4.5: J–V characteristics of devices made with 5-nm Cu, and different metals as current-carrying electrodes.

The devices made with Al electrode, had a very large R_s which also resulted in a very low short-circuit current (3.7 mA/cm^2), but the open-circuit voltage (751 mV) was not significantly different from the devices with higher performance. This suggests the problem is mainly related to the formation of a resistive electrode resulting from the

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

reaction of Al and Te. The current density at a forward bias of 1 V, was higher than 40 mA/cm^2 for all the devices, except those with an Al electrode, where it was smaller than 4 mA/cm^2 and minimally resembled a diode.

Table 4.1: PV parameters of SnO_2/CdS/CdTe devices with evaporated–Cu/metal contacts

metal	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]	R_{sh} [Ω-cm^2]	R_s [Ω-cm^2]	J_o [mA/cm^2]	A
Ag	642	11.1	50.5	3.6	400	4	-	-
Al	751	3.7	27.5	0.8	-	40	-	-
Au	780	23.5	68.1	12.5	900	0.2	2.8×10^{-5}	2.8
Ni	790	23.4	67.8	12.5	1100	0.9	3.5×10^{-4}	2.8
Pd	774	23.7	66.4	12.2	700	0.8	2.8×10^{-4}	2.7
Pt	770	22.4	66.6	11.5	600	0.4	8.7×10^{-4}	2.8

The shunt resistances extracted from the dark J–V were reasonably high for all devices (including for devices made with Ag and Al electrodes), which suggested that the poor performance of the devices made with Al and Ag is not related to a shunting effect. The poor performance for the device made with Al electrode is likely due to a resistive layer of Aluminum telluride. Al is highly reactive with Te, the heat of formation for Al_2Te_3 is H_f = -76.1 kcal/mol. In contrast, Pt is non reactive with Te, and for PtTe; H_f = -10 kcal/mol [41]. The heats of telluride formation for different metals are shown in Table 4.2.

The conclusion is that metals used to form the current-carrying electrode that are highly reactive with Te can also substantially affect the overall device performance.

Little difference in device parameters was found when Au, Ni, Pd and Pt electrodes were used. This indicates that for these contact metals, the back-contact interface is controlled predominantly by the CdTe/Cu_xTe interface, and hence most metals with

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

reasonable conductivity can be used. However, the diffusion of the metal can alter the back-contact interface or the CdTe/CdS junction (such as Ag and Al), hence a metal choice should be made to prevent this from occurring.

Table 4.2: Heats of telluride formation

Metal	Telluride	ΔH_f [kcal/mol]
Ag	Ag_2Te	-8.6
Al	Al_2Te_3	-76.1
Au	$AuTe_2$	-4.5
Cd	CdTe	-24.1
Cu	Cu_2Te	-10.0
Pt	Pt_2Te	-10.0

The performance of the cells made with 5-nm Cu, annealed at 200°C, which had Au, Ni, Pd or Pt current-carrying electrode is comparable to the cells made with the standard Cu-doped graphite paste when the same CdTe absorber is used. This is a very encouraging result, which will avoid some of the problems associated with the formation of back–contact to CdTe layer, furthermore this approach is compatible with module fabrication technologies.

Figure 4.6, compares devices with evaporated-Cu contacts and Cu-doped graphite contacts. The performance of the cells with evaporated-Cu contact was significantly improved when the back-contact annealing temperature was lowered to 200°C. The 280°C anneal temperature was optimized for the standard Cu-doped graphite contacts, however, this temperature was somewhat higher when elemental Cu was used as a source, and hence the diffusion of Cu was enhanced that resulted in increased Cu-related recombination, which resulted in reduced collection efficiency. This detrimental effect of Cu diffusion was minimized when the anneal temperature was lowered.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

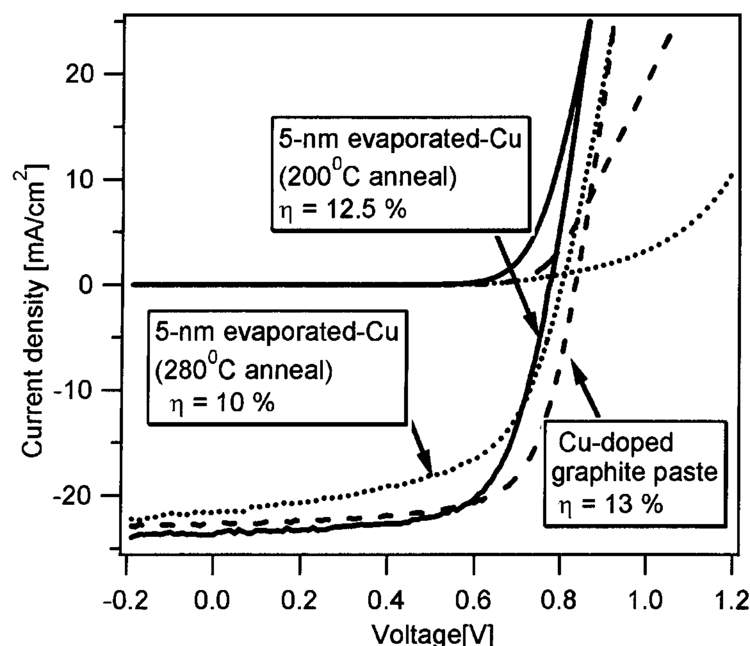

Figure 4.6: Comparison of the J-V curves for devices made with different back-contact processes.

(C) Alternative cell structure.

In addition to the back–contact process, the earlier processes such as the $CdCl_2$ treatment and the quality of the CdTe layer could also have a significant impact on the diffusivity of Cu, and the other metals, that are deposited to form back-contact. To investigate the effect of such processes, devices made with a slightly different structure, the modified glass/Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe structure were used. The $CdCl_2$ treatment was done at higher temperature and for longer time than in the conventional structure. Also, a different TCO layer was used to form the front contact. The NP acidic etch was similar to that used in the conventional structure. Here also, elemental Cu of varying thickness were evaporated, followed by anneal in He atmosphere at temperature of 240^{0}C, then a thick layer of un-doped graphite paste was brushed on, and devices were completed with a Ag paste to form an electrode.

The current-voltage characteristics of the Cd_2SnO_4/Zn_2Sn0_4/CdS:O/CdTe/Cu/graphite/Ag

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

devices made with varying amounts of Cu are shown in Figure 4.7, and the corresponding performance parameters are tabulated in Table 4.3. It should be noted that the diode quality factors were somewhat artificially high. A clear observation with this set of de-

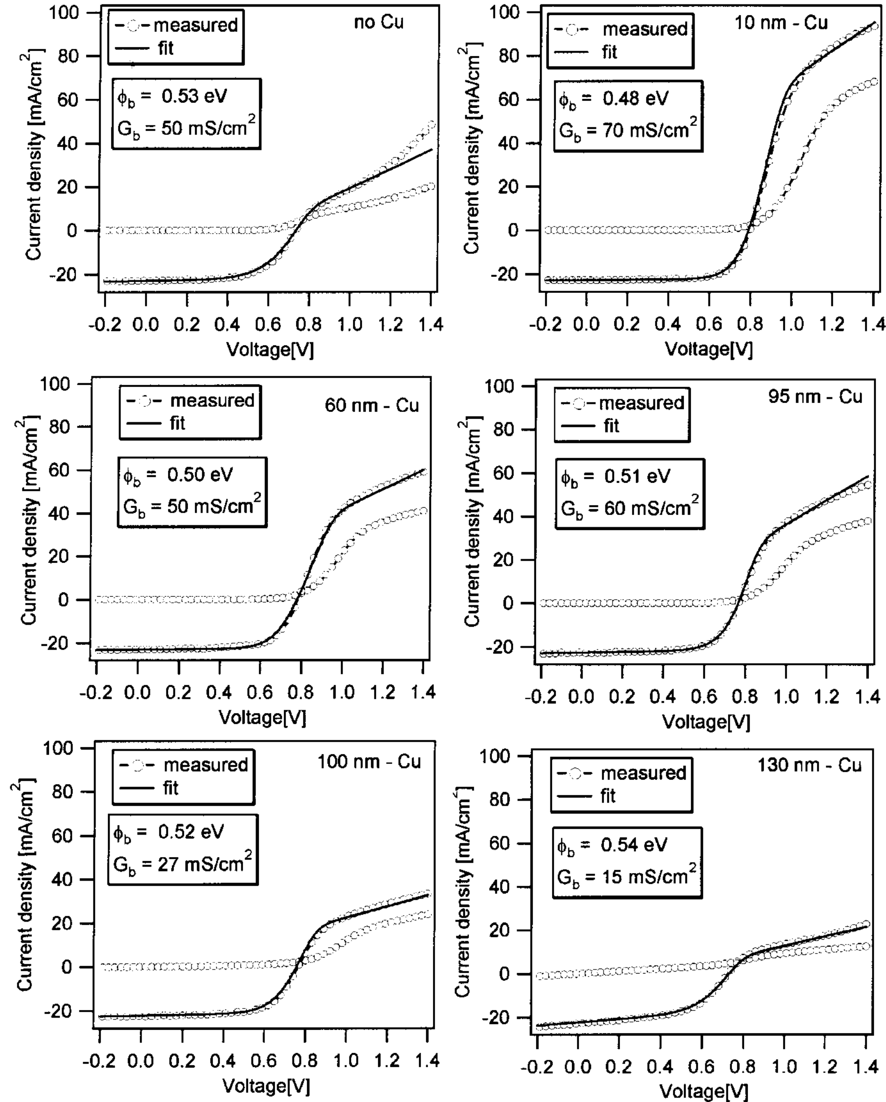

Figure 4.7: J-V curves as a function of Cu thickness for Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe devices.

vices is that the current–limiting effect (rollover) was seen always. However, the degree of the rollover was dependent on the amount of Cu used. The back-barrier heights were estimated using the technique described in chapter 2. The device made with 10-nm Cu

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Table 4.3: PV parameters of Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe devices with evaporated–Cu contacts

Cu thickness nm	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]	R_{sh} [Ω-cm^2]	R_s [Ω-cm^2]	J_o [mA/cm^2]	A
0	733	23.0	59.8	10.1	750	0.8	9.4x10^{-3}	3.6
10	797	22.7	71.3	12.9	1900	1.1	1.2x10^{-5}	2.1
60	783	23.2	68.0	12.1	900	1.8	2.9x10^{-5}	2.2
95	767	22.7	67.2	11.7	700	0.3	3.5x10^{-4}	2.6
110	761	22.2	65.5	11.1	600	1.1	2.8x10^{-4}	2.6
130	730	23.0	53.2	8.9	130	2.1	8.7x10^{-4}	2.8

has the lowest barrier height (0.48 eV), and highest conversion efficiency (12.9%). As the amount of Cu is increased further, an increased back-barrier height was observed, and consequently the efficiency was lowered. Also, the device made with no intentional Cu has a higher barrier height (0.53 eV) than the device made with 10-nm Cu, but smaller than devices with excess Cu. Figure 4.8 shows FF and barrier height as a function of the Cu amounts.

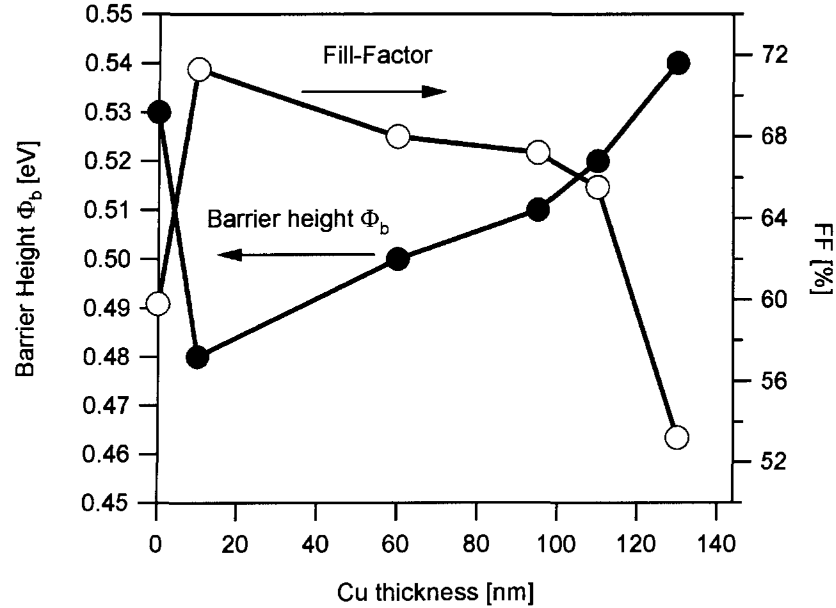

Figure 4.8: FF and Barrier height as a function of Cu amounts for Cd_2SnO_4/Zn_2SnO_4/CdS:O/CdTe devices.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Note that modest changes in barrier height corresponds to large changes in fill-factor. XRD analysis of those devices after the deposition of Cu, but before the application of the graphite layer showed the formation of different phases of Cu_xTe dependent on the amount of Cu used, and device performance was correlated with the phase of the Cu_xTe [42]. This suggests that the barrier height at the CdTe/Cu_xTe junction changes with the Cu:Te ratio in the Cu_xTe layer.

4.2 Effect of Cu on the CdTe (absorber) layer

Cu is deposited at the back-contact to improve the CdTe/back-contact property. However, Cu is known to be a fast diffuser in p-CdTe, and hence, a significant amount of Cu can be present in the CdTe layer in different forms.

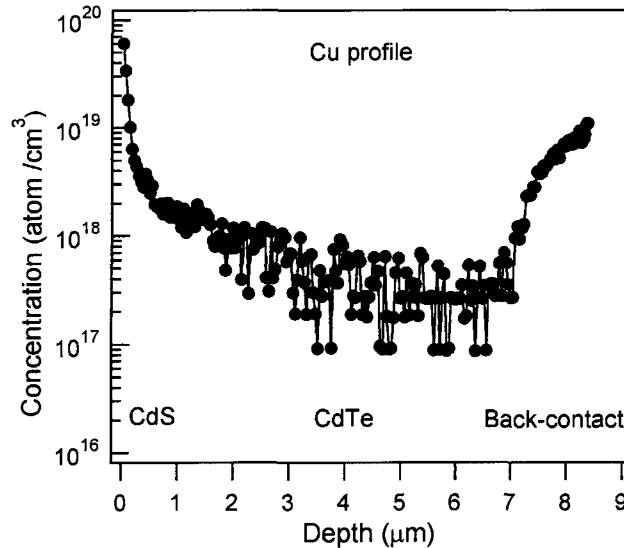

Figure 4.9: SIMS profile of Cu in CdS/CdTe devices with Cu-doped graphite paste contacts.

Figure 4.9 shows the Secondary Ion Mass Spectroscopy (SIMS) profile of Cu in CdS/CdTe device made with the standard Cu-doped graphite contacts that clearly shows the presence of significant amount of Cu in each layer. Cu can form both deep donors

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Cu_i and acceptors Cu_{Cd} in a p–CdTe layer. Substitutional Cu (Cu_{Cd}) will dope the CdTe more p-type, but interstitial Cu (Cu_i) should compensate the p–CdTe. Cu^+ and Cd_2^+ ions are similar in size, based on classical Pauling radii, and hence Cu^+ is believed to substitute readily for Cd_2^+ in CdTe [43, 44] and act as an acceptor. Cu is also believed to form complexes of the types $Cu_i^+ - Cu_{Cd}$ and $Cu_i^+ - V_{Cd}^-$ [45–47]. The application of a varying amount of Cu at the back-contact provides a systematic way of studying what Cu does to the CdTe absorber layer.

Current-voltage (J-V) measurements

J-V curves of devices made with different back-contact processes were shown in the previous section (figure 4.1, figure 4.3 and figure 4.5). In general, the open–circuit voltage is highest for an optimal amount of Cu. For SnO_2/CdS/CdTe devices made with the $Cu_{1.4}$Te:HgTe doped graphite back–contact, the open–circuit voltage was only 775 mV without Cu, but increased to 830 mV with the inclusion of Cu at the back–contact layer (figure 4.1). Similarly, for devices with evaporated-Cu back-contact, the open–circuit was only 700 mV with no Cu and increased to 800 mV with the application of 5-20 nm of Cu that was annealed at 280°C (figure 4.3).

Capacitance-voltage (C-V) measurements.

The C–V profile of the devices was found to vary with the amount of Cu used at the back-contact. Room–temperature capacitance vs. voltage (C-V) measurement of the SnO_2/CdS/CdTe devices made with varying amounts of Cu and then annealed at 280°C are shown in figures 4.10(a). The carrier densities estimated from the C-V measurements are shown in figure 4.10(b).

C-V measurements have shown that the apparent hole density in CdTe increases after the application of a modest amounts of Cu (5-20 nm) at the back contact. As a

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

result higher V_{oc} is obtained. A further increase in Cu (100 nm) resulted in a higher apparent hole density, but a smaller depletion width and a lower V_{oc}. In general, C-V

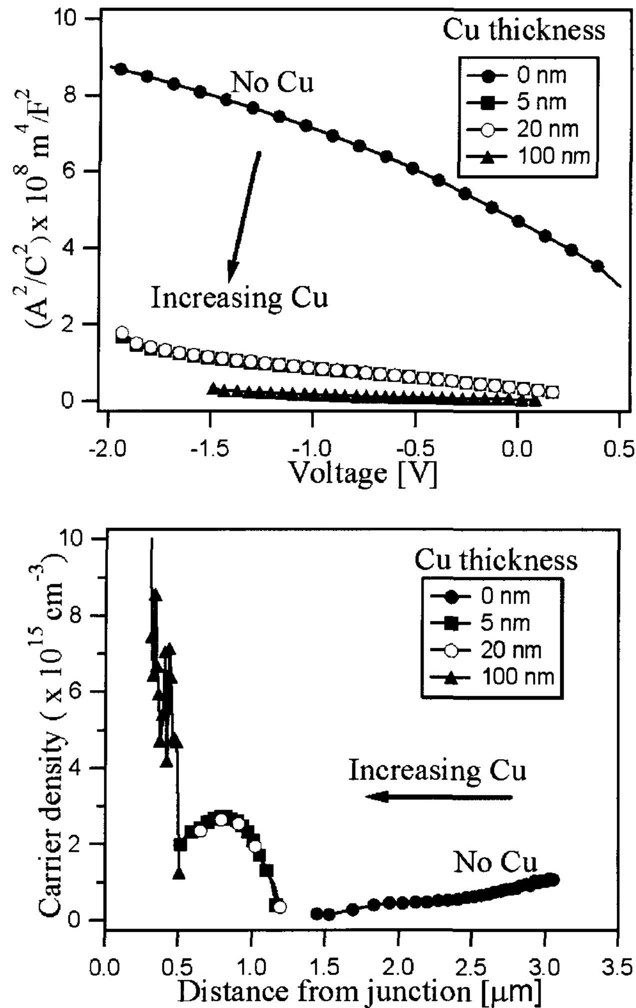

Figure 4.10: (a) Room temperature capacitance-voltage measurement of devices with varying Cu amounts annealed at 280°C, and (b) hole density as a function of the distance from the junction.

measurements show that in the absence of Cu, there is a wide depletion width and a low carrier density. When excess Cu is used, the depletion width becomes smaller, and thus the collection of photo-generated carriers is reduced, resulting in lower V_{oc} and FF.

Since room-temperature C-V measurements may not yield the true hole density, drive–level–capacitance–profiling (DLCP) measurements, as described in section 3.2.4, were

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

used to obtain a more accurate assessment of the free carrier and trap densities. The drive-level carrier density, N_{DL}, obtained from DLCP for two representative devices, without Cu and with 20-nm Cu are shown in figure 4.11.

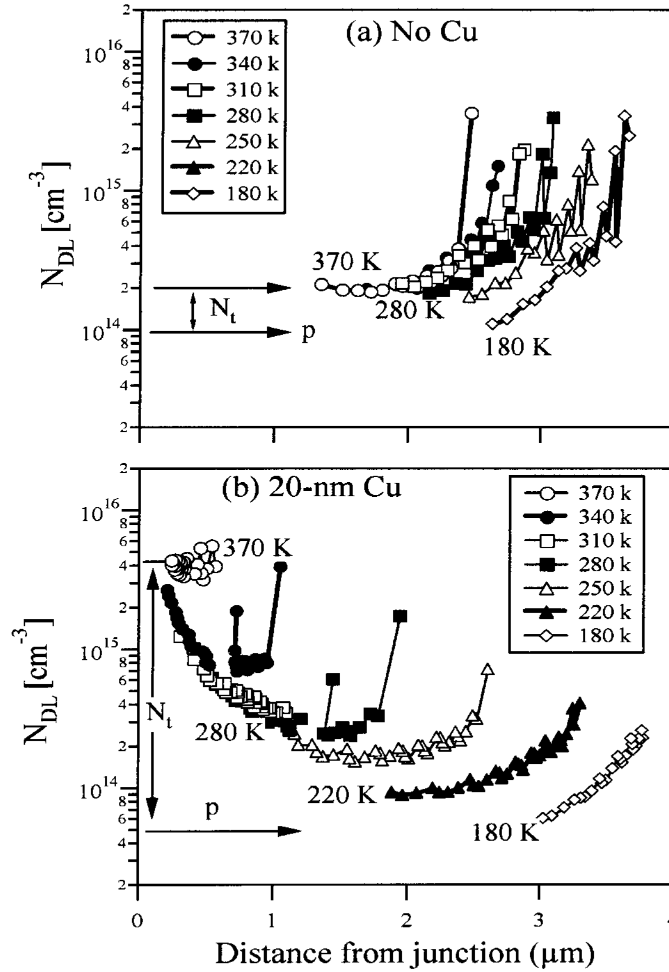

Figure 4.11: Carrier density as a function of the distance from the junction estimated from DLCP measurement (a) no Cu and (b) 20–nm Cu.

At relatively low temperature, the response from deep trap states is minimal, and hence N_{DL} is mainly due to free carrier density p. As temperature is increased, the value of N_{DL} increases because of the ionization of deep trap states. An order of magnitude increase (from 10^{14} cm^{-3} to 10^{15} cm^{-3}) in trap state density was observed as Cu at the back–contact was increased from 0 to 20 nm.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

In general, the defect state concentration was found to increase with the amount of Cu used. This increase in defect states was also corroborated by low-temperature photoluminescence (PL) measurements that recorded a two-order-of magnitude reduction of PL intensity as well as an additional sub–bandgap peak when Cu was added (figure 4.12). The increase in deep-level trap density is arguably responsible for the reduced lifetimes observed with increasing Cu.

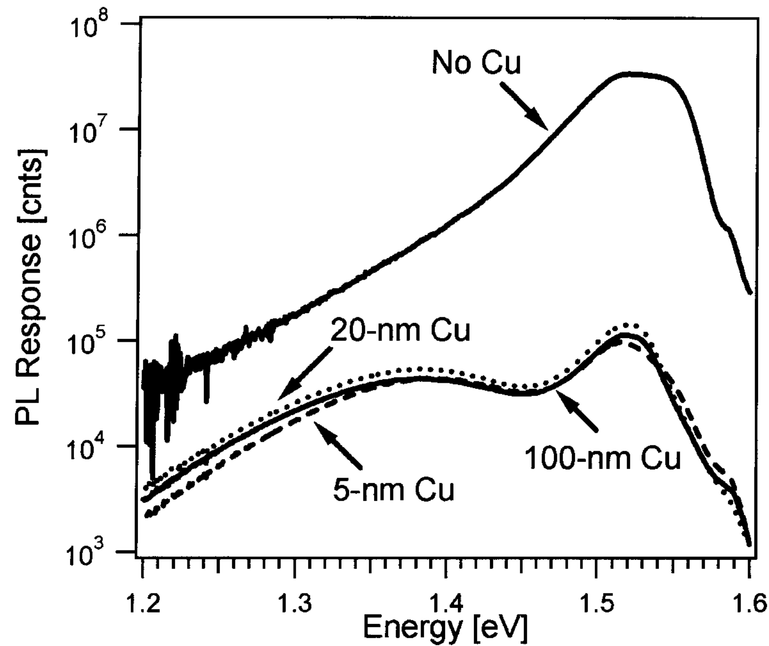

Figure 4.12: Low-temperature (10 K) PL response as a function of Cu amounts

The time-resolved-photoluminescence (TRPL) decay curves for devices made with different amount of Cu, annealed at 280°C, are shown in figure 4.13. Varying the injection level by three orders of magnitude did not significantly affect the decay rates. As shown in figure 4.13, the TRPL-determined lifetime decreased significantly with even a 5–nm addition of Cu and then systematically decreased by small amounts with further Cu addition. The 5-nm case is particularly interesting in that the large lifetime decrease occurred under the same conditions as the large increase in V_{oc} shown in figure 4.3.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

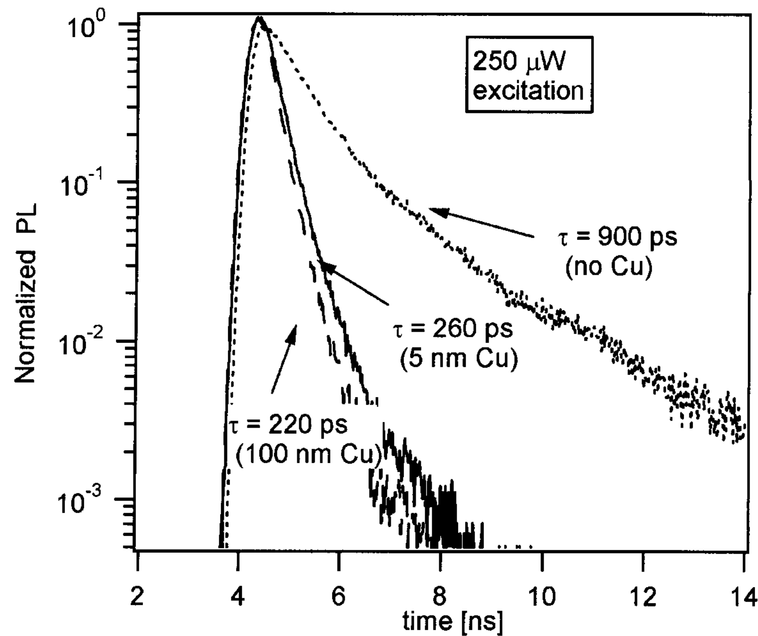

Figure 4.13: Normalized time-resolved photoluminescence (TRPL) decay curves as a function of Cu thickness.

The reduced carrier lifetimes (TRPL result) and reduced depletion widths (C-V result) with increasing Cu amounts also had a significant effect on current collection. The quantum efficiency (QE) measured at zero bias as a function of Cu thickness is shown in figure 4.14a. The primary feature observed is the reduction in longer wavelength response with increasing Cu. In the absence of Cu, a significantly higher long–wavelength response is observed. This again strongly suggests higher recombination of photogenerated carriers in the CdTe layer when Cu-related defects are present.

By systematically increasing the recombination (lowering the lifetime) in the absorber layer, the measured QE curves shown in figure 4.14a could be reproduced numerically. The AMPS-simulated QE curves are shown in figure 4.14b, and the trends are similar to the measured ones.

The QE measured as a function of applied voltage, figure 4.15, indicates minimal voltage–dependent spectral response for devices made without Cu, but increasing voltage

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

dependence when Cu is present. The observed voltage-dependent collection is consistent with the reduced fill-factor in the J-V curve. The curved J-V region below V_{mp} in

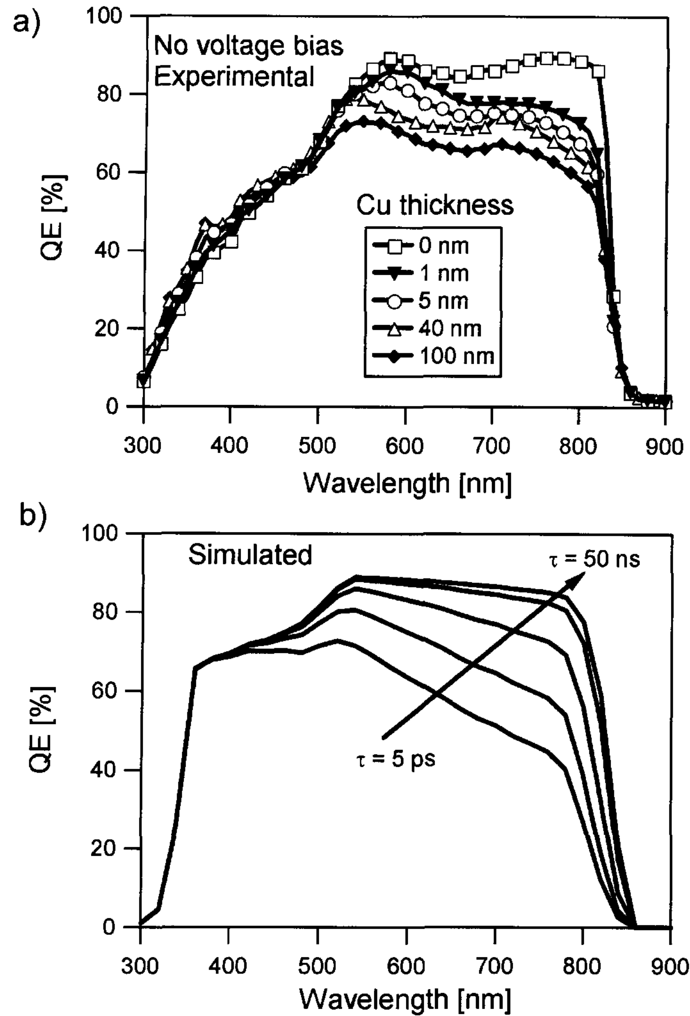

Figure 4.14: (a) QE curves as a function of Cu thickness (no voltage bias), and (b) Evolution of QE curves with changes in lifetime (simulated).

figure 4.16(a) is also a signature of voltage-dependent collection. Defect levels in the CdTe that act as a recombination centers play a major role in reducing the lifetime of photogenerated carriers that will generally result in voltage-dependent collection. The simulated J-V curves in figure 4.16(b), illustrates the correlation of a small carrier lifetime and the resulting degree of voltage-dependent collection.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

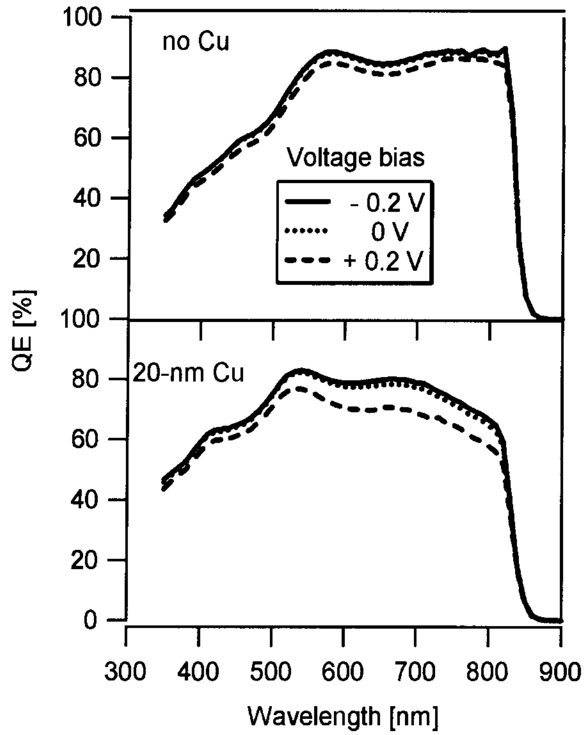

Figure 4.15: QE curves as a function of voltage bias for devices with and without Cu.

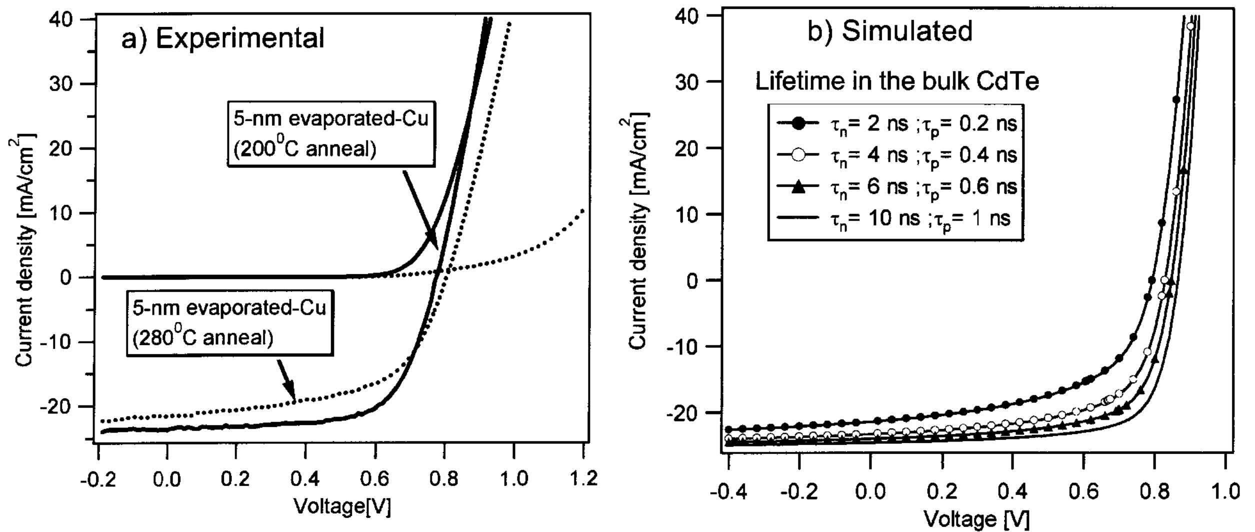

Figure 4.16: (a) Curved J-V (b) the effect of lifetime on the current–voltage characteristics (simulated).

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Analysis of the J-V measurement at different intensities indicates intensity-dependent leakage conductance. Figure 4.17 shows the J-V results at different intensities for devices made with and without Cu. All devices shown in figure 4.3 have dark shunt resistances

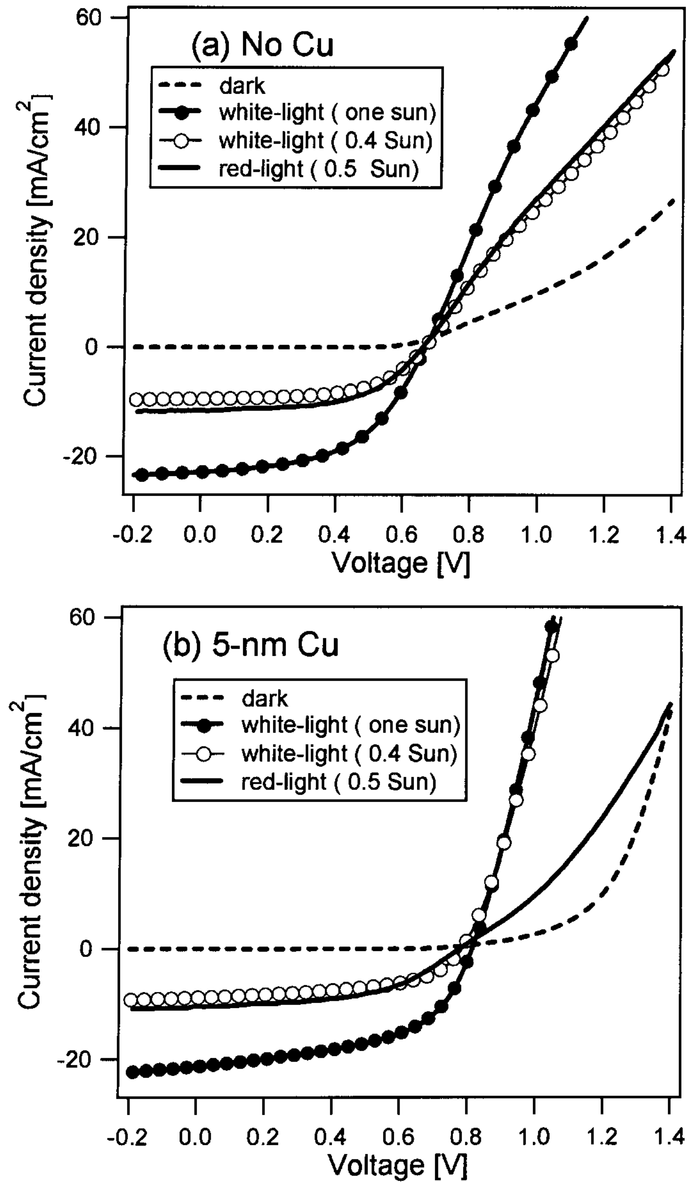

Figure 4.17: JV characteristics as a function of intensity of illumination for: (a) no Cu, and (b) 5-nm Cu devices

larger than 10 kΩ -cm^2. However, under one sun illumination the plots of dJ/dV vs. V near J_{sc} are not flat, and the upper-bound estimates of the "apparent shunt resistances"

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

were in the range of 170-600 Ω -cm^2, dependent on the amount of Cu used. The apparent shunt resistance, Rsh, was found to decrease with increasing Cu thickness. It also decreased with increasing intensity. The increase in leakage conductance (G = 1/R_{sh}) with intensity is probably due to interface defect states whose occupancy is changed by the intensity of illumination.

The standard diode analysis discussed in section 1.3 uses the basic diode equation that assumes photocurrent(J_L= J_{sc}), series and shunt resistance that are independent of voltage and illumination intensity. However, these assumptions may not be true in thin–film polycrystalline solar cells where impurities play a major role in the property of devices. One common deviation from the standard diode behavior is a voltage-dependent current collection, and in the case where the photocurrent is voltage dependent, the plot of dJ/dV plot near J_{sc} will not be flat,

$$\frac{dJ}{dV} \simeq G + \frac{dJ_L}{dV} \tag{4.1}$$

Hence, the extraction of reasonable value of the leakage conductance is difficult, and if the second term in the above equation is neglected, as it often is, then an upper bound for the value of G can be obtained, but this will most likely overestimate the actual value.

In general, the use of the standard techniques for extracting J-V parameters in the presence of voltage-dependent collection and/or spectral-dependent shunt resistance, may not yield credible values. For example, when applied to devices shown in figure 4.3, diode quality factors larger than 3 were estimated from the slope of semi logarithmic plot of the forward current (J+J_L+ VG) vs. (V-JR_s). Such large values should not be possible according to existing recombination theory. Nevertheless, large values of diode

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

quality factors are common with CdTe based solar cells, when the standard approach is implemented. The fact that the parameters are significantly different with and without illumination, strongly cautions against the use of analysis techniques that assume illumination-independent parameters.

Effect of back-contact annealing temperature.

As is shown in figure 4.6, the performance of the devices were substantially improved by lowering the back-contact anneal-temperature to 200°C. However, the open-circuit voltage decreased as anneal temperature decreased, which may suggest that lower temperate will also reduce the Cu p-doping effect in the CdTe layer.

The C-V curves of devices with 5-nm Cu evaporated contact, annealed at 200°C and made with a variety of evaporated metal electrodes, are shown in figure 4.18, and for comparison device made without Cu is also shown.

It was found that these devices had wider depletion and relatively lower carrier density when compared to devices annealed at 280°C. This could explain the lower V_{oc} but higher FF. The TRPL-determined lifetimes of those devices were in the range 820-850 ps, which is much higher than devices with high annealing temperature and similar to those made without Cu. These indicate that by lowering the annealing temperature the concentration of Cu-related defects in the CdTe was minimized, and as a result the overall conversion efficiency was improved.

The capacitance measurements as a function of temperature and frequency of the devices with different current-carrying electrodes are shown in figure 4.19. The responses for devices with Au, Ni, and Al electrode look somewhat similar. However, the device with Ag electrode has a different signature due to different trap levels related to the diffusion of Ag.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

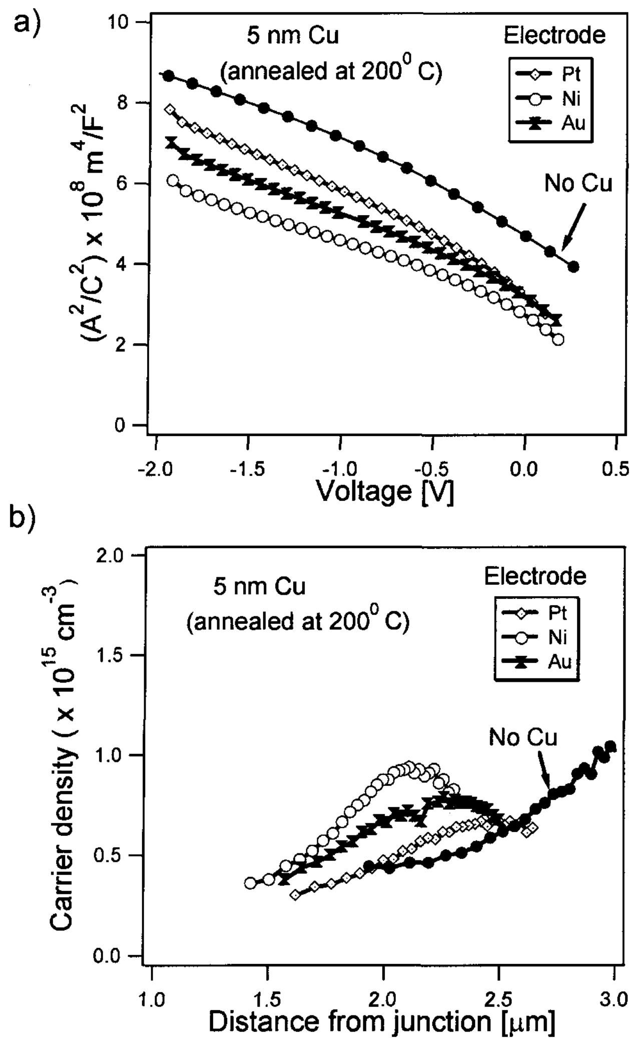

Figure 4.18: (a) Capacitance-voltage measurement, and (b) Carrier density as a function of the distance from the junction, estimated from C-V measurement, for the devices with different metal electrodes.

Local Variations (non-uniformity):

Inherently, polycrystalline materials are non-uniform and local variations are expected in microscopic areas. Device uniformity variations associated with impurity diffusion from the back-contact layer were studied by Light-beam-induced-current (LBIC) measurements. LBIC is a small-spot measurement technique that uses a focused diode laser with intensity at the cell adjusted to approximately one sun [48].

The measurements were performed at zero bias by scanning a 100-μm spot-size laser

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

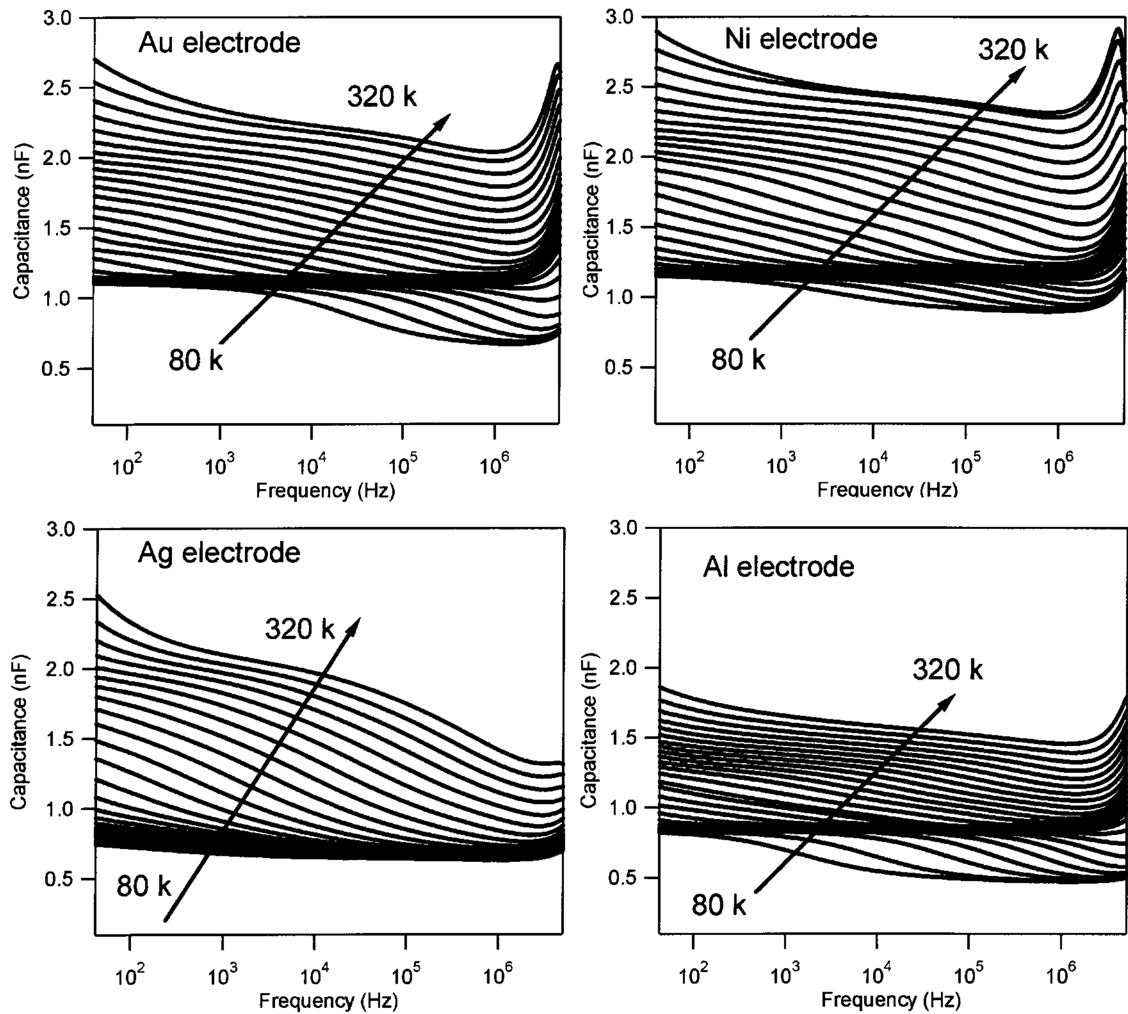

Figure 4.19: Capacitance-frequency measurements as a function of temperature for devices with Au, Ni, Ag and Al current-carrying electrodes.

beam at 638 nm (well above the CdTe band gap) over the device area through the glass substrate, and the resulting photocurrent mappings are shown in figure 4.20. The devices that use Au and Ni (and similarly Pd, and Pt) as a current-carrying electrode showed a reasonably uniform response, the device contacted with Ag has showed non-uniformity in mm scale, which is likely due to the diffusion of Ag. The device made with Al contact had overall a much lower response probably due to a non-uniform resistive layer at the contact.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

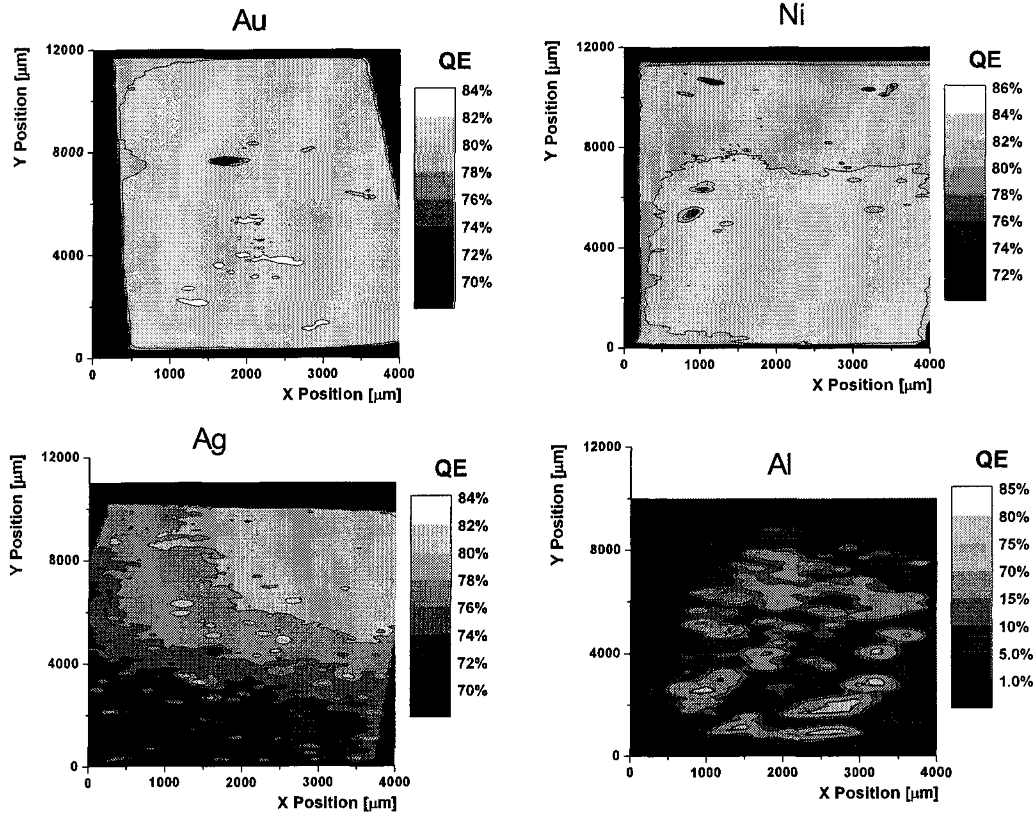

Figure 4.20: LBIC photocurrent mapping of devices made with Au, Ni, Ag, and Al as a current-carrying electrode.

4.3 Effect of Cu on the CdS (window) layer

The secondary-ion-mass-spectroscopy (SIMS) profile, figure 4.9, showed that in CdS/CdTe solar cells a significant amount of Cu diffuses toward the CdS/CdTe junction and much of it accumulates in the CdS layer. Cu concentrations in the CdS are found to be comparable to the Cu concentration in the back-contact where Cu was deposited. Cu is known to form acceptor states at about 0.34 and 1.2 eV (mid-gap) from the valence band in n-CdS [49] that readily compensate the CdS, which likely result in more intrinsic CdS. The effect of the presence of Cu in the CdS layer was also studied by applying varying amounts of Cu at the back-contact layer, followed by different temperature anneal steps. It was found out that the presence of Cu in the CdS has minimal impact on the

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

actual device performance, but was responsible for non–idealities in the dark data: (a) dark/light J-V crossover and b) apparent quantum efficiency (AQE) larger than unity, observed in CdS/CdTe solar cells. The results are discussed below.

a) Dark/light Crossover.

Ideally, the J-V curve in the light is the J-V curve in the dark shifted by the photocurrent, as shown in figure 1.4 of chapter 1. However, this is not true when the parameters of the device in the dark differ from the values under illumination. Consequently, the J-V curves in the dark and under illumination will in some cases cross each other. This situation is commonly known as dark/light crossover. The J-V curves of the devices made with varying Cu amounts, figure 4.3 and figure 4.7, had a large crossover. However, the devices made without Cu did not show significant crossover. This is a strong evidence that the crossover is related to the inclusion of Cu in the device.

The presence of Cu related acceptors in the n-CdS layer significantly impacts the photosensitivity of CdS. These deep acceptor states trap most of the free electrons contributed by the donors, resulting in low free electron concentration, and hence increased resistivity of CdS in the dark. Under illumination, however, photons absorbed in the CdS layer will greatly increase the concentration of both free electrons and holes, and many of the deep defect levels will be occupied by photogenerated holes, and thus the carrier density of CdS will increases substantially under illumination [50]. Hence, the difference in carrier density of CdS between the values in the dark and under illumination (photosensitive CdS) is responsible for the dark/light crossover observed in devices made with Cu at the back–contact. The fact that no significant crossover is observed in the absence of Cu, is strong evidence that crossover is related to the presence of Cu in the CdS.

The trends in the crossover were investigated in detail by taking J-V measurements

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

under limited spectrum (sub-bandgap photons only) and under varying intensity of illumination (figure 4.21).

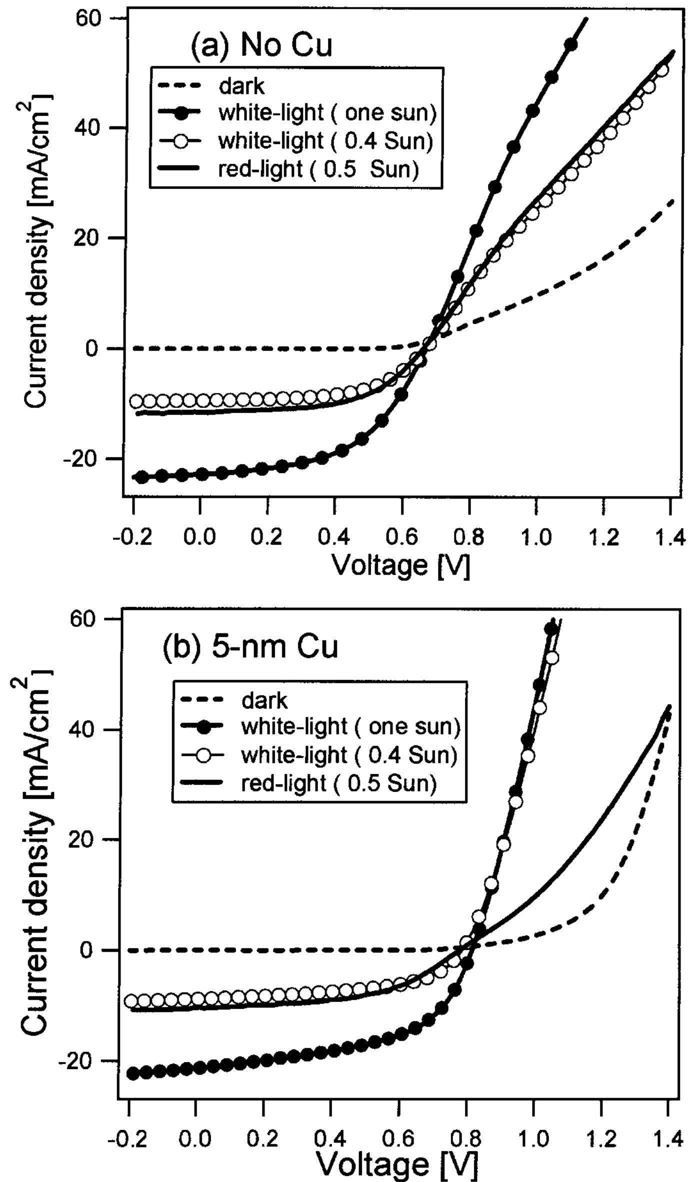

Figure 4.21: JV curves under white-and red-light illumination of comparable intensites of devices made (a) without Cu and (b) with 5-nm Cu at the back-contact.

For devices with no intentional Cu, the J-V curves under red-light and under white-light illumination of similar intensities were very similar. However, in the presence of Cu, a larger crossover was observed under white-light illumination than under red-light

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

illumination of comparable intensity. Moreover, the J-V curve in the first-quadrant of the device with Cu was intensity independent, no distinction was seen among 0.4 and 1 sun white-light illumination (figure 4.21(b)) . In general, the trend of the J-V curve in the first-quadrant was sensitive to the spectral content of the illumination in the presence of Cu. In contrast, no systematic change was seen in the absence of Cu. This indicates that the crossover observed is mainly attributed to the photosensitivity of CdS due to the absorption of blue photons in the CdS.

Figure 4.22, shows a numerical simulation (AMPS-1D) result that shows crossover as a function of defect state concentration in the CdS. As the defect concentration in

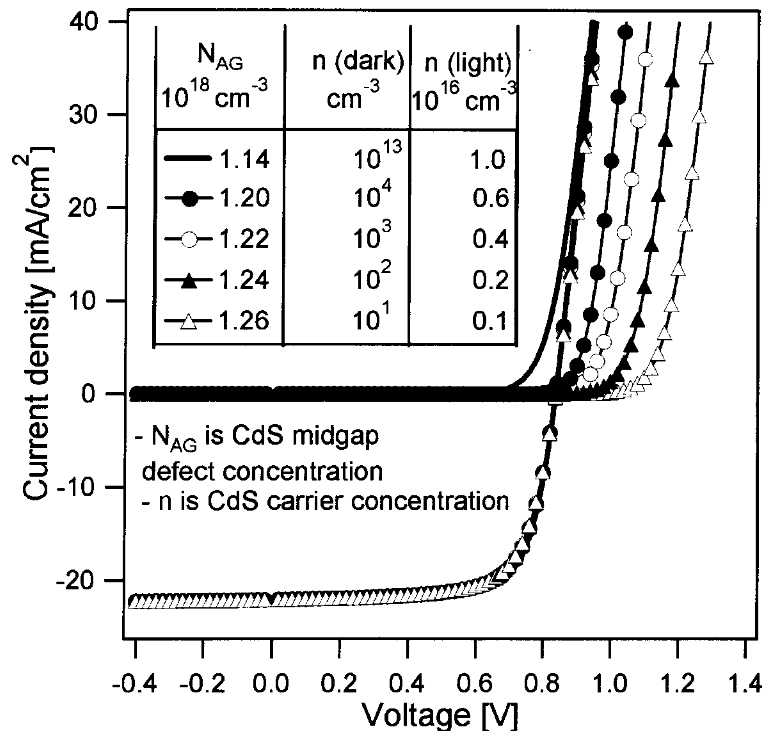

Figure 4.22: Increase in the crossover of the dark/light curves with increase in defect concentration in CdS. The corresponding carrier densities in the dark and under illumination are also shown in the inset.

the CdS is systematically increased, the dark free carrier density in the CdS is decreased dramatically. However the carrier density under illumination is not significantly affected,

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

and hence the dark/light difference in carrier concentration in the CdS. The degree of crossover increased progressively in the simulation with increasing defect density in the CdS layer, but no significant change in J–V curve was observed under illumination.

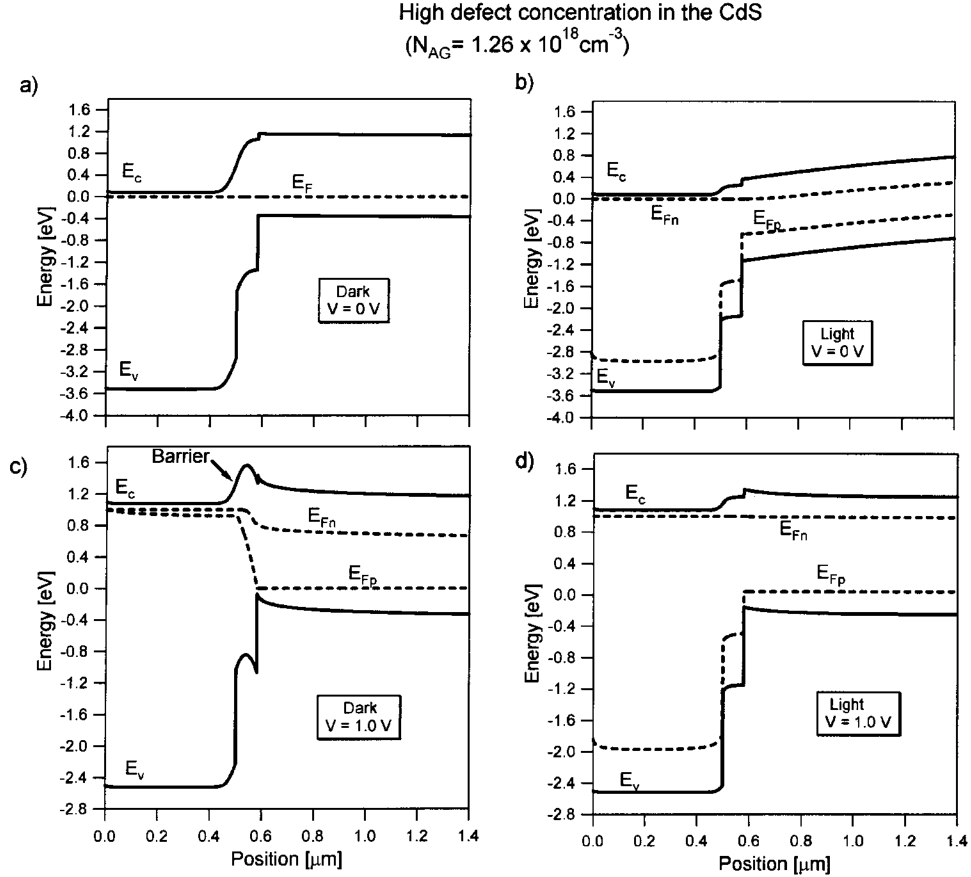

Figure 4.23: The CdS/CdTe energy band diagram in the presence of significant defect concentration in the CdS layer. (a) In the dark and at 0 V bias, (b) Under white light illumination and 0 V bias, (c) In the dark and 1.0 V bias, (d) Under white light illumination and 1.0 V bias.

The donors in the n-CdS layer are compensated by acceptor-like defects, and hence in the dark the Fermi level is closer to midgap, and as a result a barrier is formed at the CdS/CdTe junction. In the light, photo-generated holes neutralize some of the ionized negative charges in the CdS layer that lead to lowering of the barrier at the junction, and this light modulated barrier is mainly responsible for the crossover. Figure 4.23, shows the changes in the conduction band under one-sun illumination and in the dark due to

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

a significant acceptor-like defect concentration in the CdS layer, which resulted in the light-modulated-barrier at the CdS/CdTe junction.

Dark/light crossover is often observed on CdTe based solar cells, and it is also a common observation on NREL devices made with the standard Cu-doped graphite paste contacts, which suggested that even in devices with fairly high efficiency a significant amount of Cu reaches the CdS. However, its impact on device performance should be minimal. The correlation between photosensitive CdS and crossover was further studied by exposing devices to blue-light illumination, which contains photons that are absorbed in the CdS layer.

The crossover disappeared after devices were exposed to blue-light for about 3 hrs. Then, devices were stored in the dark and J–V measurements were performed at a regular time intervals. The crossover was, however, recovered after longer than weeks storage in the dark (figure 4.24), and the likely mechanism that explains the observation is, persistent photoconductivity (PPC) of CdS. When a CdS layer that has low carrier density in the dark due to compensation by Cu-related defects is exposed to a blue-light for a sufficient duration of time , then its carrier density increases and it could stay in the state with relatively higher carrier density for a longer time scale after the illumination is removed, and during this time no crossover will be observed. However, after extended storage in the dark, the devices will relax back to the state with a low carrier density in the dark, and subsequent J–V measurements will display crossover.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

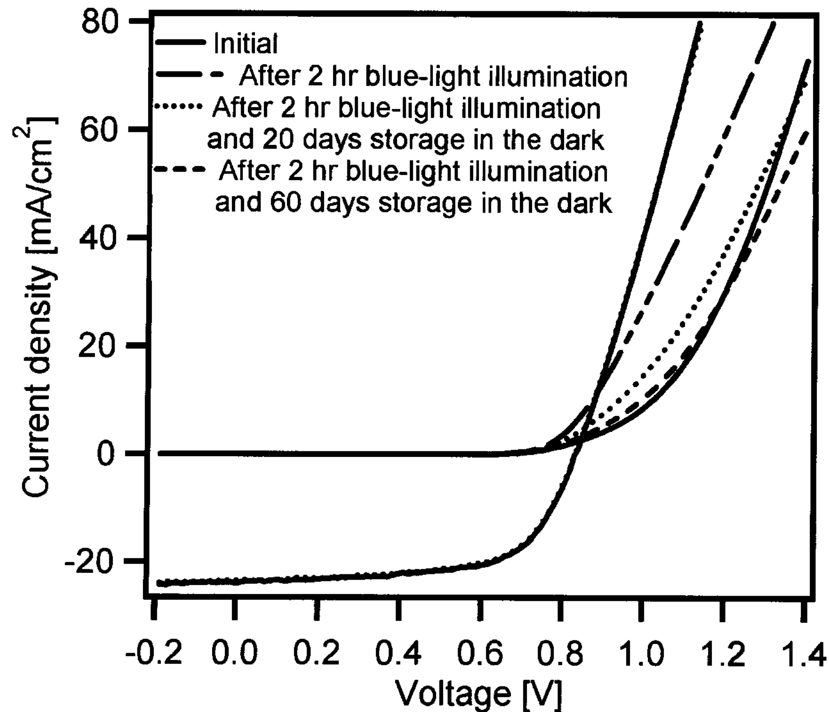

Figure 4.24: Dark/light crossover before and after exposure to blue-light illumination and storage in the dark for a device made with Cu at the back-contact.

Apparent quantum efficiency

Standard quantum efficiency (QE) measurements should yield values less than unity, but when a measurement is done under illumination with a limited spectral range, quantum efficiency larger than unity could be obtained, and this is commonly referred as apparent quantum efficiency (AQE). It should be noted that large AQE does not imply higher conversion efficiency. More importantly, no relationship exist between AQE and device performance. AQE is purely an anomalous effect that is related to the presence of Cu-related defects in the CdS.

In an effort to sort out the effect of Cu in the CdS, QE measurements were done under white-light (entire spectrum), red-light (λ > 600 nm) and blue-light bias (λ <550 nm). Apparent quantum efficiency (AQE) larger than unity under white-light and red-light bias were observed on devices with Cu (5-100 nm) that were annealed at 280°C (figure

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

4.25). The magnitude of the AQE increased with increasing Cu, and it was not observed in the absence of Cu. This strongly suggested that the presence of Cu-related defects are responsible for the AQE effects, and hence, this technique can be effectively used to investigate the presence of Cu related defects in the CdS layer.

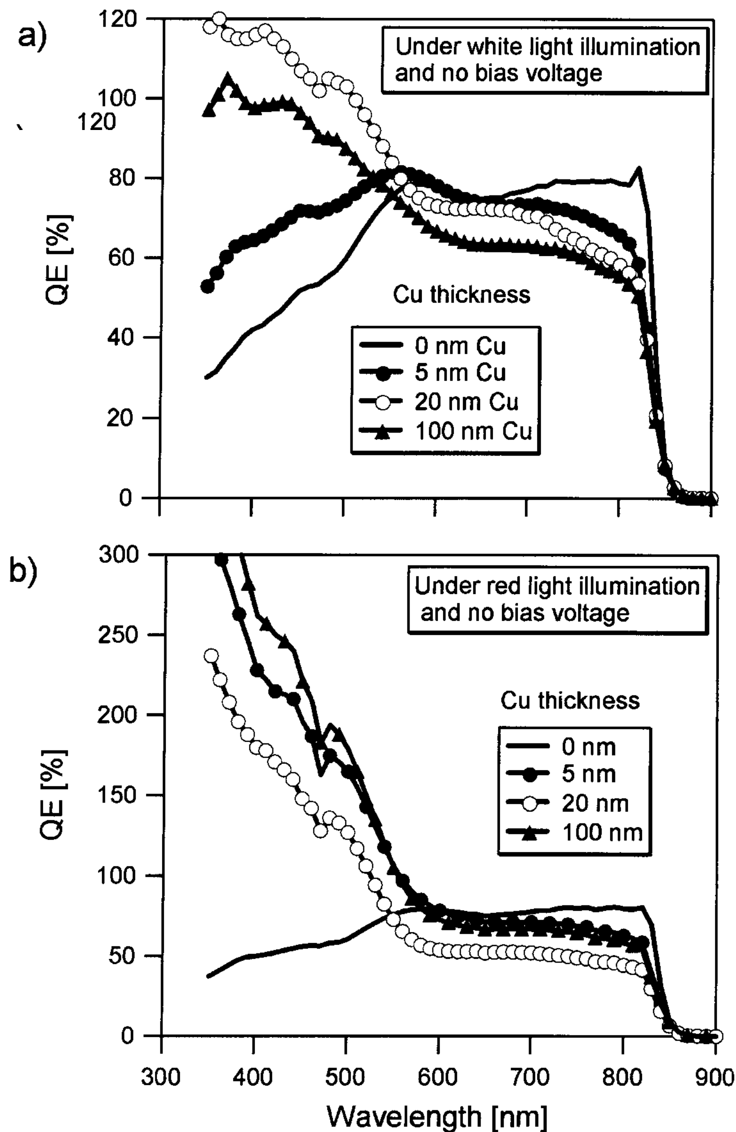

Figure 4.25: QE measured as a function of Cu amounts under light bias: a) white light and b) red light.

Under red-light ($\lambda > 600$ nm) bias, the carriers generated by the red-light will yield a dc current that should be rejected by the lock-in technique, but the chopped blue probe

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

beam of a fixed frequency used in the QE measurement could affect the photosensitivity of CdS, and this change is synchronized with the frequency of the probe beam, thus the depletion width and the barrier at the CdS/CdTe junction will be modulated in phase with the ac probe beam, and as a result some of the carriers generated by the red light bias will be collected by the modulated field, resulting in an ac current that is in phase with the current generated by the probe beam. This current adds to the photocurrent response of the probe beam, consequently, an apparent quantum efficiency larger than unity could be measured. For device with high amounts of Cu (20-100nm), AQE larger than unity were observed under white-light bias, and this suggests that excess Cu is reaching the CdS. A similar AQE observation under red-light illumination in CdS/CdTe solar cells has been reported [51], in which Cu was intentionally incorporated in the CdS layer. Other groups have also discussed AQE effects in CdS/CdTe solar cells [52, 53].

Numerical simulation with AMPS-1D is done to interpret and reproduce experimental results. The input parameters used in the modeling are listed in Table 3.1. A flux density of 1×10^{15} photons/cm^2-s is used for the monochromatic probe beam. Under red-light bias illumination and when the concentration of acceptor-like midgap defect states in the CdS is varied, the series of curves in figure 4.26 are generated. As N_{AG} is increased, the QE values are found to increase in the blue region ($\lambda < 550$ nm), and eventually become larger than unity. The simulated and measured AQE curves have a somewhat similar trend.

In summary, the result shows that the presence of Cu in the CdS is found to be responsible for the dark/light crossover and apparent quantum efficiency observed, however, under operating conditions (one-sun illumination) the presence of Cu in the CdS layers seems benign, but could in the extreme case contribute to series resistance of the

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

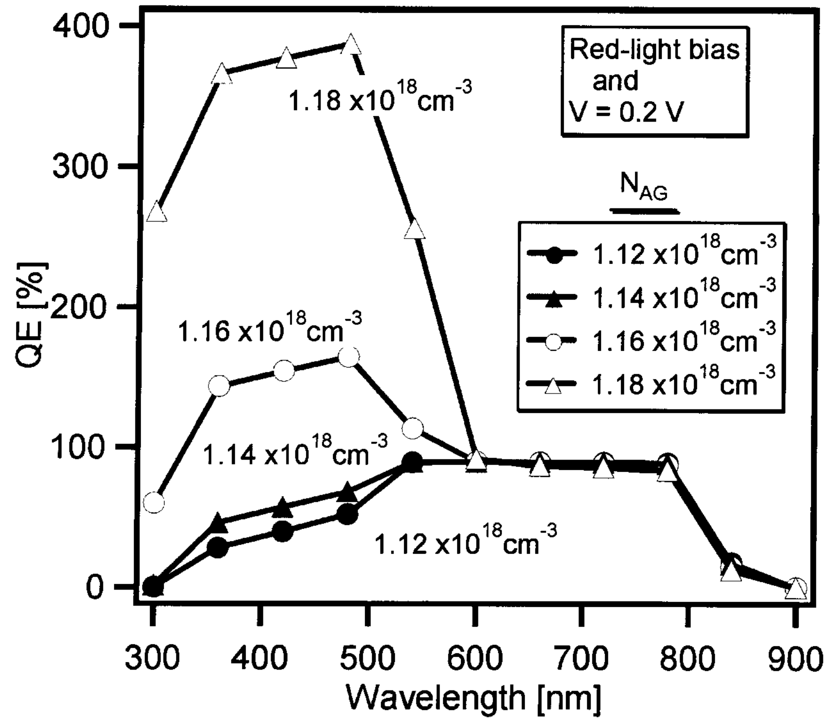

Figure 4.26: AQE as a function of the defect concentration N_{AG} in CdS.

device, which in turn contributes to a lower fill-factor. The disappearance of crossover after prolonged illumination with blue-light with no significant effect on the J–V curve under illumination is a strong evidence that the impact of the presence of Cu in the CdS should be minimal.

For devices made with 5-nm Cu, annealed at low temperature (200°C), figure 4.5, no dark/light crossover, or AQE effect under red–light bias was observed. This indicates that lowering the anneal-temperature the diffusion of Cu was slowed down, and as a result the amount of Cu reaching the CdS layer was minimized, hence non-idealities related to Cu residing in the CdS were not observed.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Chapter 5

Stability of CdS/CdTe solar cells

During long-term stability studies, solar cells, are subjected to combinations of illumination, voltage bias, and elevated temperature for extended periods of time. These conditions will be collectively refereed as stress conditions. Laboratory stress measurements attempt to mimic the conditions a solar module sees outdoors during its lifetime. To accelerate the results, laboratory experiments are often performed at elevated temperature and continuous illuminations (accelerated test). In this study, stability studies focus mainly on degradation (changes) associated with the back-contact layer and the impact of the diffusion of impurities from the back-contact into the CdTe.

5.1 Effect of stress temperature

The temperature at which devices are stressed may activate different modes of device degradation. The stress conditions at which a laboratory-size device should be subjected are not well defined, nor is there a general consensus on what type of accelerated stress conditions best simulate the long–term stability corresponding to real-life conditions.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Typical temperature that ranges from 60°C to 200°C have been used by different groups. The effect of different elevated temperatures should be linked by an acceleration factor, F, which can be expressed by the empirical Arrhenius relationship [54]:

$$F(T, T_u, E_a) = exp\left[\frac{E_a}{k}\left(\frac{1}{T_u} - \frac{1}{T}\right)\right] \quad (5.1)$$

where T_u the effective use temperature, T is the stress temperature, k is Boltzmann constant, and E_a is the activation energy. If the activation energy were 1 eV and an effective use temperature of 50°C, a stress study performed at 100°C for 700 hrs approximates nearly 10 years of actual use. Actual device degradation depends on the climate of the location. For example, field array data from Denver, CO, should have an acceleration factor of 1000 when stressed at a temperature of 100°C [55].

A solar cell stressed at low temperature might appear stable, but the same device stressed at higher temperature or operated in a hotter climate may well deteriorate noticeably overtime. To identify temperature activated degradation, this study stressed similar devices at open-circuit voltage, one–sun illumination, and at four different temperatures (60°C, 80°C, 100°C, and 120°C) in dry air for over 700 hrs. The devices had the conventional SnO_2/CdS/CdTe structure and a $Cu_{1.4}Te$:HgTe doped graphite back-contact. At each temperature, six similar devices were stressed, resulting in a total of 24 devices. The evolution of the current-voltage curves with stress time for those devices that were stressed at different temperatures is shown in figure 5.1. A smoothly increasing back-contact degradation is observed with increasing stress temperature. Rollover (distortion) is observed in the first quadrant of the J-V curves, and the degree of the rollover increased with the stress temperature, clearly indicating a temperature activated degra-

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

dation of the back-contact. This degradation resulted in a reduced fill–factor due to increased series resistance and/or the formation of a blocking contact.

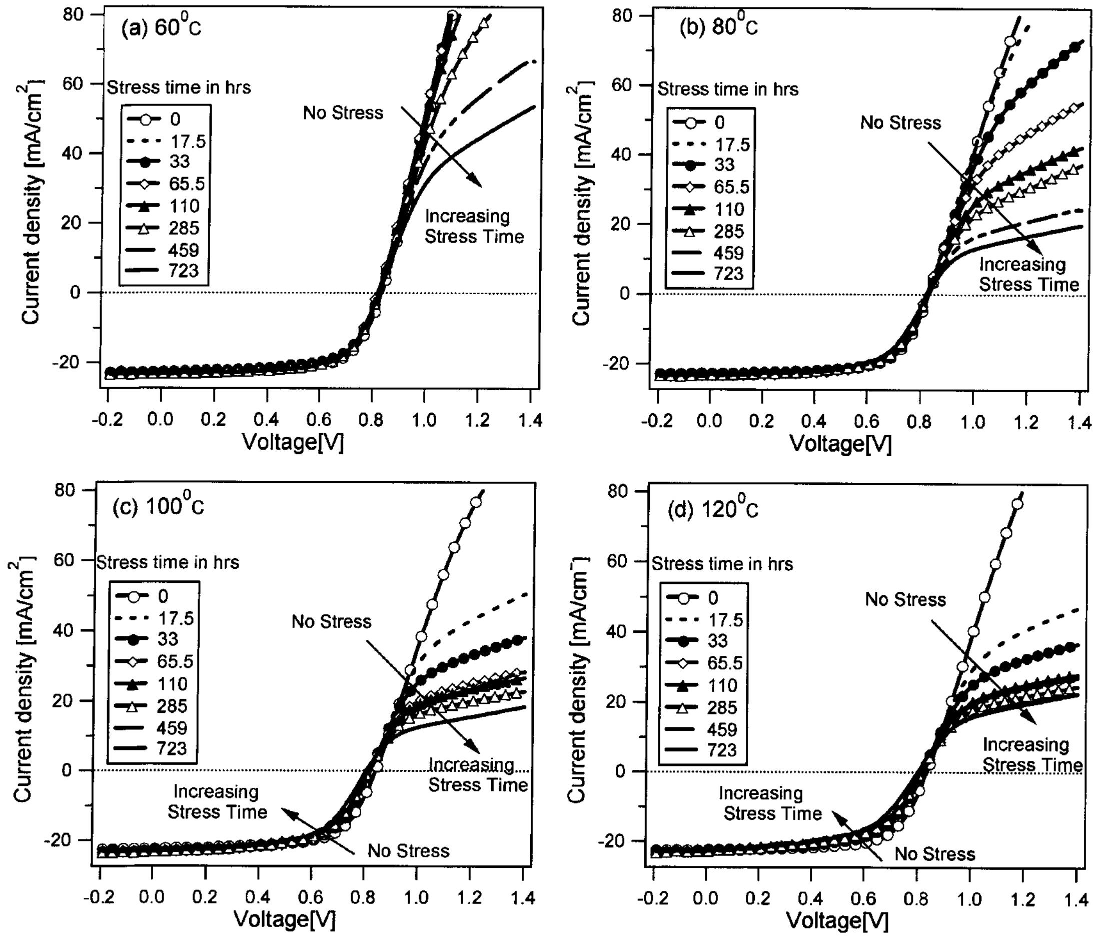

Figure 5.1: Evolution of JV curves with stress time as a function of stress temperature: (a) 60°C, (b) 80°C, (c) 100°C and (d) 120°C.

The changes in solar cell parameters with stress time for the devices stressed at different temperature are shown in figure 5.2. In addition to fill-factor, reduction in open-circuit voltage was found to be systematically dependent on the stress temperature: a V_{oc} drop of 30-40 mV is observed with devices stressed at higher temperature (100°C and 120°C), but very small changes with low temperature stress.

After 723 hrs of stress the hole densities estimated from C-V measurement did not

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

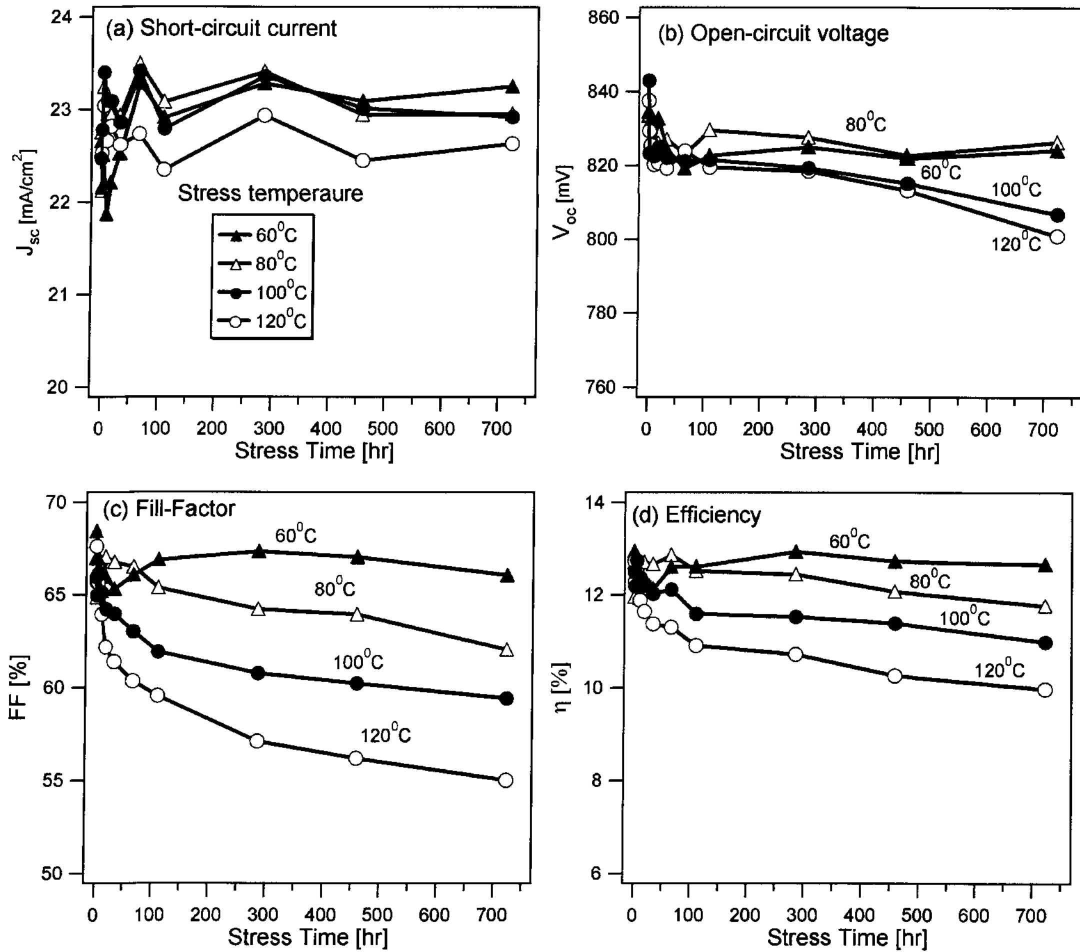

Figure 5.2: Changes in parameters with stress time as a function of the stress temperature: (a) J_{sc} (b) V_{oc} (c) FF and (d) efficiency.

show any significant dependence on stress temperature. However, TRPL measurement showed lower lifetime for the devices stressed at higher temperature. This suggests an increase of Cu-related recombination with increase in stress temperature, which lowers the lifetime, and hence reduces FF and V_{oc}. QE measurements have also confirmed a larger reduction in the infrared response with increased stress temperature.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

5.2 Degradation of devices made with and without Cu at the back–contact

In chapter 4, it was shown that the back-contact barrier is minimized, the open–circuit voltage is increased, and the performance of CdS/CdTe devices is improved with a modest amount of Cu at the back-contact layer. However, elevated-temperature enhanced diffusion of Cu from the back contact region toward the CdS/CdTe junction during accelerated life tests appears to be responsible for both back-contact degradation and decreased voltage due to increased recombination. In general, the Cu-diffusion is greater in forward bias where there is less junction field to oppose diffusion of positive ions into the junction region [55].

The Cu-diffusion effect was studied here by investigating the stability of four sets of devices made with and without Cu, and with and without $CdCl_2$ treatment. Otherwise, all devices were processed and stressed identically. Two samples were used for each of the four conditions. All were subjected to 100°C, open-circuit voltage bias, and one-sun illumination for just over 600 hrs. The J-V curves of the devices before and after 602 hrs of stress are shown in figure 5.3, the absolute changes of the parameters from the initial values are also shown in the insets. The largest degradation was observed with the device that contains Cu, and that was $CdCl_2$ treated. This suggests the diffusion of Cu is somewhat enhanced by the $CdCl_2$ treatment. The devices that has Cu, but was not $CdCl_2$ treated, were relatively stable.

Though Cu inclusion at the back contact layer insures a non–rectifying contact, its use has been also linked to stability problems in CdTe solar cells. The apparent problem is double edged: (1) Cu diffuses away from the back contact, leaving behind a Cu-depleted

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

rectifying back contact and (2) Cu diffuses toward the CdS/CdTe main junction and forms Cu-related recombination centers that reduce V_{oc} and FF.

The J-V curves in figure 5.3 show that the impact of Cu on the stability of the devices is affected by whether the device was $CdCl_2$ treated.

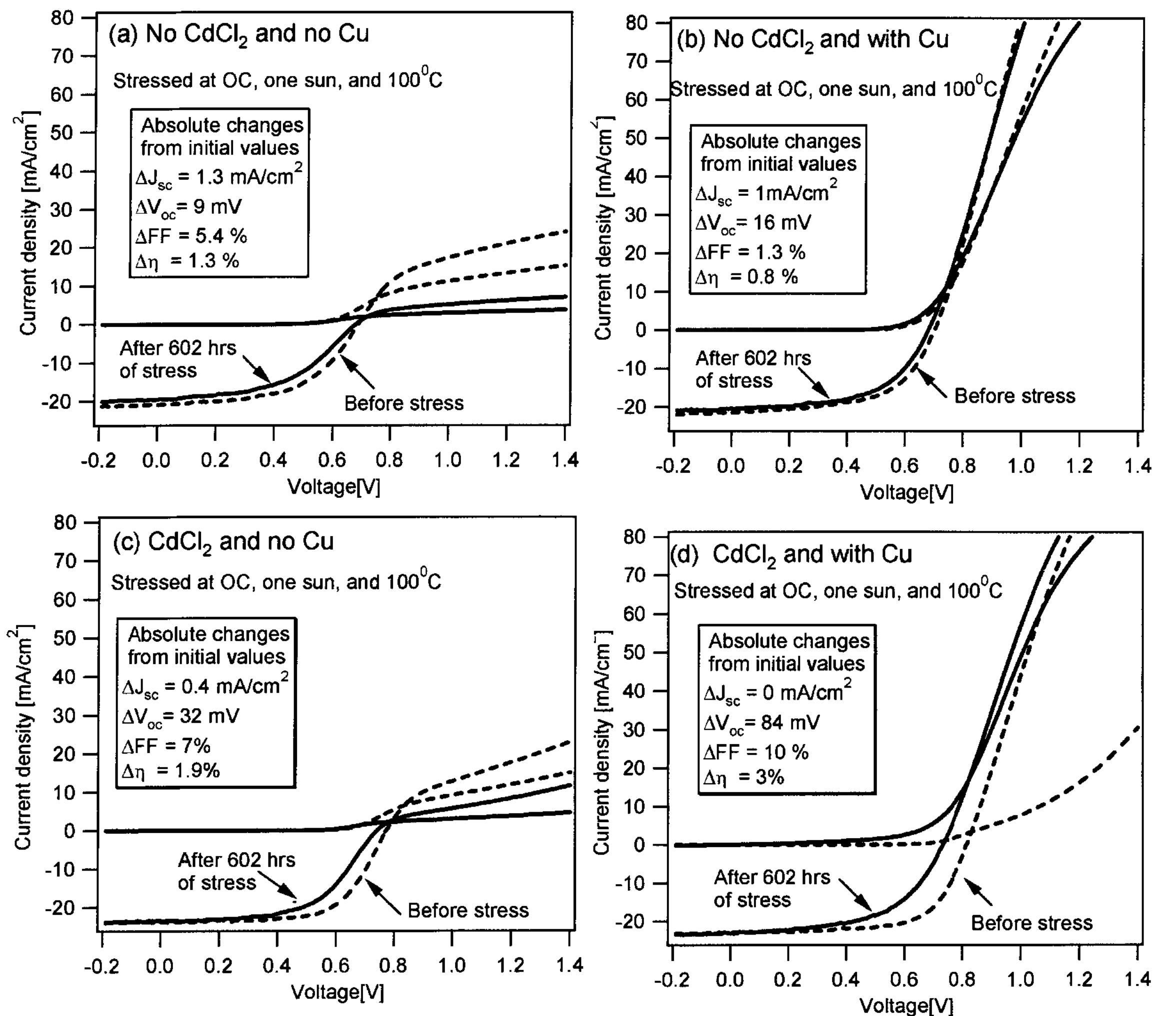

Figure 5.3: The current-voltage curves before and after stress of devices made with and without Cu, with and without $CdCl_2$ treatment.

It is well known that $CdCl_2$ treatment is a vital step in achieving high-performance devices, however devices without $CdCl_2$ treatment were relatively stable when compared to the $CdCl_2$ treated devices, this is likely due to the fact that the $CdCl_2$ treatment is

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

providing a diffusion path for Cu, hence more Cu diffusion in the $CdCl_2$ treated devices. Although this may require further investigation, it provides some insight to the correlation between $CdCl_2$ treatment and Cu diffusion.

5.3 Influence of a graphite layer at the CdTe/ back-contact interface on stability

Role of graphite layer

The role of graphite in a $Cu_{1.4}Te$ + HgTe doped graphite paste contact on solar cell stability was studied by completing devices with and without such a layer between the CdTe and the metallization. The primary goal was to investigate diffusion of Cu and other metals from the back contact region, and the possible role played by the graphite in slowing such diffusion.

The $Cu_{1.4}Te$ + HgTe doped graphite layer was applied to a set of cells, these devices were then divided into two groups. In one group, the graphite paste was intentionally removed by ultrasonic rinsing in methylethylketone (MEK) while in the remaining group, the graphite layer was left intact. Each group was further subdivided in half to be coated with either a silver- or a nickel-impregnated paint to serve as the back metallization. Finally, all devices were placed in an oven and air-annealed at 100°C for one hour to cure the paste. This procedure resulted in four sets of devices, two devices per set. The structures will be referred to as: (1) graphite/Ag, (2) graphite/Ni, (3) Ag-only, and (4) Ni-only contacts. It should be noted that all devices initially had the same Cu-doped, Te-rich interface between the CdTe and the back contact structure.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Device characterization was performed immediately after fabrication and at various time intervals during the subsequent elevated-temperature stress tests performed under one sun illumination, 100°C, and open-circuit bias conditions. Current-voltage (J-V) measurements on stressed devices were performed after 12-24 hours of dark storage at 25°C to minimize any storage-state transients.

JV measurement

The measured J-V characteristics of four representative devices using each contact structure, before and after 707 hours of elevated-temperature stress, are shown in figure 5.4.

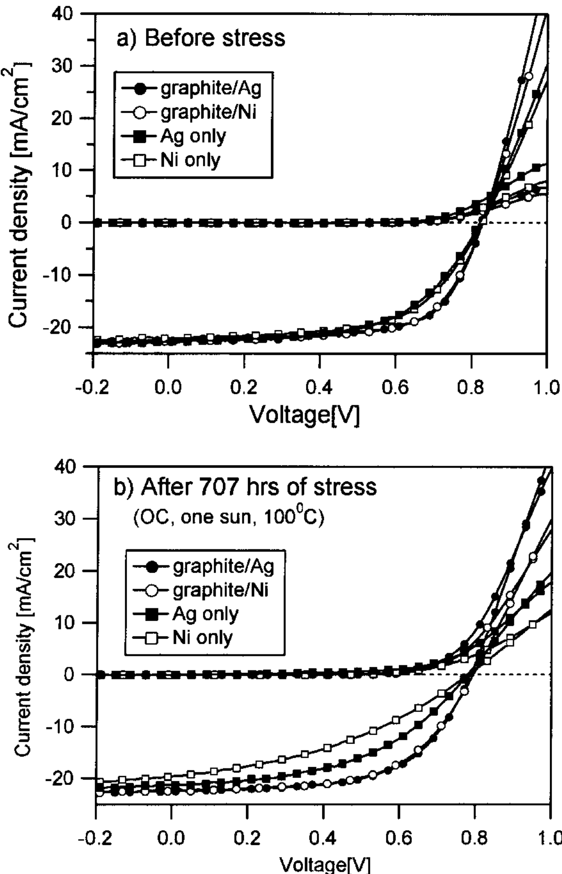

Figure 5.4: J-V curve (a) before stress and (b) after stress.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Initially all devices had similar open-circuit voltage (V_{oc}) and short-circuit current density (J_{sc}), but the fill-factors (FF) of devices made with the graphite layer removed were somewhat smaller (due to higher series resistance) than those made with the graphite layer intact.

After 707 hrs of stress, devices with graphite/Ag and graphite/Ni back contacts showed modest degradation, but more significant degradation was observed in devices made with the graphite layer removed. The Ni-only back contact device showed the most degradation. In this case, degradation resulted primarily from a reduction in FF, due to a large increase in series resistance. The changes in FF, V_{oc}, J_{sc} and efficiency (η) of the representative devices shown as a function of the stress time are shown in figure 5.5.

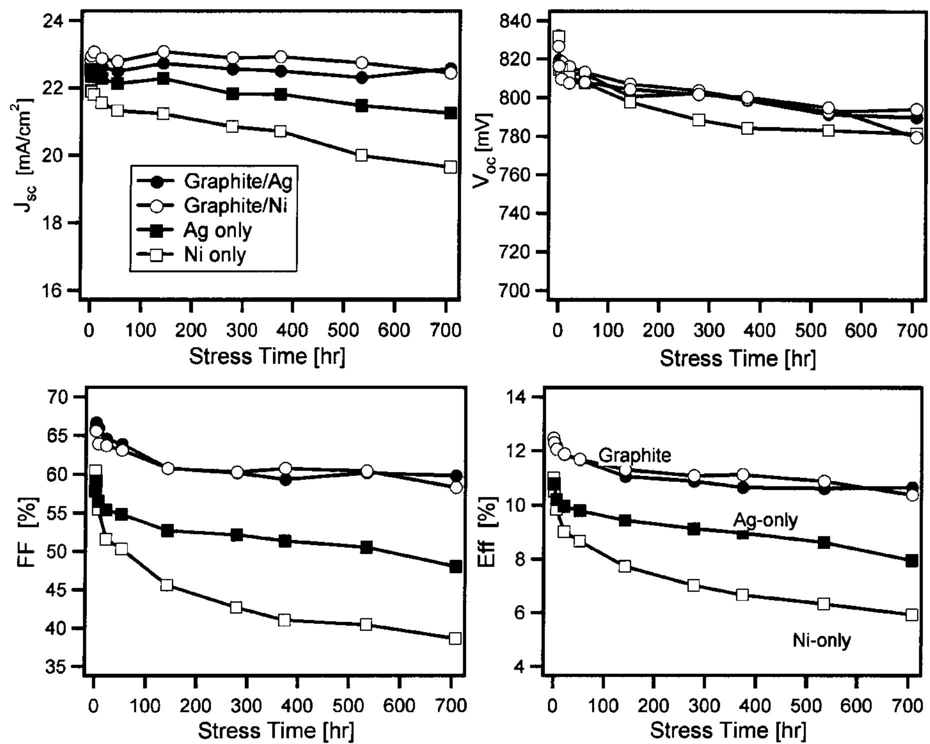

Figure 5.5: Performance parameters as a function of stress time.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Capacitance Voltage Characteristics

C-V measurements and the resulting carrier density profiles before and after 707 hours of stress are shown in figure 5.6. Of the four different contact structures studied, all behave similarly except the Ag-only case. It is also apparent that the zero-bias depletion width of all devices except the Ag-only case increases with stress. At the same time, the Ag-only device net carrier density estimated from the C-V measurement is approximately twice as large as the remaining devices both before and after stress. Since Ag is known as a fast diffuser and dopant in p-CdTe [56], the above C-V data suggests that Ag may be contributing as a dopant (in addition to Cu) in the Ag-only devices. The decreased carrier density after stress observed primarily in the graphite/Ag, graphite/Ni, and Ni-only devices is commonly observed in CdTe devices that use Cu-based back contacts. Such an effect has been attributed to Cu diffusion. The reason for the absence of this behavior in the Ag-only device may be related to the magnitude of dopant source available for indiffusion from the contact structure. All devices in this study have a common characteristic Te-rich interlayer between the CdTe and back contact layers. This interlayer effectively "getters" Cu from the graphite paste mixture during the 280^0 C paste anneal [57, 58] and serves as a source of Cu during subsequent stress. This outdiffusion of Cu is present in all devices. In the Ag-only case however, this finite (200-300 nm) Cu source outdiffusion is augmented by a much larger source of Ag in the form of a very thick (50-100 μm), Ag-conatining paste layer. This constant replenishment of Ag into the device is likely responsible for the considerably smaller decrease in carrier density observed with stress in the Ag-only case.

The C-V profiles of no-Cu devices (figure 4.10) and stressed-devices with Cu (figure

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

5.6) have a somewhat similar trends. This is an additional evidence that Cu diffuses from the back-contact during stress.

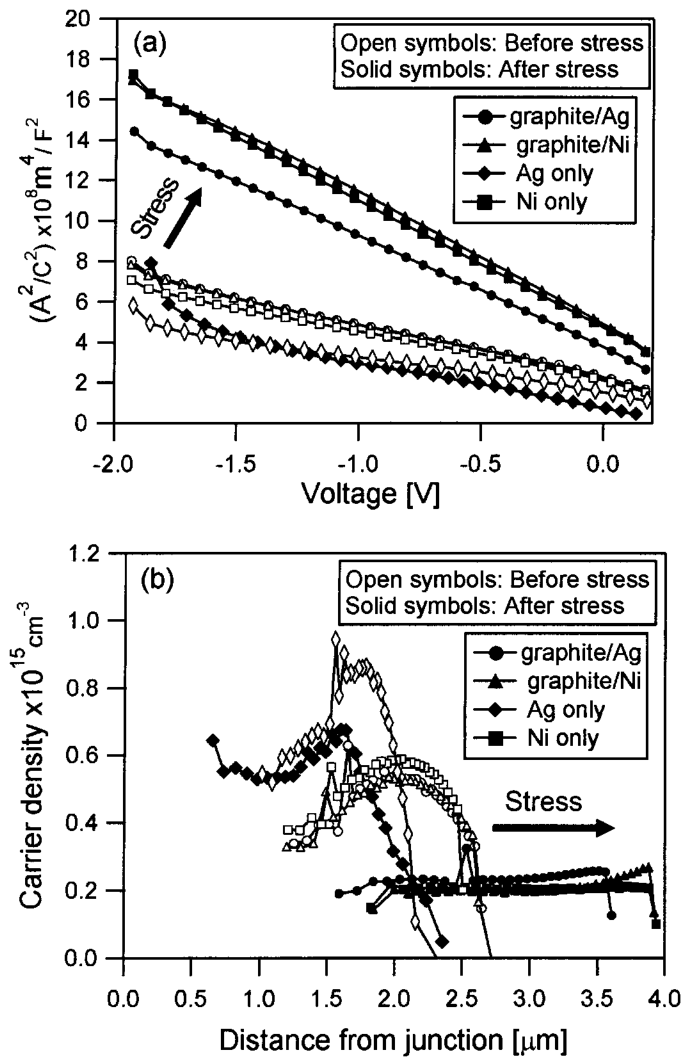

Figure 5.6: (a) capacitance versus voltage measurements and (b) carrier density as function of depletion width for devices before and after 707 hours of stress.

LBIC

LBIC measurements were performed at zero bias by scanning a 100-μm spot-size laser beam at 638 nm (well above the CdTe band gap) over the device area through the glass substrate. The histogram data presented in figure 5.7 shows the statistical distributions

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

of measured apparent quantum efficiency (AQE) values obtained during a complete scan before and after 707 hours of stress. All devices had full-width half-maximum (FWHM) uniformity of $< 1\%$ variation in AQE before stress. The measurements after stress showed little change in this value for devices which used a graphite layer, but an increase to 2% and 6% variation for the Ni-only and Ag-only devices respectively.

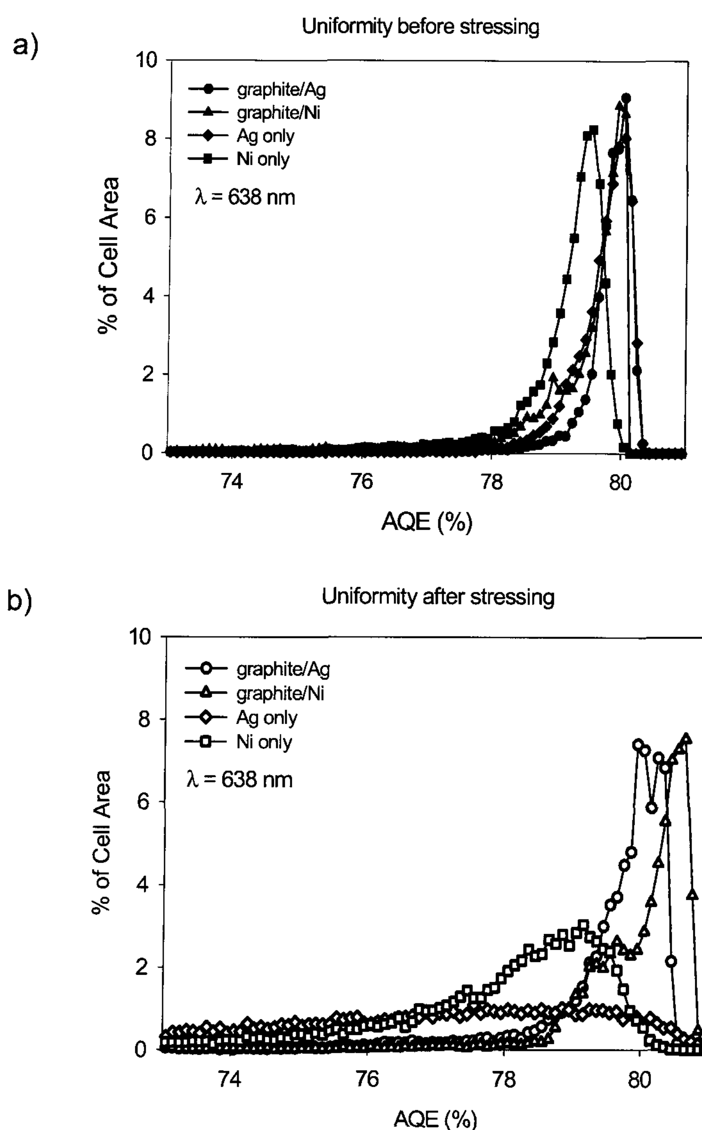

Figure 5.7: The statistical distribution of absolute quantum efficiencies measured across devices, a) before and b) after 707 hours of stress, using a 100 μm sampling beam. Peak width correlates with non-uniform behavior.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

The increase in FWHM observed in the Ni-only and Ag-only devices effectively reflects the greater formation of micro-non-uniformities in these devices with stress relative to devices that use the graphite paste structure. Reasons for poorer collection of generated carriers may be explained by ohmic micro-shunts or possibly by increased recombination due to larger defect concentrations in the CdTe and CdS layers. These effects likely have resulted from the increased probability of metal diffusion into the absorber material in the absence of the graphite layer.

Graphite as a diffusion barrier

The J-V, capacitance, and LBIC data all strongly suggest that the layer acts as a diffusion barrier to metals that might otherwise diffuse into the CdTe from the back contact. Hence, devices with the graphite layer had much better stability relative to the devices without the graphite layer. The graphite paste used to make the devices contains a polyacrylic-acid (PAA) polymer that constitutes nearly 70% by weight of the graphite paste once it is dried. The ability of the PAA to bind metal cations is the likely underlying reason why the graphite paste behaves like a diffusion barrier.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Chapter 6

Conclusions

The use of Cu to form the back-contact to CdTe solar cell absorbers avoids, or at least mitigates the current limitation, rollover, and/or distortion in the current-voltage characteristic, which is a signature of a rectifying contacts with barrier heights above 0.5 eV. With the application of a small amount of Cu (5-nm) at the CdTe back-contact layer higher FF is achieved, and moreover, the open-circuit voltage is improved. The application of a small amount of Cu on the Te-rich CdTe surface, followed by an appropriate anneal, resulted in a quasi ohmic-contact with significantly lowered the barrier height. The absence of observable rollover or other distortion implied the back barrier height was smaller than 0.4 eV. This barrier is sufficiently small that its impact on the current transport is not significant at room temperature. Hence, the fill-factor and efficiency were significantly improved with the inclusion of Cu.

When Cu was incorporated at the back-contact, however, it was found to diffuse into the CdTe and the main junction. Secondary-ion-mass-spectroscopy (SIMS) analysis clearly showed the presence of a significant amount of Cu in both the CdTe and CdS

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

layers. With the application of small amount of Cu (5-20 nm) the hole density increased, as a result higher V_{oc} is observed. However, with excess Cu (100 nm), the depletion width was significantly reduced, and thus the collection of photo-generated carriers was reduced, resulting in lower FF and V_{oc}. TRPL and DLCP measurements suggested an increase of Cu-related recombination in the CdTe when excess Cu is used, which corroborates the observed reduction in performance with excess Cu.

The presence of Cu in the CdS layer, when 5-100 nm of Cu was deposited at the back-contact, has minimal effect on the actual device performance. Cu in the CdS, however, formed compensating defect levels that were found to be responsible for anomalies such as dark/light crossover and apparent quantum efficiency. These anomalies can be used to study whether significant Cu diffuses from the back-contact toward the main junction. When excess Cu (170 nm) was used, the device was severely shunted, and a clear signature of the shunt was observed in LBIC and IR (infrared) images. In general, both beneficial and deleterious effects of Cu to the performance of the devices were identified.

The behavior of the back-contact was found to strongly depend on multiple factors: back-contact surface preparation, Cu amounts, annealing temperature, and the current-carrying electrode that was applied following the annealing of the Cu-layer. Devices made with 5 nm-Cu, annealed at 200°C, have resulted in good back-contact behavior and overall device performance. However, reduced performance was achieved when annealed at 280°C due to enhanced Cu-diffusion. The performance of the devices that were annealed at lower temperate is comparable to devices made with the standard Cu-doped graphite paste contacts when the same absorber is used.

Numerous metals: Au, Cr, Pd, Pt, and Ni were found to form good current-carrying electrodes. Ag and Al, however, did not perform well. Devices made with the Al-electrode

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

had reasonable V_{oc} but significantly low fill-factor most likely due to the formation of a resistive layer of Al_2Te_3 at the back-contact electrode. In contrast, devices made with Ag-electrode have lower V_{oc}. Moreover, non-uniformity on a mm scale was observed, which is likely related to diffusion of Ag toward the CdTe layer.

With exposure to elevated temperature (60–120°C) for extended period of time (700 hrs), diffusion of Cu from the back contact was found to cause back-contact degradation and increased CdTe recombination. This degradation resulted in a reduced fill-factor due to the formation of a Cu-depleted blocking contact and a reduced collection efficiency. The increase of degradation with increase in stress temperature indicated that the diffusion of Cu is enhanced by higher temperature.

FUTURE WORK:

In this work, with the application of small amount of evaporated Cu (5-nm), annealed at 200°C, and with ~0.5 μm of evaporated metals (Au, Pd, Ni or Pt) as electrodes, devices with reasonably good initial performance have been demonstrated. Furthermore, no dark/light crossover trend was observed, which suggests that the amount of Cu reaching the CdS layer is minimized by lowering the anneal temperature. This is an indication that during long-term stability study (stress), the diffusion of Cu in these devices might also be low, which would hopefully result in a better stability. This reasonably educated speculation should be experimentally verified. In light of this, at NREL, similar devices using this back-contact recipe have already been fabricated, and the reproducibility was quite good, these devices will be exposed to stress conditions, in the near future, to test their stability .

The CdTe thicknesses of the devices studied were ~9 μm, which is common for NREL devices, and very recently, in a separate project from this thesis work, devices

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

with relatively thinner CdTe ($\sim 2\mu$m) with respectable efficiencies were fabricated, using the Cu-doped graphite paste back-contact. In the future, similar devices with this relatively thinner CdTe and that incorporate evaporated-Cu and metal electrodes are under consideration. This back-contact approach that consists of evaporated-Cu and evaporated-metal electrodes, is easily controllable, and scalable to industrial size, and in combination with a thin-CdTe layer will result in significant contribution in lowering the cost of commercialized CdTe solar cells.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

Bibliography

[1] D. Chapin, C. Fuller, and G. Pearson, J. Appl. Phys. **25**, 676 (1954).

[2] K. Zweibel, The Terawatt Challenge for Thin–film PV: A Technical Report, 2005.

[3] N. Lewis, A Global Energy Perspective. http://www.its.caltech.edu/mmrc/nsl/energy.html. (2004).

[4] M. Green, Solar Cells, 1986.

[5] V. Lyahovitskaya, L. Chernyak, J. Greenberg, L. Kaplan, and D. Cahen, J. Cryst. Growth, **214/215**, 1155 (2000).

[6] X. Wu et al., in *Proc. 17th European Photovoltaic Sol. Energy Conf.*, pages 995–1000, 2001.

[7] X. Liu, I. Eisgruber, and J. Sites, in *Proc. 23th IEEE Photovoltaic Specialist Conf.*, pages 405–408, 1993.

[8] S. Demtsu and J. Sites, in *Proc. 30th IEEE Photovoltaic Specialist Conf.*, pages 744–747, 2005.

[9] A. Abken, C. Hambro, P. Meyers, R. Powel, and S. Zafar, NCPV and Solar Program Review Meeting , 39 (2003).

[10] K. Barth, R. Enzenroth, and S. Sampath, in *Proc. 29th IEEE Photovoltaic Specialist Conf.*, pages 551–554, 2002.

[11] C. Ferekides, J. Britt, and Y. Ma, in *Proc. 23th IEEE Photovoltaic Specialist Conf.*, pages 389–393, 1993.

[12] S. S. Hegedus and W. N. Shafarman, Prog. Photovoltaics **12**, 155 (2004).

[13] J. R. Sites and P. H. Mauk, Solar Cells **27**, 411 (1989).

[14] T. Humphreys, M. Patterson, and R. Willimas, J. Vac. Sci. Technol. **17**, 886 (1980).

[15] J. Werthen, J. Haring, A. Fahrenbruch, and R. Bube, J. Phys. D: Appl. Phys. **16**, 2391 (1983).

[16] D. Friedman, I. Lindau, and W. Spicer, Phys. Rev. B **37**, 731 (1987).

[17] Y. Bilevych, A. Sukach, and V. Tetyorkin, phys. stat. sol. c **1**, 317 (2004).

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

[18] T. Chu, S. Chu, and S. Ang, J. Appl. Phys. **58**, 4296 (1985).

[19] H. Toyoma et al., Jpn. J. Appl. Phys. **43**, 6371 (2004).

[20] M. Hernandez et al., phys. stat. sol. b **220**, 209 (2000).

[21] A. Fahrenbruch, Solar Cells **21**, 399 (1987).

[22] H. Uda, S. Ikegami, and H. Sonomura, Sol. Energy Mat. Sol. Cells **35**, 293 (1994).

[23] B. McCandless, Y. Qu, and R. Birkmire, in *Proc. 1st World Conf. Photovoltaic Energy Conversion*, pages 107–110, 1998.

[24] J. Ponpon, Solid State Electron. **28**, 689 (1985).

[25] T. Chu, S. Chu, K. Han, and M. Mantavadi, in *Proc. 20th IEEE Photovoltaic Specialist Conf.*, pages 1422–1425, 1988.

[26] T. Gessert, A. Duda, S. Asher, C. Narayanswamy, and D. Rose, in *Proc. 28th IEEE Photovoltaic Specialist Conf.*, pages 654–657, 2000.

[27] N. Romeo, A. Bosio, and R. Tedeschi, in *Proc. 2nd World Conf. Photovoltaic Energy Conversion*, pages 446–447, 1998.

[28] G. Stollwerck and J. Sites, in *Proc. 13th European Photovoltaic Sol. Energy Conf.*, pages 2020–2023, 1995.

[29] A. Niemegeers and M. Burgelman, J. Appl. Phys. **81**, 2881 (1997).

[30] T. McMahon and A.Fahrenbruck, in *Proc. 28th IEEE Photovoltaic Specialist Conf.*, pages 539–542, 2000.

[31] P. Nollet, M. Burgelman, and S. Degrave, Thin Solid Films **361-362**, 293 (2000).

[32] B. McCandless, J. Phillips, and J. Titus, in *Proc. 2nd World Conf. Photovoltaic Energy Conversion*, pages 448–452, 1998.

[33] S. Demtsu and J. Sites, Thin Solid Films **510**, 320 (2006).

[34] D. H. Rose et al., Prog. Photovoltaics **7**, 331 (1997).

[35] D. Levi, D. S. Albin, and D. King, Prog. Photovoltaics **8**, 591 (2000).

[36] P. Mauk, H.Tavakolian, and J. Sites, in *IEEE Trans. Elect. Devices*, pages 422–427, 1990.

[37] J. Heath, J. Cohen, and W. Shafarman, J. Appl. Phys. **95**, 1000 (2004).

[38] W. K.Metzger, D. Albin, P. D. M. J. Romero, and M. Young, J. Appl. Phys. **99**, 103703 (2006).

[39] M.Gloeckler, A. Fahrenbrcuch, and J. Sites, in *Proc. 3rd World Conf. Photovoltaic Energy Conversion*, pages 491–494, 2003.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

[40] C. Ferekides, V. Viswanathan, and D. Morel, in *Proc. 26th IEEE Photovoltaic Specialist Conf.*, pages 423–426, 1997.

[41] A. K. Wahi, G. P. Caret, T. T. Chiang, I. Lindau, and W. E. Spicer, J. Vac. Sci. Technol. **A7**, 494 (1989).

[42] X. Wu et al., Thin Solid Films , in press (2006).

[43] K. Dobson, I. Visoly-Fisher, G. Hodes, and D. Cahen, Sol. Energy Mat. Sol. Cells **62**, 295 (2000).

[44] H. Chou, A. Rohatgi, E. Thomas, S. Kamara, and A. Bhat, J.Electrochem. Soc. **142**, 254 (1995).

[45] J. Chamonal, E. Molva, and L. Pautrat, Solid State Commun. **43**, 801 (1982).

[46] J. Laurenti, M. R. G. Bastide, and R. Triboulet, Solid State Commun. **67**, 1127 (1988).

[47] B. Monemar, E.Molva, and L. Dang, Phys. Rev. B **33**, 1134 (1986).

[48] J. F. Hiltner, PhD thesis, Colorado State University, 2001.

[49] P. Peka and H. Schulz, Solid State Commun. **89**, 225 (1994).

[50] I. L. Eisgruber, J. E. Granata, J. R. Sites, J. Hou, and J. Kessler, Sol. Energy Mat. Sol. Cells **53**, 367 (1998).

[51] S. Hegedus, D. Ryan, K. Dobson, B. McCandless, and D. Desai, Mat. Res. Soc. Symp. Proc. **763**, 447 (2003).

[52] M. Gloeckler and J. R. Sites, J. Appl. Phys. **95**, 4438 (2004).

[53] G. Agostinelli, D. L. Bätzner, and M. Burgelman, in *Proc. 29th IEEE Photovoltaic Specialist Conf.*, pages 744–747, 2002.

[54] W. Meeker and L. Escobar, Statistical Methods for Reliablity Data, 1998.

[55] J. F. Hiltner and J. R. Sites, in *AIP Conf. Proc.*, volume 462, pages 170–175, 1998.

[56] B. Warlick, C. Blanchard, and J. Barbot, in *Materials Science and Engineering*, pages 254–257, 2000.

[57] D. Albin, D. Levi, S. Asher, A. Balcioglu, and R. Dhere, in *Proc. 28th IEEE Photovoltaic Specialist Conf.*, pages 583–586, 2000.

[58] D. Albin et al., Mat. Res. Soc. Symp. Proc. **719**, 383 (2002).

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.