DISSERTATION

INVESTIGATION OF PROCESSING, MICROSTRUCTURES AND EFFICIENCIES OF POLYCRYSTALLINE CDTE PHOTOVOLTAIC FILMS AND DEVICES

Submitted by

Amit Harenkumar Munshi

Department of Mechanical Engineering

In partial fulfillment of the requirements

For the Degree of Doctor of Philosophy

Colorado State University

Fort Collins, Colorado

Spring 2017

Doctoral Committee:

Advisor: W.S. Sampath

James R. Sites
Susan P. James
Rick C. Powell
Troy B. Holland

ABSTRACT

INVESTIGATIONS OF PROCESSING, MICROSTRUCTURES AND EFFICIENCIES OF POLYCRYSTALLINE CDTE PHOTOVOLTAIC FILMS AND DEVICES

CdTe based photovoltaics have been commercialized at multiple GWs/year level. The performance of CdTe thin film photovoltaic devices is sensitive to process conditions. Variations in deposition temperatures as well as other treatment parameters have a significant impact on film microstructure and device performance. In this work, extensive investigations are carried out using advanced microstructural characterization techniques in an attempt to relate microstructural changes due to varying deposition parameters and their effects on device performance for cadmium telluride based photovoltaic cells deposited using close space sublimation (CSS).

The goal of this investigation is to apply advanced material characterization techniques to aid process development for higher efficiency CdTe based photovoltaic devices. Several techniques have been used to observe the morphological changes to the microstructure along with materials and crystallographic changes as a function of deposition temperature and treatment times. Traditional device structures as well as advanced structures with electron reflector and films deposited on $Mg_{1-x}Zn_xO$ instead of conventional CdS window layer are investigated. These techniques include Scanning Electron Microscopy (SEM) with Electron Back Scattered Diffraction (EBSD) and Energy dispersive X-ray spectroscopy (EDS) to study grain structure and High Resolution Transmission Electron Microscopy (TEM) with electron diffraction and EDS. These investigations have provided insights into the mechanisms that lead to change in film structure and device performance with change in deposition conditions. Energy dispersive X-ray spectroscopy (EDS) is used for chemical mapping of the films as well as to understand interlayer material diffusion between subsequent layers. Electrical performance of these devices has been studied using current density vs voltage plots. Devices with efficiency over 18% have been fabricated on low cost

commercial glass substrates with processes suitable for mass production. These are the highest efficiencies reported by any university or national laboratory for polycrystalline thin-film CdTe photovoltaics bettered only by researchers at First Solar Inc.

Processing experiments are traditionally designed based on simulation results however in these study microscopic materials characterization has been used as the primary driving force to understand the effects of processing conditions. Every structure and efficiency reported in this study has been extensively studied using microscopic imaging and materials characterization and processing conditions accordingly altered to achieve higher efficiencies. Understanding $CdCl_2$ passivation treatment out of this has been critical to this process. Several observations with regard to effect of $CdCl_2$ passivation have allowed the use to this treatment to achieve optimum performance. The effects of deposition temperature are also studied in rigorous details. All of these studies have played an important role in optimization of process that lead to high efficiency thin-film CdTe photovoltaic devices.

An effort is made in this study to better understand and establish a 3-way relationship between processing conditions, film microstructure and device efficiency for sublimated thin-film CdTe photovoltaics. Some crucial findings include impact of grain size on efficiency of photovoltaic devices and improvement in fill-factor resulting from use of thicker CdTe absorber with larger grain size. An attempt is also made to understand the microstructure as the device efficiency improves from ~1% efficiency to over 18% efficiency.

ACKNOWLEDGEMENTS

After God Almighty, I would like to take this opportunity to thank my advisor, Professor W.S. Sampath, for his guidance and patience. I would also like to express my gratitude towards my committee members, Professor Susan James, Professor James Sites, Prof. Troy Holland and Dr. Rick Powell, for their time and commitment. I would like to thank the funding organization NSF I/UCRC (Industry & University Cooperative Research Program) for funding this study.

I highly appreciate my colleagues, Jason Kephart, Drew Swanson, Tushar Shimpi, Jennifer Drayton and Davis Hemenway for their help and support. My special thanks to Kurt Barth and Kevan Cameron for their kind support at all important junctures. I would also like to thank John Raguse and Russell Geisthardt for their help with EL measurements. I am also thankful to our undergraduate staff for their consistent help with lab maintenance and sample preparation as well as electrical characterization.

I cannot thank enough Dr. John Walls, Dr. Geoff West and Dr. Piotr Kaminski at Loughborough University, UK for opening the doors of their laboratory and other facilities to allow me to perform advanced characterization of specimen samples. Some of the figures (~40%) presented in this manuscript were obtained by Dr. Ali Abbas and are being presented to ensure completeness for study. He also provided extensive help and support with characterization as well as training me on various instruments including FIB dual beam and TEM for which I am extremely thankful to Dr. Ali Abbas.

Last but not the least; I am highly grateful to my friends and my entire family who inspired me throughout my academic career. My father Harenkumar Munshi and mother Bhargavi Munshi who was also my teacher at primary school supported me during my worst academic crisis that allowed me to emerge as a student I am today. I cannot thank my brother Jay Munshi and sister Jigna Jariwala enough for his support and encouragement throughout my life. Also, I show my gratitude to my grandparents Late Shri Prafulchandra Joshi and Late Smt. Jayvidya Joshi, whose blessings and confidence in my ability played a crucial role in carving my career and life.

DEDICATION

I dedicate this work to billions of people around the world

that can benefit from affordable and sustainable green energy

that would lead them to better life

and access to sustainable food, energy and water

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1 INTRODUCTION

1.1 SOLAR ENERGY OVERVIEW

1.1.1 THE NEED FOR SUSTAINABLE CLEAN ENERGY. The global energy demand is currently estimated at about 16 terawatts and is expected to double over next 30 years[1]. Additionally, continued growth of developing countries will also increase the demand of energy required for industrial as well as domestic consumption. On the other hand the amount of energy consumed by humans over a year is approximately the same as the solar energy that reaches the earth in an hour[2]. For a developed country like U.S., photovoltaic (PV) installation on about 0.6% of the land could be enough to meet the entire country's electricity demand[3]. Figure 1.1 shows approximate area of land required to meet electricity and energy demand of U.S. if they were to be installed with photovoltaic fields. These approximations are based on estimates for 10% efficiency photovoltaic modules while currently 16% efficiency panels are being manufactured and installed. Photovoltaics thus can be seen as a green, abundant, renewable, safe and sustainable energy solution.

FIGURE 1.1 Approximate area of photovoltaic installation required to meet US energy demands

1.1.2 THE POTENTIAL OF CDTE PHOTOVOLTAICS. CdTe PV has demonstrated the lowest cost solar electricity generation, particularly for utility scale applications. CdTe is a p-type absorber that has a band gap of 1.45 eV which is nearly optimum for photovoltaic conversion. Approximately 2 µm is sufficient

to absorb most of the visible solar spectrum[4], [5]. Typical crystalline silicon PV requires 150-200 micron wafers. Moreover, silicon based photovoltaics require capital-intensive process. CdTe films are typically deposited on glass substrates using low cost hardware and high deposition rate processes

FIGURE 1.2 Examples of current CdTe field installations: A. 550 MW Topaz Solar Project, California B. 50 MW Macho Springs CdTe Solar Project, New Mexico C. 290 MW Agua Caliente CdTe Solar Power Plant, Arizona

reducing production costs. With commercial field installations exceeding 14 GW and production expected to increase two fold in next 2-3 years[6], polycrystalline CdTe photovoltaic technology poses as a viable alternative to fossil based fuels as well as other photovoltaic technologies such as c-silicon. CdTe photovoltaics have shown substantial improvement in device conversion efficiency over last decade. Figure 1.2 shows examples of some polycrystalline CdTe utility scale commercial photovoltaic installations. Thus, CdTe photovoltaics have been demonstrated as green, sustainable, renewable and affordable source of energy that is being scaled to create an energy solution. The current dominant technology for commercial photovoltaic application is Silicon. But silicon panels are more difficult and expensive to manufacture.

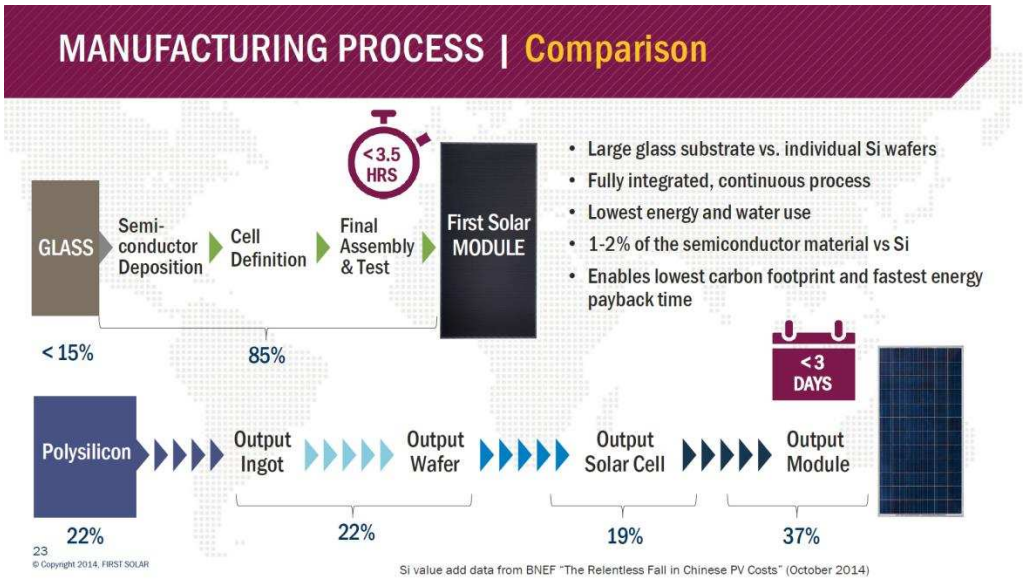


FIGURE 1.3 Comparison of CdTe manufacturing process with p-Si. Shows CdTe manufacturing to be simpler and faster.

1.1.3 CDTE PHOTOVOLTAICS: COST AND MARKET. The low cost manufacturing of thin film CdTe PV has enabled the signing of a record low cost power purchase agreement of ¢3.87/kWh for a 100 MW field[7], which is significantly lower than the average cost of electricity in the United States which is ¢11.0/kWh. With recent improvements, research scale small devices have recorded efficiencies of 22.1%[6] while modules with up to 18.6% efficiency have been produced[8]. The leading CdTe PV commercial manufacturer, First Solar Inc., has increased average production module efficiency from 13.5%[9] in the first quarter of 2014 to 16.2%[10] in the first quarter of 2016. Average levelized cost of energy from these First Solar installations are between ¢7/kWh and ¢15/kWh. Comparison of cost of electricity from polycrystalline CdTe PV to other established technologies in various countries is shown in figure 3. Moreover, First Solar Inc. became the first solar panel manufacturing company to lower its manufacturing cost to $1.00 per watt in 2009 and these prices were for panels produced at 14% efficiency at a reported cost of 59 cents per watt. In 2015, panels with up to 18.6% efficiency were produced and expected to further reduce the cost of these panels to less than 40 cents per watt[6]. Based on these developments it is clear that CdTe photovoltaics is now a mainstream energy solution at utility scale and

is growing at a rapid rate. Further improving the efficiency without substantial increase in production cost will further improve the energy cost structure for CdTe photovoltaics.

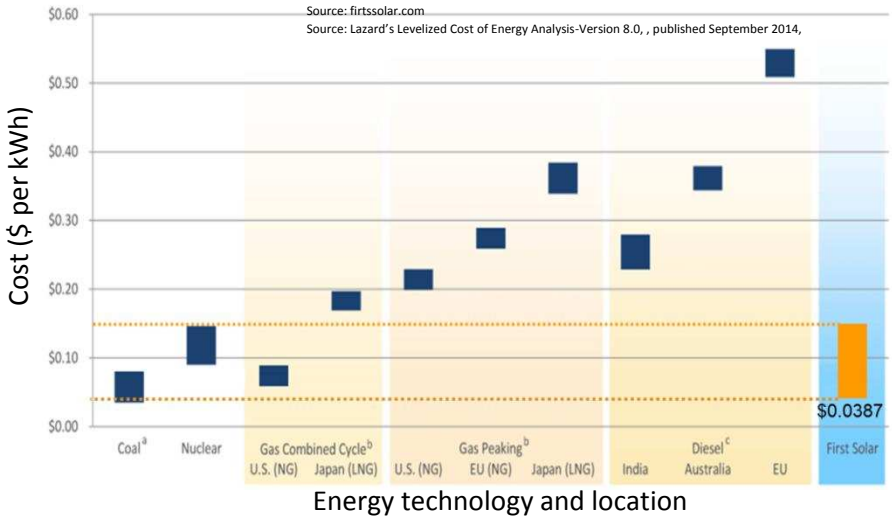


FIGURE 1.4 Commercial cost of CdTe PV installation (best case) compared to other energy technologies across the world

1.2 AVAILABILITY AND EXTRACTION OF CD AND TE

CdTe is manufactured from pure Cd and Te, both of which are byproducts of smelting prime metals such as Cu, Zn, Pb and Au. Both these materials are collected from secondary mineral streams and are not primarily mined for. Cd is collected during Zn and Pb smelting in from of dust and sludge. Te is a rare metal which similar to Cd is extracted as byproduct of processing Cu, Pb, Au and Bi ores. Metallurgical grade (99.99% pure) Cd and Te metal are used in most applications that are refined by leaching with sulfuric acid. Higher purity materials are achieved by electrolytic purification and subsequent melting and atomization or by vacuum distillation. These refining processes do not produce any atmospheric emissions of these respective materials and all waste is recycled[11]. Refined Cd and Te are used to synthesize CdTe for photovoltaic application. CdTe is produced from Cd and Te powder using proprietary methods. Reportedly, 100% of feedstock is used and there are no quantifiable emissions during CdTe synthesis[11]. Melting and atomization steps necessary to form the powder emit about 2% of the feedstock that is captured using HEPA filters that can be recycled[11].

1.3 LIFECYCLE ASSESSMENT AND ENVIRONMENTAL IMPACT

Allocation of emissions refers to the question of what portion of emissions is attributed to certain byproduct in a refining or manufacturing process. Since cadmium is a byproduct of zinc refining process allocation of emissions for cadmium is a fundamental question[12]. As per ISO (International Standard Organization) directives, in such situations where physical relationships alone cannot be established or used for basis for allocation, inputs should be allocated between products in proportion to the products' economic values. As per this method of allocation emissions from Cd is only 0.58% of total emission from refinement of Zn ore. Moreover, atmospheric Cd emissions from lifecycle of CdTe photovoltaics is estimated at 15.0 g Cd/ton Cd[11]. An important question to consider is what would happen to cadmium if it was not used. Cadmium is a group 1 carcinogen and the unabsorbed Cd generated by metal smelting process is stockpiled, cemented and buried or disposed of in landfills. Cutting down on refining of Zn and Pb to cut down on Cd production is not a viable alternative. Therefore, it is most desirable to use Cd in ways that prevent its flow into the environment. Use of Cd in CdTe based photovoltaics is one such application alongside Ni-Cd batteries. Use of Cd in CdTe photovoltaics is considered more environmentally friendly since CdTe is a more stable compound as compared to the other application where it is used as either Cd or $Cd(OH)_2$.

Tellurium is a rare metal that is most primarily achieved as a byproduct of Cu refining. During pyrometallurgical separation, air is bubbled through molten blister copper where Te gets separated as an oxide in form of slime. The slime is leached with caustic soda to form sodium telluride that is later refined using electrolysis to get metallurgy grade Te that can be used for CdTe photovoltaics after further refinement[11]. Estimates of Te availability for photovoltaic application after subtracting competitive uses show that the total annual CdTe photovoltaic production that can be supported by Te availability through primary refining and secondary recycling is estimated at 98-205 GW by 2020 and rising to 0.6-2.7 TW by 2050[13]. In addition, new sources of Te are being discovered such as in China and Mexico where direct mining of Te is economically feasible[13]. Earlier Te availability was considered to be a

limiting factor in large scale manufacturing of CdTe photovoltaics. Moreover, in recent years with discovery of new sources and improvement in recycling technology, Te production is expected to conveniently support extensive industrial production of CdTe for photovoltaic application.

1.4 PRODUCTION SUSTAINABILITY AND COST

In 2009, optimistic assumptions suggested that CdTe thin film photovoltaics would be able to achieve 14% conversion efficiency by the year 2020[13]. However, surpassing these estimates by far in 2015 the conversion efficiency of CdTe thin film photovoltaics of 21.5% has already been demonstrated[14]. CdTe has been also demonstrated as a commercially viable alternative to not only Si based photovoltaics but also fossil fuels based conventional electricity generation. While the average electricity cost to consumer in US is estimated at US10.22 cents/kWh[15], leading CdTe photovoltaics manufacturer First Solar Inc. in 2015 finalized a power purchase agreement with a US based utility company, Berkshire Hathaway Energy, for a 100 MW installation at $0.0387 per kWh[16]. This is not only the lowest rate photovoltaic electricity but probably the cheapest electricity available in USA. Average levelized cost of energy from these First Solar Inc. installations are between 7 cents to 15 cents per kWh. Moreover, First Solar Inc. became the first solar panel manufacturing company to lower its manufacturing cost to $1.00 per watt in 2009 and these prices were for panels produced at 14% efficiency at a reported cost of 59 cents per watt[17]. In 2015, commercial panels with upto 18.6% [8]efficiency are produced that are expected to further reduce the cost of these panels to less than 40 cents per watt[18]. With lower production costs and higher efficiencies CdTe thin film photovoltaics is proving to be a sustainable and cost effective means of energy generation and provides a substantial advantage in the competitive energy market.

1.5 ENVIRONMENTAL IMPACT

The positive impact of CdTe photovoltaics is not restricted to only cost and sustainability. It is also been rated as the most eco-efficient solar technology in the industry that produce more energy, at a lower cost with the smallest life cycle impacts. CdTe has the smallest carbon footprint of 18 gCO2-

eq/kWh, fastest payback time of under 1 year and lowest water input per unit of 0.27 kg/kWh which gives it an edge over not only other competitive solar technologies such as Si based photovoltaics but also all other conventional energy sources[12]. CdTe photovoltaics also have the lowest gross energy requirement among all photovoltaic systems of about 7.6E+3 MJ/kW with the closest competitor technology requiring nearly 2 times the energy[12]. Furthermore, large scale uses of CdTe photovoltaics present minimal risks to health and the environment[12]. Currently nearly 10 GW of CdTe photovoltaics are installed globally which every minute displace nearly 10 metric tons of CO_2 emission, the equivalent of removing two cars off the road[19]. From safety perspective, CdTe modules are proved to present a competitive advantage over all other mainstream photovoltaic technologies with resistance to chemical, environmental and operational impacts[12], [19]. In addition to all the advantages mentioned, this technology also provides employment to over 40,000 individuals globally[19].

1.6 $CdCl_2$ PASSIVATION TREATMENT AND HIGH TEMPERATURE CdTe DEPOSITION

1.6.1 INTRODUCTION TO $CdCl_2$ PASSIVATION.

An important process step in the fabrication of high efficiency CdTe photovoltaic devices is the cadmium chloride ($CdCl_2$) passivation treatment. This passivation treatment improves film microstructure and electrical characteristics of CdTe photovoltaic devices[20]. Cells made in our laboratory without $CdCl_2$ treatment exhibit about ~1% efficiency while passivation treatment improves the efficiency to over 13%[20]. An earlier study has shown that annealing treatment in absence of $CdCl_2$ reduces the density of stacking faults in CdTe grains. However, the treatment time and temperature without $CdCl_2$ does not have substantial effect on electrical performance and cell efficiency remains low[21]. Use of cadmium chloride has been known to remove the stacking faults. Studies carried out on our sublimated CdTe have also shown that the passivation process initiates preferentially at the CdTe/CdS interface[22].

This study focuses on improving the understanding of effects of $CdCl_2$ passivation treatment and deposition temperature on CdTe thin-film microstructure and electrical performance. Our baseline devices exhibit an efficiency of approximately 13%. These are 2.2 µm – 2.4 µm CdTe thin-films typically

sublimated under modest vacuum of 40 mTorr on a 120 nm – 130 nm CdS n-type window layer which is also deposited using sublimation process. These films are deposited on commercial soda-lime glass and following the deposition of CdS and CdTe films, $CdCl_2$ passivation treatment is performed followed by Cu doping of the back surface to form an ohmic contact. Higher CdTe deposition temperature for CdTe absorber showed some promise but the study was restricted due to resublimation of CdS during preheating of the substrate prior to CdTe deposition. Moreover, CdS is a strong absorber of light with energy above its band-gap of 2.4 eV. The light absorbed in this layer is wasted because carriers photogenerated in the CdS are not collected.

1.6.2 $Mg_xZn_{1-x}O$ INSTEAD OF CDS FOR HIGHER DEPOSITION TEMPERATURE. To overcome these limitations of using CdS *n*-type window[23], [24], various high resistance transparent (HRT) layers were investigated by Kephart *et al*. $Mg_xZn_{1-x}O$ gave the best performance and allowed complete elimination of CdS layer. $Mg_xZn_{1-x}O$ films (~100 nm thick) have high transmission thus significantly reducing absorption losses. In addition, $Mg_xZn_{1-x}O$ is very stable at elevated temperatures and thus allowed deposition of CdTe at much higher substrate temperatures[25]. This $Mg_xZn_{1-x}O$ layer was incorporated in this study to allow higher deposition temperatures. Additional incorporation of Te back contact layer and refined fabrication process led to some of the highest reported efficiencies for polycrystalline CdTe photovoltaic cells. A 18.3% device was certified by ILX Lightwave, Newport under this study[26][27]. Only First Solar Inc. has so far reported cells exceeding this efficiency using polycrystalline thin film CdTe.

1.6.3 OVERVIEW OF HIGH EFFICIENCY DEVICES AND CHARACTERIZATION. High efficiency performance results and characterization reported here are for sublimated CdTe films on radio-frequency (RF) sputter deposited $Mg_xZn_{1-x}O$ resistive buffer layer. The devices were fabricated with deposition processes that were high rate and similar to those used in manufacturing. These results were repeatable and the best performing device out of multiple fabricated devices with similar efficiency had been externally certified by ILX Lighwave, Newport to verify the internal measurements performed at Colorado State University.

Detailed materials characterization used to better understand the impact of process modification include transmission electron microscopy (TEM) and high resolution transmission electron microscopy (HRTEM) to understand film morphology, linear defects and grain structure. Material distribution within the film was studied using Energy dispersive X-ray spectroscopy (EDS) and X-ray diffraction (XRD) was used to understand the grain orientation and film texture. Electrical characterization was performed using current vs voltage (J-V) plot to measure open circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF) and external conversion efficiency (η).

CHAPTER 2 BASICS OF PHOTOVOLTAIC CELLS AND ELECTRICAL CHARACTERIZATION

2.1. THE P-N JUNCTION OF CDTE

2.1.1 THE SEMICONDUCTORS. Fundamentally a solar cell is a p-n junction that has two primary layers: a p-type and an n-type material. When these layers are exposed to light, a potential difference is created between the layers due to photoelectric effect. The voltage causes a direct-current electrical energy. This takes place when the material absorbs light that creates free charge career i.e. electrons which can perform work in an external circuit. To make a solar device three main parts must be satisfied:

a. A semiconductor which is sensitive to light

b. A p-n junction that creates an electron-hole pair

c. Electrical contacts on either side of the p-n junction to allow generated current to be used for performing work

Mostly light absorber is a semiconductor with a band gap between 1 and 1.5 eV. This range is considered optimum as higher band gap material would absorb less light while lower bandgap material would extract less energy from each photon due to reduced separation of valence and condition band that will lead to reduced conversion efficiency. Figure 2.1 shows band diagrams for p-type and n-type material with Fermi level (EF), valence band (VB) and conduction band (CD).

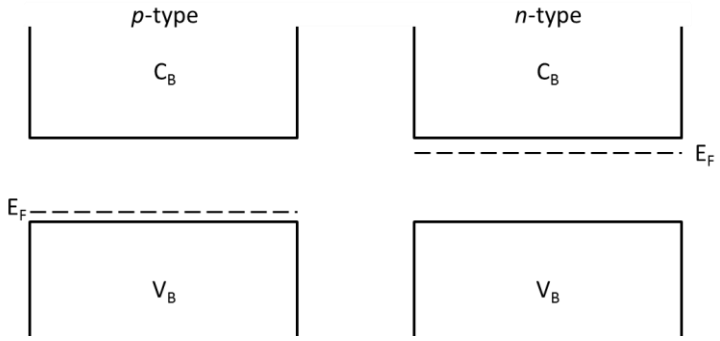


FIGURE 2.1 Schematic diagrams of band positions with reference to Fermi level for a p-type and an n-type semiconductor material

This suggests that if a p-type and an n-type material are bought in contact they would from a p-n junction. The electrons would move from n-type material to the p-type material and the holes would move in the opposite direction. The carriers diffuse from higher concentration to the lower until there is a depleted region created that is positive on the p-side due to high concentration of ions while negative on the n-type side as there is an equally high concentration of holes.

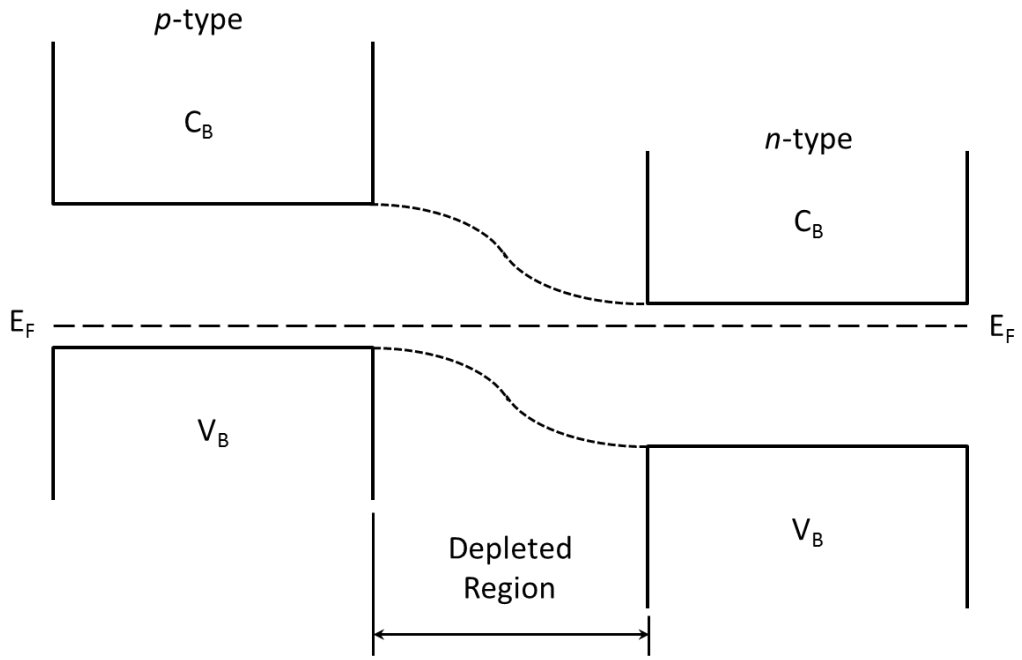


FIGURE 2.2 Schematic diagram showing p-n junction with depleted region and energy bands

2.1.2 PHOTOVOLTAIC DEVICE OPERATION. When the concentration of the electrons and holes has built up on either side of the junction the diffusion will stop and the gradient of carriers is balanced. This causes the Fermi levels in the p-type and n-type material to become equal and therefore the conduction and valence bands are forced to bend as shown in figure 2.2. Due to this build-up of charge on either side of the junction an electric field is formed which is critical for the photovoltaic effect.

CdS/CdTe forms a hetrojunction cell. This means that the p-type and the n-type materials are not the same merely distinguished by change in doping to create p-type and n-type. Due to this materials must be so selected that there is minimum lattice mismatch. In CdS/CdTe cells, CdS is an *n*-type material as it

has a wider band gap that allows larger current generation from higher energy electromagnetic waves or photons.

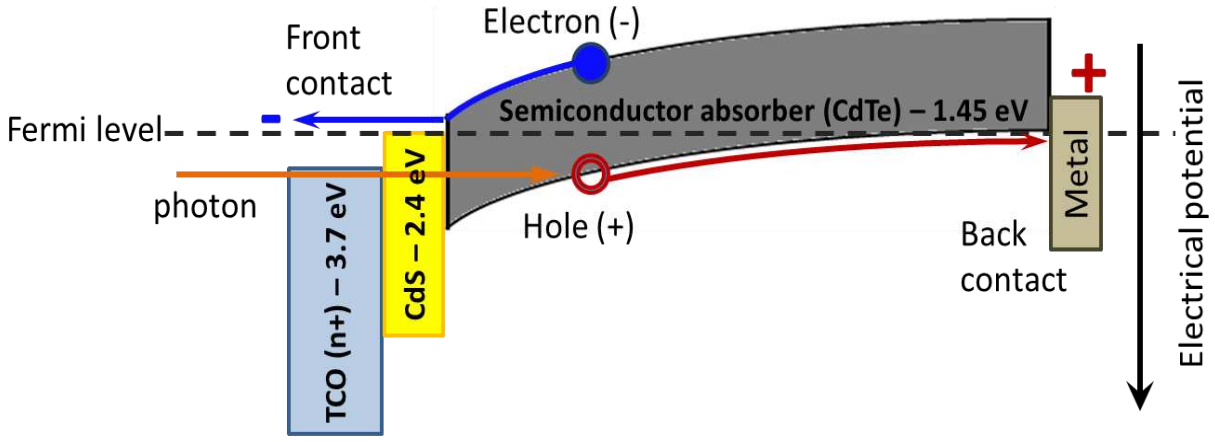


FIGURE 2.3 Schematic diagram showing band diagram energies of a cadmium Sulphide/cadmium telluride cell.

As mentioned earlier, electricity is generated due to photoelectric effect. The electromagnetic radiation is absorbed by the semiconductor material to create electron-hole pair, which are charge carriers. Then these electron-hole pairs are separated at the junction followed by migration of charge carriers to a

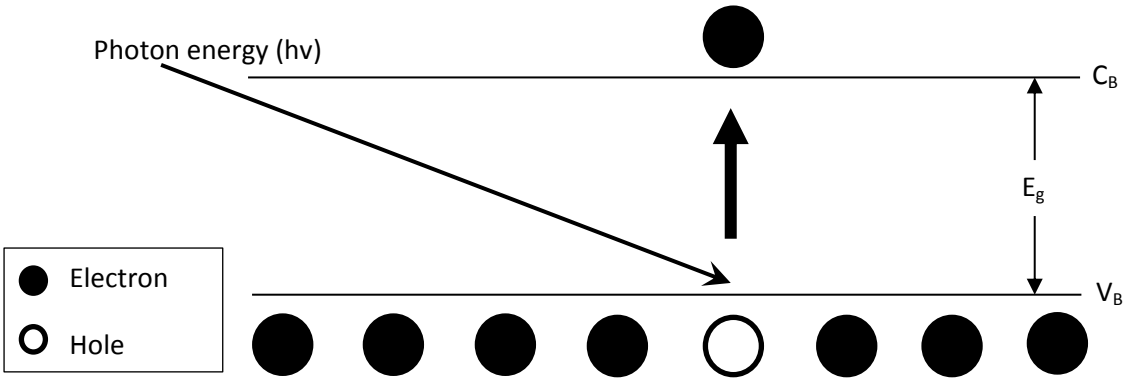


FIGURE 2.4 Schematic diagram of photovoltaic effect showing separation of electron-hole pair

junction where they are collected by electrical contacts. Generation of electron-hole pair takes place when energy of incoming photon is greater than the band gap energy.

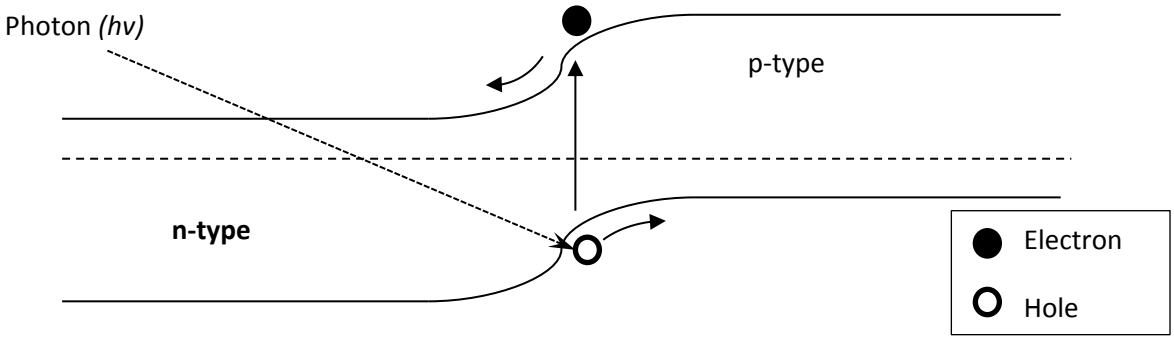


FIGURE 2.5 Schematic diagram of a p-n junction showing the influence of an electric field during charge creation

2.1.3 CDTE AS A MATERIAL FOR PHOTOVOLTAIC APPLICATION. CdTe is a direct band gap material which makes it a good photovoltaic material. The photons are absorbed within a ~2µm thickness of the film. And it has a band gap of 1.45 eV which is close to optimum for absorbing solar spectrum. Every photon with higher energy than the band gap that is absorbed will create a free electron and a free hole. To create voltage and current to perform external work, this electron-hole pair must separate and then recombine. An electric field is generated due to charge build-up on either side of the p-n junction which favors the diffusion of electrons on the *n*-type side of the junction. The electrons that are generated at the *n*-type material fall into the electron filed that will be forced downhill across the p-n junction as represented in figure 2.5.

The hole generated will interact with the electric field and will be forced into the *p*-type material. Similarly, when photons are absorbed the electrons will tend to go to the opposite direction to the *n*-type material causing them to separate. This movement caused by the electric field within the depleted zone is called drift. All these charge carriers are responsible for current generation. The electron-hole pairs generated outside the junction that need to be kept separated until they can travel to the junction. The time for which these electron-hole pairs remain separated is called their lifetime. If these are close enough to the junction so as to travel to the junction without recombining, they contribute to current charge generation. The time they spend in their mobile state depends on the material. Defects in the material such as dislocations and impurities also affect the lifetime. Direct band gap materials generally have shorter

carrier lifetime, however their absorption coefficient is much higher and therefore allows total absorption of the visible spectrum with a thinner material (e.g. ~2µm for CdTe). The surface of the absorbing layer is the area where most of the charge carriers are generated and it is important that the surface properties minimize the loss of free carriers here.

2.2 Electrical characterization of photovoltaic cells

2.2.1 Terminologies and measurements. Solar cells act as diodes under no external illumination. In a way, they are very similar to diodes except that they are composed of energy absorbing material and have a large area to collect electromagnetic radiation (photons). One the main characteristic of a solar cell is that the junction is very close to the surface to allow more photons to penetrate through. Due to similar properties to diodes, the current relationship of a solar cell may be expressed as:

$$J = J_0 \left[e^{\frac{qV}{kT}} - 1 \right]$$

where, J is the cell current, J_0 is the reverse saturation current, V is the voltage across the cell, q is the electronic charge, k is the ideality factor and T is the thermal voltage.

On photo generation of carriers, they ideally get collected at the respective contacts since they are separated within the bulk material rather than being injected. This is considered as reverse current. A photovoltaic cell behavior is characterized by the current that passes through the cell at each voltage point that is called the current density v/s voltage (J-V) curve. The main performance parameters used for characterization of a photovoltaic device are short circuit current (J_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and efficiency (η). As mentioned earlier, in the dark, a photovoltaic device behaves as a diode but in light it is ideally shifted by a constant J_L which is ideally equal to the rate at which photons are absorbed. If non-ideal series and shunt resistance are considered, the resulting J-V curve follows the following equation:

$$J = J_0 \left[e^{\frac{q(V - R_{Series} * J)}{kT}} - 1 \right] - J_L + \frac{V}{R_{Shunt}}$$

While illuminated, there is an exponential increase in forward current along accompanied by a reverse current due to collection of photo-generated carriers. The point at which these currents sum up to zero is the open circuit voltage (V_{OC}) and the current density at V = 0 is short-circuit current density (J_{SC}). The power produced by a photovoltaic cell at any given voltage bias is the product of current density and voltage. Maximum power point can be used to evaluate the conversion efficiency (electrical power output divided by optical power input) and the fill factor. These are defined as below:

$$Efficiency = \frac{V_{mp} \cdot J_{mp}}{P_{in}}$$

$$Fill\ Factor = \frac{V_{mp} \cdot J_{mp}}{V_{OC} \cdot J_{SC}} = \frac{P_{max}}{P_T}$$

where, V_{mp} is voltage at maximum power, J_{mp} is current at maximum voltage, P_{in} is the input optical power, P_{max} is maximum power and P_T is theoretical power. Figure 2.6 below gives a better understanding of the *J-V* curve with important data points.

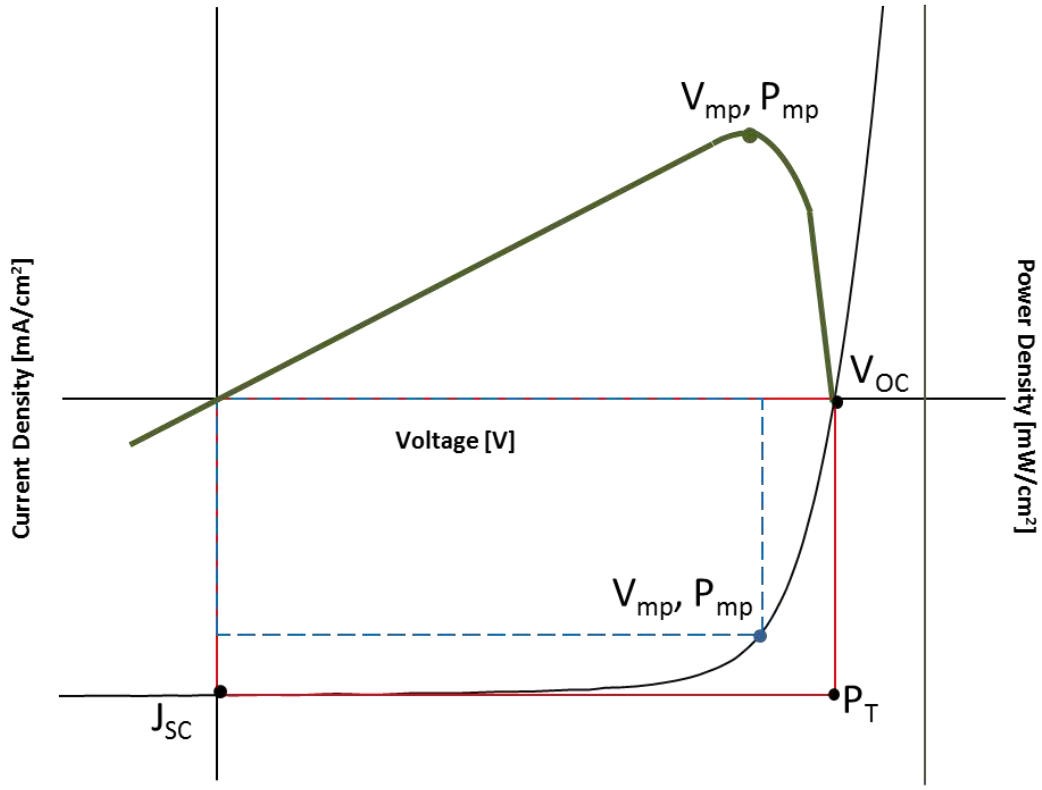


FIGURE 2.6 A model J-V curve illustrating the point of maximum power and other important data points

The fill factor is thus described as the ratio of power available at maximum power point against the open circuit voltage (V_{OC}) and short circuit current (J_{SC}). It basically the measure of the squareness of the *J-V* curves. It is therefore clear that greater squareness of curve is preferable.

2.3.2 ELECTRICAL (CURRENT DENSITY V/S VOLTAGE) MEASUREMENT: Electrical measurements were performed with a Model 10600 solar simulator from ABET Technologies using a high-pressure xenon arc lamp with an AM1.5 filter. Current density v/s voltage curves generated based on electrical measurements performed using Keithley 2420 SourceMeter controlled by a LabView program. The default measurement configuration is from -0.8 V to 1.2 V in 25 mV increments. Any arbitrary set of voltages can be enabled in the settings along with limiting current to prevent cell damage. Device areas are measured using a webcam that takes an image of a backlit solar cell and counts the pixels below certain brightness. Both the light intensity and area are calibrated for each set of measurements. Short-circuit current density was calibrated to cells measured by NREL. The cells are contacted by a fixture of spring loaded pins that provide 4-point connection and collect current from all around the front contact of the device.

In addition, Electroluminescence (EL) images was collected and studied for some devices using an EL setup that was fabricated and optimized in the Department of Physics at Colorado State University[28].

CHAPTER 3 CHARACTERIZATION METHODS

3.1. SCANNING ELECTRON MICROSCOPY (SEM)

3.1.1. SPECIMEN PREPARATION FOR SEM. In order to record good results and collect good images with a scanning electron microscope, good sample preparation is a very critical step. For this reason the sample must be fairly flat and conductive. The surface must also be thoroughly cleaned to get rid of any unwanted contamination or residue. The CdTe samples were therefore cleaned with isopropanol and dried with ultra-high purity nitrogen or argon gas to minimize residue on the surface. SEM chamber and stage size limits the size of sample that may be imaged. The samples were cut to ~1 cm^2 so that multiple samples could be imaged without breaking vacuum. The samples were cut using a glass cutter and mounted on brass stub/stage. CdTe is non-conductive but there is a layer of transparent conducting oxide under the CdTe layer. To make a good conduction path for the electrons, a small area on the CdTe film surface is scratched and a copper tape placed that connected the film to the specimen stub/stage. This allowed the charge to dissipate for clear undistorted micrographs to be collected.

3.1.2. FIELD EMISSION SCANNING ELECTRON MICROSCOPE IMAGING (FEG-SEM). A Jeol JSM-6500F Field Emission Gun Scanning Electron Microscope (FEG-SEM) was used for microstructural analysis of the cadmium telluride solar cell stacks, as well as the individual layers which make up a cell. The FEG-SEM was generally used to look at the surface of the depositions using an in-lens detector, which requires a short working distance as it detects low energy secondary electrons coming from the surface of the sample. A high acceleration voltage of 20 kV with an aperture of 30 μm was used. Energy Dispersive X-ray (EDX) analysis was also carried out in the FEG-SEM using a 20 kV acceleration voltage and 60 μm aperture to give both qualitative and qualitative chemical analysis with Thermo Noran energy-dispersive spectrophotometer (EDS).

3.2. TEM SAMPLE PREPARATION USING FOCUSED ION BEAM (FIB)

With TEM the quality of specimen prepared is normally reflected in the quality and integrity of the results obtained. High quality TEM samples were prepared using an FEI Nova 600 Nanolab dual-beam system where, a standard in-situ lift-out procedure was used. Step by step procedure for FIB specimen preparation is described in detail in appendix I. It is important to note that normally terms samples and specimen are loosely used interchangeably. However, with electron microscopy, sample refer to the substrate or object that is being characterized while specimen refer to the particular area on the sample or part of it that may be isolated from the sample for the purpose of characterization.

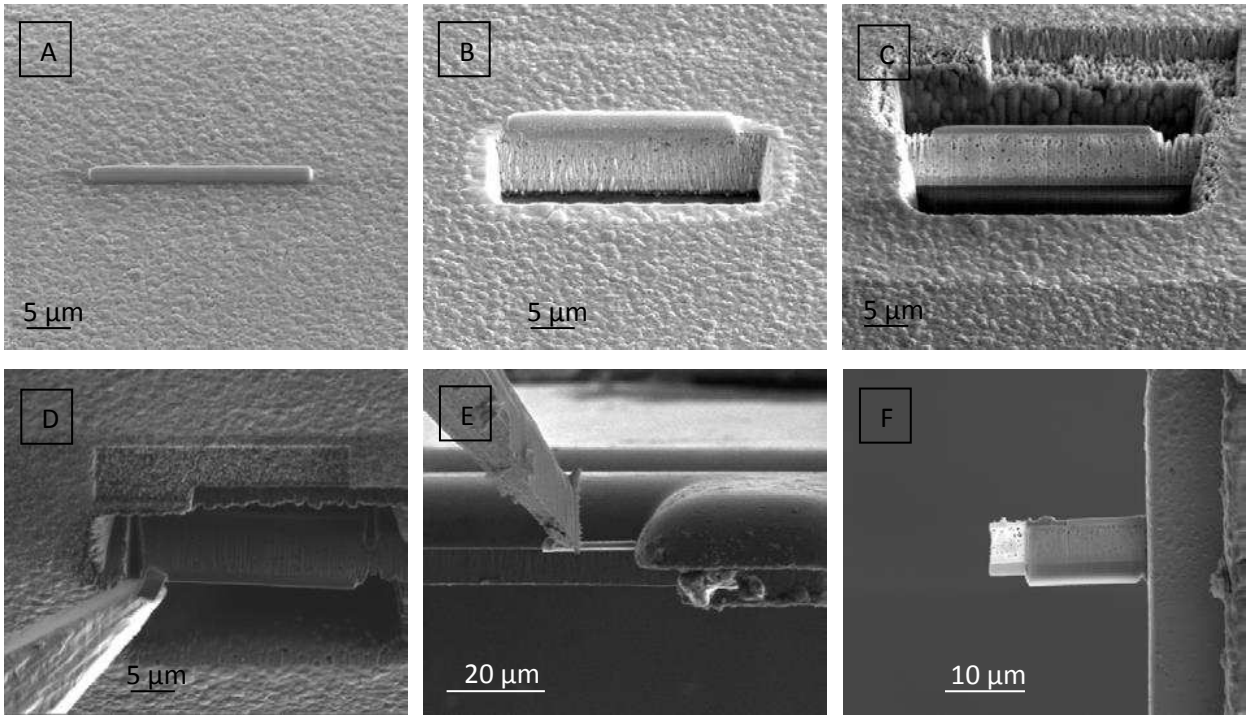


FIGURE 3.1 SEM and FIB induced SE micrographs captured at various stages of the in-situ TEM lift-out procedure. A) shows and SEM image of the platinum layer deposited onto the surface; B) shows the trench formation; C) shows the sample after the cleaning cross section; D) omniprobe attached to TEM specimen; E) TEM specimen attached to probe and copper grid; E) specimen after final thinning – ready for TEM imaging

This involved depositing a layer of platinum onto the sample surface above the area to be analyzed, using the ion beam with a current of 0.5 nA. A typical area of 20 µm by 2 µm was covered, with a thickness of 2 µm. An SEM image showing the sample after it is deposited is shown in Figure 3.1A. If the top 50 nm of the sample is required for analysis then a layer of electron beam deposited platinum (using a

voltage of 5 kV and current of 1.1 nA) was deposited before the ion beam platinum. Electron beam platinum has the advantage that it does not implant ions into the sample surface; however the deposition of platinum with the electron beam is too slow to use for the whole platinum layer thickness. Two staircase trenches are then cut either side of the platinum layer which is approximately 25 μm x 15 μm, the depth depends on the sample etching rate, but it is usually of the order of less than 10 μm using an ion beam current of 20 nA shown in Figure 3.1B. After the formation of the trenches a few micrometers from the platinum, a cleaning cross section is used at the lower current of 7 nA to clean up to the platinum, leaving a sample of approximately 1 micrometer thick shown in Figure 3.1C. Once this is done the sample is tilted to 7º and a U-shaped cut is formed leaving a small uncut part to support the sample shown in Figure 3.1D. The omniprobe is then inserted and welded onto the platinum protective layer, with platinum at 50 pA shown in Figure 3.1D and the final support of the TEM sample to the bulk sample is disconnected using 1 nA beam. Once this is done the sample should be free and lifted out on the needle by lowering the stage. The next step is to attach the TEM sample to a copper grid and detach it from the omniprobe, using a platinum weld at 50 pA and ion beam at 1 nA respectively shown in Figure 3.1E.

Once the sample is attached to the copper grid it can be further thinned down to approximately 100 nm as shown in Figure 3.1F. This is achieved by milling the sample with the ion beam starting at 1 nA with the sample tilted 0.7º either side of 52º. The sample is milled until it is 500 nm thick. The ion beam current is then reduced to 0.5 nA and the end 10 μm of the sample is milled each side until the sample is 200 nm thick. The current is further reduced to 0.3 nA and the end 5 μm is thinned to 150 nm. Finally the last 5 μm of the sample is thinned using a 100 pA current until the thickness is ~100 nm or less.

3.3. TRANSMISSION ELECTRON MICROSCOPY (TEM)

TEM was carried out using a Jeol JEM 2000FX equipped with an Oxford Instruments 30 mm^2 EDX detector and a Gatan Erlangshen ES500W digital camera above the phosphor screen. The TEM provides a more clear view of the grain structure than most other electron based techniques as the electrons are passing through the sample and being detected the other side giving a small interaction volume. As the

sample is ultra-thin, EDX can also be carried at a higher resolution; therefore the detection of any inter-diffusion between layers is possible. The TEM samples dimensions are relatively small in comparison to SEM samples. A normal size would be 5 μm - 10 μm in length. This means that the location where the sample must be extracted from must be chosen with care. If a sample is not homogenous several TEM samples must be produced at different locations to be able to see any variation.

3.3.1. STACKING FAULT CHARACTERIZATION IN TEM. The stacking fault density is measured by counting how many stacking faults intersect a 1μm line orthogonal to the stacking faults. For each sample 10 grains were measured and an average calculated. As the visibility of stacking faults changes with grain orientation, a double tilt holder was used in the TEM. The grain was tilted to the [110] zone axis prior to analysis by moving the Kikuchi pattern into the center as shown in Figure 3.2A. In Figure 3.2A the grain shows almost no signs of stacking faults and when the Kikuchi pattern is collected from the grain, no zone axis was in the center. The sample was then tilted until the [110] axis is centered. The electron beam is then directed along the (111) plane which makes the stacking faults visible as shown in Figure 3.2B. This exercise was performed for each grain to measure stacking fault density.

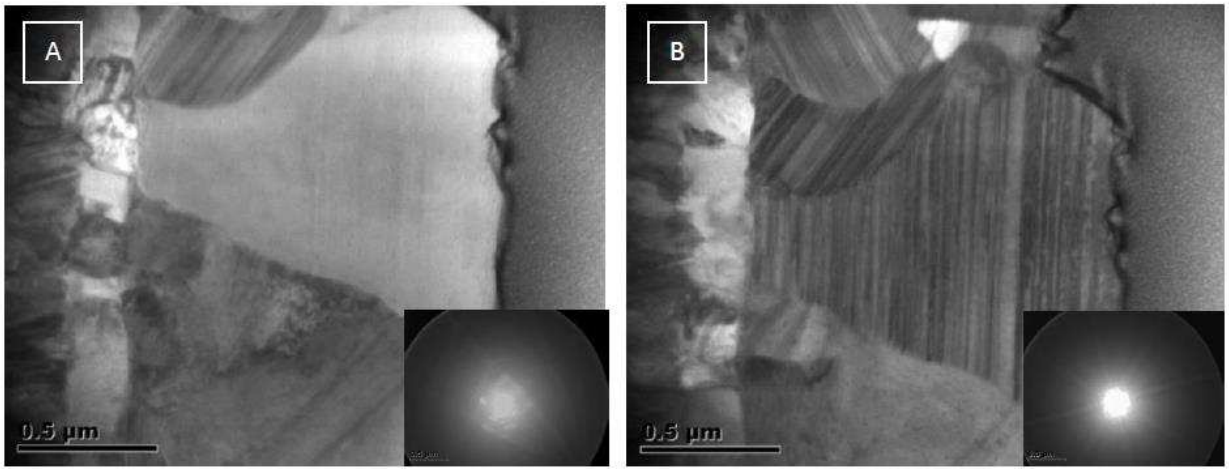


FIGURE 3.2 Bright field TEM micrographs showing the effect of orientation on the visibility of stacking faults: A) shows the grain not at a low order zone axis; B) shows the same grain as in image A tilted to the [011] zone axis (convergent beam diffraction patterns for these orientation are inset)

3.3.2. HIGH RESOLUTION TRANSMISSION ELECTRON MICROSCOPY (HRTEM). High Resolution Transmission Electron Microscopy (HRTEM) was also carried out using a FEI Tecnai F20 (S)TEM.

When the samples were prepared they underwent an extra step, a low voltage FIB clean-up of each side of the sample. The voltage of the ion beam was reduced to 5 kV and the current to 70 pA and the sample was tilted 2º each side of 52º (in-line with ion beam) and milled with the ion beam for 2 minutes. This reduces the amount of ion implantation and beam damage for better lattice imaging. HRTEM can be a useful technique for characterizing defects within the lattice of cadmium telluride and cadmium sulphide grains. Providing the sample is prepared well and the orientation of the sample is at the correct zone axis, a resolution of 0.2 nm can be obtained. This gives atomic resolution images so that stacking sequences can be interpreted and defects characterized as twin boundaries, intrinsic stacking faults or extrinsic stacking faults. Lattice spacing can be measured from the atomic resolution images using software to characterize the image.

3.3.3. SCANNING TRANSMISSION ELECTRON MICROSCOPY (STEM). Scanning Transmission Electron Microscopy (STEM) was carried out in a FEI Tecnai F20 S/TEM equipped with Gatan Bright and Dark field STEM detectors, Fischione High Angle Annular Dark Field (HAADF) STEM detector, Gatan Enfina Electron Energy Loss Spectrometer and an Oxford Instruments X-Max 80mm2 windowless energy-dispersive spectrometer (EDX). STEM imaging was performed at 200 kV with a camera length of 100 mm and condenser aperture size of 70 μm using a spot size of 7. HAADF images were collected in conjunction with STEM bright field images. HAADF imaging gives a unique perspective as the higher the atomic weight of the material the more the electrons passing through the sample will be detected. Therefore the amount of signal collected will depend on the atomic weights of the sample, giving atomic weight contrast in the image.

3.3.4. ENERGY DISPERSIVE X-RAY (EDX) IN SCANNING TRANSMISSION ELECTRON MICROSCOPY. The (S)TEM system is equipped with a Silicon Drift Detector (SDD) allowing high spatial resolution Energy Dispersive X-ray (EDX) measurements and chemical mapping. This was largely used for mapping diffusion of elements such as chlorine and sulphur in the cadmium telluride matrix. Point analysis is also useful as quantification of elements can be acquired with a sensitivity of ~0.5 at% for light elements such

as chlorine. EDX spectra were collected for 120 seconds. Maps were collected using the largest condenser aperture (150 μm) with the largest spot size. This allowed for a high number of counts. The dead time was controlled by changing the process time; each frame took approximately 120 seconds to collect. Maps were collected from 10 minutes up to 1 hour with no discernible sample drift.

3.3.5. ELECTRON BACKSCATTER DIFFRACTION (EBSD). Electron Backscatter Diffraction (EBSD) is a microstructural crystallographic technique which can be used to map grain orientation as well as phase identification, grain boundary angle information, grain defect information and grain size measurements. EBSD was carried out in the dual beam FEI Nova 600 nanolab using an ultra-high speed Hikari EBSD camera. The sample was tilted to 70º and a background signal subtracted to improve the Kikuchi patterns. An electron beam voltage of 20 kV was used with a nominal current of 24 nA. The collection rate of the Kikuchi patterns was 46 frames per second due to the slow scan speed required due to the small grain size of the material, which were indexed against a cubic/hexagonal cadmium telluride structure file. EBSD requires a very smooth surface for effective microstructural mapping. Therefore to analyse the surface of the cadmium telluride directly, a section of the surface was smoothed with a FIB using a beam current of 1 nA. The result of this sample preparation provides an adequately smooth surface for EBSD measurements to be obtained as shown in Figure 3.3.

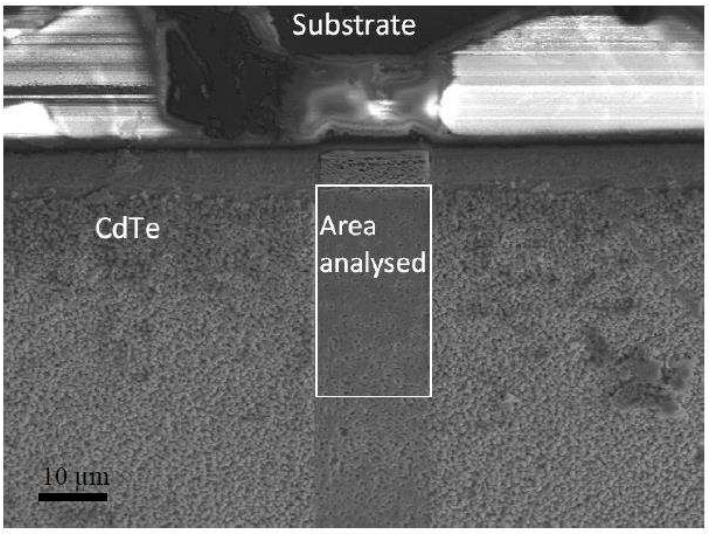


FIGURE 3.3 SEM image showing the area of analysis of treated cadmium telluride sample after being polished by FIB

The resolution of Electron Backscatter Diffraction can be improved from tens of nanometers to around 5 nanometres if an electron transparent film is produced and positioned at 20º to the horizontal. Kikuchi patterns can be produced and collected from transmitted electrons from the underside of the sample. This setup is shown in Figure 3.4. An electron beam voltage of 30 kV was used and a current of 6.9 nA. This increases the spatial resolution of EBSD which is advantageous for this study due to the small grain size and defects such as twins present in some of the samples.

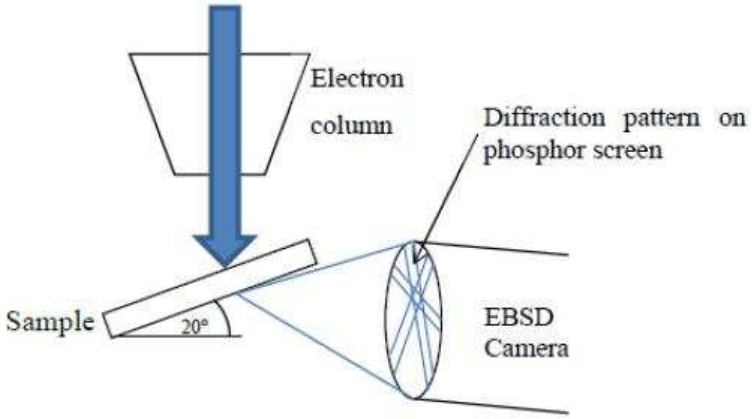


FIGURE 3.4 Schematic of Transmission Electron Backscatter Diffraction hardware and sample position

3.3.6. SECONDARY ION MASS SPECTROSCOPY (SIMS). Secondary Ion Mass Spectroscopy (SIMS) was carried out at Loughborough Surface Analysis (LSA) for elemental distribution of cadmium, tellurium, copper, oxygen, chlorine, tin and sulphur. A Cameca IMS 3F and 4F were used for SIMS depth profiling. The analysis was performed using Cs+ primary ion bombardment at 10 keV with a current of 1 μA with a spot size of 60 μm and negative secondary ion detection to optimise the sensitivity to chlorine. O2+ primary ion bombardment at 10 keV with a current of 20 μA with a spot size of 10 μm and positive secondary ion detection was used to optimize the sensitivity to copper. The chlorine data was quantified using an implanted reference sample of chlorine in cadmium telluride. No suitable reference sample was available with which to quantify the copper data.

3.3.7. X-RAY PHOTOELECTRON SPECTROSCOPY (XPS). Additional elemental characterization was performed using a Phi-5800 XPS which utilized a monochromatized Al Kα x-ray source and a neutralizing electron shower to reduce charging. The films were sputtered with a rastering Argon ion beam at a voltage of 5 kV over an area of 9 mm^2 for depth profiling at Colorado State University.

CHAPTER 4 DEVICE FABRICATION

4.1. TOOLS FOR DEVICE FABRICATION

4.1.1. BASELINE FILM DEPOSITION SOURCE. CdTe thin-films are deposition, $CdCl_2$ passivation treatment and CuCl deposition is carried out using an optimized sublimation deposition process using a single vacuum chamber with multiple sublimation sources called the Advanced Research Deposition System (ARDS)[29]. The ARDS consists of graphite sublimation sources that have nichrome based resistive heaters embedded within the source. All the necessary processes for making CdTe photovoltaic cells may be

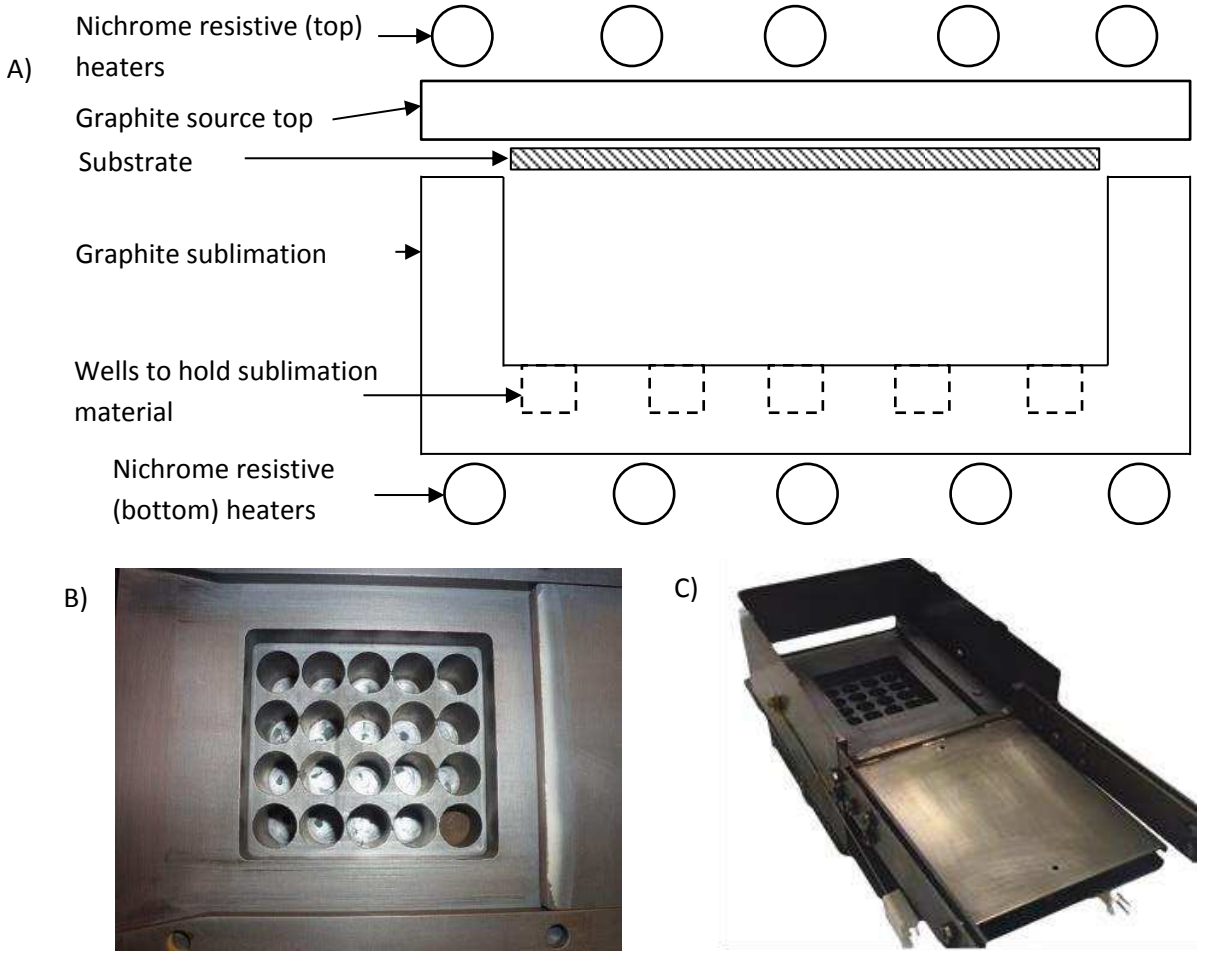
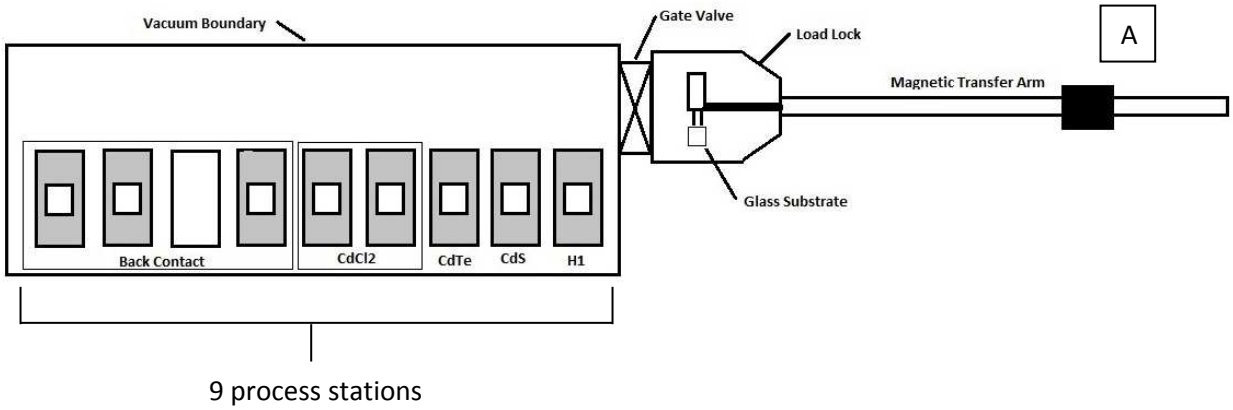


FIGURE 4.1 A) Schematic diagram of graphite vapor source for sublimating CdS, CdTe, CdCl2 and CuCl B) Deposition wells as seen from top of a graphite sublimation source C) A typical ARDS sublimation source

executed in this system. These sources have wells drilled in them that contain CdS, CdTe, $CdCl_2$, CuCl and other heating as well as controlled cooling sources that are used to control substrate temperature during the process. A schematic diagram of one such graphite sublimation source is shown in Figure 4.1A.

4.1.2. SUBLIMATION TOOL. Figure 4.1B and 4.1C are photographs representative of typical ARDS sublimation sources. Control of bottom source temperature allows the control of vapor pressure leading to control over the deposition rate of each species. The top temperature in combination with bottom controls the radiative power and therefore the temperature of the substrate through the process. All the sources control temperature using a proportional-integral-derivative controller that is tuned to minimize variability. This allows maintain the temperature to ± 1ºC during all processes. An automated transfer arm



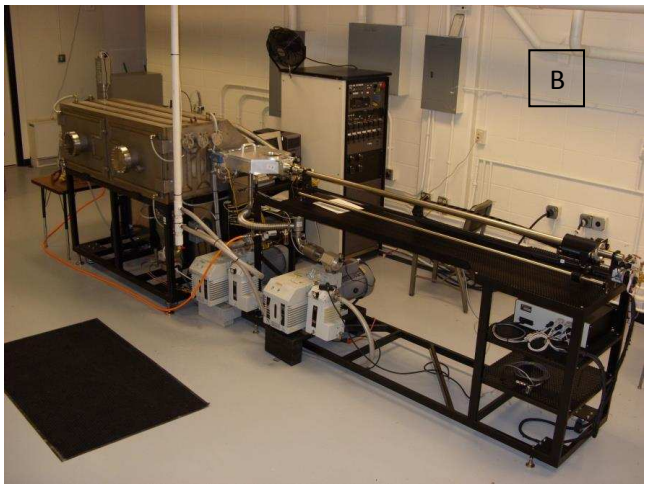


FIGURE 4.2 A) Schematic diagram and B) Photograph of the Advanced Research Deposition System (ARDS)

allows control over the sequence and duration of the processes. The process is based on a continuous process with 2 minute cycle time. However, as per requirement of the experiment, the sequence as well as cycle time may be altered and executed[30]. The system also allows switching between standard ambient of 2% O_2 in N_2 and pure N_2 as per the call of the experiment plan. The motion of the transfer arm may be controlled using a LabView program which also allows monitoring of system pressure and substrate temperature[30].

4.1.3. SPUTTER DEPOSITION OF $MG_XZN_{1-X}O$. The thin films are deposited on NSG TEC 10 soda lime glass that is coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). 100 nm $Mg_xZn_{1-x}O$ films are deposited using RF planar sputter deposition process. The process gas pressure is set at 5 mTorr with a composition of 1% oxygen in argon. The target has a composition of 11 wt% MgO with 89% ZnO and a diameter of 10 cm. The substrates were not heated during the sputter deposition. Deposition was carried out at room temperature. Approximately 10 minutes of deposition at 180 Watts gave the desired film thickness of 100 nm. The target was set at a distance of 15 cm from the substrate and a shutter mechanism was used to ensure cutting off deposition was prompt at the end of desired time[25].

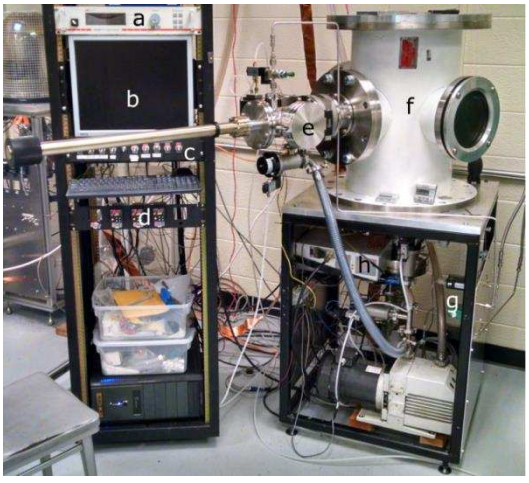


FIGURE 4.3 RF sputter deposition system with a) RF generator b) computer control from gas pressure and species c) pump controls d) temperature measurements using PID substrate temperature control e) load lock with magnetic transfer arm f) stainless steel vacuum chamber g) control MFCs for Ar and O h) RF match network

4.2. FILM DEPOSITION METHODS

Following section describes the standard film deposition procedures and conditions used in this study. Any deviation from these deposition conditions will be specified in respective sections.

4.2.1. ANTIREFLECTION COATING DEPOSITION. A 4-layer antireflection coating is deposited on the uncoated soda-lime glass side of the TEC 10 substrate using ion beam sputter deposition in a Veeco SPECTOR system. This film is of the Reichert design and is based on the coating reported by Kaminski *et al*. The design uses smooth oxide layers of precise thickness to provide destructive interference over a wide range of wavelength and angle of incidence. In this case Ta_2O_5 is used for the high-index layer and SiO_2 is used for the low-index layer. Refractive indices for the two oxide materials are measured using variable angle spectroscopic ellipsometry (VASE); thickness results are verified with profilometry. A program is written in MATLAB which calculates the front-surface reflectance of the structure using the transfer-matrix method. This reflectance is multiplied by the photon flux at each wavelength for the AM1.5G spectrum, and a global optimization is performed to minimize the calculated loss in short-circuit current due to reflection. Reflection measurements are performed using an integrating sphere at 8° from normal[27].

4.2.2. CDS N-TYPE WINDOW LAYER DEPOSITION. A 120 nm -130 nm layer of CdS is deposited using sublimation tool using the ARDS. The standard deposition of CdS is carried out at substrate temperature of ~520ºC. For this purpose the substrate is preheated in the preheating source where the top and bottom heaters are set at 620ºC. Preheating is performed for 110 seconds after which the automated magnetic transfer arm moves the substrate to the CdS sublimation source. This CdS sublimation source has bottom source temperature of 615ºC - 625ºC and the top source temperature is set at ~420ºC[30].

4.2.3. $MG_{0.23}ZN_{0.77}O$ BUFFER LAYER DEPOSITION. The thin films are deposited on NSG TEC 10 soda lime glass that is coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). 100 nm $Mg_{0.23}Zn_{0.77}O$ films are deposited using RF planar sputter deposition process. The process gas pressure is

set at 5 mTorr with a composition of 1% oxygen in argon. The target has a composition of 11 wt% MgO with 89% ZnO and a diameter of 10 cm. The substrates are not heated during the sputter deposition[25].

4.2.4. CDTE P-TYPE ABSORBER THIN-FILM DEPOSITION. Devices described in this study are fabricated on the $Mg_{0.23}Zn_{0.77}O$ films using a continuous vacuum process in a conventional superstrate configuration. The CdTe sublimation source has a bottom heater to heat the material for sublimation. A top heater positioned above the substrate enables the substrate to be maintained at the desired temperature. A graphite vapor source containing CdTe is heated to 552ºC - 558ºC bottom and 360ºC top while the substrate is preheated to ~610ºC in a separate heater before introducing the hot substrate into the sublimation source. These temperature and time set points are determined after several empirical experimental iterations to achieve the desired thickness of CdTe films. The thickness of the CdTe films is maintained at ~3.0 μm[30].

4.3. PASSIVATION TREATMENT AND BACK CONTACT

4.3.1. $CDCL_2$ PASSIVATION TREATMENT. After deposition of CdTe film the substrate is then passed over a $CdCl_2$ source for the $CdCl_2$ deposition and activation process immediately after CdTe deposition, without breaking vacuum. Approximately 4 μm $CdCl_2$ film is sublimated on CdTe where the $CdCl_2$ bottom source temperature is maintained at 447ºC while the top heater to maintain substrate temperature is set at 387ºC. This deposition takes 180 seconds after which $CdCl_2$ activation is carried out for another 180 seconds where in both top and bottom heaters temperatures are maintained at 400ºC[30]. The cadmium chloride passivation treatment is carried out in N_2 atmosphere. After $CdCl_2$ activation for 180 seconds the substrate is taken to a cooling station for 300 seconds which has only a top heater maintained at 435ºC. This station does not possess a bottom heater. Following cooling, the substrate is removed from the ARDS and rinsed using deionized water.

4.3.2. CUCL TREATMENT. Copper chloride in controlled quantity has been known to be critical for formation of back contact and bulk doping of CdTe photovoltaic films[31]. For Cu treatment CdTe film

with CdCl2 passivation is reintroduced into the ARDS and heated for 75-85 seconds using a heating source set at 330ºC. Following the preheating step, the substrate is introduced into the CuCl sublimation source where the bottom source temperature is set at 190C while the top heater for the substrate is set at 170ºC. CuCl sublimation is performed for 110 seconds and then the film is annealed in another process station within the ARDS at 200ºC top and bottom source temperature for 220 seconds[30].

4.3.3. TE BACK CONTACT DEPOSITION. 20 nm tellurium back contact is deposited using a Cooke Vacuum Products physical vapor deposition (PVD) system model MK VII – FR. 99.999% pure tellurium pieces used for deposition are obtained from Sigma-Aldrich Corporation. Tellurium pieces are placed in a molybdenum evaporation boat coated with alumina. Acoustic impedance of the controller for deposition is set at 9.81 g cm-2 s-1. During deposition the electric current is set between 70 A and 90 A to achieve a steady deposition rate of 5-10 Å/s. The deposition rate and thickness are measured using a quartz crystal monitor and monitored via an external digital display. A sliding shutter between the deposition boat and the substrate allows abrupt start and termination of Te deposition on the substrate. This shutter is manually operated from outside the vacuum chamber. The pressure during Te deposition is maintained at 10-5 Torr or less. Substrate is not heated during Te deposition.

4.3.4. CARBON AND NICKEL BACK ELECTRODE FABRICATION. Following the deposition of 20 nm Te back contact layer the films are ready to be coated with carbon and nickel paint to form the back electrode. Carbon (graphite) paint in polymer matrix that is diluted using methyl ethyl ketone (MEK) is sprayed on the Te surface to a thickness of about 50 µm. This paint is allowed to dry for 2-5 minutes after which similar nickel paint is sprayed. The nickel paint is made from fine nickel particles suspended in a polymer binder diluted with methyl ethyl ketone. The thickness of this nickel paint is about 100 µm. The painted surface is allowed to dry for 6-8 hours.

4.3.5. DELINEATION AND PHOTOVOLTAIC DEVICE FABRICATION. Once the paint is completely dry, the films are delineated into 25 square devices on each substrate with each square device measuring

approximately 0.65 cm^2. Delineation is carried out by masking the painted surface of the film and bead blasting the unmasked regions thus exposing the TCO in the unmasked areas. Thin line of indium is soldered in the regions between the cells that have TCO exposed to from the front electrode contact.

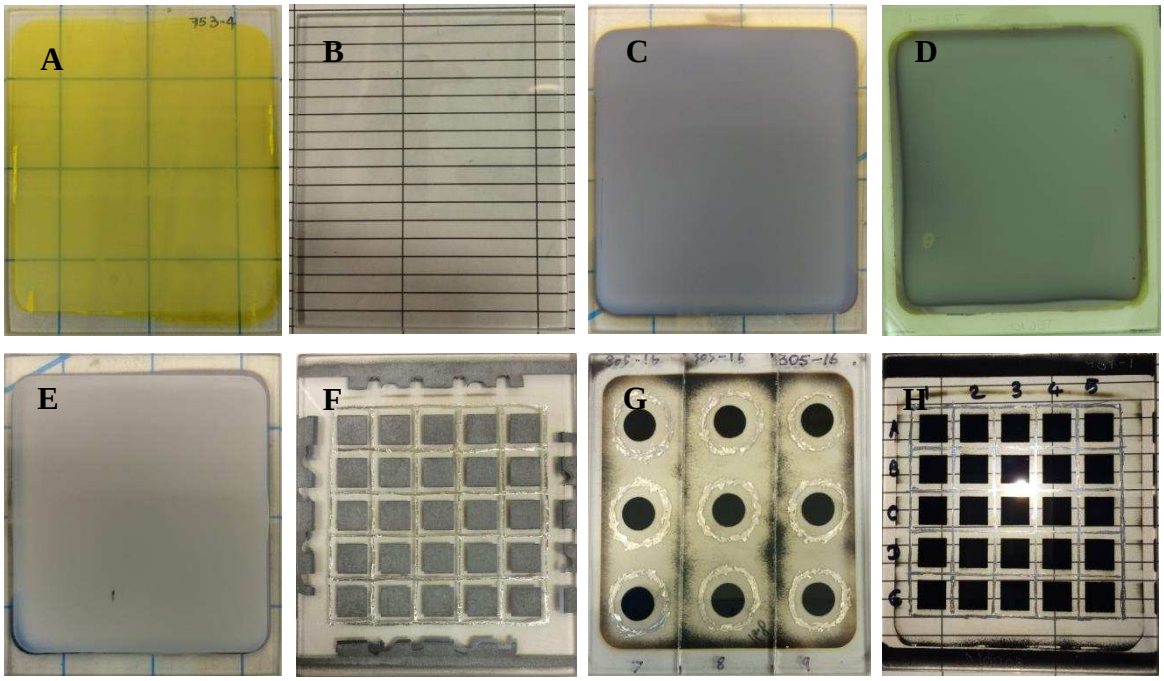


FIGURE 4.4 A) CdS deposited on Tec12 D soda lime glass coated with SnO2:F; B) MgxZn1-xO sputter deposited on Tec10 soda lime glass coated with SnO2:F; C) CdTe sublimated on CdS or MgxZn1-xO; D) $CdCl_2$ deposited on CdTe before being rinsed with deionized water; E) Te deposited on CdTe after CdCl2 rinse and Cu treatment F) Film painted with C and Ni paint and bead blasted to be delineated into 25 cell format g) film painted with C and Ni paint and bead blasted to be delineated into a 9 cell format h) cells as the appear from front side of glass

4.4 PROCESS AND PERFORMANCE REPEATABILITY OF CDTE DEVICES

The in-line sublimation tool has been extensively used for fabrication of CdS/CdTe and $Mg_{1-x}Zn_xO$/CdTe photovoltaic device fabrication. These films exhibit very good repeatability of film structure as well as device performance. Once the parameters are dialed in for desired configuration of film stack, the tool allows repeated fabrication of multiple films that have identical performance. Since 2010, the system has been operational for over 1050 days allowing fabrication of an average of 7-10 substrates each day. Each substrate has 6, 9 or 25 devices. All devices on each substrate and subsequent substrates fabricated using similar process parameters have identical performance and the process is highly

repeatable. This has been demonstrated with several different film configurations with over 100,000 fabricated small area devices.

To keep a check on repeatability of process and maintain a constant reference, CdS/CdTe baseline cell are fabricated from time to time. These baseline devices are fabricated using identical process parameters. Figure 4.5 represents average performance of these baseline devices over a period of 36 months. Very consistent performance repeatability is observed over these 36 months with 100s of devices. Over time reduction in the spread of performance is observed which may be attributed to reduction in time that the vacuum chamber is exposed to atmosphere. The system undergoes a biweekly preventive maintenance and reloading of deposition materials and apart from occasional breakdowns, these are the only times the vacuum chamber is exposed to environment. Table below also shows standard deviation of each performance parameter. Such statistically significant data set gives researchers the ability to confidently conduct scientific studies that are statistically relevant.

Table 1

Average J-V performance of fabricated devices over a period of 36 months[30]

V_{OC} [mV]	**J_{SC} [mA/cm^2]**	**FF (%)**	**η (%)**
762 ± 23	**21.3 ± 2**	**73 ± 2**	**12 ± 0.6**

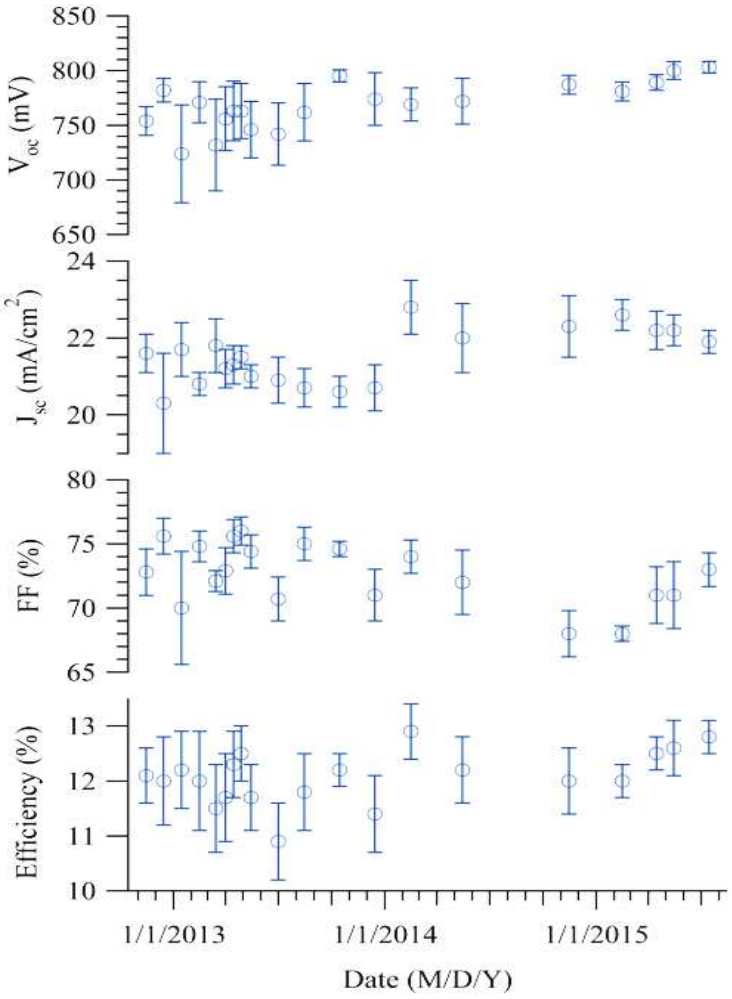


FIGURE 4.5 Average performance (± a standard deviation) for each sample set over 36 months period[30].

CHAPTER 5 EFFECTS OF $CDCL_2$ PASSIVATION TREATMENT

5.1 $CDCL_2$ TREATMENT METHOD

$CdCl_2$ passivation treatment is performed using several different methods. These methods include vapor treatment, wet treatment and sublimation treatment. All these treatments are followed by high temperature activation process. The $CdCl_2$ treatment described and investigated in this study is performed by sublimating $CdCl_2$ on as deposited CdTe in the ARDS. For sublimation of $CdCl_2$ the sublimation source temperature is maintained at about 435ºC while the top heater is maintained at about 385ºC when the substrate enters the $CdCl_2$ sublimation source[32]. When the substrate enters the $CdCl_2$ sublimations source after CdTe film deposition the temperature of the substrate is approximately 460ºC. The sublimation is carried out for 180 seconds under baseline conditions followed by 180 seconds of activation. The activation is performed in the ARDS primary chamber at the annealing station where the bottom and top temperature of the annealing source is maintained at 400ºC. At the end of $CdCl_2$ passivation process and activation treatment there is few microns of $CdCl_2$ residue that is left on the CdTe film surface that is rinsed using deionized water. Our baseline devices see an improvement of electrical performance from about 1% to over 12% in efficiency with this $CdCl_2$ passivation treatment[20], [22], [33]. This improvement is caused by enhancement of all major performance parameters viz. short-circuit current, open-circuit voltage and fill-factor.

$CdCl_2$ passivation treatment is known to have a major impact on device performance for several decades but the precise cause of such improvement has not been very well understood. Through this study it is understood to have at least 3 major effects on CdTe film structure and electronic properties:

1. CdTe thin-film grain growth
2. Recrystallization of CdTe
3. Chlorine doping the CdTe grain boundaries

In the subsequent sections the understanding developed during this to better understand and refine $CdCl_2$ treatment for CdTe photovoltaics will be described.

5.2 CdTe thin-film grain growth

Grain growth in CdTe films can be observed with change in surface morphology of CdTe films under an SEM as well as change in grain size observed under a cross-section TEM specimen. Figure 5.1 shows SEM images of CdTe film surface at increasing passivation times. It can be distinctly noticed that as deposited CdTe thin-films without a $CdCl_2$ passivation treatment has faceted grains with prominent troughs between the grains. As the passivation time increases there is a gradual increase in efficiency observed along with change in surface morphology. The grains become less faceted with increasing passivation time and coverage of the films appears to get more homogenous. Reduction in troughs between the grains is also observed and it gets increasingly difficult to distinguish individual grains with increasing passivation time[20].

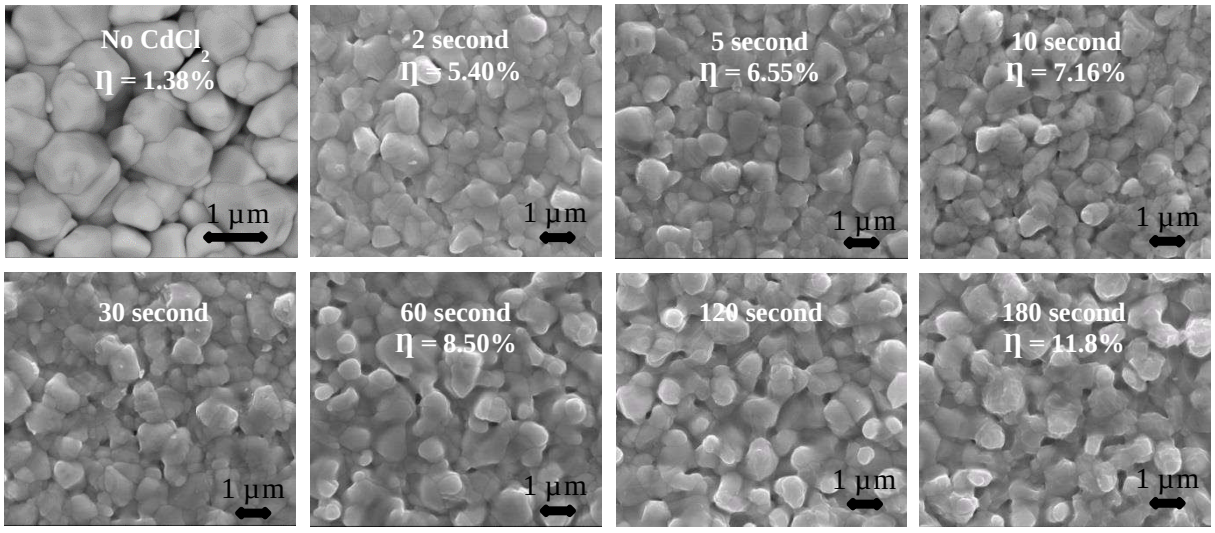


FIGURE 5.1 SEM images of CdTe surface as it changes with $CdCl_2$ passivation time.

Cross section TEM images also show change in grain size. As deposited films appear to have several smaller grains at the CdS/CdTe grain boundary with another 1-2 layers of grains that form an approximately 2.4 µm film. As $CdCl_2$ passivation time is increased there is a clear reduction in density of

smaller grains observed at the CdS/CdTe grain boundary and larger CdTe grains are progressively observed. This trend can be clearly seen in figure 5.2.

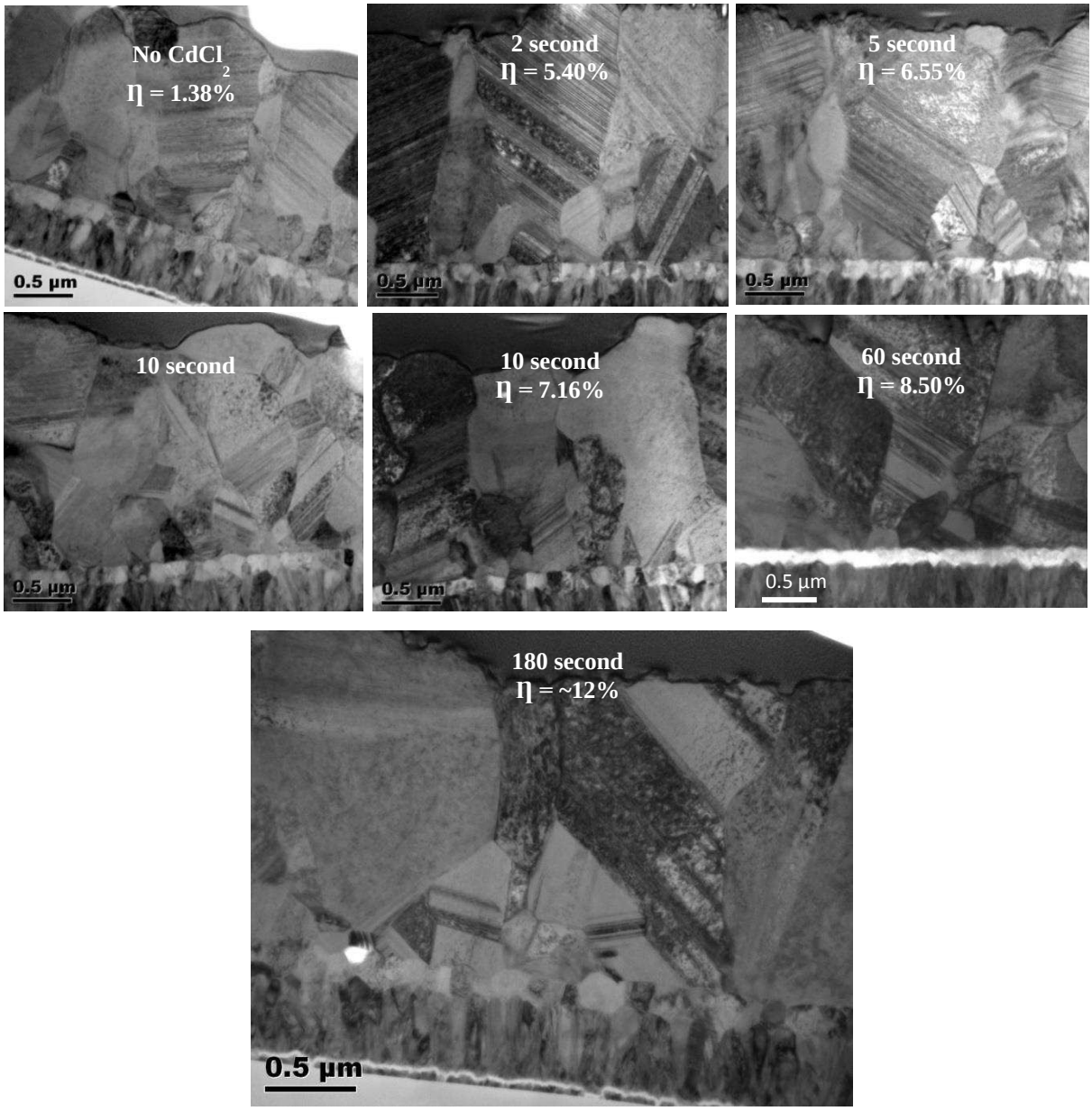


FIGURE 5.2 Cross section TEM images of CdTe film as it changes with $CdCl_2$ passivation time.

The representative TEM image of CdTe film treated for 180 seconds also suggests that after 180 seconds of treatment there are CdTe grains that appear to grow from CdS/CdTe interface to the back

surface of the film. This is a trend observed in several other TEM micrographs with 180 seconds or longer passivation treatment[26][22].

Terheggen *et al* have shown that $CdCl_2$ passivation treatment initiates at the back surface[34]. The best understanding for this mechanism suggests that Cl travels to the CdS/CdTe interface through the CdTe grain boundary and after some accumulation at the interface begins changing the grain structure. Figure 5.3 shows cross section EDS map of baseline CdS/CdTe films with Cl decorating the CdS/CdTe interface and CdTe grain boundaries.

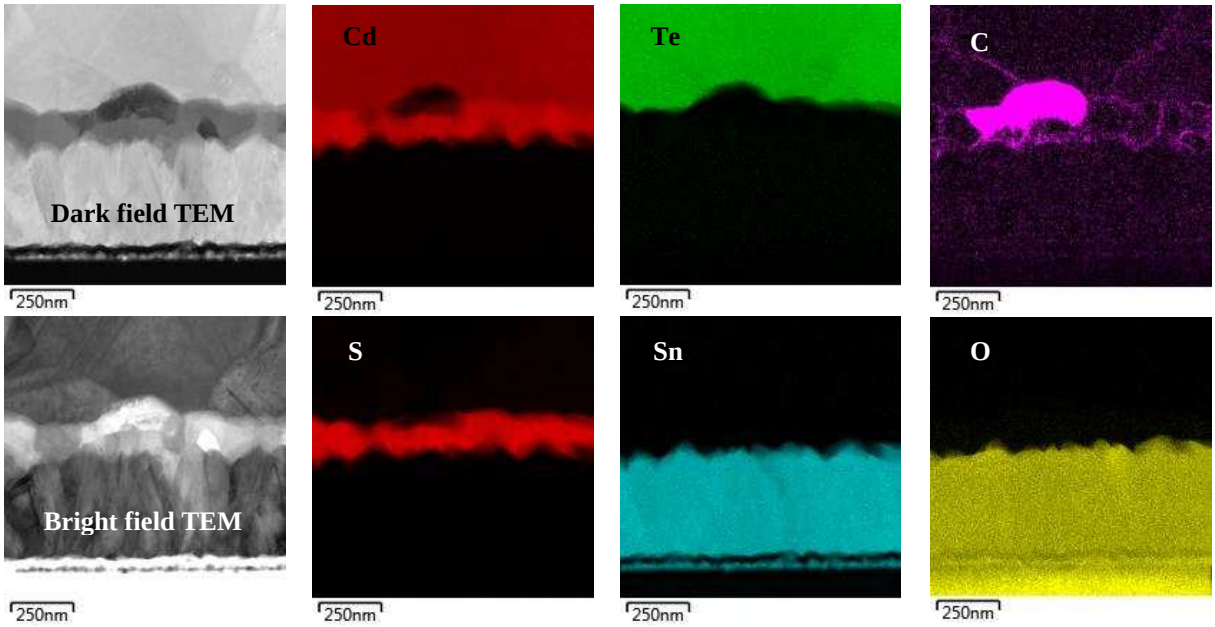


FIGURE 5.3 Cross section EDS maps of CdS/CdTe interface and parts of CdTe grain boundaries after 180 seconds $CdCl_2$ passivation treatment.

Study was also performed to understand whether presence of Cl is in form of $CdCl_2$ or as independent chlorine. Since the film has dominant content of Cd, EDS maps with $CdCl_2$ treated were not conclusive. Therefore, for imaging purpose CdTe films were treated with $MgCl_2$[35]. With this study it was revealed that Cl at the grain boundaries was in from of chlorine and no Mg signal was detected at CdTe grain boundaries or interface. A reaction between $CdCl_2$ and CdTe to for independent chlorine is not a feasible reaction. However, when vacancy Te (V_{Te}) being replaced with Cl is considered for Gibbs free energy calculation, breaking down of $CdCl_2$ to form independent Cl appears feasible. V_{Te} and Cl_{Te} is considered

it gives a value of 531.9 kJ/mole while the energy of formation for $CdCl_2$ is 343.9 kJ/mole[36]. This explains the presence of Cl at grain boundaries in form of chlorine and not as a chloride. This explanation is suggested by Li *et al* has shown through electron energy loss spectroscopy (EELS) and density functional theory (DFT) modeling that V_{Te} exist in CdTe thin films[37].

$$CdCl_2 \rightarrow Cd + 2Cl \ (\Delta G = +343.9 \text{ kJ/mole})$$

$$CdCl_2 \rightarrow 2Cl_{Te} + Cd \ (\Delta G = -531.9 \text{ kJ/mole})$$

Study published by Zhou *et al* explains the mechanism involved in CdTe grain growth and elimination of small grains[38]. $CdCl_2$ preserves its linear molecular structure in the vapor phase and exhibits high vapor pressure. Temperature of 400ºC at which our $CdCl_2$ activation treatment is preformed sufficient $CdCl_2$ exists within the CdTe films. The interaction between CdTe and $CdCl_2$ is sufficient to affect the polycrystalline grain structure. Study of CdTe-$CdCl_2$ phase diagram reported by H.Tai *et al* [39]and liquid phase epitaxial growth study published by Saraie *et al*[40] suggests formation of a eutectic liquid that causes recrystallization of CdTe grains to form larger grains and elimination of small grains. CdTe and $CdCl_2$ phase diagram shows that at 508ºC they form a eutectic liquid. Thermal modeling shows that initial temperature of our substrate during $CdCl_2$ treatment reaches such temperature.

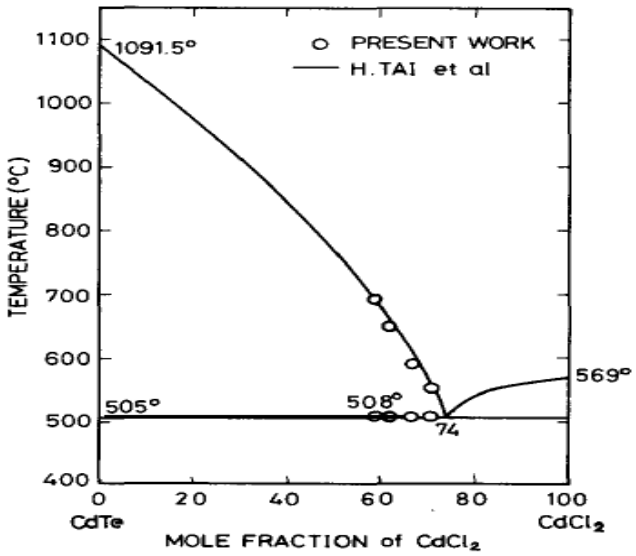


Figure 5.4 Phase diagram of the CdTe-$CdCl_2$ system

5.3 RECRYSTALLIZATION OF CDTE

$CdCl_2$ is believed to act as a flux agent that increases the atomic mobility of CdTe at annealing temperatures. CdTe films before $CdCl_2$ passivation treatment show very high density of stacking faults as

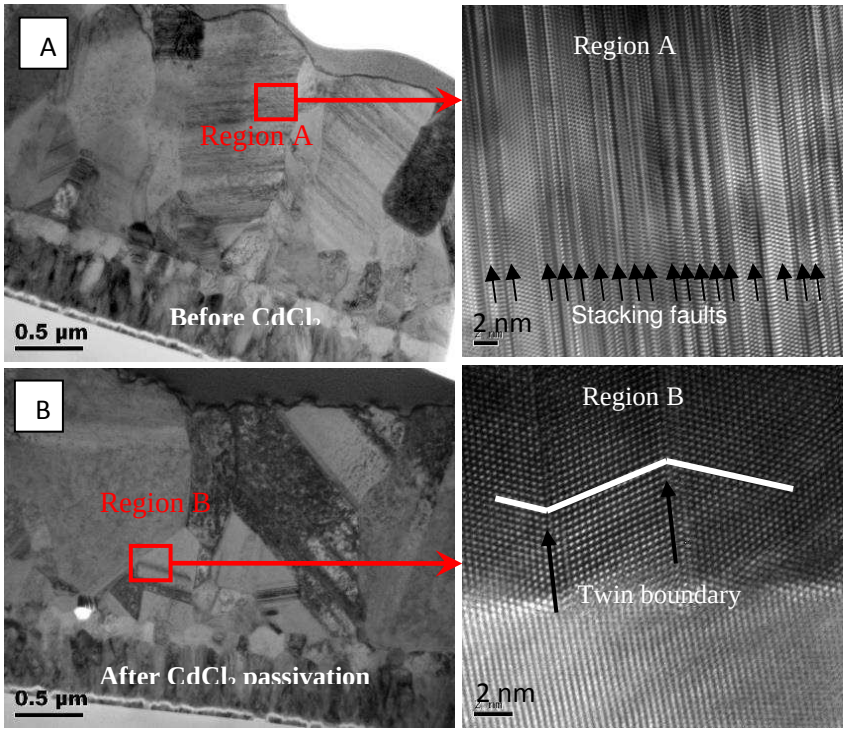


FIGURE 5.5 TEM and HRTEM showing stacking faults (A) before $CdCl_2$ passivation and presence of only twin boundaries (B) after passivation treatment.

can be seen in the TEM image in figure 5.5A. HRTEM image of a small region A confirms the presence of stacking faults prior to $CdCl_2$ passivation treatment. After $CdCl_2$ passivation treatment stacking faults are eliminated as can be seen in the representative TEM image in figure 5.5B. Twin boundaries persist in the CdTe microstructure after $CdCl_2$ passivation treatment but these twin boundaries are benign to CdTe photovoltaic performance as shown by Hyun Yoo *et al*[41]. Studies by Kim *et al*[42] and Abbas *et al* [33]have also shown that only temperature in absence of $CdCl_2$ do not have any effect on orientation and texture of CdTe films. Exposure of these films to high temperature in absence of $CdCl_2$ does not remove the stacking faults. However, presence of $CdCl_2$ does cause randomization of CdTe film crystals. During this randomization process CdTe films recrystallize during which Cl atoms are understood to be occupying V_{Te} sites resulting in elimination of stacking faults. This explanation can be supported by the

study conducted by Abbas *et al*[22] that showed stacking faults reappear when the chlorine is removed from the films by reheating the passivated substrate under vacuum.

5.4 CHLORINE DOPING THE CDTE GRAIN BOUNDARIES

Chlorine plays a greater role than mere recrystallization and grain growth of CdTe grains. Cl is known to dope the CdTe grain boundaries *n*-type that leads to higher device performance. This is understood to be caused increase in electron mobility induced by creation of better conduction path created by *n*-type doping the grain boundaries in *p*-type absorber material. Mao *et al*[43] have shown that over 90% of Cl in the CdTe films is concentrated at CdTe grain boundaries. It is also calculated using EBSD and SIMS under the same study that Cl concentration of $2.4x10^{14}$atoms/cm^2 relates well to the measured Cd and Te concentration that ranges between $3.4x10^{14}$ to $5.5x10^{14}$atoms/cm^2. These results imply that upto 60% of the available Te atoms are bound to Cl at the grain boundaries. Cl concentration in the grain bulk is measure at $4x10^{17}$atoms/cm^3. In support of these observations Abbas *et al*[44], Li *et al*[45] and Mao *et al*[43] have detected higher concentration of Cl at CdTe grain boundaries using ToF-SIMS (time of flight secondary ion mass spectroscopy) and EDS. Similar Cl signature is also observed in our sublimated CdTe films as seen in TEM/EDS maps in figure 5.3 as well as ToF-SIMS maps shown in figure 5.6. Depth profiling is not a good measure of Cl concentration in the film since over 90% of the Cl signal is associated with grain boundary and larger grains would have fewer grain boundaries. Therefore, films with larger grains will show much lower Cl content in the film compared to films with smaller grains. However, the concentration of Cl at the grain boundaries of both these specimen may not be very different.

In addition, Li *et al* have shown using EBIC (electron beam induced current) imaging that a CdTe photovoltaic device before $CdCl_2$ treatment has dark grain boundaries while after treatment are bright and show high current collection[37]. EELS (electron energy loss spectroscopy) of such a grain boundary also show that Cl occupies V_{Te} sites. These studies also relate well to the results obtained from DFT (density

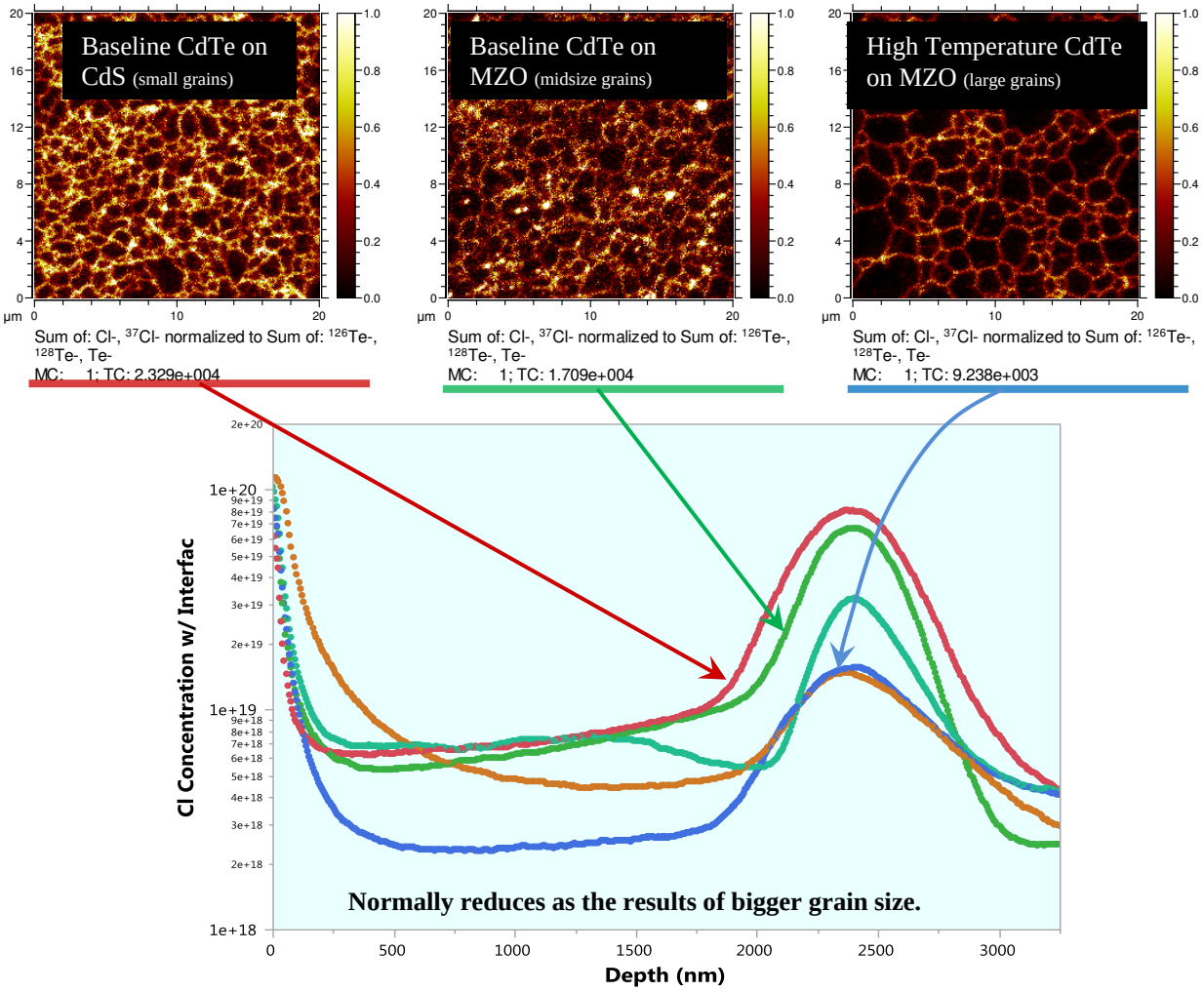


FIGURE 5.6 ToF-SIMS (time of flight secondary ion mass spectroscopy) showing Cl concentration at CdTe grain boundaries (top 3 images) and SIMS depth profile showing lower Cl concentration for films with larger grains (bottom plot).

function theory) modeling that strongly imply that any grain boundary will absorb sufficient Cl to clean up the gap and turn the material *n*-type explaining EBIC observations[41]. The built-in field formed in the regions between the grain boundary and grain interior help separate photogenerated carriers and reduces carrier recombination. Electrons get attracted to the grain boundaries while holes are repelled making

grain boundaries and grain interiors independent pathways for electron and hole conduction respectively. Figure 7 shows a schematic of band diagram representing formation of a *p-n-p* junction at the CdTe grain boundary.

These results imply Cl has a major role in not only altering the crystallographic and morphological characteristics of CdTe films but also in enhancing its electronic properties to form a good photovoltaic device.

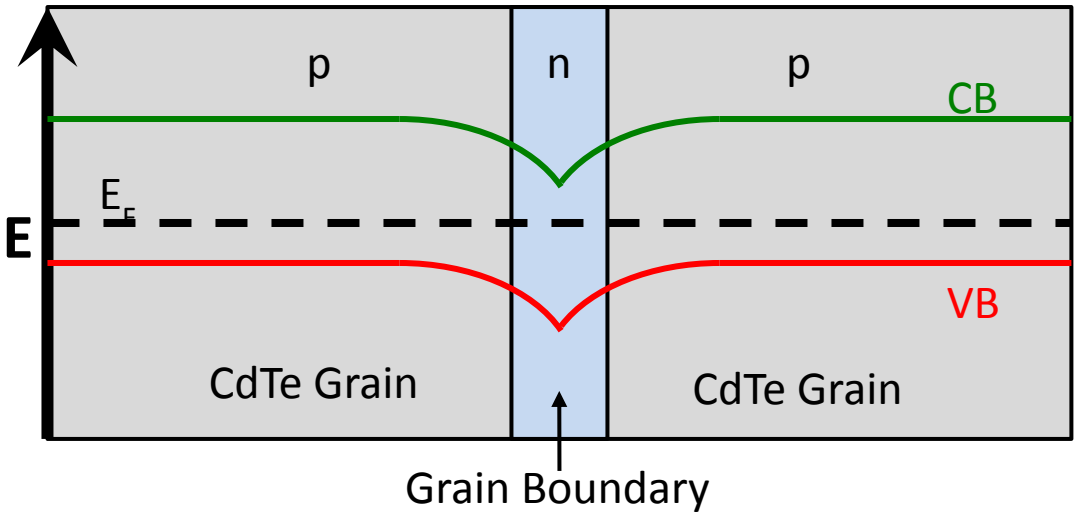


FIGURE 5.7 Schematic sketch showing band diagram of the p-n-p junction at CdTe grain boundary[37]

CHAPTER 6 CHARACTERIZATION OF BASELINE CDTE FILMS AND DEVICES

6.1 STRUCTURE OF BASELINE CDTE FILMS

Cadmium telluride thin films are deposited using optimized sublimation based deposition on NSG-Pilkington TEC 12D soda lime glass that is coated with fluorinated tin oxide (FTO) that acts as a transparent conducting oxide (TCO). A continuous vacuum process is carried out to deposit the films in an inverted configuration[30]. Graphite vapor sources containing CdS, CdTe and $CdCl_2$ are heated to the sublimation temperatures of the respective materials. The superstrate is passed over different sources and forms a sealing arrangement with the graphite. A ~ 120 nm layer of cadmium sulfide is first deposited onto FTO layer followed by ~2.4 µm layer of CdTe. Cadmium chloride passivation treatment at 400°C in 2% oxygen atmosphere is then carried out followed by annealing. The baseline passivation treatment time for these kinds of films is 180 seconds that is considered as the baseline reference in this study. Following this a copper doping process is carried out. Each substrate allows fabrication of 9 research scale cells <1 cm in diameter. Multiple cells with each process condition are prepared and the electrical characterization presented here shows the best performing device from each such substrate while all the fabricated devices follow the trend.

Baseline samples are prepared by preheating the substrate at 620ºC for 110 seconds. Thereafter, a 120 nm CdS layer is deposited at 440ºC substrate temperature followed by deposition of the CdTe layer. Entering the CdTe source the temperature of the substrate is 445°C. This is followed by $CdCl_2$ deposition where the substrate temperature when it enters the $CdCl_2$ source is 406°C. The temperature of the substrate at each stage is determined using advanced thermal modeling software that is designed using LabVIEW[30].

An important process step in the fabrication of high efficiency CdTe photovoltaic devices is the cadmium chloride ($CdCl_2$) passivation treatment. This passivation treatment improves film microstructure and electrical characteristics of CdTe photovoltaic devices. Cells made from films using closed space

sublimation discussed here, without chloride treatment exhibit ~2% efficiency while passivation treatment improves the efficiency to ~12% or higher. An earlier study has shown that annealing treatment in absence of $CdCl_2$ reduces the density of stacking faults in CdTe grains [8]. However, the treatment time

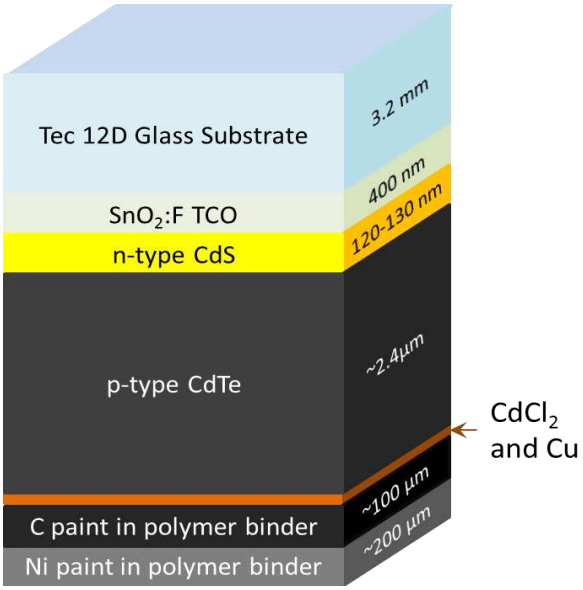


FIGURE 6.1 A schematic diagram of baseline CdTe thin film photovoltaic device (not to scale)

and temperature without $CdCl_2$ does not have substantial effect on electrical performance and cell efficiency remains low. Use of cadmium chloride has been known to remove the stacking faults[6, 9].

6.2 MATERIALS CHARACTERIZATION OF BASELINE CDTE FILMS

6.2.1 OVERVIEW OF CDTE FILMS. To understand the microscopic properties of CdTe films it is important to understand the basic structure of the film as can be seen under a transmission electron microscope.

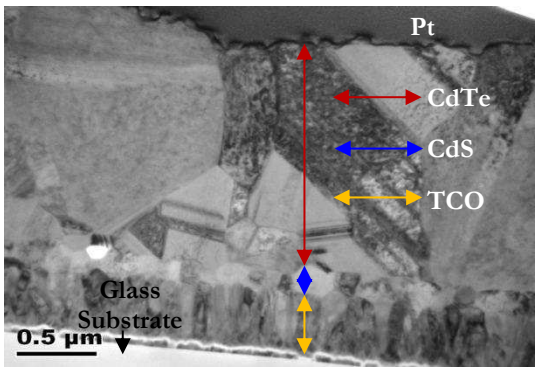


FIGURE 6.2 cross section tem micrograph showing various layers of a baseline cdte film[20]

As can be observed in the cross section TEM micrograph, the film consists of distinct layers of transparent conducting oxide (SnO:F), CdS and CdTe. $CdCl_2$ passivation treatment is applied after depositing the CdTe layer. Once the $CdCl_2$ haze is rinsed with deionized water, substrate is reheated to ~90ºC and Cu doping is performed by sublimating CuCl followed by 220 seconds of annealing at 220ºC.

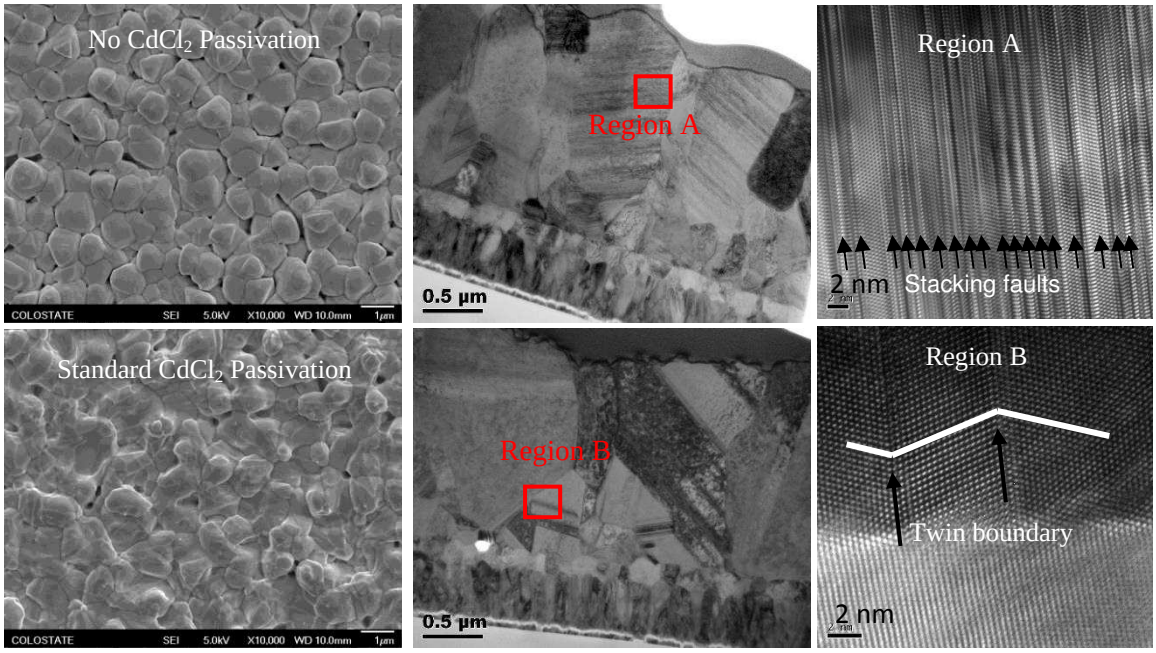


FIGURE 6.3 Surface SEM (left), BF- STEM (center) and HRTEM (right) showing effect of $CdCl_2$ passivation on grain microstructure in CdTe film of baseline samples.

6.2.2 EFFECT OF $CDCL_2$ PASSIVATION ON CDTE FILMS MICROSTRUCTURE. Grains of the CdTe layer have a very high density of stacking faults before $CdCl_2$ passivation treatment is carried out. The difference between the internal structures of such grains can be observed in the HRTEM images in figure 6.3.

As deposited CdTe films without $CdCl_2$ passivation show distinct grains that can be seen in the surface SEM micrograph. Cross section BF-STEM image shows smaller grains at the CdS/CdTe interface and high density of stacking faults that can be confirmed from the HRTEM image. After 110 second baseline $CdCl_2$ passivation is carried out, SEM image reveals a more homogeneous coverage of CdTe. Further, BF-STEM image show no signs of stacking faults while HRTEM confirms elimination of stacking faults. Presence of twin boundaries is seen post $CdCl_2$ passivation treatment.

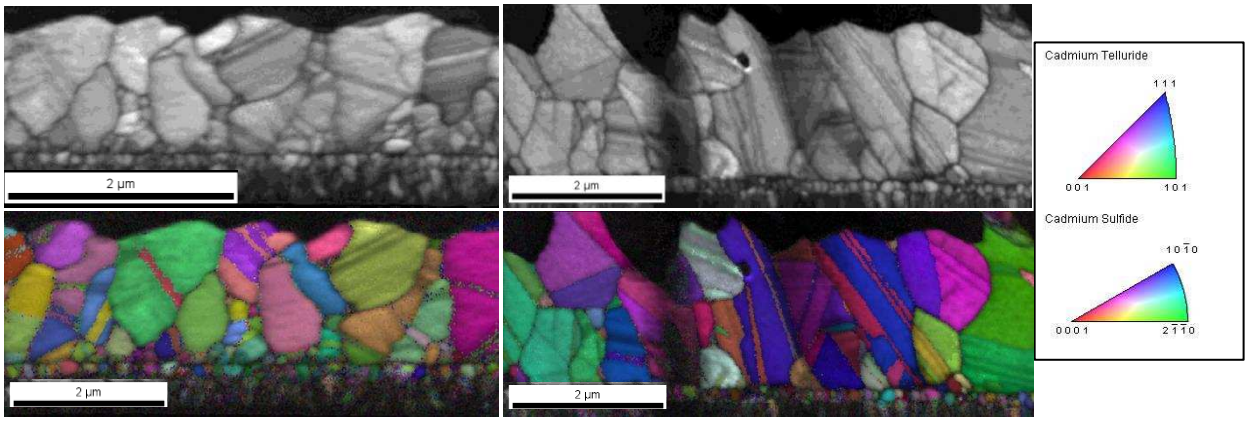
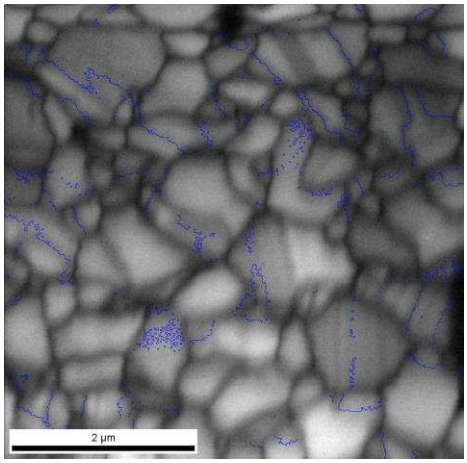


FIGURE 6.4 cross section ebsd of as deposited (left) and cdcl2 treated (right) cds/cdte films

EBSD proved to be a very important tool in understanding grain orientations as well as defects such as stacking faults and grain boundaries in CdTe and CdS films. Cross section EBSD map in figure 5.4 shows larger concentration of smaller grains at the interface of CdS and CdTe. Such large concentration of small grains is not observed in films that underwent $CdCl_2$ passivation treatment. Also, it is observed that grains after passivation treatment that are adjacent to each other have similar orientation unlike as-deposited films. In addition, for as-deposited films it can be seen that some regions show multiple colors in the same region as well as abrupt change in orientation within a grain. This suggests presence of defects that are not seen in film after $CdCl_2$ passivation treatment.



2.38 Microns of twin boundary length per square Micron

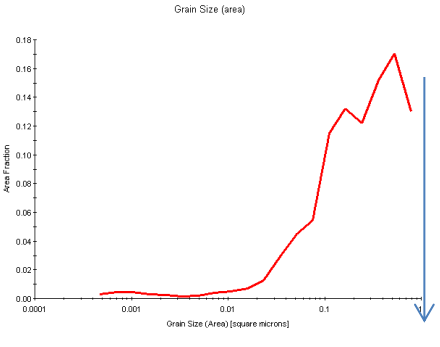


Chart: Grain Size (area)

Edge grains included in analysis

Area [square microns]	Area Fraction
0.000473642	0.00302227
0.000699623	0.00469615
0.00103342	0.00436292
0.00152648	0.00320826
0.00225479	0.00251856
0.00333058	0.00145689
0.00491964	0.00210009
0.00726687	0.00391345
0.010734	0.00502937
0.0158553	0.0073077
0.0234201	0.0124688
0.0345942	0.0291843
0.0510996	0.0449544
0.0754799	0.0543466
0.111492	0.115094
0.164687	0.131965
0.243261	0.122139
0.359325	0.151617
0.530763	0.170503
0.783998	0.130113

Average	
Number	0.0324864
Standard Deviation	0.0989853
Area	0.3337

Boundaries: Twin (Axis-Angle with K1 Plane)

	Plane Normal	Direction	Angle	Tolerance	Phase	K1 Plane	K1 Tolerance	Fraction	Number	Length
—	1 1 1	1 1 1	60°	5°	Cadmium Telluride	1 1 1	1°	0.255	6879	59.57 microns

Figure 6.5 Grain size and defect analysis using EBSD in as deposited CdTe film

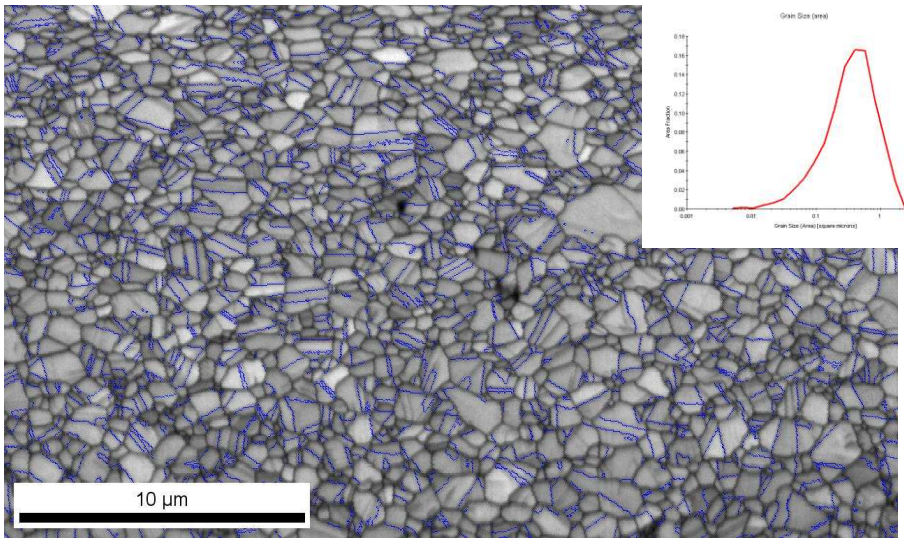


Chart: Grain Size (area)

Edge grains included in analysis

Area [square microns]	Area Fraction
0.00519035	0.000828317
0.00745741	0.00160856
0.0107147	0.00114633
0.0153947	0.00381248
0.0221189	0.00654518
0.03178	0.0107496
0.045661	0.020279
0.065605	0.0317053
0.0942603	0.0481977
0.135432	0.0684655
0.194586	0.104287
0.279578	0.148328
0.401694	0.165848
0.577147	0.16468
0.829236	0.113564
1.19143	0.070651
1.71183	0.0289097
2.45953	0
3.53382	0
5.07733	0.0103946

Average	
Number	0.189297
Standard Deviation	0.255397
Area	0.533764

2.08 Microns of twin boundary length per square Micron area

Boundaries: Twin (Axis-Angle with K1 Plane)

Plane Normal	Direction	Angle	Tolerance	Phase	K1 Plane	K1 Tolerance	Fraction	Number	Length
1 1 1	1 1 1	60°	5°	Cadmium Telluride	1 1 1	1°	0.345	43273	1.25 mm

Figure 6.6 Grain size and defect analysis using EBSD CdTe film after baseline passivation treatment

EBSD analysis of CdTe grains on the surface before (figure 5.5) and after passivation treatment (figure 5.6) shows a significant increase in grain size as the average size goes from ~0.34 μm^2 to ~0.54 μm^2 with passivation treatment. The EBSD map also reveals that average length of twin boundaries reduces from 2.38 $\mu m/\mu m^2$ to 2.08 $\mu m/\mu m^2$ as we go from as deposited to $CdCl_2$ passivated CdTe film. This signifies that not only is there an increase in grain size with $CdCl_2$ passivation treatment but also notable decrease in line defects that may be playing a crucial role in improvement of CdTe device performance.

6.2.3 EFFECT OF $CDCL_2$ PASSIVATION TIME ON CDTE FILM MICROSTRUCTURE. As deposited films have very well defined grains which can be observed in the surface SEM images CdTe. With increase in passivation time there is a gradual change seen in surface morphology of the film. Particularly going from 30 second treatment to 60 second treatment, on close observation, grains can be seen to get more dense. On further continuing the treatment, the surface becomes more homogeneous and voids between the grains appear to reduce. However, surface SEM images do not provide detailed information about the

film microstructure. Therefore, to understand this better, cross section images were collected for some of the same set of samples that are presented in figure 5.8.

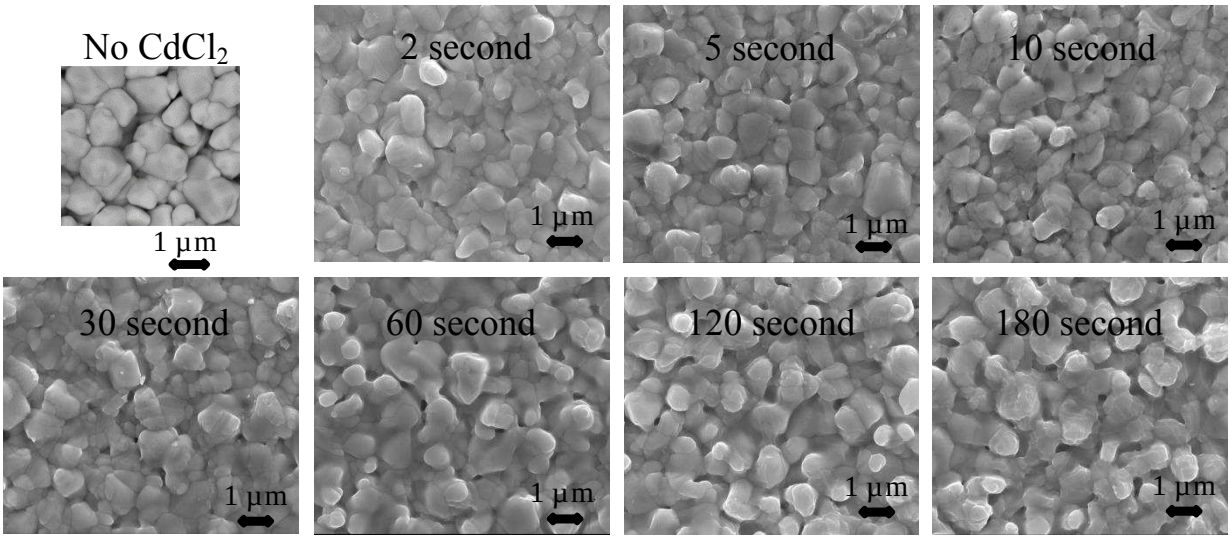


FIGURE 6.7 SEM images of CdTe surface as it changes with $CdCl_2$ passivation time

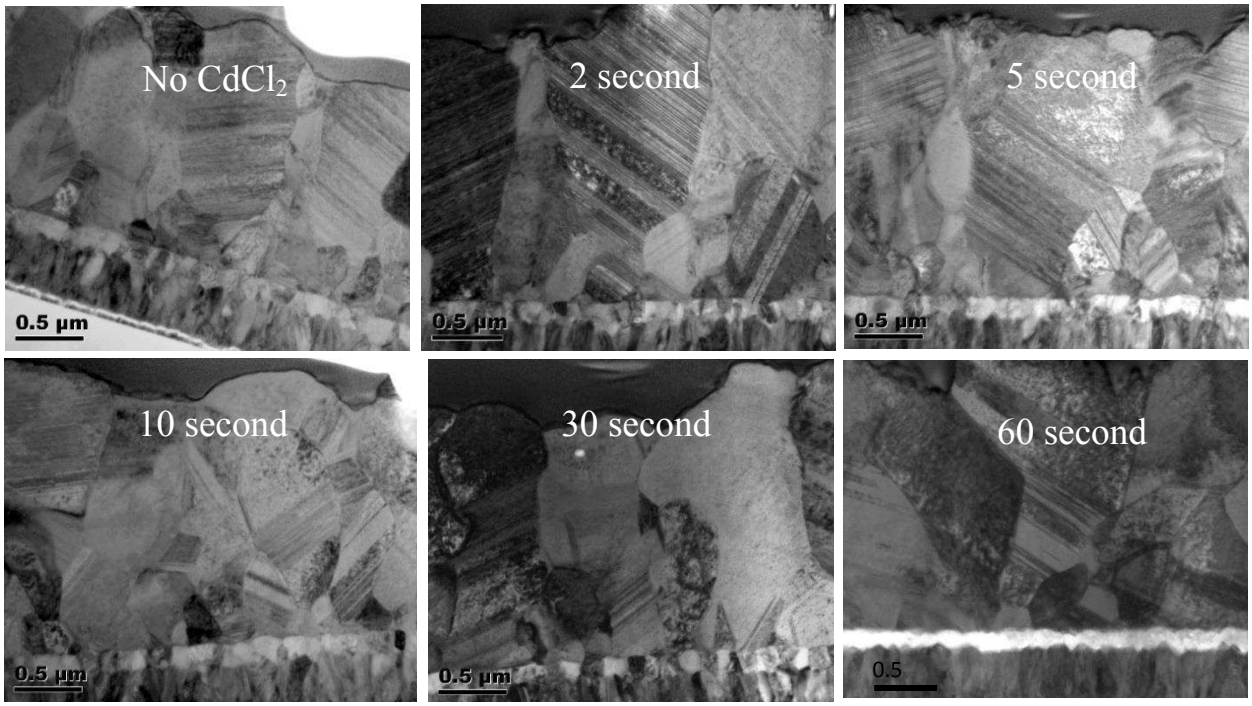


FIGURE 6.8 Cross section TEM images of CdTe film as it changes with $CdCl_2$ passivation time

Cross section TEM images appear to have line defects clearly visible in as deposited films. However, as passivation time for these films is increased, the density of these defects reduces. The grains also seem to be getting larger and morphology appears to be getting cleaner. To achieve a better understanding of

these higher magnification as well as high resolution (atomic resolution) images were studied. Figure 5.6 shows higher magnification of one of the grains which shows large density of defects in an as deposited CdTe film without $CdCl_2$ passivation treatment. On looking at a higher magnification image stacking faults are visible in large grains.

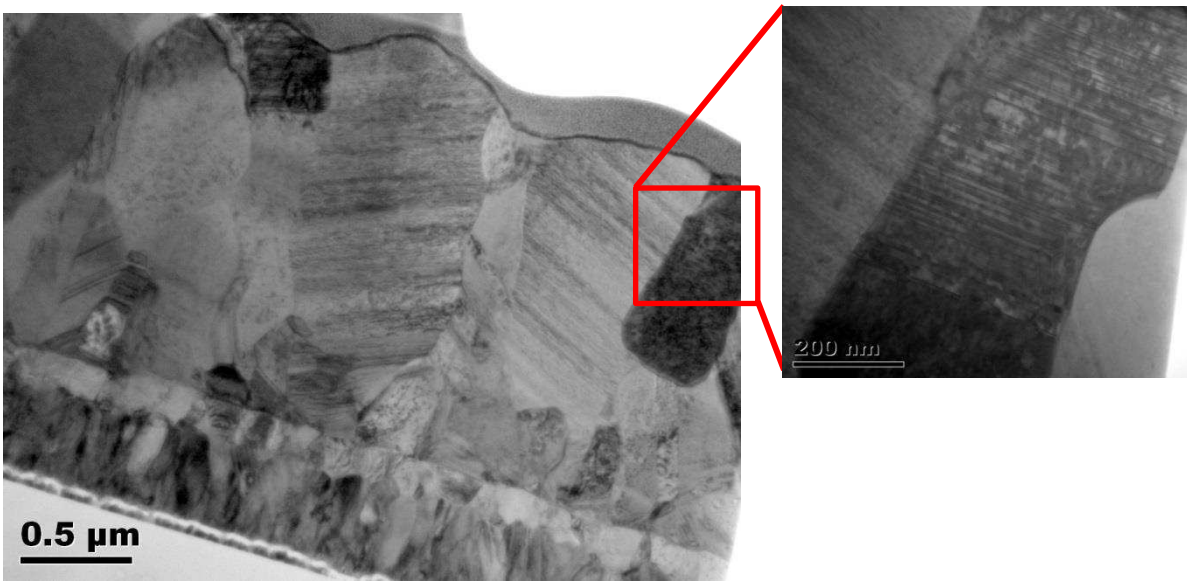


FIGURE 6.9 Cross section TEM images of as deposited CdTe film with higher magnification of a region showing stacking faults

Further investigation of these linear defects and what happens to them after passivation was of most interest. And therefore, high resolution TEM images were studied.

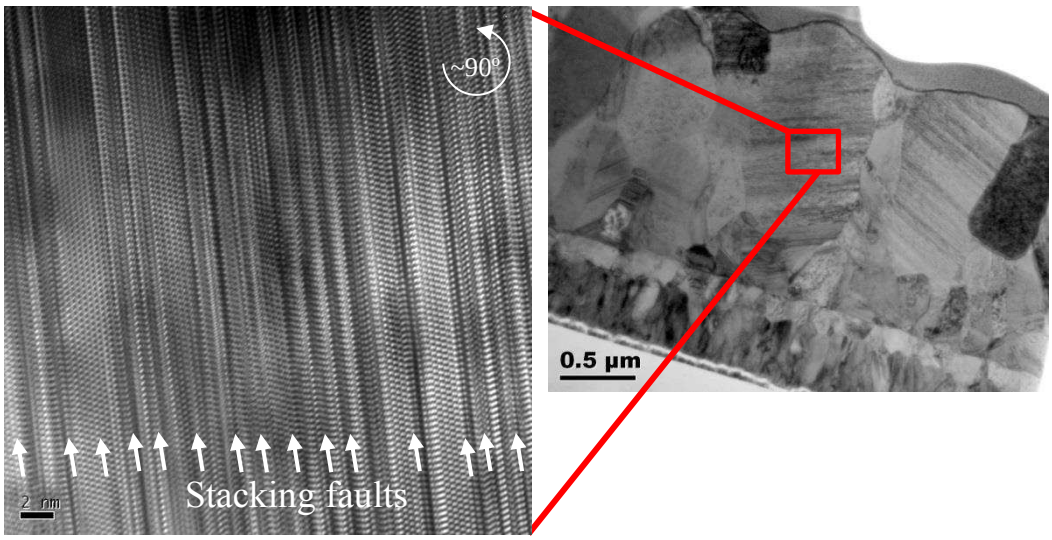


FIGURE 6.10 HRTEM image of a region within the grain reveals definitive signs of high density of linear defects seen in CdTe grains (twins and stacking faults) in as deposited CdTe film

HRTEM image confirms the presence of stacking faults in as deposited films that did not undergo $CdCl_2$ passivation treatment. It is also observed in another HRTEM image captured post $CdCl_2$ passivation treatment shows no stacking faults but twin boundaries still persist.

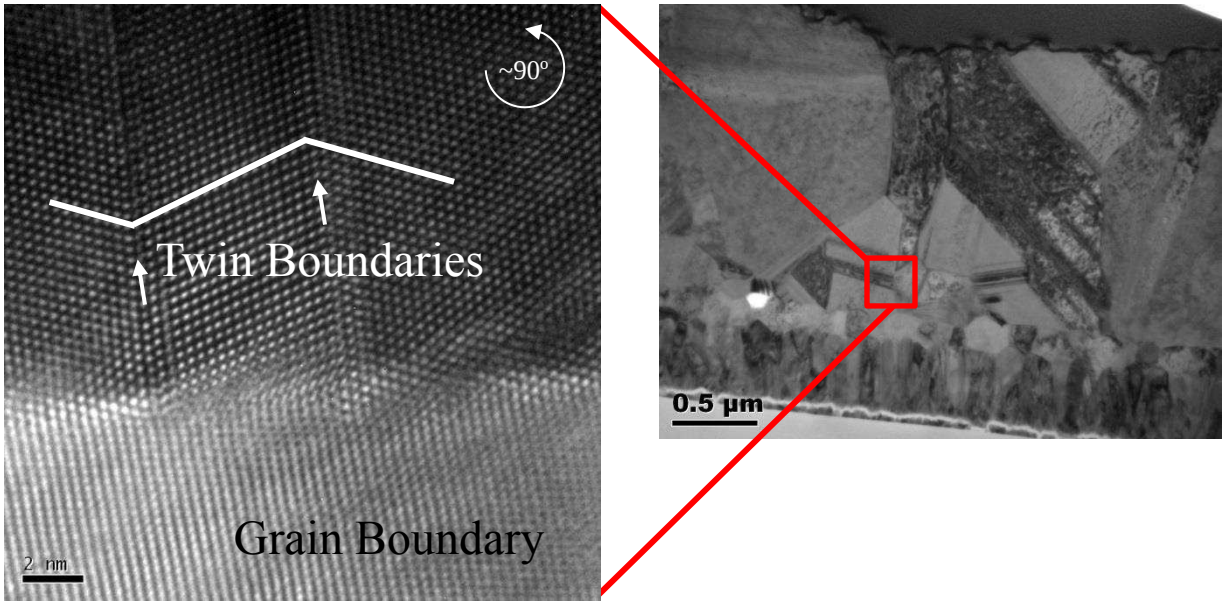


FIGURE 6.11 HRTEM image of a region within the grain reveals definitive signs of twin boundary after $CdCl_2$ passivation treatment.

To summarize, baseline samples without $CdCl_2$ passivation treatment have high density of stacking faults and twin boundaries. Passivation treatment removes stacking faults but twin boundaries continue to persist. These twin boundaries are clearly visible in TEM images as well as EBSD map and can be confirmed with HRTEM images. There is a significant increase in average grain size observed after passivation treatment that may be observed in grain size analysis performed using EBSD.

6.3 ELECTRICAL CHARACTERIZATION OF BASELINE CDTE FILMS

Table 2.
Electrical Performance of Baseline Devices.

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%Η
Baseline CdTe, No Passivation	531	8.5	34.3	1.5
Baseline CdTe, Baseline Passivation	790	20.6	72.2	11.8

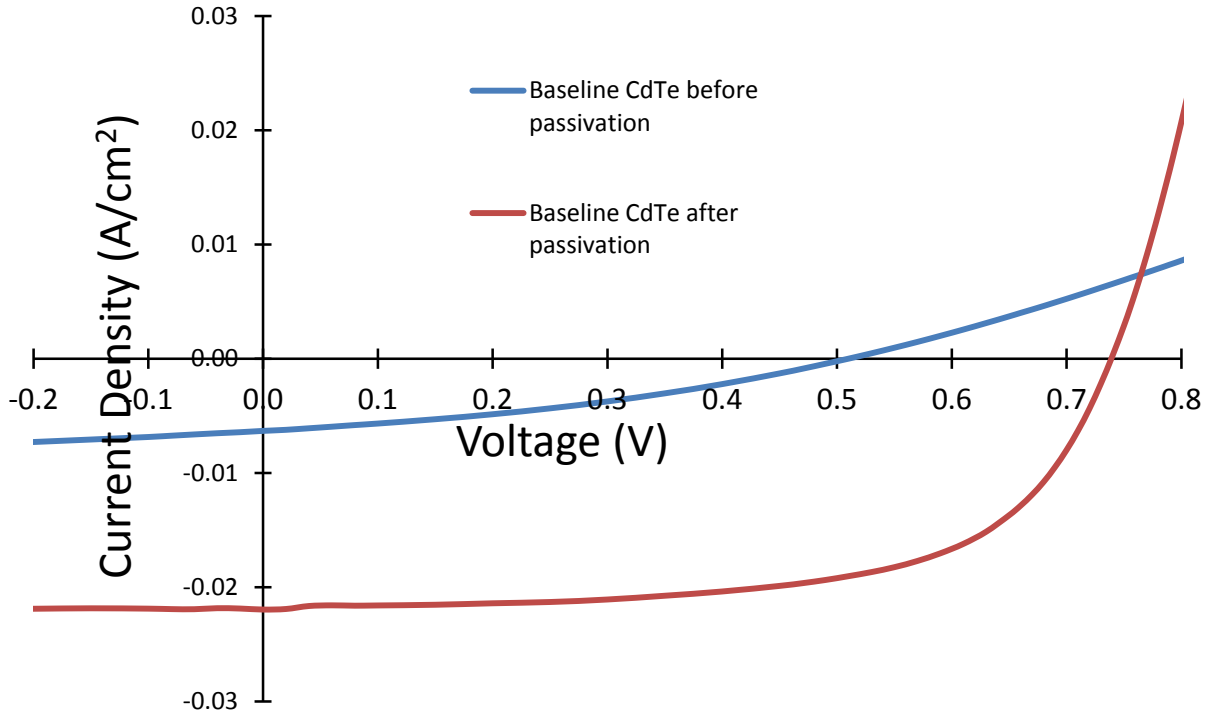


FIGURE 6.12 Current density v/s Voltage plot showing effect of $CdCl_2$ passivation treatment on electrical performance of CSS CdTe thin film devices

Table 1 shows the electrical measurements of the baseline CdTe cells with and without $CdCl_2$ passivation treatment. There is a drastic improvement in cell device performance after baseline $CdCl_2$ treatment is performed as compared to cells fabricated from as deposited CdTe films without any passivation treatment. There is a notable improvement in open circuit voltage, short circuit current and fill factor. All combined improve the efficiency of the device by almost an order of magnitude. Relating this to the observations made with materials characterization, it can be said that presence of stacking faults and smaller grain in CdTe film have a detrimental effect on the device performance. Removing these stacking faults and improving grain size results in considerable improvement in performance of devices made from such films.

CHAPTER 7 CHARACTERIZATION OF EFFECTS OF TEMPERATURE ON CDTE FILMS AND DEVICES

7.1 VARYING CDTE AND CDS DEPOSITION TEMPERATURE

7.1.1 HIGHER TEMPERATURE CDTE AND CDS DEPOSITION. To understand the effect of substrate temperature during deposition on device performance and structure, cells was fabricated with CdS deposited at 505ºC instead of 440ºC and CdTe deposited at 510ºC instead of 445ºC which were 65ºC higher than the baseline substrate temperature.

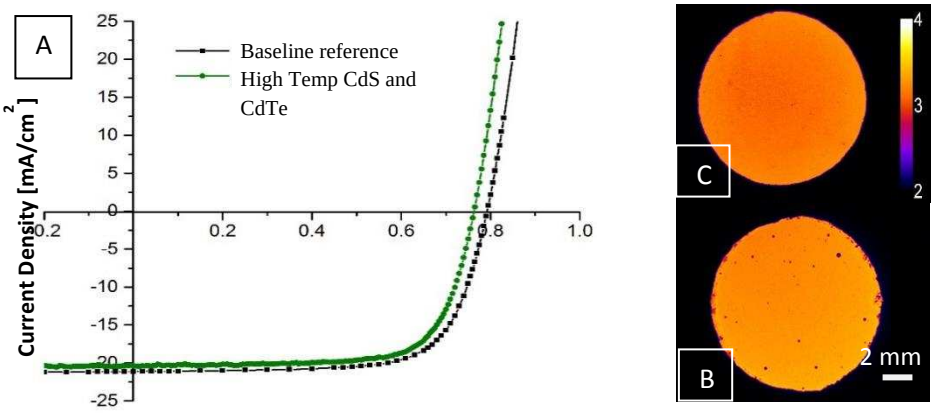


FIGURE 7.1 Current density vs. voltage plot(A), electroluminescence image of device made with CdS and CdTe deposited at higher temperature (B) and baseline device (C)[20].

Electrical characterization of the devices deposited at 65ºC higher subtrate temperature during CdTe and CdS deposition showed a decrease in open circuit voltage (V_{OC}) and short circuit current (J_{SC}) as well as efficiency when compared to samples deposited at standard conditions. Fill factor was similar to standard devices was measured on these devices. A summary of electrical measurements can be seen in Table 3.

Table 3

Electrical Performance of Devices with CdTe and CdS Deposited at 100°C Higher Substrate Temperature

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%η
Baseline reference device	790	20.6	72.2	11.8
High temp CdTe and CdS	763	20.5	72.7	11.3

7.1.2. HIGHER TEMPERATURE CDS AND BASELINE CDTE DEPOSITION. In earlier experiments it was observed that devices with higher substrate temperature for CdS and CdTe deposition gave slightly worse performance than all standard conditions. In an attempt to isolated the cause of the change, films were therefore deposited at 505ºC substrate temperature for CdS and while the CdTe was deposited under baseline deposition conditions. As before the baseline $CdCl_2$ passivation treatment was applied to the film stack.

The cells were analyzed before and after the $CdCl_2$ passivation treatment. Surface SEM image showed a good CdTe coverage on the surface (figure 7.2C). However, the grains appeared to have a different texture as compared to films deposited under standard conditions (Figure 5.3). The CdTe coverage appeared to be very uniform with no pin holes or voids on the surface. Surface SEM images showed smaller CdTe grains than baseline samples that were not very well defined. Cross section BF-STEM micrograph of these films showed that there were multiple grains stacked on top of one another creating several grain boundaries between CdTe/CdS interface and the CdTe back surface (figure 7.2D). Earlier, CdTe layer did not show signs of any stacking faults but there were twin boundaries present when deposited on CdS at baseline temperature. These grain boundaries may be responsible for impeding charged carriers resulting in reduced device performance.

To get a better understanding of CdS deposited at 505ºC substrate temperature and SEM of CdS layer without CdTe deposited on it was studied.

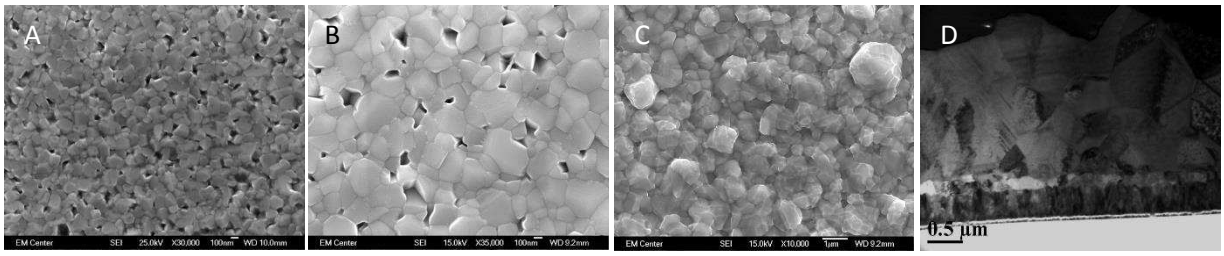


FIGURE 7.2 Surface SEM of CdS deposited at baseline substrate temperature (A) and higher substrate temperature (B) Surface SEM (C) and cross section BF-STEM micrograph (D) of films with CdS deposited at 505ºC and CdTe at baseline substrate temperature.

Comparing CdS film using surface SEM micrograph showed the grains in films deposited at baseline temperature had smaller grains than in the films deposited at 505ºC. Larger grains in the CdS layer might have allowed more nucleation sites during CdTe deposition which may explain several smaller grains in the CdTe film grown on CdS deposited at 505ºC.

EL images of these devices were also collected (figure 7.3B). These images showed reduced EL intensity as compared to baseline sample. In addition, there were dead spots that were observed. Further electrical characterization was carried out. They showed a marginally higher short circuit current as compared to standard devices. Efficiency was similar to standard devices but there was a substantial drop in open circuit voltage and fill factor. Summary of electrical characterization based on the current density vs. voltage plot can be seen in the table III below:

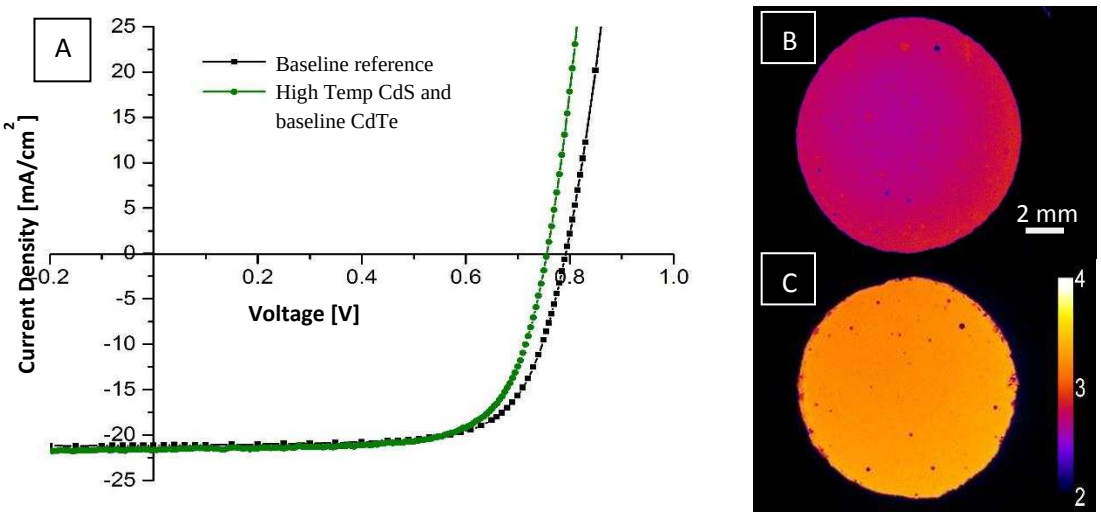


FIGURE 7.3 Current density vs. voltage plot (A), electroluminescence image of baseline CdS/CdTe cell (B) as compared to cell with CdS layer deposited at 505ºC substrate temperature and CdTe deposited at standard substrate temperature (C)[20].

Table 4
Electrical Performance of Devices with CdS Deposited at 505ºC Substrate temperature and baseline CdTe Deposition Temperature

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%Π
Standard Sample, Standard Passivation	790	20.6	72.2	11.8
High temp CdTe and CdS, Standard Passivation	756	21.6	70.4	11.5

7.1.3 LOWER TEMPERATURE CDTE AND BASELINE CDS DEPOSITION. To understand the effect of substrate temperature on device performance, cells were fabricated with CdTe deposited at 345ºC which was 100ºC lower than the baseline substrate temperature during deposition. The cells were analyzed before and after the $CdCl_2$ passivation treatment to ensure that they follow the same performance trend as baseline samples. Films without the passivation treatment showed highly columnar CdTe grains, as well as a high density of smaller grains nucleating above the CdS layer (figure 7.4C). Also, voids at the CdTe free surface go deep between CdTe grains which may act as sites for chlorine accumulation when $CdCl_2$ passivation was carried out. Performing standard $CdCl_2$ treatment on the same films show grain growth and reduction in stacking faults. It was also observed that there were CdTe grains stacked one over the other forming multiple grain boundaries. These grain boundaries could potentially have a negative impact on performance by impeding charge carriers. Surface SEM showed CdTe films had a morphology different from baseline films with smaller grains that were more distinct (figure 6.4A and 6.4B).

Electroluminescence image of cells deposited at low substrate temperature that underwent a standard $CdCl_2$ passivation treatment show lower intensity and substantial non-uniformity (figure 7.5B). Cells without $CdCl_2$ passivation have very low signal intensity under EL test and therefore does not produce an image projectable on a logarithmic scale. The dark spots observed in the baseline cell were dead spots. Cell deposited at lower substrate temperature shows some regions that was bright and have darker center corresponding to poor performance.

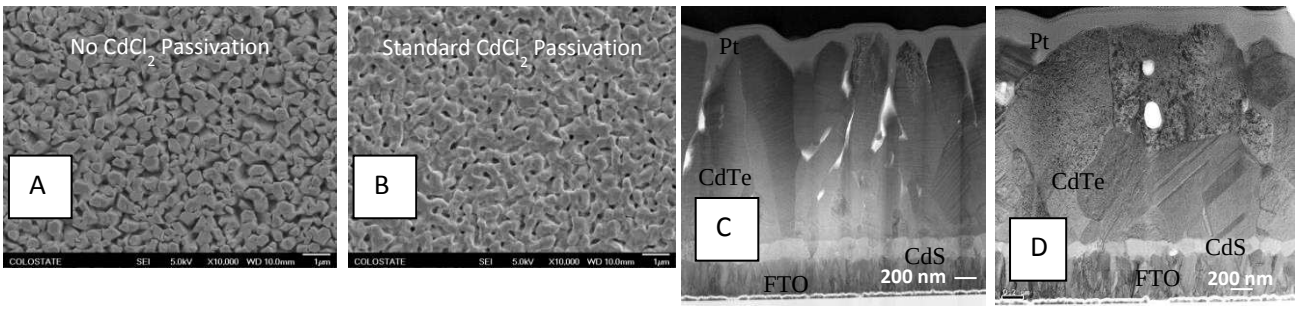


FIGURE 7.4 Surface SEM (A, B) and cross section BF-STEM (C, D) micrograph showing effect of $CdCl_2$ passivation on stacking fault and grain structure in CdTe grains in low temperature samples.

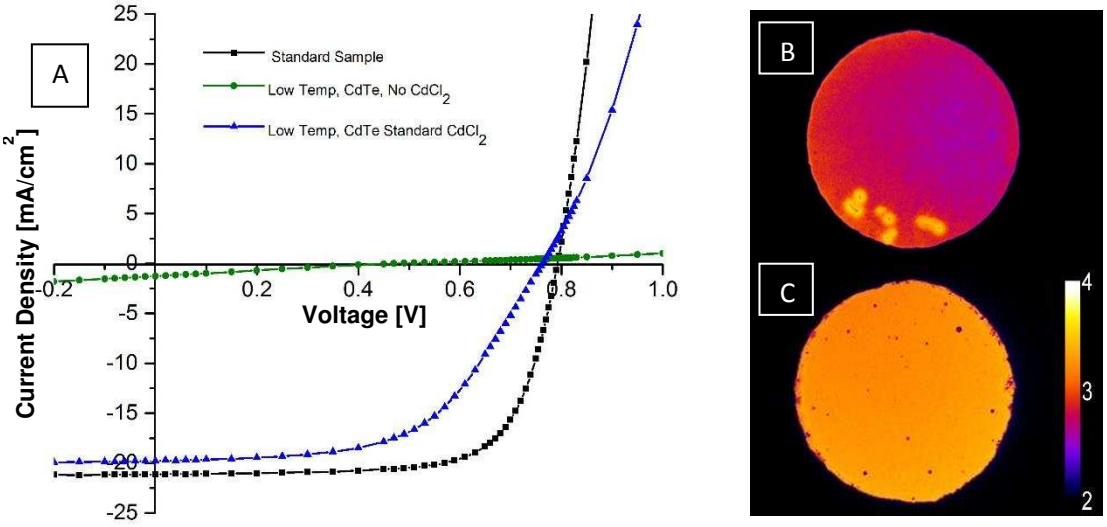


FIGURE 7.5 Current density vs. Voltage for cells with CdTe layer deposited at lower substrate temperature (A). Electroluminescence image of standard CdS/CdTe cell (B) as compared to cell with absorber CdTe deposited at lower substrate temperature (C).

Table 5
Electrical Performance of Low Temperature Devices

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%ƞ]
Standard Sample with Standard Passivation	790	20.6	72.2	11.8
Low Temp CdTe, No Passivation	474	12.7	23.1	1.4
Low Temp CdTe, Standard Passivation	763	19.8	56.2	8.5

7.1.4 HIGHER TEMPERATURE CDTE AND BASELINE CDS DEPOSITION. CdTe films were deposited at 510ºC substrate temperature that was 65ºC hotter than baseline on baseline CdS films. Such films had a 10ºC hotter $CdCl_2$ passivation since the substrate went in to $CdCl_2$ source at a higher temperature.

Cross section transmission electron micrographs of CdTe grains deposited at 510ºC are shown in figure 7. Large densities of stacking faults were observed in film that did not undergo $CdCl_2$ passivation treatment. However, standard passivation treatment causes grain growth in CdTe absorber layer, reduces stacking faults and smaller CdTe grains at CdTe/CdS interface seemed to have combined to form larger grains.

CdTe films deposited at higher temperature on baseline CdS also showed larger grains before $CdCl_2$ passivation treatment. Unlike lower deposition temperature samples, these films had comparatively larger grains and did not show signs of voids at the grain boundary.

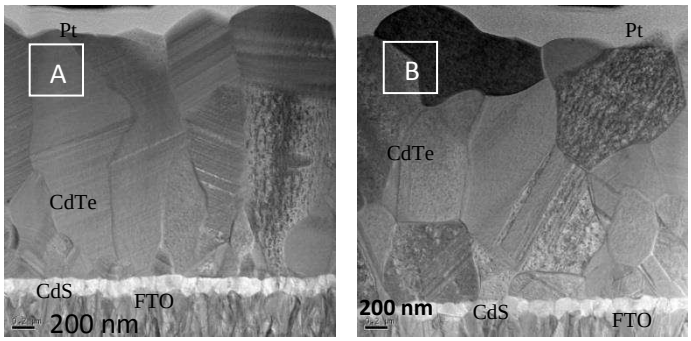


FIGURE 7.6 Cross section BF-STEM micrograph showing effect of higher deposition temperature on CdTe grains without $CdCl_2$ passivation (A) and with $CdCl_2$ passivation (B).

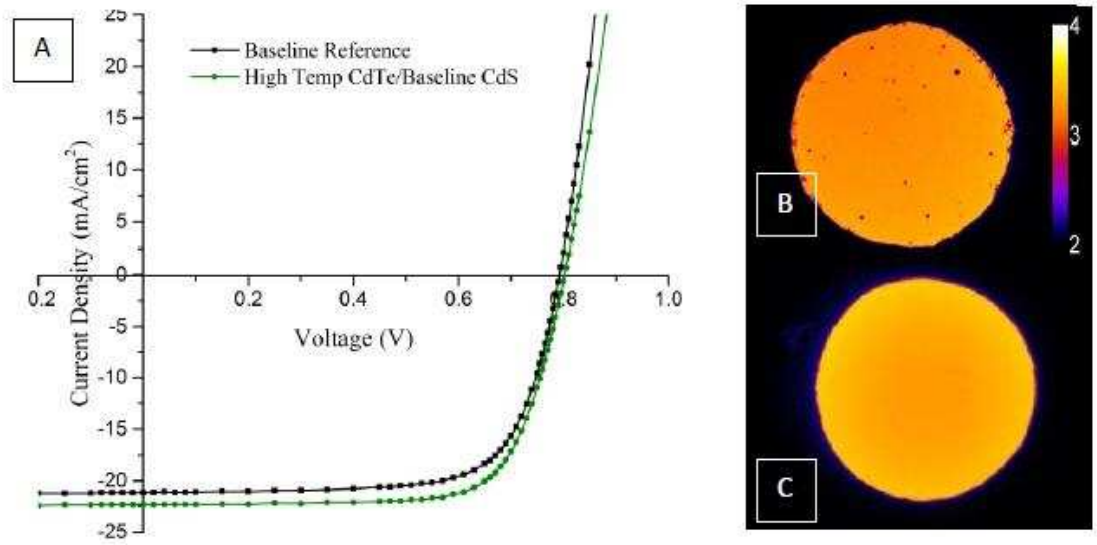


FIGURE 7.7 Current density vs. Voltage for cells with films deposited at 510ºC substrate temperature with $CdCl_2$ passivation treatment compared to a baseline sample (A). Electroluminescence image of standard CdS/CdTe cell (B) as compared to cell made from film deposition at 510ºC (C)

$CdCl_2$ treatment of the films substantially improved cell performance when compared to films without any $CdCl_2$ treatment as is observed in all other cases. Cells prepared from films that had CdTe deposited at 510ºC substrate temperature had fill factor similar to baseline device while a substantial increase in open circuit voltage and short circuit current were observed. As a result it also showed improvement in device efficiency. Electroluminescence images of such films show increase in signal

intensity as well as uniformity (figure 8C). There are no dark spots observed in such devices which suggest absence of dead spots.

Table 5 below summarizes the above mentioned observations that provide a better understanding of the cell performance.

Table 6
Electrical Performance of Devices with CdS Deposited at Higher Substrate temperature and Standard CdTe Deposition Temperature

7.2. Observations Summary

When CdTe and CdS were deposited at higher substrate temperature as compared to standard deposition conditions, a drop in V_{OC} and fill factor was observed. Further analysis of CdS film microstructure showed larger CdS grains when deposited at higher temperature. When CdS was deposited at higher substrate temperature and keeping CdTe deposition at baseline conditions, there was an improvement in J_{SC} but drop in V_{OC} and fill factor. Both these devices showed lower efficiencies compared to baseline devices.

Lower substrate temperature for CdTe deposition had a detrimental effect on device performance that could be related to film microstructure. Lower substrate temperature during CdTe deposition formed high concentration of small CdTe grains at the interface of CdTe and CdS that had detrimental effect on cell performance. This also resulted in high density of longitudinal voids between the CdTe grains that extended through a large portion of the thickness of the CdTe film.

Films with higher substrate temperature with hotter passivation treatment gave improved V_{OC} and fill factor. Higher substrate temperature during CdTe deposition formed larger grains that could be related to better device performance. These cells also exhibited the best uniformity within the scope of this study as was seen in the electroluminescence image along with higher V_{OC} and fill factor.

Study of varying temperature condition for CdS and CdTe layer showed that higher temperature CdS formed larger CdS grains and had a detrimental effect on device performance. CdTe deposited at higher substrate temperature showed positive effect on device performance with improvement in V_{OC}, J_{SC} and fill factor being observed. Longer passivation treatment of CdTe to films was not attempted since it is known lower performance of devices possibly due to accumulation of $CdCl_2$ at grain boundaries, voids and CdTe/CdS interface.

CHAPTER 8 CHARACTERIZATION OF CDTE ON $MG_{1-X}ZN_XO$ WINDOW LAYER

8.1 WHY $MG_{1-x}ZN_xO$ INSTEAD OF CDS?

It was observed when CdTe was deposited at 65ºC higher substrate temperature there was a substantial improvement in CdTe device performance. In an attempt to further improve the device performance and to characterize higher performance CdTe films an experiment was planned to deposit CdTe at 150ºC higher temperature i.e. 600ºC substrate temperature. The issue encountered during deposition at such high temperature was that CdS would begin to resublime at such elevated temperatures. Several attempts were made to alter the process to avoid this resublimation of CdS and make a good performing CdTe device. However, there was no success and devices continued to be poor due to poor film quality. In recent months, $Mg_{1-x}Zn_xO$ was identified as a highly competent material for use as a window layer. Being an oxide deposited using sputter deposition method; it is $Mg_{1-x}Zn_xO$ is known to be highly stable at elevated temperatures. Moreover, it comes with an added advantage of greater transmission since unlike CdS it does not absorb large amount of blue light from visible solar spectrum. With these extraordinary characteristics, $Mg_{1-x}Zn_xO$ had to be investigated as a candidate for this

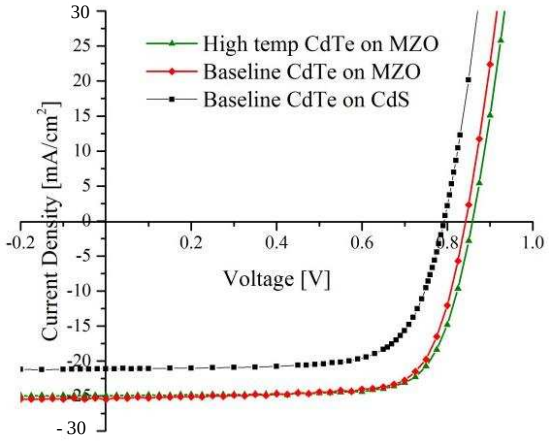


FIGURE 8.1 Current density vs Voltage for cells with varying parameters on CdS and $Mg_{1-x}Zn_xO$ window layer

application and good device performance was expected with higher J_{SC} as well as improvement in fill factor and V_{OC} leading to higher device efficiency.

With expectation for better device performance, 2.4 µm thick CdTe films were deposited on 40 nm thick $Mg_{1-x}Zn_xO$ layer at 600ºC substrate temperature.

8.2 Preliminary Materials Characterization of CdTe on $Mg_{1-x}Zn_xO$

Use of higher temperature deposition of CdTe on $Mg_{1-x}Zn_xO$ showed very promising results. To get an understanding of the effect of high temperature substrate on CdTe film deposited on $Mg_{1-x}Zn_xO$, three films were sectioned using FIB to be imaged under TEM and get some EDX chemical mapping performed. These were baseline CdTe deposition on $Mg_{1-x}Zn_xO$ with no $CdCl_2$ passivation, baseline CdTe deposition on $Mg_{1-x}Zn_xO$ with baseline $CdCl_2$ passivation and 150ºC hotter CdTe depositions on $Mg_{1-x}Zn_xO$. Results from these images are discussed in the following sections. These are very preliminary results and further investigation is being planned.

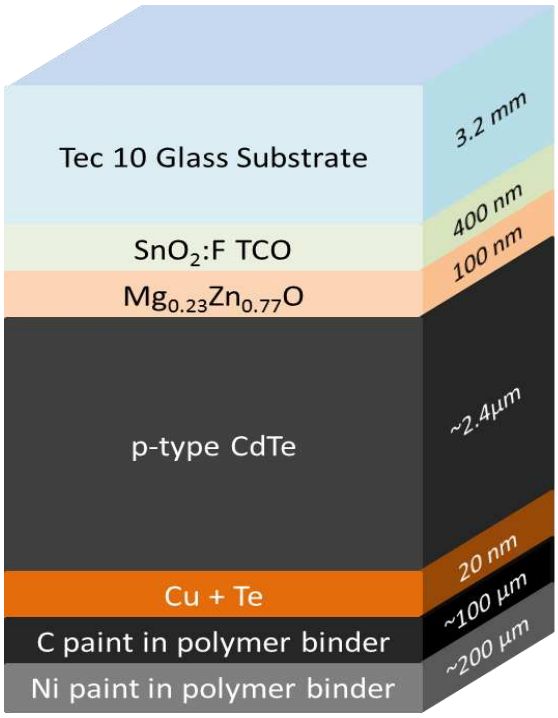


Figure 8.2 Schematic diagram (not to scale) of a baseline CdTe deposited on $Mg_{1-x}Zn_xO$ window layer

8.2.1 BASELINE CDTE DEPOSITION ON $MG_{1-x}ZN_xO$ WITH NO $CDCL_2$ PASSIVATION. As per expectations, TEM images showed good clear interface between $Mg_{1-x}Zn_xO$ and CdTe. The coverage of $Mg_{1-x}Zn_xO$ on

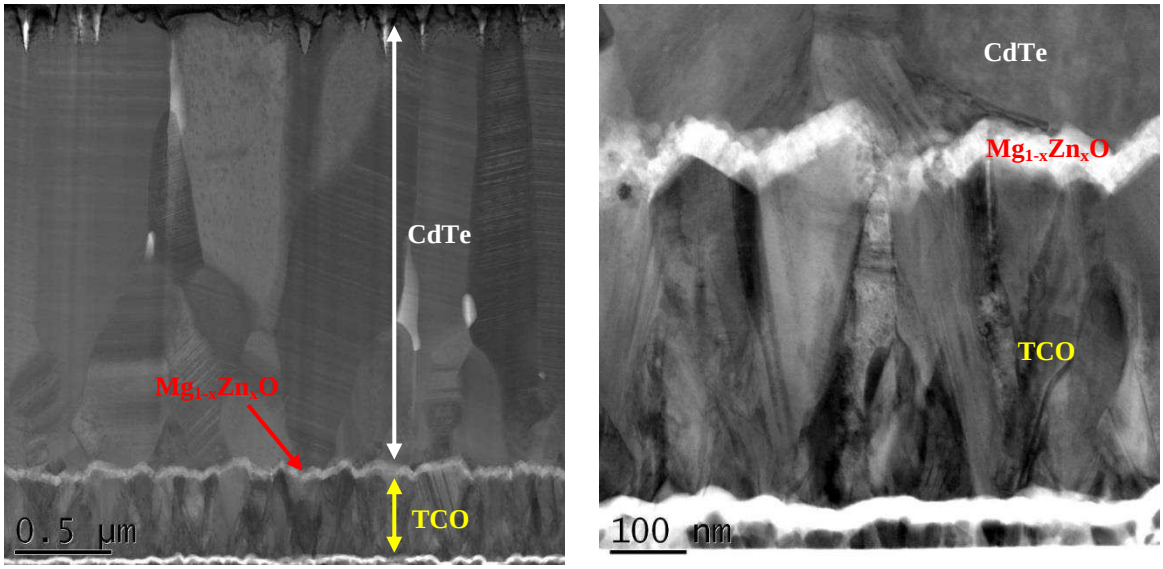


FIGURE 8.3 Cross section BF-TEM image of baseline CdTe deposited on $Mg_{1-x}Zn_xO$ window layer (left) and higher magnification BF-TEM image of CdTe/$Mg_{1-x}Zn_xO$/TCO interface (right) before $CdCl_2$ passivation

TCO was seen to be uniform and conformal to the morphology of the TCO layer. $Mg_{1-x}Zn_xO$ grains were not distinctly visible at this magnification and further work on that is in progress. CdTe grains appeared to be columnar before $CdCl_2$ passivation treatment and had very high density of stacking faults. Some voids were visible between the CdTe grains and surface of CdTe had some voids that went upto ~100 nm within the film. To get a better understanding of material distribution EDX spot analysis was performed that can be seen in figure 8.4.

EDX spot analysis was performed at several points in the CdTe and $Mg_{1-x}Zn_xO$ layer. Peaks at various spots showed that there was no diffusion of materials between the layers within measureable limits.

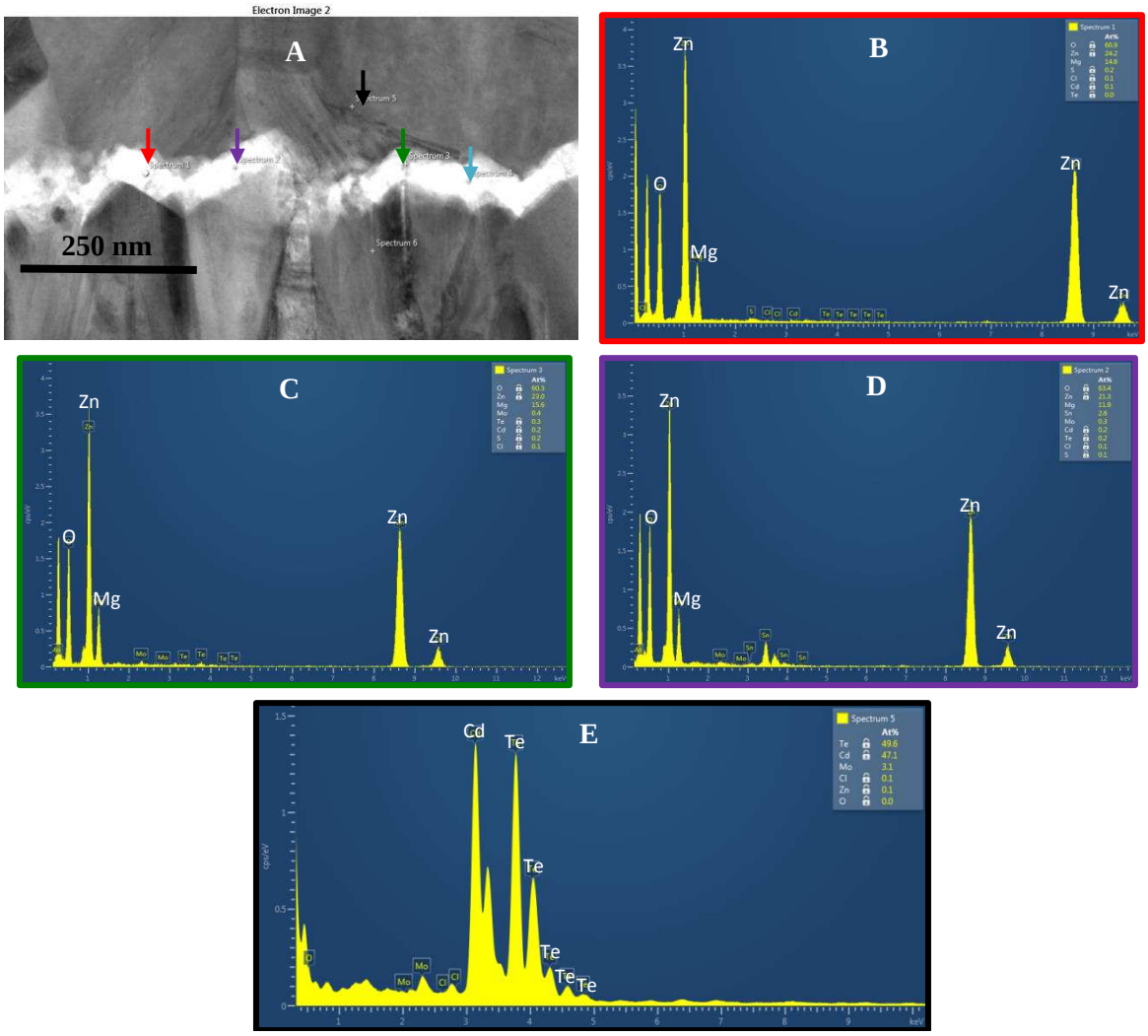


FIGURE 8.4 Cross section BF-TEM image of baseline CdTe deposited on $Mg_{1-x}Zn_xO$ window layer before $CdCl_2$ passivation treatment [A] and EDS spot analysis color coded to match the frame [B-E]

8.2.2 BASELINE CDTE DEPOSITION ON MG1-XZNXO WITH BASELINE $CDCL_2$ PASSIVATION. After baseline passivation treatment was carried out on the CdTe films deposited on $Mg_{1-x}Zn_xO$ window layer it was found that $Mg_{1-x}Zn_xO$ layer continued to be conformal to the TCO surface. The CdTe grains were much larger than the ones seen with CdS as the window layer. There were maximum of two layers of CdTe grains from the $Mg_{1-x}Zn_xO$/CdTe interface to the CdTe surface. EBSD measurements will be performed on these films to find precisely how much larger these grains are on an average as compared to the grains seen in films deposited on CdS window layer. To add to the understanding, EDX spot analysis was performed within the CdTe and $Mg_{1-x}Zn_xO$ films near their interface to find signs of material diffusion.

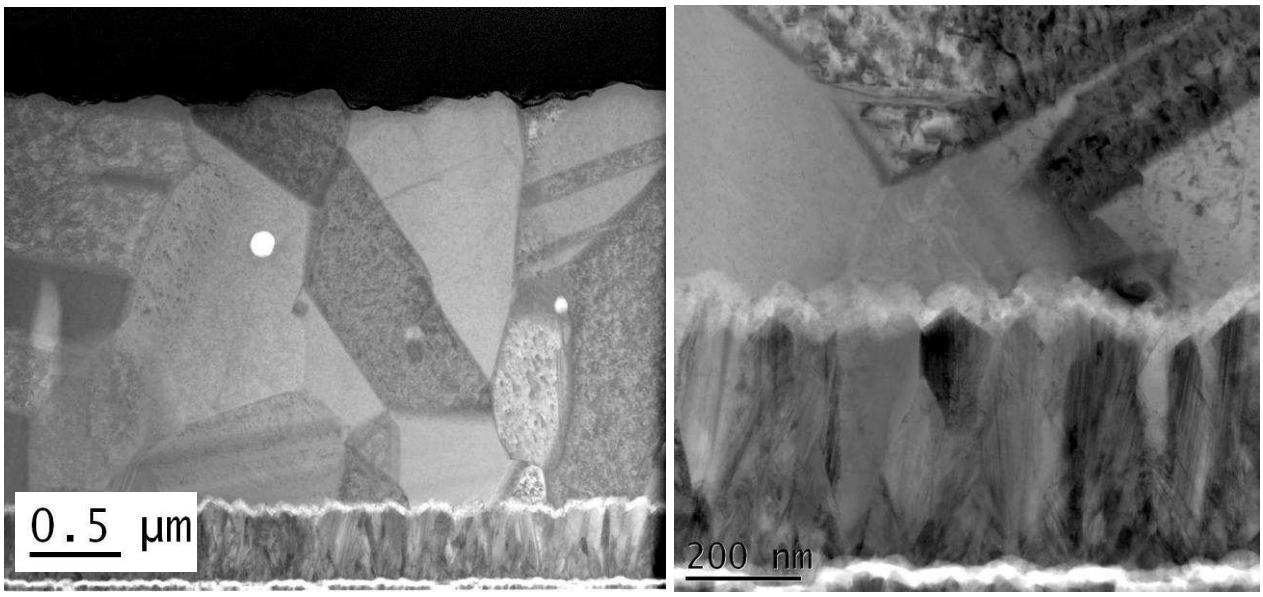


FIGURE 8.6 Cross section BF-TEM image of baseline CdTe deposited on $Mg_{1-x}Zn_xO$ window layer (left) and higher magnification BF-TEM image of CdTe/$Mg_{1-x}Zn_xO$/TCO interface (right) after $CdCl_2$ passivation

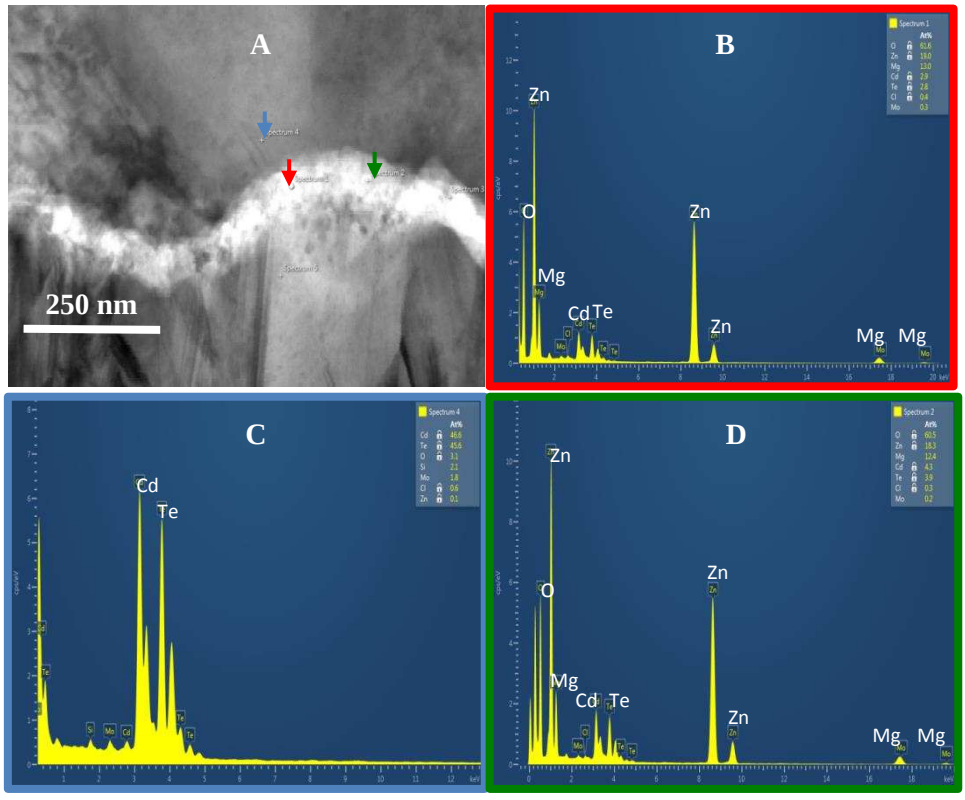


FIGURE 8.5 Cross section BF-TEM image of baseline CdTe deposited on Mg1-xZnxO window layer after $CdCl_2$ passivation treatment [A] and EDX spot analysis color coded to match the plot frame [B-D]

EDX analysis showed some diffusion of Cd and Te into the $Mg_{1-x}Zn_xO$ layer but this might be an error. The BF-TEM image shows signs of drifting of the image right in the region where the spots for analysis were selected. Another iteration of EDX analysis of similar spots will be performed to make more clear observations.

8.2.3 HIGH TEMPERATURE CDTE DEPOSITION ON MG1-XZNXO WITH CDCL2 PASSIVATION. The goal of using $Mg_{1-x}Zn_xO$ as a window layer was to make sure that the window layer does not resublime on exposure to high temperature. The J-V plot showed that the performance of these cells was good and that implied that the $Mg_{1-x}Zn_xO$ layer had survived exposure to such high temperature. But it was important to study this from materials perspective. TEM imaging was performed for these films and material distribution was studied using EDX spot analysis as well as chemical maps. With TEM images very large CdTe grains were identified. At some sites there were single large grains that went from the $Mg_{1-x}Zn_xO$/CdTe interface upto the CdTe surface. These grains were at least 2.4 µm tall. On other locations there were maximum of two grains stacked on one another. The densities of line defects were also identified to be low. Figure 7.7 shows one such region of a CdTe film deposited at 600ºC substrate temperature.

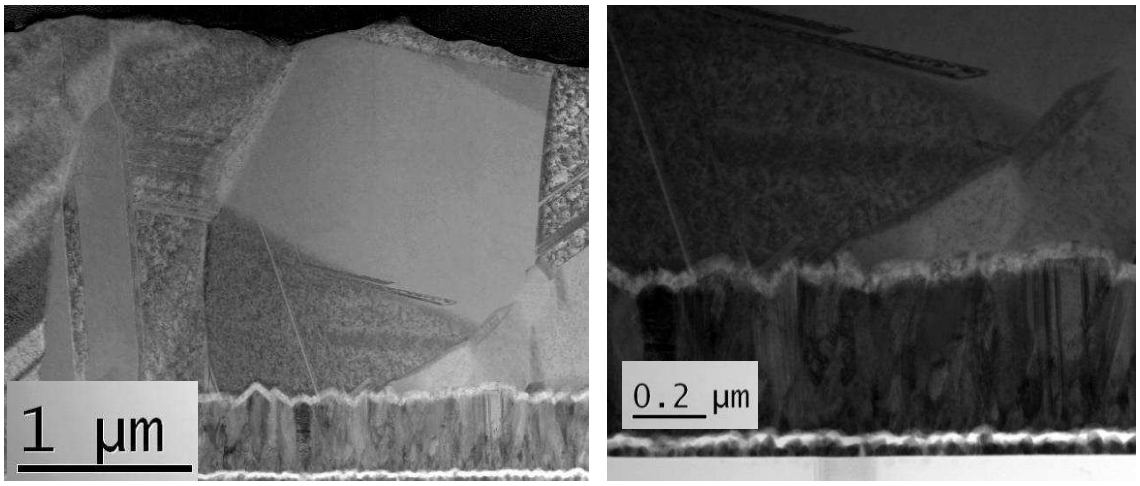


FIGURE 8.7 Cross section BF-TEM image of high temperature CdTe deposited on $Mg_{1-x}Zn_xO$ window layer (left) and higher magnification BF-TEM image of CdTe/$Mg_{1-x}Zn_xO$/TCO interface (right) after $CdCl_2$ passivation

EDX spot analysis once again provided good understanding of the film behavior. There were two spots identified very close to the $Mg_{1-x}Zn_xO$/CdTe interface, one in CdTe layer and another within the $Mg_{1-x}Zn_xO$ layer. Analysis revealed that the spot within the $Mg_{1-x}Zn_xO$ layer did not have any Cd or Te contamination from the CdTe bulk.

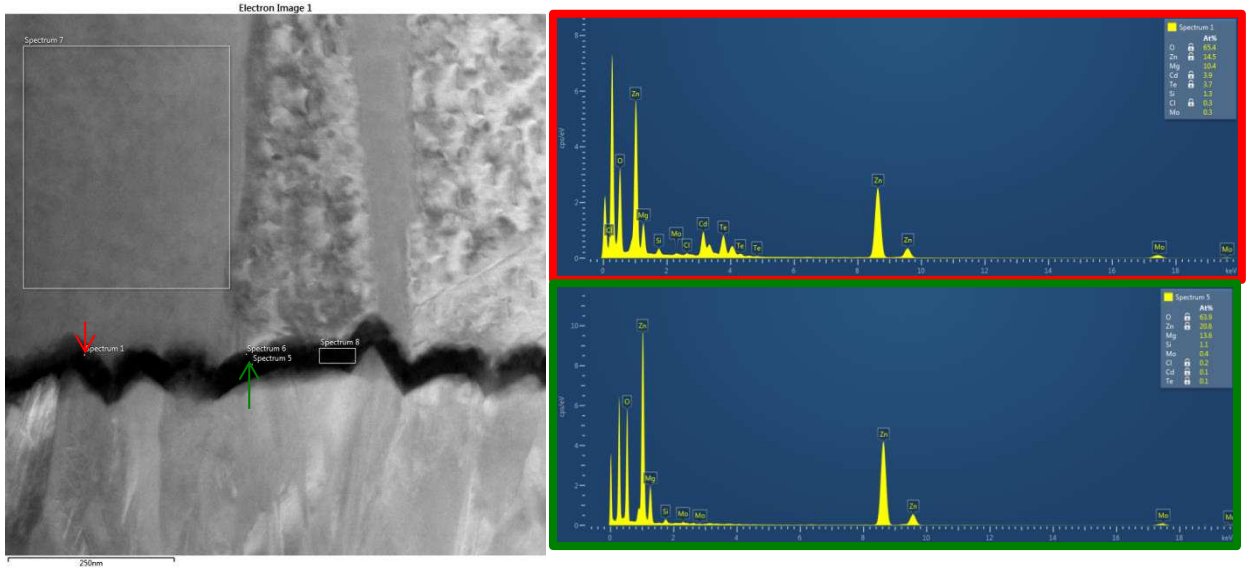


FIGURE 8.8 Cross section BF-TEM image of baseline CdTe deposited on $Mg_{1-x}Zn_xO$ window layer after $CdCl_2$ passivation treatment [A] and EDX spot analysis color coded to match the plot frame [B-D]

The spot right at the interface showed some CdTe and mostly Mg, Zn and O. More spots must be looked at to get a better understanding. In addition to these spot analyses using EDX, we also collected an EDX chemical map to visualize the material distribution within the film. This chemical map can be seen in figure 8.9.

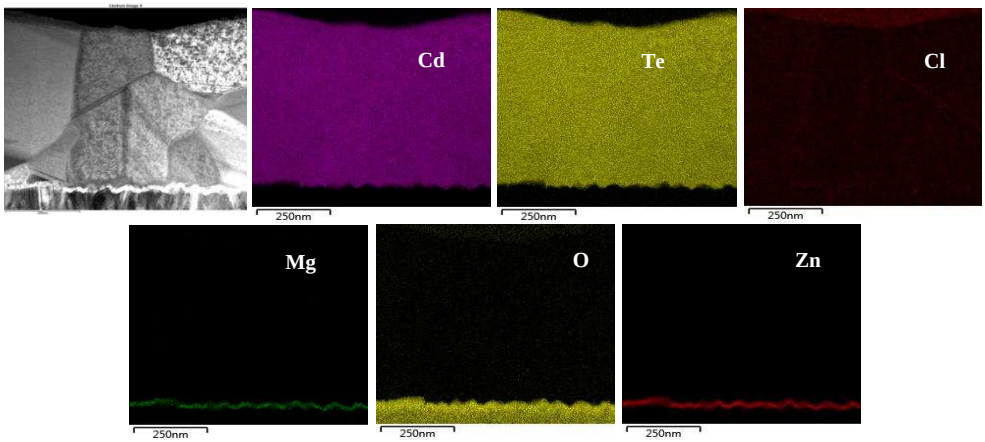


FIGURE 8.9 BF-SEM image and EDX chemical map of CdTe films with ~100 nm MgZnO buffer layer after $CdCl_2$ passivation treatment

EDX chemical map shows very distinct layers of TCO, $Mg_{1-x}Zn_xO$ and CdTe. It also clearly shows Cl decorating the grain boundaries of CdTe grains. In case of CdS, it is very common to find sulfur diffusion in to the CdTe layer. The possibility of Mg or Zn diffusion into the CdTe film from $Mg_{1-x}Zn_xO$ was being considered initially. But there is no such diffusion observed within the detection limits of EDX system.

Though further investigation is necessary, all current results point at $Mg_{1-x}Zn_xO$ absorber and CdTe film deposited at higher substrate temperature to be very promising combination of material for CdTe based thin film photovoltaics. Materials study shows good interfaces and distinct layers as well as no interlayer diffusion of material. Increase in V_{OC} of these films suggests an increase in recombination lifetime of the absorber material which may be important for higher efficiency of CdTe with $Cd_{1-x}Mg_xTe$ ER layer as well.

CHAPTER 9 FABRICATION AND CHARACTERIZATION OF HIGH EFFICIENCY CDTE DEVICES

9.1. DEVICE STRUCTURE

CdS has been traditionally used with CdTe as an n-type window layer. However, sublimated CdS window layer restricts deposition of CdTe at higher temperature due to resublimation of CdS during reheating of substrate and deposition of CdTe. Additionally, CdS is a strong absorber of light above its band-gap of 2.4 eV and thus the light absorbed within this layer cannot reach the CdTe absorber layer[25]. As a result, photogenerated carriers from CdS are not collected and the light absorbed in this layer is wasted. Use of high-resistance transparent (HRT) layer has been studied to enable use of thinner CdS layers to improve absorption within these wavelengths of light. Kephart *et al* showed that $Mg_xZn_{1-x}O$ maybe used for polycrystalline CdTe without an n-type CdS window layer to achieve higher short circuit current density as well as open circuit voltage leading to efficiency greater than 15.5%[25]. This $Mg_xZn_{1-x}O$ being more stable at elevated temperatures is used in this study to enable deposition of CdTe films at substrate temperatures over 610ºC without issues related to resublimation of CdS during CdTe deposition.

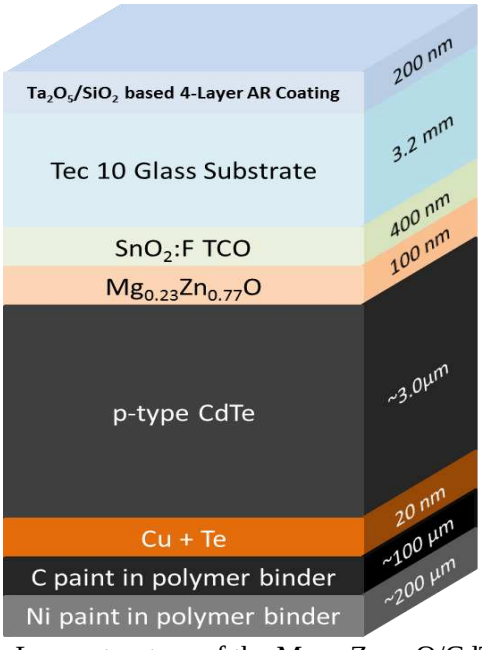


FIGURE 9.1 Device structure. Layer structure of the $Mg_{0.23}Zn_{0.77}O$/CdTe/Cu+Te photovoltaic device with carbon and nickel back electrode (not to scale)

In this study, film structure shown in figure 1 was fabricated and characterized after investigating several structures and film stacks. The reported device had films deposited on commercial low-iron soda-lime glass substrate 3.2 mm thick with ~400 nm of TCO i.e. fluorine doped tin oxide (SnO_2:F) coated on the glass by the manufacturer. A 4-layer Ta_2O_5/SiO_2 based anti-reflection (AR) coating with a total approximate thickness of 200 nm was deposited on the front of the glass that did not have coating of TCO. Alloying ZnO and MgO to create desired composition was $Mg_{0.23}Zn_{0.77}O$ was performed using radio-frequency (RF) sputter deposition and a 100 nm film was deposited on SnO_2:F TCO[25]. Thereafter ~3.0 µm CdTe film is deposited using sublimation followed by $CdCl_2$ passivation treatment and $CdCl_2$ activation process. After rinsing the residual $CdCl_2$ film, CuCl is used to deposit a very thin film of Cu on CdTe surface using sublimation process and 20 nm Te film deposited at room temperature using physical vapor deposition (PVD) to from the back contact. Following the Te deposition, carbon paint with an approximate thickness of 100 µm and nickel pain with an approximate thickness of 200 µm are sprayed as subsequent layers to form back electrode. Further details regarding film deposition method and device fabrication can be found in methods section.

9.2 Electrical Characterization

After fabrication of sublimated CdTe thin-film devices in a superstrate configuration, electrical performance of these devices was measured using a J-V measurement tool. Table1 shows performance of the best performing devices within the scope of this study. The average of measured fill factor for these devices was 79.54% while the averages of short-circuit currents was observed to be 26.98 mA/cm^2. Kephart *et al* reported TCO/ $Mg_{0.23}Zn_{0.77}O$/CdTe devices that had a V_{OC} of ~850 mV, fill factor of ~67% and J_{SC} of 25 mA/cm^2. The highest V_{OC} observed within this study was measured to be 863 mV and the increase from previous study is attributed to CdTe deposited at higher substrate temperature (610ºC) that results in larger CdTe grains and fewer grain boundaries. Te back contact is proved to have a major impact on improving the fill factor of CdTe thin-film devices as reported by Wei Xia *et al*[46]. Presence of a 20 nm Te along with Cu at the back surface appears to form an ohmic contact that has substantially reduction in recombination current that results in improvement of fill-factor for these devices[46], [47].

Improvement in short-circuit current is understood to be result of higher absorption due to presence of anti-reflective coating that is explained in next section. J-V plot in figure 2(a) shows excellent fill-factor. Higher absorption can be confirmed from the external quantum efficiency plot shown in figure 2b. External quantum efficiency also shows greater absorption at wavelengths lower than 400 nm suggesting higher charge collection in the absorber with use of $Mg_{0.23}Zn_{0.77}O$ and anti-reflection coating. Highest efficiency for devices without antireflection coatings was measured to be 17.9% (Supplementary image1).

Table 7
Summary of best performing CdTe photovoltaic devices

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)	Cell Area (cm^2)
1	858	27.1	80.5	18.71	0.661
2	858	26.9	80.5	18.61	0.667
3	858	27.0	80.2	18.59	0.665
4	856	27.0	80.1	18.55	0.669
5A	856	27.1	79.7	18.46	0.665
5B	863	26.8	79.2	18.30	0.573
6	857	27.0	76.6	18.40	0.666

*Sample 5B is certified performance for sample 5A by ILX Lightwave, Newport, CA.

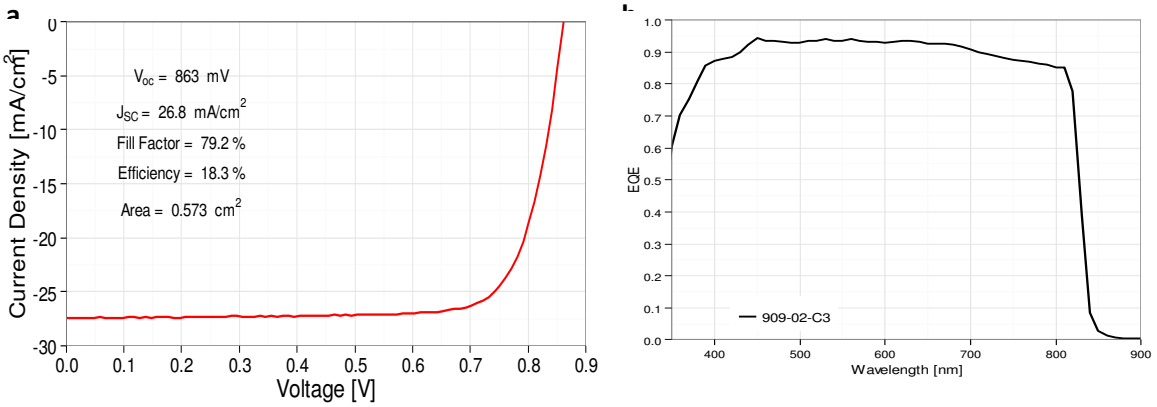


FIGURE 9.2 ILX Lightwave certified results. (a) J-V curve (b) and External quantum efficiency for device structure under investigation

9.3 ANTI-REFLECTION COATING

The calculated ideal antireflection coating has increased reflection for photon energies below the bandgap and for high photon energies where the photon flux is low. In the intermediate range there is a strong reduction in front-surface reflection. To compare the modeled anti-reflection coating with the

effect in the actual device, reflection was measured on the highest-efficiency device and a comparable device made without anti-reflection coating. The actual difference in reflection agrees well with the modeled difference (shown in figure 4**a**), with a slight shift to longer wavelengths and interference fringes from the transparent conductive and window layers. The estimated loss in short-circuit current density due to reflection for the AM1.5 global spectrum is 2.7 mA/cm^2 without the coating and 1.6 mA/cm^2 with the coating.

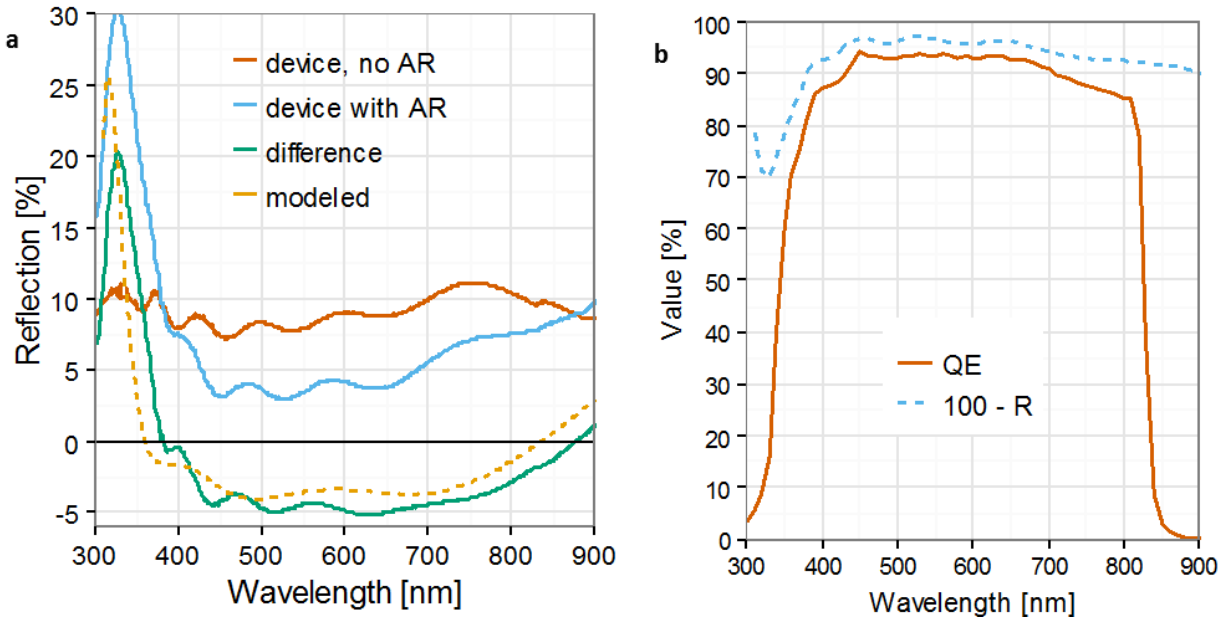


FIGURE 9.3 Characterization of antireflection coating (a) comparison of modeled anti-reflection coating to actual results (b) and quantum efficiency to estimate loss in short-circuit current density due to reflection.

9.4 MICROSCOPIC CHARACTERIZATION

Microscopic materials characterization was performed using Transmission Electron Microscope (TEM) and material distribution within the film stack mapped using Energy Dispersive X-ray Spectroscope (EDS). These films deposited at higher substrate temperature (~610ºC) exhibit large CdTe grain size when compared to films deposited at relatively lower substrate temperature[20], [43]. CdTe layer deposited here had an approximate thickness of 3 µm and CdTe grains appear to grow from $Mg_{0.23}Zn_{0.77}O$ front interface to the back surface as a continuous grain with no horizontal grain boundaries. A representative TEM micrograph is shown in figure 9.5. The interface between CdTe and $Mg_{0.23}Zn_{0.77}O$ appears to be continuous and uniform (~100 nm) with a homogenous and conformal

coverage over the Transparent Conducing Oxide (TCO) layer (figure 5b and 5c). CdS is reported to have a mismatch of 10% with CdTe and is known to have limited intermixing during high temperature deposition and $CdCl_2$ activation process[32]. Since $Mg_{0.23}Zn_{0.77}O$ has a similar crystal structure and lower lattice constant than CdS, it is understood to have greater mismatch with CdTe[25]. EDS maps of these high efficiency devices show no signs of magnesium, zinc or oxygen from $Mg_{0.23}Zn_{0.77}O$ layer diffusing into the CdTe layer within the detection limits of the instrument(figure 9.5e). In addition, High Resolution Transmission Electron Micrograph (HRTEM) shows an abrupt interface between $Mg_{0.23}Zn_{0.77}O$ and CdTe that reinforces minimal intermixing and diffusion between these layers(figure 5a and 5d). These films exhibit high efficiency (<18%) with good open circuit voltage and fill factors in spite of inherent defects as well as strain relieving at grain boundaries. This suggests that lattice matching in polycrystalline CdTe may not be of supreme importance. However, improving this interface quality between $Mg_{0.23}Zn_{0.77}O$ and CdTe may provide basis for further improvement in V_{OC}.

Other studies have shown Cl decorating CdTe grain boundaries and CdS/CdTe interface after $CdCl_2$ passivation treatment using EDS maps[21]. Li *et al* reported Cl rich region of 1~2 nm at CdTe/CdTe grain boundary using (Electron Energy Loss Spectroscopy) EELS line scan. It was also reported that grain boundary have enhanced carrier collection after $CdCl_2$ passivation treatment suggesting $CdCl_2$ playing more critical role than just promoting recrystallization[37]. It is also reported by Abbas *et al*[33] that extensive accumulation of Cl at interfaces and grain boundary have a detrimental effect on CdTe device performance. Comparatively much lower Cl is detected using EDS in CdTe films deposited at high temperature on $Mg_{0.23}Zn_{0.77}O$ buffer. Good device performance with such minimal Cl at grain boundary suggests that Cl required for enhanced carrier collection at grain boundaries is minimal. This also suggests that CdTe deposited on $Mg_{0.23}Zn_{0.77}O$ is more tolerant to $CdCl_2$ treatment and would allow more aggressive $CdCl_2$ treatment.

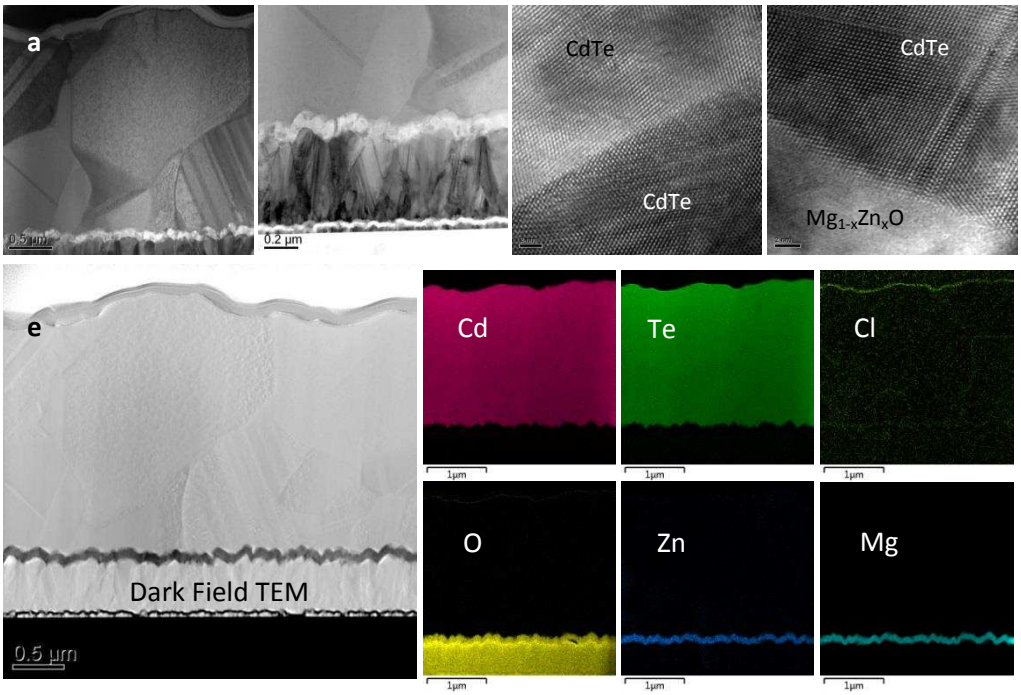


FIGURE 9.5 Microscopic analysis (a)TEM image TCO/Mg0.23Zn0.77O/CdTe/Te film stack (b) high magnification TEM image of TCO/ Mg0.23Zn0.77O and Mg0.23Zn0.77O/CdTe interface showing conformal coverage of Mg0.23Zn0.77O (c) HRTEM image of CdTe grain boundary showing no apparent signs fo line or bulk defects (d) HRTEM image of Mg0.23Zn0.77O/CdTe interface showing abrupt interface with minimal intermixing € EDS elemental map of TCO/Mg0.23Zn0.77O/Te film stack showing no diffusion of materials within EDS detection limits.

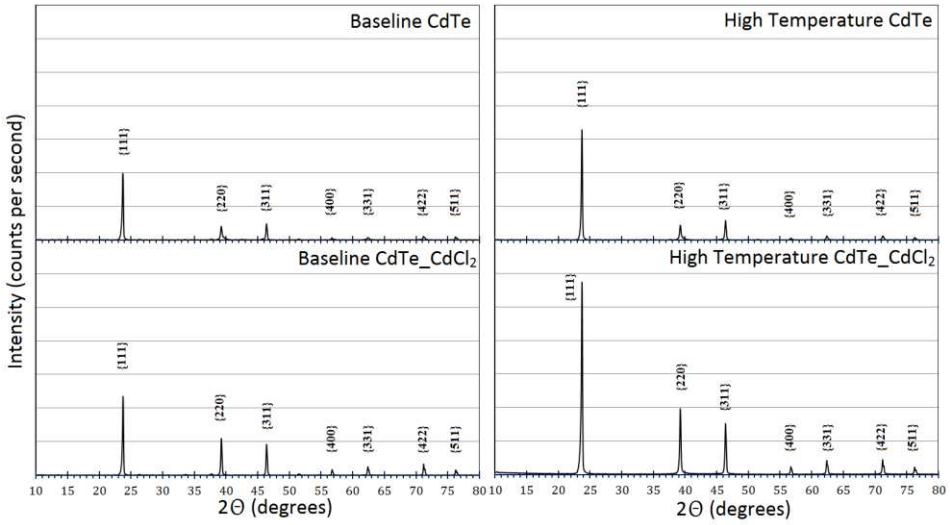


FIGURE 9.4 XRD analysis of film orientation. XRD Peak intensities showing increased {111} orientation and less randomization of CdTe films sublimated at higher temperature on $Mg_{0.23}Zn_{0.77}O$ buffer before and after $CdCl_2$ passivation treatment.

9.5 X-RAY DIFFRACTION

The measured peaks were fitted using a Pearson VII function in a R programming script (reference) and compared with JCPDS card #00-015-0770 for Cadmium Telluride.

At higher 2theta angles, peaks from K_{a2} are observed as a doublet peak. So for lattice parameter calculation, 2theta values from the first three high intensity peaks were taken into consideration and compared to the standard (Table 1). In all the cases, the change in the lattice parameter with respect to the standard value is insignificant suggesting no thermal stresses generated after the deposition and the $CdCl_2$ treatment.

Table 8
2theta values from the first three high intensity peaks were taken into consideration and compared to the standard

2Θ	*Lattice Parameter (Å)*	*% change wrt standard value*
Baseline (No $CdCl_2$)		
23.73	6.487	0.09%
39.25	6.485	0.13%
46.40	6.484	0.05%
Baseline ($CdCl_2$)		
23.76	6.480	-0.02%
39.27	6.482	0.09%
46.40	6.484	0.06%
HT (No $CdCl_2$)		
23.74	6.484	0.04%
39.26	6.484	0.11%
46.40	6.483	0.05%
HT ($CdCl_2$)		
23.75	6.482	0.02%
39.27	6.482	0.09%
46.45	6.478	-0.04%

There is an increase in the peak intensities in the samples treated with cadmium chloride (figure 9.5). This indicates that the crystalline quality of the material has increased. To evaluate preferred orientation (P_{hkl}) of a particular plane in the films, the intensities from the individual and the standard peaks were substituted in the texture coefficient formula.

$$P_{hkl} = \frac{I_{hkl}}{I_{o,hkl}} / \frac{1}{n}\sum_{i=1}^{n} \frac{I_{hkl}}{I_{o,hkl}}$$

Where I_{hkl} is the measured intensity, $I_{o,hkl}$ is the intensity corresponding to the particular plane in the JCPDS card and n are the number of the peaks considered. The calculated texture coefficients were plotted. As-deposited CdTe (baseline or HT) has a larger texture coefficient which indicates that a strong preferred orientation along {111} plane. After the $CdCl_2$ treatment in the baseline films, the texture coefficient along {111} drops significantly closer to unity. There is an increase in the texture coefficient along {511} plane indicating that the preferred orientation has changed. In the films processed at high temperature, the texture coefficient is still larger than unity after the $CdCl_2$ treatment, which suggests that the preferred orientation has not changed significantly.

The full width half maximum (FWHM) of the diffracted peaks gives information about the crystalline quality of the films. For the analysis, the FWHM was measured at the diffracted peaks of the films treated and not treated with $CdCl_2$. From the graph, it can be observed that the after $CdCl_2$ treatment, there is a decrease in the peak width which suggest that the crystalline quality of the CdTe has increased. No strong correlation was observed between the $CdCl_2$ treated samples which were fabricated at high temperature and baseline process conditions.

In addition, from microscopic analysis of CdTe films deposited at higher temperature and electrical characterization it is evident that larger grain size with no horizontal grain boundaries give higher efficiency photovoltaic devices. This can be observed in the figure below. As the grains grow larger, corresponding efficiency is observed to be increasing as well.

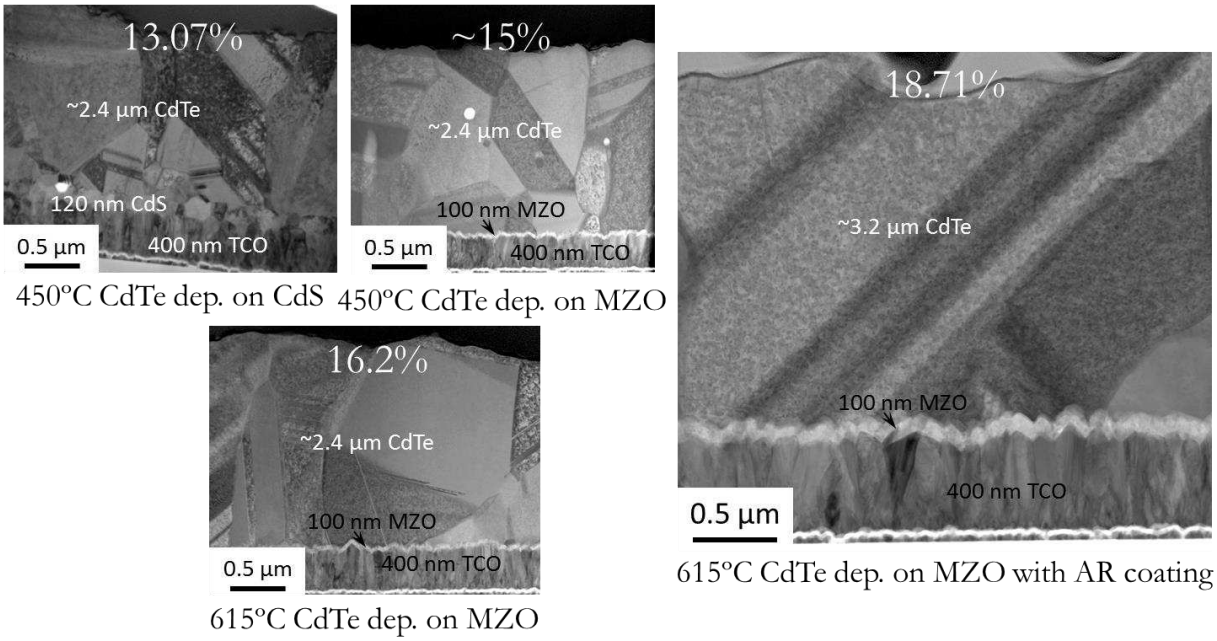


FIGURE 9.6 Comparison of grain size with increasing efficiency. It is evident that higher efficiency corresponds to larger CdTe grain size.

CHAPTER 10 OTHER PROJECTS AND CONTRIBUTIONS

10.1 CHARACTERIZATION OF $CD_{1-x}MG_xTE$ ELECTRON REFLECTOR FILM

10.1.1. ELECTRON REFLECTOR CONCEPT. CdTe material readily forms inter-granular defects that may act as electron sinks. With $CdCl_2$ passivation treatment defects may be reduced but not completely. To improve the efficiency of CdTe based photovoltaic devices, alternative means of increasing voltage and current must be investigated. One such means is the use of an electron reflector (ER) layer at the back of CdTe film. The idea is to introduce an electron reflector layer to increase the voltage by reduction of recombination near the back which acts as a conduction band barrier. Such an arrangement is expected to improve the voltage of the device by ~200 mV which would have a major impact on overall conversion efficiency of CdTe photovoltaic device. Cadmium magnesium telluride with a bang gap of ~1.9 eV is considered to be a good candidate for this purpose[48]. It is desirable to use a material that ER layer growth be epitaxial over CdTe since discontinuity between these layers would possibly reduce the device performance. In addition, cadmium telluride and cadmium magnesium telluride both have a cubic structure with similar lattice parameters which is highly desirable.

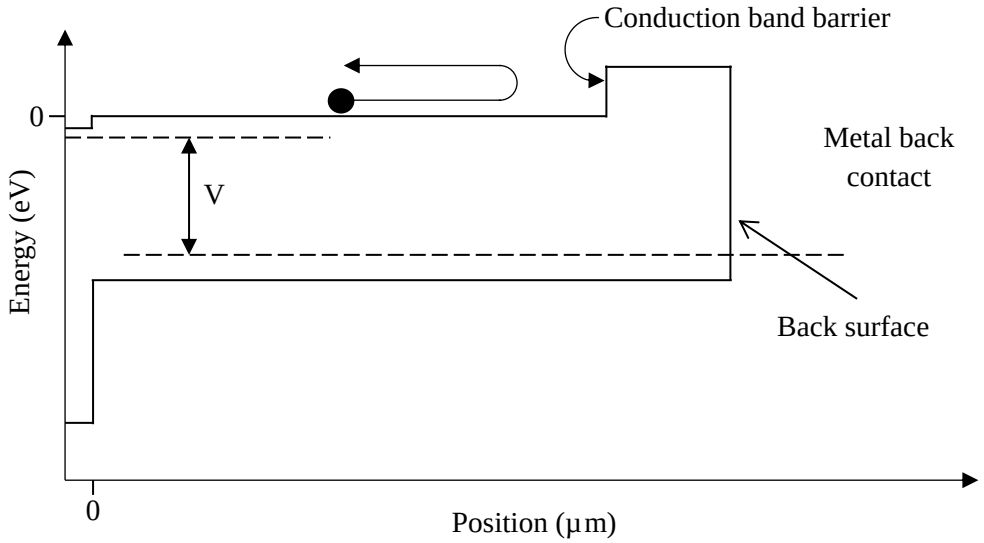


FIGURE 10.1 The band diagram of a CdTe cell with an electron- reflector layer at the back surface.

10.1.2. OVERVIEW OF CD1-XMGXTE GROWTH ON CDTE FILMS AND EARLY CHARACTERIZATION. $Cd_{1-x}Mg_xTe$ films were grown by close-space sublimation using the co-sublimation deposition source described in appendix 1. Only a very thin film (<100 nm) should be enough to perform as an electron reflector but for characterization purpose a thicker film was grown (700 nm - 900 nm). With early TEM images, there were some indications of epitaxial growth of $Cd_{1-x}Mg_xTe$ film on CdTe as grain boundaries continued through the CdTe film into $Cd_{1-x}Mg_xTe$ and so did stacking faults planes which can be seen in figure 10.2.

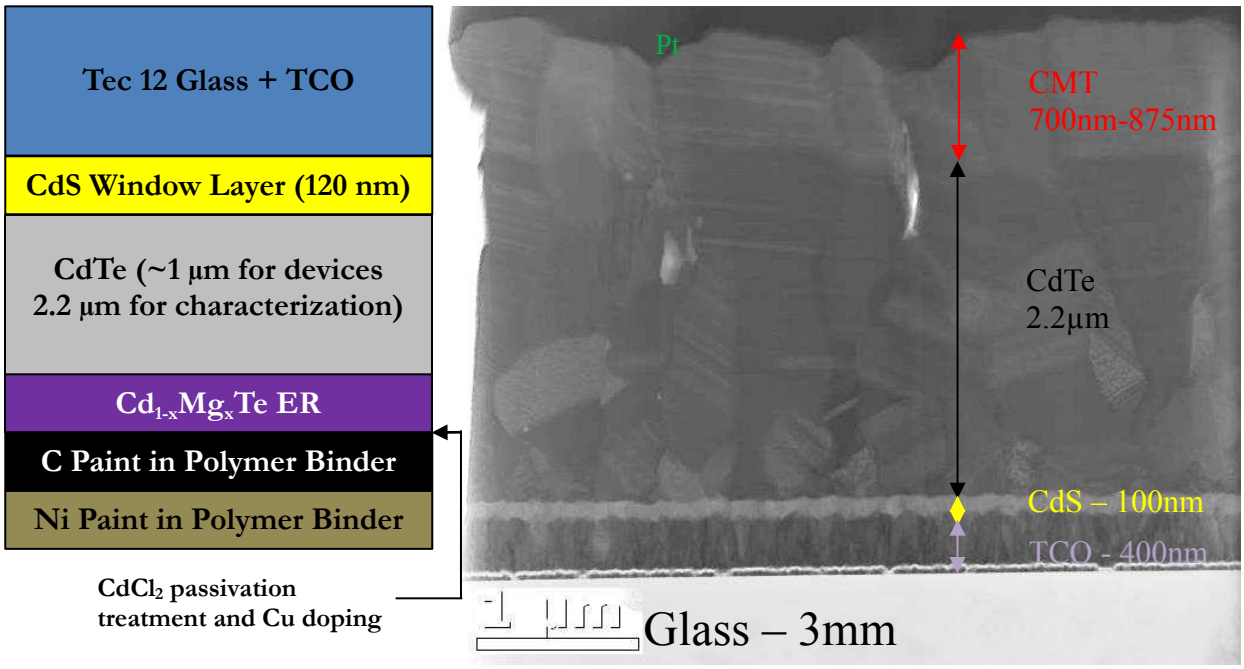


FIGURE 10.2 Schematic diagram (not to scale) of a typical $Cd_{1-x}Mg_xTe$ film stack (left) BF-TEM image distinctly showing various layers of a CdTe film with $Cd_{1-x}Mg_xTe$ ER layer (right)

To confirm the layers described earlier an EDX chemical mapping was also performed. This showed the distinct layers of $Cd_{1-x}Mg_xTe$, CdTe, CdS and TCO. EDX chemical map is shown in figure 6.3. This map clearly show who material is distributed within the CdTe film for Cd, Te, S, Mg, Sn and O. The Mg concentration varies from grain to grain and occasionally within the grain. The spot size here is too large to indicate any change in Mg concentration at the grain boundaries. The Te concentration seems to remain constant and reduction in Cd corresponds to increase in Mg concentration. This supports the Cd_{1-x} and Mg_x concentration in $Cd_{1-x}Mg_xTe$. Mg signal is seen in Pt layer but that is only background noise.

Heavier the element more will be the background it will produce. The x-ray emission energy's do not overlap for these elements. Slightly higher concentration of oxygen is observed in $Cd_{1-x}Mg_xTe$ layer as compared to the CdTe layer. More detailed study of oxygen in $Cd_{1-x}Mg_xTe$ is presented later in this chapter.

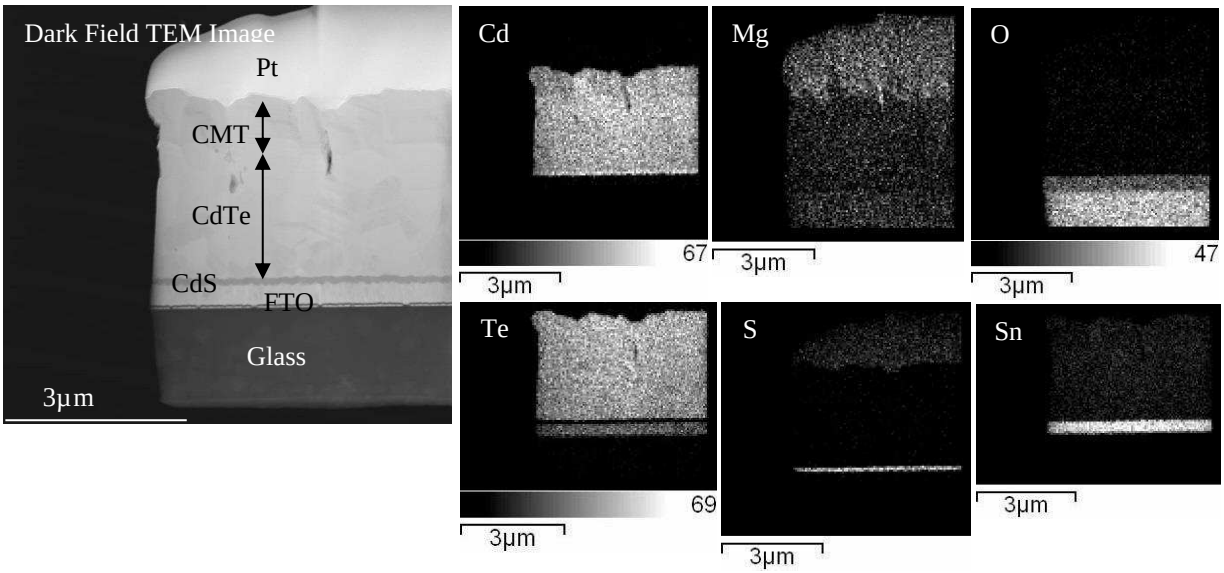


FIGURE 10.3 DF-TEM image distinctly showing various layers of a CdTe film with $Cd_{1-x}Mg_xTe$ ER layer and EDX chemical maps for Cd, Mg, O, Te, S and Sn defining material distribution within the film .

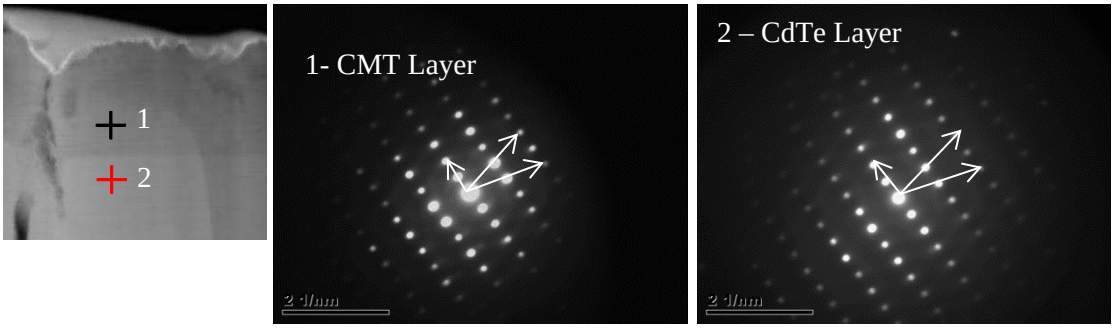


FIGURE 10.4 Electron diffraction pattern collected within the $Cd_{1-x}Mg_xTe$ ER layer and CdTe layer showing similar grain orientation

To confirm epitaxial growth of $Cd_{1-x}Mg_xTe$ on CdTe electron diffraction pattern was collected. Two diffraction patters were collected, one on a CdTe grain and other on CMT grain right about it. These patters showed very similar orientation between the two grains (figure 10.4).

These images and EDX maps as well as electron diffraction patters gave a good understanding of the basic characteristics of the $Cd_{1-x}Mg_xTe$ grown on CdTe. But to understand the film behavior under device conditions it was important to characterize these films in the configuration that would be used to make devices. The 2.2 µm CdTe films did not show any effect of $Cd_{1-x}Mg_xTe$ as an ER. Further experimentation showed its effects were visible in 1 µm thin CdTe absorber films with ~100 nm of $Cd_{1-x}Mg_xTe$ deposited on them. All the other characterization shown in the remaining part of this chapter was carried out on such films. Figure 10.5 shows higher resolution EDX map of one such film which allowed better understanding of materials distribution and interactions within the film.

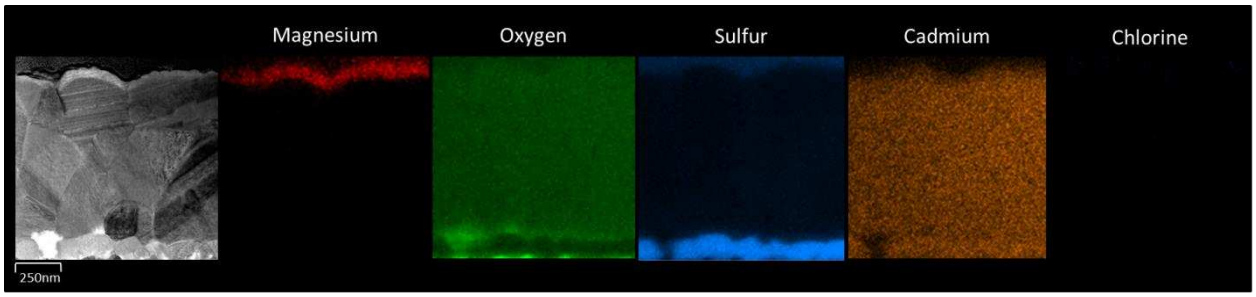


FIGURE 10.5 BF-TEM image and EDX chemical map of CdTe films with ~100 nm $Cd_{1-x}Mg_xTe$ ER layer before $CdCl_2$ passivation treatment

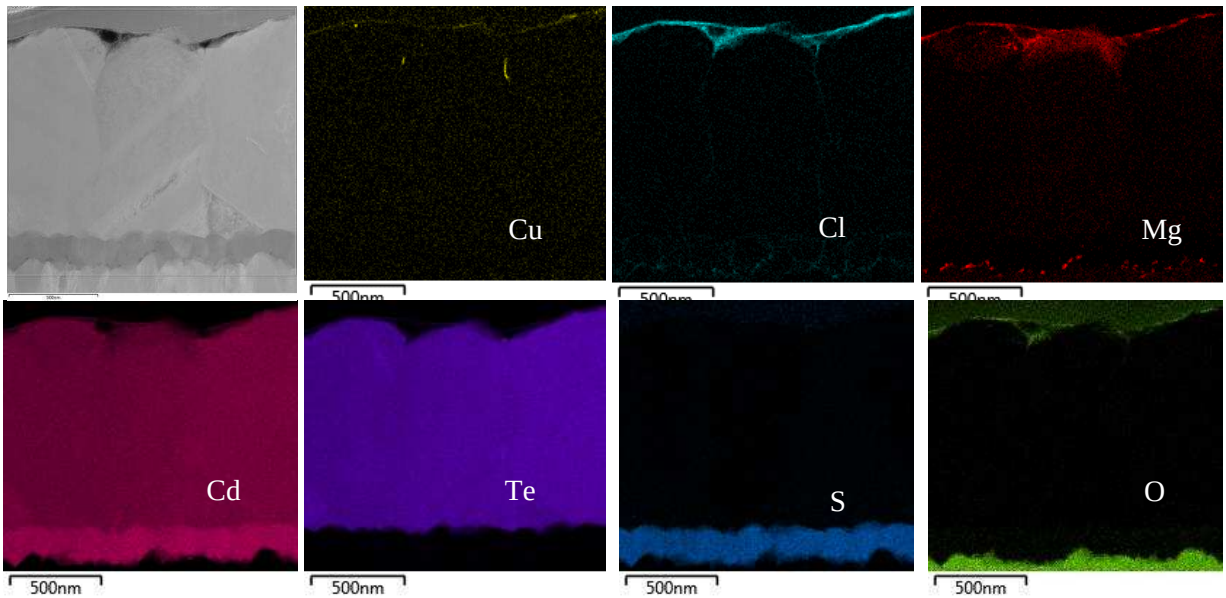


FIGURE 10.6 BF-TEM image and EDX chemical map of CdTe films with ~100 nm $Cd_{1-x}Mg_xTe$ ER layer after $CdCl_2$ passivation treatment

The grain boundaries of the two films were aligned. Cross-section TEM and EDX is presented in Figure 10.5 of an un-passivated CdS/CdTe/$Cd_{1-x}Mg_xTe$ stack. The magnesium film appeared to be continuous along the back of the CdTe cell, conforming to the shape of the CdTe morphology and maintaining epitaxial growth. There was little to no sulfur diffusion from the CdS, and no chlorine signature.

When devices were fabricated from these films performance improved. Materials characterization showed that chlorine decorated the grain boundaries. There was no apparent presence of stacking faults, and there was minimal sulfur diffusion. However, the $Cd_{1-x}Mg_xTe$ film no longer looked continuous, and it appeared that during the passivation step the $Cd_{1-x}Mg_xTe$ film degraded by substantial magnesium loss. If any oxygen or water is present, the Gibbs free energy is favorable for MgTe to react and reduce to MgO[48]. There was a strong oxygen and chlorine signature at the $Cd_{1-x}Mg_xTe$ layer, suggesting that some of the magnesium may have reacted and formed an oxide or chloride. In addition, it was also observed that Mg and Cl rich area corresponded to each other at the CdS interface. Figure 10.7 shows the response from the XPS KLL magnesium peak as a function of depth into the film. The MgTe has a peak that corresponds to ~303 eV and MgO has a peak that corresponds to ~306 eV. After passivation the MgO signature at 306 eV is apparent on the surface, and as we sputter into the device, the peak shifts towards a MgTe signature at 303 eV. This suggests that the back of the cell has reacted from MgTe to MgO.

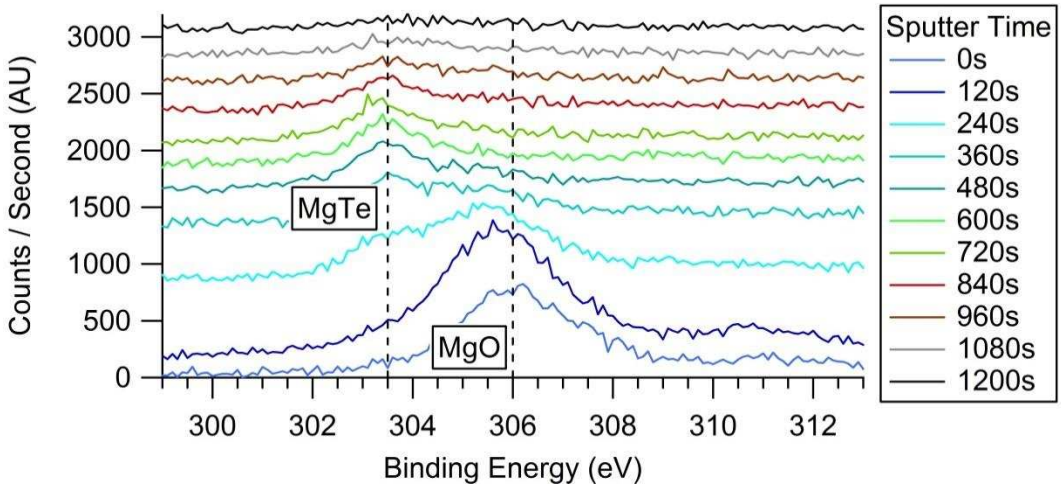


FIGURE 10.7 XPS depth profile stack of magnesium KLL peak as a function of sputter time from top to bottom

10.1.3 CDTE CAPPING LAYER ON $CD_{1-X}MG_XTE$ FILMS. In an attempt to minimize the formation of MgO, a thin CdTe capping layer was deposited on top of the $Cd_{1-x}Mg_xTe$ layer to limit exposer of the film to atmosphere with the intention of reducing oxidation and magnesium loss. Several CdTe capping layer thicknesses were sublimated and 100 nm thickness was found to give better device performance as can be seen from figure 6.8. This CdTe layer was deposited immediately after the $Cd_{1-x}Mg_xTe$ deposition and was controlled by shuttering off the magnesium vapor flux in situ. Figure 6.8 shows that with the addition of the CdTe capping layer there is an improvement in cell performance, primarily an improvement in FF. Since MgO has a large band gap (~6.72 eV) and an electron affinity of 2.8 eV, this would induce a large valance band offset at the back of the device and likely cause this reduction in FF[48]–[50].

Figure 10.10 shows cross section TEM and EDX of the passivated CdS/CdTe/ $Cd_{1-x}Mg_xTe$ /CdTe cap stack. The addition of a 100nm CdTe Cap has removed the previously seen oxygen signature at the back of the cell, indicating that the cap has helped prevent MgO formation. However, significant localized magnesium loss appears at the grain boundaries.

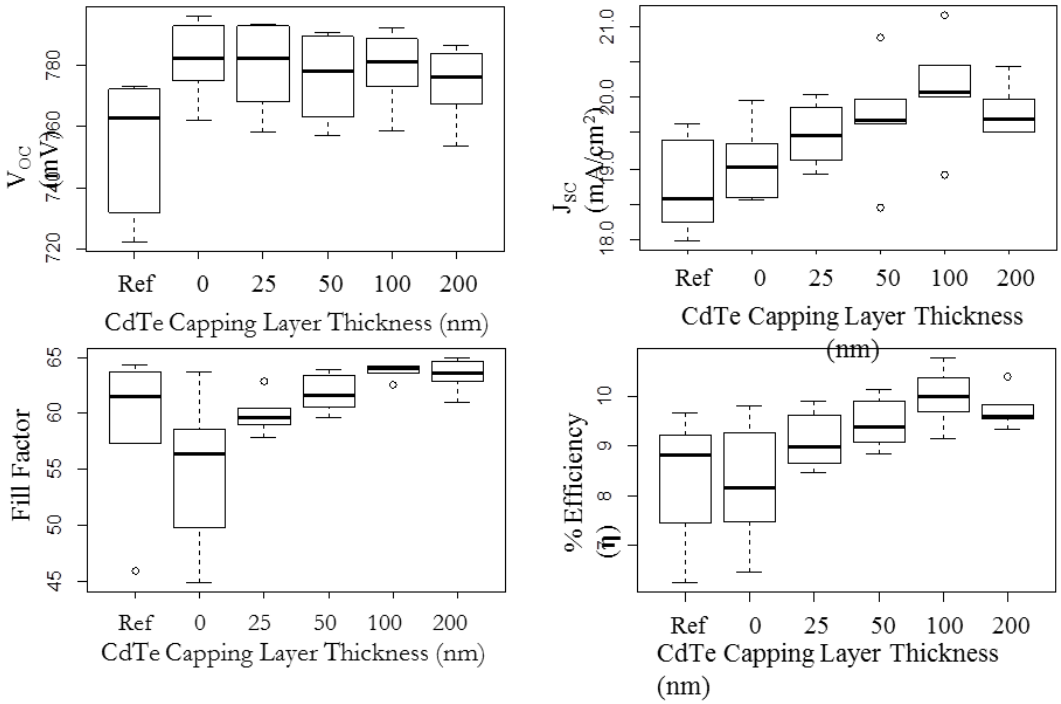


FIGURE 10.8 Box plots showing effect of varying CdTe capping layer thickness on device performance

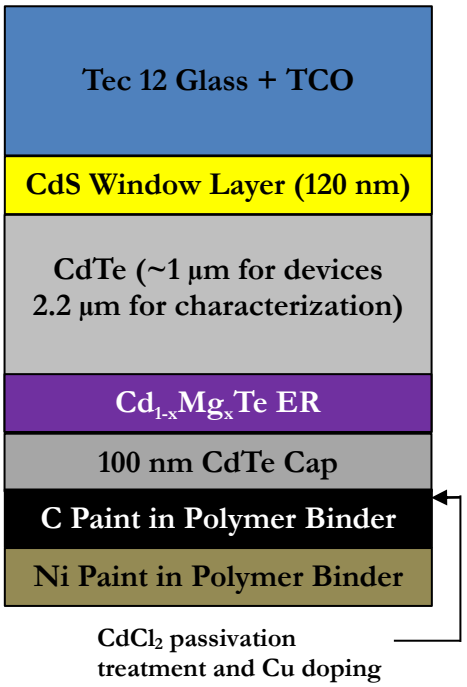


FIGURE 10.9 Schematic diagram (not to scale) of a typical Cd1-xMgxTe film stack with 100 nm CdTe cap

$MgCl_2$ has been shown to be as effective as $CdCl_2$ in passivating CdTe cells [21]. The Gibbs free energy calculation suggests MgTe reaction with $CdCl_2$ to form CdTe + $MgCl_2$ is favorable. However, if the cells were passivated with $MgCl_2$ instead of $CdCl_2$, the localized magnesium loss at the grain

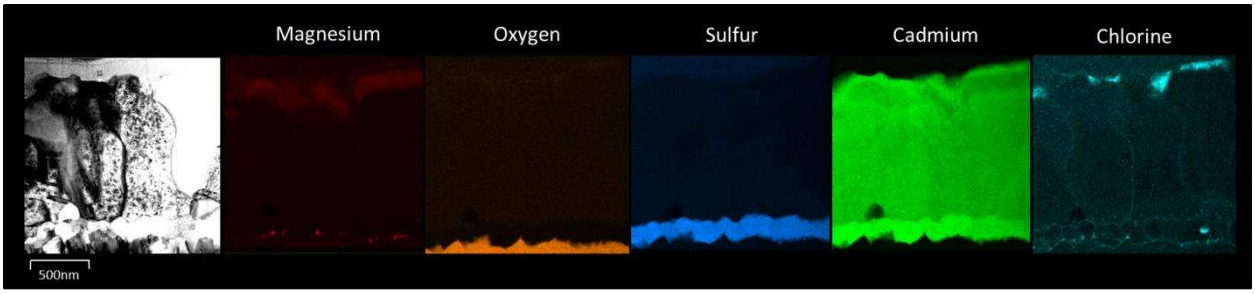


FIGURE 10.10 Cross section TEM and EDX maps of CdS/CdTe/Cd1-xMgxTe with 100 nm capping layer boundaries may be reduced [19].

Figure 6.11 shows the cross section TEM and EDX of a CdS/CdTe/$Cd_{1-x}Mg_xTe$ /CdTe Cap cell passivated with $MgCl_2$ instead of $CdCl_2$. The cell performance did not improve, and the localized magnesium loss was still seen and similar to what was observed with $CdCl_2$ passivation. This may suggest that the loss mechanism is not a reaction with $CdCl_2$ but with chlorine, since if chlorine is moving

down the grain boundaries and not $CdCl_2$, the loss mechanism would likely not be the same between $CdCl_2$ and $MgCl_2$.

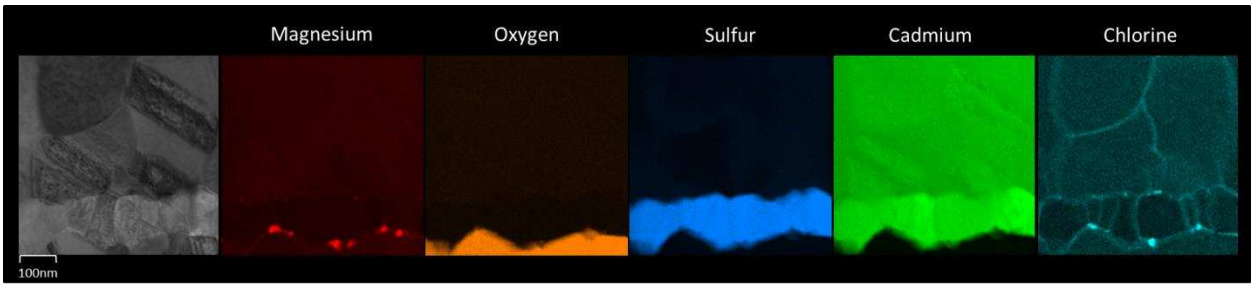


FIGURE 10.11 Cross section TEM and EDX maps of CdS/CdTe/Cd1-xMgxTe at the CdS/CdTe interface in films with 100nm capping layer after $MgCl_2$ passivation

Figure 10.11 shows a magnified view of the CdS/CdTe interface of a CdS/CdTe/$Cd_{1-x}Mg_xTe$/CdTe cap stack passivated with $CdCl_2$. It shows magnesium diffused down the grain boundaries and being collected at the CdS/TCO as well as CdS/CdTe interfaces. With no substantial oxygen or chlorine concentration to correlate with the magnesium, strong bonding between magnesium with either of them is not clear. It is possible that this is the magnesium that was lost from the CMT film during passivation and has traveled down the grain boundaries and collected at the front interfaces.

EDX line scan showed that the $Cd_{1-x}Mg_xTe$ layer had a good distinct interface and there were no prominent signs of intermixing of Mg with either the CdTe absorber or the capping layer large enough to be detected by the EDX system. This line scan can be seen in figure 10.12.

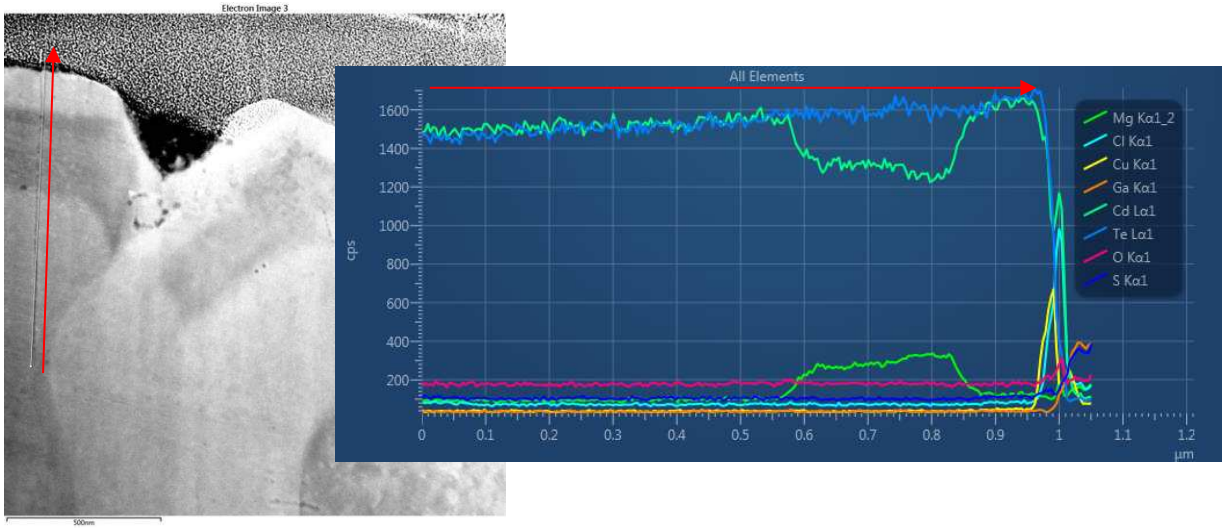


FIGURE 10.12 Cross section TEM and EDX line scan of CdTe/$Cd_{1-x}Mg_xTe$/CdTe cap interfaces scanned for material distribution study

10.2 CHARACTERIZATION OF CDZNTE FOR APPLICATION IN MULTI-JUNCTION PHOTOVOLTAICS

10.2.1 INTRODUCTION. To utilize the photons from sun's spectrum efficiently, minimize thermalization losses, and increase efficiency, a multijunction solar cell is a promising alternative to a single junction solar cell. Numerical simulations based on the daily energy densities indicate that the optimum band gap for the top cell absorber should be around ~1.72 eV in a two junction solar cell [51]. CdZnTe alloy has the zinc blende structure which is the same as that of CdTe [52],[53] and is a potential candidate for the top cell absorber in a multi-junction solar cell. Based on the zinc composition, the band gap of the alloy can be varied from 1.48 eV to 2.26 eV[54]. Using interpolation, a band gap of 1.72 eV can be obtained by using 40% zinc telluride composition in the CdZnTe alloy[55]**.**

Deposition methods such as Metal Organic Chemical Vapor Deposition (MOCVD)[55],[56], Vapor Transport[57], Close Space Sublimation(CSS)[58] and co-sputtering of CdTe and ZnTe[59] have been used to deposit CdZnTe thin films with different compositions by various research groups. The loss of zinc during the $CdCl_2$ activation treatment from the deposited CdZnTe films has been extensively reported[54],[56],[58]. However, the devices fabricated after $CdCl_2$ treatment, exhibited low photo generated current and very low fill factor. This leads to a low device performance irrespective of the deposition method used. If the $CdCl_2$ treatment is carried out at higher temperatures (in excess of 400^oC)[57],[60], an improvement in the device performance is observed. The improvement is associated with almost complete loss of zinc which reduces the band gap of the CdZnTe material to that of the lower band gap CdTe material. However, this improvement is disadvantageous since a higher band gap material is required for the fabrication of the top cell.

The cadmium chloride activation treatment of CdTe films is a critical step in improving the device performance of CdTe absorber based solar cells. The $CdCl_2$ treatment of thin film CdTe has been broadly studied and frequently reported in the literature[61], [34], [62], [63], [44], [64]. During the $CdCl_2$ treatment, chlorine is introduced into the CdTe using various techniques such as a vapor treatment[33] or by the application of $CdCl_2$ solution and then annealing at approximately 400^oC[44]. The improvement in

the device performance is caused by the presence of chlorine along the grain boundaries of CdTe[61], [34] and is attributed to recrystallization[62], [63], [44], grain growth, removal of stacking faults[33] and doping of grain boundaries n-type within the p-type CdTe absorber [61]. For CdZnTe devices, there is a lack of reports on understanding regarding the incorporation of chlorine in the bulk of the CdZnTe and in the residual CdTe, microstructural changes in the material, the status of stacking faults and recrystallization after the $CdCl_2$ treatment. In this work, the $CdCl_2$ treatment was performed on $Cd_{0.6}Zn_{0.4}Te$ films deposited by RF sputtering on CdS. Optical, material, and electrical characterizations were conducted to understand the changes caused to the CdZnTe film microstructure, the presence and distribution of chlorine together with the effect on the existence of stacking faults and other recrystallization processes caused by the $CdCl_2$ treatment.

10.2.2 EXPERIMENTAL DETAILS. For this study, samples were fabricated and characterized on TEC12D glass (Nippon Sheet Glass Co., Ltd). This glass has a coating of fluorine doped tin oxide on one side which serves as the transparent conducting oxide (TCO). The substrates were cleaned ultrasonically for 30 minutes in deionized water before deposition. Plasma cleaning at 400V, 15mA in an Ar/O_2 atmosphere was carried out individually on each sample[65]. After plasma cleaning, without breaking the vacuum, samples were transferred to a heater station for heating the substrate. The top and bottom heaters were maintained at 620^oC and the heating time was 110 seconds. The average temperature of the sample after heating was measured with a pyrometer and was about 480^oC. Cadmium sulphide (CdS) was deposited using close space sublimation (CSS) process on the fluorine doped tin oxide side of the sample. The temperature of the CdS source was 620^oC and the deposited film thickness was 125 nm. The details of deposition and a description of the vacuum system is provided elsewhere[29]. The samples were then cooled to room temperature and after breaking the vacuum, the cadmium zinc telluride (CdZnTe) sputter-deposition was carried out in a separate chamber.

Prior to the RF sputter-deposition, the chamber was pumped down to a base pressure of 10^{-5} Torr. To minimize residual oxygen, the chamber was purged several times with Ar gas. The samples coated with

CdS were baked for 15 minutes once the heaters reached the process temperature. The CdZnTe films were deposited using a single target with a composition of CdTe (60 wt%) and ZnTe (40 wt%) fabricated by Plasmaterials Inc. The CdZnTe target was plasma cleaned for 3 minutes with the shutter closed to prevent deposition. The deposition details of the RF sputtering process for CdZnTe are provided in table 1. The RF power applied to the target was 4.775 W/in^2. The substrate was heated to 400^{o}C and the distance between the target and the substrate was 4 inches. The process gas used was argon and the pressure was maintained at 10 mTorr. The thickness of the CdZnTe film measured at the center of the substrate using profliometer was ~ 1 micron.

The cadmium chloride ($CdCl_2$) treatment was carried in a horizontal CSS system (Figure 1). Approximately 10 g of $CdCl_2$ material (99.99% pure) was placed in the graphite boat. For the treatment, each sample was placed over the graphite boat and heated using infra-red (IR) lamps. A thermocouple attached to the graphite boat and the top plate recorded the process temperatures. The process gas used was Ar and the process pressure was ~10Torr. Two samples were treated at different temperatures (380^{o}C and 400^{o}C) for 3 minutes and one sample was retained untreated as a control. Other process conditions for the treatment of the two samples were maintained the same.

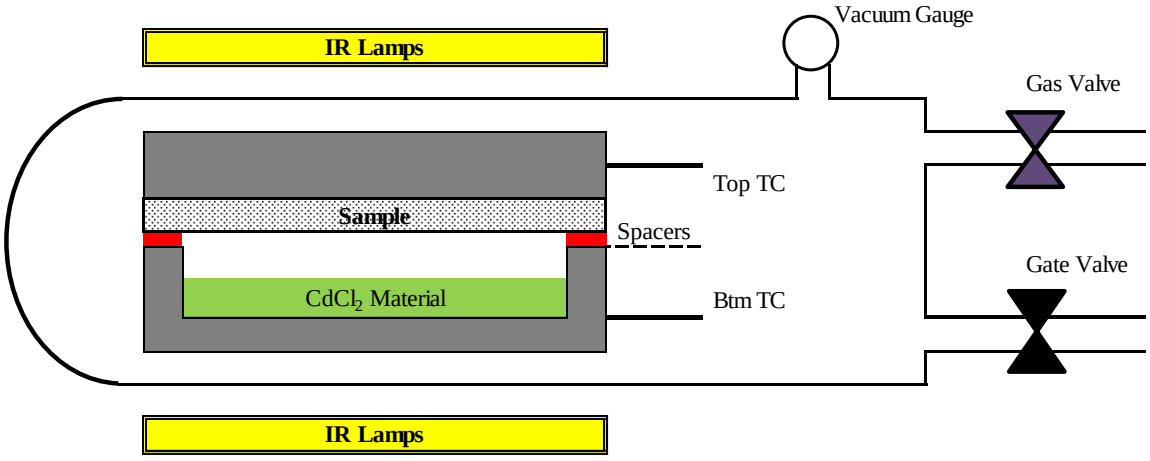


FIGURE 10.13 A schematic of horizontal bell jar used for CdCl2 activation treatment

After the $CdCl_2$ treatment, the samples were cut into two halves. On one half, optical transmission and material characterization measurements were conducted. For materials characterization, X-ray diffraction

(XRD), Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) analyses were performed. On the other half, devices were fabricated after copper doping, and carbon and nickel paints were applied as a back electrode. Current-voltage (JV) measurements on the devices were carried out under AM 1.5 conditions using an ABET Technologies solar simulator.

Transmission was measured from 350 to 1000 nm was using Ocean Optics Inc. hardware coupled with LabVIEW software. The Bruker AXS D8 system was used to conduct X ray diffraction measurements. The wavelength of Cu $K_{\alpha 1}$ radiation was 1.54046 Å and the diffracted signal was collected on scintillating counter. Surface images were obtained at 15 KV using a JEOL JSM 6500F scanning electron microscope. Sample cross sections for transmission electron microscopy (TEM) were prepared using a focused ion beam (FIB) with a dual beam FEI Nova 600 Nanolab. A JEOL 2000FX transmission electron microscope was used to obtain the TEM images.

10.2.3 TRANSMISSION ELECTRON MICROSCOPY. To locate the zinc loss from CdZnTe and to identify microstructural changes, a cross sectional specimen of CdZnTe treated with $CdCl_2$ at 400^oC was prepared using the focused ion beam specimen technique using a standard in-situ lift out method. The cross section was examined using TEM (figure 10.14) and Energy Dispersive X-ray (EDX) elemental mapping was carried out (figure 10.15) on the same cross section.

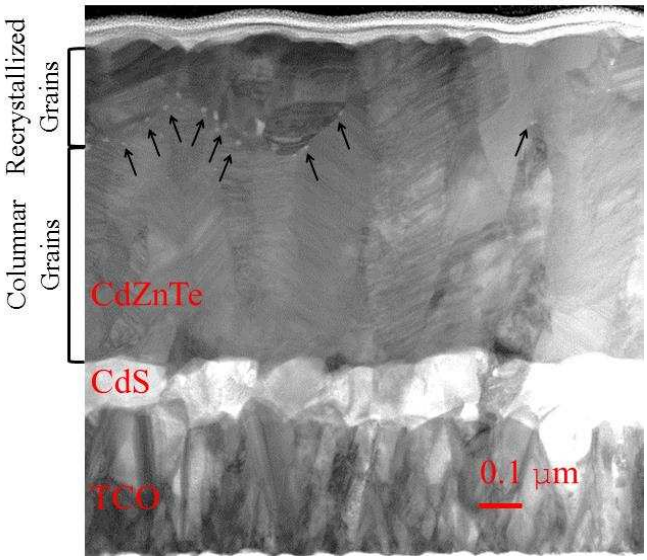


FIGURE 10.14 TEM image of a cross section of CdS/CdZnTe treated with CdCl2 at 400ºC. Arrows pointing towards the voids observed at the interface between the recrystallized and columnar grains.

In the TEM image of the cross section, the effect of $CdCl_2$ can be observed near the surface of CdZnTe films. It appears that the recrystallization starts at the surface and proceeds towards the junction of the CdS/CdZnTe. The recrystallization is incomplete. This is different to the process observed in sputtered CdTe treated with $CdCl_2$[44].The morphology of the grains near the surface changed from a columnar grain shape to an oval shape. The stresses generated during the grain growth may be a factor for inducing the voids near the grain boundaries of the recrystallized grains[33], [66]. Below the recrystallized grains, the columnar grains are observed which are the characteristic of sputter-deposited films are observed. In the columnar grains, the presence of a high density of stacking faults can be observed in the image.

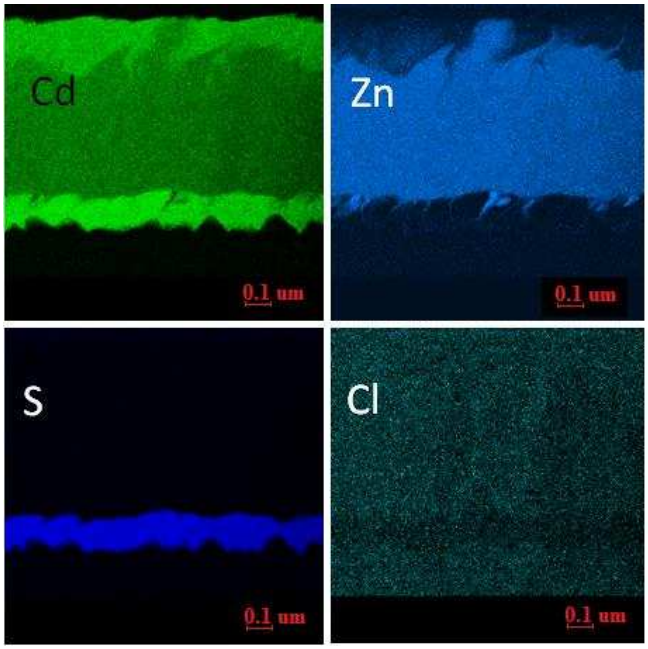


FIGURE 10.15 Elemental maps collected from the cross section of the sample treated with $CdCl_2$ at 400ºC. Individual elemental maps are labelled with the elemental symbol.

In the EDX elemental maps shown in figure 5, the zinc loss from the surface region is confirmed. The $CdCl_2$ vapors react with zinc in the CdZnTe layer and forms $ZnCl_2$[56]. At the treatment temperatures, $ZnCl_2$ has a higher vapor pressure than $CdCl_2$ and CdTe which causes zinc and chlorine to evaporate from the CdZnTe layer. At the junction of CdS/CdZnTe, zinc diffusion into the CdS can also be observed. This would probably lead to the formation of $Cd_{(1-x)}Zn_xS$ or ZnS compound in very small concentrations at the junction. Due to the low concentration, no diffracted peak signal corresponding to the $Cd_{(1-x)}Zn_xS$ or ZnS compound was detected in the XRD measurements. The critical observation was that the chlorine signal was below the detection limit of EDX in the zinc depleted region, along the grain boundaries of CdZnTe and at the junction of CdS/CdZnTe. In typical CdTe devices, optimal $CdCl_2$ treatment results in the decoration of grain boundaries with $CdCl_2$ that is clearly observed in the TEM. In the zinc depleted region of the sample, the residual compound is CdTe and there is no strong signal from chlorine. This indicates that the CdTe which has been formed after the $CdCl_2$ treatment is subsequently recrystallized but there is absence of chlorine at the grain boundaries. It has been shown that stacking faults are present, if there is no chlorine present at the grain boundaries. The absence of a discernible chlorine signal along the grain

boundaries of the CdZnTe and at the junction of CdS/CdZnTe suggests that the material present in these regions is unchanged from the as-deposited and is highly defective.

10.2.4. SCANNING ELECTRON MICROSCOPY. SEM images from the surface of the samples are shown in figure 10.16.

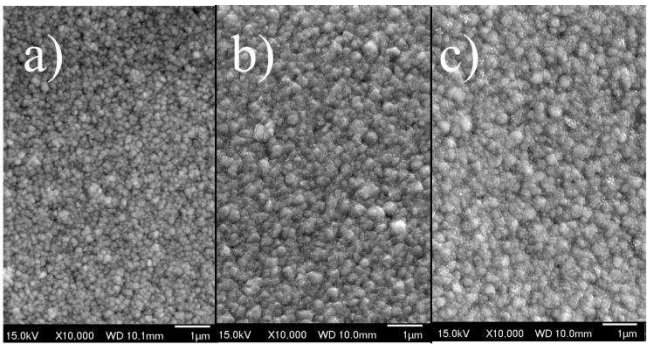


FIGURE 10.16 SEM images were taken at 15 KV accelerating voltage and 20 KX magnification. a) As-deposited CdZnTe, b) CdZnTe treated with $CdCl_2$ at 380ºC and c) CdZnTe treated with $CdCl_2$ at 400ºC

The grains are spherically shaped and uniform on the as-deposited CdZnTe sample. Recrystallization, grain coalescence and enlargement are observed in the $CdCl_2$ treated samples. In the sample treated with $CdCl_2$ at 380^{o}C, spherical shaped grains and newly formed larger grains are observed. At the higher $CdCl_2$ treatment temperature, large grains are formed by the fusion of small grains with distinct grain boundaries. It has been reported that after $CdCl_2$ treatment on CdTe, grains coalesce and grain boundaries are hard to distinguish under SEM. Such effects were not observed in the $CdCl_2$ treated CdZnTe.

10.2.5. PHOTOVOLTAIC PERFORMANCE. The current voltage measurements were carried out on all the devices under AM 1.5 illumination. The voltage was swept from -0.8 V to 1.2 V. The performance parameters obtained are listed in table 9.

Table 9

Device performance values obtained from Current Density – Voltage graph

Sample Description	Open circuit voltage (mV)	Short circuit current density (mA/cm^2)	Fill Factor
As-deposited CdZnTe	260	0.75	28
$CdCl_2$ treated CdZnTe at 380^oC	447	1.8	27
$CdCl_2$ treated CdZnTe at 400^oC	524	2.8	30.5

For a material with a band gap of 1.72 eV, the theoretical open circuit voltage and short circuit current density should be ~ 1.4V and ~ $20mA/cm^2$ [67]. The open circuit voltage, short circuit current density and fill factor values of all the three samples are substantially below these theoretical values. This is probably due to the grain boundaries not being doped with chlorine along with incomplete recrystallization and the existence of stacking faults which would act as recombination centers.

10.3 Fabrication of CdSeTe graded absorber to improve short-circuit current density

Improvement in short-circuit current density of CdTe based photovoltaic devices is an important step in improving efficiency of CdTe photovoltaic devices. Impact of incorporation of Se in CdTe devices has been demonstrated by First Solar Inc. It has been shown that using CdSeTe at the front interface of the film stack and gradual graded reduction of Se in the absorber would result in substantial improvement in short-circuit current density and thus efficiency. Initial work on such application of Se incorporation using advanced co-sublimation hardware at Colorado State University was demonstrated by Swanson *et al.* However, the expected improvement in device efficiency was not observed. TEM/EDS images and elemental mapping showed that Se grading in the absorber was not sufficient and therefore a new approach as investigated under this study.

Initial electrical characterizations of these films showed promising results with improvement in short-circuit current density. The measured value of J_{SC} was comparable to the highest value demonstrated in our laboratory of 27mA/cm^2. The J_{SC} for our certified cell was measured at 27.1mA/cm^2 and this device had a 5 layer anti-reflection coating. Achieving such improvement suggested that the CdSeTe grading was effective. This was confirmed using quantum efficiency measurements that showed that there was greater absorption at higher wavelength corresponding to published results on similar study.

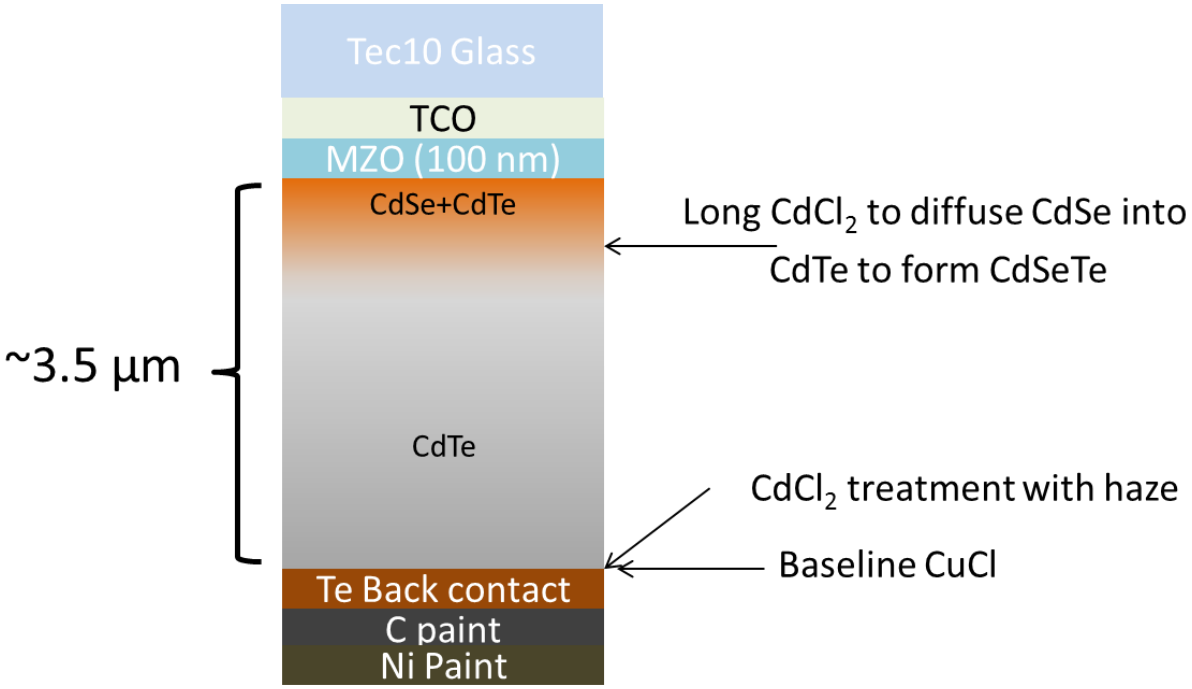


FIGURE 10.17 Schematic of film stack with CdSeTe graded absorber

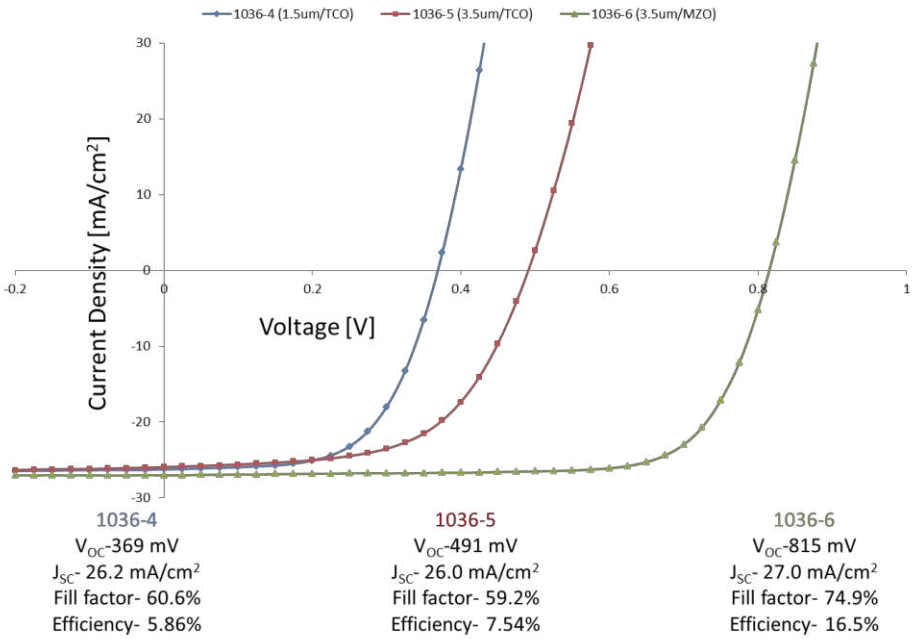


FIGURE 10.18 J-V plot show improved performance with CdSeTe graded absorber when deposited on MgZnO buffer

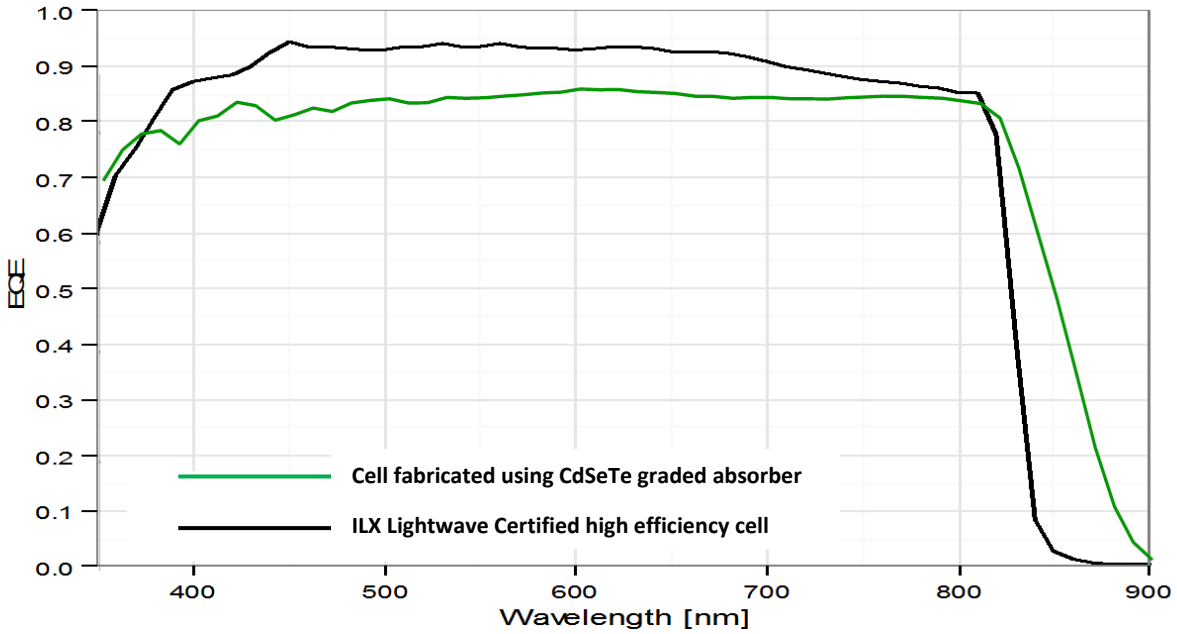


FIGURE 10.20 Quantum efficiency measurement showing enhanced absorption at higher wavelength with CdSeTe graded absorber

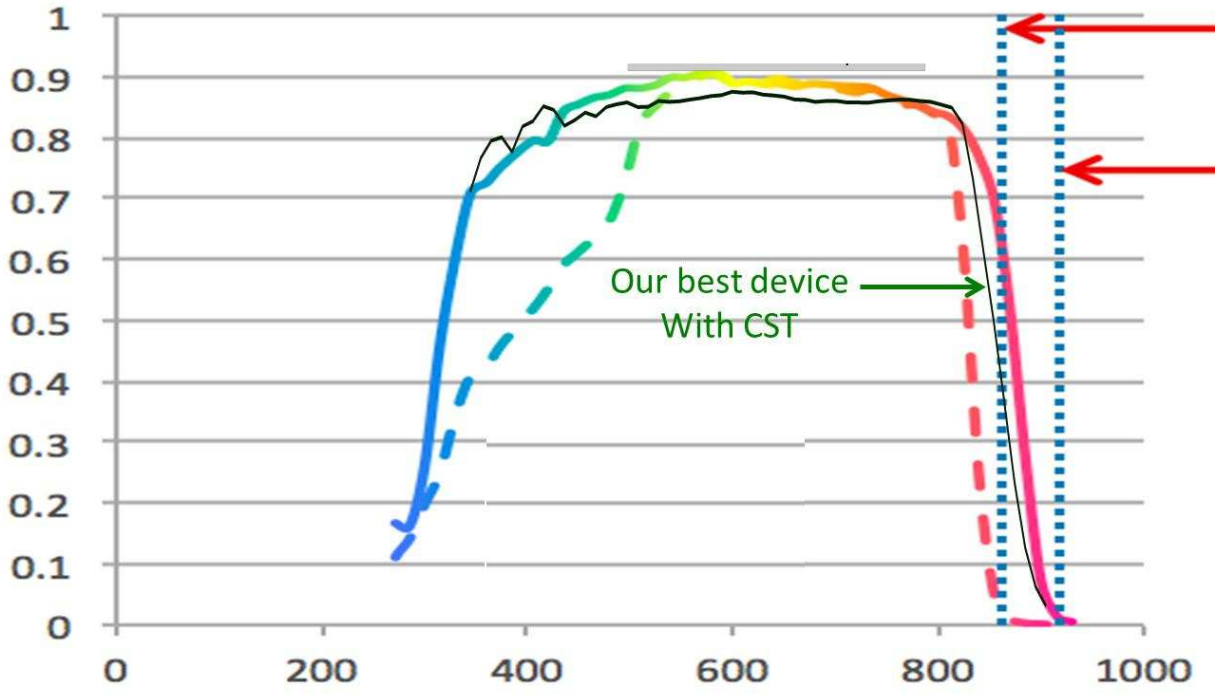


FIGURE 10.19 Quantum efficiency measurement of CdSeTe graded absorber compared to results published by First Solar Inc. for similar devices. Suggests a similar trend and good incorporation of Se in the absorber

10.4 6N PURE CDTE WITH 5N8 PURE $CdCl_2$

Semiconductor materials are known to be highly sensitive to impurities. These impurities act as dopants for the material and have a substantial effect on performance of their application. Although CdTe is a more forgiving material than other semiconductors such as silicon, it is important to investigate the effect of purity on CdTe photovoltaic devices. For this purpose 99.9999% pure CdTe was acquired from 5N Plus Inc. and 99.9998% pure $CdCl_2$ was acquired from Sigma Aldrich. The ARDS sublimation chamber was rigorously cleaned of all traces of earlier use and sublimation sources other than CdTe and $CdCl_2$ such as CuCl were removed from the deposition chamber to avoid contamination of pure CdTe and $CdCl_2$. After this the new pure material was loaded into the system and various films were deposited.

Devices fabricated from films deposited on CdS with higher purity material without Cu back contact had efficiency of 5.55% which was found to be much lower than the efficiency seen with less pure material that exhibits an efficiency of ~8.5%. This suggests that presence of trace quantities of contaminants and/or presence of CuCl in the tool in very small quantities does have a major impact on CdTe device efficiency.

Further investigation was carried out using MgZnO buffer on Tec10 glass substrate with CdTe deposited at high temperature with no Cu back contact showed improved device efficiency with Te back contact. Best performing device from this experiment demonstrated efficiency of 16.55% without any intentional Cu for back contact or doping. These devices did not show any kink in J-V plot suggesting Te back contact can remove charge barrier in CdTe devices and Cu is not necessary for fabrication of good CdTe devices. Figure 10.21 shows J-V plots for films fabricated with high purity material without Cu back contact and effect of Te back contact on device performance for such films. It is important to note that these are some of the highest efficiencies reported for polycrystalline CdTe photovoltaic devices fabricated without Cu back contact.

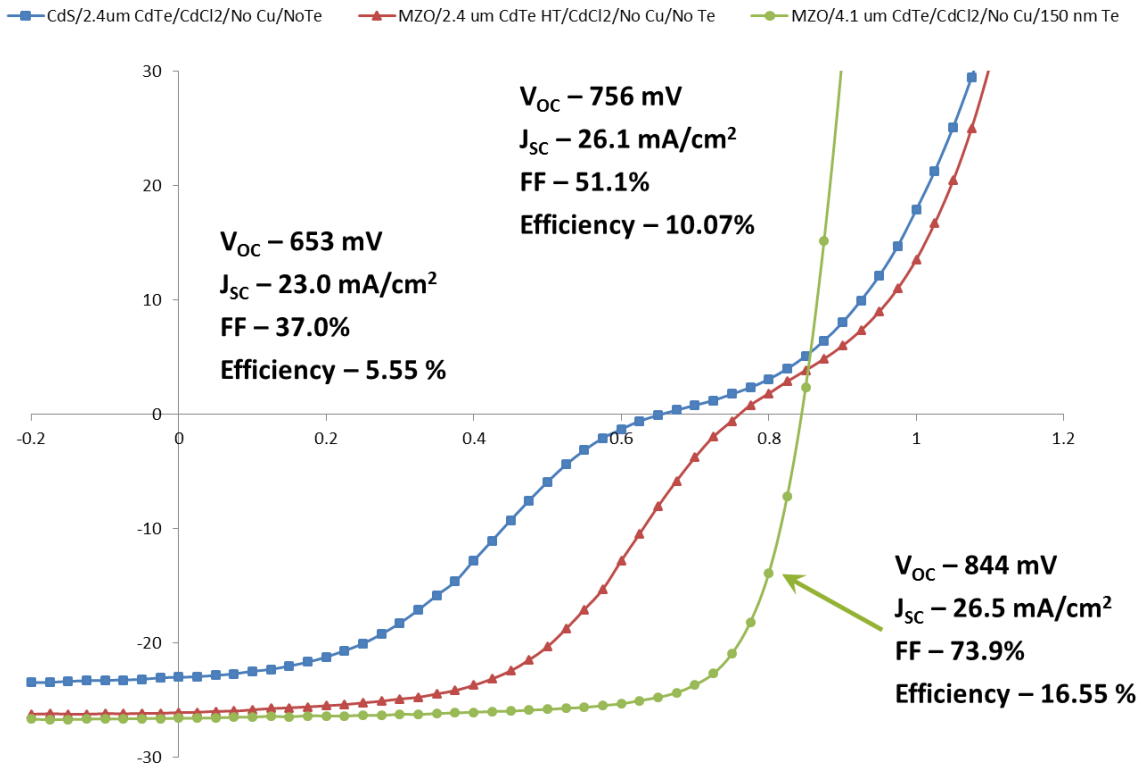


FIGURE 10.21 J-V plots for devices fabricated using high purity CdTe and $CdCl_2$ without Cu back contact

CHAPTER 11 CONCLUSIONS

11.1 SUSTAINABILITY OF CDTE PHOTOVOLTAIC TECHNOLOGY AND ENVIRONMENTAL IMPACT. The environmental and cost performance of modern CdTe thin film photovoltaic technology show a substantial competitive advantage over conventional methods of electricity generation. The material recyclability with CdTe at competitive cost makes it a unique energy source with greater sustainability. All these clearly suggest that CdTe photovoltaics can be seen as the energy solution in the long term. In addition, study shows that there is further scope of improving the efficiency of CdTe based photovoltaics by improving the fundamental understanding of materials science and evolution of better collection of photons resulting in improvement of voltage as well as current generation. Some results presented here suggest $CdCl_2$ passivation results in improvement of microstructural qualities such as increase in grain size and loss of stacking faults. Such fundamental understanding would be necessary for successful incorporation of electron reflector layers as well as development of high efficiency multijunction thin film photovoltaic devices. In conclusion, CdTe photovoltaics hold great promise for sustainable electricity generation.

11.2 EFFECT OF VARYING PROCESS TEMPERATURE ON DEVICE PERFORMANCE. Lower substrate temperature for CdTe deposition has a detrimental effect on device performance that can be related to film microstructure. Films with higher substrate temperature with hotter passivation treatment gives improved VOC and fill factor with current and efficiency comparable to standard cells which can also be related to film microstructure. Longer passivation treatment forms chlorine rich regions which may be related to lower device performance. Energy Dispersive X-ray Spectroscopy of TEM samples shows chlorine build up in the voids between the grains at the grain boundaries. Chlorine may be diffusing through the grain boundaries to reach the CdTe/CdS interface as can be seen from SIMS depth profile of the films and the EDS data collected with BF-STEM. This may cause the initiation of passivation treatment at the CdTe and CdS interface.

Lower substrate temperature during CdTe deposition form high concentration of small CdTe grains at the interface of CdTe and CdS that has detrimental effect on cell performance. This also results in high density of longitudinal voids between the CdTe grains in the absorber layer and that extended through the thickness of the CdTe film. Higher substrate temperature during CdTe deposition forms larger grains that can be related to better device performance. Such films in addition to larger grains have grains that are well defined and do not show a lot of voids between CdTe grains. Relationships between these process parameters and uniformity of cells can be established using EL images. High substrate temperature cells with 10ºC hotter $CdCl_2$ treatment temperature exhibits the best uniformity within the scope of this study along with higher V_{OC} and fill factor.

11.3 CHARACTERIZATION OF OVER 18% EFFICIENT DEVICES. We have provided here a comprehensive study of sublimated polycrystalline CdTe thin-film photovoltaic film and devices with efficiency exceeding 18%. There is a clear evidence suggesting polycrystalline CdTe as an excellent photovoltaic material for utility scale energy production. Modification of fabrication process can lead to high efficiency without substantial addition to manufacturing cost. Sublimated CdTe PV devices with efficiency up to 18.7% are reported here with the highest measured fill factor of 80.5%, short circuit current density of 27.1 mA/cm^2 and open circuit voltage of 863 mV. These improvements have been achieved through several process modifications.

Eliminating CdS window and using $Mg_{0.23}Zn_{0.77}O$ enables sublimation of CdTe at temperature higher than 600ºC. Higher substrate temperature at the beginning of CdTe sublimation gives larger CdTe grains. Films sublimated were about 3 µm thick and CdTe grains appeared to grow from $Mg_{0.23}Zn_{0.77}O$/CdTe interface to CdTe back surface. It has been consistently observed that larger grain size corresponds to higher device efficiency (supplementary image 1). In addition, using thicker CdTe films would suggest that back surface recombination is reduced since the back surface is located at a larger distance from the CdTe absorber bulk. Etching the back surface to form a Te rich surface and forming a Cu+Te ohmic contact has shown improvements in device efficiency in other studies. In the reported study we show that

tellurium deposited using PVD at room temperature has similar effect as forming Te rich back surface by etching. PVD allows deposition of Te in a more controlled manner and TEM images show good conformal coverage of Te on the back surface as shown in supplementary image 2. Reduced recombination in the bulk as well as reduced back surface recombination seems to manifest in form of high fill factor suggesting higher device quality. Higher device quality can also be confirmed from the fact that the A-factor for these devices were measured at 1.4 and hysteresis measurement showed minimal memory as the plots swept both ways almost shadowed each other (supplementary figure 3).

For epitaxial grown films the interface between absorber and underlying layer must be closely matched to reduce defects and fabricate good devices. However, CdTe is cubic while $Mg_{0.23}Zn_{0.77}O$ is hexagonal and HRTEM images show an abrupt interface between CdTe and $Mg_{0.23}Zn_{0.77}O$. EDS maps show no signs of substantial diffusion of Mg or Zn into CdTe absorber layer reinforcing the observation that there is no noteworthy diffusion between CdTe and $Mg_{0.23}Zn_{0.77}O$. This suggests that for polycrystalline CdTe interface between absorber and underlying layer may not be of paramount importance otherwise it would not form high-quality devices.

Using $Mg_{0.23}Zn_{0.77}O$ resistive layer gives an added advantage of eliminating CdS window layer. $Mg_{0.23}Zn_{0.77}O$ increases the optical band-gap of the layer that gives better ultraviolet transmission. This reduces losses from absorption of photons in the CdS layer allowing greater generation of photo-current leading to higher short circuit current. Adding a Ta_2O_5/SiO_2 anti-reflection layer further reduces reflection losses that improved short circuit current by allowing greater photo-generation of current.

The GXRD studies confirmed that as-deposited CdTe (baseline or high temperature) has a strong preferred orientation along {111} plane. After the $CdCl_2$ treatment on the high temperature deposited CdTe, the preferred orientation along {111} plane was maintained. The FWHM comparisons indicated increase in the crystalline quality of CdTe after the $CdCl_2$ treatment.

11.4 EFFECT OF $CdCl_2$ PASSIVATION TREATMENT ON CDTE FILMS AND DEVICES. $CdCl_2$ is known to be a crucial process step in fabrication of high efficiency CdTe devices. There are 3 main effects of $CdCl_2$ passivation that we understand to cause an improvement in CdTe device efficiency.

- Removal of stacking faults
- Increase in grain size
- Doping grain boundaries n-type

We have shown Cl presence at CdTe grain boundaries using EDS and ToF-SIMS. $CdCl_2$ reaction suggests that presence of Cl in V_{Te} sites. We understand that while Cl occupies V_{Te} sites it acts as a block in correcting the stacking sequence of CdTe crystal that results in removal of stacking faults after $CdCl_2$ treatment. Further evidence that suggests this action is the fact that removal of Cl using high temperature anneal under vacuum results in returning of stacking faults and on passivating the film again the stacking faults are again removed. Presence of Cl at grain boundaries is thus critical for good grain structure in CdTe films.

Increase in grain size after $CdCl_2$ passivation is observed in polycrystalline CdTe films. This is understood to occur due to formation of eutectic liquid phase in CdTe film during $CdCl_2$ passivation. Presence of such a phase accelerates the recrystallization process in CdTe film resulting in merger of smaller grains to form large grains. Fewer nucleation sites during CdTe grain growth also have an impact on grain size but $CdCl_2$ passivation treatment is understood to be of primary importance.

While Cl occupies V_{Te} at CdTe grain boundaries it also dopes the grain boundaries n-type in p-type absorber material. This gives a clear path for the conduction of holes and electrons through grain bulk and grain boundary respectively. This has been explained using EBIC and EELS measurements by Li *et al*. This further explains the importance of $CdCl_2$ passivation treatment in fabrication of high efficiency CdTe devices.

11.5 EFFECT OF CDTE GRAIN SIZE. We see in this study that larger grain size correspond to higher device efficiencies. Smaller grains have larger density of grain boundaries and that would mean presence of grain

boundaries perpendicular to the direction of hole conduction. We also know that grain boundaries are doped n-type in CdTe. This would mean horizontal grain boundaries would act as barrier for the conduction of charges affecting device performance. With larger grains we reduce the density of grain boundaries and when grains grow from front interface to the back surface of the device, the absence of grain boundaries perpendicular to the direction of charge conduction allow greater electron and hole mobility. This means that large grains are necessary for fabrication of high efficiency CdTe devices. However, the reason for this maybe the lower density of grain boundaries rather than larger grains themselves.

11.6 $CdCl_2$ PASSIVATION OF CDZNTE FILMS. The effect of the $CdCl_2$ treatment was studied on the stack comprising of TEC12D/CdS/CdZnTe by varying the treatment temperature. The as-deposited CdZnTe was a single phase with a preferred orientation along the {111} plane and had a band gap of 1.72 eV. Surface images showed that the grains were spherically shaped and uniformly distributed over the surface. After the $CdCl_2$ treatment at various temperatures, the absorption edge moved toward the higher wavelength region which is an indication of zinc loss and resulted in a reduced band gap of the material. The XRD results confirmed that the CdZnTe film was no longer a single uniform composition alloy after the treatment as peaks corresponding to CdTe were identifiable. There was more loss of zinc with the increased treatment temperature. Important insights were obtained from the TEM image and the EDS elemental maps of the sample treated at 400ºC which showed the absence of chlorine along the grain boundaries of CdZnTe and residual CdTe after zinc loss. Recrystallization and grain growth were observed at the surface of the CdZnTe and it appeared that grain growth started at the surface and proceeded toward the junction of the CdS/ CdZnTe. High densities of stacking faults were present in the columnar grains below the recrystallized region. The SEM images showed that the grain boundaries were distinct. The absence of chlorine along the grain boundaries of CdZnTe and residual CdTe, incomplete recrystallization, and the presence of stacking faults were considered responsible for the poor performance in the fabricated devices.

CHAPTER 12 FUTURE WORK

- After an extensive study of hundreds of CdTe films and devices a better understanding of $CdCl_2$ passivation treatment has been developed. To further understand the role of Cl in removal of stacking faults from CdTe grains and recrystallization of CdTe to from large grains greater microscopic imaging capabilities would be needed. These capabilities include but not limited to aberration corrected high voltage transmission electron microscope with high resolution multiple detection aberration corrected EDS system that can image presence of Cl at grain boundaries and establish its relationship with Cd and Te.
- Higher deposition temperature for CdTe resulting in larger grain size and higher efficiency has been demonstrated. Further reduction in deposition rate and larger grain size must be investigated that may lead to higher device efficiencies.
- Using CdMgTe electron reflector with thinner CdTe films has shown promising results. Microscopic imaging and elemental mapping has played an important role in improving processing conditions. This study needs to be further extended to get a complete effect of CdMgTe electron reflector for CdTe devices that would be able to address the voltage deficit and thus lead to higher device efficiency.
- Better understanding of CdZnTe microstructures has been developed using high resolution electron microscopy and that has helped in improving passivation process for these films. These studies need to be continued to aid complete passivation of CdZnTe films for successful fabrication of top cell for multi-junction CdTe devices.
- Initial results with CdSeTe graded absorber has shown promising results and this composition must be further refined to achieve higher J_{SC}. This may also lead to better electron-hole recombination lifetime which might be necessary for successful application of CdMgTe electron reflector.

- Developing an understanding of stacking faults and their effect on electrical characteristics of CdTe thin-film photovoltaics as well as their effect on grain growth and recrystallization needs to be studied more extensively. Su-Hyun Yoo et al have shown evidence that a reduction in the high density of stacking faults in the CdTe grains is a key process step that occurs during $CdCl_2$ passivation treatment. Computational investigation and density function theory (DFT) modeling have found low-energy faults are electrically benign and high energy faults act as hole traps. These modeling observations are consistent with atomic-resolution micrographs. Further study of these faults with such computational and mathematical modeling to understand the stacking fault energy as well as the effect of residual stress would require detailed investigation to understand the individual effect of these parameters. This study has shown that presence of chlorine has a strong relationship with stacking faults in CdTe film. Using such mathematical modeling it would be also important to understand bonding of chlorine at the grain boundaries and the relationship of Cl with stacking faults. This may allow better understanding of role of chlorine in electrical performance of CdTe thin-film photovoltaics.

BIBLIOGRAPHY

[1] B. Petrol, “BP Statistical review of world energy.”

[2] O. Morton, “A NEW DAY DAWNING ?,” *Nature*, vol. 443, no. September, pp. 19–22, 2006.

[3] P. Denholm and R. M. Margolis, “Land-use requirements and the per-capita solar footprint for photovoltaic generation in the United States,” vol. 36, pp. 3531–3543, 2008.

[4] K. Mitchell, A. L. Fahrenbruch, and R. H. Bube, “Photovoltaic determination of optical - absorption coefficient in CdTe,” vol. 829, no. 1977, pp. 29–31, 2016.

[5] D. T. F. Marple, “Optical Absorption Edge in CdTe : Experimenal*,” *Phys. Rev.*, vol. 1351, no. 1965, pp. 728–734, 1966.

[6] Garabedian Rafi, “Technology Update,” 2016.

[7] C. Ian, “Buffett strikes cheapest electricity price in US with Nevada solar farm,” *pv-magazine*, 2015. [Online]. Available: http://www.pv-magazine.com/news/details/beitrag/buffett-strikes-cheapest-electricity-price-in-us-with-nevada-solar-farm_100020120/#axzz40eM9WRtt.

[8] W. Eric, “Exclusive: First Solar’s CTO Discusses Record 18.6% Efficient Thin-Film Module,” *Greentech Media*, 2015. [Online]. Available: http://www.greentechmedia.com/articles/read/Exclusive-First-Solars-CTO-Discusses-Record-18.6-Efficient-Thin-Film-Mod.

[9] S. Krum, D. Brady and S. Haymore, “First Solar, INC. Announces First Quarter 2014 Financial Results,” Tempe, AZ, 2014.

[10] S. Krum and S. Haymore, “First Solar, Inc. 2016 First Quarter Financial Results,” Tempe, AZ, 2016.

[11] V. M. Fthenakis, *Life cycle impact analysis of cadmium in CdTe PV production*, vol. 8. 2004.

[12] M. Raugei, S. Bargigli, and S. Ulgiati, “Life cycle assessment and energy pay-back time of advanced photovoltaic modules : CdTe and CIS compared to poly-Si,” vol. 32, pp. 1310–1318, 2007.

[13] V. Fthenakis, “Sustainability of photovoltaics: The case for thin-film solar cells,” *Renewable and Sustainable Energy Reviews*, vol. 13, no. 9. pp. 2746–2750, 2009.

[14] M. A. Green, E. Keith, H. Yoshihiro, W. Wilhelm and E. D. Dunlop, “Solar cell efficiency tables (Version 45),” *Prog. Photovoltaics*, vol. 23, no. 1, pp. 1–9, 2015.

[15] U. S. Energy Iinformation Administration (EIA), “Electric Power Monthly with Data for Novermber 2015,” 2016.

[16] T. Kenning, “Buffett project’s record low cost part of pricing ‘trend’, says First Solar,” *pv-tech.org*, 2015. [Online]. Available: http://www.pv-tech.org/news/buffett_projects_record_low_cost_is_part_of_pricing_trend_says_first_solar.

[17] L. Caldwell, “First Solar and Solar Energy Innovation.” [Online]. Available:

www.laurencaldwell.com/.../lauren-caldwell_policy-to-drive-energy-inn...

[18] W. Eric, “First Solar Surprises With Big 2013 Guidance, 40 Cents per Watt Cost by 2017,” *Greentech Media*, 2013. [Online]. Available: http://www.greentechmedia.com/articles/read/First-Solar-Surprises-With-Big-2013-Guidance-40-Cents-Per-Watt-Cost-by-201.

[19] FirstSolar, “Environmental Impact Environmental Stewardship,” *First Solar*. [Online]. Available: http://www.firstsolar.com/en/About-Us/Corporate-Responsibility/Environmental-Impact.aspx.

[20] A. Munshi, A. Abbas, J. Raguse, K. Barth, J. M. Walls and W. S. Sampath, “Effect of varying process parameters on CdTe thin film device performance and its relationship to film microstructure,” pp. 1643–1648, 2014.

[21] Ali Abbas, Geoff D. West, Jake W. Bowers, Piotr M. Kaminski, B. Maniscalco, John M. Walls, Kurt L. Barth and W.S. Sampath “Cadmium Chloride Assisted Re-Crystallization of CdTe: The Effect of Varying the Annealing Time,” *MRS Proc.*, vol. 1638, 2014.

[22] Ali Abbas, Geoff D. West, Jake W. Bowers, Piotr M. Kaminski, John M. Walls, Kurt L. Barth and W.S. Sampath “Cadmium Chloride Assisted Re-Crystallisation of CdTe: The Effect on the CdS Window Layer,” *MRS Proc.*, vol. 1738, 2015.

[23] J. Kephart, R. Geisthardt and W.S. Sampath, “Optimization of CdTe thin-film solar cell efficiency using a sputtered, oxygenated CdS window layer,” *Prog. Photovoltaics*, vol. 23, no. 11, pp. 1484–1492, 2015.

[24] J. Kephart, J. Mccamy, Z. Ma, A. Ganjoo, F. Alamgir, and W. S. Sampath, “Solar Energy

Materials & Solar Cells Band alignment of front contact layers for high-ef fi ciency CdTe solar cells," vol. 157, pp. 266–275, 2016.

[25] J.M. Kephart, J.W. McCamy, Z. Ma, A. Ganjoo, F.M. Alamgir and W.S. Sampath, "Band alignment of front contact layers for high-efficiency CdTe solar cells," *Sol. Energy Mater. Sol. Cells*.

[26] J. Sites, A. Munshi, J. Kephart, D. Swanson and W. S. Sampath, "Progress and Challenges with CdTe Cell Efficiency," in *43rd IEEE Photovoltaics Specialists Conference (PVSC)*, 2016.

[27] A. Munshi, J. Kephart, A. Abbas, T. Shimpi, K. Barth, J. Walls, W.S. Sampath, "Characterization of CdTe Photovoltaic Films and Devices with Over 18% Efficiency Fabricated Using Scalable Sublimation Process," *Nat. Energy (Manuscript progress)*, 2016.

[28] J. Raguse, T. McGoffin and J. Sites, "Electroluminisecnse system for analysis of defects in CdTe cells and modules," in *38th IEEE PVSC*, 2012.

[29] D. Swanson, J. Kephart, P. Kobyakov, K. Walters, K. Cameron, K. Barth, W. S. Sampath, J. Drayton, and J. Sites, "Single vacuum chamber with multiple close space sublimation sources to fabricate CdTe solar cells," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 34, no. 2, p. 021202, 2016.

[30] D. Swanson, J. Kephart, P. Kobyakov, K. Walters, K. Cameron, K. Barth, W. S. Sampath, J. Drayton, J. Sites, "Single vacuum chamber with multiple close space sublimation sources to fabricate CdTe solar cells Single vacuum chamber with multiple close space sublimation sources to fabricate CdTe solar cells," vol. 021202, pp. 0–6, 2016.

[31] K. Barth, R. Enzenroth, and W. S. Sampath, “ADVANCES IN CONTINUOUS, IN-LINE PROCESSING OF STABLE CdSlCdTe DEVICES,” in *33rd IEEE PVSC*, 2008, no. 1, pp. 3–6.

[32] A. Munshi, J. Kephart, A. Abbas, T. Shimpi, K. Barth, J. Walls and W.S. Sampath, “Effect of Varying Deposition and Substrate Temperature on Sublimated CdTe Thin-Film Photovoltaics,” in *43rd IEEE Photovoltaics Specialists Conference (PVSC)*, 2016.

[33] A. Abbas, G. West, J. Bowers, P. Isherwood, P. Kaminski, B. Maniscalco, P. Rowley, J. M. Walls, K. Barricklow, W. S. Sampath, and K. L. Barth, “The effect of cadmium chloride treatment on close-spaced sublimated cadmium telluride thin-film solar cells,” *IEEE J. Photovoltaics*, vol. 3, no. 4, pp. 1361–1366, 2013.

[34] M. Terheggen, H. Heinrich, G. Kostorz, A. Romeo, D. Baetzner, A. Tiwari, A. Bosio, and N. Romeo, “Structural and Chemical Interface Characterization of CdTe Solar Cells by Transmission Electron Microscopy,” *Thin Solid Films*, vol. 431–432, no. 03, pp. 262–266, 2003.

[35] P. Kaminski, K. Barricklow, W. S. Sampath, K. Barth, U. Kingdom, F. Collins, and U. States, “The Effect of Cadmium Chloride Treatment on Close Spaced Sublimated Cadmium Telluride Thin Film Solar Cells,” pp. 1–6.

[36] S. Wei and S. Zhang, “Chemical trends of defect formation and doping limit in II-VI semiconductors : The case of CdTe,” no. May, pp. 1–10, 2002.

[37] C. Li, Y. Wu, J. Poplawsky, T. Pennycook, N. Paudel, W. Yin, S. Haigh, M. Oxley, A. Lupini, M. Al-jassim, S. Pennycook, and Y. Yan, “Grain-Boundary-Enhanced Carrier Collection in CdTe Solar Cells,” vol. 156103, no. April, pp. 1–5, 2014.

[38] T.X. Zhou, N. Reiter, R.C. Powell, R. Sasala and P. Meyers “Vapor chloride treatment of polycrystalline CdTe/CdS Films,” *IEEE*, pp. 103–106, 1994.

[39] H. Tai, S. Nakashima and S. Hori, “Optical properties of (CdTe)1-x(CdSe)x and (CdTe)1-x(CdS)x systems,” *Phys. Status Solidi*, vol. 30, no. 2, pp. K115–K119, 1975.

[40] J. Saraie, M. Kitagawa, M. Ishida and T. Tanaka, “Liquid phase epitaxial growth of CdTe in the CdTe-CdCl2 system,” *J. Cryst. Growth*, vol. 43, pp. 13–16, 1978.

[41] S. Yoo, K. T. Butler, A. Soon, A. Abbas, J. Walls, and A. Walsh, “Identification of critical stacking faults in thin-film CdTe solar cells,” *Appl. Phys. Lett.*, vol. 105, p. 062104, 2014.

[42] M. Kim, J. Lee, S. Lee, and S. Sohn, “Solar Energy Materials & Solar Cells Study of CdTe / CdS heterostructure by $CdCl_2$ heat treatment via in situ high temperature XRD,” *Sol. Energy Mater. Sol. Cells*, vol. 109, pp. 209–214, 2013.

[43] D. Mao, L. H. Feng, Y. Zhu, J. Tang, W. Song, R. Collins, and D. Williamson, “Interdiffusion in polycrystalline thin - film CdTe / CdS solar cells Interdiffusion in Polycrystalline Thin-Film CdTe / CdS Solar Cells,” vol. 352, no. 1996, 1999.

[44] A. Abbas, B. Maniscalco, J. Bowers, P. Kaminski, G. West, and J. Walls, “Initiation of the cadmium chloride assisted re-crystallization process of magnetron sputtered thin film CdTe,” *Conf. Rec. IEEE Photovolt. Spec. Conf.*, pp. 1930–1934, 2013.

[45] C. Li, J. Poplawsky, Y. Yan, and S. J. Pennycook, “Materials Science in Semiconductor Processing Understanding individual defects in CdTe thin- fi lm solar cells via STEM : From

atomic structure to electrical activity," *Mater. Sci. Semicond. Process.*, pp. 1–13, 2016.

[46] W. Xia, H. Lin, H. Ning, C. Tang, I. Irfan, C. Wang, and Y. Gao, "Solar Energy Materials & Solar Cells Te / Cu bi-layer : A low-resistance back contact buffer for thin fi lm CdS / CdTe solar cells," vol. 128, pp. 411–420, 2014.

[47] D. Kraft, A. Thissen, J. Broetz, S. Flege, M. Campo, A. Klein, W. Jaegermann, D. Kraft, A. Thissen, J. Broetz, and S. Flege, "Characterization of tellurium layers for back contact formation on close to technology treated CdTe surfaces Characterization of tellurium layers for back contact formation on close to technology treated CdTe surfaces," vol. 3589, no. 2003, 2016.

[48] P. Kobyakov, A. Moore, J. Raguse, D. Swanson, A. Moore, and J. Raguse and W. S. Sampath, "Deposition and characterization of Cd1 − xMgxTe thin films grown by a novel cosublimation method Deposition and characterization of Cd 1 2 x Mg x Te thin films grown by a novel cosublimation method," vol. 021511, no. 2014, 2016.

[49] B. Brennan, S. McDonnell and G. Hughes, "Photoemission studies of the interface formation of ultrathin MgO dielectric layers on the oxidised Si(111) surface," *J. Phys.*, 2007.

[50] D. Swanson, R. Geisthardt, P. Kobyakov, J. Raguse, J. Drayton, J. Sites, "Reduction of Carrier Recombination in CdTe Solar Cells by the Addition of a $Cd_{1-x}Mg_xTe$ Electron Reflector Film.," in *40th IEEE Photovoltaics Specialists Conference*, 2014.

[51] T. Coutts, J. Ward, D. Young, K. Emery, T. Gessert, and R. Noufi, "Critical issues in the design of polycrystalline, thin-film tandem solar cells," *Prog. Photovoltaics Res. Appl.*, vol. 11, no. 6, pp. 359–375, 2003.

[52] J. Yang, S. Chen, W. Yin, X. Gong, A. Walsh, and S. Wei, "Electronic structure and phase stability of MgTe, ZnTe, CdTe, and their alloys in the *B* 3, *B* 4, and *B* 8 structures," *Phys. Rev. B*, vol. 79, no. 24, p. 245202, 2009.

[53] K. Rahman, F. Haque, N. Khan, M. Islam, M. Alam, Z. Alothman, K. Sopian, and N. Amin, "Effect of $CdCl_2$ Treatment on Thermally Evaporated CdTe Thin Films," *Chalcogenide Lett.*, vol. 11, no. 3, pp. 129–139, 2014.

[54] B. McCandless, "Cadmium zinc telluride films for wide band gap solar cells," *Conf. Rec. Twenty-Ninth IEEE Photovolt. Spec. Conf. 2002.*, pp. 488–491, 2002.

[55] A. Ringel, R. Sudharsanan, A. Rohatgi, and W. Carter, "A Study of Polycrystalline Cd (Zn, Mn) Te/CdS Films and Interfaces," *J. Electron. Mater.*, vol. 19, no. 3, pp. 259–263, 1989.

[56] A. Rohatgi, R. Sudharsanan, S. Ringel, and M. MacDougal, "Growth and Process Optimization of Cdte and Cdznte Polycrystalline Films for High-Efficiency Solar-Cells," *Sol. Cells*, vol. 30, no. 1–4, pp. 109–122, 1991.

[57] B. Mccandless, W. Buchanan, and G. Hanket, "Thin Film Cadmium Zinc Telluride Solar Cells," pp. 483–486, 2006.

[58] R. Dhere, T. Gessert, J. Zhou, S. Asher, J. Pankow, and H. Moutinho, "Investigation of CdZnTe for Thin-Film Tandem Solar Cell Applications," *MRS Online Proc. Libr. Arch.*, vol. 763, p. null–null, 2003.

[59] J. Gaduputi, "Characterization Of Cadmium Zinc Telluride Films And Solar Cells On Glass And

Flexible Substrates By RF Sputtering," University of South Florida, 2004.

[60] S. H. Lee, A. Gupta, and A. D. Compaan, "Polycrystalline sputtered Cd(Zn, Mn)Te films for top cells in PV tandem structures," *Phys. Status Solidi*, vol. 1, no. 4, pp. 1042–1045, 2004.

[61] C. Li, Y. Wu, J. Poplawsky, T. Pennycook, N. Paudel, W. Yin, S. Haigh, M. Oxley, A. Lupini, M. Al-Jassim, S. Pennycook, and Y. Yan, "Grain-Boundary-Enhanced Carrier Collection in CdTe Solar Cells," *Phys. Rev. Lett.*, vol. 112, no. 15, p. 156103, 2014.

[62] B. McCandless, L. Moulton, and R. Birkmire, "Recrystallization and sulfur diffusion in $CdCl_2$-treated CdTe/CdS thin films," *Prog. Photovoltaics Res. Appl.*, vol. 5, no. March, pp. 249–260, 1997.

[63] M. Rami, E. Benamar, M. Fahoume, F. Chraibi, and a Ennaoui, "Effect of heat treatment with $CdCl_2$ on the electrodeposited CdTe / CdS heterojunction (A)," vol. 3, no. 1, pp. 66–70, 2000.

[64] J. Lee, "Effects of heat treatment of vacuum evaporated $CdCl_2$ layer on the properties of CdS/CdTe solar cells," *Curr. Appl. Phys.*, vol. 11, no. 1 SUPPL., pp. S103–S108, 2011.

[65] D. Swanson, R. Geisthardt, J. McGoffin, J. Williams, and J. Sites, "Improved CdTe Solar-Cell Performance by Plasma Cleaning the TCO Layer," *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 838–842, 2013.

[66] E. Bacaksiz, M. Altunbaş, S. Yilmaz, M. Tomakin, and M. Parlak, "Effects of CdCl2 treatment on properties of CdTe thin films grown by evaporation at low substrate temperatures," *Cryst. Res. Technol.*, vol. 42, no. 9, pp. 890–894, 2007.

[67] F. Meillaud, A. Shah, C. Droz, E. Vallat-Sauvain, and C. Miazza, “Efficiency limits for single-junction and tandem solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 18–19, pp. 2952–2959, 2006.

APPENDIX

A.1. FIB TEM sample preparation

FIB lift out procedure

1. Load the sample in the chamber, pump down to operating vacuum.
2. **Focus electron image (at 7 mm 'Z' distance).**
3. Put the cross hair under a known feature, focus, **link and move 'Z' to 5 mm.**
4. Use **5 kV, 1.6 nA** electron beam for Pt deposition using electron beam.
5. **Tilt stage to 7º**. If the cross hair moves too far from the earlier location, go to the third window and move the hair up or down to bring it back under the known feature. This way we set eucentric height.
6. **Now tilt the stage 52º (T).**
7. Insert Pt needle. Make sure Pt needle is warm before you insert.
8. In the 1st window (electron screen) make a rectangle 10x2x2 µm and set it to e-deposit surface for 5 minutes.
9. **Once done, change electron beam and ion beam shift to 0 (zero).**
10. Move to a nearby area (away from area of interest), unpause the ion beam at **0.5 nA** and focus it.
11. Use the beam shift in electron beam and bring the cross hair to the same place as the cross hair in ion beam image.
12. Bring electron beam cross hair to the center location of where the electron beam Pt is deposited.
13. Refresh to ion beam to ensure that ion beam and electron beam are in the same location.
14. Draw a rectangle in the ion beam screen, 12x2x2 µm and **deposit Pt at 0.5 nA** (should take 2-3 minutes)
15. **Withdraw the Pt needle.**
16. **Change ion beam current to 20 nA.**

17. Using e-beam move away from the area of interest and focus with ion image. It won't get crisp and clear but fairly visible to cut the trench. Pause the ion image as quickly as possible.
18. Unpause the electron beam and make sure bother images are aligned.
19. Draw a rectangle cross section 2-3 µm away from the area of interest 15x15x4 µm and start **cut at 20 nA.**
20. When done, rotate the rectangle 180º, place it on the other side and repeat step 19.
21. Change the ion beam **current to 7nA**. Open focus box on the **bottom 1/3rd of the ion image** and focus. Make sure you are at a safe distance from the area of interest.
22. Refresh the ion beam screen once at 1000x magnification.
23. Using cleaning cross section clean the area within the trench. Use a box ~15x12.5x1 µm **at 7 nA.** It should not take longer than a couple of minutes.
24. Repeat step 23 on the other side after rotating the box 180º.
25. **Tilt the stage to 7º**. Reduce ion beam current to 3 nA.
26. Move the area of interest to the side of the screen using electron beam while the Pt layer is still slightly visible. While you can still see the sample in the ion beam screen focus it at **3 nA**.
27. Move back to the area of interest and refresh the screen only once at 10,000x or 8,000x magnification such that the area of interest is in the middle of the screen.
28. Draw two rectangles where the U-cut is desired.
29. Press parallel cut to process the cuts simultaneously.
30. Make sure the two rectangles overlap and are not too far into the glass layer.
31. Change time to a couple of minutes and press play. While cutting change the contrast so that the cut is visible. When it is done stop the cut.
32. **Tilt the stage back to 0º and 'Z' to 7 mm. Ion current must be 50 pA.**
33. Insert omni probe and Pt needle (sequence does not matter).
34. Zero both tilt shifts (ion beam and electron beam)

35. Using electron beam focus the cross hair to the corner of the sample where you want to attach the needle.
36. Use **negative 'Z'** axis to move omni probe right above the cross hair.
37. Use 'X' axis to make fine adjustments.
38. Watching the 'Z' distance value slowly bring it from **7 mm to 5.6 mm**.
39. Realign the cross hair to corner of the sample by double clicking in the electron beam window and omni probe right over it.
40. Adjust the ion beam current to **50 pA**.
41. Unpause the ion beam, reduce contrast and use beam shift to shift the edge of the omni probe needle to cross hair.
42. Demagnify the ion window such that you can see the lift out area and the needle in the middle of the screen. Focus as needed.
43. Move stage up very carefully as the ion beam is unpaused.
44. When about **50 µm from the sample**, stop moving the stage up and refresh the electron beam.
45. Using electron beam make sure the needle is at the sample edge.
46. Unpause the ion beam and move stage up slowly till about **10-15 µm** away from the sample.
47. On second tab, change actual to relative and change **'Z' from 0 to -0.001 mm (1 µ)** and press go to.
48. Keep refreshing the electron beam and hitting go to till the omni probe needle just touches the sample. Move final micron or half till its touched.
49. Draw a small rectangle to cover both sample and the needle (~1x1x1 µm)
50. Change to Pt, go to advance tab, **change overlap to 50%.** Deposit ion beam Pt for about a minute.
51. Beam shift ion beam till the same is still attached to the bulk at **50 pA**.
52. Change ion beam to **1 nA.** Refresh such that only the uncut end of the sample is visible.
53. Cut the remaining area using the rectangle so that the sample is free from the bulk.

54. Change the coordinates to relative and change '**Z' to 0.001 <u>(positive)</u>** and press go to once. During this electron beam must be unpaused and the sample is visible. Repeat few times till the sample is out of the trench.
55. Move stage down using 4th screen. When clear retract the omni probe out using **<u>positive</u> 'Z' half way.**
56. Remove both needles.
57. Move to the TEM grid. **Make sure the 'Z' movement is deactivated.**
58. Choose the area on the grid and focus where sample needs to be placed. **Link it.**
59. **Move to 7 mm 'Z' distance** and insert both needles.
60. Using negative 'Z' put omni probe all the way in the center.
61. Change ion beam current to **50 pA**. Unpause ion beam. Focus cross hair to where you want to attach the sample using beam shift at **50 pA**.
62. Demagnify all the way to minimum magnification and position the sample such that it would slip into the grid just to the side of the post.
63. Beam shift to the edge of the sample.
64. Click on the screen to move the sample to just touch the post on the grid. Up and down using electron beam and sideways using ion beam.
65. Deposit Pt to stick sample to the grid for about **2 minutes with 50% overlap**.
66. Beam shift in the ion beam where you can see needle and Pt.
67. Change ion beam current to **1 nA**, make a rectangle and cut the weld. Unpause so that the cut is visible.
68. Retract omni probe using 'Z' all the way and then remove both needles.
69. Now the sample is ready for final thinning.

FIB final thinning procedure:

1. Plan to perform final thinning and polishing in **3-5 steps**.
2. Use a small section away from the post for final thinning to make sure that even if a part is damaged, there is more specimen left that can be used for imaging.
3. The first layer maybe milled at relatively high current of **0.5 nA.** Mill with this current only on one side of the specimen (preferably the side facing the operator)
4. Take the current down to **120 pA** and with the stage tilted to **53.5º** mill approximately **50 nm** layer.
5. Change to stage angle to **50.5º** and mill **50 nm** from the far side.
6. Repeat step **4 and 5 2-3 times** till the sample is approximately **100-120 nm** thin.
7. Reduce beam current to **70 pA** and repeat **step 4 and 5 1-2 times** milling approximately **20 nm** at a time.
8. Be very careful with step 7 since there is largest probability of damaging the sample during this step. Keep the ion beam screen paused and refresh electron beam every few seconds to make sure the specimen is not getting damaged and areas of interest are not getting burnt.
9. Once the specimen with thickness of **50-70 nm** is ready low voltage beam clean up maybe performed.
10. Change stage tilt angle to **52º.** Reduce ion beam voltage to **5 kV** and beam current between **1 and 2.5 nA.** Unpause the ion beam screen (Lower magnification to ensure the entire specimen is visible on the screen).
11. The specimen at this point will be barely visible and definitely very difficult to focus. Get the best focus possible and run the low voltage beam for 2-3 minutes. Keep refreshing electron screen to make sure there is no damage to the area of interest from final clean up.
12. Step 11 would remove most surface defects that are induced by the earlier aggressive milling steps.

3.2. Films deposition of CdTe films with Electron Reflector

Higher band gap $Cd_{1-x}Mg_xTe$ is being investigated as a prominent candidate for electron reflector (ER) layer. Deposition of $Cd_{1-x}Mg_xTe$ thin films has been carried out using physical vapor deposition (PVD) in the past. But using PVD method for such films gives slow growth rate and poor spatial uniformity. Therefore close-space sublimation that can deposit CdTe based films with greater rate and better spatial uniformity had to be developed. Co-sublimation of CdTe and Mg onto a single substrate was made possible with appropriate hardware. A schematic diagram of such co-sublimation source is shown in figure 3.3. This design stacks two thermally independent sublimation sources and connects them through a vapor feed. The vapor feed provides a conduit for flux of the bottom source to reach the substrate. Valves in the conduit could be used to cut off the feed as needed. Source temperatures control both vapor fluxes and the overall growth rate.

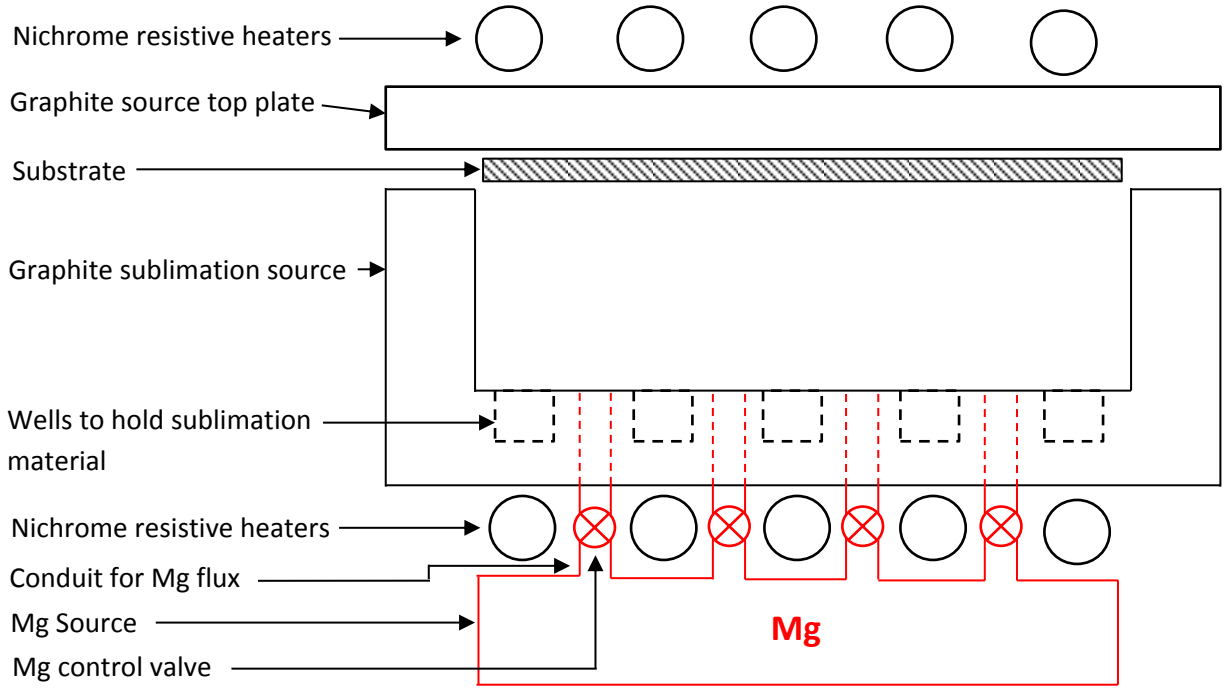


Figure 3.3. A schematic diagram of graphite vapor source for sublimating $Cd_{1-x}Mg_xTe$, CdTe, $CdCl_2$ and CuCl

This stacked source design will be referred to as “co-sublimation source” and the process as “co-sublimation” in this manuscript.

This source gives several advantages. The films could be graded by slowly opening or closing the valves gradually. Slow grading from CdTe to $Cd_{1-x}Mg_xTe$ should reduce potential interface states that could lead to recombination. The use of this source design is not limited to Mg and CdTe deposition. Other source materials may be incorporated to form various ternaries and quaternaries. This design may also be used for slow doping. Proportion of Mg can also be altered by changing the temperature of the Mg source and that may act as a useful tool in control of band gap of $Cd_{1-x}Mg_xTe$.

A.3. SPUTTER DEPOSITION OF $MG_{1-X}ZN_XO$

$Mg_{1-x}Zn_xO$ films were deposited using a Plasma Enhanced Sputter Deposition system developed and operated at PV Manufacturing Laboratory. The process was carried out at 5mTorr pressure of process gas that was 1% O_2 in Ar. Deposition was carried out at room temperature. Approximately 10 minutes of deposition at 180 Watts gave the desired film thickness of 50 nm. The target was set at a distance of 15 cm from the substrate and a shutter mechanism was used to ensure cutting off deposition was prompt at the end of desired time.