THESIS

THERMOELECTRIC PROPERTIES OF SI/SIC THIN-FILM SUPERLATTICES GROWN BY ION BEAM SPUTTERING

Submitted by

Corson Lester Cramer

Department of Mechanical Engineering

In partial fulfillment of the requirements

For the Degree of Master of Science

Colorado State University

Fort Collins, Colorado

Spring 2015

Master's Committee:

Advisor: John Williams

Walajabad Sampath
James Neilson

ABSTRACT

THERMOELECTRIC PROPERTIES OF SI/SIC THIN-FILM SUPERLATTICES GROWN BY ION BEAM SPUTTERING

There are many mechanical systems that convert heat to work and processes that utilize heat including power plants, automobiles, and foundries. Most of these systems expel large amounts of waste heat to the environment that goes unused. One way of recovering the waste heat is to use a solid-state energy converter based on thermoelectric processes. Nano-scaled materials are of interest for use in thermoelectric devices because their properties enhance the efficiency over those obtained using bulk materials. Some nano-scaled materials systems being considered are thin-film superlattices that utilize quantum confinement effects. Thin-film, superlattice thermoelectric devices could revolutionize traditional heat-to-work systems and heat-only processes if they are coupled to the systems to recycle a fraction of the waste heat into usable power. The advantage of thermoelectrics over traditional mechanical systems is that they use solid-state processes instead of moving parts and working fluids. As a result, they can be made to be more reliable and require less maintenance. This thesis focuses on the characterization of a thin-film, superlattice (SL) thermoelectric material formed by alternating silicon and silicon carbide layers to form an n-type quantum well. Superlattices of 31 bi-layers of Si/SiC (10 nm each) were deposited on silicon, quartz, and mullite substrates using a high-speed, ion-beam sputter deposition process, and the Seebeck coefficient and electrical resistivity are measured as a function of temperature and used to compare film performance. In addition,

SL layer thicknesses of 2 and 5 nm were deposited on mullite to determine the effect layer thickness has on the thermoelectric properties.

ACKNOWLEDGEMENTS

First and foremost, my advisor, John Williams, provided a huge amount of guidance in my research and I am grateful for his input. He has been a mentor to me as a scientist, as a teacher, and as a person. His utter enthusiasm for the world around him and unbridled desire to share it with everyone he meets is contagious.

I would also like to express my gratitude to my committee members. Professors Walajabad Sampath and Jamie Neilson have not only served on my committee, but also made themselves available when my research crossed into their respective specialties. They are also gifted educators, and I was privileged to take classes from them.

I want to acknowledge the members of the CEPPE Laboratory for their help and support over the past five years. Mrs. Daisy Williams was always who I turned to when something absolutely had to get done, and she provided enough chocolate and summer vegetables from her garden to get me through. Drs. Casey and Cody Farnell were constantly willing to offer technical assistance, especially in my brief forays into coding and data acquisition. I would like to thank Mr. Jack Clark for his excellent technical research help in surface characterization and Dr. Roy Geiss for help in preparing professional SEM and TEM images of my materials. I would like to thank Joseph Fellows of Ceramtec for providing mullite substrates. My special thanks go out to the graduate students and research scientists who have come through the CEPPE Lab during my tenure for the office conversation and Ping-Pong games.

I want to convey my heartfelt appreciation to my family and friends for their encouragement over the past years. My parents, Scott and Joanie, exceeded all

expectations of generosity and support when I conveyed my goals of attaining higher degrees in engineering. I would really like to thank my grandfather, Lester Cramer, for being a driving force in my life for all my endeavors. I would also like to express my appreciation of support from my siblings Katelyn Wyatt, Storrie Cramer, and Hayden Cramer.

TABLE OF CONTENTS

LIST OF FIGURES

1 Introduction

Energy, in the form of heat and electricity, is an integral part of modern life for humans. We depend on energy sources like power plants and powered vehicles to get us through our everyday lives. Over time, there has always been an increasing demand for energy and the direct conversion and storage of it. An estimated 1.1×10^{14} kW-hr of energy is produced every year by human activities, and a majority of this energy is provided by sources such as coal, oil, natural gas, nuclear, hydro, and biofuels as shown in Figure 1.1 [1]. In a more understandable perspective, this energy consumption rate corresponds to 40 kW-hr per person per day, which is slightly higher than the average house hold usage in the United States of 20 kW-hr per day.

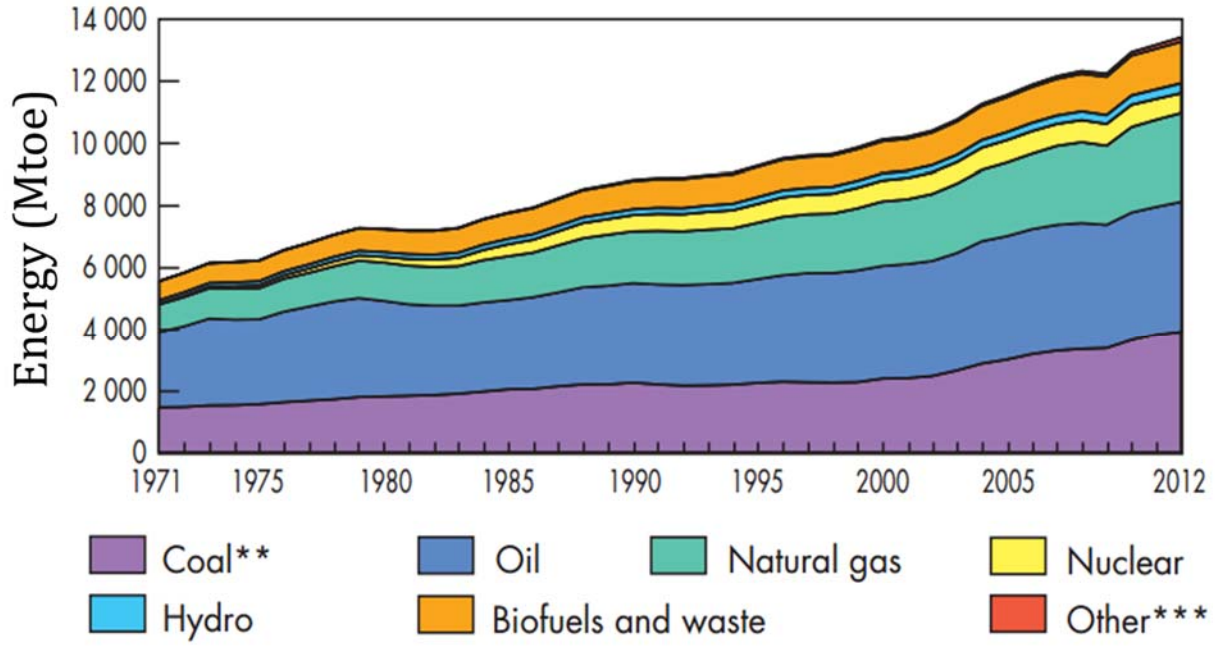

Figure 1.1: World total energy supply from 1971 to 2012 by fuel in Mtoe [1].

Harnessing enough energy in a reliable and stable manner in an ever increasing rate is one of the world's biggest problems. Civilization has historically turned to energy sources that are finite to produce energy. These energy sources are typically converted to heat, which is then either used directly in a process or converted to useful work in a mechanical-based thermodynamic process. Most of these systems that use heat as the first step in the energy conversion process are inefficient and expel large amounts of high quality waste heat energy. It is typical that more than 75% of the original heat energy put into a system or process is wasted by means of dissipation to the environment. One simple way to capture waste heat energy is to utilize a solid-state energy converter like a thermoelectric generator that converts a fraction of the waste heat to electrical power. This process is shown in Figure 1.2.

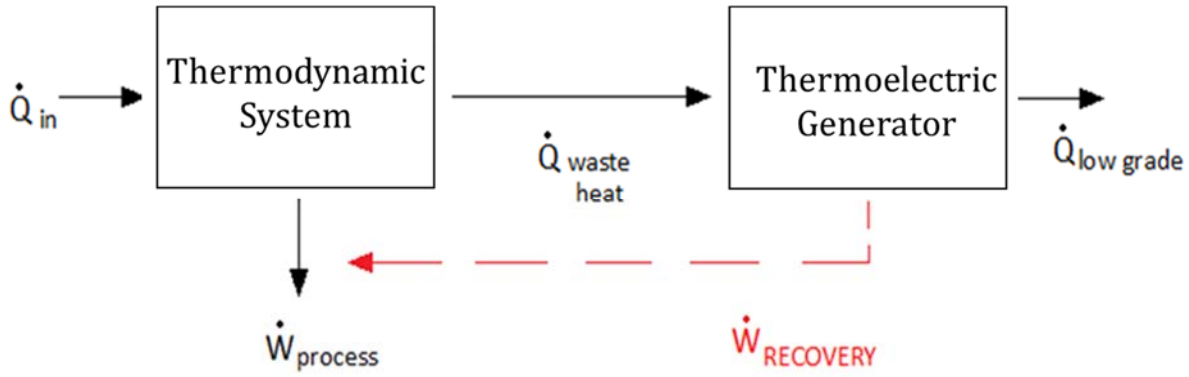

Figure 1.2: Thermodynamic system expelling heat that is partially recovered by a solid state energy converter.

Solid state energy conversion is attractive because it uses no moving parts or working fluids as in conventional turbo machinery- or internal combustion, engine-based, energy conversion systems. This thesis focuses on the characterization of a material that is intended for use in a thermoelectric generator. A thermoelectric generator is a device that utilizes a heat source to induce a temperature difference across its internal, hermetically-

sealed components. The temperature difference causes a voltage to be built up that can be used to drive current through an external load to capture useable power in the form of electricity.

Since the discovery of the Seebeck effect in 1821, which is the voltage resulting from a temperature difference imposed across a material, there was little progress in TEG efficiency above 1% until semiconductors and semi-metals were utilized in the early 1950s [2]. This is because the early materials used to exploit the thermoelectric effect were metals, which have low Seebeck coefficients in general [2]. Efficiencies improved in the 1950s and 1960s to the 2-4% range with semi-metals but stagnated until 1996 when nano-scaled and structured materials were proposed and investigated. A time line of the Figure of Merit versus time is shown in Figure 1.3.

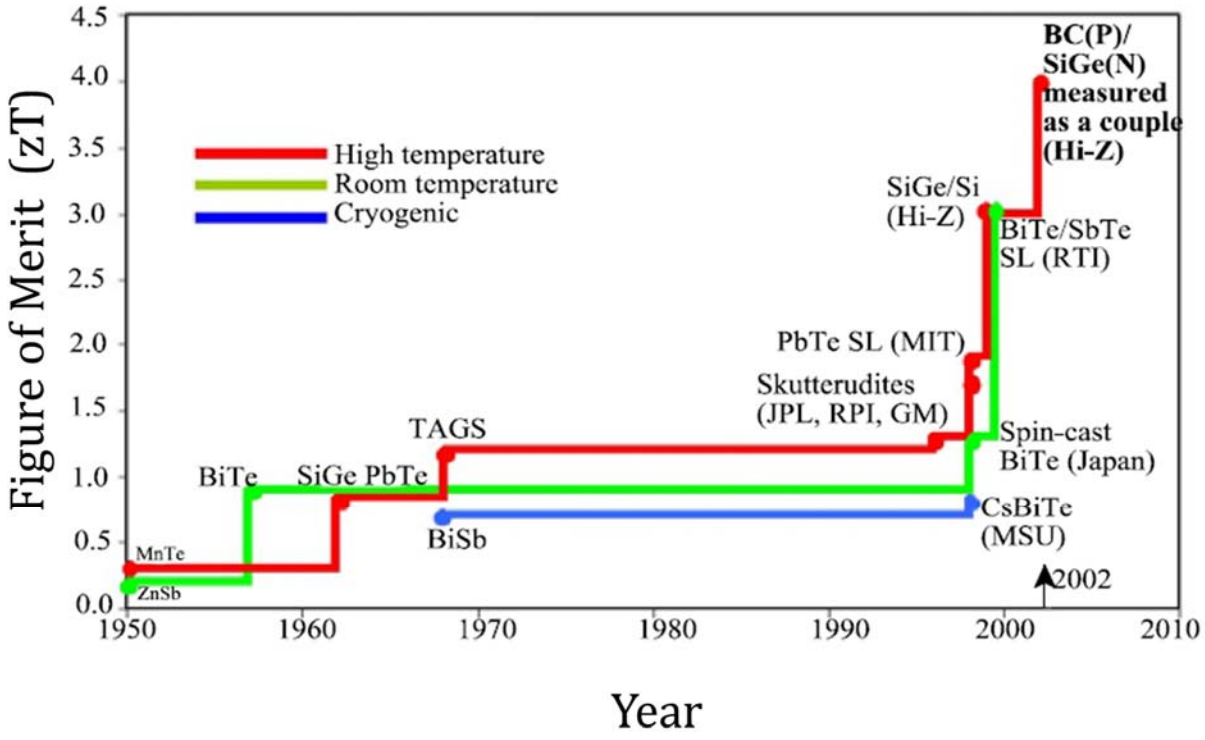

Figure 1.3: Time line of thermoelectric progress in terms of the Figure of Merit, which is a parameter that is discussed later in this thesis [2].

As indicated in Figure 1.3, nano-scaled materials show high promise for thermoelectrics due to the tradeoffs with the properties that determine efficiency and theoretical studies suggest that nano-scale technology could push TEG efficiency into the 10% and higher range. The nano-structured materials highlighted in Figure 1.3 are superlattice configurations that will be described below. Some of these data have come under scrutiny due to difficulties in the independent reproduction of results, and this thesis addresses some of the concerns that have been raised.

There are two ways to fabricate nano-scaled thermoelectric materials, one of which is a self-arranging, nano-scaled structure that scatters phonons to limit heat conduction and has favorable band structure for enhancing Seebeck coefficient and electrical conductivity [3]. The other approach is based on applying engineering principles to form ordered quantum confinement features like those in quantum superlattices, wires, and dots. Superlattices are periodic, alternating layered structures of two or more materials that have epitaxial and single crystal growth. In our case, the films are not single crystal nor epitaxial, but we will refer to our films as SLs because this is the historical conventional term for these multilayers found in the literature, and previous studies of thin-film multilayers of Si/SiC have used the term superlattices. To fabricate organized nano-scaled materials like superlattices, proven micro-electronics-based manufacturing methods such as magnetron and ion beam sputtering can be used to speed fabrication and reduce production costs. In a thermoelectric generator module, there are two legs comprised of n-type and p-type materials that are polarized oppositely when a temperature difference is imposed across them. The research presented in this thesis is focused on characterization

of a high temperature, n-type, nano-scale, thin-film, superlattice (SL) material system that has the theoretical promise to achieve high efficiency.

The following sections contain information on thermoelectricity, TE device configuration, and efficiency metrics. Next, a summary of advanced TE materials is presented along with a brief discussion of theoretical concepts of material properties that affect TE device performance.

1.1 Thermoelectricity

The thermoelectric effect encompasses the Seebeck, Peltier, and Thomson effects. The Peltier effect is a temperature difference caused at the junction of dissimilar materials when current is passed through the junction. The Thomson effect is the rate of generation of reversible heat in a material with an imposed current flow and temperature gradient. The Seebeck effect is a voltage caused by a temperature difference imposed between the point where two dissimilar materials are joined and their free ends. The Seebeck effect is easiest to understand by considering the thermocouple setup in Figure 1.4. There are two junctions at a reference temperature (T_1), and the ends of the two dissimilar metals form another junction to be placed in the sense area (T_2). The two dissimilar metals are wired to add the voltages induced by the temperature difference, which can be calibrated to a temperature. The Seebeck coefficient is defined in Equation 1.1 as the derivative of the voltage with respect to the temperature difference [4]. It is the most important materials property for TE materials because of its strong influence on energy conversion efficiency.

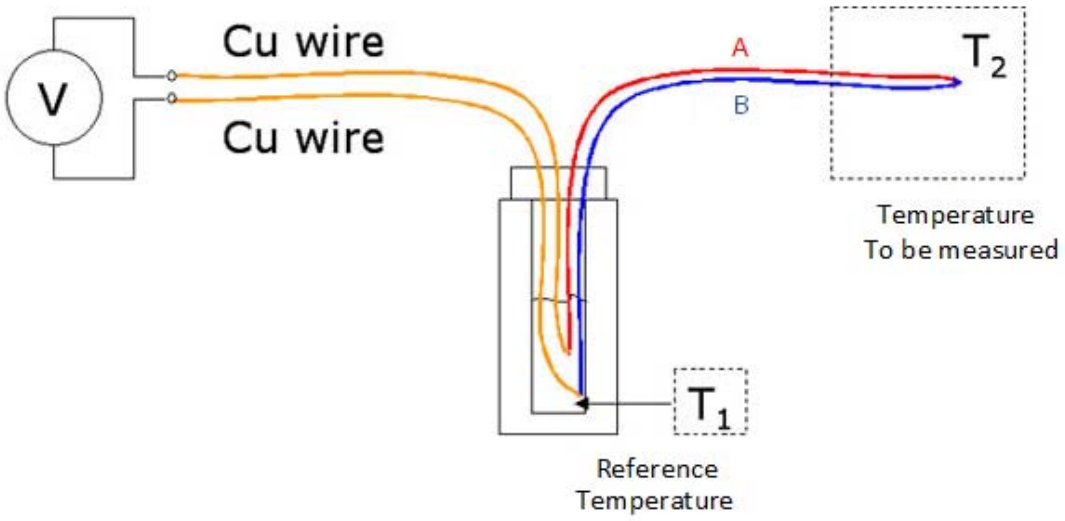

Figure 1.4: Schematic of a thermocouple utilizing the Seebeck Effect. Voltage will build up when the ends of the different materials are at different temperatures.

$$\alpha(T) = \frac{dV}{dT} \tag{1.1}$$

Thermoelectric power generation can be explained by performing an energy balance at the hot and cold side junctions of a TEG device like the one shown in Figure 1.5. The net heat supplied to the hot junction, q_H, and the net heat removed from the cold junction, q_C, are shown in Equations 1.2 and 1.3, where $\bar{\alpha}_{pn}$ is the average Seebeck coefficient of the couple, I is the current, T_H is the hot side temperature, K is the total thermal conductance of the couple, and R_g is the total internal resistance of the couple.

$$q_H = \bar{\alpha}_{pn} T_H I + K\Delta T - \frac{1}{2} I^2 R_g \tag{1.2}$$

$$q_C = \bar{\alpha}_{pn} T_C I + K\Delta T + \frac{1}{2} I^2 R_g \tag{1.3}$$

The heat supplied to the hot side is broken down into three components, the Peltier cooling, conduction cooling, and joule heating. The charge carriers get promoted to a level where they can conduct electricity and heat, and this energy promotion consumes heat and is referred to as the Peltier cooling term. One can think of the Peltier cooling at the hot junction as the act of blooming electrons in the n-type leg and holes in the p-type leg that then diffuse to the colder junction. The n- and p-type leg materials conduct heat via phonon lattice vibrations and electronically by electrons and holes. The TEG legs also heat themselves due to current flow, I, that is referred to as Joule heating. As mentioned above, the blooming of holes and electrons creates a buildup of carriers on the hot ends of the n- and p-type materials, which creates a concentration gradient. The carriers then diffuse toward the cold side causing current to flow. Simultaneously, some heat is conducting to the cold side. The total Joule heat is I^2R_g, and half of this term is traditionally assigned to the hot junction, and it reduces the amount of heat that needs to be supplied to the hot junction to maintain the hot junction temperature. When an external load completes the circuit, the carriers that were created at the hot side can then flow to the cold side and be recombined sustaining a current when the temperature difference is imposed across the TE device. The heat removed from the cold side is also broken down into three components, the Peltier heating, conduction heating, and joule heating. In the case of the cold side, the one-half of the Joule heat is required to be removed, and, consequently, it increases the amount of heat that must be removed at the cold junction to maintain the temperature there.

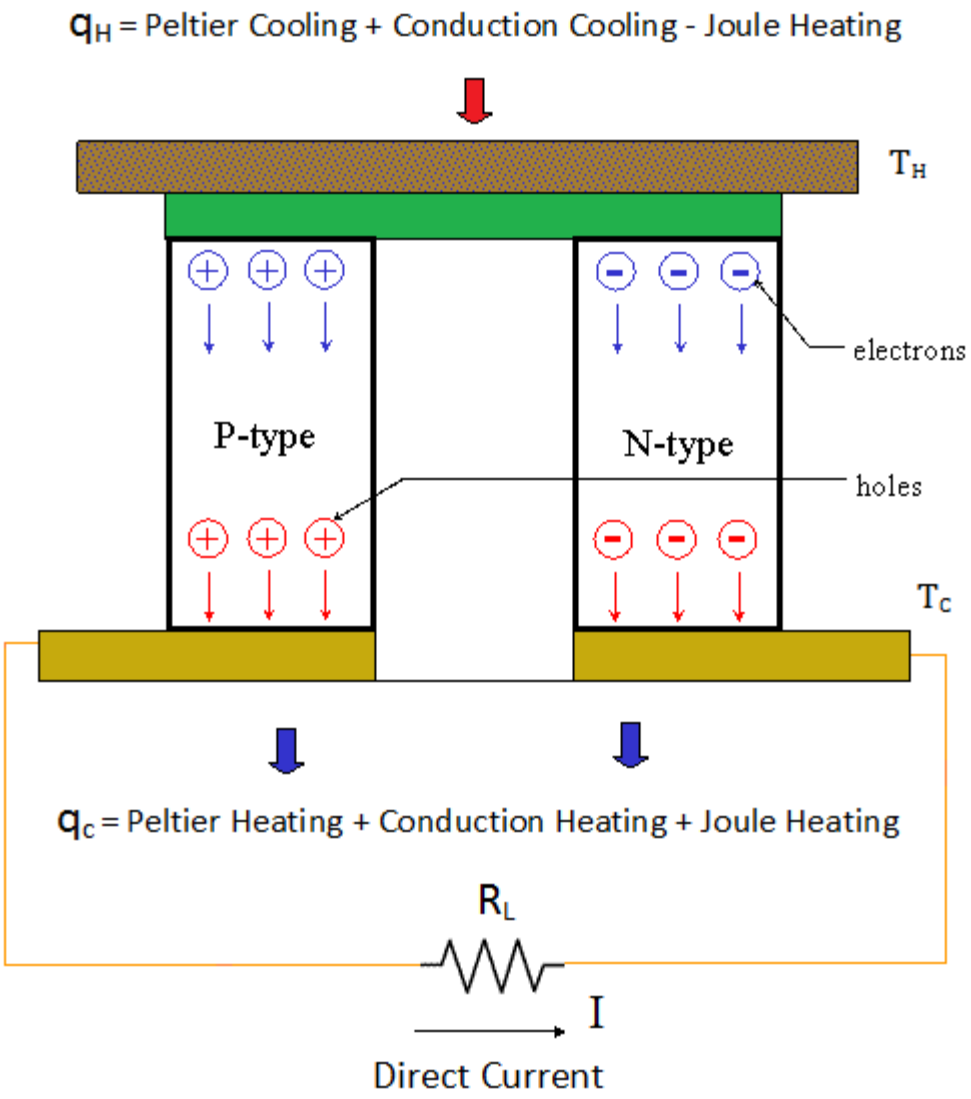

Figure 1.5: Thermoelectric Generator.

1.2 Thermoelectric Efficiency Metrics

Thermoelectric materials are ranked according to a parameter called the non-dimensional figure of merit, zT. This parameter is defined in Equation 1.4, where α is the Seebeck coefficient in V/K, T is the temperature in K, ρ is the electrical resistivity in Ω-m, and κ is the total thermal conductivity in W/mK due to steady state phonon and electronic

heat transport. These parameters will be discussed throughout this thesis as we move into characterization of thin-film, quantum-well-superlattice thermoelectric materials.

$$zT = \frac{\alpha^2 T}{\rho k} \tag{1.4}$$

The figures of merit for several semi-metal, n-type thermoelectric materials are shown in Figure 1.6. The material with the highest zT is nano-structured PbTe, which is 80% higher than bulk PbTe, which has been used since 1960 [5]. Figure 1.6 shows that Bi_2Te_3 is best for low temperature applications no higher than 250°C, and, although PbTe can be used in lower temperature ranges like Bi_2Te_3, it works best in the 400-600°C range. Finally, the semi-metals $CoSb_3$, La_3Te_4, and SiGe are best used in higher temperature applications.

The non-dimensional figure of merit, zT, is a property of a material at a given temperature. Another related quantity that is used to describe the performance of a TE couple in the configuration shown in Figure 1.5 is the figure of merit for a couple, ZT, which is defined in Equation 1.5, where $\bar{\alpha}_{pn}$ is the average Seebeck coefficient of the module for both legs over the temperature range from T_C to T_H, T is the average of T_C and T_H, R_g is the total resistance of the n- and p-type legs, and K is the total thermal conductance [4].

$$ZT = \frac{\bar{\alpha}_{pn}^2 T}{R_g K} \tag{1.5}$$

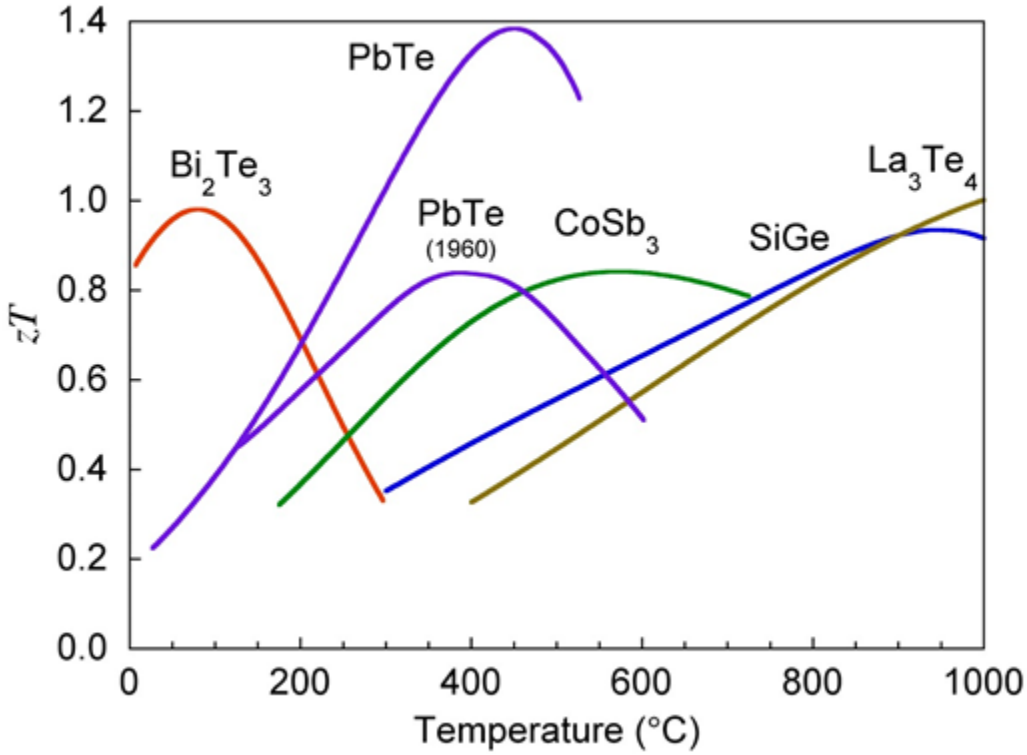

Figure 1.6: zTs of common thermoelectric materials [5].

The thermal efficiency is defined as the total amount of work done by the system divided by the heat supplied to the hot side of the couple. The resistance of the load, R_L, can be used to obtain the total work generated by the system. With some algebraic manipulation of the definition of the efficiency as shown in Equation 1.6, the efficiency can be put in terms of temperature and ZT.

$$\eta_t = \frac{w}{q_H} = \frac{q_H - q_C}{q_H} = \frac{\bar{\alpha}_{pn}\Delta T I - I^2 R_g}{\bar{\alpha}_{pn} T_H I + K\Delta T - \frac{1}{2} I^2 R_g} = \frac{I^2 R_L}{\bar{\alpha}_{pn} T_H I + K\Delta T - \frac{1}{2} I^2 R_g} \qquad (1.6)$$

$$\eta_t = \frac{\left[\sqrt{1+ZT} - 1\right][(\Delta T / T_H]}{\sqrt{1+ZT} + 1} \qquad (1.7)$$

The efficiency calculated using Equation 1.7 is shown in Figure 1.7 as a function of ZT and the hot side temperature, and Figure 1.7 shows that the efficiency increases as the

hot side temperature is increased for a fixed cold side temperature of 300°C. Also, by increasing the module figure of merit, the efficiency increases as well [4]. The thermoelectric efficiency is a fraction of the Carnot efficiency, ($\Delta T/T_H$), so the maximizing parameter is the material properties and the geometry of the n- and p-type legs. The main point to draw from Figure 1.7 is that in order to increase the couple ZT, the zT of the materials must be increased. The plot shows that 30% efficiencies are achievable at a temperature difference of 1150°C – 300°C and at a module ZT of about 4. As of now, the best TEG devices have a ZT of about 1 and operate at a relatively low temperature and small temperature difference. For example, a module made of PbTe can operate in the 400°C range based on Figure 1.6, so, if the hot side is maintained at 550°C and the cold side is maintained at 300°C, then the efficiency is only about 7%. The four-fold increase in efficiency from about 7% to 30% is necessary to bring thermoelectric-based energy conversion systems into common use, and this thesis is focused on the characterization of a nano-structured material system that shows the potential for achieving this goal.

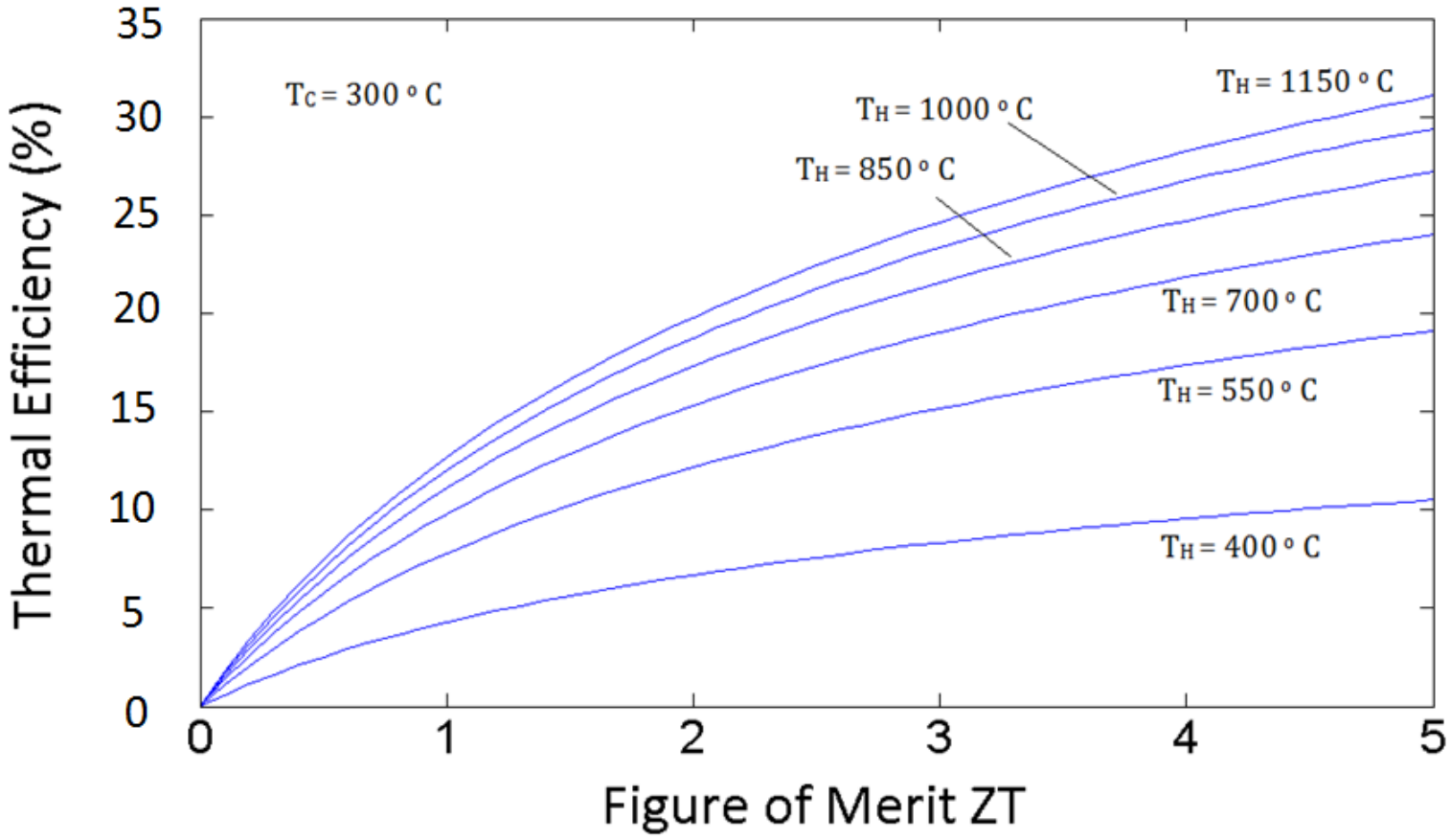

Figure 1.7: Curve of the thermal efficiency of a thermoelectric generator as a function of the figure of merit and hot shoe temperature. The cold shoe temperature is assumed to be 300 K.

1.3 Background of Advanced TE materials

As mentioned earlier, a superlattice is a promising material concept for achieving high thermoelectric (TE) efficiency, where each leg in a module is composed of thousands of nanometer-scale thick bi-layers as shown in Figure 1.8. Superlattice systems, such as the n-type Si/SiC films described herein, aim to take advantage of quantum-scale effects. The superlattices are deposited onto substrates that are then metallized and brazed into a hermetically sealed module. A mockup up of the process is shown in Figure 1.8 along with a photograph of an early prototype module.

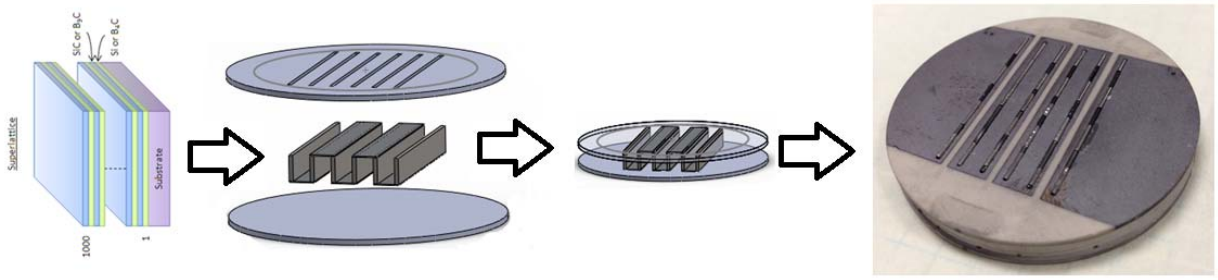

Figure 1.8: A SL-based TEG fabrication mockup and photograph of an early CSU prototype.

Theoretical work of Hicks and Dresselhaus showed that nano-scaled superlattices will display a quantum well effect that increases the carrier effective mass, which increases the Seebeck coefficient, while leaving the mobility unchanged and increasing the electrical conductivity. This theory suggested that zT values could be ~13 times higher than bulk material values [6]. In later work, Chen et al [7] and Ezzahri et al [8] both showed that electrical conductivity increases and thermal conductivity decreases in a superlattice structure. Consequently, these three studies show that all three properties of the figure of merit are affected such that the zT is increased with a superlattice structure. In related work and more recent work, Lee et al [9] show enhanced Seebeck coefficient with $SrTiO_3/SrTi_{0.8}Nb_{0.2}O_3$ superlattices, and Liu et al [10] show promising in-plane TE

properties on Si/Ge SLs. These more recent studies show increases of the figure of merit by an order of magnitude over bulk material. Also, recent data from superlattices of GaN/AlN/AlGaN grown by chemical vapor deposition at high temperature show that enhanced zT values can be obtained over bulk properties when the material is tested at room temperature [11]. Further theoretical work and testing done by Ghamaty and Elsner [12] and Balusu and Walker [13] show a decoupling of the Seebeck coefficient and electrical conductivity due to the quantum well effect, which allows zT optimization.

In addition to superlattices, Dresselhaus et al [14] show promising thermoelectric properties with nano-structured materials, such as clathrates, skutterudites, and zero- and one-dimensional, quantum-well materials. They show that the nano-structured materials enhance scattering of phonons resulting in decreased thermal conductivity. Also, these nano-scaled materials allow for controlled doping of the material to increase the electrical conductivity without detrimentally decreasing the Seebeck coefficient, which is one promising angle of research in thermoelectrics. Another angle of nano-scaled, thermoelectric materials research that has not received as much attention is the enhancement of the Seebeck coefficient at lower carrier concentrations. Theoretically, superlattices enhance the Seebeck coefficient, and, if the right materials fabrication processes are used that result in low defect concentration within the layers, the electrical conductivity could be increased as well resulting in a breakthrough in zT and thermoelectric efficiency.

The interface quality of the materials is important for superlattices, and three different deposition techniques using different particle arrival energies and background pressures have been used. Early n-type $Si/Si_{0.8}Ge_{0.2}$ and p-type B_4C/B_9C superlattices were

deposited using molecular beam epitaxy [15] and magnetron sputtering [16], but a potentially faster and cheaper method is ion beam sputtering because the ion energies are higher [17]. Furthermore, excellent thermoelectric properties have been reported for Si/SiC, Si/$Si_{0.8}Ge_{0.2}$, and B_4C/B_9C superlattices using magnetron sputtering. A module ZT near 4 at 250°C was reported for these materials [18, 19, and 20], and more recent data for Si/SiC superlattices on silicon substrates made by magnetron sputtering [21] and ion beam sputtering [22] indicates even higher zT in high temperature applications.

These findings of the Si/SiC, Si/$Si_{0.8}Ge_{0.2}$, and B_4C/B_9C superlattices are not generally accepted in the thermoelectrics community because the resistivity of the TEG material was measured when the superlattices were deposited on a silicon substrate, and the Si substrate was likely affecting the measurements. The company Hi-Z Technologies Inc. claimed thermoelectric properties that would yield a figure of merit of around 10 and has a patent for the in-plane superlattice configuration [21]. Reproducibility of the claims by Hi-Z film has been a problem because of the substrate issue; and no independent group has yet been able to achieve as low of a resistivity of the films on a non-silicon substrate. One thesis partially reproduced the Hi-Z values at high temperature, but it is likely that the same problem with the silicon substrate affected the resistivity measurements [22]. Hi-Z shows good room temperature resistivity, but in our recent studies, low resistivity at room temperature is not observed. This thesis investigates Si/SiC superlattices deposited on silicon and ceramic substrates in an effort to resolve this issue.

The additional motivation to investigate alternative substrates is to find one with low thermal conductivity that is compatible with growing high performance TEG SL films. To address this challenge, we tested the properties of the Si/SiC superlattices on three

different substrates that were deposited using a high-speed, ion-beam-deposition process. The films are characterized by their non-dimensional figure of merit, zT, where the Seebeck coefficient and resistivity are measured directly, and the thermal conductivity is estimated from the literature and justified by measurements made using a MEMS technique performed by the University of Denver [22]. Several studies have shown that superlattices in the 5-10 nm layer thickness range have thermal conductivity of less than 5 W/mK including the Aubain et al [23] study of the lattice thermal conductivity and the Mazumder et al [24] study of the total thermal conducvity at different temperatures on Si/SiC films specifically. These thermal conductivity measurements include the 3-ω transient method and the thermal reflectivity method, which are both well accepted techniques.

1.4 Thermoelectric Property Theory

If the Fermi level is the average energy of a crystal in a material at any temperature, then the ideal band structure of a thermoelectric has a sharp band or high density of states near the Fermi level to enhance Seebeck and dispersive bands to enhance the electrical conductivity [3]. This band structure of a metal with good thermoelectric properties is shown in Figure 1.9. For a good thermoelectric material, there should be high density of states near the Fermi level as in Figure 1.9, but the dispersive bands should not be cut by the Fermi level nor should they be touching.

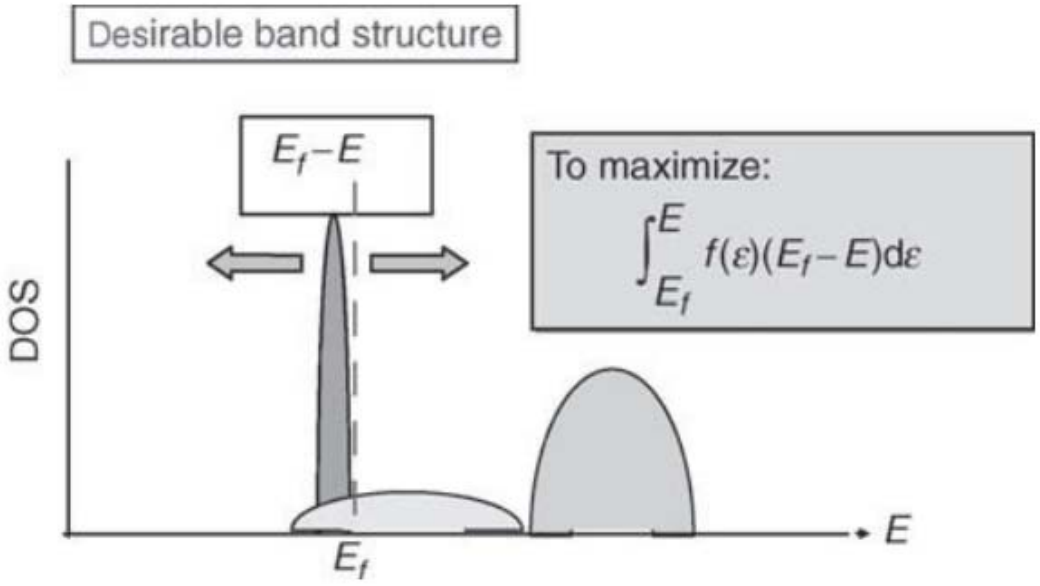

Figure 1.9: Schematic of band diagram for a metal with good thermoelectric properties [3].

Materials with relatively low carrier concentration ($n << 10^{19}$ cm^{-3}) such as semiconductors can have large Seebeck coefficients and high mobility. The relationship between carrier concentration and Seebeck coefficient can be determined from relatively simple models of electron transport. Two-dimensionally confined carriers in a superlattice quantum well whose layer thickness is close to the Fermi shell of the free carrier, exhibit quantum effects whereby the Seebeck coefficient can be increased due to increased density of states (DOS) without the other important properties decreasing [3]. Other quantum effects such as the effective mass of carriers are governed by energy surface shape in the valence and conduction bands, which can, along with carrier and phonon scattering behavior, strongly affect electronic phenomena [3]. For metals or highly doped semiconductors, the parabolic band, energy-independent scattering approximation is used to derive the Seebeck coefficient shown in Equation 1.8 where n is the carrier

concentration, m^* is the effective mass, T is the temperature, k_b is the Stefan-Boltzmann constant, h is Planck's constant, and e is the elementary charge [5].

$$\alpha = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^{\frac{2}{3}} \tag{1.8}$$

The electrical conductivity (σ) and electric resistivity (ρ) are related to the carrier density and the carrier mobility, where n is the carrier concentration, e is the elementary charge, and μ is the mobility of the carriers. The mobility gives a measure of how well the carrier will flow through the material. Ideally, if the mobility is high and the carrier density is moderate, then the Seebeck coefficient will remain high and the electrical conductivity (shown in Equation 1.9) won't be compromised, resulting in a good thermoelectric material.

$$\sigma = \frac{1}{\rho} = ne\mu \tag{1.9}$$

Figure 1.10 shows the tradeoffs between Seebeck coefficient and electrical conductivity in bulk thermoelectric materials that must be met to maximize the figure of merit. The maximum value of carrier concentration typically occurs at carrier concentrations between 10^{19} and 10^{20} cm^{-3} which corresponds to semi-metals that fall in between common metals and semiconductors in terms of carrier concentration. Our SL materials are in the concentration range for low carrier concentration semiconductors ($n < 10^{18}$ cm^{-3}), but with a high or giant Seebeck coefficient.

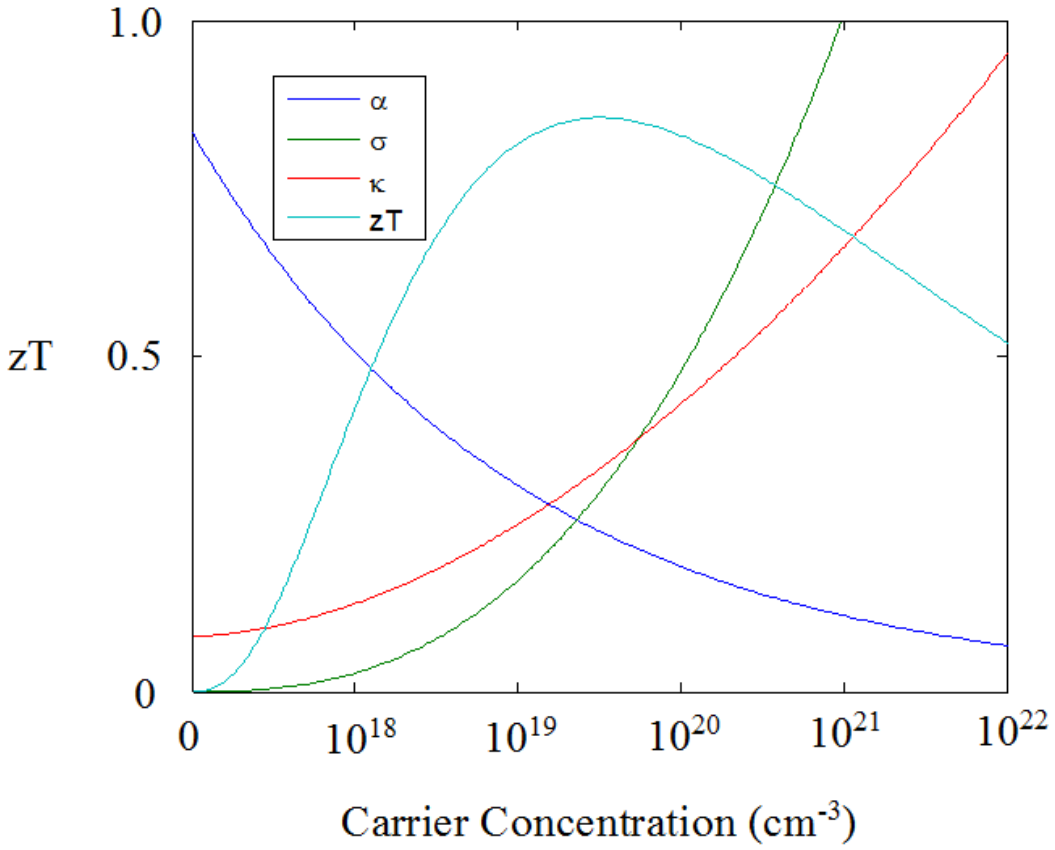

Figure 1.10: Tradeoffs of thermoelectric properties as a function of carrier density. Only typical values are shown for the zT curve. The other properties are normalized for visualization purposes. [This plot is adapted from Ref. 4.]

The effective mass of the charge carrier provides another compromise of zT because a large effective mass produces high Seebeck coefficients but lower electrical conductivity. The m^* in Equation 1.8, refers to the density-of-states effective mass, which increases with flat, narrow bands with high density of states at the Fermi surface [5]. However, the inertial effective mass is also directly to m* and the high band curvature in SL materials enhances inertial effective mass. Heavy carriers will move with slower velocities, and therefore have smaller mobility, which in turn leads to lower electrical conductivity as indicated in Equation 1.9. The relationship between effective mass and mobility is

complex, and depends on electronic structure, scattering mechanisms, defect concentration, and anisotropy [5].

Additional materials design conflicts arise from the necessity for low thermal conductivity. Thermal conductivity in thermoelectrics comes from two sources: (1) electrons and holes transporting heat (κ_e) and (2) phonons travelling through the lattice (κ_l).

$$k=k_e + k_l \tag{1.10}$$

$$k_e = L\sigma T = ne\mu LT \tag{1.11}$$

Most of the electronic term (κ_e) of thermal conductivity is directly related to the electrical conductivity through the Wiedemann–Franz law, where L is the Lorenz factor, 2.4×10^{-8} $J^2K^{-2}C^{-2}$ for free electrons [5]. There will always be a small conduction contribution from the electrons transporting heat, but the steady-state lattice term is usually the dominant term in low-carrier-concentration semiconductor materials, and reducing lattice thermal conductivity is the focus to block heat conduction. Nano-structures and SLs can significantly reduce the k_l value by factors of 10 to 100 [23, 24].

1.6 Thesis Outline

In Chapter 2, we discuss the sample preparation and ion beam sputtering process, and all measurement techniques are presented that are used to characterize zT. The results are presented in Chapter 3 where we first analyze the two different superlattice materials individually. Next, we analyze the morphology of the SL using SEM and TEM. The effect of the silicon substrate is substantial, and data explaining this effect is presented

and discussed. The materials characterization and morphology for superlattices grown on different surfaces such as quartz and mullite is then presented. Next, we present the data from different layer thicknesses on mullite substrate. Finally, the conclusion and recommendation for future work are presented in Chapter 4.

References

[1] International Energy Agency. *Key world energy statistics*. International Energy Agency, 2014.

[2] Ghamaty, S., J. C. Bass, and N. B. Elsner. "Quantum well thermoelectric devices and applications." In *Thermoelectrics, 2003 Twenty-Second International Conference on-ICT*, pp. 563-566. IEEE, 2003.

[3] Rowe, David Michael. *Thermoelectrics handbook: Macro to nano*. Boca Raton: CRC/Taylor & Francis, 2006.

[4] Angrist, Stanley W. *Direct Energy Conversion*. Boston: Allyn and Bacon, 1965.

[5] Snyder, G. Jeffrey, and Eric S. Toberer. "Complex thermoelectric materials." *Nature materials* 7, no. 2 (2008): 105-114.

[6] Hicks, L. D., and M. S. Dresselhaus. "Effect of quantum-well structures on the thermoelectric figure of merit." *Physical Review B* 47, no. 19 (1993): 12727.

[7] Chen, G., "Nanoscale heat transfer and nanostructured thermoelectrics," vol. 29, no. 2, pp. 238–246, 2006.

[8] Ezzahri, Younès, G. Zeng, K. Fukutani, Zhixi Bian, and Ali Shakouri. "A comparison of thin film microrefrigerators based on Si/SiGe superlattice and bulk SiGe." *Microelectronics Journal* 39, no. 7 (2008): 981-991.

[9] Lee, Kyu Hyoung, Yoriko Mune, Hiromichi Ohta, and Kunihito Koumoto. "Thermal stability of giant thermoelectric Seebeck coefficient for $SrTiO_3/SrTi_{0.8}Nb_{0.2}O_3$ superlattices at 900 K." *Applied physics express* 1, no. 1 (2008): 015007.

[10] Liu, W. L., T. Borca-Tasciuc, J. L. Liu, K. Taka, K. L. Wang, M. S. Dresselhaus, and G. Chen. "In-plane thermoelectric properties of Si/Ge superlattice." In *Thermoelectrics, 2001. Proceedings ICT 2001. XX International Conference on*, pp. 340-343. IEEE, 2001.

[11] Sztein, Alexander, John E. Bowers, Steven P. DenBaars, and Shuji Nakamura. "Polarization field engineering of GaN/AlN/AlGaN superlattices for enhanced thermoelectric properties." *Applied Physics Letters* 104, no. 4 (2014): 042106.

[12] Ghamaty, Saeid, and N. B. Elsner. "Si/SiGe quantum well thermoelectric materials and devices for waste heat recovery from vehicles and industrial plants." In *International Symposium on Nano-Thermoelectrics*. 2007.

[13] Bulusu, A., and D. G. Walker. "Modeling of thermoelectric properties of semi-conductor thin films with quantum and scattering effects." *Journal of heat transfer* 129, no. 4 (2007): 492-499.

[14] Dresselhaus, Mildred S., Gang Chen, Ming Y. Tang, R. G. Yang, Hohyun Lee, D. Z. Wang, Z. F. Ren, J-P. Fleurial, and Pawan Gogna. "New Directions for Low-Dimensional Thermoelectric Materials." *Advanced Materials* 19, no. 8 (2007): 1043-1053.

[15] Elsner, N. B., S. Ghamaty, J. H. Norman, J. C. Farmer, R. J. Foreman, L. J. Summers, M. L. Olsen, P. E. Thompson, and K. Wang. "Thermoelectric performance of $Si_{0.8}Ge_{0.2}$/Si heterostructures synthesized by MBE and sputtering." In *The thirteenth international conference on thermoelectrics*, vol. 316, no. 1, pp. 328-333. AIP Publishing, 1994.

[16] Yu, Tianhua, Harry Efstathiadis, Richard Matyi, Pradeep Haldar, Saeid Ghamaty, and Norbert Elsner. "Large Area Depositions of Si/SiC Quantum Well Films for Thermoelectric Generator Applications." In *MRS Proceedings*, vol. 886, pp. 0886-F04. Cambridge University Press, 2005.

[17] Zheng, Z. H., P. Fan, T. B. Chen, Z. K. Cai, P. J. Liu, G. X. Liang, D. P. Zhang, and X. M. Cai. "Optimization in fabricating bismuth telluride thin films by ion beam sputtering deposition." *Thin Solid Films* 520, no. 16 (2012): 5245-5248.

[18] Hendricks, Terry J. "Comparison of skutterudites and advanced thin-film B_4C/B_9C and Si/SiGe materials in advanced thermoelectric energy recovery systems." In *Thermoelectrics, 2005. ICT 2005. 24th International Conference on*, pp. 369-375. IEEE, 2005.

[19] Ghamaty, S., "Quantum well thermoelectrics for converting waste heat to electricity," Hi-Z Technology Inc., DOE Award De-FC26-03NT41974. Quarterly Technical Progress Report. San Diego, CA, July, 2005.

[20] Martin, P., and L. Olsen. "Scale Up of $Si/Si_{0.8}Ge_{0.2}$ and B_4C/B_9C Superlattices for Harvesting of Waste Heat in Diesel Engines," No. CONF-200308--107. Pacific Northwest National Lab., Richland, WA (US), 2003.

[21] Ghamaty, Saied, and Norbert B. Elsner. "Thermoelectric device with Si/SiC superlattice n-legs." U.S. Patent 6,828,579, issued December 7, 2004.

[22] A. L. Jurgensmeyer, "High efficiency thermoelectric devices fabricated using quantum well confinement techniques," pp. 1–44, M.S. Colorado State University, 2011.

[23] Aubain, Max S., and Prabhakar R. Bandaru. "Determination of diminished thermal conductivity in silicon thin films using scanning thermoreflectance thermometry." *Applied Physics Letters* 97, no. 25 (2010): 253102.

[24] Mazumder, Monalisa, Theodorian Borca-Tasciuc, Sean C. Teehan, Emilio Stinzianni, Harry Efstathiadis, and SLowa Solovyov. "Temperature dependent thermal conductivity of Si/SiC amorphous multilayer films." *Applied Physics Letters* 96, no. 9 (2010): 093103.

2 Experimental Methods and Measurements

The work presented in this thesis focuses on the ion beam sputtering deposition technique and measurements of thermoelectric properties at high temperatures. There are different methods of fabricating thin films such as chemical vapor deposition and physical vapor deposition (PVD). Ion beam sputtering is one method of PVD and is our method of choice due to speed and ease of fabrication. The films are deposited using ion beam sputtering in one chamber, tested for thermoelectric properties as a function of temperature in another chamber, and are transported to other facilities for more analysis. The mobility, band gap, and stress of the individual films are also measured at room temperature. In the following sections, we describe the ion beam deposition process, Seebeck coefficient and resistivity measurement apparatus, mobility measurement setup, and all material characterization techniques.

2.1 Sputter Deposition

Before installing the silicon and quartz substrates into vacuum, they were cleaned and rinsed with acetone, isopropyl alcohol, and deionized water and dried. No pre-cleaning preparation was done with the mullite substrates as they were pre-cleaned by the supplier, Ceramatec. The configuration of the sputter deposition process is shown in Figure 2.1. Inside the chamber, a stage moved targets under a stationary ion beam in order to sputter deposit different materials onto the substrates. The targets are mounted at forty-five degrees relative to the ion beam and substrate holder as shown in Figure 2.1. A second stage was used to position a mask over the substrate to control layer thickness. During deposition, the temperature of the substrates was held constant at about 500^{o}C. A titanium

getter heated to roughly 1300°C is used to lower the oxygen partial pressure during deposition. This is important when making silicon films because oxygen in the chamber will react with the silicon and produce defects. The deposition rate is slowed to 3 nm/min by lowering the ion beam energy to 300 eV during the first nanometer of growth of each layer to insure sharp interfaces and less mixing at the interfaces. The remainder of each SL layer is grown more quickly at 10 nm/min using 1000 eV ions. A total of 31 bi-layers of silicon and silicon carbide were deposited to form our superlattices.

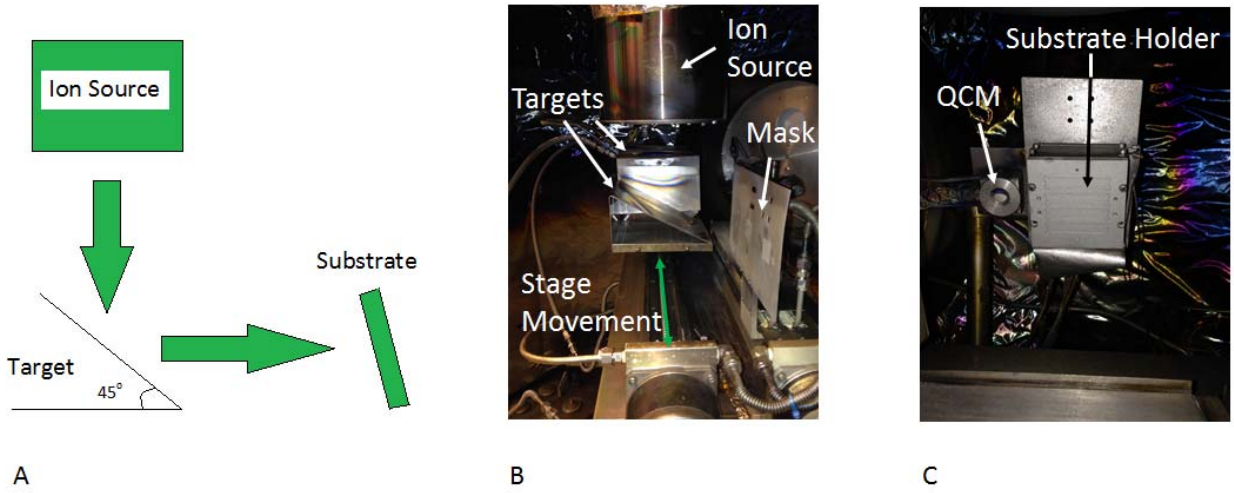

Figure 2.1: Configuration for the sputter chamber deposition setup. A is a schematic. B is a photograph showing the direction of target movement. In B, the substrate holder is behind the mask. C is a photograph of the substrate holder viewed perpendicularly to the target motion.

2.2 Seebeck Coefficient and Resistivity Measurement

After the SL films were deposited onto substrates, they were installed into a separate vacuum test facility where the Seebeck coefficient and electrical resistivity were measured over a temperature range from 300 K to 900 K. A photograph of the test setup is shown in Figure 2.2. Two substrates can be mounted onto a sample holder and tested at the same time.

The substrate holder is made of boron nitride, and a tungsten wire-based heater is used to control the temperature of each side such that a small temperature difference is established across the substrate. A maximum temperature of 800°C was possible to achieve. Resistance Temperature Detectors (RTDs) are used rather than thermocouples for measuring temperatures. Because the RTDs are embedded in a boron nitride block above the TE samples, an FEA simulation was performed to more accurately estimate the temperature at the ends of the SL where metal contacts were made.

The model predictions of the temperature difference sustained across the holder when one end of the holder is at 800°C is shown in Figure 2.3. The heater settings for this condition produced a cold side temperature that was 20 degrees lower than the hot side.

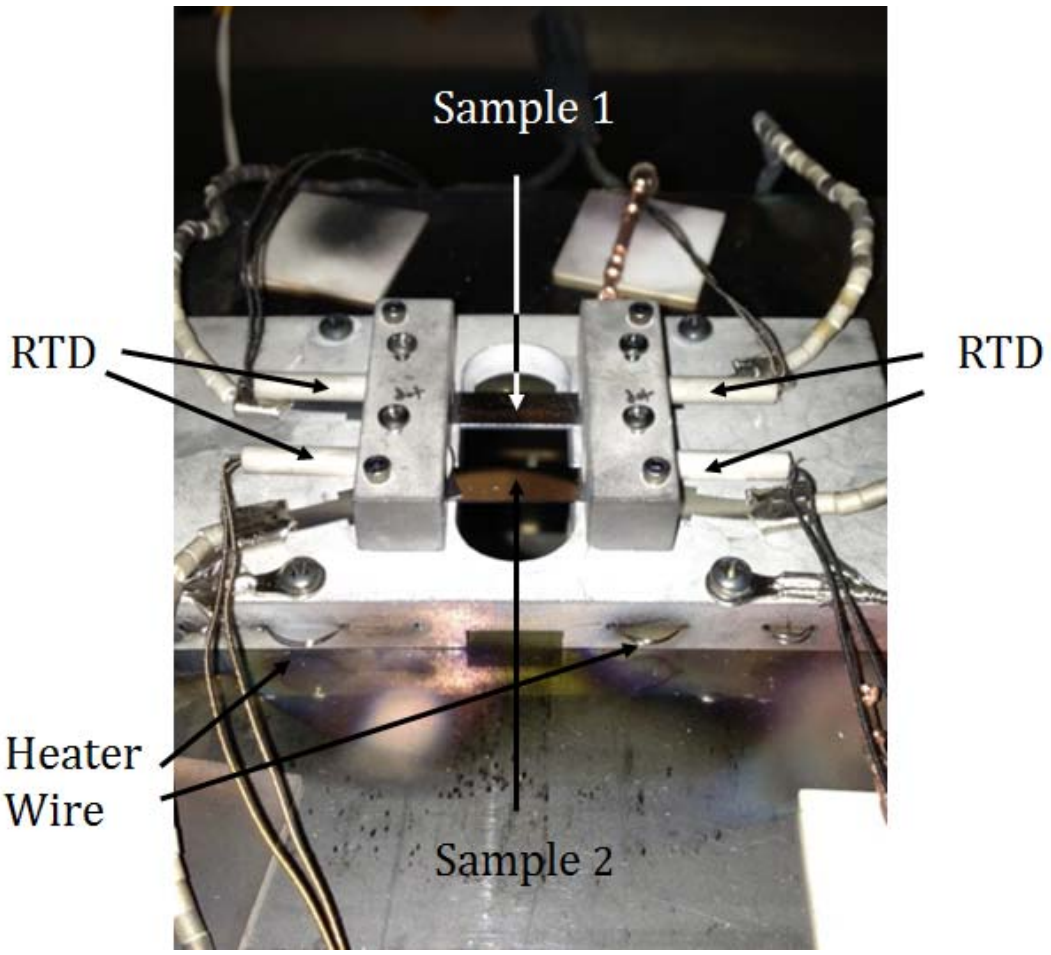

Figure 2.2: Thermoelectric Property Measurement Setup. Two samples can be tested at one time.

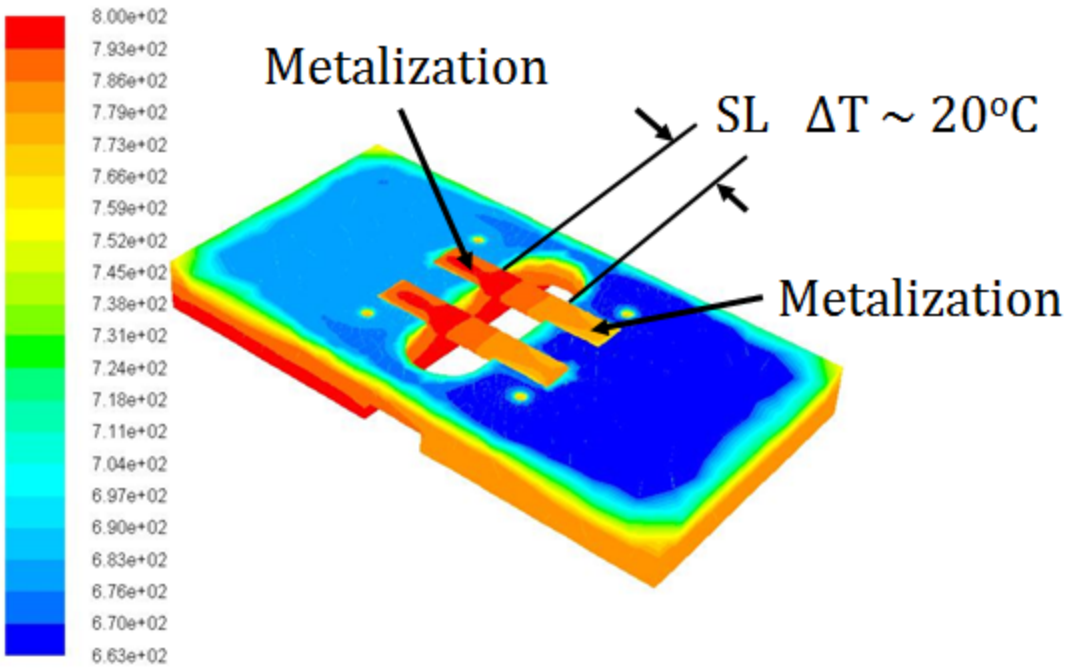

Figure 2.3: ANSYS Fluent simulation of the temperature gradient across a SL for a given heater power condition.

The holder and the substrates are modeled to predict the temperatures at the surface of the thermoelectric material using the RTD measurements as inputs. The temperature difference calibration factor was found to be 2.0. This means that the temperature difference measured using the RTDs needs to be divided by 2 to reflect the actual temperature across the SL in the region between the metalized contacts.

To measure the Seebeck coefficient, α, an induced temperature difference is needed along with a method to measure the voltage difference across the sample [1, 2]. One way of measuring α as a function of temperature is to create a temperature difference and then ramp the temperature of both sides uniformly while measuring the voltage. The Seebeck coefficient is the voltage divided by the temperature difference. The resistance, R_{SL}, of the SL can also be measured as the temperature is increased. One can calculate the resistivity

of the SL from Equation 2.1, where A is the cross sectional area of the SL calculated by multiplying the film width by the thickness, and L is the distance between the metalized ends of the sample.

$$\rho_{SL} = \frac{R_{SL}A}{L} \tag{2.1}$$

When a thermal gradient exists and the SL produces a significant voltage, a problem can occur when reading the resistance as shown in Figure 2.4. It is better to test the sample for Seebeck coefficient by inducing a temperature difference, and then test it again for the resistance with both sides of the sample held at the same temperature to minimize any problems with the resistance measurement [3, 4].

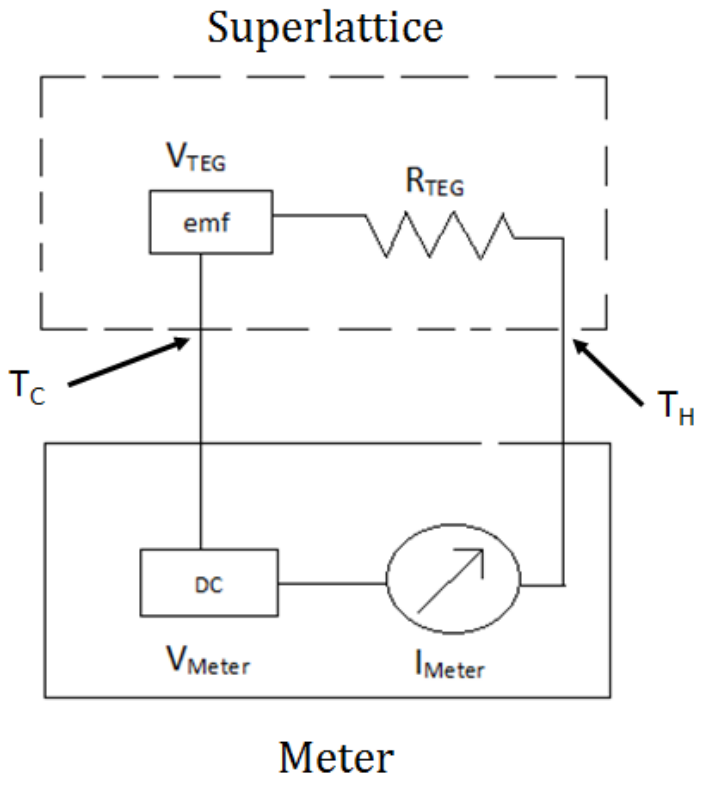

Figure 2.4: Schematic of measurement system when a SL sample is introduced to a temperature difference. It will produce its own voltage that interferes with the true resistance measurement.

2.3 Thermal Conductivity Measurements

In bulk materials, the thermal conductivity can be large because phonons, or lattice vibrations, can propagate easily through the material, but, in a nano-structured superlattice, the phonons are scattered at the layer interfaces resulting in less propagation of heat. There have been many studies that show the reduction of thin film thermal conductivity [5, 6]. There have also been studies of Si/SiC superlattice thermal conductivity specifically [7]. We used a value of 2.0 W/mK estimated from the available literature. A measurement at the University of Denver of one of our SL films was substantially lower than this value, but the data have some inconsistencies that cast doubt on the measurements [8]. To eliminate this doubt, other techniques such as the 3-ω transient and thermo-reflectance techniques can be used to measure the thermal conductivity [9, 10].

2.4 Hall Mobility Measurements at Room Temperature

The mobility was measured at room temperature using the Van Der Pauw Method with the apparatus shown in Figure 2.5. This method is a Hall measurement that uses the differences in carrier transport in an applied electric due to a changing magnetic field. Once the mobility is measured, one can measure the resistance of the film no magnetic field is applied and calculate the carrier concentration using Equation 1.9.

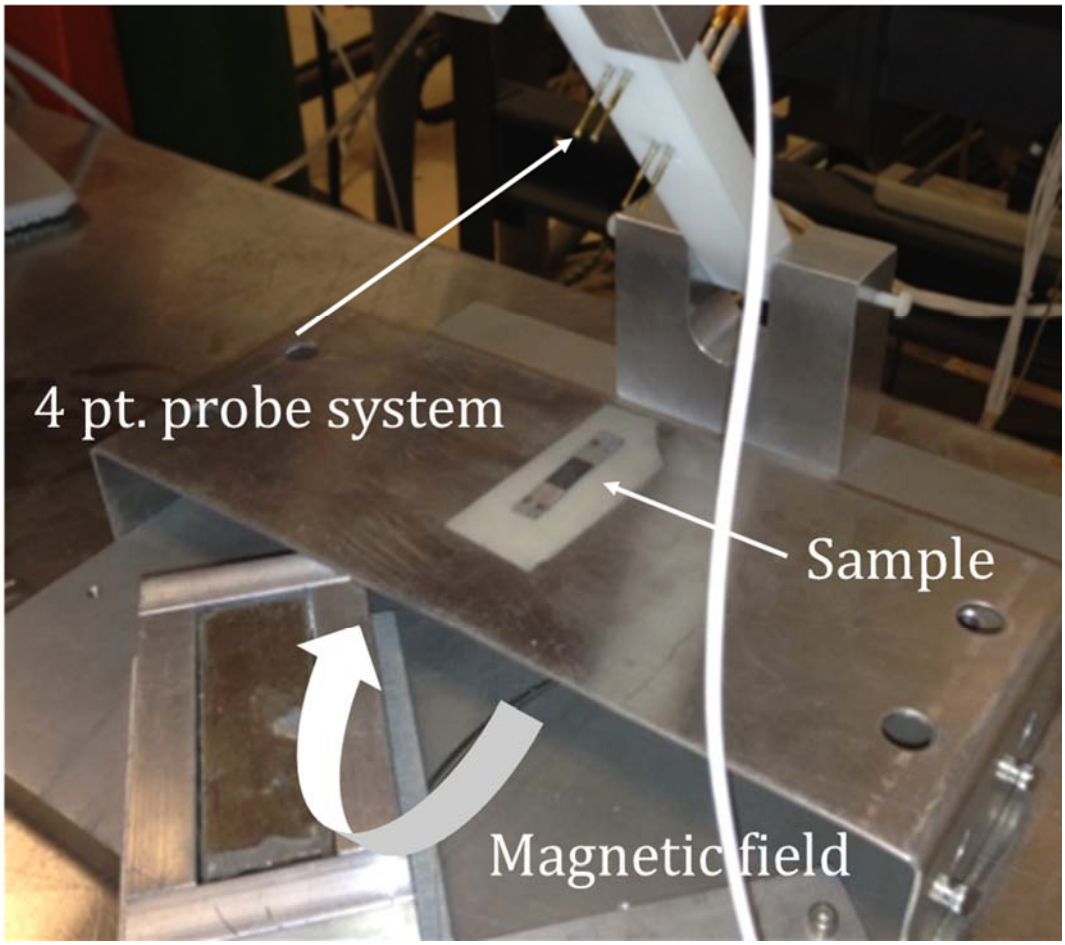

Figure 2.5: Van der Pauw Hall Measurement Setup.

2.5 Thickness of SL Films

Thickness of the SL layers is an important parameter to control. To obtain accurate layer thickness, a quartz Crystal Microbalance (QCM) was used to measure in-situ thickness [11]. SL film thickness was verified with Scanning White Light Interferometry (SWLI) and contact profilometry. Because the substrates are placed beside the QCM, there is a correction factor that is used to set the deposition time for a given layer thickness. Correction factors for Si and SiC films are listed in Table 2.1.

Table 2.1: QCM calibration for film thickness.

Material	Thickness calculated from QCM (nm)	Measured thickness (nm)	Correction Factor
Silicon	100	113	1.13
Silicon Carbide	100	150	1.5

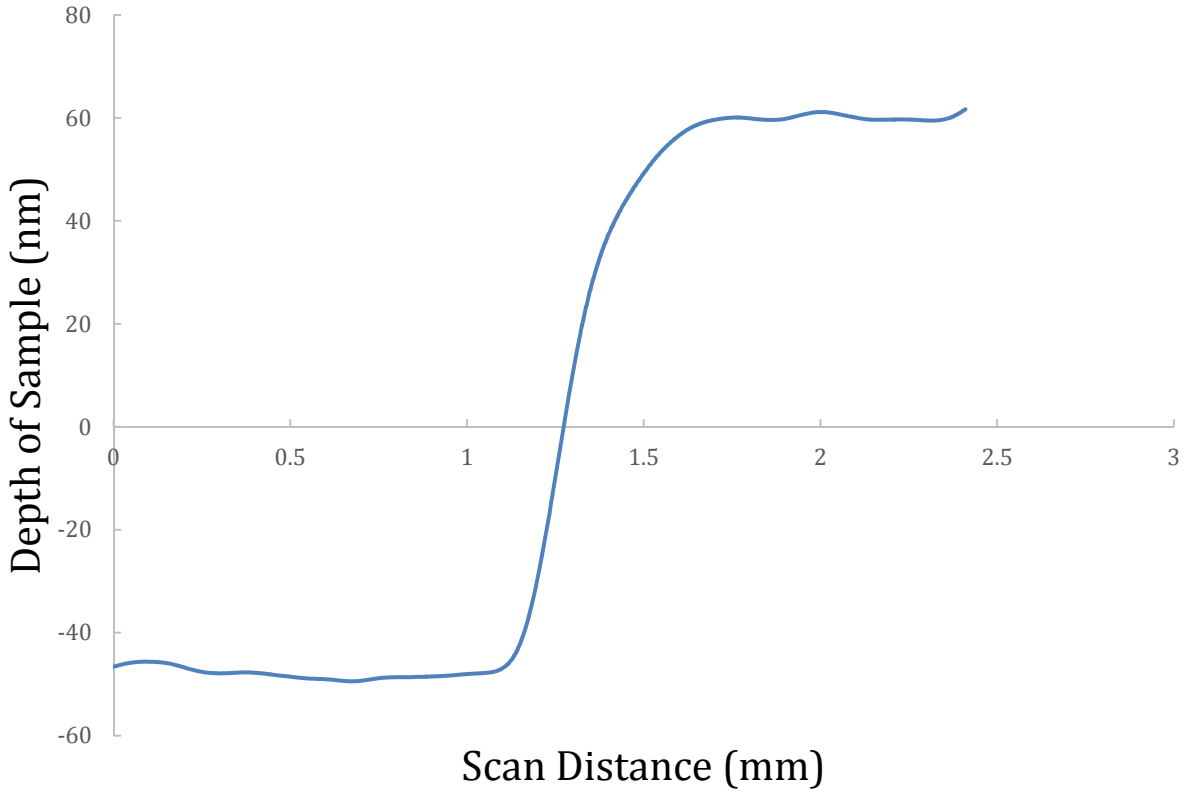

Figure 2.6: Data from a typical SWLI data slice done on a SiC film showing the step height. The flat area of the curve on the left is the reference part of the substrate, and the height is measured relative to the substrate surface. A step height of about 100 nm is observed.

2.6 Other Material Properties

Several other material properties are presented along with α, ρ, and μ in the next chapter for the SL films deposited on silicon, mullite, and quartz substrates. Stress is calculated by measuring the deflection of the substrate with the SWLI before and after film deposition. Density is calculated by measuring the mass and thickness before and after

deposition. Band gap is calculated using photo spectrometer measurements of the transparency as a function of the photon wavelength. And finally, the composition and bonding state of silicon carbide is examined using X-ray photoelectron spectroscopy (XPS).

References

[1] Angrist, Stanley W. "Direct energy conversion." Allyn and Bacon (Boston), (1965).

[2] Resel, R., E. Gratz, A. T. Burkov, T. Nakama, M. Higa, and K. Yagasaki. "Thermopower measurements in magnetic fields up to 17 teSLa using the toggled heating method." *Review of scientific instruments* 67, no. 5 (1996): 1970-1975.

[3] Rowe, David Michael, ed. *Thermoelectrics handbook: macro to nano*. CRC press, 2005.

[4] Schroder, Dieter K. *Semiconductor material and device characterization*. John Wiley & Sons, 2006.

[5] Aubain, Max S., and Prabhakar R. Bandaru. "Determination of diminished thermal conductivity in silicon thin films using scanning thermoreflectance thermometry." *Applied Physics Letters* 97, no. 25 (2010): 253102.

[6] Völklein, F. "Thermal conductivity and diffusivity of a thin film SiO_2-Si_3N_4 sandwich system." *Thin Solid Films* 188, no. 1 (1990): 27-33.

[7] Mazumder, Monalisa, Theodorian Borca-Tasciuc, Sean C. Teehan, Emilio Stinzianni, Harry Efstathiadis, and SLowa Solovyov. "Temperature dependent thermal conductivity of Si/SiC amorphous multilayer films." *Applied Physics Letters* 96, no. 9 (2010): 093103.

[8] Mason, Sarah. "University of Denver thermal conductivity meausrements." Personal interview. 19 Sept. 2014

[9] Borca-Tasciuc, T., A. R. Kumar, and G. Chen. "Data reduction in 3ω method for thin-film thermal conductivity determination." *Review of Scientific Instruments* 72, no. 4 (2001): 2139-2147.

[10] Malen, Jonathan A., Kanhayalal Baheti, Tao Tong, Yang Zhao, Janice A. Hudgings, and Arun Majumdar. "Optical measurement of thermal conductivity using fiber aligned frequency domain thermoreflectance." *Journal of Heat Transfer* 133, no. 8 (2011): 081601.

[11] Ohring, Milton. *Materials science of thin films*. Academic press, 2001.

3 Results and Discussion

This chapter focuses on presenting measurements of the thermoelectric properties of the Si/SiC superlattices. We also present the structure and morphology of a SL using SEM and TEM. The effect of substrate material with a SL layer thickness of 10 nm was found to be substantial, and, in particular, the silicon substrate electrical properties, which changed during processing and testing, prevented us from determining SL properties. Finally, the effect of quantum confinement size is presented for layer thicknesses of 2, 5, and 10 nm for SLs deposited on mullite.

3.1 Investigation of Si and SiC Film Properties

Two micrometer thick films of silicon and silicon carbide were sputter deposited on silicon, quartz, and mullite substrates to characterize the materials used to form superlattices. Good adherence to the substrate is integral for thin films. Our first attempt to determine the properties of the materials used to make our SLs showed that the silicon carbide films did not stick on the silicon or quartz substrates when the substrates were not heated, however, the films adhered nicely to the substrates when they were held at 500°C. Although several hundred SLs were produced in this research over a very wide range of conditions, all SLs discussed in this thesis and in this chapter in particular were deposited at a substrate temperature of 500°C. Table 3.1 shows properties of the sputter deposited films of silicon and silicon carbide at room temperature. The silicon film was found to be under mild compressive stress, the density is very close to that of bulk silicon, and the band gap measurements suggest that it is poly- or micro-crystalline. The silicon carbide film was under higher compressive stress that could result in some cracking of the film when

thermally cycled. The density is lower than bulk silicon carbide, and the band gap measurements suggest that the material is highly doped [1, 2, and 3]. The room temperature mobility was measured as well and found to be near nominal bulk Si values for the silicon film and much lower than nominal for the silicon carbide film. The carrier densities are both quite low at room temperature, but the silicon carbide film carrier concentration is about one thousand times higher than the silicon film. The higher carrier concentration, higher stress, and lower mobility of the silicon carbide film suggest a relatively higher defect concentration in the SiC film compared to the Si film.

Table 3.1: Properties of individual superlattice materials found with SWLI and a photo spectrometer by measuring before and after film deposition.

	Stress (GPa)	Density (g/cm^3)	Band Gap (eV)	Mobility ($cm^2/V\ s$)	Carrier Density (cm^{-3})
Silicon film	0.4 (C)	2.3	1.25	1369	5.4×10^{11}
Silicon Carbide film	2.0 (C)	3.0	1.63	170	1.6×10^{14}

XPS measurements of the silicon carbide film verified silicon carbide is sputtered deposited in the SiC chemical state onto the silicon substrate. Specifically, the carbon 1s at 284 eV indicates bonding to silicon, and the silicon 2p at 101 eV indicates bonding to carbon. XPS measurements were done after sputter cleaning the top surface oxides. X-ray Diffraction (XRD) was done and found to be inconclusive, and further XRD analysis should be done.

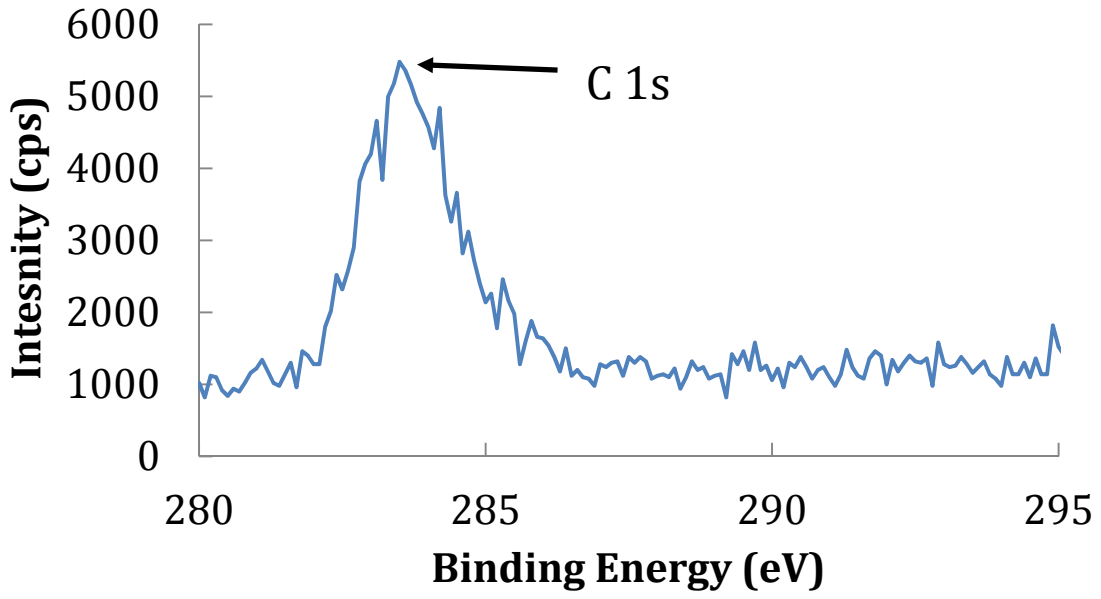

Figure 3.1: XPS data of Carbon 1s. The peak location at 284 eV indicates bonding with silicon.

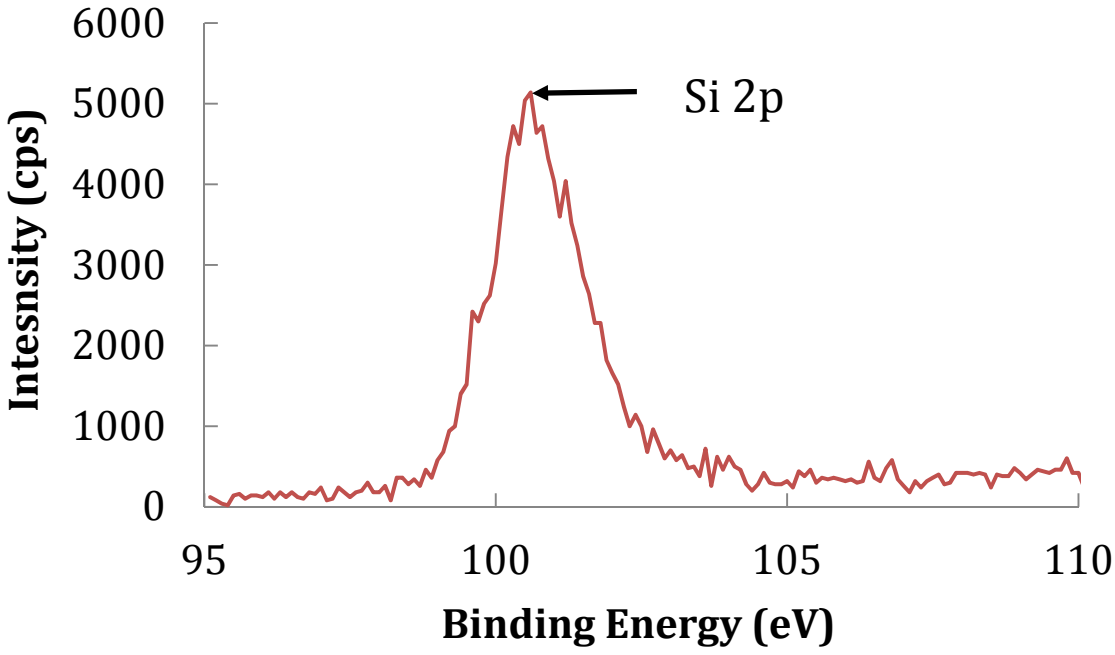

Figure 3.2: XPS data of silicon 2p. The peak location at 101 eV indicates bonding with carbon.

To obtain thermoelectric properties as a function of temperature, 500 nm films of silicon and silicon carbide were deposited on two separate mullite substrates. These samples were tested for thermoelectric properties to compare with properties of superlattices deposited on mullite. The resistivity as a function of temperature is shown in Figure 3.3, and the Seebeck coefficient is shown in Figure 3.5. The Seebeck coefficient is low and is in the opposite polarization than the superlattices indicating p-type behavior. The resistivity plot shows that the silicon is more conductive by ~3 orders of magnitude, and that the silicon carbide resistivity data contain some noise likely due to the large resistances of the SiC film, which was close to the limit of the resistance meter that was used. The films from the two materials, individually, do not have thermoelectric properties that would result in good thermoelectric devices.

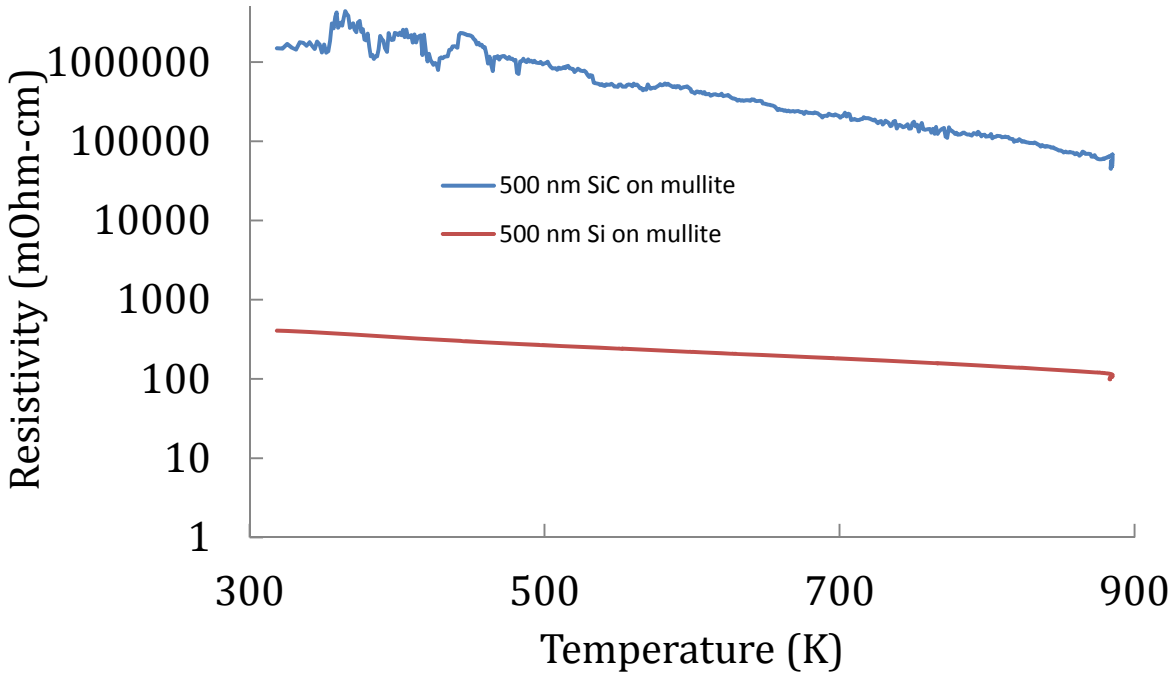

Figure 3.3: Resistivity as a function of temperature of individual films of Si and SiC on separate mullite substrates.

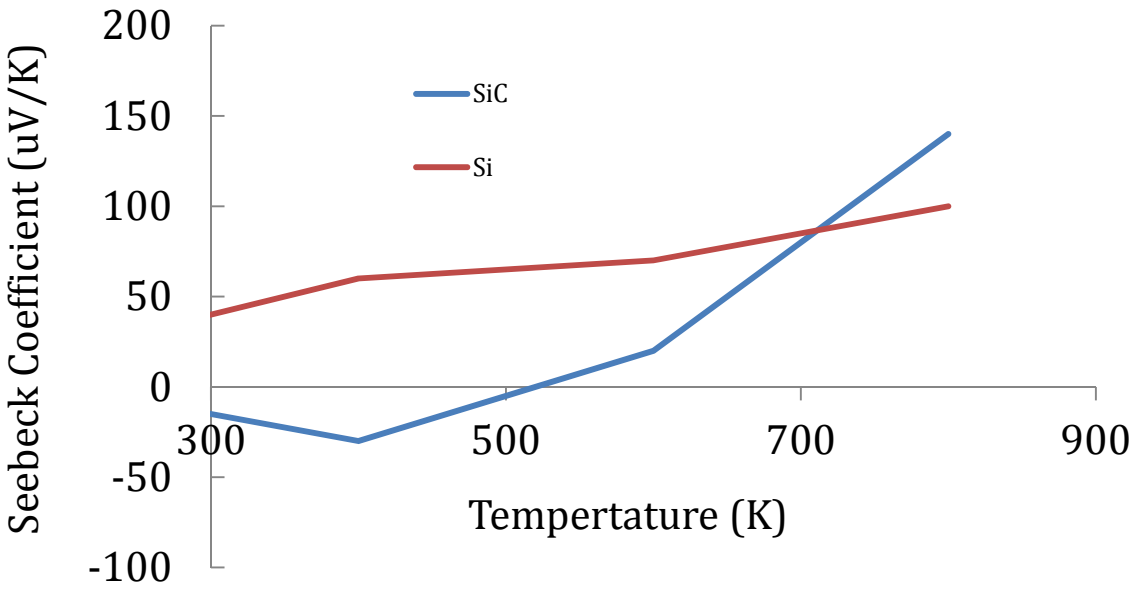

Figure 3.4: Seebeck coefficient as a function of temperature of individual materials on mullite substrate.

3.2 Investigation of Si/SiC Superlattices with SEM and TEM

The SL structure was investigated using Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) of a cross section of a SL film deposited on silicon for the SEM and quartz for the TEM. In both cases, the films were deposited at 500°C and tested in the thermoelectric property measurement system from 50°C to 630°C. The SEM image of the superlattice structure on a silicon substrate shown in Figure 3.5 verifies the SL structure and the layer thickness and uniformity, but it is hard to tell how much intermixing there is at the interfaces between the layers.

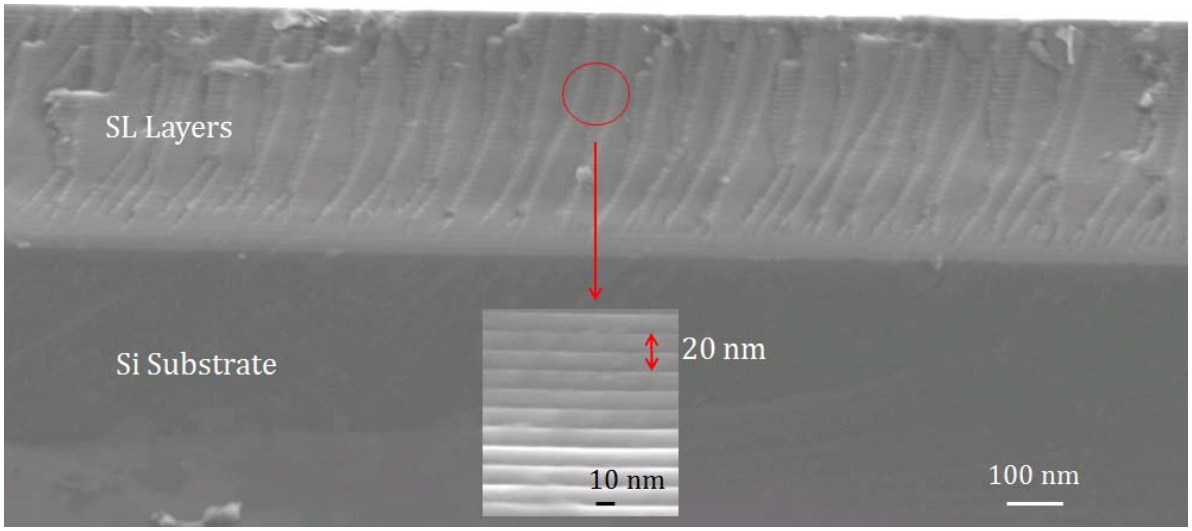

Figure 3.5: SEM image of cross section of a 10 nm layer superlattice film on silicon.

To investigate intermixing and morphology, TEM images are taken of a SL that was ion milled out of a sample by a focused ion beam (FIB) at Colorado School of Mines. The substrate for this sample was quartz. The TEM images in Figure 3.6 also verify the SL structure, but, like the SEM image in Figure 3.5, they also do not yield much information about intermixing at the interfaces due to poor contrast at the interfaces. The morphology of the SL films is mostly amorphous, but there are some regions of micro-crystallinity in both layers as evident in high magnification image in Figure 3.5. An even closer look at the SL structure in the high magnification TEM image in Figure 3.7 confirms that there is some micro-crystallinity in both the layers of the SL film. This could help improve electrical conductivity and provides evidence that micro-crystallinity is likely responsible for the relatively low band gap measurements of the individual films on the quartz substrates that was discussed in Section 3.1. The materials mapping data from the TEM measurements were inconclusive likely due to the FIB mixing the materials. There is more crystallinity in one of the layers, and that is likely the silicon layer.

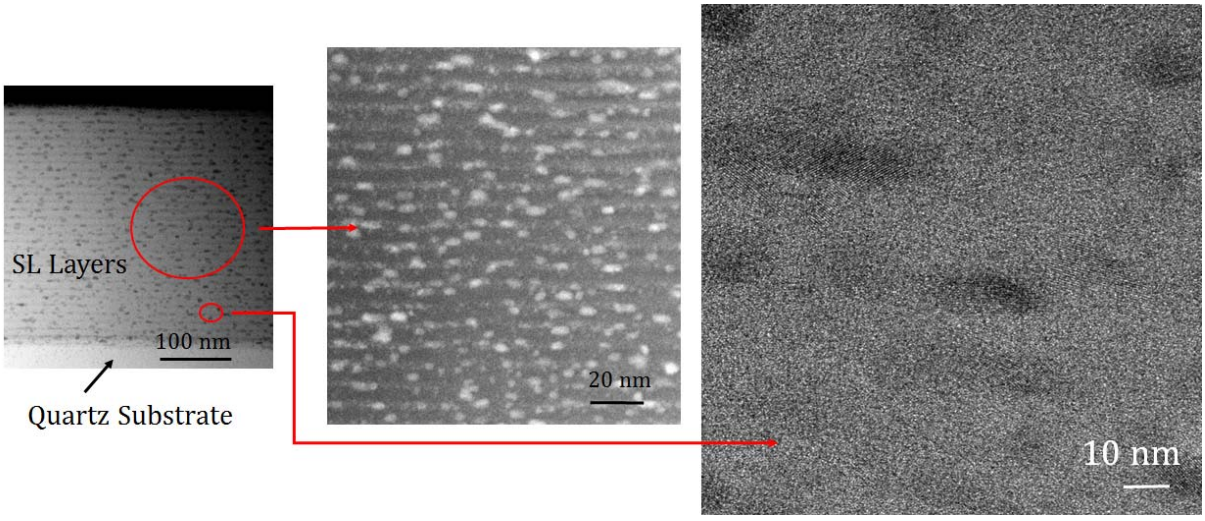

Figure 3.6: TEM images of cross section showing layers and morphology. The far left image shows the substrate and layers. The middle image is a close up of the layers. The far right image is a close up of grains of silicon and silicon carbide in dark field mode showing a mostly amorphous layer with some grains.

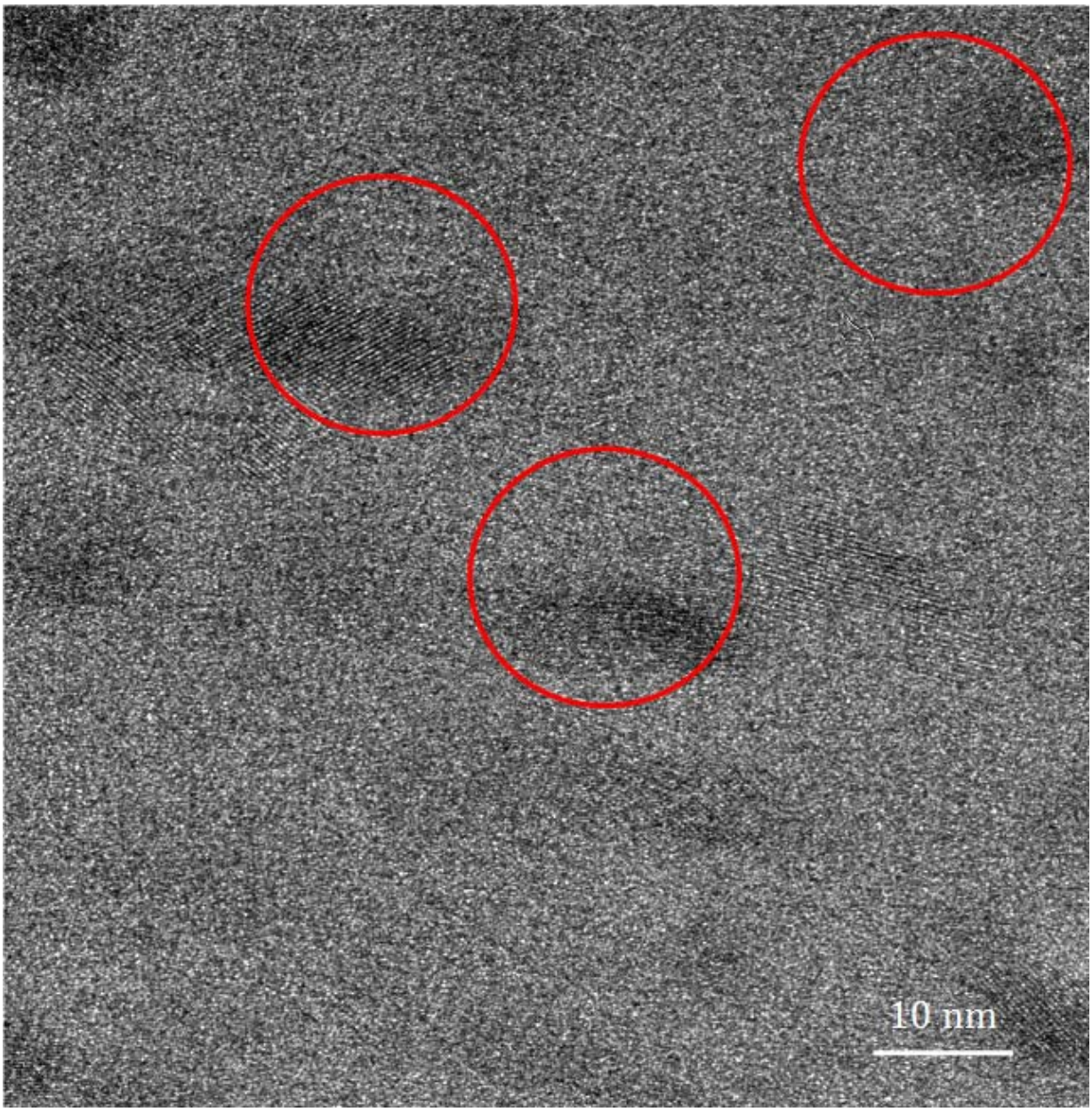

Figure 3.7: TEM dark field emission image of the grains of the silicon and silicon carbide layers showing some micro-crystallinity within the red circles.

3.3 Investigation of SLs on Different Substrates

To test the SL performance on different substrates, SLs of 31 bi-layers of 10 nm layers each were deposited on silicon, quartz, and mullite and tested. The best substrate was then selected to study thinner layer thicknesses of 5 nm and 2 nm. It should be noted that more than 400 SL samples were fabricated during this thesis to find the best film

fabrication technique, and that only the most important studies are shown in this thesis. The first substrate was a silicon wafer that is diced out of silicon #C977 from El-Cat Inc. The second is the same silicon wafer with an insulating film (500 nm) of mullite ($3Al_2O_32SiO_2$) sputter deposited on top. The third substrate is fused quartz which provides a smooth insulating surface for thin films. The last substrate used is sintered, bulk mullite, which is very rough. Mullite has a thermal expansion coefficient very close to that of silicon and also has very low thermal conductivity, so it is a great substrate candidate for superlattices intended for TE applications. Table 3.2 shows AFM data of the roughness of the SL samples grown on the three main substrate candidates. The mullite is by far the roughest, and the silicon and quartz are two orders of magnitude less rough.

Table 3.2: Roughness measurements of SL samples on different substrates.

Substrate	Roughness (RMS)
Silicon	4.86 nm
Mullite	365 nm
Quartz	2.16 nm

The resistance as a function of temperature of the silicon substrate, SL on silicon, and SL on deposited mullite on silicon is shown in Figure 3.8. The samples deposited on silicon have nearly the same resistance as the substrate, which means the substrate can strongly affect the measurement especially if its resistance changes during processing or during testing at high temperatures. Specifically, the data in Figure 3.8 suggest that conduction is primarily through the silicon substrate, and that the resistance of the

substrate needs to be subtracted out in order to obtain an accurate resistance measurement of the SL. This is difficult to do, and, hence measurements of SL properties of the SLs deposited on silicon substrates are not trustworthy and are not reported. It is interesting to note that the bare silicon substrate has a lower resistance than the silicon substrate with the SL. This is unexpected because the presence of the SL should reduce the resistance of a sample compared to the bare silicon substrate. It is possible that this occurs due to differences in substrates that are cut from different regions of the Si wafer.

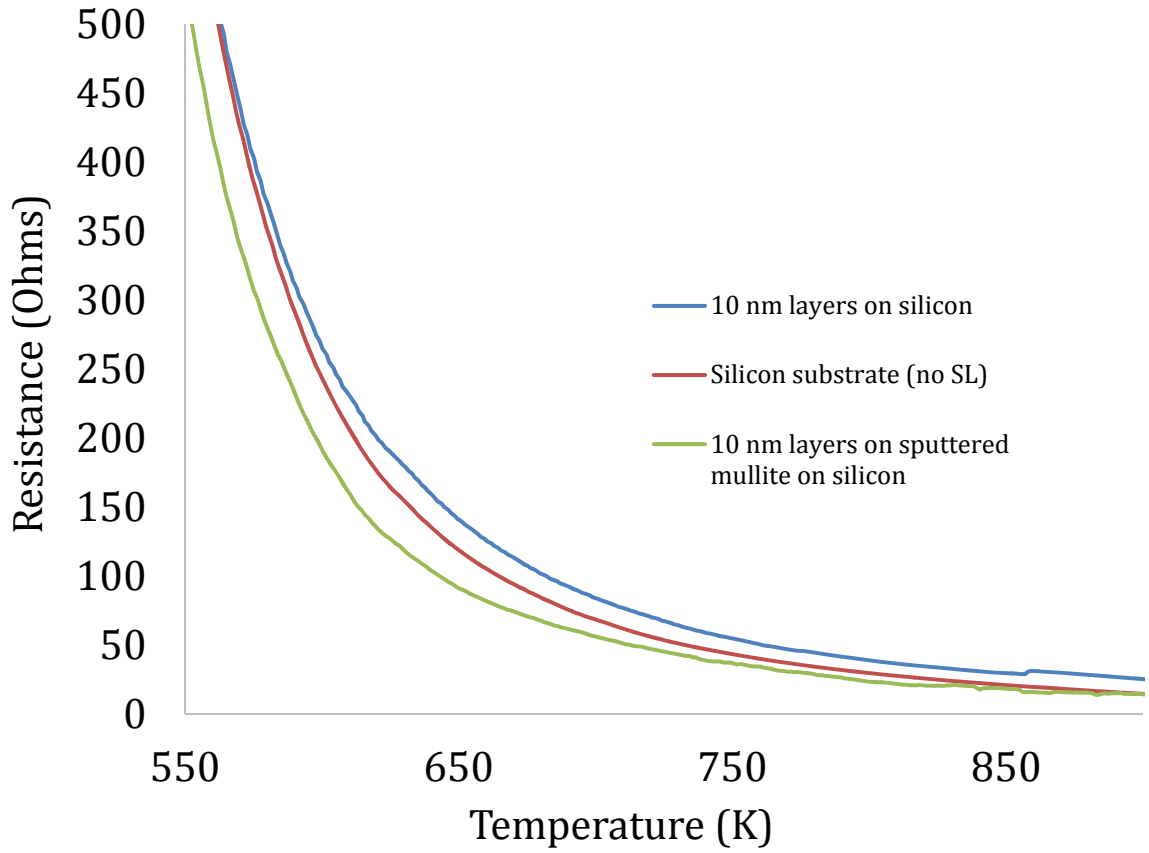

Figure 3.8: Resistance of samples deposited on silicon substrate as a function of temperature.

The Seebeck coefficient of the silicon substrate, SL on silicon substrate, and SL on deposited mullite on silicon substrate is shown in Figure 3.9. These data also show that the Seebeck coefficient of the SL samples are close to that of the pure silicon substrate

indicating that the silicon substrate is likely strongly to be affecting the measurement once again because most of the temperature difference and conducting is through the Si substrate and not the SL.

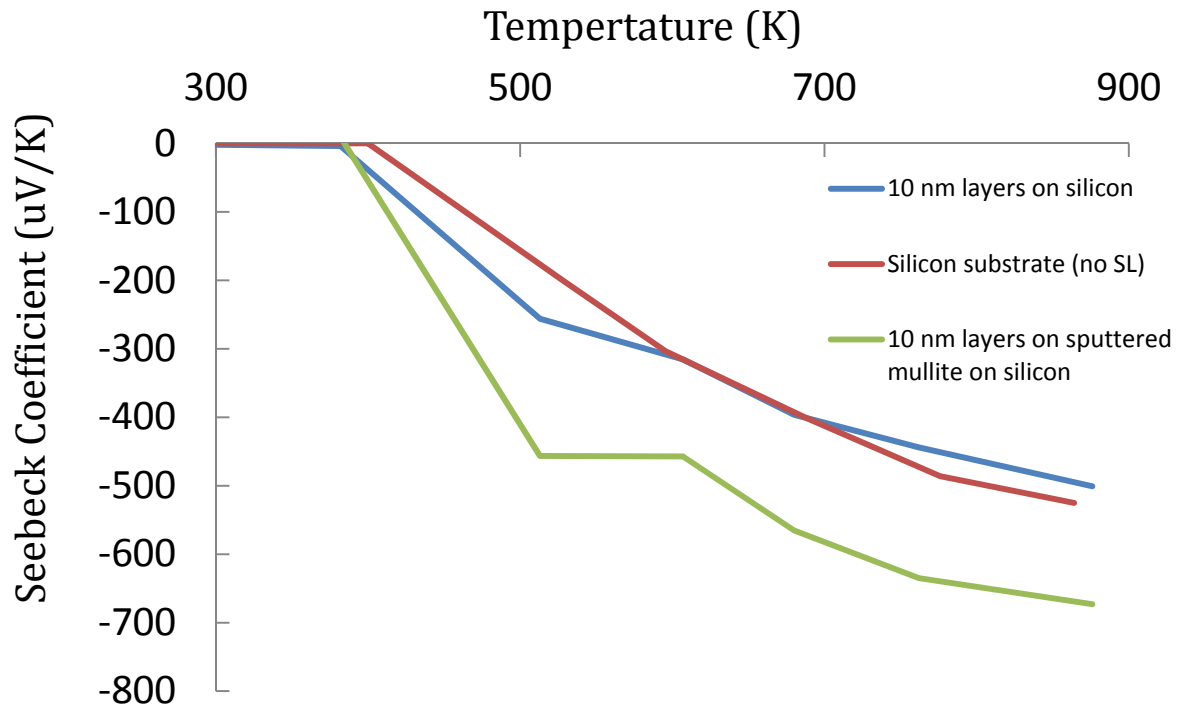

Figure 3.9: Seebeck coefficient of samples deposited on silicon substrate as a function of temperature.

Next, the resistivity of the SL on mullite, SL on quartz, and SL on sputtered mullite on quartz is shown in Figure 3.10. We switched to quartz from silicon for the sputter deposited mullite because the silicon substrate was preventing us from measuring SL properties even with the insulating mullite film coating the Si substrate. The SLs on quartz and mullite substrates have significantly higher resistivity compared to the SL on sputtered mullite on quartz. The 500 nm sputtered mullite film is likely not fully oxidized and is more conductive than we expected, so its resistivity was lower, and the Seebeck coefficient of the SL on sputtered mullite on quartz was similar to those of metals (see Figure 3.11). In

hindsight, the sputtered mullite film could have been fired in an air furnace to ensure full oxidation, but it is likely that the sample would not have differed much from the SLs on quartz and mullite substrates. The film has evidence of reduction of the silica or alumina materials because the film turns out purplish and greenish.

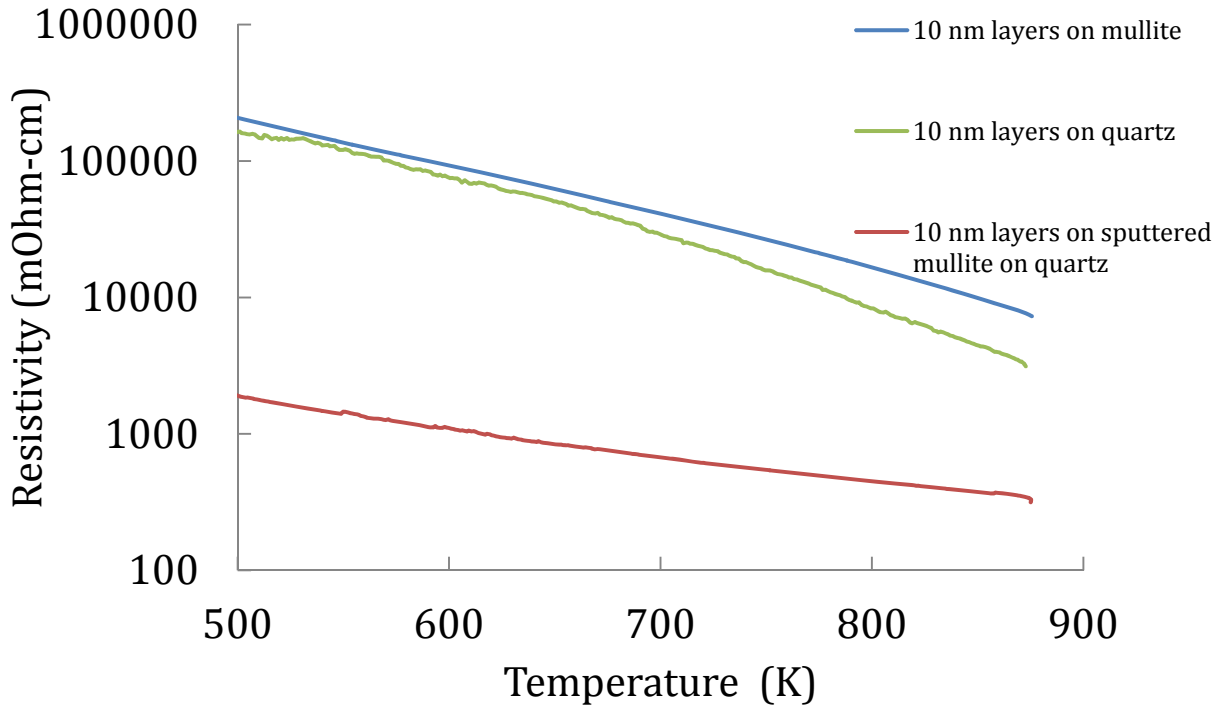

Figure 3.10: Resistivity of the four candidate substrates as a function of temperature.

The Seebeck coefficient of the SL on mullite, SL on quartz, and SL on sputtered mullite on quartz is shown in Figure 3.11. The quartz and mullite samples have very low Seebeck coefficient until reaching an average temperature of 800°C at 40 degree temperature difference. The samples have the highest Seebeck coefficient ever recorded in our lab, and, in some conditions, they produced an emf of over 100 mV. The quartz sample that has a sputtered mullite film on it did not behave the same way and had almost no emf generated during the tests. The giant Seebeck coefficient obtained on the quartz and mullite is repeatable as we have seen it multiple times with multiple samples. The giant

Seebeck does tend to degrade slightly after testing it multiple times. Table 3.3 shows that the degradation of the Seebeck coefficient is 5.8% and 6.5% on the SLs on quartz and mullite substrates respectively after 3 cycles. Also, the metal contacts tended to flake off of SL film of quartz after just one cycle, so this adversely affects the repeated resistivity measurements. The resistivity of the quartz and mullite SL samples improved at room temperature and at 870 K by about 5% and 7% respectively. The best thermoelectric properties are obtained with the quartz substrate, but the SL film cracked on the quartz due to the mismatch in thermal expansion coefficient. These two problems led us to use the mullite for the layer thickness studies because the SL film is robust and does not flake off mullite.

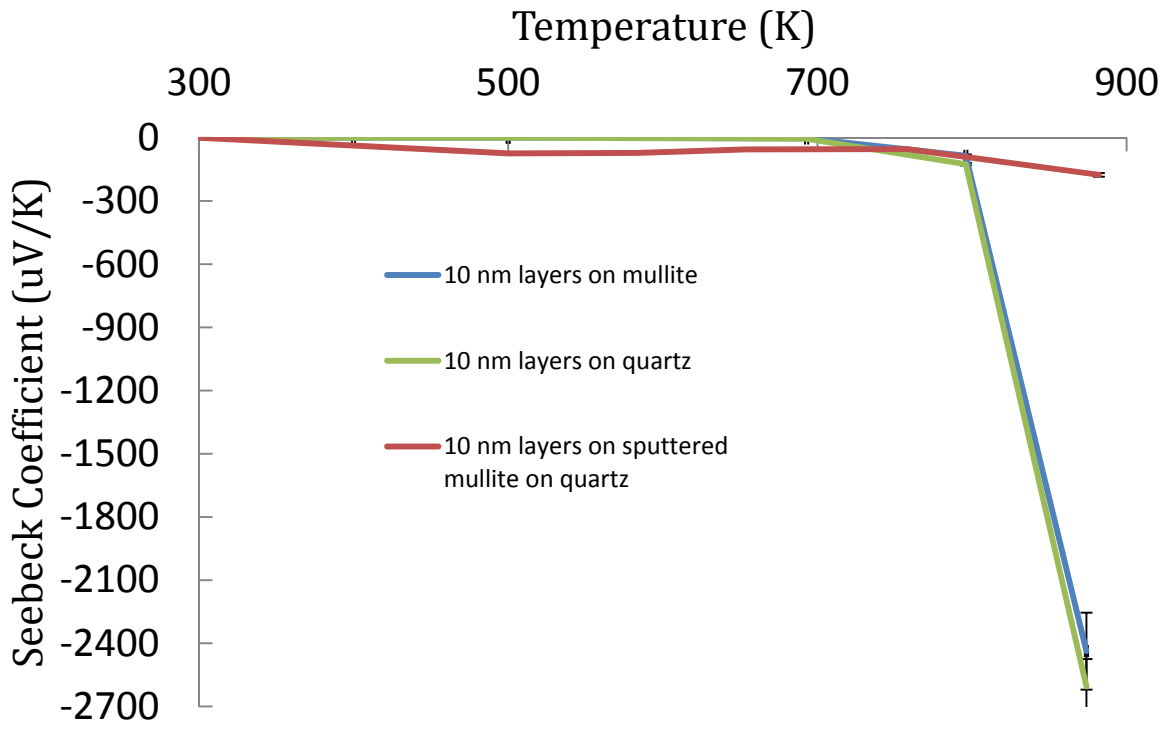

Figure 3.11: Seebeck coefficient of samples on different substrates.

Table 3.3: Degradation of Seebeck coefficient of SL on different substrates.

Number of tests	Seebeck coefficient of SL on quartz (μV/K)	Seebeck coefficient of SL on mullite (μV/K)
1	-2600	-2300
2	-2500	-2250
3	-2450	-2150

Finally, the mobility of the SLs is compared In Table 3.3 to delineate the carrier density and mobility of the SL as a whole. Surprisingly, the mobility is relatively high and close to the mobility of bulk silicon. It is also noted that the room temperature carrier concentration is relatively low. This result is very similar to the superlattices of GaN/AlN/AlGaN that have mobility of 1176 cm^2/Vs [4]. These results are surprisingly high for amorphous materials, so verification of these results should be done with another Hall mobility system. The mobility of amorphous silicon is in the 0.1-10 cm^2/Vs range [5, 6]. The then checked the mobility of the ML films using a four-point Ecopia HMS-3000 Hall measurement system to verify the results, and this system gave us a more accurate measurement. The mobility is very low and indicative of amorphous material composition.

Table 3.4: Mobility and carrier concentration of Si/SiC SL samples on mullite and quartz at room temperature using Ecopia HMS-3000.

	Mobility (cm^2/Vs)	Carrier Density (cm^{-3})
mullite	3.9×10^{-2}	-3.2×10^{17}
quartz	1.0×10^{0}	-3.3×10^{15}

3.4 Investigation of Superlattice Layer Thickness

Superlattices of 2 nm, 5nm, and 10 nm layers were deposited on mullite and compared. The correlation between the resistivity and layer thickness is shown in Figure 3.12, and the -2 and 5-nm layer SLs have lower resistivity compared to the 10-nm layer SL over the temperature range from 600K to 870 K.

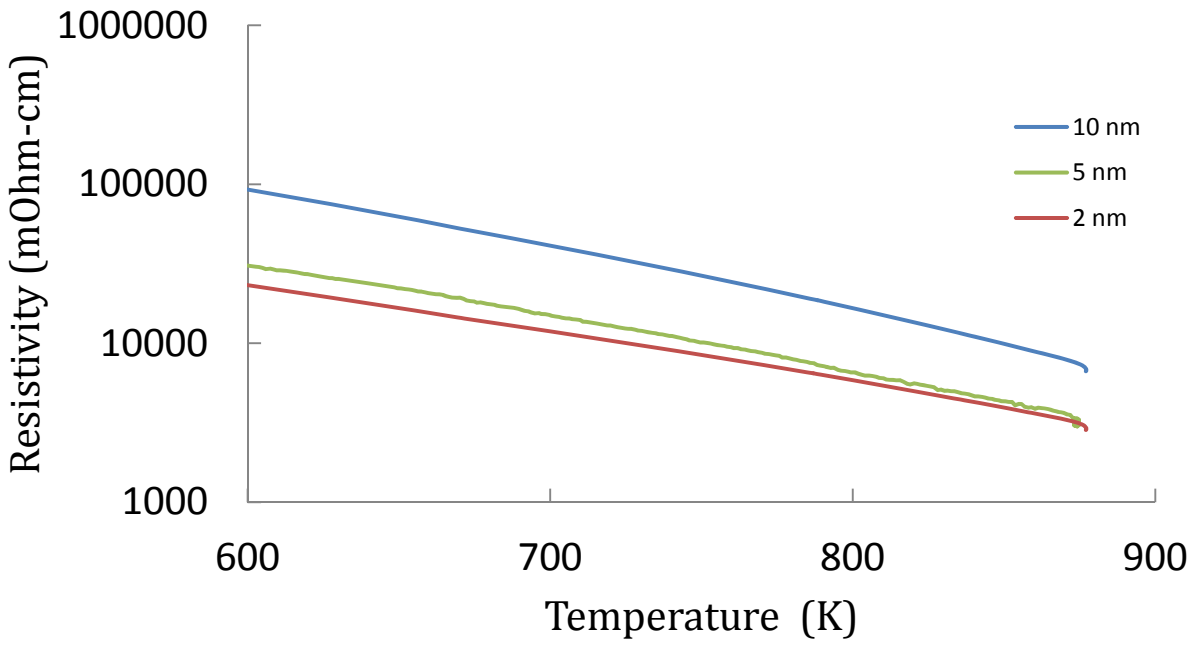

Figure 3.12: Resistivity as a function of temperature of samples of different layer thickness on mullite substrate.

The correlation between the Seebeck coefficient and the layer thickness is shown in Figure 3.13, and the 2- and 5-nm layer SLs have smaller Seebeck coefficient relative to the 10-nm layer SL at 870 K. At temperatures of 650 K and 750 K, the 5-nm layer SL displays the highest Seebeck coefficient followed by the 2 nm layer and then the 10 nm layer SLs.

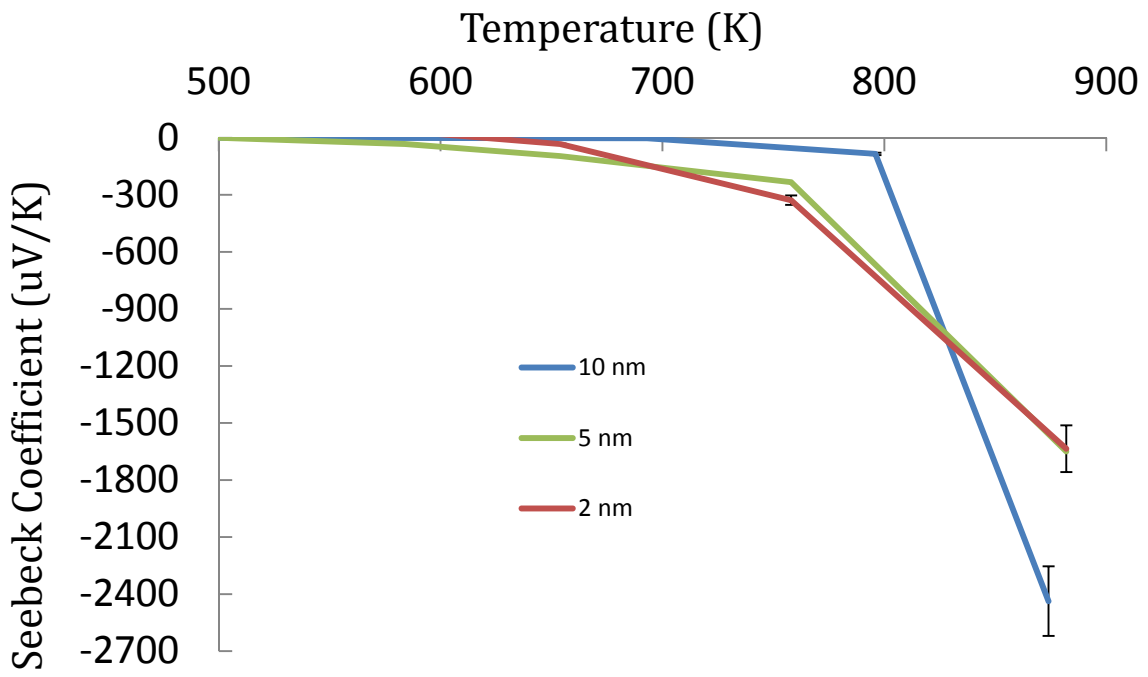

Figure 3.13: Seebeck coefficient as a function of temperature of samples of different layer thickness on mullite substrates.

3.5 Discussion

The morphology of the SLs shows that the SL structure is retained and that there is some micro-crystallinity meaning that the films could have been influenced by temperature and been annealed at growth or during testing at high temperatures. A limited number of TE property measurement tests were redone several times to determine the repeatability of the measurements. Relatively good repeatability was obtained on SLs on mullite substrates where the SLs and metal contacts did not crack excessively, and so annealing temperatures above ~800K would likely be necessary to determine if annealing could be used to affect TE properties.

Data from the company Hi-Z Technology Inc. on Si/SiC SLs on silicon substrate is summarized in Table 3.5. From their data and an inferred thermal conductivity of 2 W/mK, the figure of merit was calculated and listed in the fourth column. These values are very

large compared to the best materials developed to date by the materials science community.

Table 3.5: Data for Si/SiC superlattices as reported by Hi-Z Technology, Inc. Column four contains zT data calculated from the reported values of resistivity and Seebeck coefficient and assuming a thermal conductivity of 2 W/mK.

Temperature (°C)	Resistivity (mOhm-cm)	Seebeck Coefficient (μV/K)	Calculated zT
25	2.15	-750	3.9
250	1.71	-1080	17.8
500	1.52	-1240	39.1

It is not evident from the available literature that Hi-Z doped the Si/SiC layers on silicon substrates, and we believe the only difference from our SL process is that Hi-Z uses magnetron sputtering instead of ion beam sputtering. Their reported properties would yield zTs higher than 10 and close to 40 if an appropriate number for the thermal conductivity is used. It is likely that the Hi-Z samples were strongly affected by the bulk resistance of the silicon substrate as was found to be the case in this thesis. Using an inferred thermal conductivity of 2 W/mK, the zT at 900 K is calculated for our samples and is shown in Table 3.6. The best zT is the 10-nm layer SL on quartz. In our opinion, the resistivity measured by Hi-Z Technology, Inc. cannot be trusted due to the influence of the silicon substrate, and thus the calculated zT for the Hi-Z samples is severely over estimated. We believe the maximum zT that these materials can achieve with ion beam deposition and no doping is in the 0.05-0.1 range at a temperature of ~870 K. Higher zTs might be

possible at higher temperatures, but it is not practical to operate TEGs at such high temperatures.

The interesting phenomenon in our SLs is the turn on of the Seebeck effect at high temperature on SLs deposited on the quartz and mullite substrates. The turn on of the giant Seebeck is not well understood, but it is hypothesized that it is a strain-induced effect due to the mismatch of the interfaces. They likely line up and allow the emergence of phenomena at the interfaces when the samples are given enough thermal energy to reduce the strain in the films. Our apparatus could not be used to drive the temperature above ~900 K, and so no data are available above 900 K. We also note that our metal contacts began to degrade when tested to 900 K, and so both better contacts and a higher temperature measuring system are necessary to further study the emergent phenomena that have been observed.

Our superlattice structure likely has enhanced the effective mass and has high DOS near the Fermi level at temperature, which might lead to an enhanced Seebeck coefficient if an unknown mechanism is suppressing the minority carriers at elevated temperature. The SL majority carrier density is relatively low, which also can lead to high Seebeck coefficient. The SL materials produced in this study have inherently low electrical conductivity, and, because we had no systematic method of doping the silicon or silicon carbide, it isn't surprising that we observed the tradeoff in the thermoelectric properties that yielded a relatively low figure of merit.

One group that has been able to combat the tradeoff between carrier concentration and Seebeck coefficient is at Oak Ridge National Laboratory [7, 8, 9, and 10]. They use perovskite-structured titanates for their materials. Their hypothesis is that if a superlattice

structure were made of oxides that can be doped controllably without generating excessive defects at the interfaces, then the resistivity could be decreased without detrimentally decreasing the Seebeck coefficient. The group at Oak Ridge National Laboratory has demonstrated this by controllably doping perovskite superlattices. In addition, the band structure of oxide perovskites can be manipulated to have favorable thermoelectric properties. Our Si/SiC SLs are difficult to construct with low defect concentrations, and it is also difficult to dope the active SiC layer without adversely affecting the Si layer. A transition metal oxide (TMO) like the ones being studied at Oak Ridge National Laboratory is ideal for enhancing electronic phenomena because the s-shell electrons in the transition metal are transferred to the oxygen in the formation reaction, and the remaining d-shell electrons determine and enhance the TE properties of the TMO [7]. In TMO superlattices, the d-shell band is empty until it is lightly doped and overlapped, and then the interfaces can have very good conduction while the materials in the layers are band insulators. It has been shown that the mobility in oxide superlattices, namely perovskites and titanates, can be tuned [8], and that the mobility can be maintained at high levels even with very high carrier density that is appropriate for TE materials [9]. In our Si/SiC SLs, the mobility decreases as the carrier density increases. It is also difficult to tune the interface due to the relatively large lattice misfit between the SiC and Si. Finally, the amorphous morphology makes it difficult to tune the bands to draw out the desired quantum confinement effect. Using careful oxide superlattice doping techniques that are possible in pulsed laser deposition (PLD), the Seebeck coefficient has been greatly enhanced resulting in a three-fold increase in thermal power ($\alpha^2\sigma$) without compromising the mobility [10].

Table 3.6: Material zTs for 10 nm layers of Si/SiC on different substrates.

Substrate	zT (at 870 K)
mullite	0.07
quartz	0.08
sputtered mullite on quartz	0.003
sputtered mullite on silicon	0.05

The figure of merit was calculated for the SLs of different layer thickness on mullite. The different layer thicknesses show that the best thermoelectric leg is the 2-nm layer SL. This is because the resistivity is better and the Seebeck coefficient has not decreased too much relative to the 5- and 10-nm layer samples. There is a large jump of the Seebeck coefficient in all the samples on mullite at high temperature just like the 10-nm layer SL on quartz. This means that the giant Seebeck effect that was observed isn't related to the substrate that the SLs are grown on.

Table 3.7: Material zTs for samples of different layer thickness on mullite.

Sample	zT (at 900 K)
2 nm	0.07
5 nm	0.07
10 nm	0.06

The large Seebeck coefficients at high temperature suggest the giant Seebeck coefficient effect has been observed in the Si/SiC SL system. This is the highest Seebeck coefficient to date for our Si/SiC SL system. The giant Seebeck coefficient is a term

reserved for systems that enhance the Seebeck coefficient beyond bulk values with quantum confinement. Most of these giant Seebeck coefficient systems utilize oxides and precise doping. Ohta et al [11] and Lee et al [12] have both shown the giant Seebeck coefficient in $SrTiO_3$ systems, and Song et al [13] have shown the giant Seebeck coefficient for MnO_2. These studies provide additional evidence that Hicks and Dresselhaus's [14] theoretical work is correct. Fully decoupling the carrier concentration and Seebeck coefficient may never be acheived, but we and other researchers have proved that the giant Seebeck coefficient exists. Systems designed for high Seebeck coefficient like superlattices have the potential for performing carrier concentration tuning, thus, shifting the zT versus carrier density plot to the left and upward for a higher, more efficient material with relatively lower carrier concentration, which is the reverse of the current approach that is being followed by the materials science community in skutterudites, clathrates, and chalcanogides [15].

References

[1] Kakinuma, H., M. Mohri, D. M. Sakamoto, and T. Tsuruoka. "Structural properties of polycrystalline silicon films prepared at low temperature by plasma chemical vapor deposition." *Journal of applied physics* 70, no. 12 (1991): 7374-7381.

[2] Baccarani, G., B. Ricco, and G. Spadini. "Transport properties of polycrystalline silicon films." *Journal of applied physics* 49, no. 11 (1978): 5565-5570.

[3] Seto, John Y.W. "The electrical properties of polycrystalline silicon films."*Journal of Applied Physics* 46, no. 12 (1975): 5247-5254.

[4] Sztein, Alexander, John E. Bowers, Steven P. DenBaars, and Shuji Nakamura. "Polarization field engineering of GaN/AlN/AlGaN superlattices for enhanced thermoelectric properties." *Applied Physics Letters* 104, no. 4 (2014): 042106.

[5] Carlson, David E., and Cristopher R. Wronski. "Amorphous silicon solar cell."*Applied Physics Letters* 28, no. 11 (1976): 671-673.

[6] Le Comber, P. G., and W. E. Spear. "Electronic transport in amorphous silicon films." *Physical Review Letters* 25, no. 8 (1970): 509.

[7] Hwang, H. Y., Y. Iwasa, M. Kawasaki, B. Keimer, N. Nagaosa, and Y. Tokura. "Emergent phenomena at oxide interfaces." *Nature materials* 11, no. 2 (2012): 103-113.

[8] Choi, Woo Seok, Suyoun Lee, Valentino R. Cooper, and Ho Nyung Lee. "Fractionally δ-doped oxide superlattices for higher carrier mobilities." *Nano letters* 12, no. 9 (2012): 4590-4594.

[9] Cooper, Valentino R., Sung Seok A. Seo, Suyoun Lee, Jun Sung Kim, Woo Seok Choi, Satoshi Okamoto, and Ho Nyung Lee. "Transparent conducting oxides: A-doped superlattice approach." *Nature Materials* 4 (2014).

[10] Choi, Woo Seok, Hiromichi Ohta, and Ho Nyung Lee. "Thermopower enhancement by fractional layer control in 2D oxide superlattices." *Advanced Materials* (2014): 1521-4095.

[11] Ohta, Hiromichi, SungWng Kim, Yoriko Mune, Teruyasu Mizoguchi, Kenji Nomura, Shingo Ohta, Takashi Nomura et al. "Giant thermoelectric Seebeck coefficient of a two-dimensional electron gas in $SrTiO_3$." *Nature Materials* 6, no. 2 (2007): 129-134.

[12] Lee, Kyu Hyoung, Yoriko Mune, Hiromichi Ohta, and Kunihito Koumoto. "Thermal stability of giant thermoelectric Seebeck coefficient for $SrTiO_3/SrTi_{0.8}Nb_{0.2}O_3$ superlattices at 900 K." *Applied Physics Express* 1, no. 1 (2008): 015007.

[13] Song, FangFang, Liming Wu, and S. Liang. "Giant Seebeck coefficient thermoelectric device of MnO_2 powder." *Nanotechnology* 23, no. 8 (2012): 085401.

[14] Hicks, L. D., and M. S. Dresselhaus. "Effect of quantum-well structures on the thermoelectric figure of merit." *Physical Review B* 47, no. 19 (1993): 12727.

[15] Dresselhaus, Mildred S., Gang Chen, Ming Y. Tang, R. G. Yang, Hohyun Lee, D. Z. Wang, Z. F. Ren, J-P. Fleurial, and Pawan Gogna. "New Directions for Low-Dimensional Thermoelectric Materials." *Advanced Materials* 19, no. 8 (2007): 1043-1053.

4 Conclusion and Future Work

4.1 Conclusion

An ion-beam-based deposition system was configured to grow Si/SiC superlattices on silicon, mullite, and quartz substrates. Typical SL films consisted of 31 bi-layers of 10-nm layer thickness. The SLs where found to be highly amorphous with some limited regions of microcrystallinity. The Seebeck coefficient was negative for the SLs as expected, and giant Seebeck coefficient behavior was observed at a temperature of 870 K. An impressive Seebeck coefficient of ~2600 □V/K was measured at this temperature along with a higher, less than desired, resistivity of 3.4 □-cm. A zT of 0.08 was calculated when these values are combined with an assumed thermal conductivity of 2 W/mK. Although this is too low for use in a thermoelectric generator, we believe that nano-structures like superlattices are still very promising. This belief is based on the very large improvement in zT that is observable with SLs of Si/SiC over zTs corresponding to bulk Si or SiC or films of Si or SiC.

Every precaution was made to ensure quality SL films were grown and tested including minimizing the oxygen in the vacuum chamber during the sputter deposition process, slowing the growth rate at the interfaces, and carefully transporting the SL films between vacuum testing facilities. Regardless of the care, we were unable to reproduce the very high zT values obtained by others with Si/SiC superlattices on Si substrates. Our films on silicon superlattices also showed promising zT properties, but, upon careful follow on testing, we determined that the silicon substrates were strongly affecting the results and that changes in the silicon substrates during SL deposition and subsequent testing at high

temperature was causing the SL film resistivity to be severely underestimated. Consequently, our investigation of Si/SiC superlattices sputter deposited on silicon substrates showed that silicon is not a good substrate candidate for these materials due to difficulty in measuring the SL properties. Although mullite and quartz substrates allowed the SL properties to be measured, the resistivity was too high and the zT was less than 0.1, which is too low to be useful in TE devices, as mentioned above. The best SLs were the ones deposited on mullite using 10-nm layer thickness because it is robust and comes within 95% of the properties observed on the quartz substrate sample. Although the SL on quartz displayed better TE properties, it cracked after one thermal cycle and flaked off.

We have measured the highest Seebeck coefficient to date with Si/SiC superlattices on insulating substrates with values greater than 2000 μV/K. We show evidence that there is a Seebeck enhancement effect due to quantum confinement. With superlattices made of semiconductor materials, the electrical conductivity is poor compared to traditional bulk TE materials that are in the semi-metal materials class. It is believed that the density of states effective mass was increased in our SLs on mullite and quartz, which resulted in an increase of the Seebeck coefficient at higher temperatures. The turn on of the giant Seebeck coefficient at high temperature is not well understood, but it is thought to be due to a strain-related effect.

4.2 Directions for Future Work

The resistivity of our SLs is low especially at low temperatures below 600 K, and this is bad for the figure of merit of the materials. To improve the resistivity, the SL layers could be doped, but finding a way to do this is challenging because the dopants for Si are not always compatible with SiC, and sputtering a doped wafer does not guarantee the same

substitution of the dopant in the film. It is recommended that a doping material or materials be found and that systematic tests be done to study the affect doping has on TE properties of SLs on mullite substrates.

A limited number of cycles to high temperature were performed on the films in this work. In addition, no annealing was performed on the samples. Although TEM studies showed that some crystallization exits, most of the SL was in the amorphous state. Hence it is suggested that the SLs should be cycled or annealed several times to see if the SLs become more crystalline or if the interfaces break down or mix. This is important because the annealing might help the resistivity, but it should be done in a manner that does not disrupt the interfaces or adversely affect the Seebeck coefficient or thermal conductivity. The annealing and cycling might also lead to an understanding of the lifetime of these materials for real world devices. Finally, the annealing process might enhance the electrical conductivity if optimized, but one would need to take care to avoid generating compensating donor-acceptor pairs or converting the n-type material to p-type.

As mentioned above, there was limited crystallinity content in the Si and SiC layers. If the SiC can be grown around its crystallization temperature, then it might have better resistivity, and further TEM work would need to be done to show this. The SiC is 3 orders of magnitude larger in resistivity, so it making it more crystalline could help the overall SL resistivity. Consequently, if the annealing studies above result in improvement, then it is suggested that the deposition temperature be increased to study its effect on SL TE properties. If we reach more uniform crystallinity, the term superlattice will really be appropriate. Right now, we have almost no crystallinity, so the term superlattice is used because previous studies have used this term with Si/SiC thin-film multilayers. In addition,

we note that further mechanical polishing preparation for the TEM might prevent the mixing of the materials and show the individual layers materials more accurately, which might be necessary to show that layer intermixing doesn't occur at higher deposition temperatures.

Another improvement for Si/SiC SLs is to find a better metal contact to the SLs. This is important for testing the materials to higher temperature and for eventually making them into module legs if adequate performance is achieved. Molybdenum and titanium adhere well and seem to work directly after the contact deposition, but they sometimes flake off after testing the samples at high temperatures. Some studies with alloys can be done to ensure a good metal contact can be made to the Si/SiC SL films, and the contacts should withstand thermal cycles. The best contacts for Si/SiC might be tungsten, nickel, copper alloys that are known to have coefficients of thermal expansion that is close to silicon.

Other fabrication techniques should be investigated, and different materials could be used to form other superlattice systems. It is possible that the ion beam sputtering process is causing a problem with the growth leading to interfaces that are not sharp. Also, there could be too much strain in the Si/SiC SLs given the lattice mismatch. Most other superlattices are not fabricated with ion beam sputtering, and they usually use the same material for the layers but dope the active layer, so the mismatch is extremely small yielding limited strain in the SL structure. It is recommended that a general study be done to identify materials that could be made into SLs with low lattice mismatch values.

Elsner et al [1] showed that Si/SiGe superlattices had good resistivity and maintained a Seebeck coefficient near bulk values. Ohta et al [2] and Lee et al [3] have

shown enhanced properties in $SrTiO_3/SrTi_{0.8}Nb_{0.2}O_3$ superlattices but they did not measure the thermal conductivity. The thermal conductivity measurement is important because one would like to know the actual zT and not an estimate of it. Choi et al [4] had some success with out-of-plane superlattices of $La_xSr_{1-x}TiO_3/SrTiO_3$; however, they also did not measure the thermal conductivity. Recent data from SLs of GaN/AlN/AlGaN show an increase in mobility and good resistivity [5]. These are all motivation for working with SL systems and finding the best fabrication technique, materials configuration, and materials choice to fabricate a thermoelectric material that could have zTs near the 10 range and higher.

The titanate superlattice thermoelectric materials at Oak Ridge National Laboratory [4], if still enhanced in the in-plane direction, should have thermoelectric properties better than any known material, and further research of these materials is recommended. They have not tested the thermal conductivity, which would most likely be higher than 2 W/mK due to the much higher carrier density. They also did not test these superlattices to any substantial temperature above room temperature, and it looks like their Seebeck will be large at higher temperatures as it already is at -600 μV/K at room temperature. Consequently, it is strongly recommended that additional work be done with TMO superlattices and that their in-plane electrical and thermal properties be measured.

Studying the differences of fabrication of oxide thermoelectric materials with ion beam sputtering, spark plasma sintering, and magnetron sputtering is recommended because there might be a difference of the quality of films and the sharpness of the interfaces. Annealing of the superlattices could be done to test the ratios of materials and make sure they are the same as the superlattices done at Oak Ridge National Laboratory.

Then one could compare the thermoelectric properties to see if that is a viable option for fabricating perovskite oxide thermoelectric superlattices for high temperature devices.

References

[1] Elsner, N. B., S. Ghamaty, J. H. Norman, J. C. Farmer, R. J. Foreman, L. J. Summers, M. L. Olsen, P. E. Thompson, and K. Wang. "Thermoelectric performance of $Si_{0.8}Ge_{0.2}$/Si heterostructures synthesized by MBE and sputtering." In *The thirteenth international conference on thermoelectrics*, vol. 316, no. 1, pp. 328-333. AIP Publishing, 1994.

[2] Ohta, Hiromichi, SungWng Kim, Yoriko Mune, Teruyasu Mizoguchi, Kenji Nomura, Shingo Ohta, Takashi Nomura et al. "Giant thermoelectric Seebeck coefficient of a two-dimensional electron gas in $SrTiO_3$." *Nature Materials* 6, no. 2 (2007): 129-134.

[3] Lee, Kyu Hyoung, Yoriko Mune, Hiromichi Ohta, and Kunihito Koumoto. "Thermal stability of giant thermoelectric Seebeck coefficient for $SrTiO_3/SrTi_{0.8}Nb_{0.2}O_3$ superlattices at 900 K." *Applied physics express* 1, no. 1 (2008): 015007.

[4] Choi, Woo Seok, Suyoun Lee, Valentino R. Cooper, and Ho Nyung Lee. "Fractionally δ-doped oxide superlattices for higher carrier mobilities." *Nano letters* 12, no. 9 (2012): 4590-4594.

[5] Sztein, Alexander, John E. Bowers, Steven P. DenBaars, and Shuji Nakamura. "Polarization field engineering of GaN/AlN/AlGaN superlattices for enhanced thermoelectric properties." *Applied Physics Letters* 104, no. 4 (2014): 042106.