A Mixed-Signal Implementation of an ADC-Less Ping-Pong Temporal Front-End for Sensor-to-Photonic Processing

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Abstract

Edge sensing systems require front-end architectures that reduce data movement, latency, and energy before full downstream processing. This paper presents a mixed-signal implementation and system-level adaptation of an ADC-less ping-pong temporal sensor front-end for low-overhead frame-difference sensing. The underlying ping-pong PWM pixel principle is adopted from prior CMOS vision-sensor work; this paper does not claim the base ping-pong pixel concept itself as new. Instead, the contribution is the implementation, validation, and sensor-to-photonic interface adaptation of that temporal front-end. The adopted front-end uses odd/even phased analog state reuse and in-pixel temporal differencing to extract motion-relevant information before full-frame digitization. A PWM representation of temporal difference is digitized by a compact counter-based readout path, producing a DATA_VALID-qualified digital interface. Preliminary one-pixel mixed-signal results in a TSMC 0.18 µm environment demonstrate functionally correct operation, stable analog boundary waveforms, verified odd/even lane alternation, and repeatable interleaved 8-bit code capture. Simulation-extracted readout timing shows a 1.017 µs DATA_VALID window with zero odd/even overlap, while current architecture-level estimates indicate 70 µW to 75 µW total power and 700 fps to 1000 fps potential. The same front-end provides an electrical interface to a downstream near-sensor photonic processing stage, where temporally preprocessed outputs can be converted to optical activations rather than exporting raw image data.

CCS Concepts

• **Hardware → Sensor devices and platforms**; *Emerging optical and photonic technologies.*

Keywords

ADC-less image sensor, ping-pong pixel, frame difference, mixed-signal front-end, PWM readout, temporal sensing, optical interface, near-sensor photonic processing

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1 Introduction

Near-sensor photonic computing is increasingly attractive for edge visual intelligence because it promises low-latency, low-bandwidth inference directly at the sensor edge. Recent cross-layer photonic studies have shown that moving visual processing toward the sensor can substantially reduce cloud traffic and improve energy efficiency, yet they also make clear that the sensor-side interface remains a decisive part of the overall system cost [5, 6, 8, 9]. In conventional vision pipelines, raw pixel data are first converted and stored before any task-relevant filtering occurs, even when the primary objective is only temporal change detection.

This paper focuses on the front-end circuitry needed before a downstream photonic processor. We explicitly adopt the ping-pong PWM temporal pixel concept from prior work [3]; the base odd/even ping-pong pixel principle is not claimed as a new invention here. Our work instead implements and validates a compact mixed-signal readout/interface path around that concept and adapts it for frame-difference operation in a sensor-to-photonic processing flow. The implemented front-end stores and reuses analog temporal state across odd and even lanes, allowing consecutive temporal samples to be compared before a conventional full-frame ADC stage would normally be invoked. Instead of exporting raw full-frame image data, the front-end converts temporal change into a PWM-coded signal that is captured by a compact counter-based readout block.

The specific contributions of this paper are: (1) a TSMC 0.18 µm mixed-signal implementation and validation flow for an adopted ping-pong PWM temporal front-end; (2) a low-voltage counter-based readout path with DATA_VALID-qualified odd/even 8-bit capture; (3) source-synchronous timing characterization including DATA_VALID width, odd/even non-overlap, and one-clock capture latency; and (4) a photonic-interface-oriented adaptation in which temporal-difference outputs serve as compact electrical activations for later optical modulation. These contributions define the implementation and interface layer around the prior ping-pong pixel concept rather than re-claiming the pixel concept itself.

2 Background and Motivation

Recent work from the near-sensor photonic community provides the larger motivation for this front-end. A recent cross-layer summary of OISA, Lightator, and Neuro-Photonix shows that sensor-edge optical processing can reduce the cost of transmitting raw data to the cloud while enabling increasingly capable visual workloads [9]. At the same time, those studies emphasize that the overall

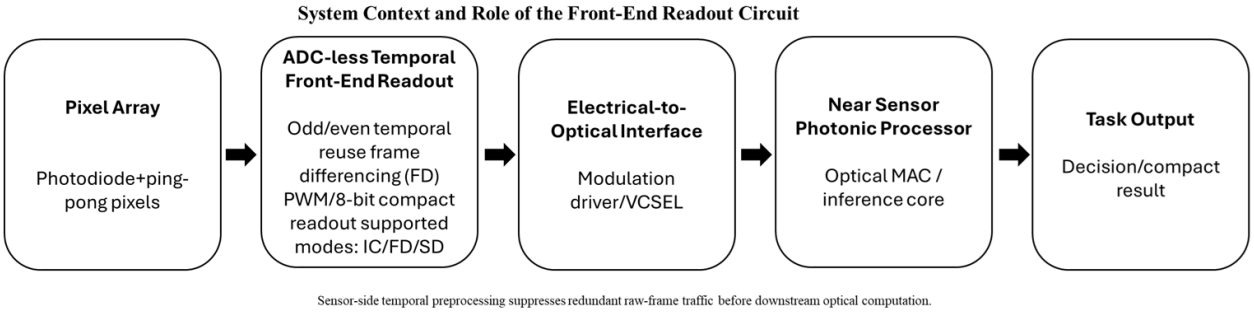

Figure 1: Paper-level system context. A sensor pixel array feeds an ADC-less temporal front-end and compact counter-based readout/interface stage before downstream electrical-to-optical modulation and near-sensor photonic processing. The highlighted block denotes the focus of this paper.

system still depends on the quality of the sensor-side electrical interface.

OISA introduced an optical in-sensor accelerator with ADC-free VCSEL-based activation modulation and a lightweight CMOS interface for first-layer processing [5, 9]. However, that front-end was tailored to low-bit first-layer activations rather than to a more general-purpose temporal readout circuit. Lightator later added a comparator-based reading circuit and a selector to raise activation precision and support multilayer processing [6, 9], which underscores that the readout/interface stage remains a key co-design problem rather than a solved detail.

Broader near-/in-sensor literature identifies the same bottlenecks repeatedly: power-hungry ADC/DAC chains, redundant data movement, storage overhead for intermediate features, and the need for compact front-end preprocessing before data reach downstream compute [1, 2, 4, 7, 8, 10–15]. The goal of the present work is therefore not to redesign the photonic processor itself, but to provide a compact temporal readout circuit that reduces the burden placed on that processor.

3 Relation to Prior Ping-Pong PWM Pixel Work

The ping-pong PWM pixel concept used in this work is based on the prior 0.8 V multimode CMOS vision sensor of Hsu *et al.* [3]. That work introduced the core odd/even temporal storage principle and demonstrated multimode CMOS image-sensor operation, including image capture, frame difference, and saliency-oriented operation. Therefore, the present paper should be read as an implementation and system-adaptation study, not as a re-proposal of the original ping-pong pixel architecture.

The distinction is important for both technical clarity and publication positioning. The novelty in the present work lies in how the adopted ping-pong temporal front-end is implemented, validated, and connected to a different system objective. First, we build a one-pixel mixed-signal validation environment around the adopted front-end, including low-voltage timing/control, PWM detection, PCLK-driven counting, and DATA_VALID-qualified 8-bit output capture. Second, we emphasize FD-mode readout behavior and the associated odd/even lane timing needed for a compact front-end interface. Third, we position the temporally preprocessed PWM/code output as an electrical precursor to optical activation generation for near-sensor photonic processing. These additions are outside the original CMOS-only ping-pong sensor demonstration and define the contribution boundary of the present work.

4 Front-End Functions and Operating Modes

For a near-sensor photonic processing chain, a useful front-end should provide more than raw image export. Relevant functions include temporal differencing, compact readout of motion-relevant information, suppression of redundant pixel traffic, and an electrical output representation that can directly drive a later modulation stage. These functions are consistent with recent near-/in-sensor processing frameworks, which aim to reduce pre-inference conversion and transmission cost before data reach downstream compute [7–10, 12–15].

The broader ping-pong architecture supports three useful modes: image-capture (IC) readout for full image reconstruction, frame-difference (FD) operation for motion-oriented sensing, and saliency/spatially downsampled (SD) output for sparse event reporting [3]. Among these, FD mode is the most relevant to the sensor-to-photonic interface considered here because it suppresses static background information and presents a compact temporal code instead of a raw frame. Accordingly, the front-end implemented and validated in this work focuses on the FD operating mode.

5 Ping-Pong Temporal Front-End and Readout Circuit

Following the prior ping-pong PWM pixel principle [3], the front-end implemented in this work adopts alternating odd and even storage paths. One lane stores the previous temporal state while the other integrates the current exposure result; the roles then swap in time. This phased reuse of analog state enables frame-to-frame differencing without relying on full-frame digital storage.

At the pixel/front-end level, the key internal nodes are the odd/even gate-state nodes and the corresponding analog pulse-generation nodes that determine the eventual PWM output. A global threshold ramp is used during readout so that the crossing time between the ramp and the stored analog state determines the pulse width. Temporal difference is therefore encoded directly

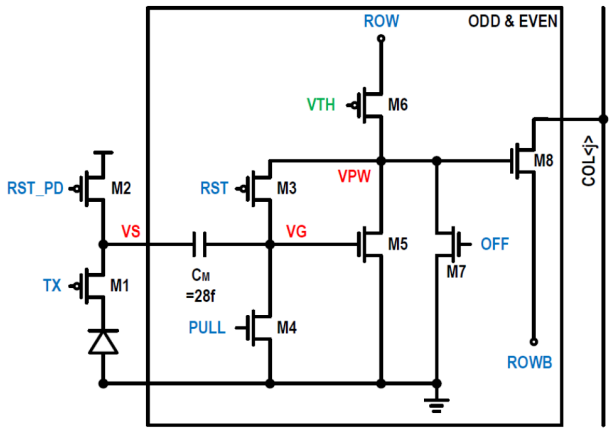

Figure 2: Simplified ping-pong PWM pixel/front-end schematic, redrawn from the ping-pong PWM temporal pixel concept in [3]. The odd and even lanes alternately store temporal state, while a global threshold ramp converts the stored analog difference into a PWM-coded temporal output for downstream readout.

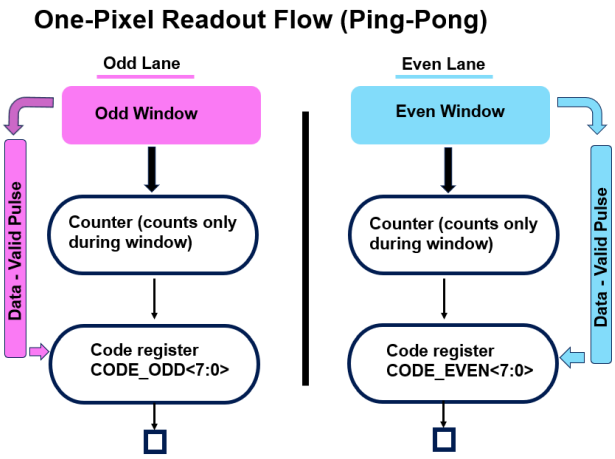

Figure 3: One-pixel ping-pong readout flow. Separate odd and even windows drive lane-specific counting and code-register capture, while DATA_VALID strobes identify when each 8-bit lane output is ready for downstream sampling.

in the time domain and later digitized through a compact counter-based path rather than through a conventional per-column ADC.

To validate the front-end, we developed a one-pixel mixed-signal testbench in TSMC 0.18 µm with 0.8 V logic levels. The testbench combines the analog ping-pong pixel front-end, a Verilog-based timing/controller block, comparator-based PWM detection, a PCLK-driven counter, and an 8-bit output-capture path. The readout path counts only inside the intended active window and uses a single-clock DATA_VALID pulse to latch the current 8-bit value, providing clean byte framing and explicit odd/even lane qualification.

Table 1: Current validation and architecture-level metrics. Power and throughput are preliminary architecture-level estimates rather than full-chip measured silicon results.

Metric	Current value / observation
Technology	TSMC 0.18 µm mixed-signal
Core logic level	0.8 V
Readout code width	8 bits
PCLK period	0.390 µs
DATA_VALID width	1.017 µs (≈ 2.61 PCLK cycles)
Odd/even valid overlap	0
Capture latency	Next PCLK edge after DATA_VALID assertion
Estimated power	70 µW to 75 µW
Estimated throughput	700 fps to 1000 fps
4×4 storage state	128 DFFs for 16 × 8-bit pixel codes
4×4 total digital state	168 DFFs incl. storage, counters, support logic

6 One-Pixel Validation Results

The one-pixel mixed-signal environment demonstrates correct alternating odd/even behavior, stable holding of the 8-bit value between DATA_VALID pulses, and consistent end-of-window latching. Simulation-extracted source-synchronous timing from the current validation flow shows a PCLK period of approximately 0.390 µs and a DATA_VALID width of approximately 1.017 µs, corresponding to about 2.61 clock periods. The extracted odd/even DATA_VALID overlap is zero, so each valid event is unambiguously associated with one lane only.

At the digital interface, the readout rule is simple: on DATA_VALID assertion, the 8-bit code is captured on the next PCLK rising edge. This implies a one-clock source-synchronous capture latency while still leaving at least two PCLK edges within the valid window, which provides comfortable timing margin for downstream sampling. The interleaved code plots confirm that codes update only on their designated valid windows and remain stable otherwise.

Current architecture-level estimates, based on the validated one-pixel readout concept and supporting system analysis, indicate a total front-end power of roughly 70 µW to 75 µW and a throughput potential of roughly 700 fps to 1000 fps. These benefits follow from eliminating column-level ADCs, operating the supporting digital logic at 0.8 V, and overlapping temporal storage and readout through the ping-pong scheme. Because these numbers come from the present simulation and system-estimate stage rather than from full chip measurements, they should be regarded as preliminary but still representative of the current design direction. They are reported to characterize the present implementation path and are not intended as a direct normalized power or speed comparison against the original ping-pong PWM sensor [3].

The present validation effort also clarifies implementation overhead. For a 4×4 demonstrator, storing one 8-bit value per pixel requires 128 DFFs, and the total digital state including storage, counters, and support logic is 168 DFFs. This small-state overhead is consistent with the intended role of the front-end as a compact temporal preprocessing and interfacing block rather than as a heavy digital back-end.

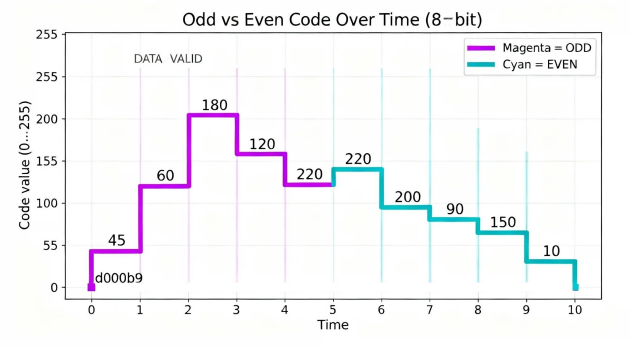

Figure 4: Representative one-pixel validation results. Alternating odd/even 8-bit code capture demonstrates correct lane interleaving, stable code holding between updates, and repeatable mixed-signal timing behavior.

7 Bridge to Near-Sensor Photonic Processing

The output format of the implemented front-end is well suited to a downstream optical processing stage because it already converts raw photodiode activity into a temporally meaningful, reduced-bandwidth electrical representation. This photonic-interface use case is a central distinction from the original ping-pong PWM sensor context [3]. Instead of forwarding raw frame data, the sensor can export frame-difference information in PWM or compact-code form, which is a more appropriate electrical precursor for optical activation generation.

In such a workflow, the temporally preprocessed output of the adopted ping-pong front-end would drive a subsequent modulation stage, allowing motion-relevant electrical information to be forwarded into an optical compute path. The value of this bridge is that temporal differencing is performed before the photonic stage is invoked, thereby reducing the amount of redundant data and lowering the required burden on later optical modulation and compute blocks. The paper therefore contributes an interface-oriented adaptation and validation path for sensor-to-photonic processing rather than a new claim on the underlying ping-pong pixel principle.

8 Conclusion

We presented a mixed-signal implementation and sensor-to-photonic adaptation of an ADC-less ping-pong temporal front-end for low-overhead frame-difference sensing. The underlying ping-pong PWM pixel principle is adopted from prior CMOS vision-sensor work; the contributions here are the low-voltage implementation, DATA_VALID-qualified counter readout, one-pixel mixed-signal validation, and photonic-interface positioning. Preliminary validation demonstrates stable analog boundary waveforms, correct odd/even temporal sequencing, a 1.017 µs DATA_VALID window with zero odd/even overlap, and repeatable interleaved 8-bit output capture. Together with current 70 µW to 75 µW and 700 fps to 1000 fps design estimates, these results establish the adopted front-end as a practical sensor-side temporal preprocessing block and a candidate electrical interface stage for later near-sensor photonic processing.

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