DISSERTATION

THE EFFECT OF TRAPPING DEFECTS ON CIGS SOLAR-CELL PERFORMANCE

Submitted by

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In partial fulfillment of the requirements

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WE HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER OUR SUPERVISION BY PAMELA K. JOHNSON ENTITLED THE EFFECT OF TRAPPING DEFECTS ON CIGS SOLAR-CELL PERFORMANCE BE ACCEPTED AS FULFILLING IN PART REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY.

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ABSTRACT OF DISSERTATION

THE EFFECT OF TRAPPING DEFECTS ON CIGS SOLAR-CELL PERFORMANCE

The relationship between basic solar-cell parameters and carrier-trapping states is explored through current-voltage, quantum efficiency, and temperature-dependent capacitance measurements, including admittance spectroscopy (AS) and drive-level capacitance profiling (DLCP). The study focuses on several categories of $CuIn_{1-x}Ga_x(Se_{1-y}S_y)_2$ (CIGS) solar-cell devices. Some devices were produced by evaporation, and some by selenization of metal films. Within each of these two groups of devices, some devices have a standard CdS buffer layer separating the CIGS absorber from the ZnO window layer, while others have had the CIGS absorber treated in a Cd-containing bath, but no CdS layer deposited between the absorber and the ZnO window layer. The latter device preparation technique (Cd PE treatment) tended to result in devices with a weaker junction.

Although there are numerous ways in which the devices studied can be categorized, three sets of general experimental trends were noted. One set of comparisons was made between all evaporated and all selenized devices. Another set of trends was observed when comparing CdS devices to their Cd PE counterparts. The final set of trends was observed when comparing all selenized devices to each other. Within these studies, all evaporated $CuIn_{1-x}Ga_x(Se_{1-y}S_y)_2$ devices had y = 0, and all selenized devices had y $\approx$ 0.3. The

typical maximum value of x in all devices studied is 0.3, although x varies differently with depth in the evaporated than in the selenized devices.

Comparisons between evaporated and selenized devices yielded several strong trends. The evaporated devices tend to have higher open-circuit voltages (V_{OC}) when considering comparable junctions, lower defect activation energies (E_a), and fewer defect states detected near the interface than the selenized devices. Slightly weaker trends observed include a tendency of the evaporated devices to have a lower diode quality factor than selenized devices made with a comparable junction. Admittance spectroscopy results imply that the overall defect density (N_t) of the evaporated devices is lower.

Within the group of selenized devices, the observed trends were somewhat surprising. A higher trap density deduced from DLCP appears to modestly correlate with a higher V_{OC}. This correlation suggests that the majority of the detected traps do not participate in recombination that limits the performance of the devices. When the total response of the DLCP measurements is evaluated, i.e. the approximate trap density plus the free carriers, the devices with larger DLCP responses were the devices with larger V_{OC}. Thus, the detected traps may be affecting a device much like non-frequency dependent shallow acceptor levels. Barring other differences, the larger the density of shallow acceptor states in a device, the larger the open-circuit voltage of the device. This must now be put in perspective with the aforementioned observations comparing evaporated and selenized devices. Based on V_{OC}, it does not appear that the best selenized devices have the lowest trap density. Thus, although the selenized devices do have a higher trap density than the evaporated devices, the overall number density of shallow traps may not be the reason the selenized devices do

not perform as well as the evaporated devices, rather merely the presence of a measurable density of defect states near the interface may be the reason for the performance difference.

Although the best devices (evaporated) seem to have an overall trap density that is lower than the other devices, it does not appear likely that the density of traps within the detection range is what is limiting the performance of the selenized devices. However, the location of the traps (near the interface vs. in the bulk) does appear to be related to device performance. Thus, based on this work, the CIGS research community should use the DLCP technique supplemented with AS for evaluating more precise free carrier densities for the best devices and DLCP data analyzed using multiple analysis techniques for evaluating trap states near the interface, but should perhaps focus on other techniques that are more likely to probe deeper into the band gap to search for recombination centers in the bulk in all well-behaved devices.

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1.1.1 Renewable Energy Aspect

1.1.1.1 Supply of Finite Energy Resources

We live in a world where now more than ever electrical and mechanical power resources are political power. Currently, some of the most commonly used sources of electrical and mechanical power combined are oil and its derivatives. Almost every person in the United States is dependent in some way on oil, whether it be for transportation or comfort heating. This country's need for oil has wielded for some time, and continues to wield considerable influence on our foreign policy. As we near a predicted peak of world oil production due to the finite world oil supply (see Figure 1.1), we can only anticipate an increased influence of the demand for oil on the foreign policy of the United States. This influence could conceivably even affect the stationing of military troops and in what practices they engage. While in the near term it is not conceivable that this country will lack in need for foreign oil, increasing our dependence on renewable energy could most certainly temper our foreign-oil need and perhaps lead to more altruistic motivations for foreign policy decisions. This could potentially bolster dwindling world respect for the United States, which could also lead to increased safety for its citizens. In addition, as Figure 1.1 and others like it predict, in the next ten years the amount of oil available for consumption on

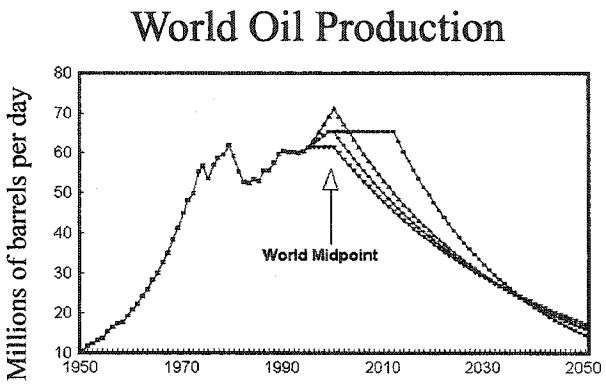

Figure 1.1. Campbell World Oil Production Plot

a daily basis will already be declining. Not all sources agree on the immediacy of this decline [1], however there can be no disputing that oil is a finite (i.e. non-renewable) resource. Due to the finite world oil supply, in the future we will be forced to take an even larger share of the world's available oil unless we as a country utilize stringent conservation practices or alternative energy sources. Currently, citizens of other countries are growing increasingly vocal regarding the disproportionate amount of oil used by the United States. While several alternatives to oil exist, historically the United States citizenry has been much more amenable to the use of renewable energy sources compared to other sources, such as nuclear power. Consequently, we must continue to develop the technology required to harness renewable energy since the supply of oil, whether regulated by geological or political means, will not always be sufficient.

1.1.1.2 Pollution Considerations

Not only can renewable energy play a substantial role in freeing the United States from the struggle for a large portion of the world's oil supply, but it can also play a significant role in preventing pollution. In particular, the use of renewable energy sources such as wind and solar power can significantly decrease the amount by weight of regulated air pollutants emitted into the atmosphere on an annual basis. A recent study shows that in addition to high levels of air pollution creating breathing difficulty for the elderly, and those who suffer from emphysema and asthma, air pollution may actually cause asthma [2]. The cited study focused on pollutants commonly emitted from internal combustion gasoline engines. The logical question to ask now, in the context of this manuscript, is how can power from solar cells can help improve this situation? Solar energy can contribute to the reduction of gasoline burned on our streets and highways by providing the energy

to produce another renewable energy source. That energy source is hydrogen. Many automobile manufacturers, including Ford, Honda, Toyota, BMW and Daimler-Chrysler, have built hydrogen-powered vehicles and are continuing to ready them for the market. However, extracting hydrogen from water requires an energy source. In order to achieve the maximum pollution reduction possible by using hydrogen instead of gasoline to power passenger vehicles, the hydrogen would need to be both extracted using a renewable energy source and be extracted near the distribution point for passenger vehicles. Solar cells can meet both of these requirements. Thus, proposals have been made that solar cells be this energy source.

Another use of solar cells motivated in part by pollution considerations is use by electrical utilities. A utility company in Arizona has already installed solar cells that have lenses increasing the intensity of the incident sunlight in order to provide power to its customers much like any other power-generation unit powered by a non-renewable resource.

1.1.1.3 Off-grid Applications

Yet another use for solar cells occurs when conventional power lines are not feasible to use or install in remote locations. These uses exist around the world. In the United States, off-grid applications vary from powering roadside emergency phones to powering vacation or permanent homes in remote locations. On average in the United States, solar cells are more economical than connecting to the utility grid for homes that are 1 km or more away from the nearest grid.

1.1.2 Polycrystalline Thin-film vs. Other Solar Cells

Just as biomass, wind, solar, and other renewable energy sources all have relative benefits, thin-film and single-crystal solar cells also have relative benefits. Currently, the obvious benefit of single-crystal solar cells is their higher power conversion efficiency. This is a significant benefit in an industry that sees high efficiency cells as the key to survival, since it is the most straight-forward way to deliver lower cost solar power to the consumer. Consequently, thin-film solar cells must have other significant advantages in order to compete with the single-crystal cells. One of the relative advantages of thin-films, although not necessary in all applications, is that the much lighter thin-films are superior when mass is a constraint. Another benefit of thin films is less raw materials usage, and hence lower materials cost for solar cells. Polycrystalline thin-films can also typically be more forgiving of small amounts of impurities in the material due to feedstock or relaxed manufacturing standards compared to single-crystal devices. In addition to being somewhat tolerant of impurities, thin-films are also typically somewhat tolerant of, and to some extent even benefit from, "imperfect" boundaries between the crystallites, whereas single-crystal devices typically demand significant consistency from one unit cell to the next. Such tolerances result in thin-films being rather amenable to large-scale production. While all thin-films share these benefits, polycrystalline thin-film products currently have the benefit of greater stability (i.e. longer service lifetime) than the amorphous-silicon thin-film products.

1.2 Operation Basics of Polycrystalline Thin-film Solar Cells

At the heart of any solar cell is a p-n junction. This junction is located near the metallurgical interface of two thin films, but tends to be just inside the material with the lower

band-gap. While single-crystal technology uses controlled techniques and off-valence elements for doping, polycrystalline thin-films take advantage of naturally occurring dopants, i.e. native defects. Native defects exclude systematically introduced off-valence elements. Native defects are just one of the multiple mechanisms through which polycrystalline thin-films achieve the characteristics of a doped material. Not all of the mechanisms are intentional or known. The results of these mechanisms include, but are not limited to, lattice defects present due to the boundaries between the tiny crystals (grain boundaries) within the film, as well as lattice mismatch between the different semiconducting layers of the film. While all defects in the lattice will lead to available energy states, only some will result in states near the band edge, yet within the band gap. It is these states that account for some of the naturally occurring doping. In addition to lattice strain, co-evaporated $CuIn_{1-x}Ga_xSe_2$ (CIGS) in particular, is generally thought to be laden with substitutional impurities and vacancies. Most substitutional impurities arise from either the Cu, In, or Ga cations, or the Se anions. According to Zhang and Wei [3–5], either cation vacancies or Cu substitutional impurities are the most likely of the native defects to act as p-type dopants, i.e. create available states near the valence band edge. However, some impurities in CIGS may also arise from unintentional elements in the vacuum chamber. Again, these defects, if present, could also contribute to available states near the band edge. However, sufficient work has not been reported regarding the energetic location of non-native defects to make a definitive statement. For chemical-bath deposited materials, such as CdS in the devices of interest in this work, there are often remnants of the bath constituents in the final film. These impurities may be yet another instigator of available states near the band edge. Thus,

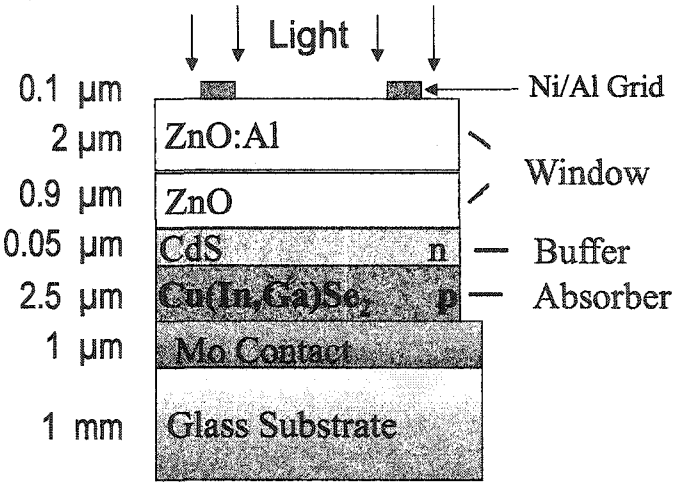

Figure 1.2. Schematic drawing of CIGS-based solar cell configured for laboratory use with window, buffer and absorber layers noted.

it is most likely through some subset of these mostly unintentionally occurring defects that the thin-film materials of interest are produced n- or p-type.

In a direct-gap CIGS-based polycrystalline thin-film solar cell, the topic of this thesis, one finds materials with more systematically controlled compositions surrounding the aforementioned polycrystalline p- and n-type materials. As seen in Figure 1.2, beneath the p-type CIGS is a layer of molybdenum (Mo) on top of soda-lime glass (SLG). On top of the n-type CdS layer is radio-frequency (rf) sputtered ZnO underneath a layer of rf sputtered ZnO doped with Al. The phrase "buffer layer" when used later in the text will serve to describe the CdS or similarly positioned layers, whereas the phrase "window layer," when used later in the text, will serve as a descriptor pertaining to either of the ZnO layers. Test cells are covered with fine Ni/Al grids for securing electrical contact and maximizing gathered current while minimizing shading of the cell.

As seen in Figure 1.2, light is first incident on the ZnO, then the CdS, and finally the CIGS. Photons with enough energy to excite an electron across the band-gap into the

conduction band (typically 1.14 eV for room-temperature CIGS) are then absorbed in the CIGS. Electrons excited into the conduction band are then subjected to a force provided by the electric field created by the p-n junction. Electrons consequently accelerate towards the n-side of the device. The majority of the electrons that make it to the n-side are then subjected to two other electric fields due to the potential difference between the n-side and the first ZnO layer and that layer and the top conducting ZnO layer. The conducting ZnO layer then connects the solar cell to a pertinent external circuit.

The band gaps of the layers on top of the CIGS would optimally be greater than about 3.0 eV, so as to eliminate absorption of a large majority of the photons available for electron-hole pair creation in the CIGS. However, finding a material with such a band-gap that can create an efficient solar cell when paired with CIGS has proven challenging. Consequently, not all light incident on the solar cell is typically transmitted to the CIGS absorber, where the majority of the successful photon to electricity conversion begins.

1.3 Challenges to Fully Realizing the Polycrystalline Thin-film Potential

There are several challenges to improving the efficiency of not only test solar cells, but the modules that will eventually incorporate similar cells. These challenges include using an in-line process, avoiding wet processes where possible, reducing the use of strictly regulated materials, keeping processing temperatures low, and achieving the maximum current and voltage possible from the device. Currently, the best CIGS cells are made using a combination of vacuum techniques, chemical bath deposition, and sputtering [6]. This combination of processes can obviously not be done in-line without great difficulty. Indeed, these materials are not currently processed in-line. In addition, vacuum techniques tend to

be energy intensive due to creating and maintaining the vacuum and the high temperatures often used with these techniques. Consequently, they are an inefficient use of capital and natural resources. Chemical bath techniques also have drawbacks on their own accord in that they often generate more waste than dry processes. In addition, the chemical bath that produces CdS results in environmentally sensitive waste. Consequently, this manufacturing by-product does not promote environmental stewardship, and is more costly to dispose of than less strictly regulated waste. Finally, the community is challenged by the search for an n-type layer that absorbs less of the incoming light than CdS without resulting in excessive carrier (electron or hole) recombination near the p-n junction.

1.4 The Defect Challenge

Before becoming immersed in a discussion of defects in polycrystalline thin-film solar cells, the reader requires knowledge of what a defect is in the context of this thesis. The defects discussed in this work are a subset of defects as defined in a typical solid-state physics text book. These defects include, but are not limited to, point defects such as vacancies, interstitials, or substitutional impurities; dislocations; stacking faults; and grain boundaries [7]. The defects of interest in this work are those that (1) exist in the semiconductor primarily responsible for electron-hole pair production (CIGS) and (2) have resulted in an allowed energy state in the band-gap which is too deep (i.e. far away from the band edges) to unequivocally be a dopant state. These defects are often referred to as trap states.

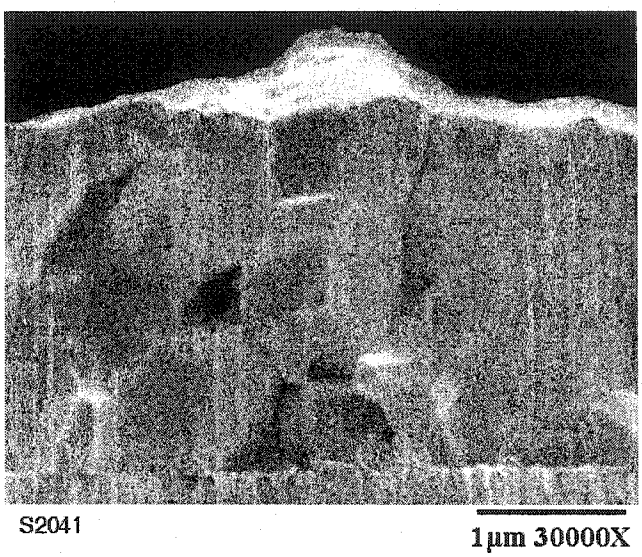

Figure 1.3. Scanning electron micrograph of CIGS film on Mo-coated soda-lime glass substrate. The CIGS film is the dominant part of the image, with Mo seen beneath the CIGS. Image courtesy of National Renewable Energy Laboratory.

1.4.1 The Curiosity and Challenge of Polycrystalline Thin Films

Polycrystalline thin-films are somewhat defect tolerant, yet not completely. Thus, we can accept defects in the materials, but only a certain range of concentrations and energies seems to be conducive to an efficient solar cell. This work aims to shed light on what range of defect concentrations and energies yield the highest efficiency devices.

Detecting most of these defects is complicated in these films as a result of their polycrystalline nature. Grain boundaries are easily observed under a scanning electron microscope (SEM), as seen in Figure 1.3. In addition, transmission electron microscopy (TEM) has also shown dislocations [8]. However, merely making an essentially visual observation of a defect is not sufficient to ascertain whether the defect is electrically active. Also, it is difficult to completely resolve defects other than grain boundaries and dislocations by SEM, TEM or other electron micrograph methods. Consequently, we are left to use elec-

trical characterization methods that provide us with an electrical signature rather than a somewhat direct visual picture.

Just as visual pictures have limits on their resolution, electrical characterization techniques do also. The limits on these techniques are set by the device parameters as well as by experimentally-achievable temperatures and input signal frequencies. Solely using electrical characterization techniques to find these defects makes it almost impossible to clearly establish the defect density in the same measurement as the precise spatial and energetic defect location, but it is currently the most comprehensive approach to characterizing defects.

1.4.2 Defects' Effects on Device Performance

As discussed in Section 1.2, in order for a solar cell to produce electricity, electrons excited into the conduction band in the p-type (absorber) material, must be conducted into the n-type material. Frequently, not all electrons make it to the n-type material, which results in loss of light-generated current. The most common cause of failure to cross to the n-type material is recombination with holes in the valence band through mid-gap states (i.e. trap states). This type of recombination is known as Shockley-Read-Hall (S-R-H) recombination [9]. Recently, Herberholz et al. claimed that "a lower concentration of hole traps is correlated to higher device efficiency," [10]. In addition, a group from the Institute for Physical Electronics (IPE) at the University of Stuttgart has claimed that the same mid-gap states that are limiting the performance of the solar cell through recombination, and are responsible for voltage loss, can be detected using admittance spectroscopy [11, 12], one of the techniques used to collect data for this dissertation. Eventually, enough parallels may be found to have convincing circumstantial evidence that some of the defects detected

using electrical characterization techniques are the same defects responsible for voltage and light-generated current loss in solar cells. This work aims to contribute to that evidence in as solid and convincing a manner as possible.

1.4.3 Summary of Results from Published Defect Studies

1.4.3.1 Theoretical Results

Until recently, researchers were detecting defect states, mostly in $CuInSe_2$ (CIS), yet did not have a very solid theoretical model with which to compare the energy levels of the defects they detected. Consequently, there was a growing amount of experimental results, with very little theory to guide the researchers regarding what elements were most likely causing the detected defects. However, in recent years, a combination of technological advances and increased interest in CIS and its alloys with $CuGaSe_2$ (CGS), encouraged scientists at the National Renewable Energy Laboratory (NREL) to theoretically investigate energy levels of defects in both CIS and CGS [3, 4]. This work not only provided very useful theoretical values for comparison with experimentally determined values, it also compiled many experimental results regarding defects in CIS. Although this was very useful, an analogous study has not been done for CIGS, the most common of the three materials for making high efficiency devices. Consequently, I have estimated where in the CIGS band gap these levels are likely to be, based on a linear interpolation of the calculated levels in CIS and CGS, and the relative band gaps of CIS, CIGS, and CGS. Not all of the defect levels required for these calculations have been published. These values were instead obtained through personal communication [5]. All band gaps used in the estimates were low-temperature band gaps, as that is what the original publications used.

Also, when defects are experimentally detected, they are typically detected at temperatures below room temperature. The assumed Ga/(In+Ga) ratio was ~0.3 for CIGS. The most likely defect levels in CIGS, related levels in CIS and CGS, and their assigned composition are given in Figure 1.4. The likelihood of occurrence was determined based on defect formation energies (where available), assumption of Cu-deficient material, and comparison with experimentally determined levels. A comprehensive figure containing all calculated levels appears in the Appendix.

1.4.3.2 Experimental Results

Studies published thus far on this topic have concentrated on reporting results of activation energies, densities, and capture cross sections of defects in solar cells within a certain efficiency range, typically near 12%. The studies cited here have reported defects in the absorbers of CIS as well as CIGS-based devices, most with n-type CdS layers, similar to Figure 1.2. The left side of Figure 1.5 displays calculated defect energy levels within the CIS band gap [3]. Displayed levels were chosen using the same criteria used when choosing the CIGS levels presented. The right side of Figure 1.5 displays experimentally determined defect levels in CIS, grouped by the activation energy and type (donor or acceptor) of the defects. In contrast to the typically monocrystalline results published in [3], the experimental results are almost solely from working polycrystalline thin-film CIS devices with efficiency greater than 8%. However, the efficiency was not given in every case. These results are compiled from several sources [10,11,13–20]. While some of the theoretical and experimental levels are aligned with each other, some show definite discrepancies with the other.

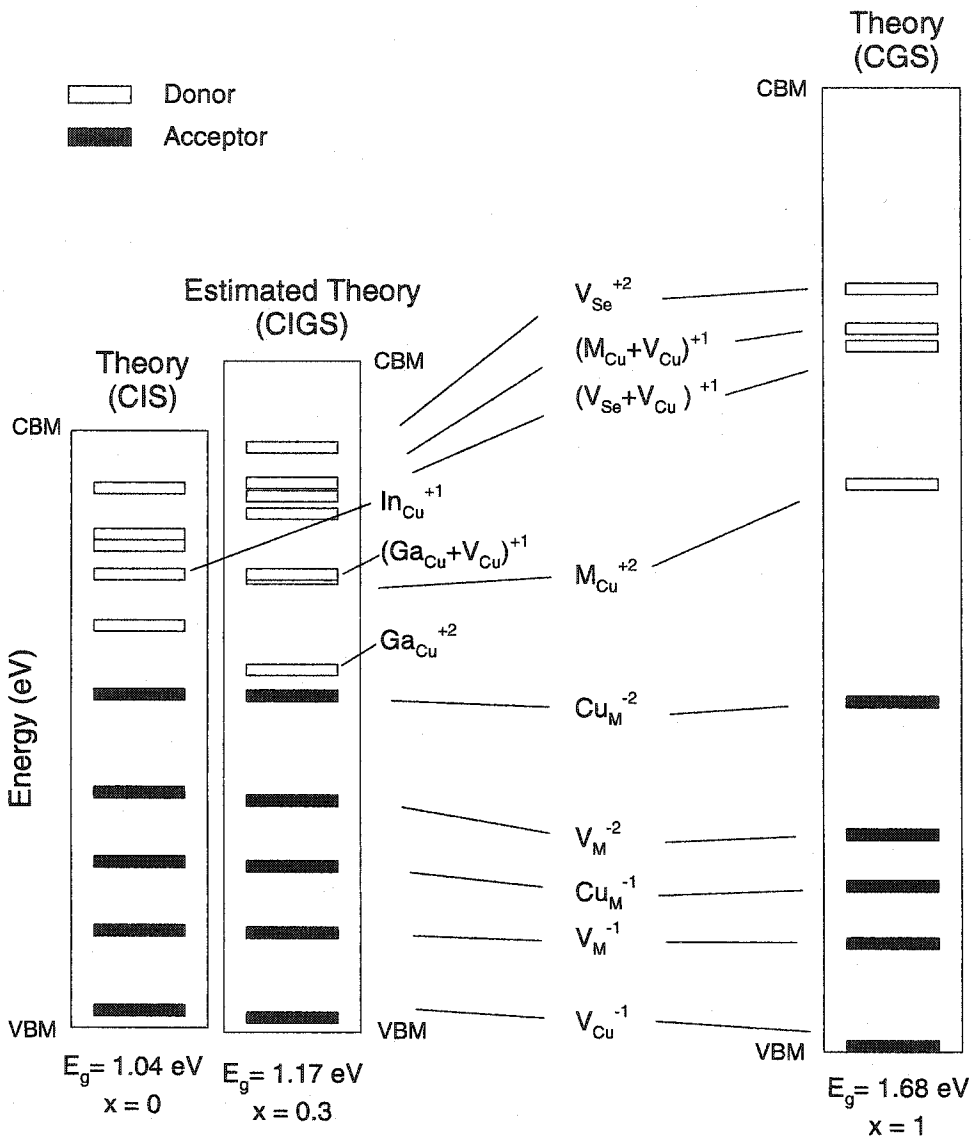

Figure 1.4. Calculated defect levels in the CIS and CGS band gap,[3, 4], and interpolated defect levels in CIGS. M pertains to Ga for CGS, In for CIS, In for CIGS donors, and either In or Ga in the case of acceptors in CIGS. Only the levels most likely to form in each material type are shown.

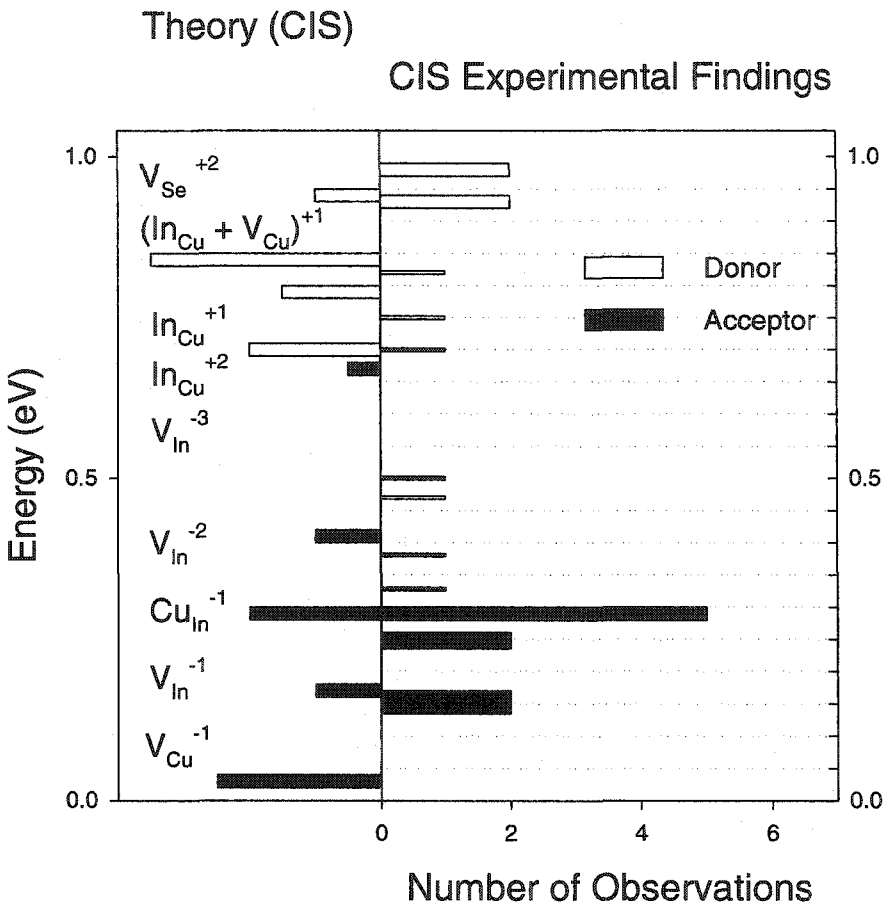

Figure 1.5. Theoretical and experimental defect levels in CIS, after Zhang [3]. Width of the experimental bars indicates range of published values; length indicates number of samples reported within the defect range. The length of the theory bars is proportional to the likelihood of defect formation.

The nomenclature used at the University of Stuttgart (IPE) and closely collaborating institutions labels the major defects detected in CI(G)S as N1 and N2. N1 has been assigned by IPE and several collaborators in Europe to donor-like defects (electron traps) found at the interface of CI(G)S and the nearest window layer. Typical activation energies range from 50 - 200 meV. These collaborators typically assign N2 to acceptor-like defects (hole traps) with an activation energy generally ranging from 200 - 300 meV. However, admittance spectroscopy (AS) studies undertaken at the University of Oregon on CIGS devices have only shown one defect, with properties similar to N1 [20]. The defects found at Oregon have activation energies that range from 50 - 300 meV. The defect property similarities are outside the scope of this text, but are discussed thoroughly by Heath [20]. These and other defects, primarily in polycrystalline thin-films, including defects in $CuIn_{1-x}Ga_x(Se_{1-y}S_y)_2$ (CIGSS) are shown in Figure 1.6. Although the energetic location of the defects are not likely to be exactly the same, since the incorporation of S tends to pull the valence band down, they are likely to be fairly close given the similarity of the band gap of the CIGSS materials studied and typical CIGS. Indeed, several experimental and theoretical results are closely aligned in the figure. Table 1.1 lists the reported activation energies of the defects in Figure 1.6, the detection method, and the group that reported the values. In some cases, Table 1.1 also lists the group that made the samples as a secondary item under the heading Research Group.

While CIGS-deposition differences may not explain the lack of two different defect signatures in AS measurements, it should be noted that the majority of the devices showing two defects in the European work incorporated CI(G)S from a single-step evaporation process, while the majority of the devices studied in Oregon incorporated CIGS from a 3-

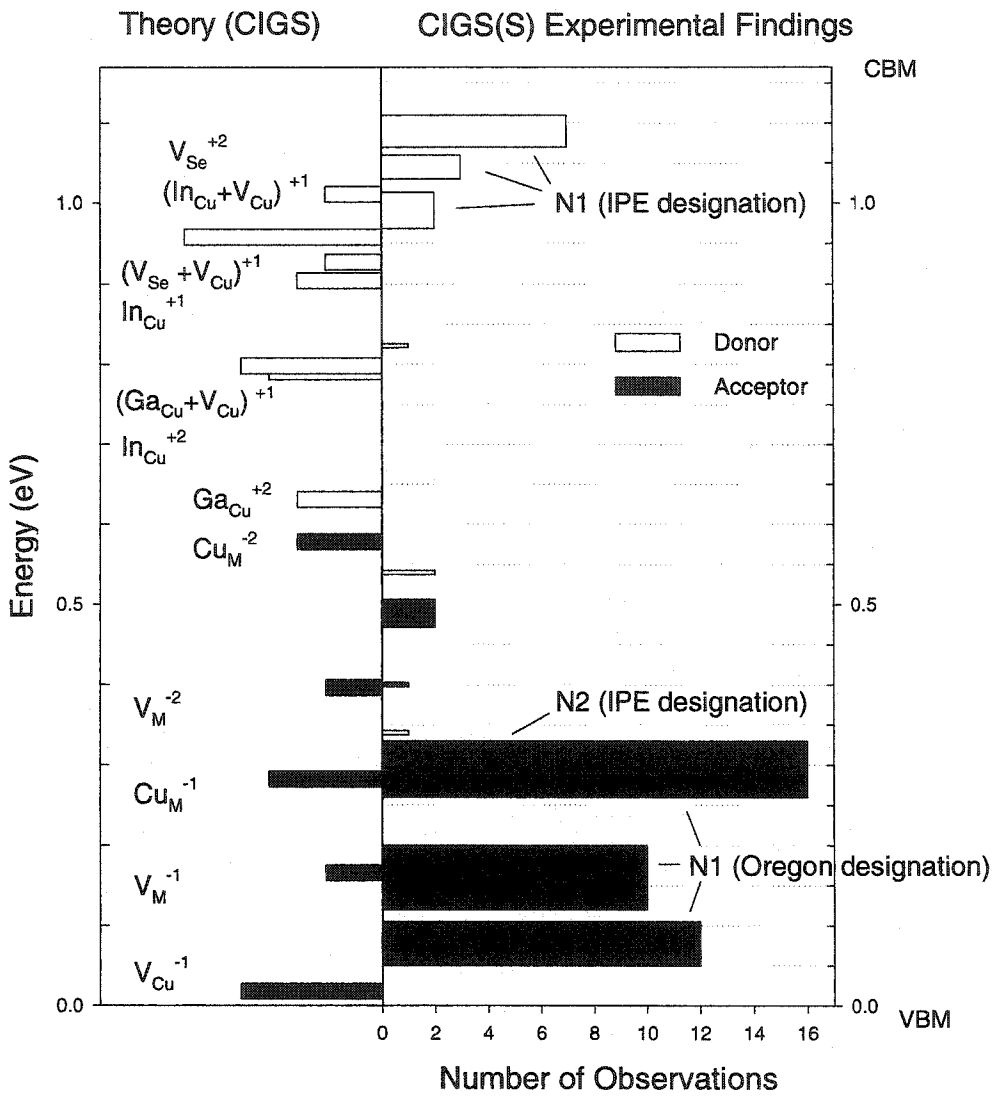

Figure 1.6. Theoretical and experimentally determined defect levels in CIGS, after Zhang [3]. The vertical extent of the experimental bars indicates the range of published values, while the horizontal extent of the bars indicates the number of samples reported with a defect in that range.

stage evaporation process. Based on admittance spectroscopy, an argument has been made [20] that N1 is not an energetically continuous interface state, but rather a bulk state. This argument is based on the implications of layer thickness and conductivity type if N1 was an interface state, both of which contradict known parameters of the n-type layers in these devices.

There are two studies [20, 21], that attempt to correlate defect densities with cell performance that include more detailed parameters of the studied devices than just efficiency. However, the conclusion of one of these studies [20] is that there doesn't seem to be any apparent correlation between activation energies or defect densities with Ga content or with efficiency (η), fill factor (FF), or other performance indicators discussed in Chapter 3. However, the other study correlates a higher open-circuit voltage (V_{OC}) with a less than "standard" concentration of midgap defects [21]. This same study attributes free carrier contributors to shallow acceptor-like defect levels detected using AS.

The aim of the current work is to bring some clarity to the complex picture of defects in CIGS solar cells by coupling comprehensive device performance and defect-state analysis. The desired result is to help increase the efficiency of polycrystalline thin-film CIGS solar cells by examining defects within the band gap of the CIGS. The following two chapters will discuss sample preparation and laboratory measurement and analysis techniques. The subsequent chapters will return to data analysis and discussion to explore correlations between defects and device performance. This exploration will provide some clues as to why some studies find correlations between defects and device performance, while others find none.

Detection Method	Electron Trap Level [meV]	Hole Trap Level [meV]	Research Group	Reference
AS	60, 70, 110		Gent and IPE	[22]
AS, DLTS	77		IPE	[19]
DLTS	90, ~100	270	NREL	[23]
AS	~100	105	IPE	[11]
AS	120-140	290	IPE	[24]
AS	130		IPE and Warsaw	[10]
AS, DLTS	157		IPE	[19]
DLTS	200		Warsaw	[25]
AS, DLTS	347		IPE	[19]
DLTS	630		NREL	[26]
DLTS	830		NREL	[23]
AS		50, 75	Bayreuth	[21,27]
AS		66, 74	U of Oregon/NREL	[20]
AS		61, 70, < 100, ~100	U of Oregon	[20]
AS		120-190	Bayreuth	[28]
AS		~150, 187, ~200	U of Oregon	[20]
DLTS		260	NREL & Warsaw	[23,25]
DLTS, AS & MPC		260-280	Workshop participants**	[29]
AS		280-330	Bayreuth	[30]
AS		280	IPE	[12]
AS		~300	IPE	[11]
AS, DLTS		308	IPE	[19]
AS		320*	U of Oregon/ Illinois	[20]
AS		400	IPE	[31]
AS, DLTS		470, 508	IPE	[19]
*Measured on epitaxial CIGS films				
**Universities of Gent & Bayreuth; Dresden & Warsaw Technical Universities; ENSCP Paris, IPE, Hahn-Meitner Institute, & Siemens Research Laboratories				
DLTS – deep level transient spectroscopy, MPC – modulated photocurrent				

Table 1.1. Defects Detected in CIGS(S) Devices

Chapter 2

Device Fabrication Techniques

All devices in this study incorporated soda-lime glass (SLG) substrates coated with molybdenum. Absorbers, and in some cases buffer layers, were deposited after the molybdenum. Subsequent deposition processes of ZnO windows and Al/Ni grids for electrical contacts were identical. However, the CIGS absorbers were deposited using two substantially different processes. These processes are described below.

2.1 Patented Three-Stage NREL Process for CIGS Deposition

The three-stage process is a process to deposit the absorber that involves 3 different processing stages, differentiated by the temperature of the process and the elements deposited. Although the three-stage process is intended for industrial use, the research laboratory version of three-stage deposition is typically done by physical vapor deposition (PVD), a process that is not well-suited for industry [32, 33]. Since intended for industry use, however, the scheme commences by depositing materials that can be deposited at relatively low substrate temperatures. These materials deposited in the first stage are In, Ga, and Se, at a substrate temperature between 250 and 300 °C. Although the final Se-content of the CIGS is stoichiometric, the Se flux is typically three times that of the metals. The resultant film from this first stage is $(In_{1-x}Ga_x)_2Se_3$. In both this preliminary film and the completed film, x is nominally 0.3, with some variation with depth. The second continuous stage involves exposing the films deposited in the first stage to Cu and Se flux at a significantly higher substrate temperature, between 500 and 560 °C. Again, the Se flux is

about three times that of the Cu flux. This Cu-rich (when compared to the other cations) growth stage is credited with increasing the grain size of the resultant film as compared to the film grown in the first stage. The third stage consists of depositing the remaining 10 - 20 % of the In and Ga, again in a Se atmosphere. The substrate temperature remains the same as during the second stage of film growth. While not labeled as such, a fourth (i.e. the final) stage involves cooling the sample to 350 °C in a Se atmosphere.

The 3-stage process results in a CIGS absorber with a graded band gap. The band gap is greatest at the back of the CIGS, next to the Mo, and decreases towards the top surface. In the top approximately 10% of the CIGS, the band gap then increases with decreasing distance to the as-deposited CIGS surface. Devices fabricated from absorbers produced in this manner will be referred to as evaporated devices. This is the absorber preparation technique used in the current world-record efficiency CIGS solar cell. A schematic of this device was shown in Figure 1.2.

2.2 Selenization of Sputtered Metal Precursors in a Manufacturing Environment

The absorber layers of the remaining devices in this study were fabricated by the selenization of sputtered metal precursor films at Siemens (now Shell) Solar Industries (SSI) in Camarillo, California. These absorbers were deposited on SLG substrates that had a SiO_2 barrier layer deposited prior to the molybdenum deposition [34]. The SiO_2 serves as a barrier to Na out-diffusion from the SLG. This industrial fabrication process involves sputtering Cu, Ga, and In precursors on the Mo/SiO_2 base electrode. These precursors are then heated in H_2Se and H_2S to form the $CuIn_{1-x}Ga_x(Se_{1-y}S_y)_2$ absorber, with x ranging from near 0 at the front of the device to 0.3 near the back of the device and y nearing 0.3 at

the front and back of the device, and significantly lower elsewhere. The manufacturing line on which these absorbers were produced typically produces circuit plates ~30 x 120 cm. From these relatively large semiconductor-coated plates, pieces no larger than 10 x 20 cm were cut and sent to NREL for further processing. Devices produced in this manner will be referred to as selenized devices. When completed at SSI, absorbers fabricated using this process yield what at times have been world-record efficiency CIGS solar cell modules.

2.3 Subsequent Processing

Both sets of absorbers designated for this study (evaporated and selenized) were divided into two groups. One group had a CdS buffer layer deposited prior to the ZnO window layer, and the other group received a treatment in a Cd-containing bath that did not deposit a CdS layer, prior to the ZnO window layer deposition. The latter devices are referred to as Cd PE treated devices. More detail on these processes is given in the following subsection. Within each of these groups, some of the devices received a post-annealing treatment in air at 200 °C for 5 minutes prior to the ZnO deposition, while others did not. This process variation is only mentioned for completeness, as not all device variations regarding annealing were able to be studied, and among those studied, no universal performance correlations among the cells with similar annealing treatments were noticed. However, other researchers involved in a subset of these experiments did note what appeared to be a change in the activation energy of the detected defects with annealing among the selenized devices [20]. Since this was just one parameter out of many, this work will not distinguish between those devices that received an annealing treatment and those that did not.

2.3.1 CdS Deposition vs. Cd PE Treatment

CdS layers were grown from an aqueous solution containing 0.0015M $CdSO_4$, 1.5M NH_4OH, and 0.0075M thiourea at a maximum temperature of 65 °C for 15 min. For the Cd bath treatments, the procedure was similar to the CdS deposition, but the thiourea was omitted and the process temperature was slightly higher (75 °C, 30 min. or 80 °C, 22 min.) This step is described as a "Cd partial electrolyte (Cd PE)" treatment. Based on the photovoltaic properties of resultant devices, we know that both of these chemical bath treatments on CIGS absorbers result in the formation of a p-n junction. Since a part of the ZnO window layer is doped n-type, the natural question to ask is whether it is actually the Cd PE treatment or the ZnO that creates the successful p-n junction. Several studies have addressed this issue and determined that while a p-n junction heterostructure is created with p-type CIGS and a ZnO window layer, the photovoltaic performance is much improved when the CI(G)S is treated in the Cd PE bath prior to the ZnO deposition [35–37].

2.4 Motivations for Device Selection

2.4.1 CdS vs. Cd PE

At this time it is prudent to mention the motivation for studying the device set used in this work. The motivation for studying solar cells with a CdS layer vs. Cd PE treated devices is two-fold. The first motivation is to learn more about what in the cell fabrication process is actually responsible for creating the relatively good quality photovoltaic junction. The more that is known about how the successful junction is made, the better chances there are to make even more successful junctions, and consequently devices. The Cd

PE treatment allows us to separate the effect of the Cd on the device from the effect of the S on the S-free absorbers. We will see later that the Cd PE treatment results in a device with a somewhat inferior junction as compared to a device with a CdS layer, but an improved junction when compared to devices without either a CdS buffer layer or the Cd PE treatment. Thus, we asked the question, "Are trap states the reason the Cd PE devices have a somewhat inferior junction, compared to the CdS devices?" The results of this investigation will follow in Chapters 4 and 5.

The second motivation to create the Cd PE devices is to enhance the collection of photons in the absorber by removing or minimizing any layers above the CIGS with band gap less than ~3 eV, while still creating a sufficiently strong junction. CdS has a band gap of ~2.4 eV, which is low enough to absorb ultraviolet and blue light needed to boost current generation in the absorber. Although not obvious a priori, current collection resulting from electron-hole pairs generated by similar-wavelength photons is experimentally higher when the generation occurs in the absorber, than when the generation occurs in one of the window or buffer layers. Thus, in addition to improving our understanding of junction formation, we can also hope to understand, and consequently improve, performance of devices that maximize absorption of the sun's spectrum (discussed further in the next chapter) in the absorber layer of the device.

2.4.2 Evaporated vs. Selenized

As mentioned earlier in this chapter, the evaporated devices were made in a research laboratory setting, while the selenized devices were made on the manufacturing floor of a commercial factory. The laboratory process has resulted in multiple (including the current) world record efficiency small-area devices. The manufacturing process has resulted in

world-record efficiency solar-cell modules. However, when made into small-area (less than 1 cm^2) devices, the laboratory devices yield considerably higher efficiencies. This could be for multiple reasons. Here we investigate whether trapping states are part of the reason the small-area evaporated devices out-perform the selenized devices.

While most all of the aforementioned iterations of device preparation were intended for study, not all of the annealing variations were able to be studied due to failure of the SSI absorber material to interact well with the buffer and window layer processing at NREL. This failure to successfully interact was so unexpected that it was discussed at the most recent National CIS R&D Team Meeting [38].

2.5 General Performance Results

Although the experimental techniques must first be discussed in order to understand device performance, some general comments regarding the performance differences resulting from the various fabrication techniques will be made here to set the stage for the results presented in Chapter 4.

2.5.1 Devices from Evaporated vs. Selenized Absorbers

When comparing devices with similar subsequent processing, i.e. one Cd PE treated device to another, one device with a CdS buffer layer to another, the devices with the evaporated absorbers had consistently higher open-circuit voltages (V_{OC}) and consistently higher band gaps. Figure 2.1 demonstrates the grouping of V_{OC} values of the evaporated devices and the separate grouping of the selenized devices, all with CdS buffer layers. One device of each type is from the current study, while the other devices are from past experiments,

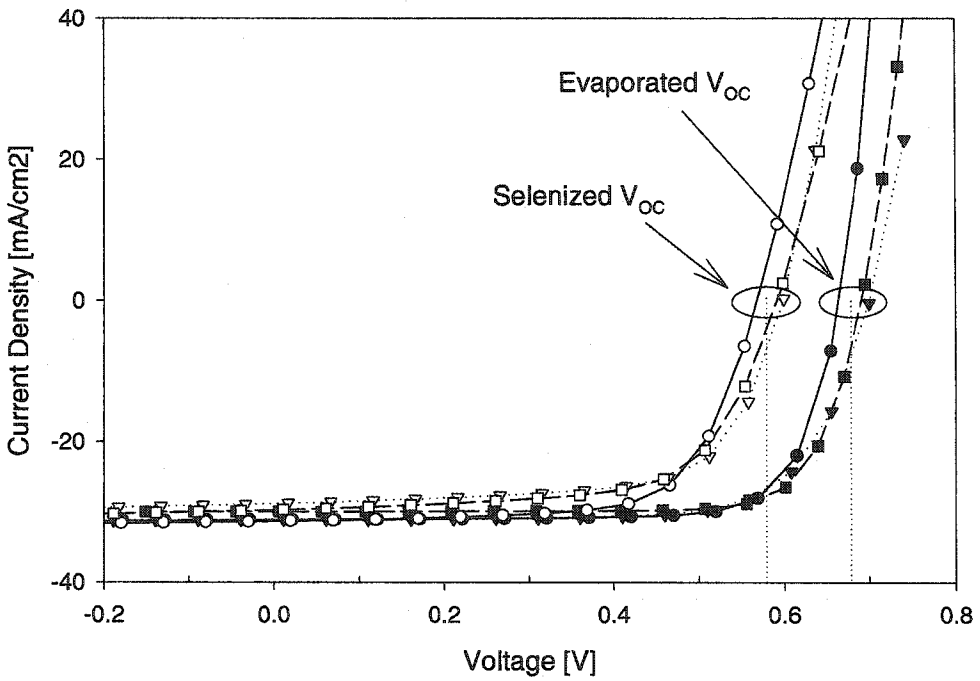

Figure 2.1. Current vs. voltage plots of devices with CdS buffer layers, emphasizing the difference in V_{OC} between the selenized and evaporated devices. Also note the similarities in V_{OC} among each device type.

demonstrating that devices made in these manners over time have had consistent ranges of V_{OC}. It is clear from Figure 2.1 that the evaporated devices consistently have a higher V_{OC} than the selenized devices.

The built-in voltage, V_{bi}, of a device is directly related to its band gap, as seen in Equation 2.1,

$$qV_{bi} = E_g - qV_D - qV_A, \tag{2.1}$$

with q the fundamental charge, E_g the band gap of the absorber, V_D the voltage difference from the conduction band edge to the dominant donor level in the CIGS, and V_A the voltage difference from the valence band edge to the dominant acceptor level in the CIGS. V_{bi} will be discussed in more detail in the following chapter. For the remainder of this discussion, the only required knowledge is that the built-in voltage is proportional to the open-circuit voltage. Since V_{bi} determines V_{OC}, one would expect devices with a larger band gap to most likely also have a higher V_{OC}. Indeed, this is the case with the devices from this study shown in Figure 2.1. To adjust for the E_g difference, we assumed that if the band gap was larger by 80 meV, than the V_{OC} should be larger by 80 mV. Even after adjusting for the band-gap difference, the evaporated devices still had larger V_{OC} values than comparable selenized devices.

In addition to the evaporated devices having a larger V_{OC} (commonly large when recombination current is low) than the selenized devices, the evaporated devices also had a general tendency to have a somewhat lower diode quality factor (commonly small when recombination current is low.) Calculating the diode quality factor of a device will be detailed in section 2. The trend of JV results for the evaporated devices indicating lower re-

combination currents when compared to the selenized devices will be discussed in further detail in Chapter 4.

2.5.2 CdS vs. Cd PE Treated Devices

The devices examined for this work showed similar performance and quantum efficiency characteristics to CdS and Cd PE devices studied previously [36]. Figures most representative of the historical trends are shown in this subsection. As can be seen in Figure 2.2, the device made from the Cd PE treated absorber has a larger short-circuit current density (J_{SC}), but a lower voltage than the device with a CdS buffer layer. The diode quality factors are roughly 2.0 for the Cd PE device shown and 1.7 for the device with the CdS buffer layer [39]. The combination of higher voltages and lower diode quality factors for the devices with CdS buffer layers point to a stronger photovoltaic junction in these devices.

By design, Cd PE devices typically have a larger J_{SC} due to the lack of a buffer layer with a band gap below 3 eV. This allows most all photons with wavelengths longer than approximately 415 nm to pass through to the absorber layer. As will be discussed in the next chapter, the quantum efficiency (QE) at each wavelength is the ratio of electrons generated and collected to incoming photons. As seen in the significantly higher QE of the Cd PE device in Figure 2.3, the absorber layer typically generates more current that is subsequently collected than the CdS buffer layer. The CdS buffer layer has a band gap near 2.4 eV, which allows it to absorb photons with wavelengths less than approximately 520 nm. Figure 2.3 clearly shows that between 550 nm and 800 nm, the QE response of the two devices is almost identical. The slight difference in response at longer wavelengths

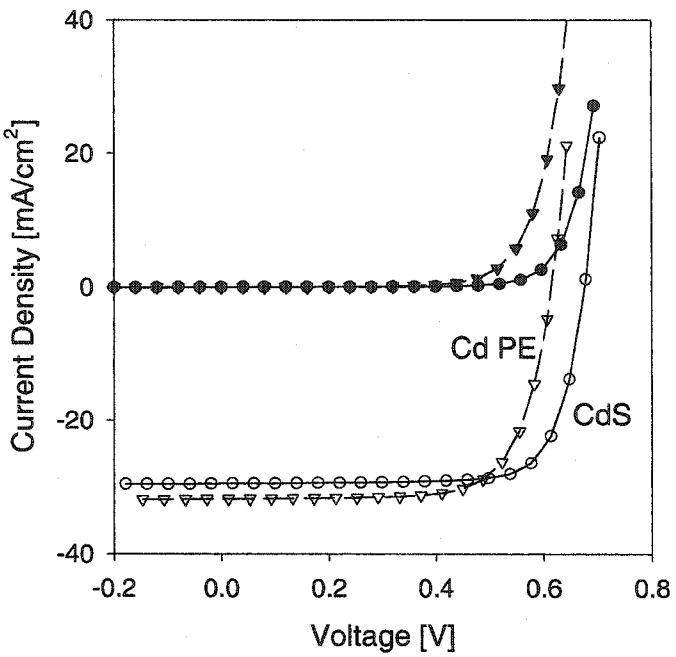

Figure 2.2. Current density vs. voltage curves for Cd PE treated devices and devices with a CdS buffer layer. Measurements taken in the dark: filled symbols. Measurements taken under standard illumination: open symbols. All absorbers were fabricated using evaporation.

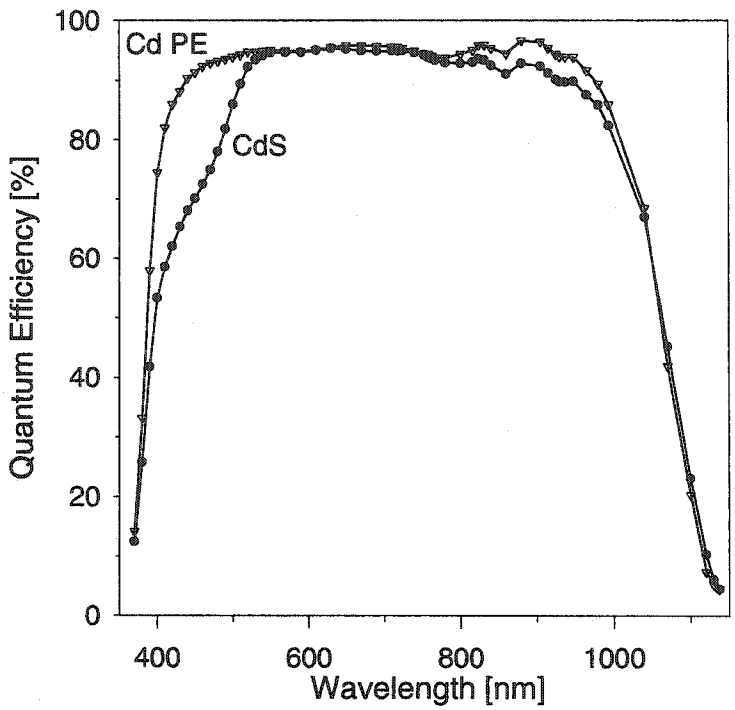

Figure 2.3. Quantum efficiency (corrected for reflection) of a Cd PE treated device and a device with a CdS buffer layer.

has yet to be explained satisfactorily. The devices shown in this figure were also made from evaporated absorbers.

Chapter 3

Experimental and Data Analysis Techniques

The goal of the majority of the thin-film polycrystalline photovoltaic community world wide is to produce economical solar cells with efficiencies approaching their theoretical maxima. To this end, the CSU Photovoltaic Laboratory measures primarily CIGS and CdTe solar cells produced at laboratories both in the U.S. and abroad. These measurements are focused primarily on gaining information regarding the performance of the solar cell and how it can be improved. Specifically, the lab focuses on mechanisms of current loss and possible causes of unrealized voltage potential. In addition to measurements which help pinpoint current loss and voltage/band-gap discrepancies such as current density - voltage (JV) and quantum efficiency (QE), temperature and frequency-dependent capacitance measurements were made in order to examine the electronic structure of the material. Some of the capacitance measurements were made at the University of Oregon in collaboration with colleagues there. This chapter details the majority of the measurements made for this work and the techniques used to analyze the data acquired from these measurements.

Several different measurements made in the CSU Photovoltaic Lab use the same mechanical equipment for mounting and contacting the test solar cells. Typical size of a laboratory-size CIGS solar cell is on the order of 0.4 cm^2. Typical sizes of a substrate containing multiple solar cells range from 1"x 1"to 1"x 2". With significant labor and design input from our engineering and shop staff, a new "light box" measurement station was designed and built under my supervision to improve throughput and integrity of measured cells. A photograph of the light box is shown in Figure 3.1. The light box was designed

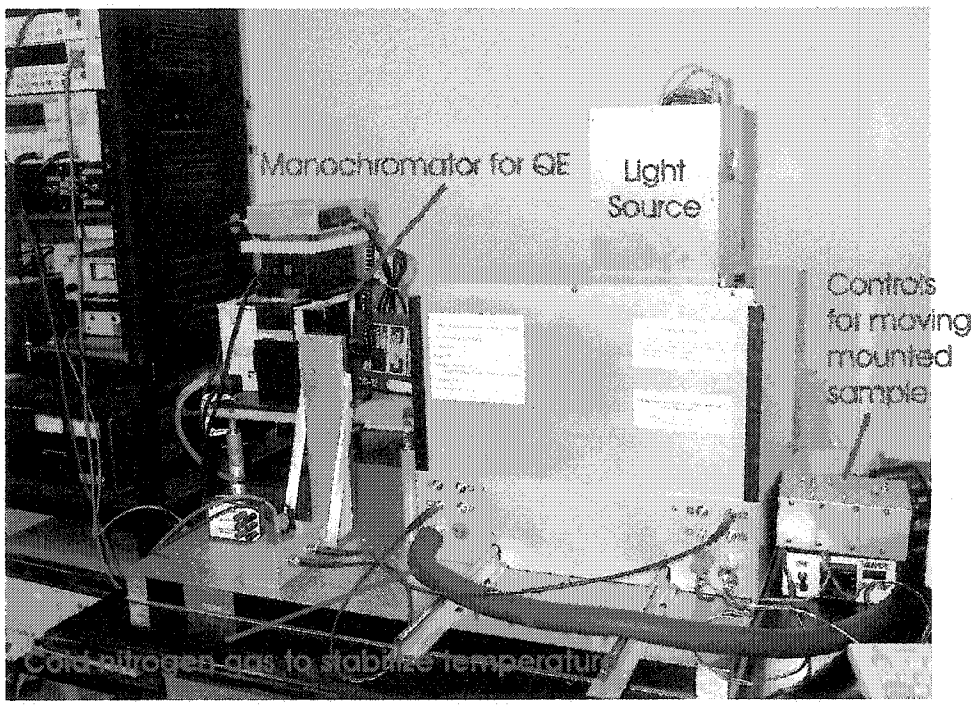

Figure 3.1. Light box measurement apparatus showing the light tower (top right), friction-less rails (middle front) and associated equipment.

to provide an environment isolated almost completely from ambient light, in addition to providing exposure to simulated sunlight or to single-wavelength light, as required by the desired measurement. The light box was also designed to facilitate making and maintaining the delicate yet robust electrical connections required to measure the test cells. To do this, we designed and built an independent "mounting plate" used to mount and contact the test cells.

This mounting plate is inserted into the light box using a low friction rail system designed to minimize mechanical disruption to the cell attached to the mounting plate. It was also designed to minimize total contacting time of test cells, as a cell can remain contacted while being switched in and out of measurement positions, as is required by our current calibration techniques for current-voltage and quantum efficiency measurements. A photograph of a cell mounted on the mounting plate as the mounting plate is being slid into measurement position is shown in Figure 3.2. The design requirements for the mounting plate included the ability to (1) simultaneously contact (electrically) multiple cells on a substrate (2) transfer contacted cells from various experimental stations to the light box and vice versa (3) mount and measure both superstrate- and substrate-based solar cells (4) accurately and efficiently control the temperature of the contacted solar cells (5) provide complete optical access to all test cells on a substrate and (6) mount and contact cells and substrates of somewhat varied geometries and sizes. These design requirements were met except for the accuracy of cooling the cells. To cool the cells, temperature-controlled nitrogen gas flows over the substrate. A cooling box (shown in Figure 3.3) was designed to attach to the mounting plate to contain the cool gas. This cooling box provides as small a thermal mass as practical under the cost and functionality constraints of

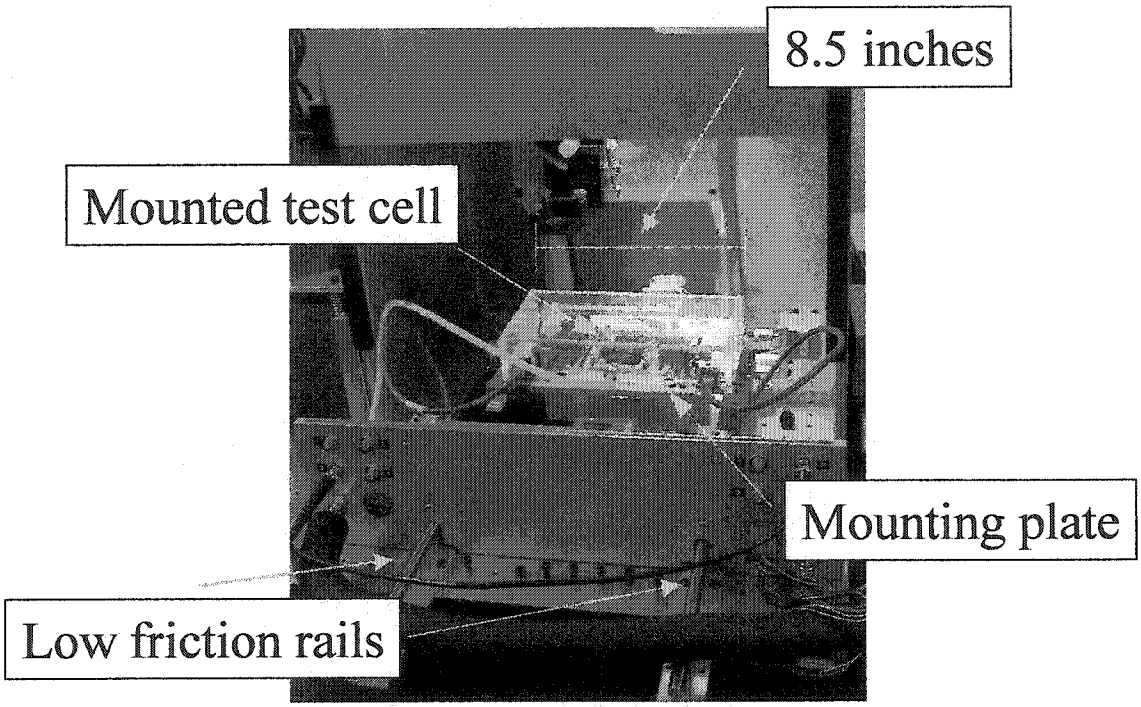

Figure 3.2. Light box as a mounted cell is slid into measurement position using low friction rails.

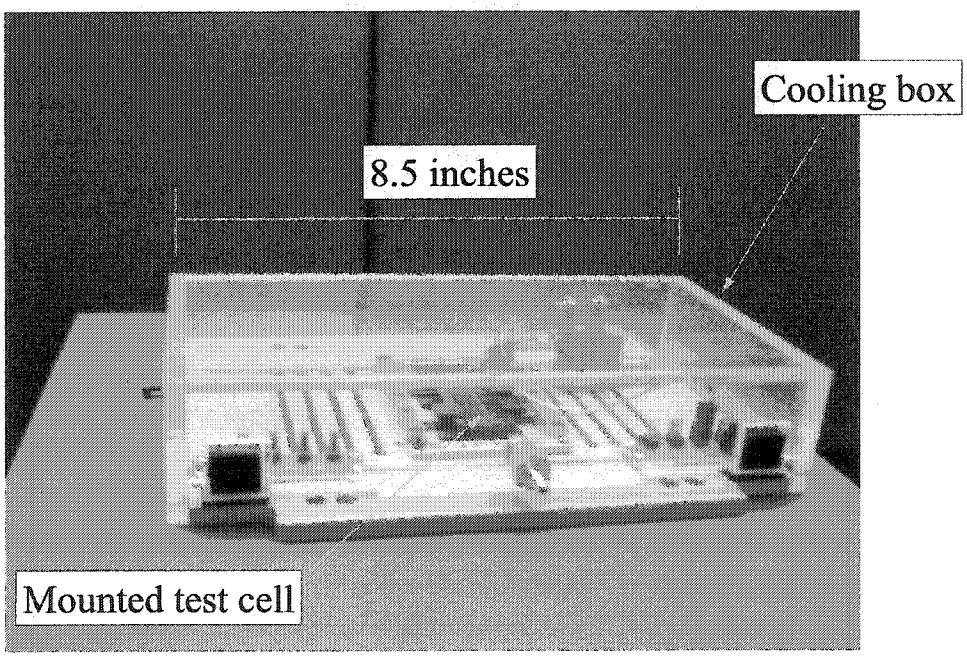

Figure 3.3. Cooling box covering cell mounted on mounting plate and contacted on the n-side of the junction.

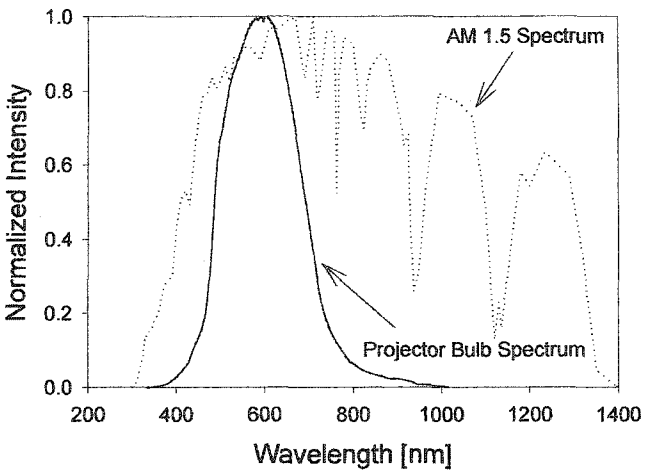

Figure 3.4. Normalized spectral intensity of projection bulbs used for JV measurements (solid line) and sunlight as received at earth's surface (AM 1.5 Spectrum).

the project. However, we have experimentally determined that there may be temperature gradients as large as 2 degrees Celsius within a distance of 4 cells side by side. These gradients are larger than desirable, but do not materially affect any of the results reported in Chapter 4.

3.1 Current-Voltage Measurements

3.1.1 Measurement Equipment

Dark and light current-voltage (JV) measurements required the light box and coordinating mounting plate, as well as sunlight simulated by 3 quartz projection bulbs for the light JV measurements. The relative spectra of the projection bulbs and sunlight as received near the earth's surface (AM 1.5) is shown in Figure 3.4. As detailed in the figure, the two spectra are similar in the region of interest, but not identical. (Recall that CIGS solar cells can only convert light up to approximately 1200 nm in wavelength into electrical

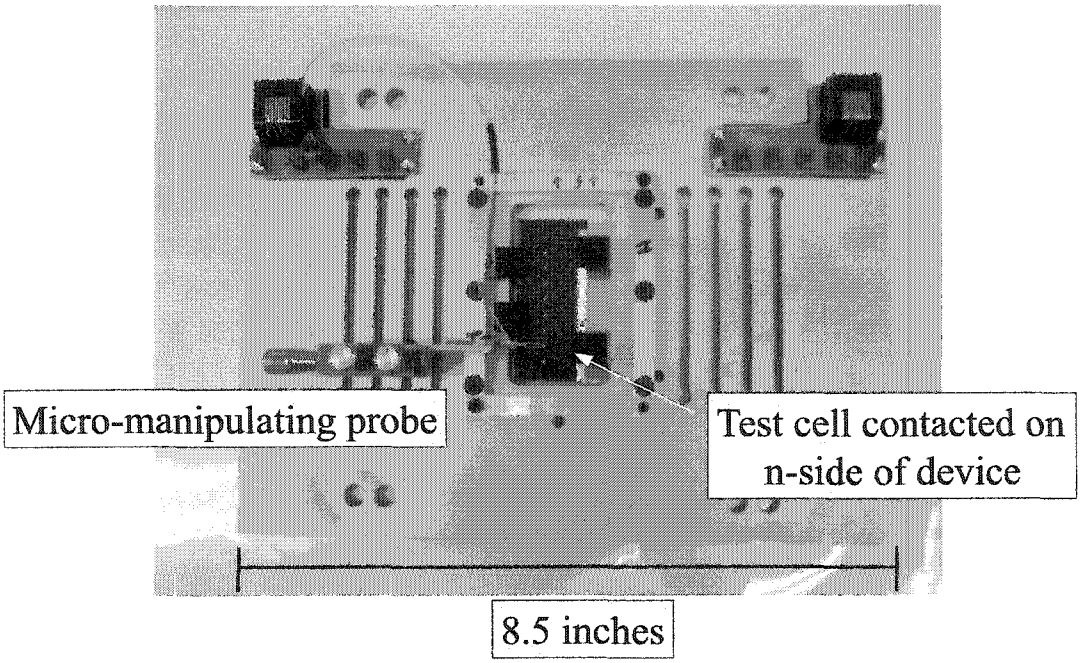

Figure 3.5. CIGS cell mounted on mounting plate with micro-manipulating double-tipped probe contacting the n-side of the device through the Al/Ni grid on the top of the cell. There are nine solar cells on the substrate shown.

current.) Due to these differences, post-measurement corrections have been made to the calibration of several measured solar cells. The details are included in the presentation of cell data.

3.1.2 Measurement Circuit

JV measurements were taken using the four-point technique, to essentially eliminate any circuit resistance from masking the true values of the measured current. The 4-point technique entails two points of contact through to the p-side of the device (current and voltage) and two points of contact through to the n-side of the device (current and voltage). Two contacts are made through each micro-manipulating probe, shown in Figure 3.5 hooked up to the n-side of the device, also designed and built with significant assistance from the engineering and shop staff as a portion of this thesis work. From these

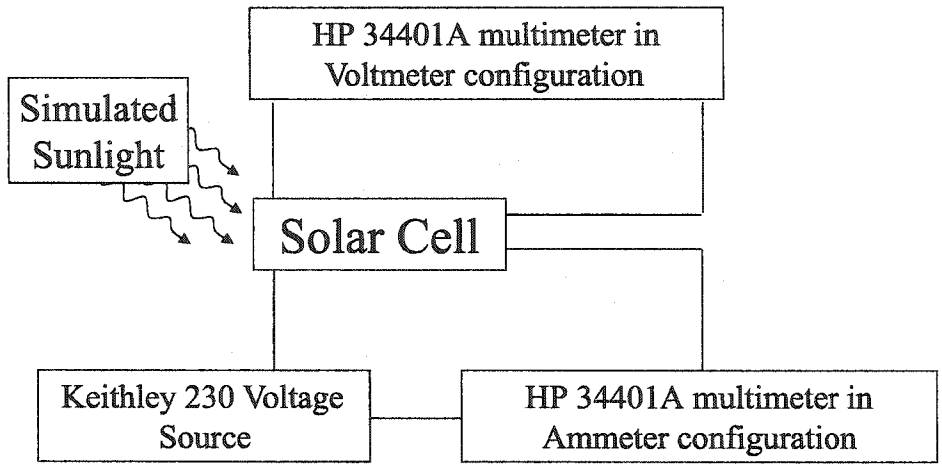

Figure 3.6. Schematic diagram of JV measurement circuit.

contacts, one circuit is completed by connecting to a Hewlett Packard 34401A Multimeter in a voltmeter configuration, and another circuit is completed by connecting to a Keithley 230 Programmable Voltage Source and subsequently to another Hewlett Packard 34401A Multimeter in an ammeter configuration, as shown in the circuit diagram in Figure 3.6 . Voltage is typically applied starting at -0.5 V and stepped in 0.05 V intervals to approximately 0.1 V above the estimated open-circuit voltage (V_{OC}). This voltage range allows one to extract the short-circuit current density, the maximum power point current density and voltage (J_{MP} and V_{MP}, respectively), and the open-circuit voltage. A slightly more limited voltage range is shown in Figure 3.7.

3.1.3 Analysis Techniques

3.1.3.1 Results from the Linear Plot

From the aforementioned parameters, the basic indicators of device performance can be calculated in a straight-forward manner. As mentioned previously, the aim of photovoltaic programs world-wide is to improve the power conversion efficiency (η) of stable

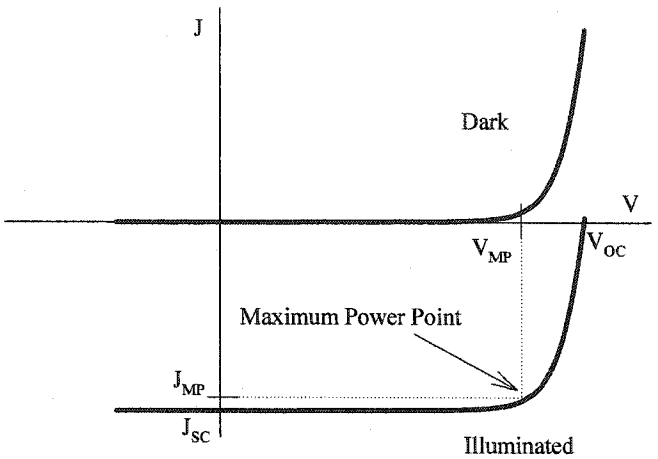

Figure 3.7. Example of illuminated (light) and dark JV measurement results with key parameters emphasized.

solar cells. The efficiency is the ratio of the power density output by the device at its maximum power point (also shown in Figure 3.7) to the power density of the incident light, and is expressed mathematically as $\eta = \frac{J_{MP}V_{MP}}{P_{In}}$. Although efficiency ($\eta$), tells us the performance level of the device, it tells us relatively little about how to improve the device. Thus, we turn to other parameters to learn more about the devices under test. One of these device performance indicators that can be extracted directly from the linear plot in addition to V_{OC}, J_{SC}, J_{MP} and V_{MP}, is the fill factor (FF), which is defined as $FF = \frac{J_{MP}V_{MP}}{J_{SC}V_{OC}}$. As can be seen by the dashed lines in Figure 3.7, the fill factor is essentially a measure of how square the diode curve is in forward bias. When current and voltage have been maximized for a particular device configuration, the FF is a comprehensive performance and diode quality indicator. A low FF is typically indicative of less than ideal values of resistances in the solar cell, or of the quality of the diode. Evaluation of the resistance values and diode quality is discussed in the next section.

3.1.3.2 Derived Parameters

The shunt resistance (r_{shunt}), the inverse of which indicates how much current is leaking through the diode and not contributing to power production, can be derived directly from the linear plot. Determining the inverse of the slope of the linear JV plot in reverse bias gives a good estimate of r_{shunt}. Although the value of the inverse slope may be low (hence, high conductivity) in a plot such as shown in Figure 3.8, that is not always indicative of a low shunt resistance, as some devices have shown signs of photoconductivity. The two phenomena can often be separated by comparing light and dark JV curves for the same device. The slope in the dark JV curve should be solely due to shunt resistance, with any

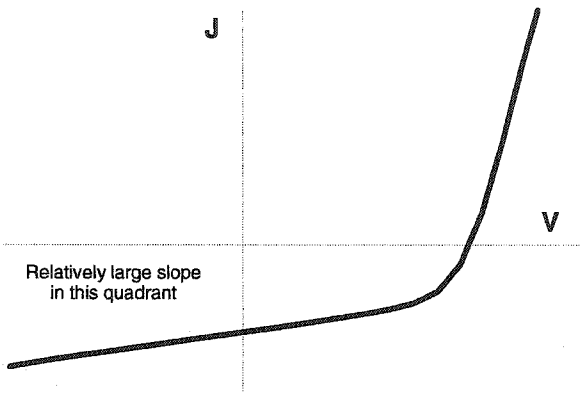

Figure 3.8. Linear JV plot with relatively large slope in reverse bias. This is indicative of a low resistance to shunting.

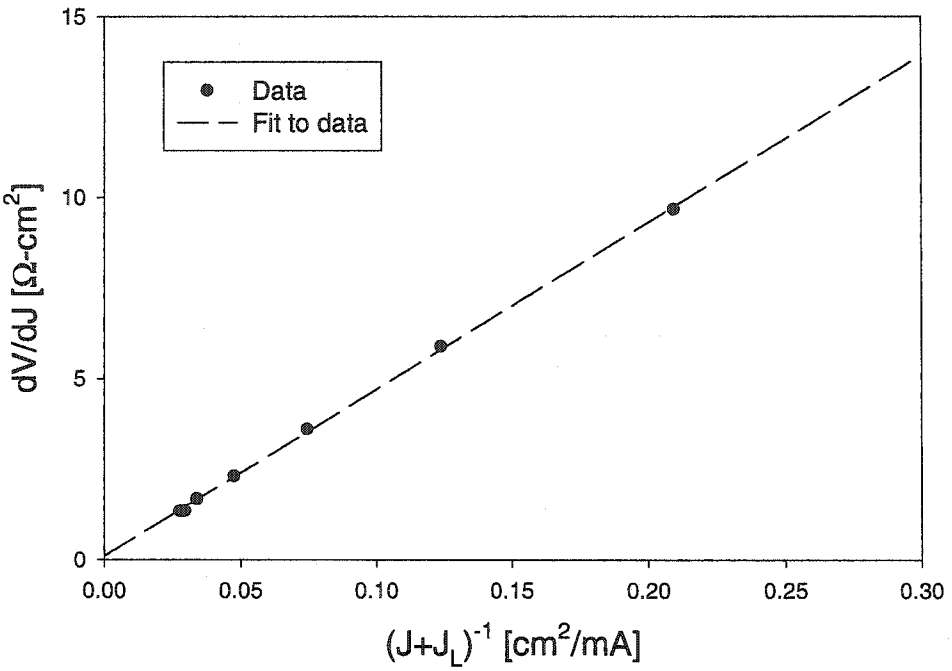

Figure 3.9. Differential plot to separate R_{SERIES} and A, after Sites and Mauk [40].

additional slope in the light JV curve most likely being a result of photoconductivity in one or more of the device layers.

Replotting the data in a semi-log plot with axes dV/dJ vs. $(J + J_L)^{-1}$, as shown in Figure 3.9, allows us to deduce the diode quality factor, A, and the series resistance, R_{SERIES}, of the device. The diode quality factor is proportional to the slope of the plot, V_o, and the series resistance is simply the intercept of the linear fit to the data. The light-induced current, J_L, is roughly equal to J_{SC}, with deviations typically resulting from significant shunting, photoconductivity, or voltage-dependent current collection. More specifically, the diode quality factor is given by $A = qV_o/kT$. Further details can be found in references [40] and [41].

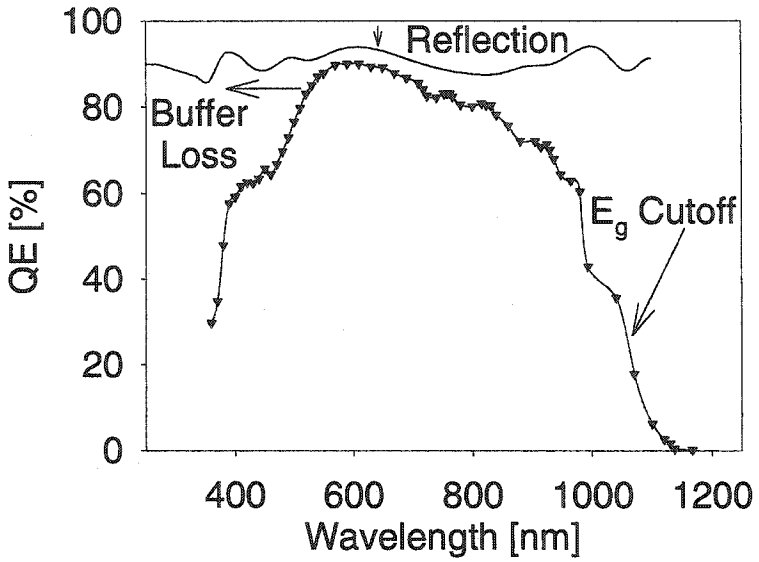

Figure 3.10. Example quantum efficiency measurement (line connecting filled triangles), highlighting window loss and band-gap (E_g) cutoff. Also shown is the reflection of the cell surface.

3.2 Quantum Efficiency

Another baseline measurement technique performed in the CSU Photovoltaic Lab is quantum efficiency (QE). Quantum efficiency is a measurement of how many electrons are excited into the conduction band per incident photon. The optimum number is 1, (i.e. 100%) but thus far it is always less than this value, as in the example shown in Figure 3.10. Some of this loss is due to the buffer and window layers through which incident light must pass in order to reach the p-n junction, as indicated in the figure. These layers and their interfaces both absorb and reflect, in addition to transmitting, incident light. The CSU Photovoltaic Lab also has the capability to measure reflection characteristics of materials as a function of wavelength. These measurements greatly enhance our ability to objectively extract information from QE measurements. Our accuracy is enhanced because we get a better idea of how much light is actually reaching the electrically active part of the cell.

Consequently, we can determine what wavelengths of light are failing to produce as much current as anticipated from the light reaching the p-n junction. Reflection measurement results are also shown in Figure 3.10.

3.2.1 Measurement Set-up

The original CSU Photovoltaic Lab QE system was completed in 1995. It was comprised of an Acton Research Monochromator Model 150, Ithaco chopper, mirror and focusing lens all attached to the frame of the original light box. After acquiring new electronic equipment several years later, the chopper was then connected to a Stanford Research System Model SR810 lock-in amplifier that received the electrical signal from the solar cell after being passed through a Stanford Research System Model SR570 current to voltage preamplifier. In the summer of 2001, I installed and aligned a new optical system mechanically isolated from the frame of the new light box as part of the new light box measurement system. The new QE system was designed to produce a spot small enough (1 mm by 3.8 mm) to fit in between grid lines slightly larger than 1 mm apart on a typical CIGS solar cell made at the National Renewable Energy Laboratory (NREL). This design constraint, as well as a pre-determined working space, called for high precision optical elements. Lenses with relatively high and constant transmission from 350 nm to 1200 nm were sought – one to collimate the beam and another to focus the beam to a relatively small spot. In addition, the aperture of the lenses needed to minimize the amount of monochromator output essentially thrown away, yet still be small enough to be focused to the 3.8 mm^2 spot. Also, the focusing lens needed to be a minimum of 5 to 6 cm away from the focused small spot. Additionally, an adjustable mirror with relatively high and constant

reflection from 350 nm to 1200 nm was required. The equipment selection and acquisition was completed in conjunction with the work for this thesis.

3.2.2 Analysis

Quantum efficiency measurements are typically analyzed in a very straight-forward manner. For example, in Figure 3.10, the cutoff due to the band-gap of the absorber material (CIGS) has been noted. The band-gap is generally designated at the long wavelength edge at which the QE has dropped to below 30%. As expected, the band-gap in energy units is found from the equation $E = h\nu$. At the band-gap turn-on for CdS, at approximately 520 nm (corresponding to ~2.4 eV), the QE decreases significantly, as seen in Figure 3.10. The reason the collected current (QE) drops once the photons have enough energy to bridge the band-gap in CdS is because although electron-hole pairs are generated in the CdS, they do not contribute substantially to the photo-generated current due to substantial recombination in the CdS.

In addition to determining the band-gap of the absorber material and qualitatively examining the current loss due to CdS and other window layers, the actual amount of current generated in any given wavelength region can be calculated. Hence, current losses in any given wavelength region can be calculated as well. To calculate the amount of current collected in any given wavelength region, one simply multiplies the integrated quantum efficiency by the light spectrum in photons/(cm^2·nm), and then multiplies again by the unit electronic charge [41]. This calculation will yield the collected current density in the wavelength region of interest.

3.3 Room-temperature Capacitance-Voltage

3.3.1 Measurement Set-up and Preparation

The light box and associated mounting plate are also used to mount cells for making room-temperature capacitance-voltage (CV) measurements. The solar cell is connected to an HP 4192A LF Impedance Analyzer, and can be electronically switched to a Hewlett Packard 34401A Multimeter in a voltmeter configuration. Before a CV measurement is made, a room temperature scan of the capacitance vs. frequency is taken using the same experimental set-up in order to determine a suitable probe frequency for the CV measurement. This and all capacitance measurements are actually measured as the impedance, i.e. the inverse of the admittance, $A = G + iC\omega$, where G is the conductance, C is the capacitance, and ω is the measurement frequency in radians. The typical frequency range swept is from 1 kHz - 1000 kHz. While the equipment is capable of a broader sweep, in most cases the cell leakage and experimental configuration used does not yield a clean signal outside this range. A suitable frequency for a room temperature CV measurement can be found by measuring the capacitance as a function of frequency (CF) at several different bias values spanning the anticipated voltage range of the CV measurement. A suitable frequency is found by eliminating frequency regions of significant slope in a CF plot and regions where the qualitative behavior of the CF for one bias varies dramatically from the qualitative behavior at other biases. In addition, for a frequency to be suitable, the real (conductive) portion of the signal cannot dominate the imaginary (capacitive) portion. The practical limit is a phase angle of 20° from the real axis.

Within the given frequency range, assuming that the capacitor is in parallel with any resistor characteristics is the most accurate way to measure a solar cell with the aforementioned equipment. The modulation voltage used is 20 mV. Typical room-temperature capacitance values for CIGS cells with a surface area ~0.5 cm^2 are the order of 10 nF.

3.3.2 Standard Analysis

Several parameters can be derived or estimated from the results of the CV measurement. The first parameter of the material is the built-in voltage, or V_{bi}. V_{bi} is essentially the difference in potential of the intrinsic Fermi level (E_i) between the n and p-type material. See, for example, p. 156 of reference [9]. If we assume a step junction, mathematically, this can be expressed as

$$A^2/C^2 = \frac{2}{q\epsilon N}(V_{bi} - V), \tag{3.1}$$

after [9], where A is the area of the solar cell, C is the measured capacitance, ϵ is the dielectric constant of the more lightly doped material (here CIGS), N is the carrier density in the more lightly doped side of the junction, and V is the applied voltage. Hence, plotting A^2/C^2 vs. V , as shown in Figure 3.11, allows us to extrapolate the built-in voltage by determining the likely x-intercept.

In addition to the built-in voltage, any capacitance measurement at zero bias can yield an estimate of the depletion width by treating the p-n junction as a parallel-plate capacitor. Thus, we begin with $C = \epsilon A/d$, where C is again the measured capacitance, ϵ the dielectric constant of the material between the plates, A the area of the plates, and d the distance between the plates. For a p-n junction A becomes the area of the solar cell surface and d, or more commonly W, the depletion width. Hence, rearranging variables we find

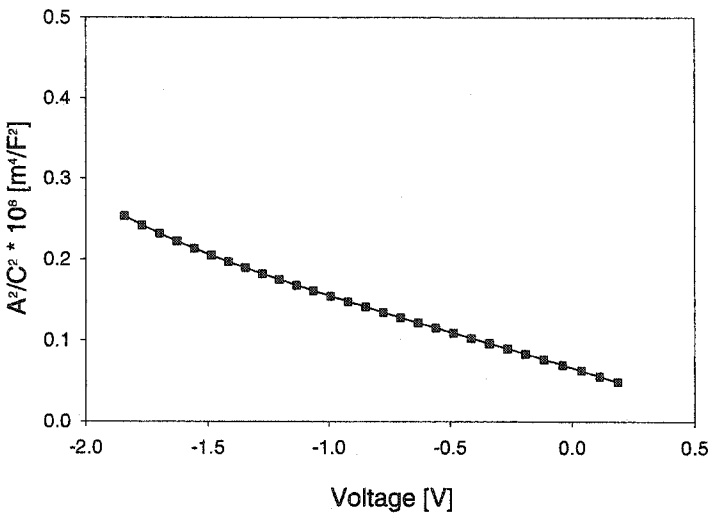

Figure 3.11. Results of a CV measurement plotted to easily extract V_{bi}.

$$W = \frac{\epsilon A}{C}. \tag{3.2}$$

Note that this expression can be used at a non-zero bias, as well. In such an instance, then W is no longer the depletion width at thermodynamic equilibrium, but rather the effective depletion width.

Another useful result from analyzing CV measurements is an estimate of the carrier concentration in the more lightly doped side of the junction. Again, in this case that is the p-type material. This approximation (after [9]) does not require a step junction, however, the depletion approximation is indeed used, rendering approximations made from an applied forward bias when current begins to flow invalid. The small signal capacitance per unit area is

$$\frac{C}{A} = \frac{dQ}{dV}, \tag{3.3}$$

where dQ commonly denotes the incremental increase in charge per unit area, rather than charge, when an incremental change in voltage, dV, is applied. Note, many authors do not use C to indicate capacitance, but instead use C to indicate capacitance per unit area. If we assume that the extra charge due to the extra applied voltage appears in the depletion region, then we can define $dQ = qN(W)dW$,where $N(W)$ is the carrier density as a function of the effective depletion width. Given that the resulting change in the electric field (E), will be $dE = dQ/\epsilon$, we can then write

$$dE = \frac{qN(W)dW}{\epsilon}. \tag{3.4}$$

Recognizing that the change in applied voltage can also be approximated as $dV = WdE$, we can then use equation 3.4 and a partial integration to write

$$dV = \frac{qN(W)d(W^2)}{2\epsilon}. \tag{3.5}$$

Substituting equation 3.2, and doing some algebra leaves us with the expression for carrier concentration for the effective depletion width modulated by the applied voltage.

$$N(W) = \frac{2}{q\epsilon}\frac{dV}{d(A^2/C^2)} \tag{3.6}$$

Due to the relatively high doping of the n-type material in CIGS solar cells (frequently CdS), it is typically assumed that over 90% of the depletion region is in the CIGS. Commonly, W is treated as if it were W_{CIGS}, leading to a possible overestimate of this value by as much as 10% if the only error is due to neglecting the extent of the depletion region in the n-type material.

3.3.3 Complications Related to Defects

Since the cells used in this work have a polycrystalline structure, the ideal semiconductor equations must be used with care. Derived values for the built-in voltage, depletion width, and carrier concentration may be altered because the measured capacitance is frequently due in part to contributions from states deep in the band gap, which may or may not respond based on the frequency and temperature at which the measurement is taken. These deep states are commonly referred to as trap states, whereas the shallower states in the band gap, which are primarily responsible for current flow and contribute to the capacitance independent of the temperature or frequency of the measurement, are labeled acceptor states or dopants. Since the deep states are not always charged, they may not contribute to the space-charge at thermal equilibrium. Hence, when they do contribute to the capacitance, they modify the derived values for built-in voltage, depletion width, and carrier concentration.

Despite that when we lack temperature-dependent data we generally do not know what portion of the capacitance results from deep states and what portion results from free carriers, room-temperature measurements should not be discounted entirely. In some very thin cells, the total film thickness derived from CV is comparable to the assumed physical thickness, within potential thickness variations of the film. In this situation, the free carrier response is likely dominating the deep state response, and derived values of carrier concentration, built-in voltage and depletion width are assumed to be reasonably accurate. Also, although room temperature CV results do not delineate free carriers from responding deep states, they can give a picture of overall majority carrier response (free and trapped) which may be helpful in initial assessment of differences in cells made by nominally the same technique, but with slight variations in deposition or post-deposition treatment. This overall response, $N(W)$ from equation 3.6, will be referred to in subsequent chapters as the apparent carrier concentration. In addition, the equations derived in this section can all be applied to temperature-dependent CV measurements. This will prove to be illuminating in the following chapter.

A new method for separating the deep state response from the carrier density in polycrystalline thin-film solar cells will be discussed in section 3.5.

3.4 Capacitance-Frequency-Temperature

3.4.1 Measurement Equipment and Mounting Technique

Initial attempts to construct a capacitance-frequency-temperature (CF-T) device in the CSU Photovoltaic Lab incorporated the portable mounting plates used with the light box.

However, excessive circuit noise prohibited the system from routinely functioning reliably. Only three samples were somewhat successfully measured using the system. As a result of the limited success of the initial CF-T systems, a cryostat with it's own mounting scheme has been acquired and may be used for future CF-T measurements at CSU. CF-T, also termed admittance spectroscopy (AS), measurements were instead made at the Materials Science Institute at the University of Oregon. The equipment in use in Oregon required an entirely different mounting technique. That technique is described in the text that follows.

Each cell was mounted on a 1 by 1 cm copper block. Consequently, the cells needed to be cut off of their substrate, and typically to a smaller size. The cutting was done using a small diamond table saw that required the substrate be adhered with soft wax to a metal block. The adhesion process required heating the metal block and wax each time a substrate was adhered or removed from the block. While the hot plate used to heat the block was kept above 300 °F, due to the very short contact time with the substrate while on the hot plate, it is believed that minimal, if any, alterations to the cell occurred. In addition, coolant was required to operate the saw. The coolant occasionally spread from the blade to the cell. However, it is unlikely reported measurement results were affected by the spreading coolant, as liquid on test cells tends to induce shunting and any cells with significant shunting can be readily identified and have not been included in the results section.

To complete the copper block mounting, a silver epoxy was applied to the copper block, substrate and portions of the purposefully exposed molybdenum. The epoxy was cured at 80 °C for approximately 2.5 hours. Since we have witnessed slight degradation of some completed cells at these times and temperatures, similar cells were performance

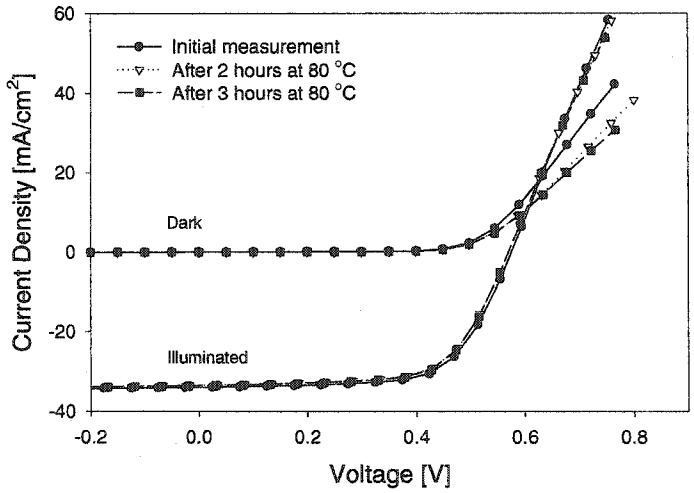

Figure 3.12. Illuminated and dark JV measurement results before, after 2 hours, and after 3 hours of 80 ^oC heat exposure in the dark.

tested before, during, and after being exposed to the heat for 3 hours. The results are shown in Figure 3.12. It is apparent that slight changes did occur in the series resistance of the devices, as seen in the dark measurements in Figure 3.12. It is not known if these changes were temporary or permanent. These resistive changes resulted in smaller voltage differences from initial to post-annealed conditions than the voltage differences among samples made from different semiconductor deposition processes.

Cells mounted with their p-side contacted to the copper blocks were then contacted on the n-side at the University of Oregon using a single wire placed on the grid on the top of the sample. The wire was attached to the rod support system to which the copper block was also connected. The rod support system also included thermocouple wire and a thermocouple, as well as a two BNC cables. The inner conductors were connected to the n- and p-sides of the sample. One BNC is then connected to an adder circuit which adds any desired bias signal to the probe signal output by an SRS 850 lock-in amplifier. The other BNC is then connected to an SRS 570 current to voltage preamplifier. The circuit is

completed by connecting the SRS 570 to the input of the SRS 850. One relatively small (few mV) ac voltage is then swept through a broad frequency range, typically 200 Hz to 70 kHz at each selected measurement temperature. By monitoring the ratio of the capacitance to the conductance signal received by the 850 during calibration and device measurement, one is able to ensure the adequacy of the separation of the two signals. Heating and cooling of the sample was accomplished by flowing temperature-controlled nitrogen gas across the small sample chamber isolated from the ambient by an evacuated glass tube.

3.4.2 Analysis

Although there are multiple methods for extracting the density of trapping states using AS, including the method of Walter [42], these methods often require a priori knowledge of device parameters that are not well-known for CIGS devices. A method yielding rough estimates, yet requiring only one parameter be estimated, will be used to extract the trap state density in all devices under study. However, the results will not be given as much weight as the extraction of trap state densities from a different measurement technique, discussed in the following section, which requires less a priori knowledge about the device to estimate the density of trapping states. The AS data, as explained below, will mainly be used to estimate activation energies (E_a) and temperature-adjusted thermal emission prefactors (ξ_o) pertaining to such states.

To estimate the trap state density from AS data such as that shown in Figure 3.13, one looks for an isotherm that appears to have both a low- and high-frequency value of capacitance that is saturated. For the data shown in Figure 3.13, the middle 3 isotherms would all be feasible choices. Then, by solving 3.1 for the apparent carrier density (N) for both the high- and low-frequency limits of the measured capacitance, and taking the

difference, one can estimate N_t, the trap state density.

$$N_t = N_{lf} - N_{hf} = \frac{2V_{bi}}{A^2 q\epsilon}\left(C_{lf}^2 - C_{hf}^2\right) \tag{3.7}$$

Here the applied voltage V, for the data in Figure 3.13 was zero, and the subscripts lf and hf refer to low frequency and high frequency values, respectively. As there are likely many different shallow dopant levels which contribute to the free carrier density, E_i, and consequently V_{bi}, are not easily determined from AS data on CIGS devices. Consequently, V_{bi} has been estimated from low temperature CV measurements where available, as described using Figure 3.11. Hence, N_t derived in this manner will not be given as much credence as N_t derived using other techniques.

The remaining AS analysis carried out in this work was to extract E_a and ξ_o from the data. To do so, one begins by identifying the inflection frequency, which we will designate as f_i, where the second derivative of $C(f)$ is zero, for a range of measurement temperatures. The solid line in Figure 3.13 connects the inflection frequencies for CF data at several measurement temperatures. A plot of temperature-scaled inflection frequency (f_i/T^2) vs. inverse temperature (Figure 3.14) can be extrapolated to zero inverse temperature to deduce ξ_o. In order to be able to do so, we begin with an expression for the hole emission rate ($1/\tau$), from a trap,

$$\frac{1}{\tau} = \sigma_p v_{th} N_v \exp[(E_v - E_T)/kT] \tag{3.8}$$

with σ_p the hole capture cross section, v_{th} the thermal velocity, N_v the effective density of states in the valence band, E_T the trap energy, E_v the valence band edge energy, and kT the thermal energy [9,28]. The expression $\sigma_p v_{th} N_v$ in equation 3.8, is commonly denoted by a single variable. Several different variables represent this quantity in the literature [20, 27, 42, 43], including ν, which will be used in this text. The quantity represented

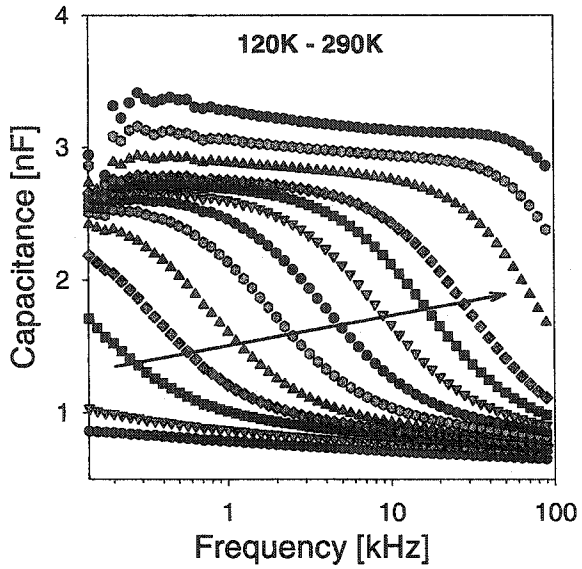

Figure 3.13. Capacitance vs. frequency at zero bias plotted for several temperatures. The solid line connects the inflection frequency for each temperature. The arrow indicates increasing measurement temperatures. The lowest three and highest four measurement temperatures are in 20 K intervals, the remaining measurement temperatures are in 10 K intervals.

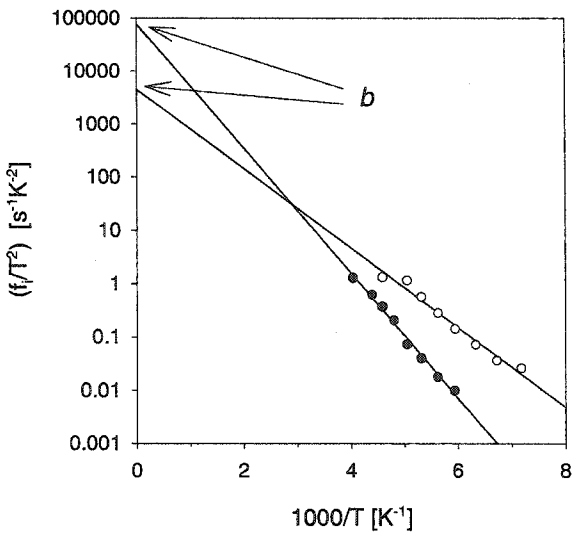

Figure 3.14. Plot of temperature-scaled inflection frequency (f_i/T^2) vs. inverse temperature (circles) and extrapolation of fits to zero inverse temperature (lines). Open circles: selenized Cd PE device. Filled circles: selenized CdS device.

by ν also has several names, including attempt-to-escape frequency and thermal emission prefactor. This text will incorporate the latter. The temperature-adjusted prefactor, $\xi_o = \nu/T^2$, also goes by several names, the most straight-forward of which is used here. Thus, ξ_o is not subject to the known temperature-dependence of the thermal velocity ($\sim T^{\frac{1}{2}}$) or of the density of states ($\sim T^{\frac{3}{2}}$). Returning to the derivation of the value of ξ_o, equating the emission rate to the inflection frequency in radians [44, 45], and substituting $\sigma_p v_{th} N_v = \nu = \xi_o T^2$, equation 3.8 can be rewritten as

$$2\pi f_i = \xi_o T^2 \exp\left(\frac{E_v - E_T}{kT}\right). \tag{3.9}$$

After a small amount of algebra, equation 3.9, becomes

$$\ln\frac{f_i}{T^2} = \frac{E_v - E_T}{kT} + \ln\frac{\xi_o}{2\pi}. \tag{3.10}$$

Hence, it is now apparent that the y-intercept (b) of the fit to the data in Figure 3.14 is $\ln(\xi_o/2\pi)$. Thus, $\xi_o = 2\pi \exp b$. In addition, it is now apparent that the slope of the fit is proportional to the energy difference between the detected trap and the valence band edge. Consequently, the activation energy ($E_a = E_T - E_v$) of the detected traps has been estimated from Figure 3.14.

At this time it is prudent to make a few notes regarding ξ_o. First, $\xi_o = \nu/T^2$, may contain some residual temperature dependence. The hole capture cross section, σ_p, is sometimes temperature dependent [46]. Due to this and other considerations, the effective capture cross section may be 50 times larger than the true value [47]. Consequently, few authors report these values in the literature. I will also abstain from reporting σ_p values. Temperature-dependence of σ_p may be the reason ξ_o seems to be correlated to behavior fitting the Meyer-Neldel rule [10, 15, 20]. Briefly, the Meyer-Neldel rule is an empirical rule describing thermally activated processes. Second, in addition to ξ_o bearing several

names in the literature, different authors relate f_i and τ differently, which can affect the derived value of ξ_o by approximately one order of magnitude. Finally, there is significant uncertainty in these values due to a somewhat limited range of measurement temperature, thus I will not use these values as hard cell parameters. However, it is still common to use the values of ξ_o, as they are required to calculate another parameter (E_e), where the error varies with the error in $\ln \xi_o$.

In addition to providing an estimate of the activation energy of the defects, AS is also useful in that it helps delineate the region(s) in frequency-temperature space in which the defects respond. The edge of this region for any given temperature is defined as E_e, the deepest energy state at which a change in charge can occur for the time window used, which can be expressed as $E_e = kT \ln \nu\tau$ [45]. This region can then be probed to find the defect density using drive-level capacitance profiling (DLCP).

3.5 Drive-Level Capacitance Profiling

3.5.1 Measurement Technique

The mounting technique and experimental set-up for DLCP at the University of Oregon is the same set-up used for the AS measurements. However, the actual experimental technique is rather different. Whereas AS uses one ac voltage while sweeping through a broad frequency range, DLCP uses multiple ac voltage amplitudes coupled with multiple, and generally negative, dc bias levels typically at one or two selected frequencies at each of several selected temperatures. As the magnitude of the ac voltage applied is increased, the magnitude of the dc bias is increased in a complementary fashion in order to maintain the

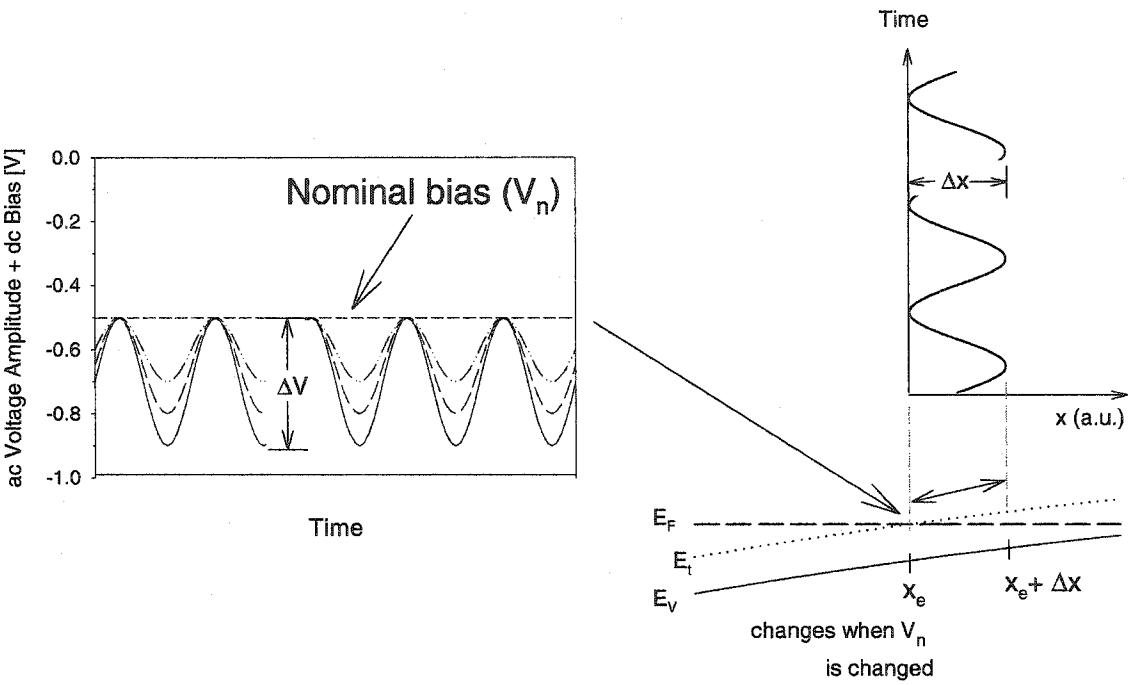

Figure 3.15. Schematic showing applied ac signal and nominal bias and how they relate to the spatial location probed for defects.

same absolute value of overall bias on the sample when the ac voltage peaks. This trade-off is shown in Figure 3.15, which illustrates the connection between the applied bias and signal and the spatial location probed by the DLCP measurement. Maintaining the same overall bias (indicated as nominal bias in Figure 3.15) keeps the value of x_e (shown in the figure and discussed below) constant [20, 48, 49].

3.5.2 Analysis

Using Poisson's Equation, one is able to find an expression for the capacitance of the semiconducting solar cell, i.e. the change in charge when a change in voltage is applied to

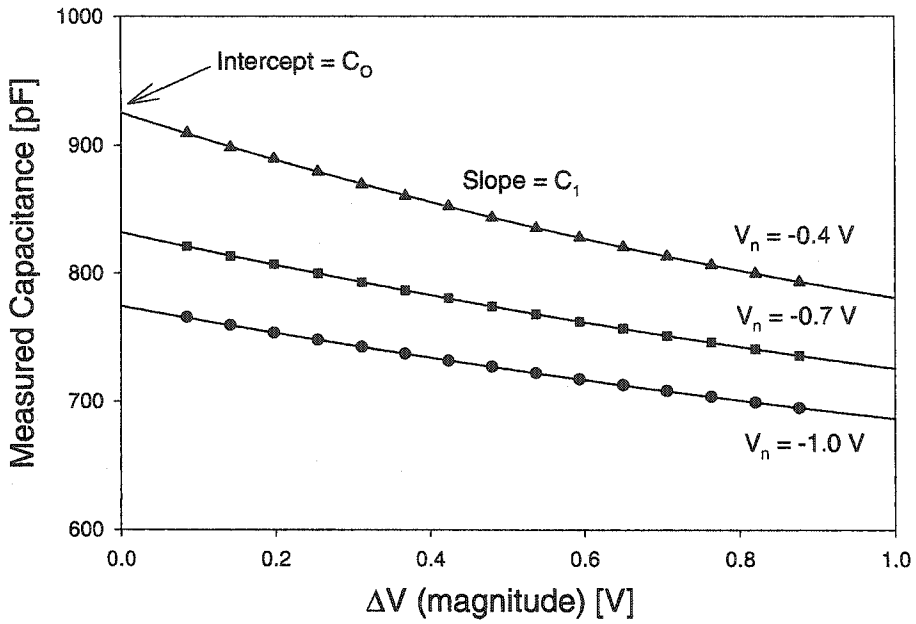

Figure 3.16. Measured capacitance as a function of the magnitude of the ac signal. These are the data points obtained directly from the DLCP measurement.

the cell

$$\frac{\Delta Q}{\Delta V} = \frac{A\rho_e\epsilon}{\epsilon F_e - \rho_e x_e} - \frac{A\rho_e^2\epsilon^2}{2(\epsilon F_e - \rho_e x_e)^3}\Delta V + \ldots , \tag{3.11}$$

for an n^+p device where A is the area of the solar cell surface, ρ_e is the change in charge density due to the application of ΔV, and F_e is the magnitude of the electric field at x_e, the position at which $E_F - E_v = E_e$ [20,48]. Equation 3.11 can also be written to explicitly show the role of the alternating voltage

$$\frac{\Delta Q}{\Delta V} = C_o + C_1\Delta V + \ldots . \tag{3.12}$$

Consequently, the capacitance data which has been gathered as a function of the alternating voltage, can be fit to this equation as shown in Figure 3.16 for data taken at 3 different values of nominal bias (V_n). The y-intercept in Figure 3.16 yields C_o, while C_1 is proportional to the slope of the plots. Although the plot does show higher order terms at larger ΔV, C_o and C_1 can be determined with good precision.

Incorporating the fitting equation (3.12) into the derived capacitance (3.11) yields

$$C_o = \frac{A\rho_e\epsilon}{\epsilon F_e - \rho_e x_e} \text{ and } C_1 = -\frac{A\rho_e^2\epsilon^2}{2(\epsilon F_e - \rho_e x_e)^3}. \tag{3.13}$$

Recognizing that the density of responding states is simply the change in charge density divided by the unit charge provides an expression for the measured response of states as a function of the fitting parameters C_o and C_1 in equation 3.13,

$$N_{DL} = \frac{\rho_e}{q} = -\frac{C_o^3}{2q\epsilon A^2 C_1}, \tag{3.14}$$

where $N_{DL} = p + \int g(E)dE$, with p the free carrier density and $g(E)$ the density of states within the band gap responding to the applied signal [20]. Thus, for devices where the N_{DL} signal can be saturated (both for a maximum and minimum value); one can find $N_{DLmax} - N_{DLmin}$, the density of defect states in the frequency and temperature space probed. Here N_{DLmin} is the signal when there are no extraneous states responding, and consequently $N_{DLmin} = p$ of the absorber for the temperatures at which N_{DLmin} is saturated. Consequently, when both the maximum and minimum responses are saturated, it is possible to calculate the average trap (deep state) density as well as the average free carrier density for the temperatures spanned by the saturation limits.

3.6 Overview of Capabilities of Capacitance Techniques

Since further chapters will compare results from all of the capacitance techniques used, it is important to understand the differences in these techniques and where they can detect states in the band gap. Admittance spectroscopy is sensitive to and will detect all states whose energy level crosses the Fermi level during the time allowed by the frequency of the probe signal. Capacitance vs. voltage is also sensitive to all states whose energy level crosses the Fermi level, in addition to states on the edge of the space-charge region that

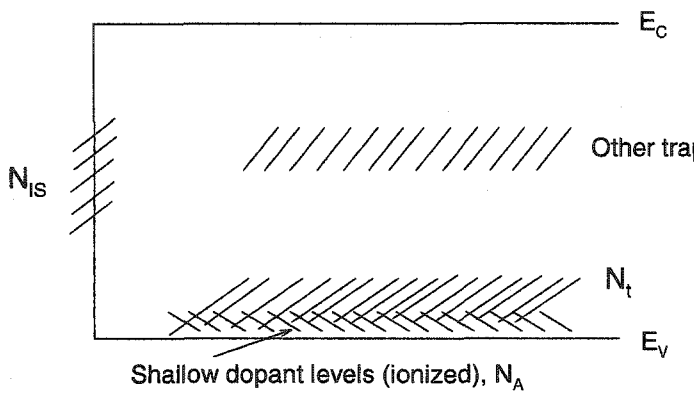

Figure 3.17. Schematic drawing of general location of states within the band gap. N_{IS} is the density of near-interface states. N_t is the density of other trapping states which can be detected using capacitance tecniques.

are exposed due to the applied DC voltage. In contrast, drive-level capacitance profiling (DLCP) will only detect states at the crossing point of the Fermi level and the trapping state (x_e) and further away from the p-n junction. These differences will serve to be fairly illuminating in the subsequent chapter.

Through a combination of these three techniques, one can detect several different types of states within the band gap. The two main types of states discussed in the following chapter are near-interface states, whose density is designated N_{IS}, and trapping states in general, whose density is designated N_t. The schematic drawing shown in Figure 3.17 shows the general locations of these and other reference states within the band gap. Again, Figure 3.17 is a schematic, in reality the conduction and valence bands bend and the states shown should track the bands.

Making a connection between the levels shown in Figure 3.17 and the aforementioned measurement techniques will also enhance the clarity of the following chapters. To serve that purpose, the following table completes this chapter by categorizing capacitance mea-

surement techniques by the states within the band gap which contribute to the measured quantities, and the state densities which can be extracted from the measured quantities.

Technique	Contributing Band-gap States	Extracted Densities	Additional Techniques Required
AS	N_{IS}, N_t,N_A: for $x < x_p$*	N_t estimate**	—
CV-T	N_{IS}, N_t, N_A	N_{IS}	DLCP
DLCP	N_t, N_A: for $x > x_e$	N_t, p	—
*x_p is the location of the edge of the depletion region in the p-type material			
**may include some near-interface states if E_a of N_t and N_{IS} overlap			

Chapter 4

Experimental Results and Discussion

Before embarking on reporting the experimental results central to this thesis, some editorial comments should be made. These are complex devices. As mentioned in Chapter 3, much of the theory on which analysis of polycrystalline thin-film solar cells is based is ideal diode theory and the theory of abrupt p-n junctions. While many of the CIGS(S) devices studied world-wide approximate some of these ideal situations, many do not. Thus, some of the inferences made by interpreting somewhat poor-performing devices may be questionable. Although weaker-performing devices often need the most analysis as they need the most improvement, we can more accurately analyze the better-performing devices. Since the devices chosen for discussion in this thesis represent two exemplary groups of devices – those made from the best laboratory material and those made from the best commercially available material, one might assume that the analysis would be relatively straight-forward. This is still not the case. As illustrated in Figure 1.3, these devices have many grain boundaries between the small crystallites, whose exact effect on carrier transport is not known. Also, due to the thin layers comprising these devices, physical characterization of exactly how thick, of what composition, and of what semiconductor type these layers are, is not conclusive in the region where it may matter the most – the interface of the p-n junction. Thus, if it appears that the conclusions reached from the data presented are conservative, it is because these devices stretch the applicability of standard semiconductor-physics theory.

As discussed in Chapter 2, the devices analyzed in this text fall into one of four categories, as shown in Figure 4.1. The symbols shown in the matrix will be used to indicate

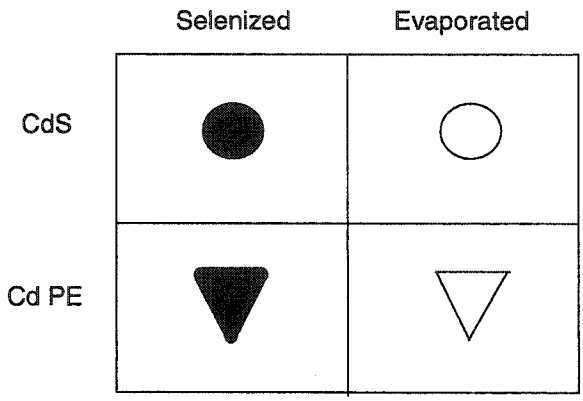

Figure 4.1. Matrix displaying the four varieties of CIGS solar cells that are the focus of this work.

each type of device in the majority of the figures in this chapter.

4.1 Current-Voltage Characterization Results

4.1.1 Open-circuit Voltage

Although power-conversion efficiency is the progress benchmark discussed most frequently, researchers must focus on improving one parameter of the cell at a time, while not sacrificing others. When dealing with relatively good-quality solar cells such as the ones discussed in this work, an improvement in V_{OC} (independent of changing the band gap), almost always results in overall improvement of the device. Consequently, in this work, which discusses good-quality devices with relatively similar performance parameters, a larger V_{OC} will be treated as a progress benchmark.

The focal point of this work is the 8 devices whose JV curves are shown in Figure 4.2. Note most all of the devices display the behavior expected of a good-quality diode. Even the selenized CdS device with the softest exponential knee, had a fill factor near 70%. Good quality devices generally fall in the 60% - 70% range, with excellent devices having fill factors nearing 80% [6].

As mentioned in 2.5.1, all of the evaporated devices have higher values of V_{OC} than all of the selenized devices. As noted in Figure 4.2, all of the evaporated devices also have a larger band gap than the selenized devices. When the band-gap difference is taken into account as discussed in section 2.5.1, the adjusted V_{OC} increases for all of the selenized devices, but the evaporated devices still have larger values of V_{OC} than the adjusted values of their selenized counterparts. Note the order in which the V_{OC} of the devices increases,

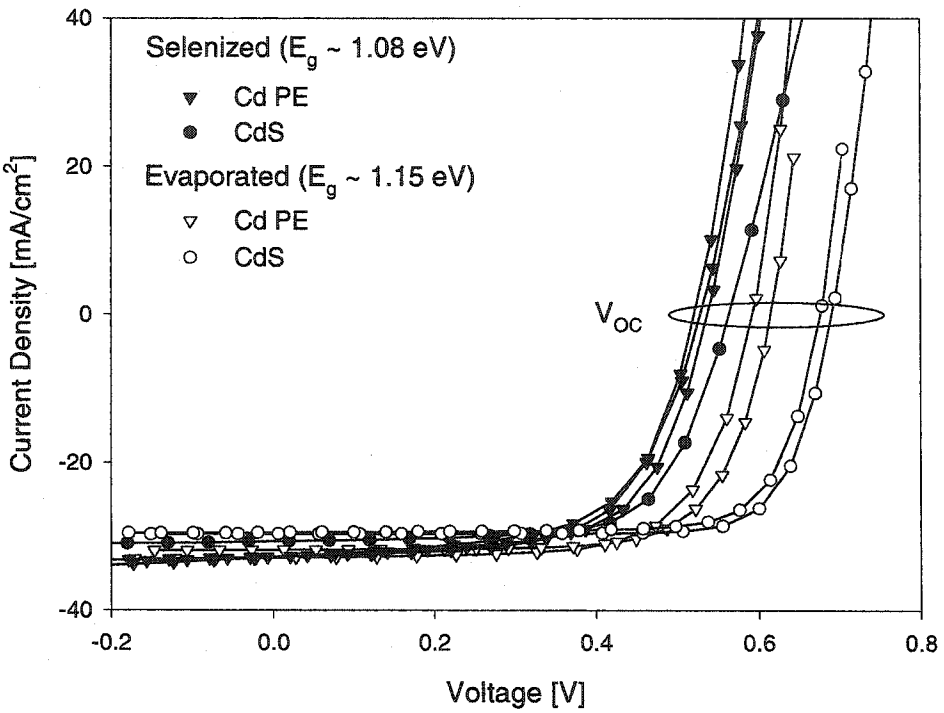

Figure 4.2. Current density vs. voltage curves for eight different devices under study. The measurements were taken at 25 °C under standard illumination.

from the selenized Cd PE to the devices with the largest V_{OC}, the evaporated CdS devices. When comparing good-quality devices, there is commonly a trade-off between V_{OC} and J_{SC}, as predicted by theory [50]. Indeed, the magnitude of J_{SC} increases in very nearly the opposite order of the V_{OC} increase, with the exception of the evaporated Cd PE devices. Although likely unrelated, these devices are also the only ones that display a noticeable cell-to-cell difference in V_{OC}.

4.1.2 Diode Quality Factor

As mentioned in the previous chapter, the diode quality factor, A, is sometimes a good indicator of the relative recombination currents in devices. Recombination currents are often cited as one reason values of V_{OC} fail to be maximized. Figure 4.3 is a semi-log plot highlighting not only the voltage difference of the devices, but also the similarities and differences of the diode quality factors for the devices. Although the actual values of A and the series resistance in the device, R_S, were calculated by plotting dV/dJ vs. $(J + J_L)^{-1}$ as described in Chapter 3, Figure 4.3 provides a better visual comparison of the relative values of A, which is inversely proportional to the slope of the plotted lines.

The evaporated CdS devices have the best (in this case the lowest), values of A, indicating once again that they likely have smaller recombination currents than the other devices. The values of A for all of the other devices were similar to each other. Due to its variation from exponential JV behavior, A was not able to be determined for one of the selenized Cd PE devices.

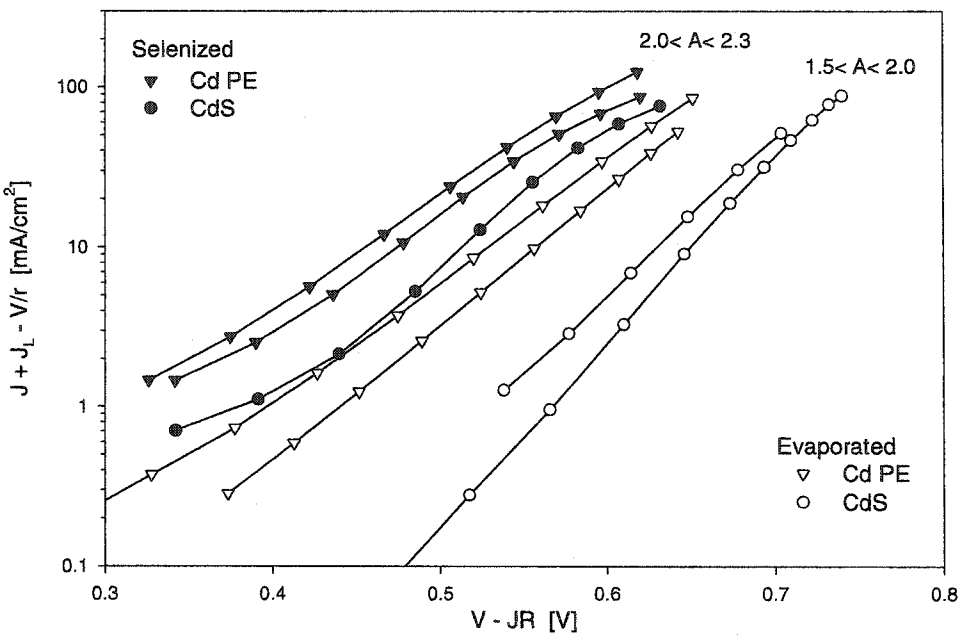

Figure 4.3. $J + J_L$, corrected for shunt resistance r, vs. V, corrected for series resistance R. The slope of each plot is inversely proportional to the diode quality factor. The JV curves in Figure 4.2 are the basis for these plots.

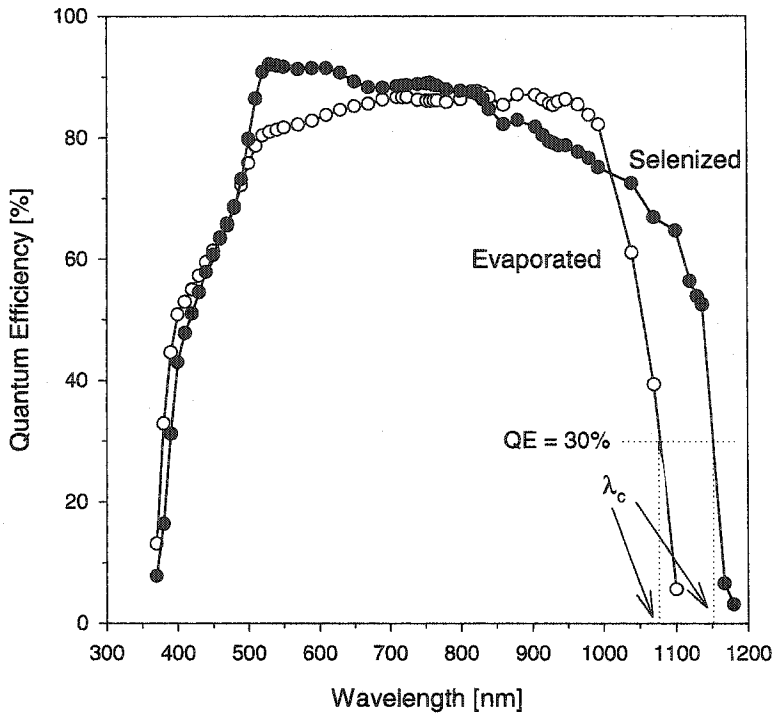

Figure 4.4. Quantum efficiency vs. wavelength for a device with a selenized absorber (filled circles) and an evaporated absorber (open circles). Both devices have a CdS buffer layer.

4.2 Quantum Efficiency Results

Figure 4.4 shows the quantum efficiency (QE) results of two of the CdS devices, one with an evaporated absorber and one with a selenized absorber. The QE of both devices has been corrected for the reflection from the top surface of the device. Recall that the CdS buffer layer can absorb photons up to approximately 520 nm in length. Since the CdS was deposited on both devices using a nominally identical process, we expect both devices to have similar CdS absorption signatures. A glance at Figure 4.4 confirms that the CdS absorption is indeed very similar among the two devices. Some of the oscillation superimposed on the general trends is due to optical interference with the thin layers.

Note the relatively flat response in the mid-wavelength range of the evaporated device (open circles). Fairly consistent collection across this relatively long wavelength range is a signature of a device with a good quality absorber and junction. The selenized device has more fall-off in the current collection from longer wavelength photons. The absorption coefficient for a semiconductor increases with the frequency of the incoming light, and hence decreases with the wavelength. Consequently, the longer wavelength light will be absorbed deeper in the semiconductor than the shorter wavelength light. Thus, the QE fall-off at longer wavelengths may be due to either a weaker electric field established by the p-n junction, or the minority carriers having a shorter diffusion length in the selenized absorber than in the evaporated absorber. Either of these are plausible reasons that photons absorbed in the bulk of the absorber will not result in the collection of an electron in the external circuit.

Figure 4.4 also indicates the wavelength cut-off at which the incoming photons begin to fail to have enough energy to excite an electron from the valence band into the conduction band. The cut-off wavelength is typically determined to be the wavelength at which the QE falls to below 30%. Using λ_c, as determined from Figure 4.4, the resultant band gap for the evaporated device shown was 1.15 eV, and it was 1.08 eV for the selenized device.

4.3 Admittance Spectroscopy

4.3.1 Defect Activation Energies

As discussed in the previous chapter, using plots such as those shown in Figure 3.13 and then Figure 3.14, one can deduce an activation energy (E_a) of the defects detected

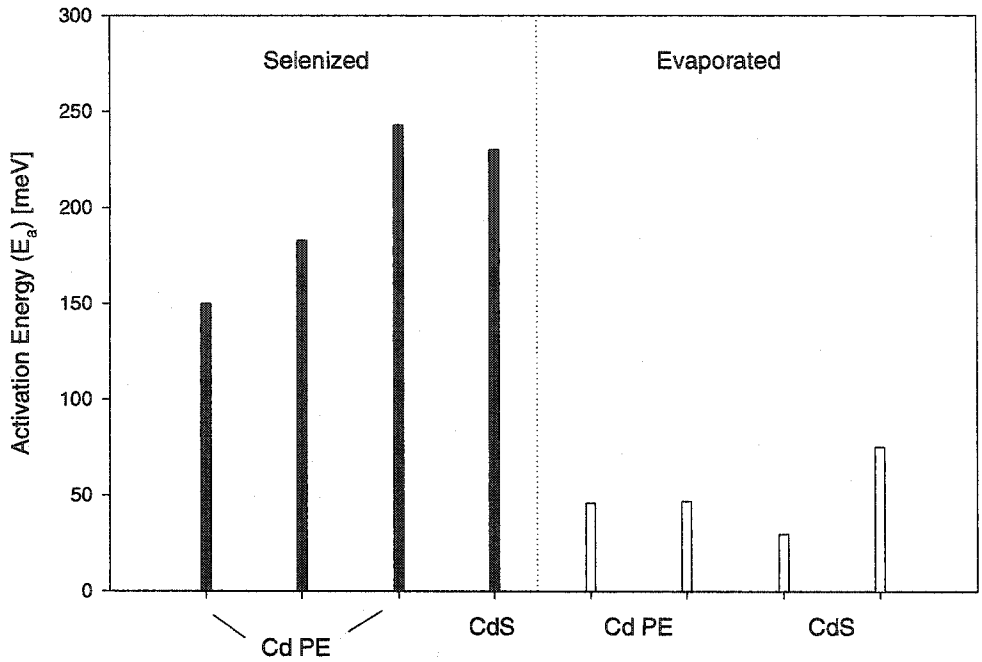

Figure 4.5. Activation energies of defects determined from AS studies. The results for the selenized devices are represented by filled bars and the results for the evaporated devices are represented by the open bars.

using admittance spectroscopy (AS). Although not as apparent in some measurements as in Figure 3.13, the step in capacitance-frequency plots was used to deduce E_a for the devices shown in Figure 4.2. The results are summarized by device type in Figure 4.5. Even after accounting for typical uncertainties on the order of tens of meV in calculating E_a, Figure 4.5 clearly indicates significantly lower activation energies for the defects detected in the evaporated devices than for the defects detected in the selenized devices.

4.3.2 Trapping State Densities

As described in section 3.4.2, trap state densities were estimated from AS data using the low- and high-frequency values of capacitance where a step in the capacitance occurred. The relative step sizes are illustrated in Figure 4.6 for an evaporated and a selenized device.

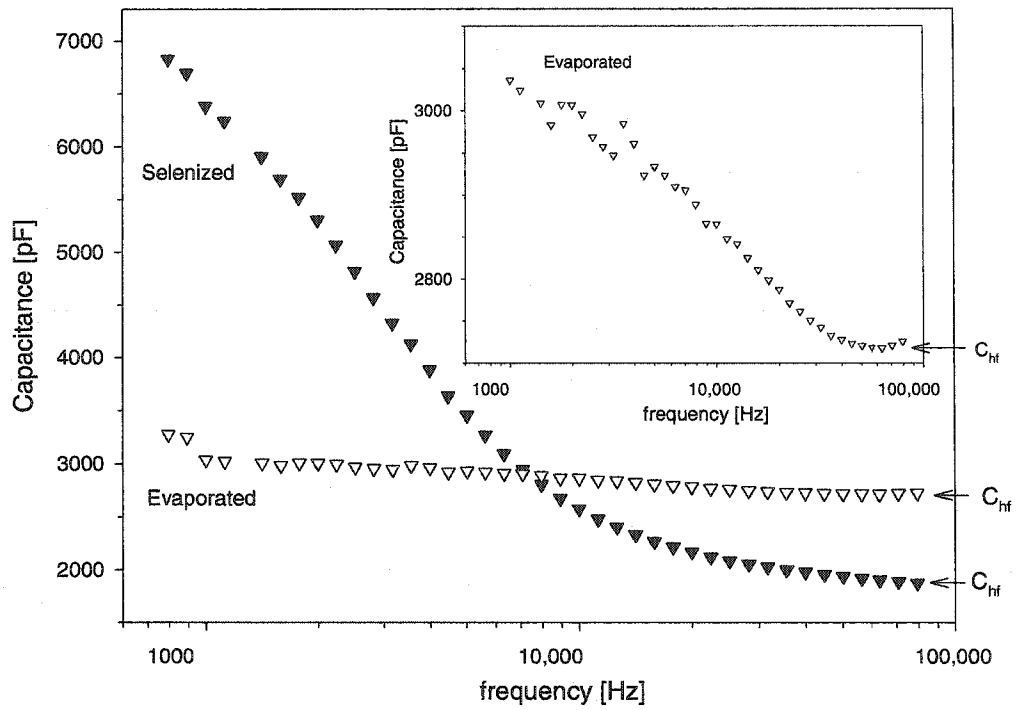

Figure 4.6. Capacitance vs. frequency for an evaporated Cd PE device and a selenized Cd PE device. The inset shows the evaporated plot magnified. The filled symbols represent the selenized data taken at 210 K and the open symbols represent the evaporated data taken at 120 K.

Both are Cd PE devices with similar areas. Although the high frequency capacitance (C_{hf}) appears to be saturated around 100 kHz, it is not clear where or whether the low frequency capacitance (C_{lf}) saturates, as the noise in the data overwhelms the results at approximately 700 Hz. The low-frequency capacitance was estimated to saturate at approximately the capacitance value for the lowest frequency data point shown. N_t is much more readily extracted from plots such as those for the selenized CdS device shown in Figure 3.13 where the low and high frequency capacitance saturation is more pronounced.

Since both devices had similar areas, as well as similar estimated values of V_{bi} (~1V), there is a clear difference in extracted trap densities due to the difference in step sizes

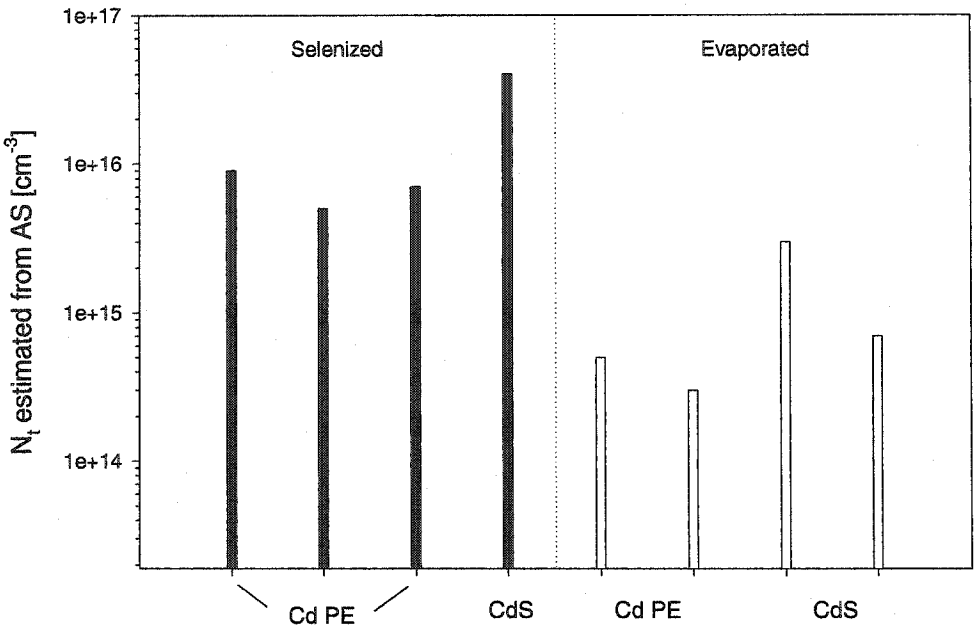

Figure 4.7. Trap density estimated from AS. Bars pertaining to selenized devices are filled, while bars pertaining to evaporated devices are open.

of the data shown in Figure 4.6. The estimated trap density for the selenized device is $7 \times 10^{15}\text{cm}^{-3}$, while the estimated trap density for the evaporated device is $5 \times 10^{14}\text{cm}^{-3}$.

A summary of all of the trap densities estimated from AS is given in Figure 4.7. By estimating the trap densities using results from different measurement temperatures and different built-in voltages, the error on these values is estimated to be a maximum of a factor of 2. Even if N_t for the selenized devices was too large by a factor of 2 and N_t for the evaporated devices too small by a factor of 2, the selenized devices would all have a larger N_t than their evaporated counterparts.

4.4 Drive-level Capacitance Profiling

4.4.1 DLCP vs. CV-T

The unique ability of DLCP to isolate the capacitance response of bulk states from the response of near-interface states allows one to extract information about interface states by comparing DLCP results to results using standard CV analysis techniques. To use standard CV measurement analysis, the measured capacitance, C_{meas}, from the 30 mV probe signal, i.e. small-signal capacitance, was taken from the data from the DLCP measurement. The corresponding nominal bias value, V_n, was then used to find $dV/d(A^2/C^2)$ and subsequently the apparent carrier density, $N(W)$, as shown in equation 3.6. Since the measurements in this work detected free and trapped carriers in the p-type material, as will be discussed in the following chapter, $N(W)$ will be labeled "apparent p", the apparent free hole density. This was done for each temperature at which the measurement was taken. These values of apparent free carrier density were then plotted on the same axis as the drive-level response, N_{DL}, as seen below in Figure 4.8 and Figure 4.9.

Although the spatial non-uniformity of the drive-level response of the evaporated devices prevented the extraction of a trapping state density or a free carrier density from DLCP results, the results were still rather illuminating. Recall from sections 3.5 and 3.6, that the drive-level technique and subsequent analysis are only sensitive to states at least a certain minimum distance, x_e, away from the p-n junction. However, traditional CV analysis is sensitive to states responding anywhere in, or at the edge of, the space-charge region. Consequently, the difference between the apparent free carrier density and N_{DL} for any given nominal bias, is a good indicator of the density of near-interface states, N_{IS}, as shown in Figure 4.10. By comparing Figure 4.8 and Figure 4.9, it is apparent that the evaporated devices have a much smaller difference between the CV-T and DLCP data than

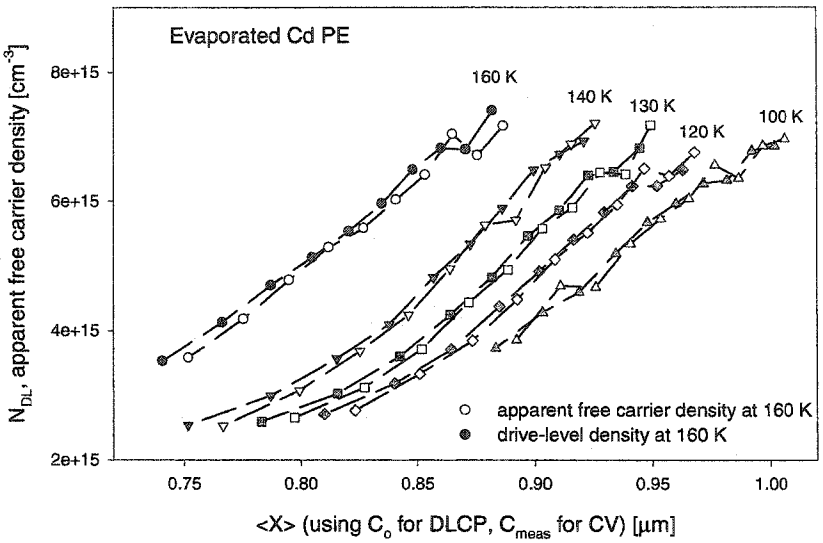

Figure 4.8. Drive-level density (filled symbols) and apparent free carrier density (open symbols) vs. relative position.

the selenized devices and hence a much smaller density of near-interface states. Note this trend is consistent for all measurement temperatures for the two devices shown in these figures.

A few explanatory notes regarding Figure 4.8 and Figure 4.9 are in order. First, $\langle x \rangle$ is the average position of charge change [20]. If the CIGS did not have any defect states that cross the Fermi level during the measurement, $\langle x \rangle$ and W, the depletion width deduced in equation 3.2, would be equal. However, any defect states that cross the Fermi level reduce $\langle x \rangle$ somewhat from W. Second, the slight shift to higher values of $\langle x \rangle$ for the CV results (shown in the open symbols) is due to the use of C_{meas} when calculating $\langle x \rangle$, as is traditionally done for CV; whereas C_o was used to calculate $\langle x \rangle$ for the DLCP results, as they are typically presented [20, 48]. Third, although the vertical scales used in the two figures differ somewhat for aesthetic reasons, the observations regarding the data hold when plotted on the same y-axis. This is confirmed by Figure 4.11, below. Finally, the

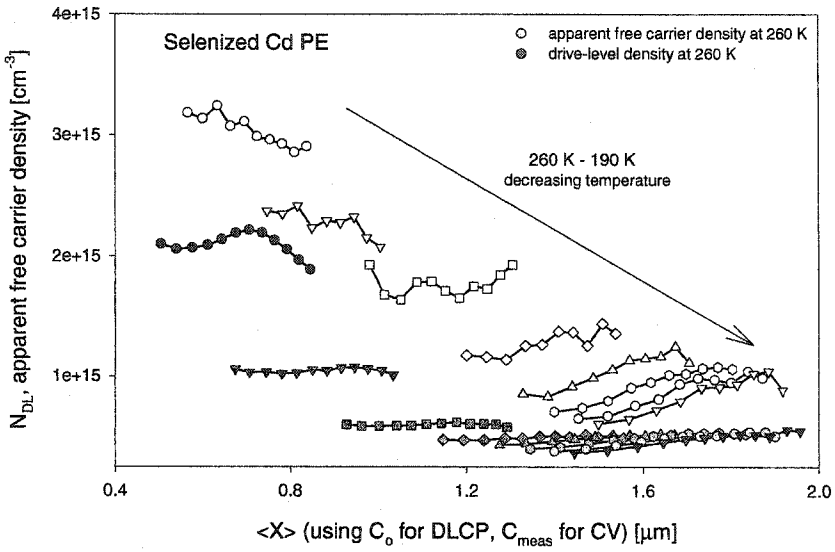

Figure 4.9. Drive-level density (filled symbols) and apparent free carrier density (open symbols) vs. relative position.

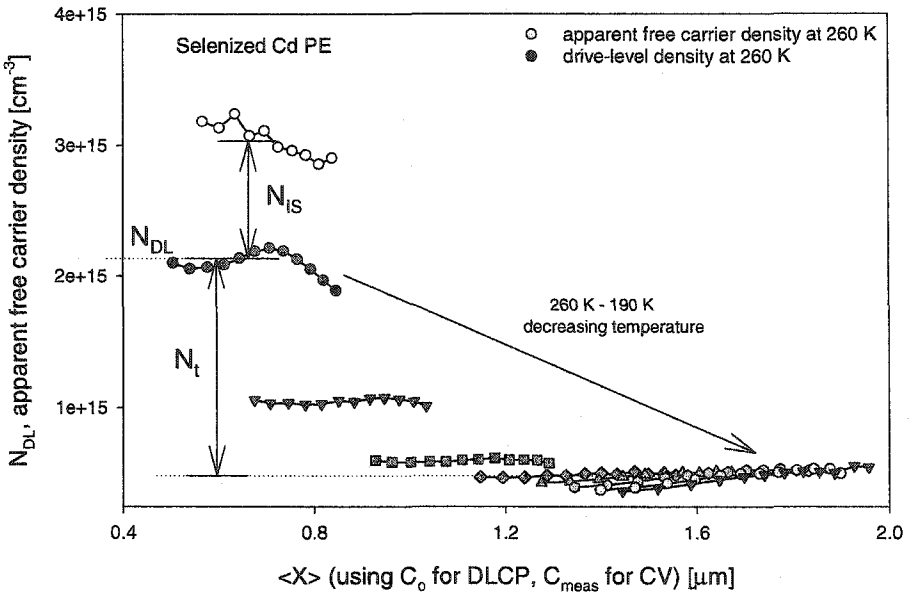

Figure 4.10. Graph of measurement results depicting the extraction of near-interface state density N_{IS} at 260 K, drive-level density N_{DL} at 260 K, and trapping state density N_t from DLCP. DLCP and CV-T results were used to make the plot.

response difference is due to a difference in the devices, and not the measurement temperature. Admittance spectroscopy was performed on all devices at overlapping temperature ranges. DLCP was then performed on each device at temperature and frequency combinations consistent with saturated AS values ranging from C_{lf} to C_{hf}.

Figure 4.11a. summarizes the trend from the DLCP and CV-T measurements on all 6 of the samples for which DLCP data was taken. The black portion of the graph represents the drive-level response at a given temperature, probe frequency, and V_n, while the total height of the bar represents states detected in the CV measurement. Thus the difference, the lighter colored portion of the graph, is a good approximation to the density of states in the band gap near the interface region (N_{IS}). Due to the ability of DLCP to extend further into the bulk than CV-T, this approximation may actually underestimate N_{IS}.

While Figure 4.11a. suggests that the actual number density of near-interface states is larger in selenized devices than evaporated devices, Figure 4.11b. gives N_{IS} as a fraction of total detected states. This graph illustrates the trend in a more distinctive manner, evaporated devices have fewer near-interface states as a fraction of total shallow states detected in the band gap.

4.4.2 Trapping State Densities

Figure 4.12 displays the drive-level response vs. E_e, the deepest energy for which a defect can respond at a given frequency and temperature. Measurements taken at two different probe-signal frequencies for each of two selenized devices are shown. The diamonds represent data taken at 60 kHz, while the hexagons represent data taken at 11 kHz. The values of N_{DL} plotted in Figure 4.12 are the average value of N_{DL} for each of the temperatures for which DLCP data was taken. Note that N_{DLmax} saturates unequivocally for the device plotted against lower E_e values, while N_{DLmin} is clearly saturated for the other device. The other two saturation points have been estimated by observing the trend of each curve and are indicated on the graph. As discussed in Chapter 3, the saturated value of N_{DLmin} is the free carrier density, and the difference between the saturated N_{DLmax} and N_{DLmin} is the trap state density. The free carrier density, p, was ~10^{14} cm^{-3} for all of the selenized devices, and N_t deduced from Figure 4.12 and others like it was ~10^{15} cm^{-3} for all of the selenized devices.

These trapping state densities were then compared with values of N_t deduced from the step in AS measurements. The estimated error in the N_t values from AS is a factor of 2. For all of the selenized Cd PE devices, N_t from both AS and DLCP were the same order of magnitude, as shown in Figure 4.13. The difference for the CdS device was somewhat

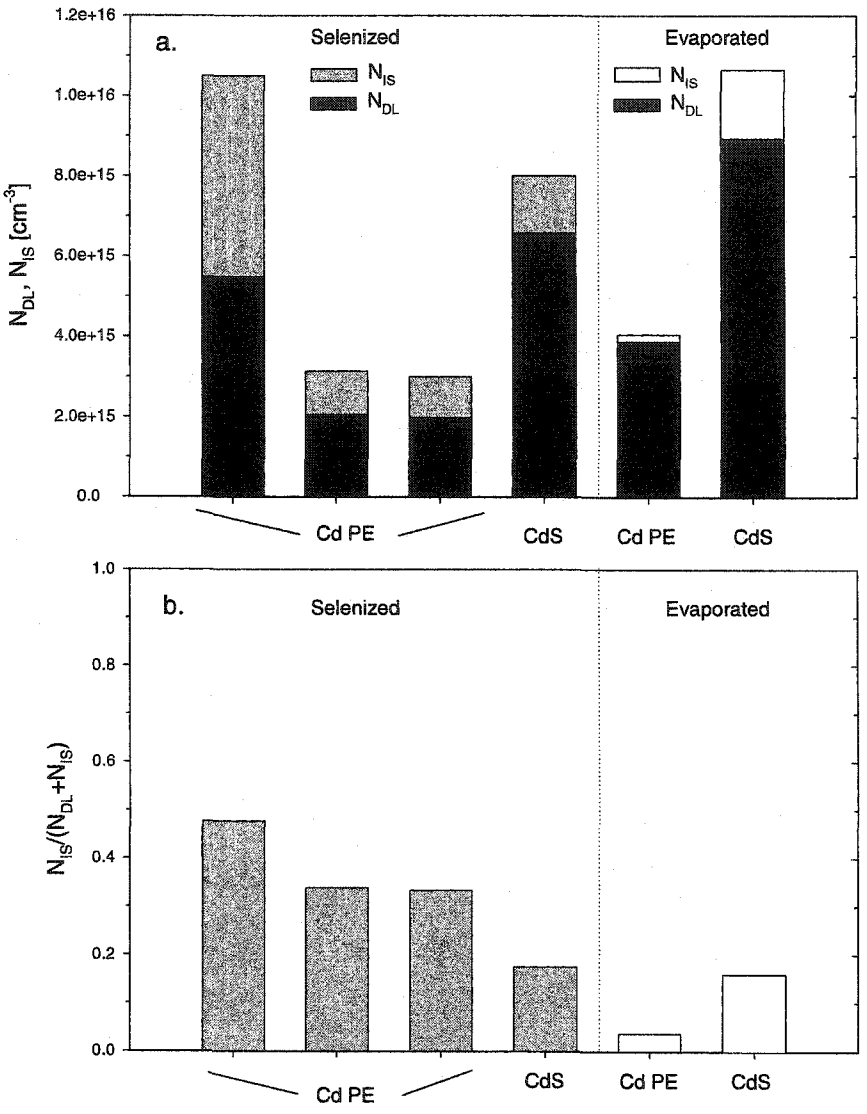

Figure 4.11. Detected interface states, by device type. N_{DL} values are the DLCP response. N_{IS} values are the difference between the CV-T and the DLCP response for a given temperature.

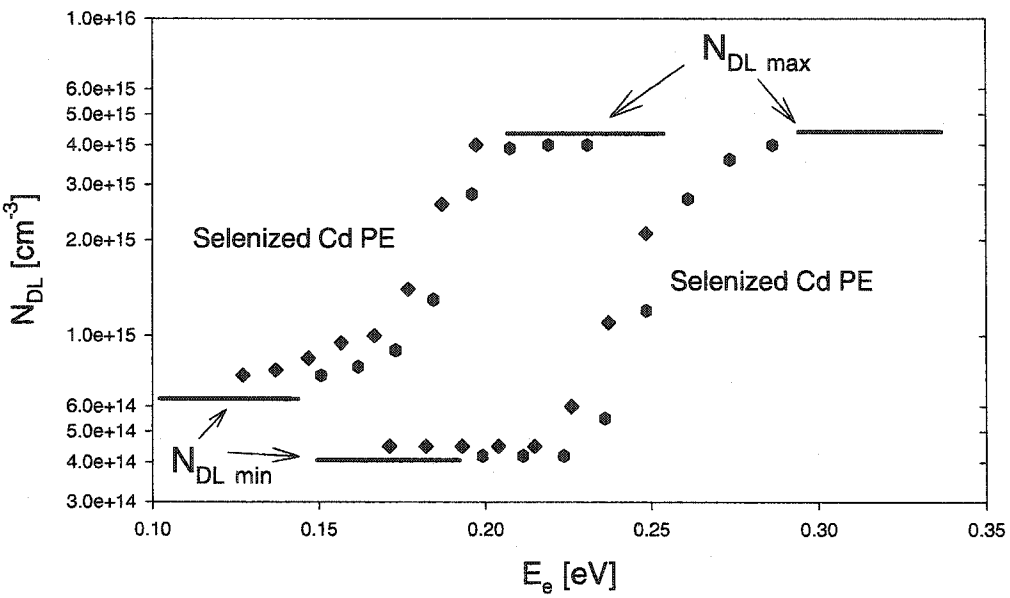

Figure 4.12. Drive-level response vs. limiting deep-state energy, E_e, for two selenized Cd PE devices. The diamonds represent data taken at 60 kHz, while the hexagons represent data taken at 11 kHz. The inflection point of each curve corresponds to the energy at which the detected trap state density is the greatest for each device.

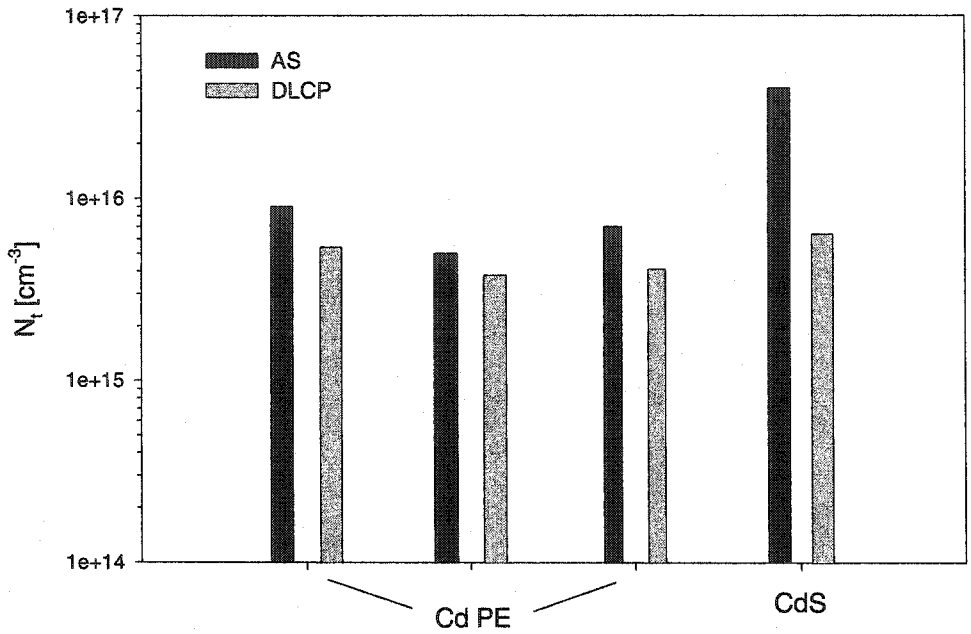

Figure 4.13. Trap density response from AS and DLCP for the selenized devices in the study. AS data is repeated from Figure 4.7. N_t deduced from the DLCP data shown in Figure 4.9 accounts for one of the gray Cd PE bars in this figure.

larger, approximately a factor of 5. These results were, however, still encouraging, as they indicate that AS measurements (somewhat easier to implement than DLCP) do provide credible values of N_t for the selenized Cd PE devices. In addition, among the different selenized devices, the relative values of N_t were consistent whether they were deduced from AS or DLCP measurements. Although some of the position space probed by AS and DLCP overlap, these two measurement techniques can also fundamentally detect defects in different spatial regions of the device. Consequently, the aforementioned correlation was unexpected and one should not assume that will be the case for other devices. Due to the spatial non-uniformity of the DLCP response of the evaporated samples, N_t and p could not be calculated for these devices from DLCP data.

4.5 Parameter Trends

4.5.1 Evaporated vs. Selenized Devices

The preceding sections have outlined several trends when comparing the evaporated devices to the selenized devices. As Figure 4.2 and Figure 4.3 show, the evaporated devices had larger values of V_{OC} than the selenized devices, in addition to somewhat lower diode quality factors. Both of these trends indicate that the evaporated devices have a more robust junction less prone to recombination than comparable selenized devices.

The defects detected in the evaporated devices also had lower activation energies (Figure 4.5) than those detected in the selenized devices. These activation energies were all lower than any reported in the publication summary figures and table in Chapter 1. Indeed, their values were more akin to the expected energy levels of shallow acceptor levels than deep-level trapping states. Authors of other studies on CIGS devices claim to have found shallow acceptor levels using AS as well [21].

Most notable among the capacitance results, the DLCP and comparable CV results shown in Figure 4.8, Figure 4.9, and Figure 4.11 indicate a much larger presence of states in the band gap near the p-n junction in the selenized Cd PE devices than in the evaporated Cd PE device. And, as Figure 4.11b. shows, on average the fraction of detected states near the interface is larger in all selenized devices than in all evaporated devices. Due to the bending of the conduction and valence bands, detected states near the junction are more likely than detected states in the bulk to be near mid-gap, since the Fermi level is closer to mid-gap near the junction than in the bulk, and trapping states must be near the Fermi level in order to be detected by capacitance techniques. Consequently, detected states near

the junction are more likely than detected states in the bulk to be effective recombination centers, thereby decreasing the voltage of a device. Thus, the difference in spatial location of some of the detected states is the likely reason why the evaporated devices consistently perform better than their selenized counterparts.

4.5.2 CdS Devices vs. Cd PE Devices

4.5.2.1 Among All Devices Studied

A rather unexpected result among all N_t values calculated, was that the N_t values for the CdS devices were all higher than their Cd PE counterparts. This was true not just for N_t calculated from AS, but also for N_t calculated from DLCP, although the differences between CdS and Cd PE were smaller for DLCP. Expectations were that the CdS devices would have fewer trapping states, as both V_{OC} and diode quality factor values point to less recombination in CdS devices than in Cd PE devices. This is yet another indicator that not all of the trapping states detected are effective recombination centers.

4.5.2.2 Among Selenized Devices

Even though the location of some of the detected trapping states in the selenized devices indicate that those states are likely recombination centers, not all of the detected trapping states in the selenized devices appear to result in weaker devices. In fact, it is likely that the near-interface states N_{IS}, shown in gray in Figure 4.11a. (the difference in CV-T and DLCP response as shown in Figure 4.10) result in recombination. It is also likely, and consistent with the data, that the trapping states (N_t) detected by DLCP (also shown in Figure 4.10) are not effective recombination centers. This is explained below.

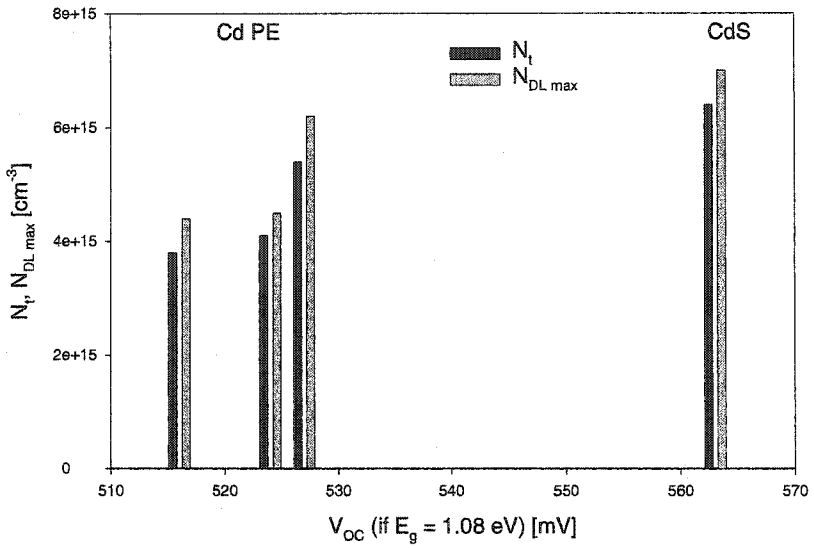

Figure 4.14. Trap density and maximum drive-level response from DLCP measurements vs. open-circuit voltage for the selenized devices.

First, recall that DLCP will not detect interface states. Among the selenized devices, a larger V_{OC} was correlated to both a larger trapping state density, N_t, and a larger $N_{DLmax} = N_t + p$, from DLCP measurements. This correlation can be seen in Figure 4.14, where the x-axis value of V_{OC} has been adjusted for slight band-gap differences among the devices (~10 meV). Both of these correlations suggest that the traps detected using DLCP do not participate in recombination that limits the performance of the devices. These detected defect states may instead be affecting a device much like non-frequency dependent shallow acceptor states, despite some of their activation energies being just barely small enough to be classified as a shallow state in a 1.1-eV band gap material. Barring other differences such as the band gap or the recombination current, the larger the density of shallow acceptor states in a the p-type region of CIGS devices, the larger the open-circuit voltage of the device.

While the similarity between N_t deduced from AS, which can detect interface states, and N_t deduced from DLCP calls this suggestion slightly into question, the N_t similarity does not void the suggestion. Since N_t from AS was consistently higher than N_t from DLCP, the difference may be related to the near-interface states apparent in Figure 4.9 and Figure 4.11. The difference in N_t from Figure 4.13 is ~10^{15}cm^{-3}, the same order of magnitude as the near-interface trap states observed in most of the selenized devices. Consequently, it is consistent to state that the evaporated devices likely perform better because they have fewer near-interface trap states, while the carrier densities of the selenized devices benefit from states in the bulk $\lesssim 0.3$ eV above the valence band.

Chapter 5

Discussion of Related Items

This short chapter will address global issues pertaining to this work.

5.1 Defect Type

As mentioned in Section 1.4.3.2, several groups believe that the defect N1, with activation energies that typically range from 50 - 200 meV, the same values determined for the defects in this work, is a donor-like trap, i.e. a state closer to the conduction than the valence band edge. This claim has been disputed by Heath [20], who has found that the capacitance step in AS measurements is not consistent with the detection of states in the thin layers of n-type material. Thus, Heath states that N1 is an acceptor-like trap. Heath asserts that since the detected states all fall on the same Meyer-Neldel line, that they are likely the same defect. Evidence in the current work supports the latter conclusion regarding defect type for those states detected by DLCP.

States detected by DLCP are almost certainly acceptor-like. Admittance spectroscopy and related techniques (including DLCP) will only yield information on majority carriers [13]. Thus, if one can determine which type of material is being probed, the type of carrier, and consequently defect state, will also be known. The nominal bias will move the edge of the depletion region in the more lightly doped side. The doping density in the CdS (an n-type material) is $\sim 10^{17} cm^{-3}$, while the doping density in the CIGS, the p-type absorber material, is $\sim 10^{15} cm^{-3}$. Thus, when a voltage is applied, the depletion region will change in the more lightly doped p-type material. Thus, since DLCP yields capacitance values that

result in the modulation of $\langle x \rangle$, the responding states are in the p-type material where the majority carriers are the holes. Consequently, we are almost certainly looking at acceptor-like traps.

To further the argument that DLCP is detecting charge change in the p-type material, and consequently acceptor-like states, refer back to Figure 4.8 and Figure 4.9. Recall that $\langle x \rangle$ is never greater than the depletion width W, and usually less than W. Note that the smallest value of $\langle x \rangle$ is 0.4 microns. Even if $\langle x \rangle$ was calculated using the lower dielectric constant for ZnO, $\langle x \rangle$ would still be much larger than the entire physical thickness of the CdS and the ZnO. Consequently, there is further confirmation that the techniques are probing states in the p-type CIGS.

Although some of the spatial locations probed by the AS and DLCP techniques are mutually exclusive, there is some overlap. Recall from Figure 4.13 that the detected trap state densities deduced by AS and DLCP had similar values and trends. Thus, the traps found using these two techniques likely overlap somewhat. Consequently, at least for some of the traps detected by AS, the carriers being trapped are holes.

Near the material interface between the CIGS absorber layer and the adjoining buffer/window material, however, the Fermi level is assumed to be closer to the conduction band than the valence band. Consequently, if there are somewhat shallow states near the interface, these states are more likely to be donor-like traps than acceptor-like traps. Assuming the activation energies for the trapping states detected near the interface using CV-T are similar to the activation energies of the states detected using AS (50 - 250 meV), these states are possibly donor-like traps. Thus, although the majority of the states detected using CV-T

are acceptor-like traps since they are also found using DLCP (see Figure 4.11b.), the states near the interface detected using CV-T are potentially donor-like traps.

5.2 Deep Defect Detected using Alternate Techniques

Recall the objective of this work was to correlate trapping state densities with device performance. While large total trap density detected by AS and DLCP techniques was not well correlated with poor device performance, other techniques may be able to investigate deeper states in the bulk whose density may undeniably correlate to device performance. For example, a trap 0.8 eV above the valence band has been found using transient photo-capacitance spectroscopy (TPC) [51]. This trap, along with other traps deeper in the band gap than the 50-250 meV states found in this work were not detected, since they were out-side the range of the measurement techniques used in this work.

The relevance of the detection of the 0.8 eV trap is two-fold. First, it confirms that there are viable techniques that can probe deeper into the band gap of CIGS-based devices. Second, Figure 1.4 and the first figure in the Appendix shed some light on this finding. The 0.8 defect was found consistently, regardless of the gallium content of the devices. Note that according to the theory presented in the aforementioned figures, there are not any native defects that are consistently pinned 0.8 eV above the valence band edge as the gallium content of the devices change. Thus, the extended theory work presented in Chapter 1 and the Appendix indicates that this 0.8 eV state is not due to a native, but rather an extrinsic, defect.

Chapter 6

Conclusions

We began by posing the question, "Are trap states the reason the Cd PE devices have an inferior junction compared to devices containing CdS buffer layers?" We then extended that question to, "Are trap states the reason that selenized devices have a somewhat inferior junction when compared to evaporated devices?" Although the answer to the first question appears to be no, we cannot say for certain since we were limited by device characteristics coupled with frequency and temperature constraints as to how deep into the band gap we could probe.

There are deeper levels, however, that could explain the performance differences. Indeed, as mentioned in the previous chapter, other researchers using optical techniques have found deeper levels that do appear to be correlated with device performance when devices have varying amounts of gallium [51]. Thus, the first conclusion from this study is that although AS combined with DLCP and CV-T can typically deduce free carrier density in the absorber, density of trapping states in the near-interface region, and density of trapping states in the bulk CIGS; these techniques do not have the capability to detect states deep in the bulk of the CIGS. Thus, to establish concretely whether it is the larger near-interface state density (N_{IS}) in the selenized devices that is responsible for the performance differences between selenized and evaporated devices, a technique which can detect deeper trapping states must be used to study comparable selenized and evaporated devices. Two potential options are transient photocapacitance spectroscopy (TPC) and deep-level transient spectroscopy (DLTS). Currently, DLTS has failed to find the deep defects in evaporated devices, but anticipated equipment improvements may increase the depth to which

DLTS can probe into the band gap. If the evaporated and selenized devices are found to have deep bulk defects with similar activation energies and similar defect densities, then it is quite likely the interface states are the reason for the performance differences.

We have also learned that there are frequency-dependent shallow states within the CIGS band gap. While their ionization state is clearly frequency and temperature-dependent, the AS results reveal that at operating temperatures these states are ionized, much like standard shallow dopant states. Based on room-temperature JV curves of these devices, it does not appear that these states detected using capacitance techniques at somewhat low-temperatures (100 K - 250 K) have detrimental effects on the devices near operating temperatures. Indeed, in some cases these shallow bulk states even appear to have beneficial effects on the devices near operating temperatures. Although it is the bulk states in the selenized devices detected by DLCP that most clearly have the beneficial effects on the devices, and the states detected by AS that are clearly ionized at room temperatures, as previously mentioned, the states detected by these two methods are not mutually exclusive.

In closing, I have several suggestions for the group most likely to be most interested in this work, the National CIS R&D Team, comprised of scientists from industry, academia and national laboratories. First, if a producer of selenized devices decides to change their buffer layer, they will most likely need to change their process in such a way as to reduce interface states in order to maintain their current performance level. Second, in the best laboratory and production-floor devices, the shallow trap state density on its own accord is likely not detrimental, however, the spatial location of detected states (near the interface vs. in the bulk) is of consequence. Contrary to the credibility several publications give stand-alone AS results, it appears that AS is not a complete study unless DLCP and CV-T

results are also incorporated. Similarly, DLCP itself will not find the recombination states in these devices, CV analysis must also be done. Finally, in the search for recombination centers in the bulk, TPC is likely the best option at this time due to its sensitivity to deeper defect states.

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APPENDIX: THEORETICAL AND EXPERIMENTAL NATIVE DEFECT LEVELS IN CIGS [3-5]