DISSERTATION

IMPACT OF THERMAL MANAGEMENT ON VERTICAL-CAVITY SURFACE-EMITTING LASER (VCSEL) POWER AND SPEED

Submitted by

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ABSTRACT

IMPACT OF THERMAL MANAGEMENT ON VERTICAL-CAVITY SURFACE-EMITTING LASER (VCSEL) POWER AND SPEED

Increasing the modulation bandwidth and output power of vertical-cavity surface-emitting lasers (VCSELs) are of great importance in a variety of applications such as data communication systems. The high temperature generated in the active region of VCSELs is one of the main limiting factors in achieving high power and high speed operation.

This work is focused on investigating the effects of thermal management on improving AC and DC properties of VCSELs and achieving higher thermal performance devices. Thermal heatsinking is obtained by surrounding the VCSEL mesas with high thermal conductivity materials such as copper and also using passive heatsinking by flip-chip bonding the laser dies on a GaAs heat spreader. The research includes fabricating and characterizing 980 nm bottom-emitting and 670 nm top-emitting oxide-confined VCSELs. This dissertation is divided into three main parts: high-power, high-speed 980 nm VCSEL arrays, low thermal resistance 670 nm VCSELs, and temperature dependent dynamics of 980 nm VCSELs.

Experimental work performed on fabricating and characterizing 980 nm, bottom-emitting, oxide-confined VCSEL arrays and single elements is presented first. The result of DC and AC characterization confirms the effectiveness of Cu electroplating of mesas

and flip-chip bonding in reducing VCSELs' thermal resistance to obtain lower operating temperatures. Uniformity of frequency response and operating wavelength across the arrays also motivates managing thermal issues and is an indication of uniform distribution of current and heat flux on the array. This research resulted in record VCSEL arrays with frequency response of approximately 8 GHz and operating CW power of 200 mW. These 28-element, 18μm aperture diameter arrays represent the highest power reported for a VCSEL or VCSEL array with greater than 1 GHz modulation bandwidth.

The second part of this dissertation details the fabrication steps and DC characterization of visible, 670 nm, top-emitting, oxide-confined VCSELs. Since achieving high operating temperatures is one of the main challenges in realizing improved red VCSELs, the effect of mesa heatsinking on improving their DC behavior using copper electroplating of mesas is studied. Thermal modeling of the copper plated VCSELs also facilitates better understanding and analysis of the experimental results. A photomask and process flow were designed to fabricate VCSELs with a variety of mesa diameters and inner and outer plating sizes to investigate the major direction of heat flow in the VCSELs and decrease VCSEL thermal resistance and thus increase the output power. Although copper plating significantly reduces thermal resistance, it did not substantially increase maximum operating temperature of the red devices and also put the mesas under stress that might not be desired. This study led us to analyzing the effects of stress on the VCSEL mesas which is induced by the copper films.

Finally, the temperature dependence of 980 nm VCSEL dynamics is investigated using noise spectra measurement. This analysis provides some useful insights in understanding how temperature alters VCSEL properties and how these properties can be

improved. A VCSEL with 7 μm aperture diameter was fabricated from the same epitaxial material and followed the same processing steps as the VCSEL arrays. Relaxation oscillation frequencies and damping factors as functions of bias current and stage temperature were extracted. These results along with the VCSEL DC measurement were used to estimate the laser differential gain as a function of temperature. The differential gain was shown to be relatively temperature independent over a temperature range of 10 ˚C to 70 ˚C with an average value of approximately 12×10^{-16} cm^2. This research led us to the conclusion that improving the output power at elevated temperatures should yield better frequency response in this case. The VCSEL output power reduction was observed to be the major cause of bandwidth reduction at elevated temperatures for the device under test. This work is the first report on the measurement of temperature dependence of VCSEL dynamics.

ACKNOWLEDGMENTS

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maintenance and were always there whenever I needed a second hand. Thank you guys for your hard work!

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Chapter 1

INTRODUCTION

1.1. Introduction

Semiconductor lasers are the most important light source for optical communication because of their high efficiency, small size, simple structure, and more importantly, compatibility with electronic chips. According to the direction of the laser beam coming out of the laser and its propagation direction with respect to the grown epitaxial layers, there are two main categories of semiconductor lasers. These two are the vertical-cavity surface-emitting laser (VCSEL) that is the main focus of this dissertation and the edge-emitting laser (EEL). The structure of both types of lasers will be discussed in the next chapter.

After their invention in the 1980s, VCSELs became very popular in both research and from a technological point of view. Since 1996 when the first commercial VCSEL was presented by Honeywell, they have become dominant light sources and replaced EELs for a wide range of applications such as short-range fiber optics communication.

VCSELs can offer a number of fascinating properties such as [1], [2]:

- Very low threshold current, I_{th}, due to small cavity volume (<0.1 mA [3])
- Single longitudinal mode operation

- High speed direct modulation (>20 GHz [4]) due to a very large relaxation oscillation frequency
- Low power consumption and high power-conversion efficiency (>50% [5])
- Relatively insensitive wavelength and thresholds to temperature changes
- Narrow circular beam and easy coupling to optical fiber
- Good reliability
- Realization of monolithic large-scale two-dimentional (2D) VCSEL arrays
- Easy bonding and on chip testing before sample cleaving; lowering manufacturing cost
- Integration with micro electromechanical systems for wavelength tuning

Such unique features of VCSELs make them popular and a potential light source for a variety of applications. These applications include short-range optical communication like Gigabit Ethernet, fiber channels, computer links, optical interconnects, high speed local area networks (LANs), position sensing, automotive applications and consumer electronics such as projection displays and laser mice [1], [6].

Table 1.1 VCSEL market by application in US$ million (reproduced from [7])

	2003	***2004***	***2005***	***2006***	***2007***	***2008***
Automotive	18	23	27	30	33	38
Computer	65	79	94	109	114	133
Consumer	63	77	93	103	112	131
Industrial	30	37	44	49	53	62
Military/Aerospace	20	24	29	32	35	41
Telecoms	25	31	37	41	45	52
Other	9	11	13	15	16	19
Total	**231**	**282**	**337**	**375**	**407**	**477**

In Table 1.1 contribution of each VCSEL application in the global market in 2003-2008 is presented in US$ million [7]. It can be seen from the table that computer related applications such as optical networks and consumer electronics such as optical mice, scanners, and sensors are two of the largest applications of VCSELs in the global market.

1.2. VCSELs at different wavelengths

The first attempts in realizing VCSELs were based on devices operating at 850 nm and 1310 nm based on GaAlAs/GaAs and GaInAsP/InP active regions, respectively [1]. VCSELs operating at 850 nm were the first commercialized multitransverse-mode VCSELs. However, the invention of oxide isolation in VCSELs opened new doors towards the single transverse-mode VCSELs which facilitate using them in sensing, printing, and optical memory applications [8]. 850 nm VCSELs were the first available VCSEL in the market and very soon became the standard wavelength for the optical communication. The highest modulation speed for commercialized 850 nm VCSELs was revealed by Panasonic in 2005 and was capable of data rates of up to 12.5 Gb/s [7].

In near infrared, in addition to 850 nm VCSELs, 780 nm and 980 nm are of great importance. 780 nm VCSELs which, like 850 nm, are already commercialized are suitable for applications in laser printing industry which has developed toner dye that is preferentially absorptive to 780 nm [8]. Commercialized VCSELs ranging from 750-870 nm are fabricated based on AlGaAs/GaAs quantum wells. Using InGaAs/GaAs QWs, one can achieve longer near infrared wavelengths such as 980 nm. This wavelength has an advantage of being transparent to the GaAs substrate that makes the VCSEL packaging easier.

Long-wavelength VCSELs (LW-VCSELs) at 1310 nm and 1550 nm have also become important for applications in high-bandwidth optical networks [9] and in communication systems based on optical fiber such as long-haul transmission lines [10]. One very interesting feature of LW-VCSELs is that they are eye safe at wavelengths >1400 nm and so they can be used in free space optical communication in which eye safety should be highly considered.

VCSELs in visible wavelengths (660-680 nm) are also finding their applications in plastic optical fiber (POF) communication, medical, and data reading/capture [11]. Applications in consumer electronics such as laser mice and barcode scanners can also be served by visible VCSELs. Red VCSELs are grown on GaAs substrate using InGaP/InGaAlP active material. Because of their relatively small band offset and consequently poor carrier confinement, it is difficult to achieve high temperature lasing using this material [8]. As a result, techniques to bring the active region temperature down are helpful for realizing better performance red VCSELs.

1.3. Research objectives and outline

In this research, 980 nm and 670 nm VCSELs have been fabricated and their different aspects characterized. Thermal resistance reduction and high speed modulation frequency with high power operation of VCSELs were investigated.

Chapter 2 discusses the background and operating principles of VCSELs including basic concept of DBRs as high reflectivity mirrors and QWs as active regions. This chapter also reviews governing equations for semiconductor laser frequency response.

In Chapter 3 the previously published work on VCSELs from their birth has been reviewed and important steps in development of VCSEL fabrication and characterization have been addressed.

Chapter 4 presents the fabrication steps of bottom-emitting flip-chip bonded VCSELs and then describes the details of fabrication and characterization of 980 nm high-speed, high-power VCSEL arrays. These arrays have the highest ever reported optical power for greater than 1 GHz modulation speed at the time of research.

Chapter 5 details the fabrication steps of top-emitting VCSELs and also discusses the attempts for thermal resistance reduction and output power enhancement of 670 nm visible VCSELs with better thermal management of active region by copper electroplating of the mesas. In addition, stress on VCSEL mesas induced by plated copper is explained. Thermal and stress modeling of copper plated red VCSELs using COMSOL multiphysics is also given in this chapter.

In Chapter 6 temperature dependence of dynamics of 980 nm VCSELs are investigated using noise spectra measurement. In this chapter after estimating the relaxation oscillation frequency and damping factor, the differential gain of the device under test as well as some other laser parameters are extracted. This work is also the first report on temperature dependence of 980 nm oxide confined VCSEL dynamics.

Finally, Chapter 7 concludes the work done in previous chapters and gives suggestions for the possible future work.

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Chapter 2

VCSEL STRUCTURE AND OPERATING PRINCIPLES

2.1. Introduction

Semiconductor lasers are the most important light source for optical communication because of their high efficiency, small size, simple structure, and more importantly, compatibility with electronic chips. In a very simple point of view, a semiconductor laser is a forward biased p-n junction in a resonant cavity which can be formed by cleaving the facets of the structure as shown in Figure 2.1. In this case, the junction of p and n regions is the active region in which electrons in conduction band recombines with holes in valence band and spontaneous emission occurs. Because of their p-n junction based structure, semiconductor lasers are also known as diode lasers.

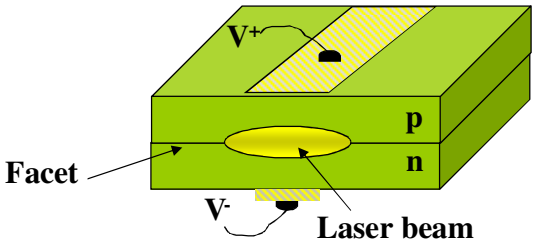

Figure 2.1 A basic p-n junction laser.

The spontaneously emitted single photon with energy equal to semiconductor bandgap energy, E_g, can generate another identical photon by stimulating the

recombination of an electron-hole pair. This photon multiplication is the key mechanism of lasing. The second photon exhibits the same wavelength and phase as the incident photon; therefore, this process doubles the amplitude of the resultant optical wave. Subsequent repetition of this process can generate very strong light fields. However, the reverse process which is absorption of photons by generation of new electron-hole pairs should also be taken into account. Absorption, spontaneous emission, and stimulated emission processes are schematically shown in Figure 2.2.

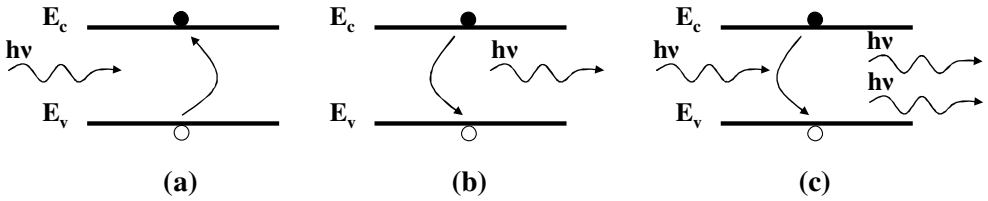

Figure 2.2 Photon-carrier interaction processes in semiconductors, (a) absorption, (b) spontaneous emission, and (c) stimulated emission.

The solution for the stimulated emission dominating absorption is carrier inversion, i.e. piling up more electrons in the conduction band than the valence band. Continuous carrier injection leads to continuous stimulated photon generation only if enough photons exist in the device to stimulate other photons. Now, an optical resonator is needed to create optical feedback and photon confinement [1].

Assume a laser structure with a gain medium surrounded by n- and p-type cladding layers all in a cavity with mirror reflectivities of R_1 and R_2 at two ends as in Figure 2.3. The whole structure in the cavity can be simply considered as a pin diode.

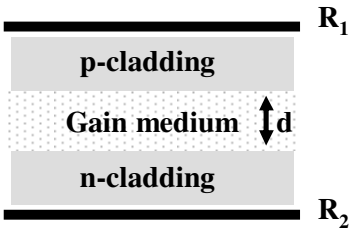

Figure 2.3 General configuration of a semiconductor laser.

In order to have a laser, total gain per unit length should overcome the total losses per unit length in the cavity. If we define G as the net power gain after a single trip in the cavity and g as the gain per unit length, these two can be related to each other by $G=exp((g-\alpha_i)d)$ where d is the length of the gain medium and laser and α_i is the internal loss of the cavity. A requirement for lasing is having a large enough gain in order that round trip gain exceeds 1 or in other words gain per unit length exceeds total losses per unit length, α. In this case $R_1R_2(G)^2 \geq 1$ and

$$R_1 R_2 e^{2(g-\alpha_i)L} \geq 1 \tag{2.1}$$

$$g \geq \alpha_i + \frac{1}{2L} ln \frac{1}{R_1 R_2} = \alpha \tag{2.2}$$

Before talking about threshold situation for lasing I would like to introduce a confinement factor, Γ, and substitute g with Γg in order to consider only the effective interaction between gain medium and photon field. Confinement factor is simply a ratio of active region volume occupied by gain, V_g, over the cavity volume occupied by photons, V_p, $\Gamma = V_g / V_p$ [2]. The threshold condition is considered as

$$\Gamma g_{th} = \alpha_i + \frac{1}{2L} ln \frac{1}{R_1 R_2} \tag{2.3}$$

$$\alpha_m = \frac{1}{2L} ln \frac{1}{R_1 R_2} \tag{2.4}$$

$$\alpha = \alpha_m + \alpha_i \tag{2.5}$$

Where α_m is the mirror loss from both mirrors.

2.2. Vertical-cavity surface-emitting lasers (VCSELs) vs. edge emitting lasers (EELs)

In a vertical-cavity surface-emitting laser (VCSEL), as illustrated in Figure 2.4(a), epitaxial layers are grown in x-y planes at different z positions, and light propagates along the normal to the epitaxial growth layers, i.e. in the z direction. Therefore, the length of the optical gain which effectively amplifies the optical field equals the active layer thickness which is in the order of ten nanometers to a few micrometers [3]. According to (2.3), with such a short cavity length, high mirror reflectivities are needed to achieve low threshold in VCSELs. Distributed Bragg reflectors (DBRs) formed by alternatively stacking layers of materials with different refractive indices can offer very high reflectivities above 99.9%. These types of reflectors will be studied in detail in Section 2.3.

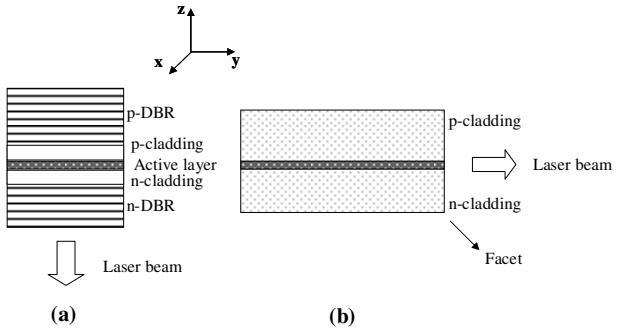

Figure 2.4 (a) VCSEL, (b) EEL.

In edge emitting lasers (EELs), as in Figure 2.4(b) laser beam propagates parallel to epitaxial layers along the y direction. In this case, the whole length of the gain medium along the propagation direction, which can be on the order of hundreds of micrometers, contributes to amplification. As a result, even with cleaved laser facets (~30% reflectivity of GaAs/Air interface) low threshold operation is achievable.

A shorter cavity length also leads to more widely spaced resonance modes in the cavity and so fewer cavity modes lie in between the low magnitude tails of the gain-loss curve of the gain material. This fact causes better single longitudinal mode operation in VCSELs compared to EELs as sketched in Figure 2.5.

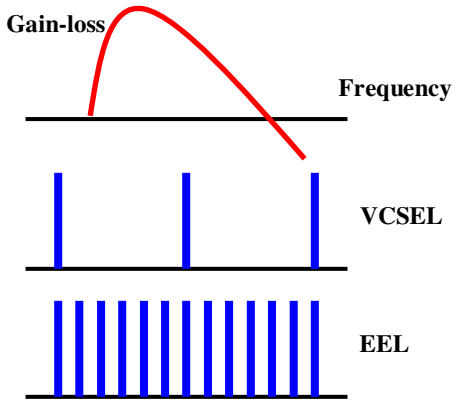

Figure 2.5 Gain-loss curve along with cavity resonance modes in VCSELs and EELs.

In next two following sections, I explain the working principles of DBRs and active regions which are two building blocks of VCSELs.

2.3. Introduction to distributed Bragg reflectors (DBRs)

Distributed Bragg reflectors (DBRs) are widely used as top and bottom mirrors in VCSELs because of their high reflectivity. Unlike hard mirrors in a Fabry-Perot cavity,

reflection points in DBRs are distributed all over the structure resulting in a mirror with varying reflection and phase change at different wavelengths [4], [5]. As in Fig 2.6, theses reflectors are formed by stacking alternating layers of semiconductor materials such as GaAs/AlGaAs or dielectric layers such as Si/SiO_2 with high and low refractive indices. If we choose a correct thickness for each layer, we can get beam reflection at each interface leading to a very large reflectivity with a constructive interference.

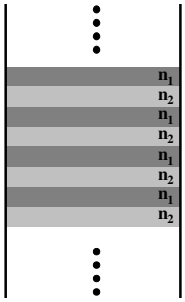

Figure 2.6 Stacking of layers with different refractive indices in a DBR.

Assume a normally incident light on an interface between two layers with refractive indices n_1 and n_2 and infinite thicknesses as shown in Figure 2.7. Incident electric field with amplitude E_1^+ hits the interface from the layer with refractive index n_1. Some portion of the beam with an electric field amplitude E_1^- reflects back to the n_1 medium. The transmitted beam which has the electric field amplitude of E_2^+ travels through the n_2 medium and as an assumption there is no incident beam from the n_2 region toward n_1, i.e. $E_2^-=0$. In this case with defining reflection coefficient, $r= E_1^-/ E_1^+$ and transmission coefficient, $t= E_2^+/ E_1^+$, the electric field in two regions can be related with a matrix called a transfer matrix, T_r.

$$\begin{bmatrix} E_1^+ \\ E_1^- \end{bmatrix} = \begin{bmatrix} 1/t & (r/t)^* \\ r/t & (1/t)^* \end{bmatrix} \begin{bmatrix} E_2^+ \\ E_2^- \end{bmatrix} = T_r \begin{bmatrix} E_2^+ \\ E_2^- \end{bmatrix} \tag{2.6}$$

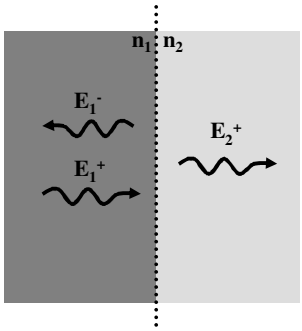

Figure 2.7 Electric fields at two sides of an interface.

From Fresnel's equation, $r=(n_1-n_2)/(n_1+n_2)$, and defining reflectivity, $R=rr^*=|r|^2$, and transmission, $T=tt^*=|t|^2$ of the interface and also neglecting absorption, by conservation of energy, we must have $R+T=1$. So

$$\left(\frac{n_1-n_2}{n_1+n_2}\right)^2+t^2=1\Rightarrow t=\frac{2\sqrt{n_1n_2}}{n_1+n_2} \tag{2.7}$$

Now let's consider another problem with 3 different media with refractive indices n_1, n_2, and n_3. Assume the n_2 medium with length d is placed between n_1 and n_3 regions which extend to infinity as drawn in Figure 2.8. Phase factors e^{ik_2d} and e^{-ik_2d} should be considered in this problem for the region 2 with thickness d and wave number $k_2=2\pi n_2/\lambda_0$, in order to count for the wave traveling through the region with a finite thickness.

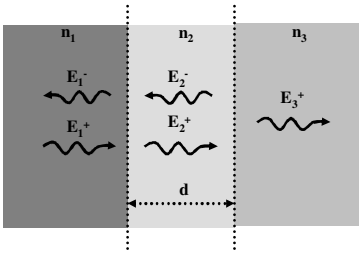

Figure 2.8 Electric fields for a two interface system.

In this case for the transfer matrix we have

$$\begin{bmatrix} E_1^+ \\ E_1^- \end{bmatrix} = \begin{bmatrix} 1/t_{1,2} & \left(r_{1,2}/t_{1,2}\right)^* \\ r_{1,2}/t_{1,2} & \left(1/t_{1,2}\right)^* \end{bmatrix} \begin{bmatrix} e^{-ik_2 d} & 0 \\ 0 & e^{ik_2 d} \end{bmatrix} \begin{bmatrix} 1/t_{2,3} & \left(r_{2,3}/t_{2,3}\right)^* \\ r_{2,3}/t_{2,3} & \left(1/t_{2,3}\right)^* \end{bmatrix} \begin{bmatrix} E_3^+ \\ E_3^- \end{bmatrix}$$

$$= T_r \begin{bmatrix} E_3^+ \\ E_3^- \end{bmatrix} \tag{2.8}$$

$$T_r = \begin{bmatrix} \frac{n_1+n_2}{2\sqrt{n_1 n_2}} & \frac{n_1-n_2}{2\sqrt{n_1 n_2}} \\ \frac{n_1-n_2}{2\sqrt{n_1 n_2}} & \frac{n_1+n_2}{2\sqrt{n_1 n_2}} \end{bmatrix} \begin{bmatrix} e^{-ik_2 d} & 0 \\ 0 & e^{ik_2 d} \end{bmatrix} \begin{bmatrix} \frac{n_2+n_3}{2\sqrt{n_2 n_3}} & \frac{n_2-n_3}{2\sqrt{n_2 n_3}} \\ \frac{n_2-n_3}{2\sqrt{n_2 n_3}} & \frac{n_2+n_3}{2\sqrt{n_2 n_3}} \end{bmatrix}$$

$$= \frac{1}{2\sqrt{n_1 n_2}} \begin{bmatrix} n_1+n_2 & n_1-n_2 \\ n_1-n_2 & n_1+n_2 \end{bmatrix} \begin{bmatrix} e^{-ik_2 d} & 0 \\ 0 & e^{ik_2 d} \end{bmatrix} \frac{1}{2\sqrt{n_2 n_3}} \begin{bmatrix} n_2+n_3 & n_2-n_3 \\ n_2-n_3 & n_2+n_3 \end{bmatrix} \tag{2.9}$$

It is easy to understand from (2.9) that if $k_2 d = m\pi$ (m integer) or $d = m\lambda/2$, the region 2 acts as a latent layer and passes the beam without any net phase change and we get the minimum reflection from the structure, while if $k_2 d = m\pi/2$ (m odd) or $d = m\lambda/4$, we have the maximum reflection and all the beam reflects back to the region 1. Similar argument for the thickness of layers is valid in DBRs. In DBRs, maximum reflectivity is achievable for a larger number of $\lambda/4$ thick layers.

In Figure 2.9, the reflection spectrum of a DBR with $\lambda_0/4n_{1,2}$ thick layers of GaAs/$Al_{0.86}Ga_{0.14}As$ (71.4 nm/83.3 nm) with corresponding refractive indices of 3.5/3 is calculated for different mirror periods. This DBR has been designed in a way to have the maximum reflection at λ_0=1 μm wavelength. For the highest reflectivity, this DBR is terminated by the higher index layer (GaAs) at both ends. It is obvious from the resultant

plot that the reflection increases with increasing the number of layers as expected. The DBR also behaves as a band pass filter which just reflects several 100s of nms above and below the center wavelength.

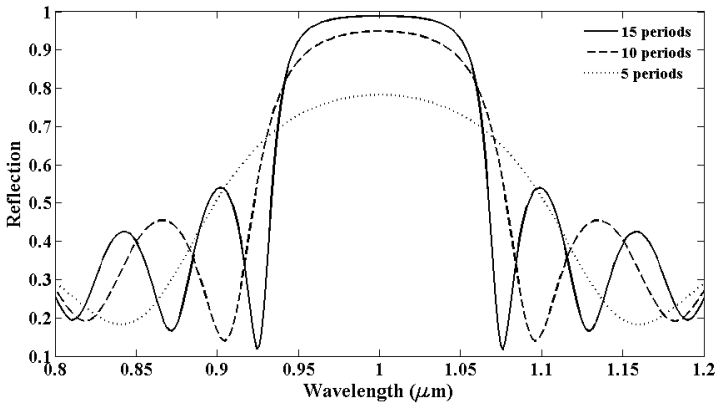

Figure 2.9 Reflection spectrum of a DBR with varying mirror periods.

A simplified expression might also be used to calculate the reflectivity at the Bragg frequency with no loss or gain [2]. With the number of mirror pairs, m, and reflectivity of each interface, r, the reflectivity of DBR at the Bragg frequency can be written as

$$r_{DBR} = \tanh\left[m \ln\left(\frac{1+r}{1-r} \right) \right] \tag{2.10}$$

In addition to optical properties of DBRs which were already discussed in this section, their electrical properties are also crucial in VCSEL operation; because, since electrical current needs to at least flow through a portion of top and bottom DBRs in VCSELs to reach electrical contacts. Although semiconductor DBRs are not perfect electrical conductors, they can be modified to improve their electrical behavior with a compromise between optical and electrical properties. When current flows through a

DBR, it meets potential barriers due to unequal bandgap energy of layers that can increase scattering and electrical resistance [4]. Compositional grading of DBR layers can smooth out the bandgap structure and reduces the carrier scattering [6]. Mirror doping can also be modulated in order to decrease series electrical resistance in DBRs [6].

2.4. VCSEL active region

The active region, where recombining carriers contribute to useful gain and photon emission, is another key element in semiconductor lasers. It is obvious that the active region in laser should be able to act as a gain region in which stimulated emission overcomes absorption for lasing.

The first semiconductor lasers were made up of homostructure devices in which only one type of semiconductor was used to fabricate lasers. These lasers showed high threshold currents even at low temperatures where the gain is higher and carrier density necessary for reaching transparency is lower than at room temperature. Besides, they couldn't operate in continuous wave (CW) [7].

The method that is now generally used to improve laser performance is utilizing heterostructure devices instead of homostructures. Let's see why heterostructures can help. We can solve (2.3) for threshold gain, g_{th},

$$g_{th} = \frac{1}{\Gamma}\left(\alpha_i + \frac{1}{2L} ln \frac{1}{R_1 R_2}\right) \tag{2.11}$$

For a bulk gain medium, and under very restrictive conditions, gain as a function of carrier density, N, can be approximated by [2], [7]

$$g \approx a\left(N - N_{tr}\right) \tag{2.12}$$

where a is the differential gain, $\partial g/\partial N$, and N_{tr} is a transparency carrier density where the gain is zero. Keep in mind that (2.12) is a limited range approximation for gain and a logarithmic function fits the gain better over a wider range of carrier densities.

Carrier density can also be written as a function of injected current density, J, [2]

$$N = \frac{\tau \eta_i}{qd} J \tag{2.13}$$

where τ is the carrier lifetime, q is the electron charge, d is the active region thickness, and η_i is the internal quantum efficiency which is the ratio of carriers generated in the active region over the injected current into the laser. Now we can combine (2.11)-(2.13) to find a simple equation for threshold current density, J_{th}.

$$J_{th} = \frac{qd}{\tau \eta_i}\left[N_{tr} + \frac{1}{a\Gamma}(\alpha_i + \frac{1}{2L} ln \frac{1}{R_1 R_2}) \right] \tag{2.14}$$

Now let's go back to our argument about using heterostructure to improve laser performance. As seen from (2.14), threshold current density is one of the parameters proportional to the active region thickness. If we can somehow decrease the active region thickness, the threshold current density would decrease as well. In the case of homostructure lasers, active region thickness is the distance traveled by a conduction electron from n-type to p-type region before recombining with a hole and can be ~1 μm for a typical GaAs homostructure (Figure 2.10(a)). Therefore, in this case there is no control on decreasing the active layer thickness. A better way to reduce the active layer thickness is using a layer with smaller bandgap energy than n- and p-type cladding layers as an active region. Carriers are confined and then recombine in the smaller bandgap region while surrounding higher bandgap materials act as barriers to block carrier flow. The resultant structure is called a heterostructure. As in Figure 2.10(b), for example, a

heterostructure can be realized by inserting a layer of InGaAs to a GaAs homostructure introduced in Figure 2.10(a). In this case, the active region thickness is basically the thickness of the low bandgap layer which can be well controlled during the growth and can be kept even smaller than 100 nm. Nowadays, these well-controlled thin layers of semiconductors can easily be grown by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) systems with very precise in situ thickness monitoring. Significantly increased excess carriers in the structure in Figure 2.10(b) will also shorten the radiative recombination lifetime and lead to a more efficient radiative recombination [8].

Heterostructures might be categorized as single heterostructures and double heterostructures depending on using one or two blocking layers. Double heterostructures provide an optical waveguide for the laser field, resulting in a higher optical confinement factor. Wider bandgap materials as cladding (blocking) layers also reduce the optical losses because blocking layers are transparent to the laser field generated in the smaller bandgap active region. The active region is usually undoped to achieve high radiation efficiency, while doping the active region causes recombination of injected carriers in the active region which decreases the carrier lifetime and increases the laser modulation frequency.

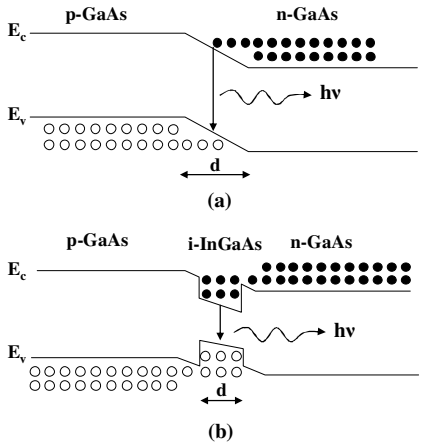

Figure 2.10 Band structure of (a) a homostructure, and (b) a heterostructure (Reproduced from [8]).

If we shrink the thickness of the lower bandgap region down to less than 100 nm, we form a quantum well (QW) structure which is frequently used in semiconductor lasers such as VCSELs. QW structures offer advantages such as more gain per injected carriers than conventional active regions. They also deliver gain with less change in refractive index than bulk lasers, resulting in lower chirp [9]. As described earlier, confinement factor is proportional to the active region volume occupied by gain, V_g ($\Gamma = V_g/V_p$). That means decreasing the active region thickness reduces Γ and according to (2.14) increases the threshold current density of the laser. Therefore, in order to obtain larger Γ, we can add several QWs to the active region and make a multiple quantum well structure (MQW). Replacing a single QW (SQW) with a MQW active region enhances Γ in the optical confinement region. However increasing the number of QWs in the active region lowers the carrier injection efficiency due to the lack of uniform carrier distribution over each well because of energy barriers of adjacent QWs [3]. The number of QWs in lasers

is always a parameter that needs to be carefully chosen in the laser design in order to balance the VCSEL behavior.

If QWs are grown in a way that both barrier and well materials have equal lattice constant, *a*, the QW is called unstrained. Otherwise, if barrier and well materials are lattice mismatched, the QW is under strain and called a strained QW. Too much lattice constant mismatch between barrier and well layers is not appropriate since that might cause undesirable defects in the structure. However, in some cases it is useful to grow strained QWs with a small lattice mismatch ($\Delta a/a$ ~1%). In a strained QW with the barrier material much thicker than the well material, the well material will be under compressive (tensile) strain if the barrier material has smaller (larger) lattice constant than the well layer. As an example in Figure 2.11, $Al_xGa_{1-x}As$/GaAs system makes an unstrained QW, while GaAs/$In_xGa_{1-x}As$ QW (small x) is a strained one with the well material (InGaAs) under compressive strain.

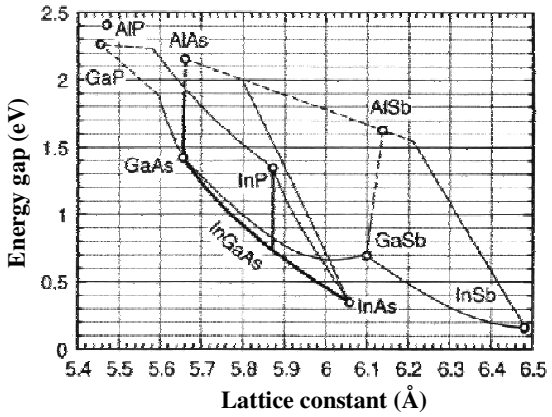

Figure 2.11 Energy gap vs. lattice constant for some III-V semiconductors (reproduced from [2]).

Strained QWs are interesting in some semiconductor laser applications because of offering some useful properties such as [10]: 1) a wider range of material combinations and thus bandgaps are available, and 2) they allow a certain amount of band structure and hence gain engineering with modifying effective masses. These properties made strained QWs very popular in VCSEL research and technology.

2.5. Current and optical confinement in VCSELs

In order to reach very efficient VCSELs, we need to confine both current and optical field in lateral dimension in a way to have maximum interaction with the active region. Optical field can be confined by either gain-guided or index-guided structures. In a gain-guided laser, the lateral extent of the laser field is controlled by the lateral size of the active region interacting with the field, while for an index-guided laser it is determined by the lateral size of the high refractive index region in a waveguide type configuration. Figure 2.12 shows two important techniques widely used in VCSELs, which are proton-implants for current confinement and oxide for both current and optical confinement. In proton implant which can be considered as a type of gain guided structure (Figure 2.12(a)), an insulating layer is formed by proton (H^+) bombardment of the structure to limit the current spreading toward the surrounding area. This method was initially very popular for fabricating commercial VCSELs. The oxide-confined structure (Figure 2.12(b)) is another popular configuration of electrical and optical confinement in VCSELs. In oxide confined VCSELs, an Al-containing layer such as AlGaAs is placed in the structure during the growth of DBR mirrors and active layer. Wet oxidation of this layer at elevated temperature forms a mechanically stable phase of Al_2O_3 which has a low

refractive index [11]. By etching laser mesas to access the AlGaAs layer from the side or bottom of the mesa, we can oxidize the oxide layer up to a certain length which should not exceed the mesa radius. In this case, the center of the mesa, which is unoxidized, has higher refractive index than the oxidized parts and acts as a index-guiding structure. One common method of oxidation is using a flow of water vapor in vicinity of the sample at elevated temperatures. The rate of oxidation can be well-controlled by changing the Al content, oxidation layer thickness, and water vapor and sample temperature [11]. Very high modulation frequency [12] and high efficiency VCSELs [13] have been made from this method.

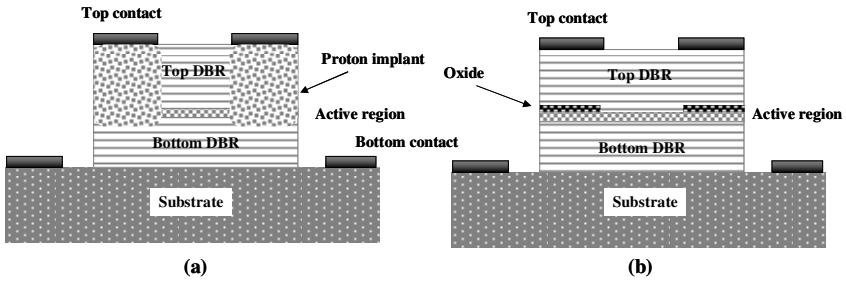

Figure 2.12 VCSEL confinement by (a) proton implantation and (b) selective oxidation.

2.6. VCSELs: dc and ac response

In this section the rate equations for carrier density in the active region and photon density of an optical mode are employed as a starting point to study semiconductor lasers under dc and ac conditions. Analyzing these two conditions enables us to understand laser dynamics which is a key point of designing lasers with desired operating parameters. The discussion in this section will be applicable to both EELs and VCSELs.

The rate equations under steady-state give us the full understanding of laser behavior under dc bias. For ac analysis, the rate equations can be solved and linearized in the presence of a perturbation, like a modulated input current to yield the small-signal modulation response of a laser. In addition to dc and modulation response, relative intensity noise (RIN) measurement of lasers can help us to find laser dynamics under dc bias such as the experimental data presented in Chapter 6. The use of this technique rather than current modulation response reduces nonlinear large signal effects, simplifies electrical probing requirements, and eliminates convolution with electrical effects due to parasitic circuit elements and impedance matching.

I first start with a steady-state solution in section 2.6.1 and then discuss modulation response and RIN measurement of semiconductor lasers in 2.6.2 and 2.6.3 respectively.

2.6.1. VCSELs under dc condition

Let's start from rate equations for carrier decay, *dN/dt*, and photon decay, *dS/dt*. *dN/dt* can be written as subtracting carrier recombination rate from carrier generation rate. The same logic can be used to write the rate equation for *dS/dt.* These equations can be written as [2]

$$\frac{dN}{dt} = \frac{\eta_i I}{qV_g} - \frac{N}{\tau} - v_g gS \tag{2.15}$$

$$\frac{dS}{dt} = \Gamma v_g gS + \Gamma \beta_{sp} R_{sp} - \frac{S}{\tau_p} \tag{2.16}$$

where I is the injected current, v_g is the photon group velocity, S is photon density, β_{sp} is the spontaneous emission factor, R_{sp} is the spontaneous recombination rate and τ_p is the photon lifetime.

It is important to know that the steady-state gain for a laser operating above threshold should always equal the threshold gain because if the gain is higher than g_{th}, optical field amplitude continues to increase and obviously this cannot happen in the steady-state. The same argument is valid for steady-state carrier density above threshold because as mentioned earlier, N is monotonically related to g. So in a laser cavity both g and N clamp at steady-state as [2]

$$g(I > I_{th}) = g_{th} \tag{2.17}$$

$$N(I > I_{th}) = N_{th} \tag{2.18}$$

Now we have all we need to find the output power of a laser. Laser output power, P_{out}, can be written as

P_{out}=(Energy of each photon)×(Number of photons in the optical mode)×(Photon escape rate from mirrors)

or

$$P_{out} = h\upsilon.SV_p.v_g\alpha_m \tag{2.19}$$

where h is Planck's constant and υ is the frequency of each photon. Now let's consider the steady-state situation (dN/dt=0) almost at threshold (N=N_{th} and I=I_{th}). In this case (2.15) reduces to

$$\frac{\eta_i I_{th}}{qV_g} = \frac{N_{th}}{\tau} \tag{2.20}$$

Also note that for a laser right below threshold, the net stimulated recombination is negligible, i.e $R_{st}=v_g g S \approx 0$.

If again we consider the steady-state but at $I>I_{th}$ and use (2.17), (2.18), and (2.20), (2.15) can be written as

$$\frac{\eta_i}{qV_g}(I-I_{th}) = \nu_g g_{th} S \Rightarrow S = \frac{\eta_i}{qV_g \nu_g g_{th}}(I-I_{th}) \tag{2.21}$$

Substituting S from (2.21) into the output power expression (2.18) with $V_p=V_g/\Gamma$, one can write output power for $I>I_{th}$ in the form of

$$\begin{aligned} P_{out} &= h\upsilon . \frac{\eta_i}{qV_g \nu_g g_{th}}(I-I_{th})\frac{V_g}{\Gamma}.v_g \alpha_m \\ \Rightarrow P_{out} &= \frac{h\upsilon \eta_i \alpha_m}{q\Gamma g_{th}}(I-I_{th}) \end{aligned} \tag{2.22}$$

or using (2.3) and (2.4) for Γg_{th}

$$P_{out} = \frac{h\upsilon}{q}\frac{\eta_i \alpha_m}{\alpha_i + \alpha_m}(I-I_{th}) \tag{2.23}$$

Now with defining a differential quantum efficiency, η_d

$$\eta_d = \eta_i \frac{\alpha_m}{\alpha_i + \alpha_m} \tag{2.24}$$

we can simplify (2.23) to be

$$P_{out} = \eta_d \frac{h\upsilon}{q}(I-I_{th}) \tag{2.25}$$

As mentioned before, these equations give P_{out} for $I>I_{th}$; so, we still need to find P_{out} at $I<I_{th}$ where spontaneous emission is the dominant process. It means that we can piece together a below-threshold LED curve with (2.25) to reach a P_{out} vs. I characteristic for a

semiconductor laser. Output power in an LED is a linear function of input current and can be formulated as [2]

$$P_{out,LED} = \eta_{ex} \frac{h\upsilon}{q} I \tag{2.26}$$

where η_{ex} is the external LED quantum efficiency which is the number of photons coupled to the receiving aperture per electron flowing into the LED [2]. Both parts of the laser characteristic are linear functions of current with different slopes. Figure 2.13 shows a typical P_{out} vs. I characteristic in solid line. In VCSELs due to the generated heat in the small active region, P_{out} cannot increase monotonically with I and a thermal roll-over causes the power to decrease at large amount of currents which differs from VCSEL to VCSEL. This phenomenon is presented in Figure 2.13 with a dotted curve. Methods of cooling down the active region temperature will be presented in later chapters.

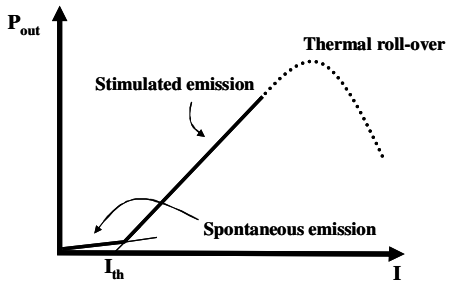

Figure 2.13 Output power vs. current characteristic of a VCSEL.

2.6.2. VCSELs modulation response

After solving rate equations under steady-state condition, let's derive small-signal intensity modulation of lasers which is a very important concept in optical communications. Consider an above-threshold dc operation of a diode laser, I_0, superimposed with a small sinusoidal ac current with amplitude I_1. In this case carrier and

photon density can also be considered to have the same form as current under an assumption of linearity. So,

$$\begin{aligned} I &= I_0 + I_1 e^{j\omega t} \\ N &= N_0 + N_1 e^{j\omega t} \\ S &= S_0 + S_1 e^{j\omega t} \end{aligned} \tag{2.27}$$

Now with substituting (2.27) into the rate equations ((2.15) and (2.16)) and let dc terms cancel out from both sides of the equation in steady-state, we find small signal rate equations

$$j\omega N_1 = \frac{\eta_i I_1}{qV_g} - \frac{N_1}{\tau} - \frac{S_1}{\Gamma \tau_p} - v_g a N_1 S_0 \tag{2.28}$$

$$j\omega S_1 = \Gamma v_g a N_1 S_0 \tag{2.29}$$

In getting to these equations we used $g_{th}=a(N_0-N_{tr})$ and also photon decay rate $1/\tau_p=\Gamma g_{th} v_g$. In order to find frequency response of a diode laser we can define its modulation transfer function as a ratio of ac optical power over input current, i.e. $P_{ac}(\omega)/I_1(\omega)$ where P_{ac} is proportional to S_1 as illustrated in (2.19) for a general case. Using (2.28) and (2.29) we can find S_1 to be

$$S_1 = \frac{(\eta_i I_1 / qV_g)\Gamma v_g a S_0}{R(\omega)} \tag{2.30}$$

where frequency dependent denominator $R(\omega)$ is

$$R(\omega) = -\omega^2 + j\omega\left(\frac{1}{\tau} + v_g a S_0\right) + \frac{v_g a S_0}{\tau_p} \tag{2.31}$$

To have the maximum photon density for maximum power, $|R(\omega)|$ should have its minimum value which occurs at $\omega=\omega_r$ when $(\partial/\partial\omega)|R(\omega)|^2=0$.

$$\omega_r{}^2 = \frac{v_g a S_0}{\tau_p} - \frac{1}{2}\left(\frac{1}{\tau} + v_g a S_0\right)^2 \tag{2.32}$$

where the last term is usually negligible compared to the first term and

$$\omega_r{}^2 \approx \frac{v_g a S_0}{\tau_p} \tag{2.33}$$

This natural resonance frequency, ω_r, is referred to as the relaxation oscillation frequency and plays an important role in understanding the high frequency behavior and dynamics of diode lasers. Now we can write the modulation transfer function of a diode laser as a function of ω_r and other known parameters.

$$\frac{P_{ac}(\omega)}{I_1(\omega)} = \frac{\eta_d (h\upsilon/q)\omega_r{}^2}{-\omega^2 + \omega_r{}^2 + j\omega\left(\frac{1}{\tau} + \tau_p \omega_r{}^2\right)} \tag{2.34}$$

The first thing from (2.34) is that the laser transfer function is much like a second-order low-pass filter response with a resonance frequency and damping factor. When the damping is small, the electrical 3 dB frequency, in which electrical power reaches to half of its dc value, is given by $\omega_{3dB} = \omega_r\sqrt{1+\sqrt{2}} \approx 1.55\omega_r$. In this case optical power reaches to $\sqrt{1/2}$ of its dc value. Using (2.19) and (2.33) we can express ω_{3dB} as a function of output power with small damping.

$$\omega_{3dB} = 1.55\sqrt{\frac{\eta_i}{\eta_d}\frac{\Gamma a v_g}{h\upsilon V_g}}\sqrt{P_{out}} \tag{2.35}$$

It might also be convenient to write (2.34) as a function of input current using (2.25) and again under small damping condition. We have

$$\omega_{3dB} = 1.55\sqrt{\frac{\eta_i \Gamma a v_g}{q V_g}}\sqrt{I - I_{th}} \tag{2.36}$$

The small-signal modulation response discussed up to this point was under some conditions to simplify the problem. More accurate analysis might be performed with considering nonlinear gain saturation as well as carrier transport effects [2]. Without going through the details of this case, let's first define gain compression factor, ε, and a transport factor, χ. A more accurate gain equation can be written for $g \geq 0$ as [2]

$$g(N,S) = \frac{g_0}{1+\varepsilon S} ln(\frac{N}{N_{tr}}) \tag{2.37}$$

where g_0 is a gain coefficient. From (2.36) the differential gain is

$$a = \frac{\partial g}{\partial N} = \frac{g_0}{N(1+\varepsilon S)} \equiv \frac{a_0}{1+\varepsilon S} \tag{2.38}$$

We can also define

$$a_p = -\frac{\partial g}{\partial S} = \frac{\varepsilon g}{1+\varepsilon S} \tag{2.39}$$

Now let's go back to a normalized general form of a diode laser modulation transfer function, $H(\omega)$ with relaxation resonance frequency, ω_r and damping factor, γ.

$$H(\omega) = \frac{{\omega_r}^2}{{\omega_r}^2 - \omega^2 + j\omega\gamma} \tag{2.40}$$

In Figure 2.14, magnitude squared of the transfer function, $H(\omega)$ is plotted with increasing relaxation oscillation frequency and damping factor as a function of ω. The 3 dB angular frequency is also shown for each curve. Both relaxation oscillation frequency and damping factor increase with increasing the laser bias current.

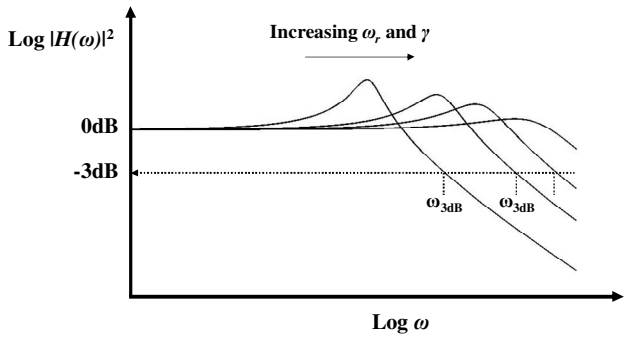

Figure 2.14 Modulation transfer function for varying values of relaxation oscillation frequency and damping.

Skipping all details, the damping factor when accounting for both gain suppression and transport effects can be expressed as

$$\gamma = Kf_r^{\,2} + \gamma_0 \tag{2.41}$$

where

$$K = 4\pi^2\tau_p\left(1+\frac{\Gamma a_p}{a/\chi}\right) \qquad \text{and} \qquad \gamma_0 = \frac{1}{\tau_{\Delta N}\chi} + \frac{\Gamma\beta_{sp}R_{sp}}{S} \tag{2.42}$$

and $\tau_{\Delta N}$ is the differential carrier lifetime that is typically smaller than τ by a factor of 2-3 [2].

From (2.40) and (2.41) with neglecting γ_0, one can find that the maximum possible 3 dB frequency occurs when $2\omega_r^{\,2}=\gamma^2=K^2f_r^{\,4}$. Therefore,

$$f_{3dB,max} = \frac{2\pi\sqrt{2}}{K} \tag{2.43}$$

Notice that ω_r approximated by (2.33) is still valid in this case.

In practice, parameters ω_r and γ can be extracted from fitting the measured frequency response data to the theoretical $|H(\omega)|^2$ equation. These two parameters can be

easily altered by changing some laser dynamics introduced earlier in this section. Dynamics can also be affected by changing the external laser parameters such as bias current and temperature. This argument leads us to determining the damping coefficient at threshold, γ_0 and the damping parameter, K from fitting (2.41) with the γ vs. f_r data extracted from frequency response measurement at different laser bias current or temperature to (2.41).

2.6.3. Relative intensity noise (RIN)

In the previous section we considered frequency response due to the current modulation. In steady-state it is assumed that carrier and photon densities are constant. However, in reality random carrier and photon recombination and generation produce instantaneous time variations in the carrier and photon densities even with applied dc current [2]. Fluctuations in photon density give rise to the variations in the magnitude of the output power that provides a noise floor and variations in carrier density lead to fluctuations in the output wavelength, which causes the spectrum of the lasing mode to broaden. The intensity noise in optical power contains information on laser relaxation oscillation frequency and damping factor that can be measured while just dc biasing the laser.

RIN is the ratio of the mean-square optical intensity noise, $<\delta P(t)^2>$ to the square of the average optical power, P_0.

$$RIN \equiv \frac{<\delta P(t)^2>}{P_0^2} \tag{2.44}$$

With further simplifications, the RIN spectral density can also be written as [2]

$$\frac{RIN}{\Delta f} = \frac{2h\upsilon}{P_0}\left[\frac{a_1 + a_2\omega^2}{\omega_r{}^4}\left|H(\omega)\right|^2 + 1\right] \tag{2.45}$$

where Δf is the filter bandwidth of the measurement apparatus and a_1 and a_2 are frequency coefficients [2]. It is usually more convenient to express RIN in [dB/Hz] as in (2.45). This equation can be further simplified by introducing new frequency coefficients A and B and using (2.40) for $H(\omega)$.

$$\frac{RIN}{\Delta f} = \frac{A + B\omega^2}{(\omega_r{}^2 - \omega^2)^2 + \omega^2\gamma^2} \tag{2.46}$$

RIN measurement offers another method for extracting parameters ω_r and γ from fitting (2.46) to the RIN data. RIN can be measured under dc current bias using a spectrum analyzer (SA) system, while for modulation response measurement a modulated current must be added to the laser dc bias current and then the output response must be measured. A vector network analyzer (VNA) is a system that offers both ports for applying and measuring ac signal and measuring the output changes. It is obvious that a photodetector is needed to convert optical signal from the laser to the electrical signal used in both SA and VNA. Calibration requirement in VNAs before measurement and dealing with ac signals make this type of measurement more complicated than SA systems that operate without any involved ac signal and any need for calibration. Also, there are electrical parasitics such as packaging that influence VNA measurement, but not RIN measurement.

2.7. Thermal properties of VCSELs

Temperature sensitivity of VCSELs is related to their structure and thermal conductivity of the constituent materials. For an instance, shallower quantum wells (QWs) in red VCSELs cause a weaker carrier confinement and thus greater over-barrier leakage than larger bandgap contrast QW VCSELs. Lower thermal conductivity of materials used in red VCSEL's QWs and DBR mirrors is another drawback to achieving high thermal performance red VCSELs. Therefore, understanding which VCSEL parameters can be altered by elevated temperatures and how temperature affects those parameters are of great importance in designing high temperature performance VCSELs.

2.7.1. Temperature effects on VCSEL operation

VCSELs parameters such as lasing wavelength, threshold current, output power, and modulation bandwidth can be affected by device operating temperature. The remainder of this section focuses on the effects of temperature on the above mentioned parameters.

Temperature dependence of longitudinal mode of a VCSEL with longitudinal mode wavelength of λ_M and cavity refractive index of n_R can be expressed as [14]

$$\frac{d\lambda_M}{dT} = \frac{\lambda_M}{n_G}\left[\left(\frac{\partial n_R}{\partial T}\right)\bigg|_{\lambda} + n_R\alpha_T\right] \tag{2.47}$$

where α_T is the linear coefficient of thermal expansion and n_G is the group index given by

$$n_G = n_R - \lambda_M\left(\frac{\partial n_R}{\partial T}\right)\bigg|_T \tag{2.48}$$

For an instance, in a GaAs resonance cavity with lasing wavelength of 850 nm, α_T of 6.4×10^{-6}/˚C [15], n_R of 3.63 [16], n_G of 4.3, and $(\partial n_R / \partial T)\big|_\lambda = 4\times10^{-4}$ K^{-1} [14], the rate of longitudinal mode wavelength change with temperature may be estimated from Equation (2.47) to be 0.84 Å/˚C. Rate of refractive index change with temperature is about an order of magnitude greater than product of refractive index and coefficient of thermal expansion; therefore, temperature dependence of longitudinal mode is mainly determined by the temperature dependence of refractive index.

Another important parameter in VCSELs that is a function of temperature is threshold current which is determined by the balance between optical gain and losses. Two important effects of increasing temperature in III-V semiconductors are energy gap shrinkage and broadening the carrier density distribution within each band and shifting its peak further into the band. Although these two factors have opposing effects, the energy gap shrinkage is dominant and thus at elevated temperatures, the gain peak shifts to the longer wavelengths and it is also lowered at a given carrier concentration. A typical value for the shift of gain spectrum with temperature in VCSELs is 3.3 Å/˚C reported by R. S. Geels et al. for InGaAs MQWs [17]. If optical losses remain unchanged, because of higher current density required to maintain the same gain level, threshold current would increase with temperature. Moreover, since higher density of carriers needed to retain the required gain level, optical losses increase with temperature resulting in increased free carrier absorption in the active region [14]. An Arrhenius-type relation given below is commonly employed to express the temperature dependence of threshold current in semiconductor lasers.

$$I_{th}(T) = I_{th}(300K)e^{(T-300K)/T_0} \tag{2.49}$$

Characteristic temperature, T_0 is a parameter describing temperature sensitivity of the threshold current and T is the operating temperature in Kelvin. Higher T_0 is favorable for having a device with constant I_{th} over a certain range of temperature. Although this relation is widely used for EELs, it is not very applicable to VCSELs. When the spacing between longitudinal modes in the resonance cavity is small, the lasing wavelength is determined by the peak of the gain spectrum and thus the operating wavelength follows the gain peak shift with temperature. In contrast, in lasers with a large longitudinal mode spacing, such as VCSELs, the lasing wavelength follows the longitudinal mode shift with temperature. Since the rates of gain peak and cavity mode shift with temperature are different (several times), detuning of cavity mode wavelength with respect to the gain peak varies at different temperatures. This is another factor that results in the temperature dependence of threshold current in VCSELs. VCSELs operate at minimum threshold current at temperatures where the cavity mode and gain peak are relatively aligned. Any nonzero gain-mode offset results in a larger threshold current. Therefore, engineering the gain-mode offset at room temperature is very critical in achieving VCSELs with desired characteristics. For example, designing a VCSEL with a negative gain mode offset at room temperature (i.e. gain peak being blue shifted with respect to the cavity mode wavelength) is favorable for high temperature operation, while a small positive gain-mode offset is important for reaching higher bandwidths in VCSELs.

According to Equation (2.18), laser output power is proportional to the number of photons in the cavity, energy of each photon, and escape rate from the mirrors. Laser power varies with temperature mainly due to the reduced number of photons in the cavity

at elevated temperatures. Reduction in internal quantum efficiency is the main effect responsible for the photon density decrease in the active region at high temperatures.

Modulation frequency is another temperature dependent parameter in VCSELs. The 3 dB angular frequency given in Equation (2.35) is related to the output power that varies with temperature as explained above. The frequency might also be temperature dependent through differential gain. Other parameters in the equation are either expected to be relatively constant with temperature or appear as the ratios, e.g., η_i/η_d, that are relatively constant.

2.7.2. Material thermal conductivity and laser thermal resistance

Different types of carriers contributing to the thermal conductivity, *K*, in semiconductors are phonons, photons, electron-hole pairs, and separate electrons and holes [18]. Phonons are the major carriers responsible for heat conduction in relatively pure semiconductors at low temperatures (<600K). Adding a large number of foreign atoms in a semiconductor increases the phonon scattering rate and thus decreases thermal conductivity due to the anharmonicity caused by mass difference between the host lattice and added atom [18]. This concept is more or less what happens in a ternary compound semiconductor. In the $A_xB_{1-x}C$ compound semiconductor, random distribution of A and B atoms in sublattice sites causes the thermal conductivity to deviate from the linear relation with the mole fraction of one compound x. In this case thermal resistivity, $W=1/K$, of the ternary material can be written as

$$W(x) = xW_{AC} + (1-x)W_{BC} + x(1-x)C_{A-B} \tag{2.50}$$

where W_{AC} and W_{BC} correspond the thermal resistivity of AC and BC binary compounds and $C_{A\text{-}B}$ is a factor arising from the anharmonicity in the ternary material and can be expressed as [19]

$$C_{A-B} = \left[\frac{\sqrt{2\pi}}{3} \frac{e\hbar^4 N_{dl}}{(kT)^{1/2}(m_h)^{5/2}(\Delta U_h)^2} \right] \tag{2.51}$$

where N_{dl} is the density of alloy sites, m_h is the hole effective mass, and ΔU_h is the alloy scattering potential. Thermal resistivities of some common binary and ternary compound semiconductors together with some useful bowing parameters, $C_{A\text{-}B}$ are given in Table 1 [19].

Table 2.1 Thermal resistivity and bowing parameter for some common compound semiconductors [15], [19].

Material	***W*** ***(cm K/W)***	$\mathbf{C_{A\text{-}B}}$ ***(cm K/W)***
AlAs	1.10	
AlP	1.1	
GaAs	2.22	
GaP	1.3	
InAs	3.7	
InP	1.47	
$Al_xIn_{1-x}P$	$1.47+14.63x-15x^2$ [(a)]	$C_{Al\text{-}In}=15$
$Al_xGa_{1-x}As$	$2.27+28.83x-30x^2$	$C_{Al\text{-}Ga}=32$
$Ga_xIn_{1-x}P$	$1.47+71.83x-72x^2$ [(a)]	$C_{Ga\text{-}In}=72$
$In_xGa_{1-x}As$	$2.27+73.43x-72x^2$ [(a)]	

[(a)] Estimated from Equation (2.50)

For many well-known ternary semiconductor compounds the maximum thermal resistivity occurs at mole fractions around x=0.5 [19].

In the $A_xB_{1-x}C_yD_{1-y}$ quaternary semiconductor alloy, in addition to considering A-B and C-D disorder due to random distribution of A and B atoms in the cationic and C and D atoms in the anionic sublattices, disordering the cationic and anionic sublattices

also need to be taken into account [20]. These additional alloy scattering terms in quaternary compounds make them to generally have greater thermal resistance than ternary and binary compound semiconductors.

Thermal resistance, R_{th} (in ˚C/W), which is a useful parameter for describing VCSEL heating is defined by the ratio of active region temperature raise, ΔT and dissipated thermal power, ΔP_{heat}, and is given by [21], [22]

$$R_{th} = \frac{\Delta T}{\Delta P_{heat}} \tag{2.52}$$

where $P_{heat}=IV-P_{opt}$ and I, V, and P_{opt} are CW current, voltage, and output optical power, respectively.

In experiment, (2.52) can be expanded and R_{th} can be found as $R_{th}=(\Delta\lambda/\Delta P_{heat})/(\Delta\lambda/\Delta T)$ which requires two sets of measurements i.e., wavelength shift with dissipated power and wavelength shift with temperature. $\Delta\lambda/\Delta T$ can be measured by biasing the VCSEL at a fixed current, while changing the stage temperature and monitoring the laser operating wavelength at each temperature. The VCSEL was in the air during the measurement and it is assumed that $\Delta T_{stage}=\Delta T_{device}$. The slope of the linear fit to the λ vs. T data gives $\Delta\lambda/\Delta T$ that can be measured once for a grown epitaxial wafer and used for all VCSELs made on that same material. To find the $\Delta\lambda/\Delta P_{heat}$, different bias currents are applied to the VCSEL under test and electrical voltage, optical power, and wavelength for each case are measured. The slope of resultant λ vs. P_{heat} for each VCSEL gives the $\Delta\lambda/\Delta P_{heat}$ for that specific laser and dividing that number by $\Delta\lambda/\Delta T$ gives the thermal resistance of the VCSEL.

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Chapter 3

VCSELS: THEIR BIRTH TO RECENT DEVELOPMENTS

3.1. Historical overview of surface emitting lasers (SELs)

Surface emitting lasers (SELs) were first invented in 1977 by Kenichi Iga of Tokyo Institute of technology [1]. He proposed the initial idea in 1978 at a conference while the first lasing operation of a SEL was reported by him and his colleagues in 1979 based on a GaInAsP/InP double-heterostructure (DH) [2]. The structure contained a stack of an n-type InP layer, an undoped GaInAsP active layer, and a p-type InP layer that were grown on a n-type InP substrate by the liquid phase epitaxy (LPE) technique. They employed metal coated top and bottom surfaces to form a resonant cavity. The laser driven by current pulses at 77 K showed a threshold current density of 11 kA/cm^2 (~0.9 A) and operating wavelength of 1.18 μm. Z. L. Liau and J. N. Walpole developed a room temperature continuous wave (CW) low threshold current, I_{th}=12 mA and high differential quantum efficiency, η_d=47% surface-emitting GaInAsP/InP laser in Lincoln Laboratory, MIT, in 1985, while they mounted the laser on a copper substrate as a heatsink [3]. The next step in realizing a low threshold current SEL happened in 1987 in which the first demonstration of a microcavity GaAlAs/GaAs SEL operating at 880 nm was reported with η_d=9%, I_{th}=4.5 and 6 mA at 77 K for CW and pulsed operation, respectively [4].

Detailed lasing characteristics of the first room-temperature CW lasing of AlGaAs/GaAs VCSELs with I_{th}=36 mA operating at 895 nm was reported in 1989 where a copper bonding heatsink was employed to reduce the thermal resistance for CW operation [5]. Since low threshold currents would reduce voltage drop and heat generation, in the same year, J. L. Jewell of AT&T Bell Labs and his colleagues reported on a room temperature low pulsed current threshold VCSEL with I_{th}=1.3 mA and 958 nm output wavelength [6]. This VCSEL which is the most similar to today's designs contained three 8 nm $Ga_{0.8}In_{0.2}As$ quantum wells with four 10 nm GaAs barriers in between. Quarter-wave AlAs and GaAs stacks were used to form 12 pairs Be-doped top and 20 pairs Si-doped bottom mirrors. Use of size-quantized heterostructures (quantum wells, wires, and dots) in lasers is beneficial for increasing the relative density of states for charge carriers near the band edges, or equivalently decreasing the density of states for carriers further from the band edges. When one of these heterostructures is employed as an active region of a laser, most of the injected nonequilibrium carriers concentrate in an increasingly narrow energy range near the bottom of the conduction band and/or top of the valence band. This leads to the enhanced material gain and reduced temperature sensitivity of the device [7].

In addition to improving the active region structure, employing high reflectivity mirrors i.e. >99% is also a key factor for submilliampere threshold and high differential efficiency VCSEL operation. Distributed Bragg reflectors (DBR) were found to be promising reflectors in VCSELs. DBRs consist of repeating pairs of high and low refractive index layers with quarter-wave thickness that can be formed either from semiconductors or dielectric materials. These types of mirrors offer a very high

reflectivity exceeding 99.9% as well as a frequency selective optical filter for single mode operation.

VCSELs became one of the hot research topics in the beginning of the 90s and different aspects of this important light source have been well studied and addressed by researchers before 1993. These developments will be briefly elucidated in the remainder of this chapter.

Different groups employed DBR mirrors in VCSELs and also worked on improving DBRs and their effects on reducing the operating voltage due to reduction in electrical series resistance as well as the threshold current [8-16]. In order to further improve the laser performance, use of multiple quantum-well (MQW) active region in VCSELs were reported for AlGaAs/GaAs [17] and InGaAs/GaAs [6]. Quantum-well (QW) structures, which were first proposed in 1972 by Charles H. Henry of Bell Laboratories, are formed with sandwiching a thin layer (several tens of nm) of low energy gap semiconductor with thin layers of two higher energy gap semiconductor. These structures introduce attractive properties such as high gain and high relaxation oscillation frequency in VCSELs.

Capability of wavelength tuning and multiplexing is very important in optical communications and optical interconnects. Multiple wavelength tunable VCSELs by using a three-mirror coupled-cavity configuration was introduced for the first time by C. J. Chang-Hasnain and her colleagues in 1991 [18]. Using this method, a full tuning range of 6.1 nm occurs with 10.5 mA variation in the driving current.

In 1991, an attempt to demonstrate the first mode-locked GaAs VCSEL occurred in Prof. John Bowers' group at UCSB [19]. This external cavity, optically pumped VCSEL

which employed a 120 GaAs/$Al_{0.29}Ga_{0.71}As$ MQW with 15 nm well and 5 nm barrier width, generated pulses with 324 fs width and 64 W peak power.

The first visible (657 nm) VCSEL operation based on InGaP/InAlGaP quantum well structure was first introduced by a group from Sandia National Laboratories in 1992 [20]. The optically pumped VCSEL consisted of 30 and 40 periods of AlAs/$Al_{0.5}Ga_{0.5}As$ top and bottom DBRs, respectively.

These great attempts made VCSELs very popular at that time period and opened a new perspective area for more research on improving the laser functionality and performance. Improving parameters such as modulation frequency, efficiency, optical power, single mode operation, thermal managing and, gain and differential gain have been topics for many articles to date.

In the next sections, I focus on two main aspects of VCSELs considered in this project, i.e. high directly modulated bandwidth as well as high optical power operation.

3.2. High modulation bandwidth VCSELs

Among all VCSEL advantages, their capability of having very high relaxation oscillation frequency and high direct modulation bandwidth is a key feature for using them in high data rate networks. It is noteworthy to mention that, today, VCSELs are also commercially available for standard >10 Gb/s datacom applications.

Laser intrinsic bandwidth, external parasitic circuit elements, thermal issues, and optical issues are the main limiting factors on VCSEL bandwidth [21]. Intrinsic bandwidth is given by laser relaxation oscillation frequency which is an indication of the interaction between photons and electronic carriers (electrons and holes) in

semiconductor lasers. Intrinsic bandwidth is the maximum achievable bandwidth with the absence of parasitic circuit limitations as discussed in Chapter 2. The laser itself has some parasitic circuit elements associated with its structure which prevents the entire external modulated signal from reaching the laser junction. Excessive junction temperature also causes a reduction in oscillation frequency due to decreased differential gain. Another bandwidth limiting factor is optical mode issues that appear in the case of multimode laser operation where the optical power is distributed among all existent modes and reduces the frequency response which is proportional to square root of optical power, $P^{1/2}$. Overcoming these limiting factors, one can achieve higher modulation bandwidth for VCSELs.

High speed modulation frequency (near 8 GHz) of top-emitting, 850 nm VCSELs based on QW active region was reported by F. S. Choa et al. in 1991 [22]. The structure employed 27.5 pairs of AlAs/$Al_{0.15}Ga_{0.85}As$ Si-doped n-type DBR and 20 periods of AlAs/$Al_{0.58}Ga_{0.42}As$/$Al_{0.16}Ga_{0.84}As$/$Al_{0.58}Ga_{0.42}As$ Be-doped p-type top DBR. The active region consisted of four 10 nm GaAs QWs separated by three 7 nm $Al_{0.3}Ga_{0.7}As$ barriers.

High-speed response of gain-guided VCSELs operating at 960 nm and 780 nm is reported in 1993 by a group at Colorado State University (CSU) and a Broomfield company, Bandgap Technology [23]. The corresponding modulation bandwidths for these two wavelengths of proton implanted devices were 9.75 GHz and 14 GHz. Although the 960 nm device was taking advantage of strained InGaAs/GaAs quantum wells, the 780 nm unstrained AlGaAs/GaAs VCSEL showed a higher modulation bandwidth. The intrinsic bandwidth of >50 GHz, which is surprisingly higher than for the faster 780 nm laser, was estimated for the 960 nm VCSEL; however, a high intrinsic

resonance frequency of >70 GHz has already been published in 1992 for a 960 nm VCSEL with InGaAs/GaAs quantum well active region using relative intensity noise (RIN) measurement [24]. The RIN of a semiconductor laser is defined as the mean square fluctuation in the photodetector current, normalized to the DC current and is a very powerful method for understanding laser dynamics as described in Chapter 2.

Dr. Kevin Lear and his colleagues at Sandia National Laboratories demonstrated the first high speed modulation response of 21.5 GHz for oxide-confined 850 nm VCSELs [25]. Proton implantation along with the oxidation layer decreased the mesa capacitance and thus increased the bandwidth with increasing the implant dose. The reported VCSELs utilized an inverted polarity structure, i.e. p-type substrate and bottom mirror and n-type upper mirror above the active region in order to reduce series resistance and improve single mode operation by decreasing current crowding effects. Reduced series resistance is due to the high electron mobility and thus lateral conductivity of the n-type top mirror [26]. Reported frequency response in this work remained the highest directly modulated response for several years.

Top emitting polyimide-planarized oxide-confined 850 nm VCSEL with 17 GHz modulation bandwidth was reported [27]. Surrounding mesas with a low dielectric constant polyimide reduced interconnect and pad capacitance. In addition to employing dielectric materials and mesa implantation, reduction of pad area and using semi-insulating substrates also decrease the capacitance. Another method for reducing the parasitic capacitance is using multiple deep oxidation layers by increasing the aluminum fraction in several first periods of the p-type top DBR. These deep oxidation layers which act as series capacitors to the oxide aperture reduced the total capacitance and so

increased the modulation bandwidth to 17.9 GHz [28]. This structure also employed AlAs followed by $Al_{0.82}Ga_{0.18}As$ in order to form a tapered oxide aperture. The lens-like aperture behavior improves the laser efficiency and decreases scattering losses as well [29]. Modulation bandwidth of >20 GHz with 35 Gbit/s operation has also been reported for 980 nm VCSELs by reducing the mesa and pad capacitance and employing a tapered oxide aperture [30] and [31]. In addition to all attempts towards high speed operation of 980 nm VCSELs, larger than 20 GHz small signal modulation bandwidth [32] and 40 Gbit/s error-free operation [33] of 850 nm oxide-confined VCSELs has been recently demonstrated. In the former work, the epitaxial design including doping and graded compositional profiles in DBRs was optimized for ultra-high speed operation. In the latter research, a double oxide aperture along with four layers of AlGaAs with 96% Al content above the two oxide layers were utilized to reduce the device capacitance. Furthermore, strained $In_{0.10}Ga_{0.90}As$ QWs rather than using the traditional GaAs QWs were employed to improve differential gain.

Improved device heatsinking also reduces the thermal resistance and consequently decreases the effect of high input current density on the junction temperature and modulation bandwidth. Before the work done at CSU on VCSEL heatsinking, electroplating of a Au layer was shown to decrease thermal resistivity by a factor of 2 with around 60% increase in output power [34]. A. Al-Omari and K. Lear at CSU investigated the effect of copper electroplated heatsinks on laser characteristics. Cu which offers lower cost and higher thermal conductivity than Au, reduced thermal resistance by 44%. 38% increase in output power and a 12% increase in modulation bandwidth was also reported for the 850 nm top emitting VCSEL [35]. In another work performed in

2006, VCSEL characteristics were shown to improve by increasing the Cu plated outside radii on VCSEL mesas [36].

In addition to mentioned proton implanted and oxide confined high modulation frequency lasers, high speed tunnel junction and quantum dot (QD) VCSELs have also been studied recently. One way to improve VCSEL performance is to remove the p-type spreading layer. This lateral hole conduction introduces large series resistance due to low hole mobility and therefore increases device threshold voltages and device heating. The high resistance p-type layer can be replaced with a reverse biased tunnel junction (TJ) in order to facilitate hole injection into the active region via a lateral electron current [37]. Buried tunnel junctions (BTJs) has been employed in InP-based long-wavelength VCSELs that suffer from some material related issues such as low thermal conductivity, low T_0, and low index contrast. Joule heating has been reduced by adding the TJ structure to a InGaAlAs long wavelength VCSEL [38]. Another work performed by the same group utilized a BTJ structure on the InGaAlAs-InP material system to reduce electrical and thermal resistances and enable CW operation of the 1830 nm wavelength VCSEL up to 90 ˚C [39]. A group from NEC Corporation in Japan realized up to 24 GHz modulation bandwidth for 1.09 μm wavelength tunnel junction VCSELs with proton implant region to reduce parasitic capacitance [40]. Tunnel junction of n-InGaAs/p-GaAsSb was formed above the active region and buried with an n-GaAs space layer. BTJ offers a lower resistance structure utilizing the low-resistance n-type spacer. Thermal resistance was also reduced by employing large mesa VCSELs. Recently, a short-cavity 1550 nm VCSEL based on BTJ is reported and shown to have frequency response of up to 15 GHz [41]. Improved bandwidth of the reported VCSEL was attributed to their better heat

management and the smaller intrinsic damping due to reduced photon lifetime. This VCSEL exhibit the optical power of 1 mW and 0.25 mW at room temperature and 90 ˚C, respectively.

Another important modification to the conventional VCSELs is using QD based active regions to achieve ultra-low threshold current density and increased material and differential gain [42]. High peak material gain is crucial for QD VCSELs because of the reduced volume of the gain medium in QD lasers compared to QW lasers. F. Hopfer et al. used the stacked submonolayer growth of QDs (SML QDs) as an alternative approach to QWs and Stranski-Krastanow grown QDs [43]. SML QDs can provide high modal gain to avoid gain saturation which is critical in high bandwidth VCSELs. Single-mode (SMSR>40 dB), 980 nm QD VCSELs reported in this paper showed a modulation bandwidth of 10.5 GHz at room temperature with the modulation current efficiency factor of 14 GHz/$(mA)^{1/2}$ for a 1 μm aperture device.

3.3. High power single VCSELs and arrays

Although VCSELs intrinsically have lower power than edge emitting lasers, many attempts are in progress to increase the output power of surface emitting lasers. High power VCSELs are suitable for a variety of applications such as laser based projection displays [44], short-range free-space optical communication [45], and light detection and ranging systems (LIDAR) [46]. Raising the output power by means of increasing the aperture size of the conventional VCSEL [47-49], optically-pumped external-cavity surface emitting lasers [49] and [50], and use of VCSEL arrays [51] and [52] have been published.

In [47], by defining large VCSEL apertures, up to 500 μm in diameter, a maximum continuous wave (CW) output power of 1.95 W was achieved for an InGaAs/GaAs VCSEL. The same group also reported an InGaAs/GaAsP VCSEL with the maximum output power of 1.09 W at room temperature by increasing the aperture diameter up to 400 μm [48]. VCSELs with 300 μm aperture diameter and 5 InGaAs QWs showed a peak pulse power of over 12.5 W at 20 A bias current [49]. Optically pumped vertical external-cavity surface-emitting lasers (VECSELs) have also produced high CW power levels such as 8 W at 10 °C [50] and 4 W at 16 °C [51]. Moreover, optical pumping can circumvent current-crowding effects occurring in large-aperture electrically injected devices. It can also provide single-mode operation even for large apertures, but at the expense of adding complexity to the system. In 1998 monolithic 2D VCSEL arrays with CW power of >2 W and pulsed power of >5 W by active cooling the laser arrays were introduced [52]. In another study, arrays of 1.08 W emitting at room temperature were mounted on a metalized diamond in order to decrease the unwanted heating effects of the lasers [53].

Although larger area of the active region increases the output power, it simultaneously reduces the laser modulation frequency and also pushes the laser toward the multimode operation regime. The highest reported bandwidth for large-aperture single VCSELs, whether electrically or optically pumped, is approximately 1 GHz [54]. 2D arrays of VCSELs have the capability of providing optical powers in the watt regime with no additional increase in cost and complexity and also offering high modulation frequency operation. Providing both high speed and high power is challenging for individual VCSELs since a physical attribute that is important for their high-speed

operation, i.e., small cavity volume, also hinders obtaining high output powers from these devices in comparison to larger cavity, but often slower, edge-emitting lasers. Although a higher power single VCSEL can be achieved by increasing the active area of the laser, this approach reduces the modulation frequency which is inversely proportional to the square root of the effective volume of the mode at fixed device currents [55].

High speed VCSELs in a 2D array configuration leads us to form a high-speed high-power VCSEL light source. High-speed, high-power VCSELs have the potential to improve the data transmission rate and image resolution for optical communication and LIDAR systems respectively. High-speed VCSEL arrays for parallel optical interconnects have been reported [56]. 1×8 and 4×8 VCSEL arrays, respectively operating at 850 nm and 980 nm wavelengths with 250 μm device pitch were fabricated and characterized. An individual 6 μm diameter active region VCSEL in the 4×8 array showed 7 mW output power and 10 GHz modulation bandwidth, but combined operation of array has not been discussed. In another similar work, a 4×12 array of 6 μm diameter individual VCSELs with device pitch of 250 μm in the x direction and 350 μm in the y direction operating at 985 nm presented optical power of 1.7 mW per laser and individual laser 3dB bandwidth of greater than 15 GHz at 70 °C [57]. The first demonstration of high power (>150 mW), high speed (>8GHz) 980 nm oxide confined VCSEL arrays were reported by Prof. K. Lear's group at CSU in 2009 [58], while a complete analysis of this work appeared in [59]. This work was believed to have the highest power reported for a VCSEL or VCSEL array with over 1 GHz bandwidth. Figure 3.1 summarizes some of the published work on the speed and power of VCSELs operating at different wavelengths.

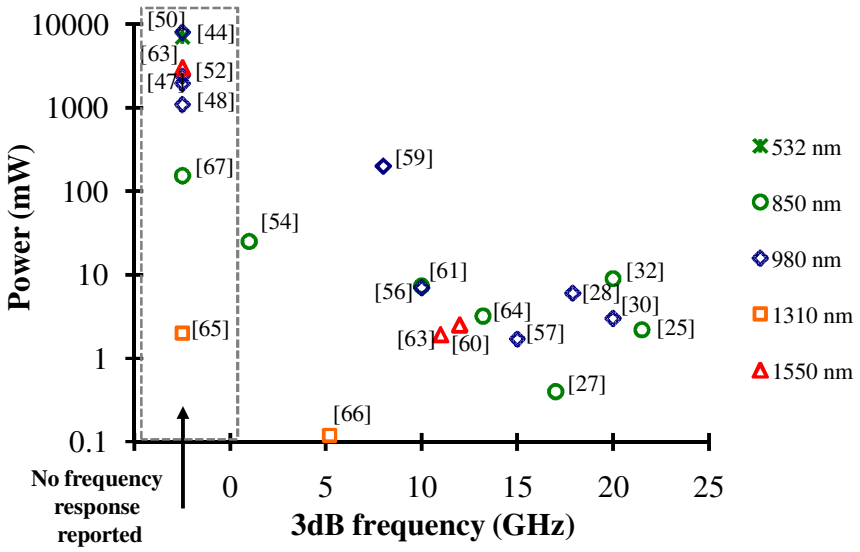

Figure 3.1 Summary of reported VCSEL power vs. 3dB frequency.

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Chapter 4

980 NM HIGH-SPEED, HIGH-POWER OXIDE-CONFINED VCSEL ARRAYS AND SINGLE ELEMENTS

4.1. Introduction

In this chapter, fabrication and characterization of 980 nm oxide-confined bottom-emitting VCSELs will be discussed with the main focus being on the work performed on realizing high-speed, high-power VCSEL arrays. These arrays are interesting light sources for applications such as free space optical communication [1] and light detection and ranging (LIDAR) systems [2]. Other applications that could benefit from a combination of high power and moderate bandwidth lasers are laser based projection displays [3] and high speed printing [4]. VCSEL arrays are the best potential fit to these applications and surpass single high power VCSELs and edge-emitting lasers.

The research described in this chapter proposes a method for achieving laser sources with both high speed and high power characteristics. These VCSEL arrays consist of single VCSELs with relatively small diameter and thus small volume of the mode that is beneficial for high speed operation. Simultaneous operation of individual VCSELs as an array multiplies the output power of each element by the number of elements that can be in the order of hundreds or even thousands of devices. Two main

challenges in attaining high-speed, high-power VCSEL arrays are high temperatures generated in the array and array nonuniformity. The former issue prevents the elements in the array from operating with the same properties as individual VCSELs. The latter can cause a nonuniform distribution of both electrical current and heat flow over the array resulting in nonuniform properties of VCSEL elements on different positions over the array. The arrays presented here are shown to only have a small temperature rise and operate uniformly due to effective thermal management. In order to check uniformity and scalability of arrays, single VCSELs similar to array components have also been measured and analyzed.

Since our VCSEL arrays are designed to be on the same chip as individual VCSELs, processing steps and measurement fundamentals are similar for both individual VCSELs and arrays. These VCSELs were fabricated from the bottom-emitting epitaxial material grown by Opticomp Corporation in 2006 (OB1 wafer) and have the assignment name OB1_11-2_2 corresponding to processing run (11) and chip location coordinate (2_2). The mask set "VCSEL_BE_JJ1" was used to fabricate the VCSELs presented in this chapter.

4.2. VCSEL design and fabrication

4.2.1. Structure

Bottom emitting, 980 nm VCSELs were fabricated from molecular beam epitaxy (MBE) layers grown on an n-type GaAs substrate. The n-type lower mirror consists of 23-period Si-doped GaAs-$Al_{0.86}Ga_{0.14}As$ distributed Bragg reflector (DBR) with a calculated reflectivity of 99.59%. Then a 1-λ, triple $In_{0.18}Ga_{0.82}As$ 8 nm quantum well cavity with 8 nm GaAs barriers and $Al_{0.21}Ga_{0.79}As$ separate confined heterostructure

layers was formed. The p-type upper mirror contains 27-period C-doped GaAs-$Al_{0.86}Ga_{0.14}As$ DBR with a parabolic grading of Al composition and calculated reflectivity of 99.67%. The p-mirror was terminated with a highly doped phase matching GaAs contact layer. A single, low index, ~λ/4, 98% Al content p-type mirror layer adjacent to the cavity was employed to form the oxide layer for the oxide-confined VCSEL structure. A detailed structure of this epitaxial material with doping of the layers and grading is given in Appendix A.

4.2.2. Fabrication

The device mesa was defined with dry etching of the patterned surface using an inductively coupled plasma (ICP)/reactive ion etching (RIE) system and Cl_2/BCl_3 gas mixture. The etching is stopped on the fifth mirror pair after the active region as determined by in situ monitoring of the surface reflection using a laser and detector. After n-metal lithography and removing the native oxide on the surface using a diluted HCl (1:1) solution for one minute, a Ni/Ge/Au (200/425/1360Å) metal system was deposited by means of an electron beam evaporation system. Next, a wet oxidation furnace with a 6 cm diameter quartz tube at 400 °C and 85 °C water steam was employed to form oxide apertures with desired oxidation lengths of 1.5 to 3 μm. After oxidation and dipping the sample in the diluted HCl solution for one minute, a Ti/Au (100/2000Å) p-type contact was evaporated on top of mesas. A 100 nm PECVD SiN_x was then deposited on the sample in order to insulate the mesa sidewalls from electrical shorting caused by metal plating. The SiN_x also decreased the pad capacitance. The vias were etched using a reactive ion etching (RIE) system in CF_4/O_2 (8% O_2) mixture plasma. In order to improve thermal behavior of VCSELs via decreasing the thermal resistance, a ~2 μm thick copper

layer was electroplated on top and around the mesas including sidewalls in order to increase lateral heat flow. Before Cu plating, a Ti/Au (100/800 Å) seed layer was deposited on the sample to make a conductive surface for electroplating. The schematic of the fabricated VCSEL is depicted in Figure 4.1. A process flow for bottom-emitting VCSELs can be found in Appendix B.

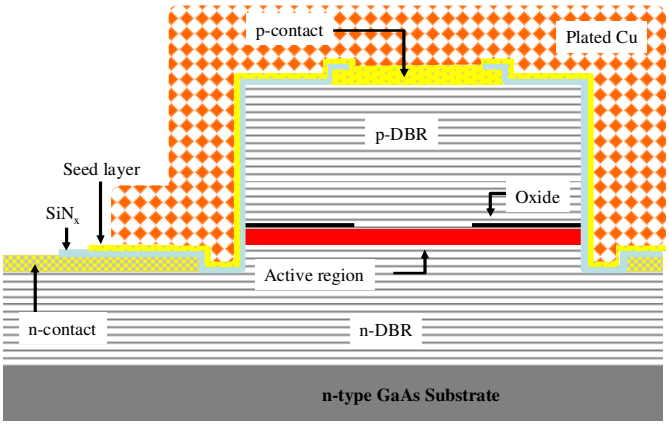


Figure 4.1 A cross section view of the fabricated VCSEL.

In order to provide better heatsinking and further reduce thermal resistance, the sample was then flip-chip bonded on a GaAs heat spreader. To improve the bonding process both chip and heat spreader were plated with indium before being flip-chip bonded [5]. Copper with very high thermal conductivity compared to GaAs can effectively transfer generated heat in the laser structure to the surrounding area. The SEM picture in Figure 4.2 shows three Cu electroplated mesas for one of our first high speed VCSEL samples fabricated by John Joseph and characterized by me in late 2006. This sample has a ~20 μm thick mushroom shape of plated Cu for better heatsinking.

Figure 4.3 shows photos of the chip before and after bonding with arrays in the middle and single devices on the perimeter of the chip. The chip was fabricated using one of our newly designed masks.

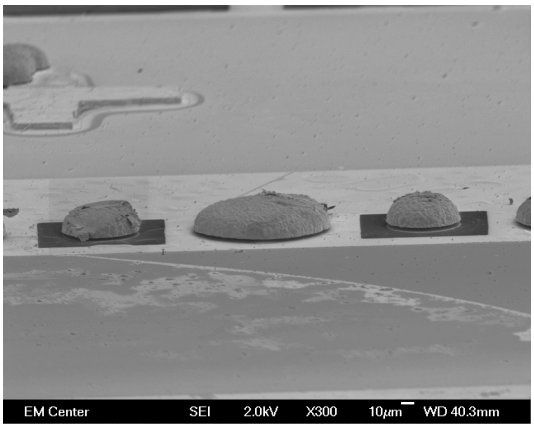


Figure 4.2 SEM picture of mesas covered with plated Cu from one of our early fabricated samples.

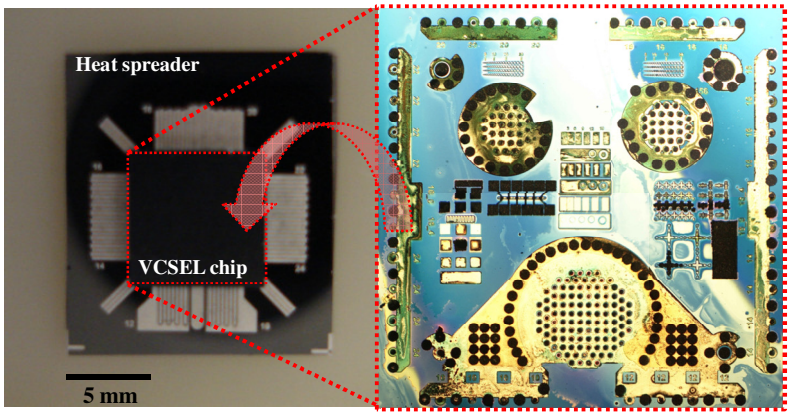
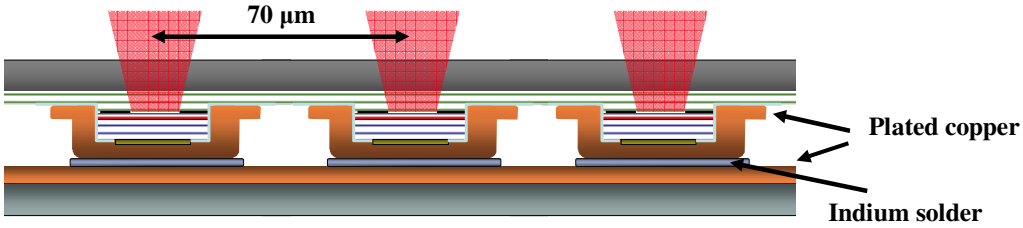


Figure 4.3 Flip-chip bonded sample (left) and sample before flip-chip bonding.

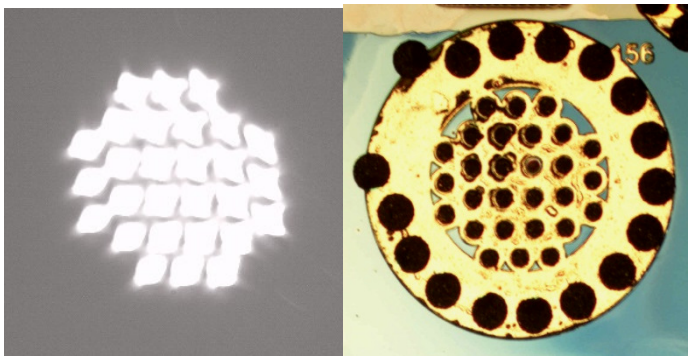
Circularly shaped VCSEL arrays were formed using 28 individual lasers with 70 μm device pitch each with 18 μm or 6 μm active diameter in a 24 μm or 12 μm diameter mesa, respectively, as shown in Figure 4.4(a). These single VCSELs are electrically connected to form a single high-speed, high-power light source. A parallel configuration

for both signal and ground paths reduces the series resistance and inductance of the flip-chipped array. The two array sizes as well as similar individual elements were used to investigate the scalability of the arrays. The $\lambda_{PL}-\lambda_{cavity}$ = -7 nm PL-cavity mode offset design for the epitaxial material is well suited for high temperature operation of lasers at high bias currents.

Ground pads were formed on the array perimeter and signal pads distributed in the middle of the array as depicted in Figure 4.4(b). The two sizes of arrays as well as similar individual elements are used for proving the scalability of the proposed arrays. Although a higher power VCSEL can be achieved by increasing the active area of a single laser, the modulation frequency will be reduced as it is inversely proportional to the square root of the effective volume of the mode at fixed device currents.



(a)



(b)

Figure 4.4 (a) Array mesa configuration and (b) array under bias current (left) and array signal and ground pads (right).

Copper plating and flip-chip bonding effectively reduce self-heating issues at elevated bias currents by means of reduction in thermal resistance for single mesas identical to those used as elements in the arrays. Figure 4.5 summarizes experimental results for thermal resistance reduction of IR VCSELs from 2005 (work done by A. Al-Omari) to 2007 to show the improved thermal resistance by plating and flip-chip bonding. As seen in the graph, plating and flip-chip bonding done in 2007 has improved the measured thermal resistance before 2007 which proves the effectiveness of our heat management methods. There are also fits to the data to approximate the thermal resistance, R_{th}, as [6]

$$R_{th} = \frac{1}{2\xi d} \tag{4.1}$$

This simple model describes the heat flow of a circular area with diameter d into a semi-infinite substrate with thermal conductivity, ξ, and is approximately valid for VCSELs mounted on top of relatively thick substrates. Using this method, effective thermal conductivity of sample "OB1_7_F" with the minimum thermal resistance, is approximated as 0.7 W/˚C-cm.

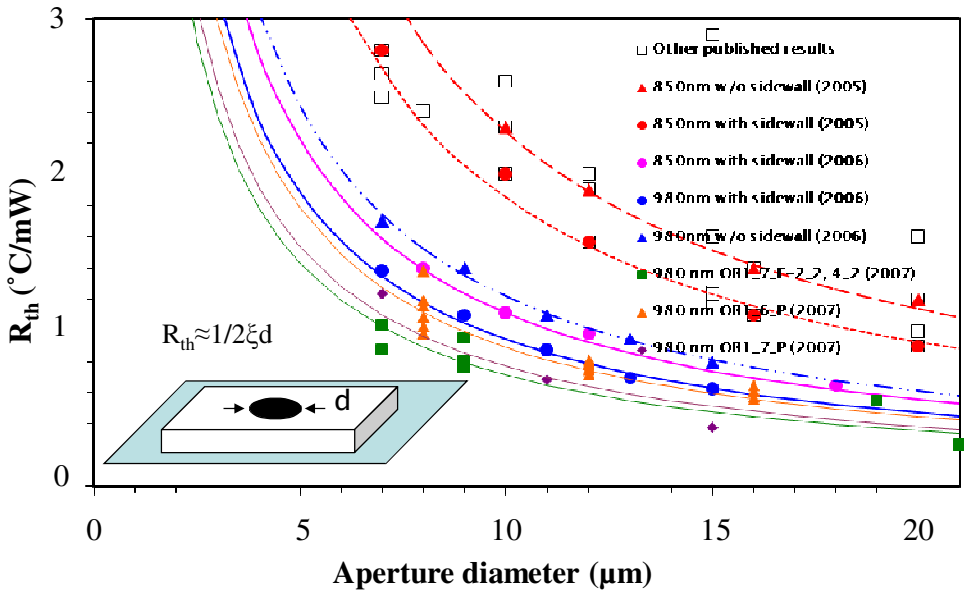


Figure 4.5 Measured thermal resistance of different IR VCSELs along with fits to data. (Data for the work done before 2007 is from Ahmad Al-Omari [7])

4.3. Array characterization

4.3.1. DC characterization

The light power and laser voltage versus laser current (LIV) measurement of the 28-element, 18 μm active diameter array was taken for CW and pulse operation. The LIV measurement was performed using a HP4156A semiconductor parameter analyzer along with a HP41501A expander unit and a silicon photodiode to measure the optical power of the array. Since the maximum photodetector current is limited to 0.5 mA an optical attenuator has been used along with the detector. The attenuator was calibrated by measuring the optical power of a single VCSEL using the photodetector with and without the attenuator and finding the ratio as attenuation factor. The array showed a CW output power of 0.15 W at 500 mA bias current and room temperature. This array with a differential quantum efficiency of η_d=0.31 and maximum wallplug efficiency of 12% has

a threshold current and voltage of 40 mA and 1.7 V respectively as presented in Figure 4.6. Pulsed measurement with 500 ms current pulse period and 0.5 ms pulse widths is also presented in Fig. 4. Around 24% improvement in the array output power at ~875 mA bias current, i.e. the CW roll over current, is achieved by decreasing the pulse width down to 500 µs i.e. 0.1% duty cycle. Since the 500 µs pulsewidth is much larger than thermal time constant of each mesa (τ_{th}~1 µs), there is not a significant improvement in the power with 500 µs pulses. However, theses pulses can alter the heatsink temperature because the thermal time constant of the heatsink is much larger than 1 µs and so more comparable to the 500 µs pulses.

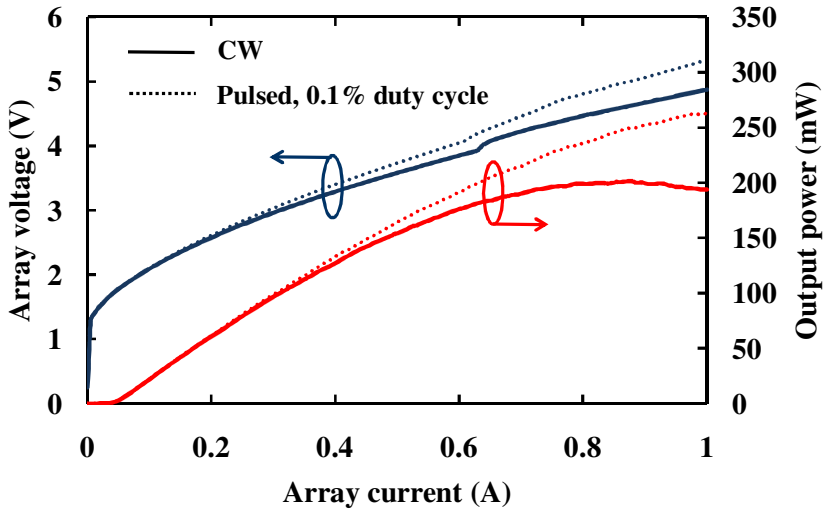


Figure 4.6 LIV curves of the 28-element, 18 µm active diameter array under CW and pulse operation.

In order to understand the behavior of an individual laser, the LIV plot of a single VCSEL identical to those used in the array is illustrated in Figure 4.7. In this experiment the HP4156A semiconductor parameter analyzer and the silicon photodiode without any optical attenuator were employed to measure the LIV curves. The single VCSEL has an output power greater than 6.9 mW at 20 mA bias current which means that if an array of

28 elements is biased at 28×20 mA=560 mA, we expect to get 28×6.9 mW=193 mW which is only ~15% larger than the array measured power at 560 mA i.e., 167 mW. The higher voltage of the array is attributed to an approximately 0.5 Ω series cable resistance. This result emphasizes the scalability and the fact that the heat flow in the 28-element array is well-distributed over the array area [8].

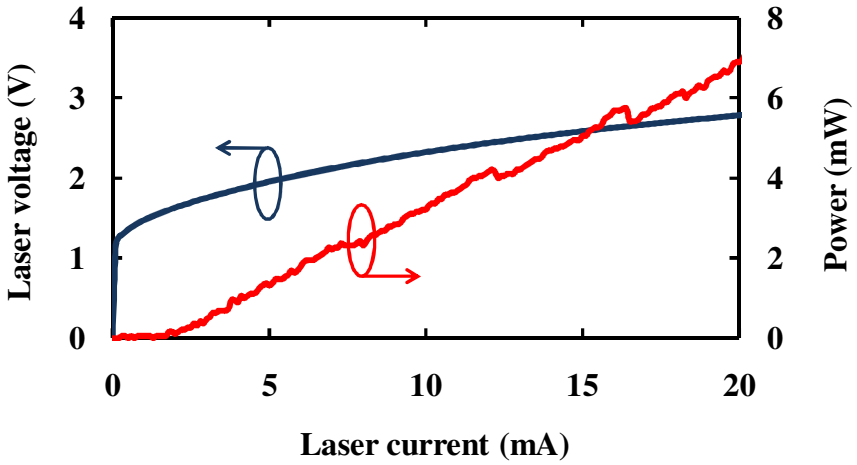


Figure 4.7 LIV curves of a single 18 μm active diameter VCSEL.

Another array with the same number of elements but with 12 μm diameter mesa and 6 μm active diameter has been also measured for evaluating the scalability of arrays which are both fabricated on the same die. As depicted in Figure 4.8, the 28-element, 6 μm active diameter array with threshold current of 10.5 mA generates an optical power of 90 mW at 300 mA input injected current. A single 6 μm active diameter VCSEL exhibits 3.2 mW optical power at 12 mA bias current as expected for a scalable array.

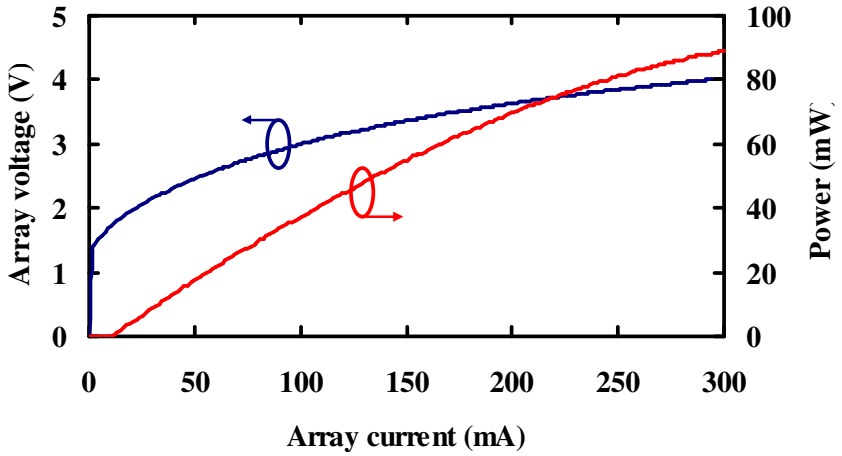


Figure 4.8 LIV curve for 28-element, 6 μm active diameter array under CW operation.

The LIV data for both arrays and corresponding single elements is summarized in Table 1. The average output power and threshold current associated with each individual element in the array is also given.

Table 4.1. Summary of LIV data for the arrays and identical single elements.

	18 μm active diameter			**6 μm active diameter**		
	Array	**Array/28**	**Single**	**Array**	**Array/28**	**Single**
P	167 mW (@560 mA)	6mW	6.7 mW (@20mA)	86 mW (@280 mA)	3.1 mW	86 mW (@280 mA)
I_{th}	40 mA	1.4 mA	1.8 mA	10.5 mA	0.37 mA	0.4 mA

4.3.2. AC characterization

Modulation responses for the 18 μm active diameter array and a single VCSEL were characterized using an Agilent 8722ET vector network analyzer (VNA) and a Cascade Microtech high frequency coplanar ACP40-GSG-125 probe. The VNA was

calibrated using a standard substrate and the GSG probe to improve the measurement accuracy. To be able to do response calibration using the substrate and probe, we need to provide the probe characterization data and recall it as the state of the system. A detailed instruction of how to save/recall the state files is given in Appendix C. The calibration procedure was carried out by reflection measurement of one port (RF OUT) from a short circuit and load on the substrate and an open circuit by keeping the probe off the substrate in the air. The calibration procedure was followed by transmission measurement between "RF OUT" and "RF IN" ports via 2 pieces of high frequency cables used in the VCSEL response measurement. Before performing the calibration procedure for the VNA, measurement parameters need to be adjusted and kept fixed during the measurement. If any of the stimulus parameters change after doing a calibration, the system should be recalibrated. In this experiment, the RF power from the test port "RF OUT" was set to -10 dBm with the frequency range of 5 MHz to 20.05 GHz. In order to reduce error and prevent frequency response distortion [9], a slow sweep rate was chosen by decreasing the IF bandwidth down to 100 Hz.

The arrays were biased using the HP4156A/HP41501A at fixed currents up to the 500 mA maximum current rating of the probe. Both DC bias and AC modulation signal were applied to the probe through a high speed high current Picosecond Pulse Labs 5585 bias tee for the array and an Anritso K251 high speed bias tee for the single VCSEL. As the measurement setup is shown in Figure 4.9, the output light was coupled into a Discovery Semiconductor DS30S p-i-n photodiode via a multimode bare 62.5 μm core diameter, 0.275 N.A. bare fiber at a vertical distance of ~1 mm above the chip surface to capture a portion of the light from all elements. The estimated coupling efficiency is

~3%. The output signal of the photodiode was then amplified by a Miteq radio-frequency low noise amplifier and the VNA extracts S_{21} parameters of the array and single VCSEL at applied bias currents.

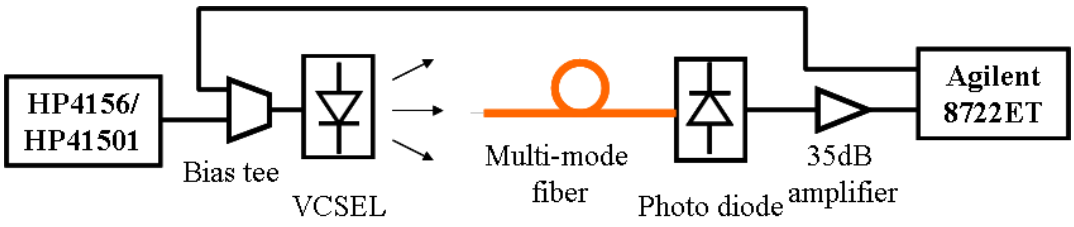
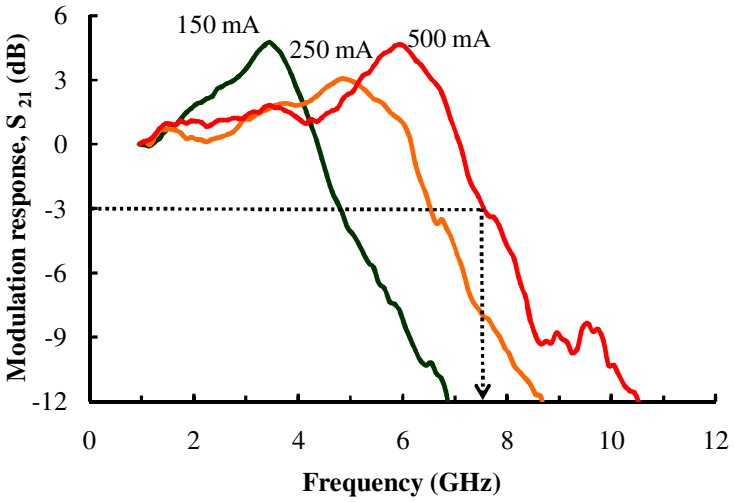
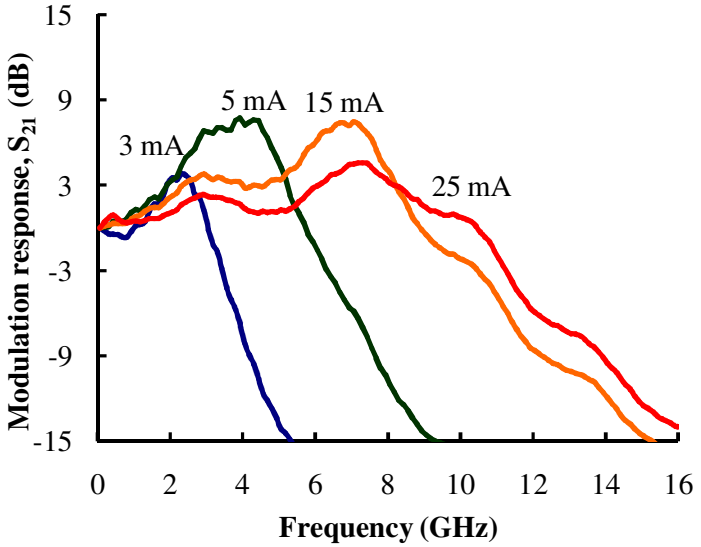


Figure 4.9 Frequency response measurement setup.

Figure 4.10(a) depicts modulation responses for selected bias currents at 20 °C for the 28-element, 18 μm active diameter array. The array exhibits a 3dB frequency of 7.6 GHz at a 500 mA bias current. Cut off frequency of the high current Picosecond Pulse Labs bias tee employed here prevents accurate measurements below 1 GHz. The laser array bandwidth could be extended to higher frequencies by increasing the bias current. Frequency response measurements for a single 24 μm mesa diameter laser nominally identical to those constituting the array show that a 3dB modulation frequency of up to 11 GHz is achievable as shown in Figure 4.10(b). The higher frequency response of the single VCSEL than the array is attributed to the higher heat spreader temperature and thus higher junction temperature resulting from the array's higher heat load as discussed in Section 4.3.4.



(a)



(b)

Figure 4.10 Frequency response (a) for the array and (b) for a single 18 μm active diameter VCSEL.

As plotted in Figure 4.11 the modulation frequency of the array increases linearly with the square root of array's optical power before getting saturated at high powers. The line is the fit to the linear portion of the curve using $f_{3dB}=DP^{1/2}$. D is a proportionality factor which is discussed in Chapter 6 of this dissertation and given by [10]

$$D = \frac{1}{2\pi}\sqrt{\frac{\partial g}{\partial n}\frac{\eta_i}{\eta_d}\frac{v_g}{V_{m,eff}}\frac{\lambda}{hc}} \tag{4.2}$$

where $\partial g/\partial n$ is the differential gain, η_i is the internal quantum efficiency, v_g is group velocity, $V_{m,eff}$ is the array effective volume of the mode, λ is wavelength, h is Planck's constant, and c is the speed of light. As a comparison, 3dB frequency of the single VCSEL with 18 μm active diameter as a function of square root of single VCSEL power×28 is also plotted in Figure 4.11 along with the fit to data.

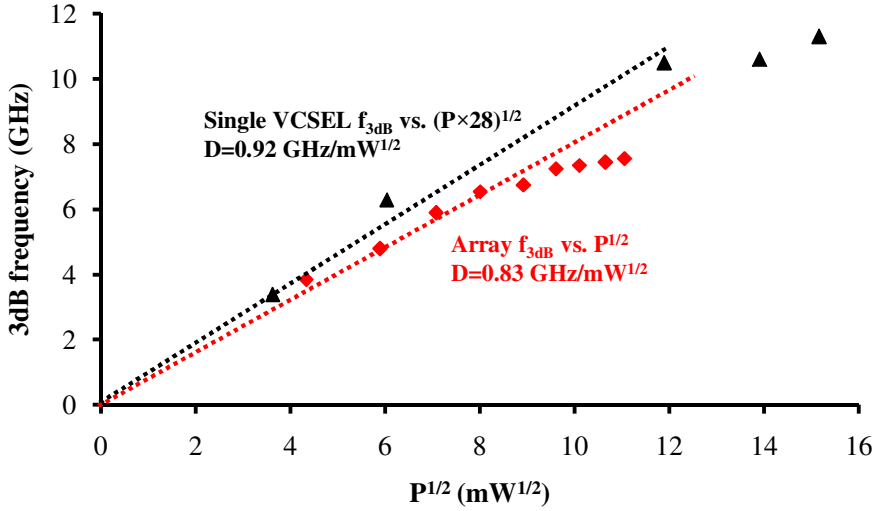


Figure 4.11 3dB frequency vs. square root of the array and scaled single VCSEL power.

4.3.3. Pulsed characterization

Pulsed measurements were performed on an array with 28 elements and 24 μm diameter mesa with 21 μm active diameter in order to evaluate its ability to generate short pulses which is very important in applications such as LIDAR systems. A block diagram of the setup used for pulse measurement is given in Figure 4.12. DC current from a HP4145 semiconductor parameter analyzer and 100 ps width pulses from an Avtech AVH-S-1 impulse generator were applied to the array via an Anritsu bias tee. A

HP8116A pulse/function generator with 100 KHz rectangular wave frequency and 100 ns pulse width was connected to the Avtech impulse generator as an external trigger. The rectangular wave had a 4 V amplitude with a 2 V offset. After coupling light into a lensed multimode fiber the same photodiode and amplifier that already used for AC measurement provided electrical signal to an Agilent 86100A wide-bandwidth oscilloscope.

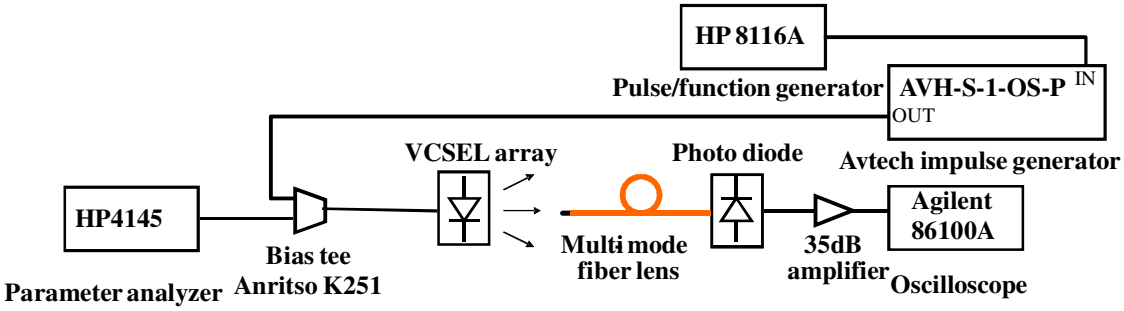


Figure 4.12 Pulse measurement setup.

In Figure 4.13, a 100 ps electrical input pulse to the array and gain-switched 60 ps FWHM output pulse from the array can be observed.

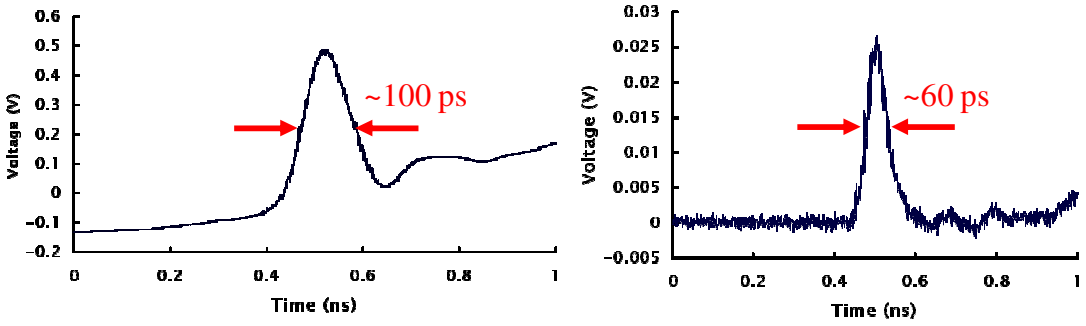


Figure 4.13 Array input electrical pulse (left) and output optical pulse response (right).

4.3.4. Thermal resistance analysis

In this section an equivalent thermal circuit model is introduced. This model quantitatively explains the temperature distribution in the mesa including the copper heatsink and the GaAs heat spreader for both VCSEL array and identical single element.

Copper plating and flip-chip bonding effectively reduce self heating issues at elevated bias currents by means of reduction in measured thermal resistance down to 425 °C/W for a single 18 μm active diameter laser. A thermal resistance of 30 ˚C/W was also measured for the 28-element array of identical 18 μm active diameter lasers. The measured total thermal resistances include thermal resistance from the junction to outside the mesa, $R_{th,mesa}$ and from outside the mesa through the heat spreader, $R_{th,HS}$. The difference in measured thermal resistances can be better analyzed using equivalent thermal circuit models for a single VCSEL and a flip-chip bonded array as depicted in Figure 4.14. The heat transfer rate is $q=\Delta T/R_{th}$ where ΔT is the temperature difference and *Rth* is the thermal resistance. If the heat transfer rate from the junction to outside the mesa for each array element equals the heat transfer rate in an identical single VCSEL, which in fact is the case here, then the heat rate in the array heat spreader, qarray is 28 times larger than that in a single device, q_{single}. This high heat load gives rise to a much higher heat spreader temperature for the array, i.e. 28 times larger than the case of a single device. The temperature difference from the junction to the copper on the outside of each mesa in the array is expected to be identical to that for a single device.

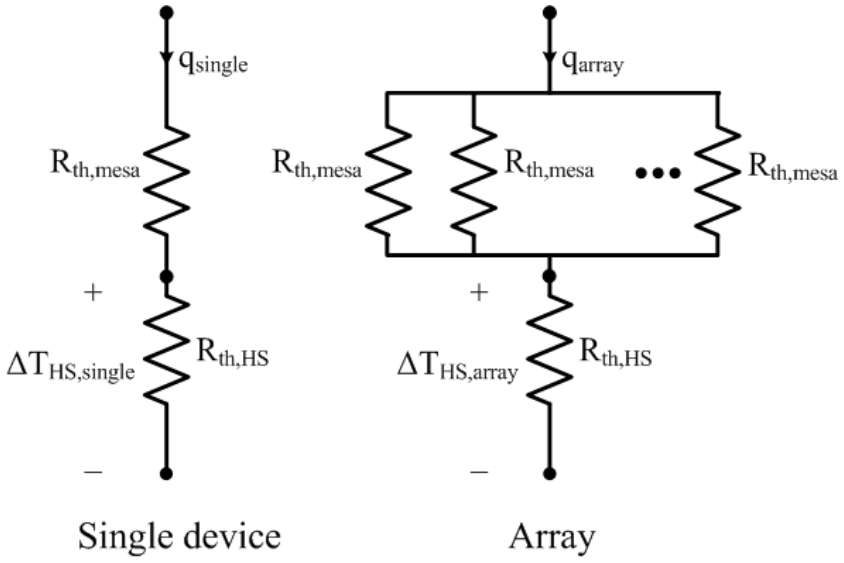


Figure 4.14 Equivalent thermal circuit models for the flip-chip bonded single VCSEL and array [11].

The magnitudes of $R_{th,mesa}$ and $R_{th,HS}$ corresponding to the thermal resistances of flip-chip bonded VCSEL elements and a copper-plated GaAs heat spreader can be inferred from the total measured thermal resistances of the single VCSEL and array. According to the models, the thermal resistances of the single VCSEL and the array can be written as $R_{th,single}=R_{th,mesa}+R_{th,HS}$=425 ˚C/W and $R_{th,array}=R_{th,mesa}/28+R_{th,HS}$=30 ˚C/W respectively which give $R_{th,mesa}$=410 ˚C/W and $R_{th,HS}$=15 ˚C/W. Note that in this model, while the temperature rise across all $R_{th,mesas}$ is the same at the same bias condition, the temperature rise across $R_{th,HS}$ is N=28 times larger for the array than for the single device. For example, the calculated temperature across the heat spreader for the single VCSEL at 20 mA bias current is 0.7 °C while that for the array at 560 mA bias current is 28.6 °C. This 27.9 °C temperature difference is the same as the junction temperature difference for

the single VCSEL and array, since the temperature rise within the single VCSEL and array mesas are the same [11].

4.3.5. Uniformity analysis

Nonuniform distribution of electrical signal over the array would cause each array element to have a different current and thus a different response. Nonuniformity of the array might be caused by unbalanced electrical or thermal distribution over the array. Temperature variation over the array which can affect the laser performance could also alter the array uniformity. Since the calculation result for temperature variation on the surface of a single VCSEL with the same effective diameter as the array showed that there would be a 72 ˚C temperature variation over such a single device, it is worth checking the uniformity of the array by comparing the 3 dB frequency response and operating wavelength of each array component.

In order to perform this analysis a bare, i.e. without a lens multimode fiber was employed to scan the array area and measure the frequency response and wavelength of array elements at different positions. While sweeping the fiber in the x and y directions the graded-index 62.5 μm core fiber with maximum N.A=0.275 was kept at a fixed ~125 μm distance above the VCSEL surface. This distance guarantees that only the output light of an individual laser is picked up at positions right above each single laser. This can be simply calculated by assuming a 10˚ divergence angle for each element in the array and other known physical dimensions as drawn in Figure 4.15. Then, the maximum distance, *h*, from the array surface that can avoid optical beam overlap between two adjacent elements can be approximated as 150 μm.

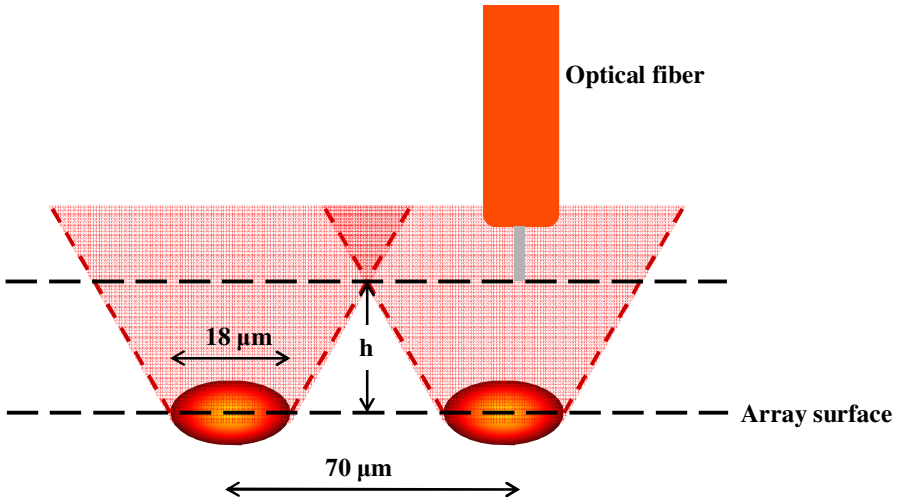
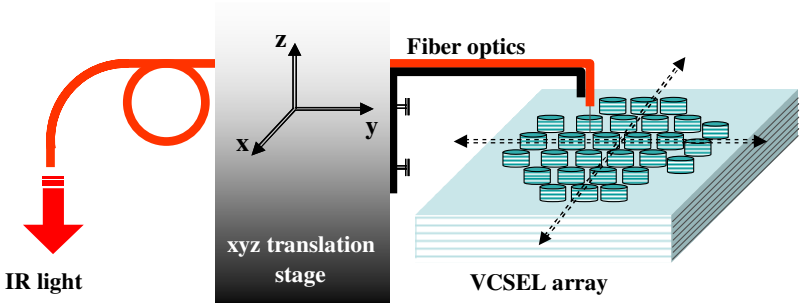


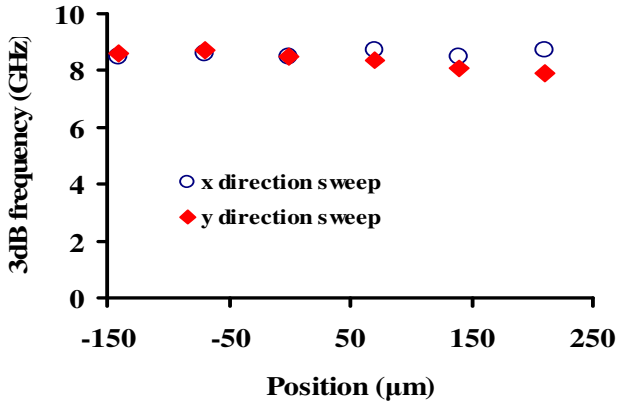
Figure 4.15 Maximum distance above the array surface for collecting the output light of only one individual VCSEL. The optical fiber is not in scale.

Figure 4.16(a) shows the apparatus for this measurement where the array is scanned in x and y directions as shown with dashed arrows. The results depicted in Figure 4.16(b) and 4.16(c) shows that the frequency response of elements of the array at different radii measured from the center of the array is nearly independent of position [8]. This result indicates that both the individual laser performance and current distribution are relatively uniform over the entire array. Hence, it is anticipated that similar VCSEL arrays may be scaled up to hundreds or thousands of elements to achieve watt level CW powers with modulation frequencies approaching 10 GHz.

Analysis of the maximum wavelength variation of around 0.25 nm over the array area in Figure 4.16(c) leads to ~3.6 ˚C ((0.25 (nm) / 0.07 (nm/˚C)) temperature variation over the array.



(a)



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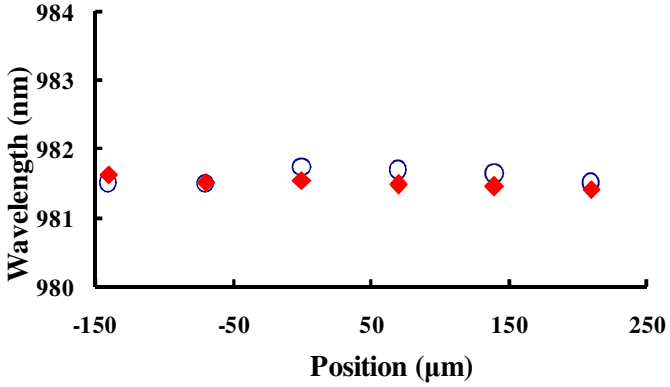

(c)

Figure 4.16 (a) Uniformity analysis apparatus, (b) 3 dB frequency, and (c) fundamental mode wavelength at different positions on the array measured from center of the array.

4.4. Conclusions

In this chapter high-speed, high-power 980 nm oxide-confined vertical-cavity surface-emitting laser (VCSEL) arrays and single VCSELs were fabricated and characterized. Lasers were fabricated from from MBE grown epitaxial layers on GaAs substrates. After defining mesas for arrays and single elements using an ICP/RIE dry etching system and depositing the n-type contact using an e-beam evaporator, VCSEL apertures were formed by wet oxidation of the sample in an oxidation furnace. Then the p-type contact was deposited on top of the mesas before seed layer deposition and copper and indium electroplating on and around mesas. As a last step of fabrication the sample became flip-chip bonded on prefabricated GaAs heat spreaders for better device heatsinking.

DC and AC measurement of arrays including 28 elements and single elements showed that the large and small arrays are capable of operating at CW powers of greater than 150 mW and 90 mW with corresponding injected currents of 500 mA and 300 mA respectively. The 28-element, 18 μm active diameter array shows a maximum CW power of 200 mW as well as a pulsed power of 260 mW at 1 A bias current with 500 μs pulsewidth and 0.1% duty cycle. LIV data taken from single VCSELs with the same active diameter as the constituent elements in the large and small array, i.e. 18 μm and 6 μm represents 6.9 mW and 3.2 mW at 20 mA and 12 mA bias current respectively. The DC data shows that these arrays can be scalable to even higher numbers of elements for higher output power. AC analysis gives the maximum bandwidth of 7.5 GHz and 11 GHz for the 18 μm active diameter array and single element, respectively. Lower frequency response for the array than for a single VCSEL might be due to high R_{th} for the chip.

The experimental results also showed that copper plating of the array elements and flip-chip bonding provides effective thermal management as well as offering uniform current and temperature distribution verified by the spatial dependence of modulation bandwidth and wavelength across the array. These arrays may be useful for mid-range LIDAR or free space optical communications systems.

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Chapter 5

THERMAL MANAGEMENT OF RED VCSELS

5.1. Introduction

Visible vertical-cavity surface-emitting lasers (VCSELs) are promising light sources in applications such as plastic optical fibers (POFs), laser printers, barcode scanners, optical mice, and medical sensors.

Fabrication and characterization of 670 nm (red) oxide-confined VCSELs are discussed in this chapter. One of the many challenges in realizing high temperature performance red VCSELs is the higher thermal resistance of the ternary alloys required in the active region and mirrors. Also, the shallower quantum wells (QWs) in red VCSELs result in a weaker carrier confinement and thus greater over-barrier leakage than larger bandgap contrast quantum well (QW) VCSELs. The resultant high junction temperatures decrease output power, roll-over current, resonant frequency, and reliability. One strategy for reducing thermal resistance is the use of a thick AlAs spacer layer [1] since it exhibits the lowest lattice thermal resistivity among all other Al compositions of $Al_xGa_{1-x}As$ [2]. Another is the minimization of semiconductor material outside the active region and surrounding the mesas in high thermal conductivity material such as copper. This method has already been used to improve infrared VCSEL performance [3] and [4]. The first investigation of the effect of mesa sidewall heatsinking by copper electroplating on the

performance of red oxide-confined VCSELs is discussed in this chapter. Some unexpected results in the VCSEL characterization led us to consider the stress on mesas induced by the electroplated copper [5]. The Comsol Multiphysics package is used to simulate the temperature distribution, thermal resistance, and stress in the copper plated red VCSELs.

5.2. VCSEL design and fabrication

5.2.1. Structure

Epitaxial materials for top emitting, 670 nm, oxide-confined VCSELs on an n-type GaAs substrate were provided by Vixar Inc. Details of epitaxial material growth such as layer doping, grading, and composition were not available at the time of writing this dissertation. For a typical design, both n- and p-type mirrors consist of DBRs with alternating layers of $Al_{0.5}Ga_{0.5}As$ and $Al_xGa_{1-x}As$ with mole fractions of $x>0.92$. A 1-3λ long active region was formed by $(AlGa)_{0.5}In_{0.5}P$/GaInP MQWs with Si-doped AlGaInP n-type and Zn-doped AlGaInP p-type spacer layers [1]. Three different material structures with almost similar design used in this work are 6535E, 6538C, and 7296B. Most of the results presented in this chapter are from wafers 6538C and 7296B which showed better performance than 6535E. Different fabrication runs are distinguished by adding a number to the name of the wafer, for example, 6538C_2 is the 2^{nd} processing run on the wafer 6538C.

5.2.2. Fabrication

Before starting the VCSEL fabrication, a 100 nm PECVD SiN_x is deposited on the sample in order to cover the sample surface and protect VCSEL top GaAs facets from

exposure to chemicals and unwanted materials in different processing steps. Device mesas with a variety of diameters were defined by dry etching of the unmasked field surface using an inductively coupled plasma (ICP)/reactive ion etching (RIE) system and Cl_2/BCl_3 gas mixture right after etching the SiN_x layer by a RIE system in a CF_4/O_2 (8% O_2) plasma. The mesa etching is stopped at ~32nd mirror pair, approximately 5 pairs before the thick AlAs spacer layer and active region and 5 pairs after the oxide layer, and determined by in situ monitoring of the surface reflection using a laser and photodetector. Next, a wet oxidation furnace with a 6 cm diameter quartz tube at 400 °C temperature containing steam from an 85 °C water bath was employed to form oxide apertures with desired oxidation lengths of 6 μm by oxidizing for ~13 min. After oxidation and dipping the sample in a $HCl:H_2O$ (1:1) solution for 30 seconds to remove the native oxide layer on the surface, a Ti/Au (50/2000Å) p-type annular contact was evaporated on top of the mesas using an electron beam evaporation system. After metal interconnect lithography and removing the native oxide on the surface using the diluted HCl solution for 30 seconds, another layer of Ti/Au (50/1500Å) was deposited by means of the electron beam evaporation system to form metal interconnects for easier VCSEL probing and/or wire bonding. In order to form the n-type electrode, a layer of Ni/Ge/Au (200/425/1360Å) metal system was evaporated on the back side of the sample. Both p- and n-type contacts were annealed at ~400 ˚C in order to reduce contact resistivity and in effect lower the laser operating voltage.

In order to improve thermal behavior of VCSELs via decreasing the thermal resistance, copper was electroplated on top and around the mesas with variety of inner and outer diameters which were defined in the mask. Before Cu plating, a

photolithography step was employed to cover the areas that would not be plated including the center of VCSEL mesas with a thin layer (~1 μm) of LOR10B in order to protect laser apertures from seed metals. A Ti/Au (100/800 Å) seed layer was then deposited on the sample to make a conductive surface for electroplating. The thin LOR10B layer was replaced with a thick AZ4400 layer (~3 μm) in later fabrication runs (7296B) in order to provide better mesa coverage and prevent laser facets from being contaminated by the deposited seed layer. After seed layer deposition another photolithography step with the same mask was used to define the areas that should and should not be electroplated by using a ~3 μm thick layer of AZ4400 photoresist. Copper electroplating process employed a commercial acid based Cu bath from Technic Inc. The plating was performed by running a current pulse with 20% duty cycle and 5 mA to 10 mA magnitudes. The plating time varied from sample to sample depending on the desired thickness. Detailed top emitting VCSEL fabrication is given in Appendix B. A cross section of the fabricated VCSEL as well as a top view of a fabricated mesa are shown in Figure 5.1. As also depicted in Figure 5.1(a) the SiN_x layer is removed from the laser facet after Cu plating to maximize the power output coupling of VCSELs.

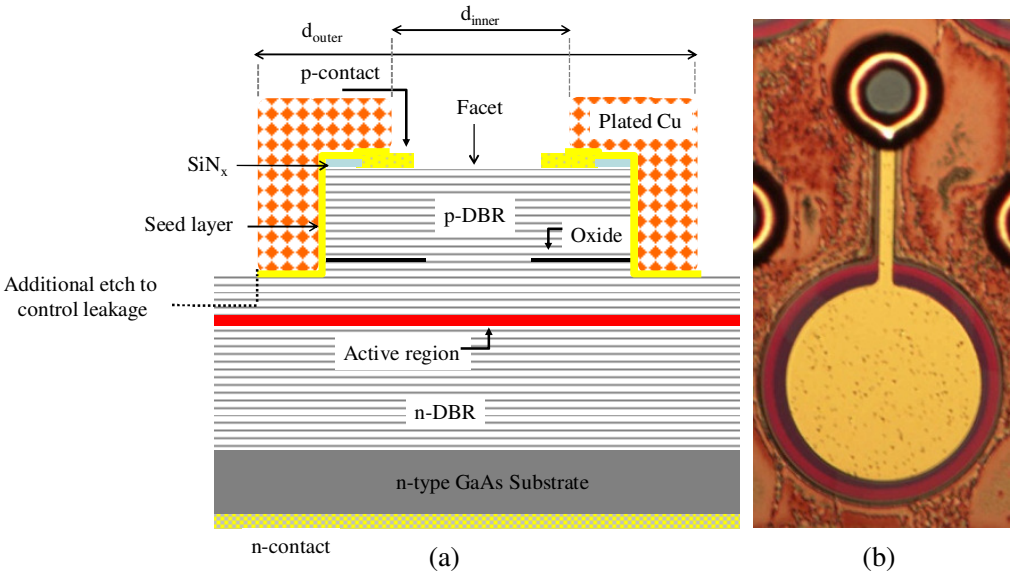


Figure 5.1 (a) A cross section view of the fabricated VCSEL (not in scale) and (b) Top view of a real mesa.

SEM pictures in Figure 5.2 show several Cu plated mesas with ~3 µm thick copper and different inner and outer plating diameters.

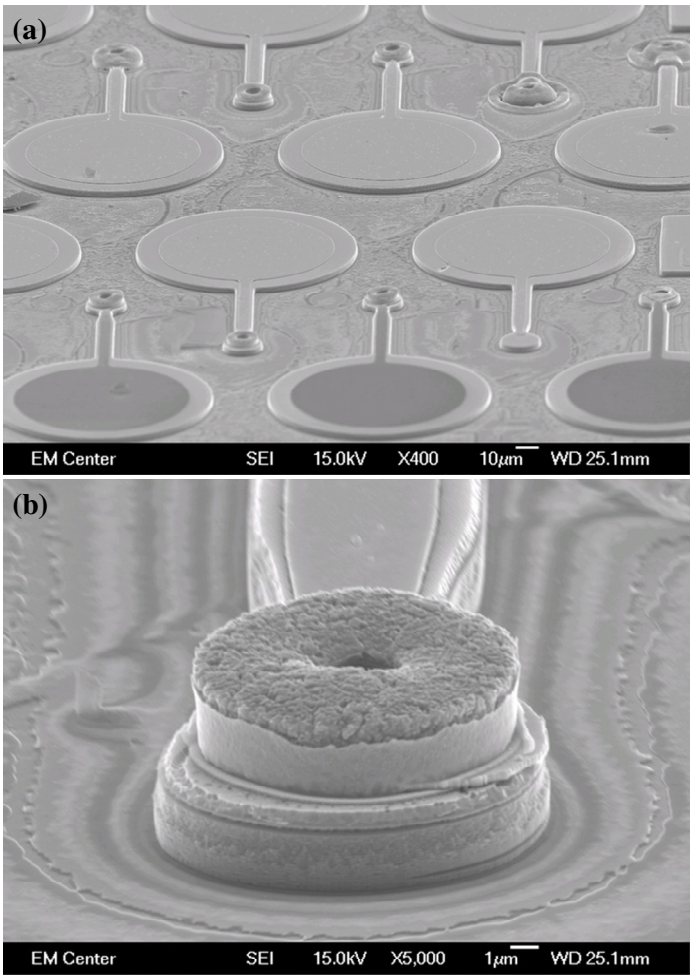


Figure 5.2 SEM pictures of (a) VCSEL mesas covered with plated Cu and (b) a VCSEL mesa with Cu only on top.

The mask design (VCSEL_TE_RS) includes VCSELs with mesa diameters of d=14, 16, 17, 18, 19, 20, 22, 27, and 32 μm with a combination of different inner and outer plating diameters. With the oxidation length, d_{ox}≈6 μm, the minimum and maximum inner and outer plating diameters were designed to be $d_{inner,min}$=d-2(d_{ox}-1), $d_{outer,min}$=d-4 and $d_{innre,max}$=d-4, $d_{outer,max}$=d+20, respectively. The variety of different mesa diameters and plating sizes allow a thorough analysis of heatsinking effects on the DC

behavior of VCSELs and help to understand the dominant direction of heat flow in plated VCSEL mesas. All different combinations of VCSEL diameters and plating sizes are listed in Appendix D. Normalized plating size, d_{norm}, is defined as $d_{norm}=(d_{outer}-d_{inner})/d_{inner}$.

The following sections discuss the copper electroplating results and plating effects on DC characteristics of 670 nm VCSELs. Characterization results for samples 6538C_2 and 7296B_2 will be presented.

5.3. VCSELs characterization before Cu electroplating

5.3.1. LIV characterization

The light power and laser voltage versus laser current (LIV) measurement of the fabricated red VCSELs for sample 6538C_2 were taken for different mesa sizes before and after Cu plating. The LIV measurement was performed using a HP4145A semiconductor parameter analyzer and a silicon photodiode to measure the optical power of each VCSEL. Figure 5.3 presents LIV curves for VCSELs with 4, 6, 8, 10, and 15 μm aperture sizes in corresponding 16, 18, 20, 22, and 27 μm mesa diameters before Cu plating. The leakage resistance path in IV curves is due to high surface conductivity of the layer that the etch was stopped on and was eliminated by etching a few more mirror periods from the sample surface as shown in Figure 5.1(a). Figure 5.4 compares the IV data for a 2 μm active diameter VCSEL before and after surface etching. Maximum output powers and threshold currents of these VCSELs have been summarized in Table 5.1.

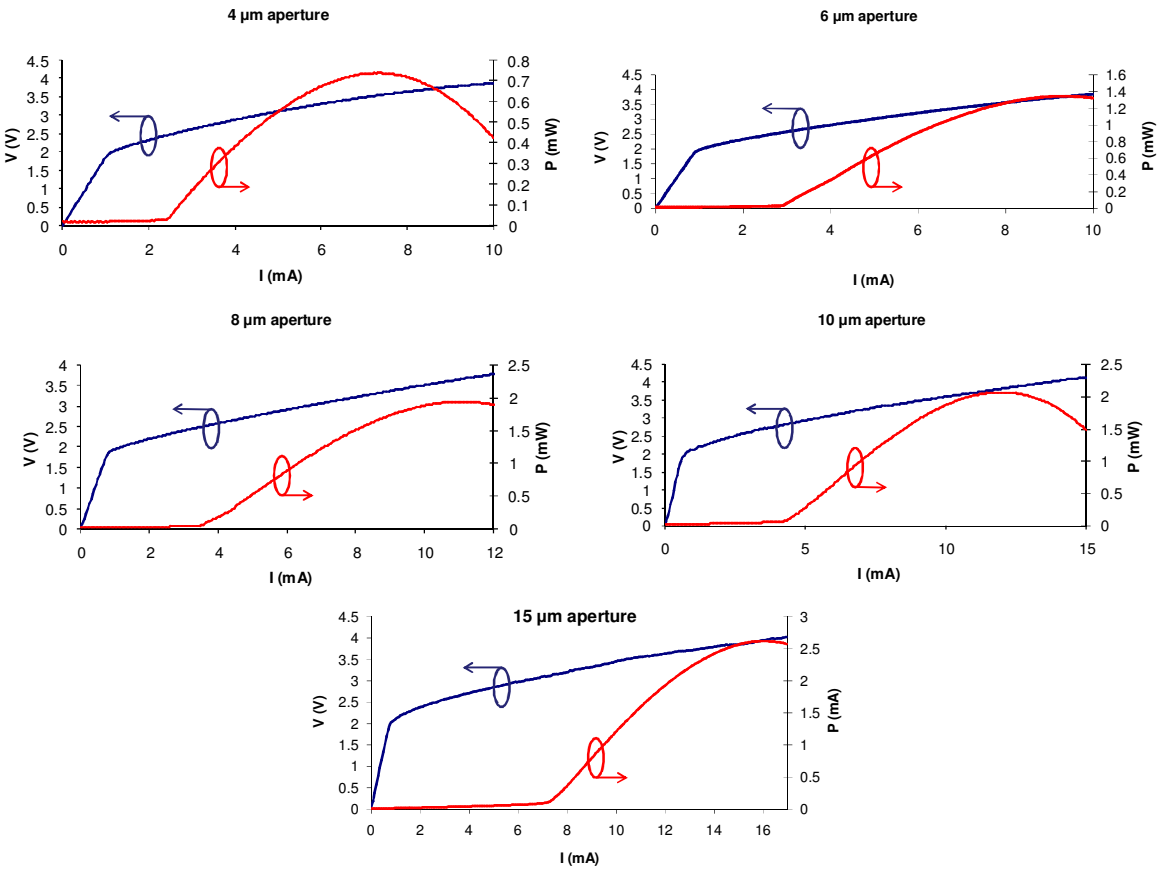


Figure 5.3 LIV curves of red VCSELs on sample 6538C_2 with variety of aperture diameters before Cu plating.

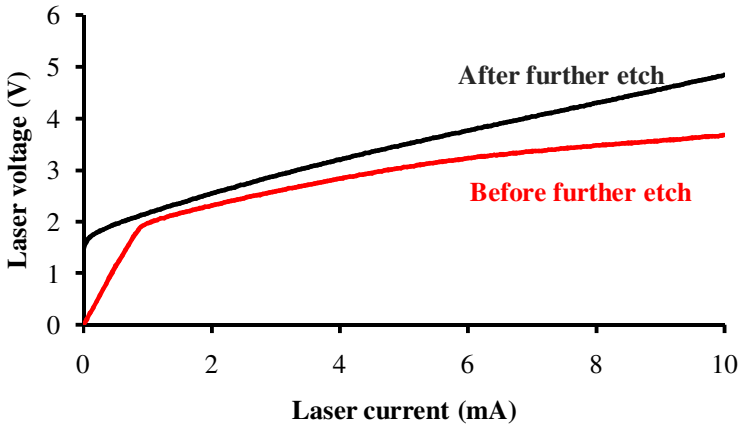


Figure 5.4 IV curves of a 2 µm active diameter VCSEL before and after additional etch as shown in Figure 5.1(a) by dotted lines.

Table 5.1 Summary of VCSELs maximum output power and threshold current for LIVs presented in Figure 5.3 for sample 6538C_2. I_{th} and P_{max} before and after plating are shown in Figure 5.13.

Mesa diameter/µm	Aperture Diameter/µm	I_{th}/mA	P_{max}/mW
16	4	2.4	0.74
18	6	2.8	1.35
20	8	3.4	1.95
22	10	4.1	2.07
27	15	7.2	2.6

The LIV data for different size VCSELs on sample 7296B_2 is also presented in Figure 5.5 and summarized in Table 5.2. This sample was etched down to the active region and thus does not suffer from the leakage resistance that appeared in the previous sample.

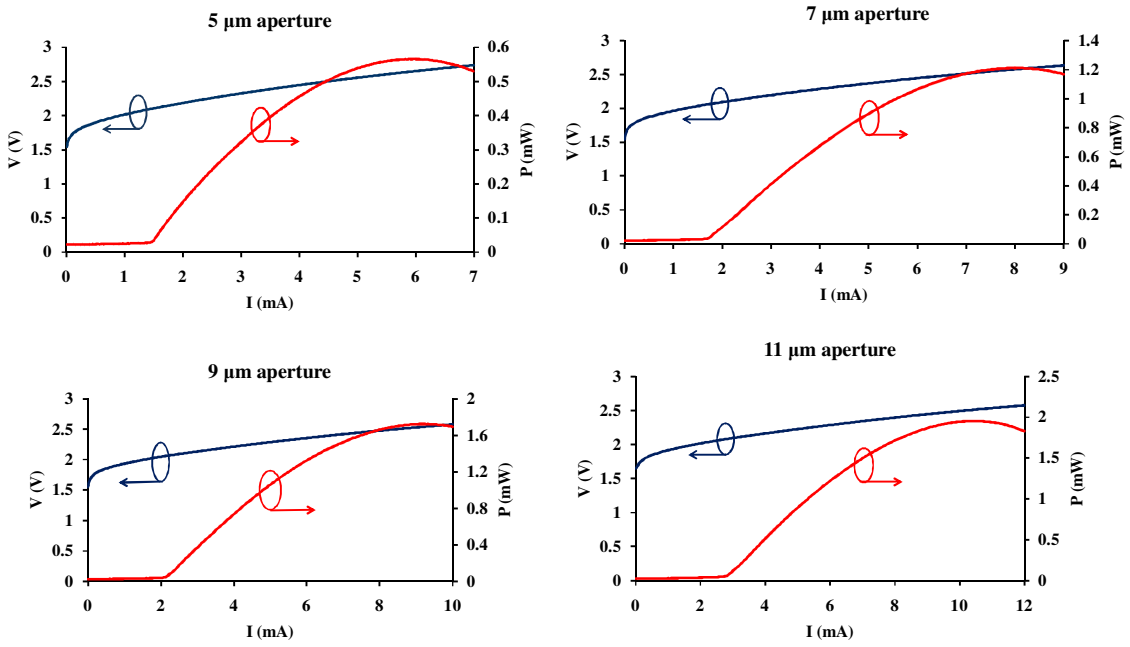


Figure 5.5 LIV curves of red VCSELs on sample 7296B_2 with variety of aperture diameters before Cu plating.

Table 5.2 Summary of VCSELs maximum output power and threshold current for LIVs presented in Figure 5.5 for sample 7296B_2. I_{th} and P_{max} before and after plating are shown in Figure 5.14.

Mesa diameter/µm	Aperture Diameter/µm	I_{th}/mA	P_{max}/mW
16	5	1.44	0.41
18	7	1.64	1.21
20	9	2.08	1.72
22	11	2.7	1.95

5.3.2. Thermal resistance measurement

In semiconductor lasers, emission wavelength is determined by both the cavity resonance and the material gain peak. In case of a VCSEL with a short cavity and thus, well-separated cavity modes, as mentioned in Chapter 2, the thermal shift in emission wavelength is determined by the shift in cavity mode and not shift in the gain peak. Thermal wavelength shift in the cavity mode is mainly due to the temperature dependence of the cavity and DBR refractive indices and less to the thermal expansion of the semiconductor layers, while, the shift in the peak gain is due to bandgap shrinkage [6]. Figure 5.5 shows an example of emission wavelength shift in a red VCSEL with elevating active region temperature by increasing the injected current. In this case, if the amount of wavelength shift with temperature is known, then the temperature raise due to the injected current can be determined. Temperature dependent wavelength in the red VCSELs that was measured using the technique defined in Chapter 2 as $\partial\lambda/\partial T$=0.05 nm/˚C for wafer 7296B and $\partial\lambda/\partial T$=0.045 nm/˚C (provide by Vixar) for wafer 6538C can be used to calculate the active region temperature shift with bias current.

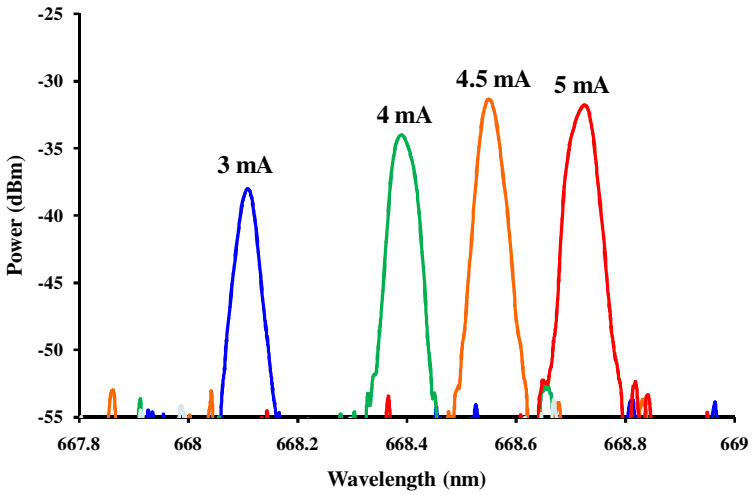


Figure 5.6 Current-dependent fundamental mode shift for the 4 μm aperture diameter red VCSEL (6538C_2-2_1-C-16C_3).

As previously mentioned in Chapter 2, thermal resistance, R_{th} (in ˚C/W) is defined by the ratio of active region temperature raise, ΔT, to the dissipated thermal power, ΔP_{heat}, and is given by [7, 8]

$$R_{th} = \frac{\Delta T}{\Delta P_{heat}} \tag{5.1}$$

where $P_{heat}=IV-P_{opt}$ and I, V, and P_{opt} are CW current, voltage, and output optical power, respectively.

R_{th} can be found by measuring wavelength shift with dissipated power, $\Delta\lambda/\Delta P_{heat}$ and wavelength shift with temperature, $\Delta\lambda/\Delta T$. λ vs. P_{heat} is plotted in Figure 5.7 for the VCSEL discussed in Figure 5.6. As seen in Figure 5.7, wavelength shifts linearly with dissipated power; therefore, thermal resistance can be accurately estimated by the slope of the linear fit to the data points using least squares fit and is determined as R_{th}=(0.087 nm/mW)/(0.045 nm/˚C) = 1.93 ˚C/mW.

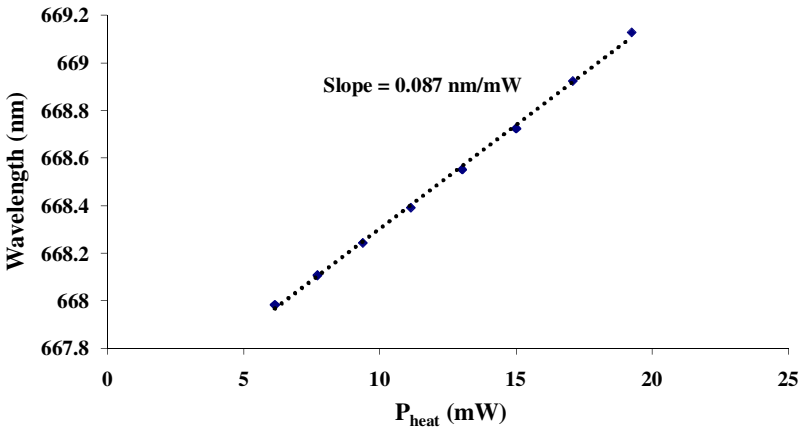


Figure 5.7 $\Delta\lambda/\Delta P_{heat}$ measurement for VCSEL 6538C_2-2_1-C-16C_3

There is also a simple model that was already discussed in Chapter 4 to describe the heat flow of a uniform temperature circular area with diameter d into a semi-infinite substrate with thermal conductivity ξ. It will be a valid approximation for VCSELs mounted on top of relatively thick substrates. R_{th} from this model is given by [9]

$$R_{th} = \frac{1}{2\xi d}. \tag{5.2}$$

This equation was employed to fit R_{th} data for different active diameter VCSELs. In Figure 5.8, the R_{th} experimental data has been plotted as a function of VCSEL active region diameter along with the least squares fit to (5.2) using the Matlab curve fitting tool. Using this method, effective thermal conductivity of this epitaxial material, ξ is approximated as 0.64 W/˚C-cm. Effective thermal conductivity measured for one of the 980 nm wafers was 0.7 W/˚C-cm. The measured effective thermal conductivity for the red VCSELs is surprisingly very close to the one measured for IR VCSELs. This may be an indication of GaAs substrate being a dominant factor in effective thermal conductivity of both samples.

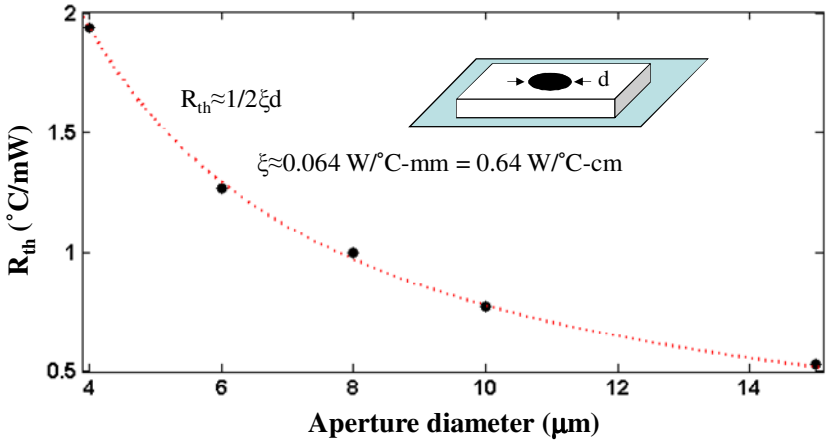


Figure 5.8 R_{th} as a function of VCSELs aperture diameter for sample 6538C_2 along with the fit to the experimental data before plating.

Thermal resistance was also measured for VCSELs on sample 7296B_2 before electroplating copper. Typical R_{th} values for variety of devices on sample 7296B_2 along with the fit are given in Figure 5.9. Devices on sample 7296B_2 generally exhibit larger R_{th}s and smaller effective thermal conductivity compared to 6538C_2.

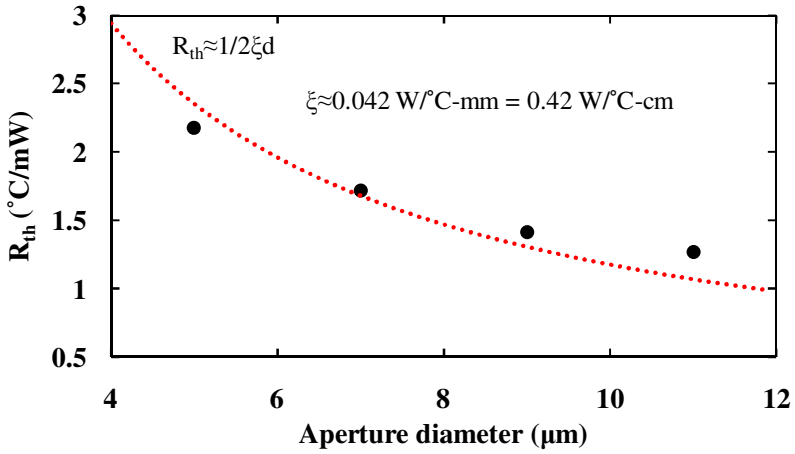


Figure 5.9 R_{th} as a function of VCSELs aperture diameter for sample 7296B_2 along with the fit to the experimental data before plating.

Data presented in Figures 5.8 and 5.9 are expressed on the log-log axes in Figure 5.10. The fitted lines to the data indicates that $R_{th}=7.47d^{-0.976}$ and $R_{th}=6.65d^{-0.696}$ are the best fits corresponding to samples 6538C_2 and 7296B_2. Unlike sample 7296B_2, the slope of the fitted line to sample 6538C_2 is close to -1, which also can be seen from Figure 5.8 with the good fit.

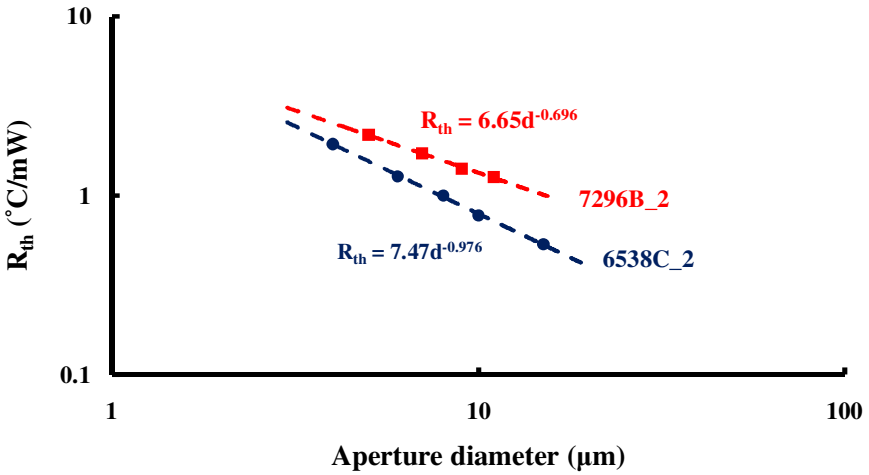


Figure 5.10 R_{th} of samples 6538C_2 and 7296B_2 as a function of aperture diameter on the log-log axes.

5.4. VCSELs characterization after Cu electroplating

In order to enhance the yield of the plating process, both samples were cleaved in half and plated each half at a time. SEM pictures in Figure 5.11 show the 1st half with ~3 µm plated Cu thickness and a rough plating surface and the 2nd half with much thicker plated Cu (~10 µm) and a smoother surface for sample 6538C_2.

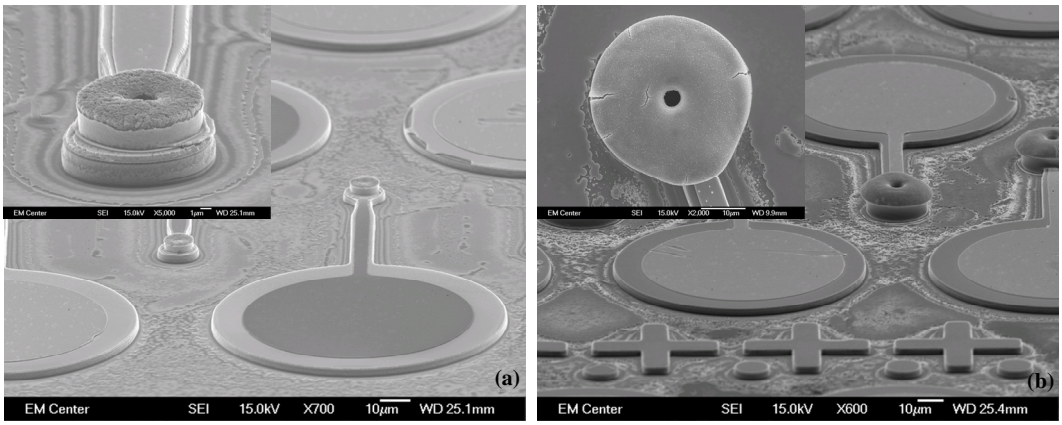


Figure 5.11 SEM pictures of (a) 1st half and (b) 2nd half of sample 6538C_2.

As mentioned in Section 5.2.2 a layer of AZ4400 photoresist with ~3 μm thickness was used to protect different portions of the sample such as VCSEL mesas from plating. In this case with a thicker electroplated Cu than the photoresist thickness, formation of plated Cu on top of the photoresist layer makes a very small opening or even a closed laser aperture after plating. This issue might cause two main problems which are 1) lowering the output power because of obscuring the aperture by Cu and 2) facing some difficulties in cleaning the laser facets after plating. The SEM picture in Figure 5.12 has been taken from the 2nd piece of sample 6538C_2 with ~10 μm plated Cu and illustrates very small mesa openings for plated VCSELs compared to non-plated ones. This problem might be solved with having a thinner plated Cu than the photoresist used in plating lithography step.

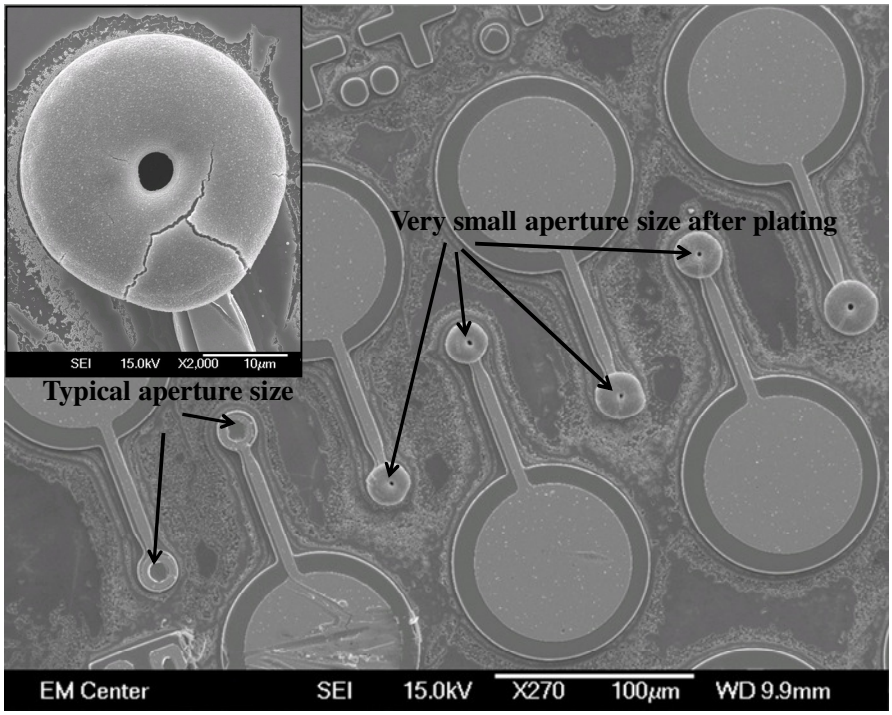
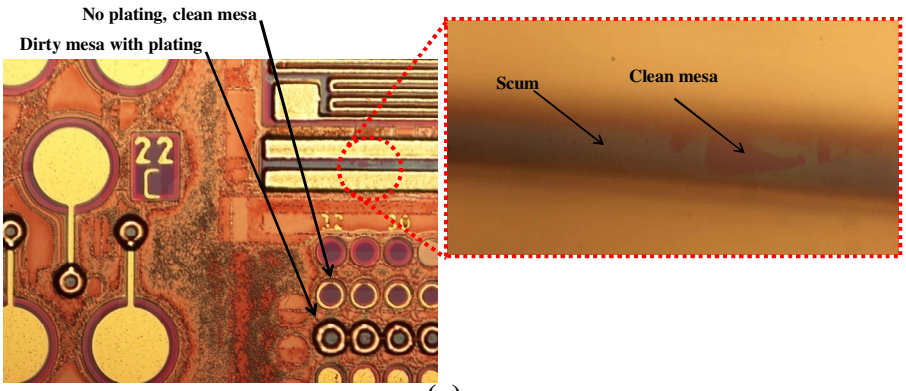


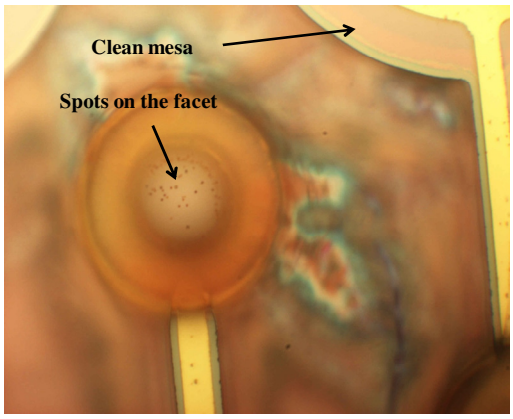
Figure 5.12 SEM picture of 20 μm mesa VCSELs on sample 6538C_2 with small apertures after plating. The inset shows a mesa with nominal inner plating diameter of 12 μm but real inner plating diameter of ~3 μm.

Another issue that needs to be considered for sample 6538C_2 is two types of scum on the plated VCSEL facets after plating as shown in Figure 5.13. Figure 5.13(a) shows a layer of residue on the sample before removing the SiN_x from the laser facet. This residue can be almost entirely removed by Ar plasma sputtering, meaning that it is most likely to be metal, possibly from the seed layer or Cu plating. Figure 5.13(b) shows a VCSEL mesa after removing the SiN_x from the laser facet. Although in this case, there is no more scum of the type shown in Figure 5.13(a), dark spots appear on the facet. EDX analysis showed that these dark spots are mostly gold and possibly from the plating seed layer. Metal particles on the facet might cause optical power loss in VCSELs and also produce

inconsistent DC measurements due to random distribution of residue from VCSEL to VCSEL.



(a)



(b)

Figure 5.13 Scum on the laser facets, (a) before and (b) after removing SiN_x from facets.

This processing issue like the previous one was solved for latter samples by replacing the thin layer of LOR10B used underneath the seed layer with a thick layer (~3 μm) of AZ4400 photoresist.

5.4.1. LIV characterization

LIV measurement has been performed after Cu plating on the sample. Unfortunately for sample 6538C_2, only a few VCSELs among the ones I measured before plating worked afterwards mainly because of processing issues in the plating step.

However, most of the plated VCSELs with large outer plating diameters performed well after plating. Average output power and average threshold current have been plotted in Figure 5.14 for four different aperture diameters on the 1st half sample before and after plating. As it is obvious from the figure, average output power increases linearly with aperture diameter particularly before plating. After plating, the average output power for the smallest aperture (2 µm) VCSEL increases, while it decreases for bigger devices. Average threshold current data also shows lower threshold current for the 2 µm aperture device and larger or equal threshold current for bigger devices after plating. We should keep in mind that the statistical analysis shown in Figure 5.14 applies an uncertainty to data analysis.

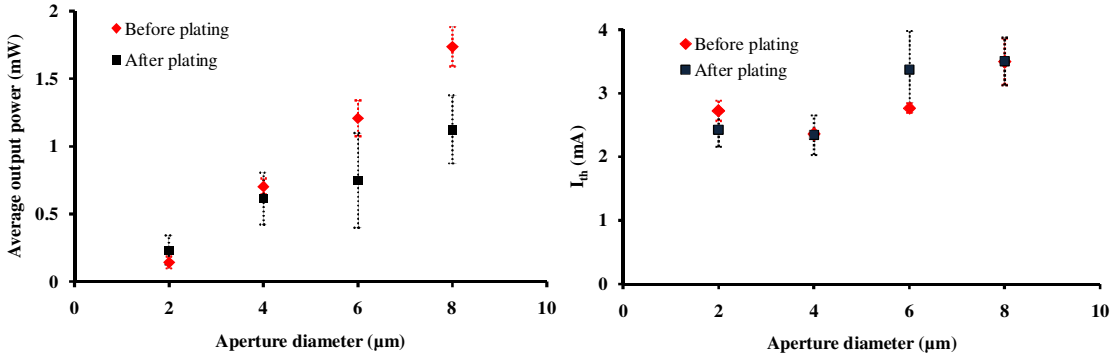


Figure 5.14 Average output power and threshold current before and after plating as a function of aperture diameter for the 1st half piece of sample 6538C_2. Error bars are representing the standard deviation. Data after plating for each aperture size consists of VCSELs with different d_{norm}.

The data reported after plating for each aperture size consist of VCSELs with different plating sizes as expressed in Table 5.3. Error bars in Figure 5.14 show that the experimental result before plating is more consistent than after plating for both plots. The processing issues mentioned in Section 5.4 might cause this problem.

Table 5.3 d_{norm} for the VCSELs reported in Figure 5.13 after plating.

d_{norm} for 2 µm aperture VCSELs	**d_{norm} for 4 µm aperture VCSELs**	**d_{norm} for 6 µm aperture VCSELs**	**d_{norm} for 8 µm aperture VCSELs**
3	2.25	1.333	1.167
3.25	2.6	1.333	1.143
2	1.167	1.333	1.143
1.4	2.6	1.333	1.143
2	1.167	1.333	1.167
3.25	2.6	2.167	1.143
1.4	2.6	2.167	1.143
1.4	2.6	1.333	
3.25	2.6	1.333	
	2.25	1	
	2.6	1	
	2.6		
	2.6		
	1.167		

Similar plots as the ones presented in Figure 5.14 for sample 6538C_2 are depicted in Figure 5.15 for sample 7296B_2. In this case the exact same devices were available before and after plating, thus their LIV curves were measured to compare the results which mostly depend upon the plated Cu.

Typical LIV curves of two VCSELs with 5 µm and 11 µm aperture diameters from sample 7296B_2 before and after plating are presented in Figure 5.16.

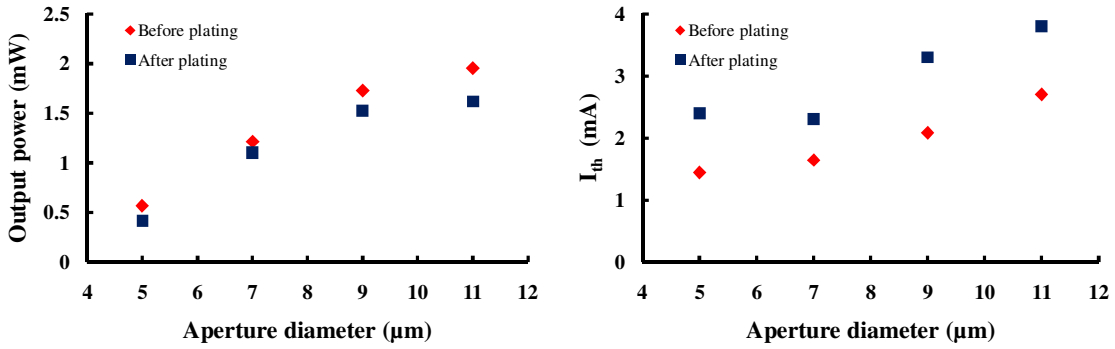


Figure 5.15 Output power and threshold current for the same devices on sample 7296B_2 before and after plating as a function of aperture diameter.

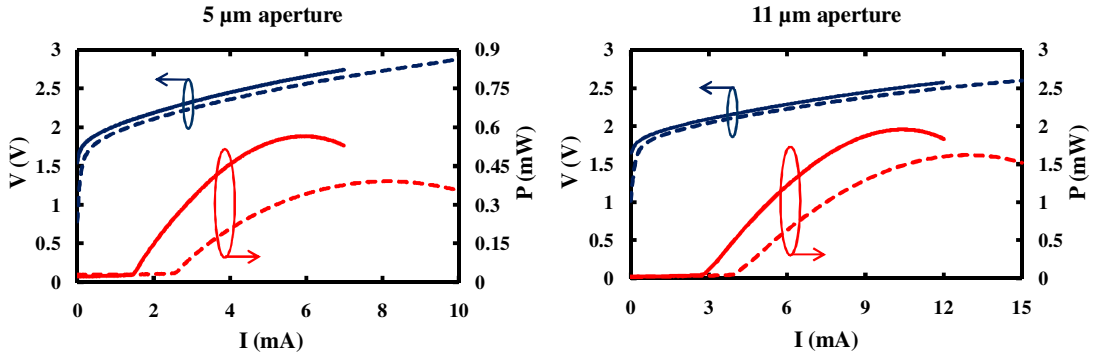


Figure 5.16 LIV curves of typical VCSELs on sample 7296B_2 before and after plating. Solid and broken curves are corresponding before and after plating data.

The presented LIV data contradicts the expected result which is increasing the output power and decreasing the threshold current after Cu plating. Metal heatsinking was already shown to increase the output power [3, 4] and decrease the threshold current [3] of VCSELs due to reduced thermal resistance and thus active region temperature. This result can be attributed mostly to some mechanical effects on VCSEL mesas caused by the plated Cu and less to covering a small portion of the VCSEL facet by the Cu. Stress induced by plated Cu will be discussed later in this chapter.

5.4.2. Thermal resistance measurement

Thermal resistance has been measured for VCSELs with different mesa and plating sizes for sample 6538C_2, both the 1st and 2nd half pieces and plotted in the same graph for better analysis of the results. VCSELs' R_{th} with 14, 16, and 18 µm mesa diameters (2, 4, and 6 µm aperture diameter) from the 1st half and VCSELs with 16, 17, 18, and 20 µm mesa diameters (4, 5, 6, and 8 µm aperture diameter) from the 2nd half sample with different plating sizes have been plotted in Figures 5.17 and 5.18 as a function of VCSEL number and d_{norm}, respectively. The inner and outer plating diameter and inner annular p-contact diameter which vary for each VCSEL number are also presented in Table 5.4 as a function of VCSEL mesa diameter, *d* with 6 µm oxidation length.

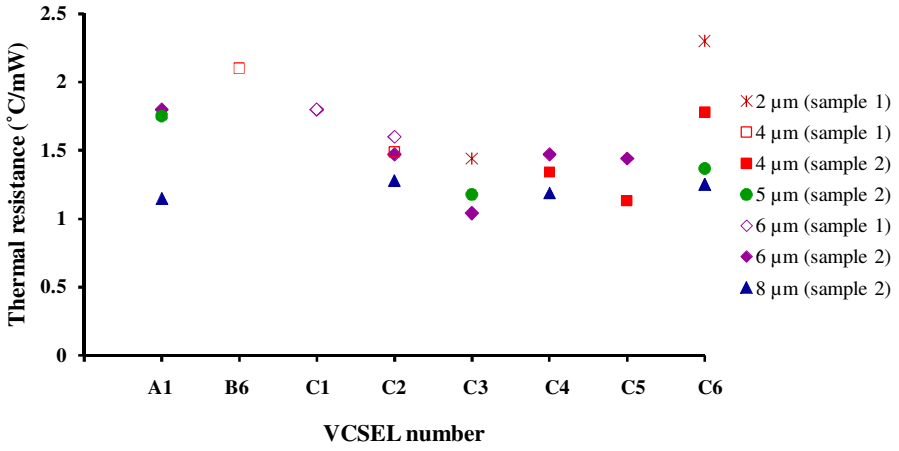


Figure 5.17 R_{th} after plating for different VCSELs from sample 6538C_2 vs. VCSEL number. Aperture diameter of the VCSELs are given in the legend.

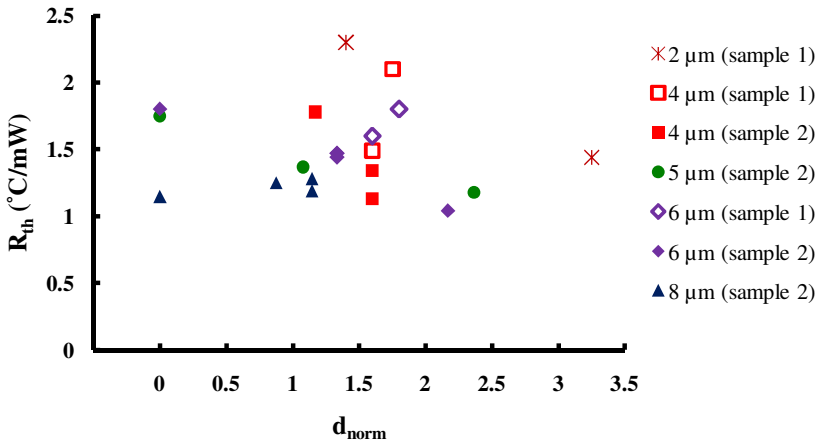


Figure 5.18 R_{th} after plating for different VCSELs from sample 6538C_2 vs. d_{norm}.

Table 5.4 Summary of VCSEL properties.

VCSEL number	Inner annular p-contact diameter	Outer plating diameter	Inner plating diameter
A1	d-10	no plating	no plating
B6	d-10	d+8	d-8
C1	d-10	d+10	d-8
C2	d-10	d+10	d-6
C3	d-10	d+20	d-6
C4	d-12	d+10	d-6
C5	d-8	d+10	d-6
C6	d-8	d+10	d-4

This result indicates that VCSELs with larger plating outer diameter and smaller plating inner diameter generally have lower thermal resistance. Thermal resistance data presents, for example, a lower R_{th} for VCSEL C3 than A1 for the 5 µm aperture device. However, measured LIV characteristics at different temperatures on both samples showed that the unplated VCSEL A1 is capable of operating up to a higher temperature (50 ˚C) than C3 which operates only up to 45 ˚C even though it has a lower R_{th}. Figure 5.19 presents a plot of maximum operating temperature as a function of R_{th} for several

VCSELs. Each data point represents a VCSEL with marked active diameter and device number.

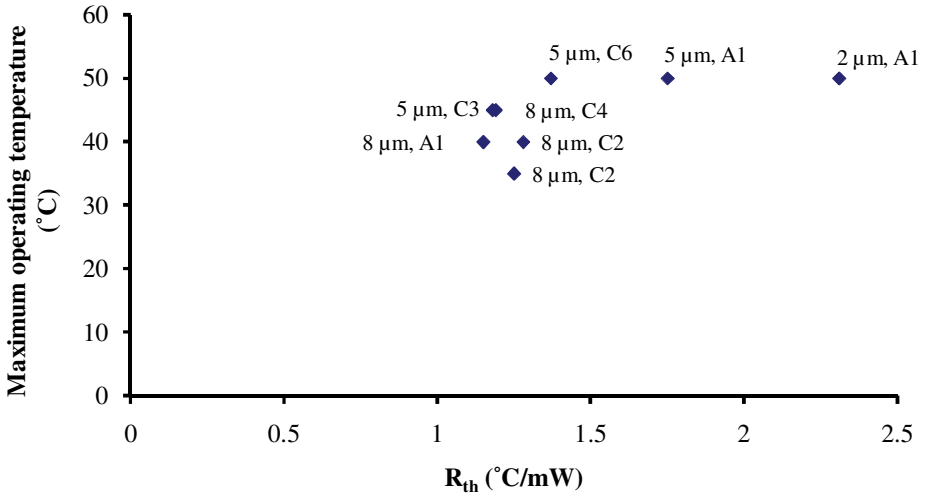


Figure 5.19 Maximum operating temperature vs. R_{th} for several red VCSELs from sample 6538C_2.

R_{th} data for sample 7296B_2 after plating is presented in Figure 5.20 along with the data before plating to better compare the effects of Cu plating on the VCSELs R_{th}. This data exhibits ~20% to 31% reduction in R_{th}s after plating which can be associated with both thermal and mechanical effects. Metal heatsinking has already been shown to reduce R_{th} by improving the lateral heat flow from the active region to the substrate via the Cu on sidewalls rather than through the bottom mirror [3]. This fact can also be the case here for red VCSELs. Although, appearance of some unexpected result in DC measurement cannot be explained by only considering the thermal model, and thus a more complete model needs to address this result. This model takes into account the stress induced on the plated mesas by the copper.

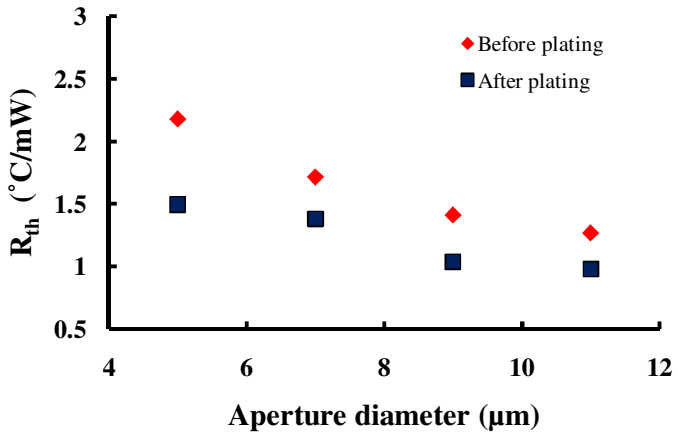


Figure 5.20 R_{th} for devices on sample 7296B_2 before and after plating.

5.5. Effects of stress in Cu plated VCSELs

In order to better study the effect of electroplated copper on DC characteristics of red VCSELs, L-I curves and R_{th}s of VCSELs were measured. Although R_{th} behaves in an expected way, i.e., decreasing after plating, threshold current and output power show an unexpected behavior after plating. This result is different from what can be explained by only a thermal model of Cu on VCSEL mesas, and thus another model is needed to explain this behavior. This section explains how Cu plating applies stress on the mesas and how this stress causes unexpected behavior in DC properties of these red VCSELs. For this section, VCSELs from sample 7296B_2 with ~11 µm aperture diameter in 22 µm diameter mesa and different plating sizes were measured.

The stress model explained here considers two scenarios associated with the donut shape plated Cu on top and around mesas. The first scenario happens when the mesa is plated by Cu but the VCSEL is off. This *initial* stress comes from the nature of the plated Cu and can be compressive or tensile depending on the plating conditions [10]. The

initial stress which depends on the amount of plated Cu on and around mesas may be increased by increasing d_{outer} and/or decreasing d_{inner}. The next stress-related effect comes into play when the laser is turned on, i.e. with the existence of a heat source, and so is called a *heat-induced* stress. Mismatch between coefficients of thermal expansion for Cu (17×10^{-6} 1/K) and GaAs (6.4×10^{-6} 1/K) results in Cu expansion of more than 2.5 times that of GaAs at the same temperature. It should be noticed that the regions close to the mesa axis show a higher temperature raise than the regions close to the mesa perimeter and thus expands more than mesa perimeters. These expansions vary with the amount of temperature raise at each point and Cu size on and around mesas. Defining a normalized plating size for different VCSELs with identical mesa diameters, assists in comparing the effect of plating size on the DC properties of VCSELs. The normalized plating size is defined as $d_{norm}=((d_{outer}-d_{inner})/d_{inner})$ where d_{outer} and d_{inner} correspond to the outer and inner diameter of the plated copper. The parameter d_{norm} increases (decreases) by either increasing (decreasing) d_{outer} or decreasing (increasing) d_{inner}. It means that a device with bigger d_{inner} exhibits a decreased R_{th} due to an improved heatsinking by covering a bigger area of mesa as seen in the simulation results presented in the previous section. It is also possible to see more stress effects on the mesas with increased d_{norm}. As previously mentioned, two parameters are needed for R_{th} measurement of VCSELs, i.e. $\Delta\lambda/\Delta P_{heat}$ and $\Delta\lambda/\Delta T$. The later was already measured for sample 7296B_2 as ~0.05 nm/˚C before plating and is typically assumed to only vary with the semiconductor material parameters and the epitaxial structure used but not with device fabrication. However, it is beneficial to measure $\Delta\lambda/\Delta T$ for each device and then calculate true R_{th}. Both $\Delta\lambda/\Delta T$ and R_{th}, plotted as a function of d_{norm} in Figure 5.21 are reduced with increasing plating size. The

measured $\Delta\lambda/\Delta T$ for the VCSELs with different plating sizes shows that it decreases with increasing d_{norm}; however, the change is not large. The scatter in the data can be associated with the nonuniformity of devices over the sample. For an example, a 0.18 nm variation in cold-cavity wavelength was also observed for the measured VCSELs, although it seems unlikely that such a small wavelength variation could cause such large scatter in R_{th}.

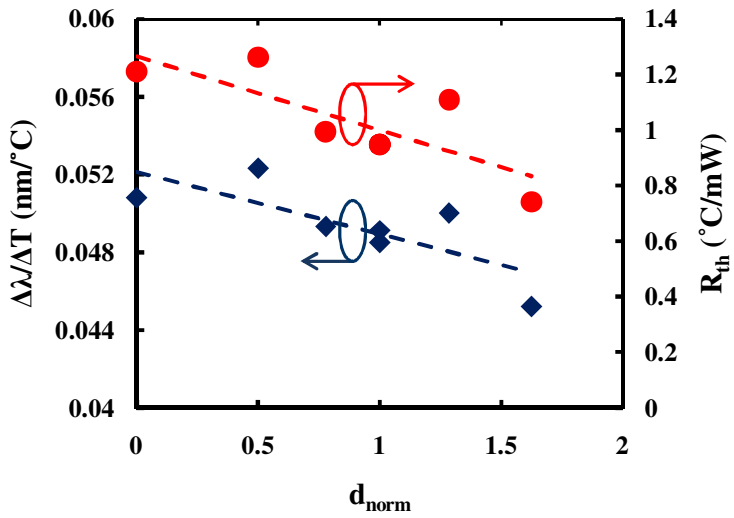


Figure 5.21 $\Delta\lambda/\Delta T$ and R_{th} as a function of d_{norm}.

Stress in VCSELs might cause a different $\Delta\lambda/\Delta T$ through changes in parameters such as laser cavity mode and thermal expansion as expressed by Equation (2.46) in Chapter 2.

Another VCSEL parameter that changed from one plating size to another is I_{th}. As mentioned in Section 5.4.1 I_{th} increases after plating which contradicts the expected result if only heating is considered. I_{th} is plotted in Figure 5.22 as a function of d_{norm} for the devices with already reported R_{th}. The observed increase in I_{th} by a factor of 2 cannot be described by only considering thermal effects of the plated Cu and their effects on reducing R_{th} without including stress effects. To better understand this contradiction, the

temperature difference at threshold, ΔT_{th}, is calculated for two VCSELs with d_{norm}=0 and 1.625 with corresponding R_{th}=1.2 and 0.78 ˚C/mW, both with 22 μm mesa diameters. Assuming both VCSELs have equal I_{th}=3 mA and V_{th}=2.1 V at room temperature, ΔT_{th} can be estimated as $\Delta T_{th}=3\times2.1\times(1.2-0.74)=2.9$ ˚C. The rate of I_{th} change with temperature will be shown later in this section to be ~0.1 mA/˚C at room temperature for the VCSEL with d_{norm}=0 which results in ~0.3 mA variation in I_{th} due to the change in R_{th}. Therefore, increasing the I_{th} from ~3 mA to 6 mA cannot be originated from the change in R_{th}. Another important factor that needs to be noted is that the VCSELs reported here have a positive gain-mode offset at room temperature that causes I_{th} to increase with increasing temperature. Therefore, temperature reduction by means of reducing R_{th} via Cu plating is expected to reduce the I_{th}, while Figure 5.22 shows an increase in I_{th}.

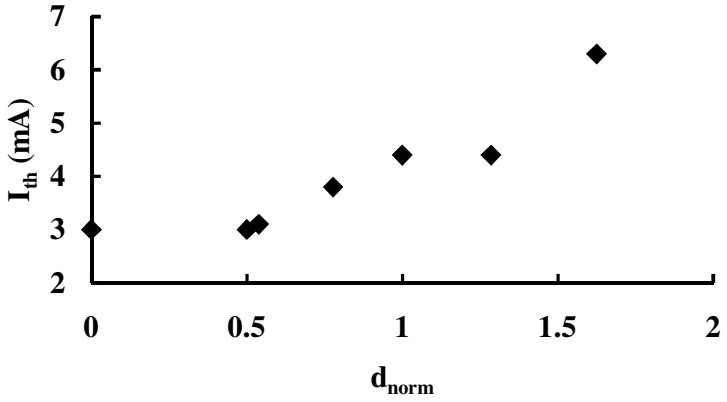


Figure 5.22 I_{th} as a function of d_{norm}.

In order to explain the measurement results we need to introduce a model that accounts for the stress applied to mesas by the plated Cu. In addition to improving the thermal resistance, increasing the normalized plating size (larger d_{norm}) also increases the

stress on the mesas. The stress can alter different laser properties such as threshold current density, optical gain, wavelength, polarization, characteristic temperature, linewidth enhancement factor, and relaxation oscillation frequency [11]. The change in most of these parameters arises from changes in the valence-band structure and its effects on degeneracy and band-to-band transitions [11]. Figure 5.23 represents typical valence band splitting and shifts caused by compressive and tensile strain for III-V semiconductors [12]. These modifications in band structure affect laser behavior via changes in parameters such as hole effective mass and band gap energy, E_g. For example, E_g shrinking (widening) leads to a red (blue) shift in the gain-peak wavelength and thus causes an operating wavelength shift in EELs and gain-mode offset (gain peak wavelength/cavity wavelength alignment) change in VCSELs.

Another result of band gap modification can be associated with the change in threshold current which is proportional to the transparency current. The transparency current itself is proportional to the square root of carrier masses and inversely proportional to the carrier lifetime [11]. Strain can either decrease or increase threshold current depending on which factor is dominant. In larger band gap semiconductors such as GaAs the Auger recombination is smaller and thus the lifetime is much larger than smaller band gap materials. Therefore, the hole mass effect is expected to be the dominant cause for threshold change. In contrast, the smaller band gap materials such as InP may have stronger effects related to band-to-band transitions that directly affect the Auger recombination processes [11]. It is not, therefore, impossible to observe different trends for laser parameters as a result of strain in different materials and structures. For instance, decrease in threshold current density with increased tensile strain for InGaAs

single QW lasers has been reported in [13], while H. Temkin et al. reported on higher threshold current in InGaAs-InP QW lasers subjected to tensile strain [14].

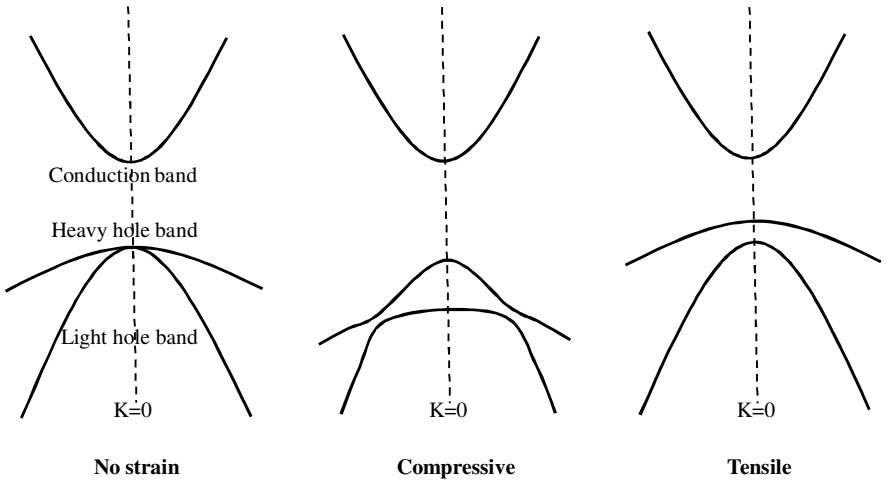


Figure 5.23 Valence band modifications due to the compressive and tensile strain.

(Reproduced from [12])

Unlike EELs, gain-mode offset dominates the temperature dependence of I_{th} in VCSELs; therefore, analyzing the temperature dependence of threshold current gives some useful insight about VCSEL gain-mode offset and better explains the effect of stress on VCSEL mesas. Minimum I_{th} ($I_{th,min}$) in VCSELs approximately occurs at a temperature that the mode is aligned with the gain peak (T_{min}) and it increases from its minimum value when temperature increases or decreases from T_{min}. Therefore, positive gain mode offset (mode wavelength blue shifted with respect to gain peak wavelength) at room temperature (T_{room}) leads to a $T_{min}<T_{room}$, while a negative gain-mode offset (mode wavelength red shifted with respect to gain peak wavelength) at T_{room} leads to a $T_{min}>T_{room}$. As previously mentione, stress can modify the valence band and change the energy gap and thus shift the gain spectrum. Depending on the direction of gain-mode

offset at room temperature, T_{min} either decreases or increases with the shift in gain spectrum. Plotting the VCSELs' I_{th} as a function of temperature for different plating sizes, one can fit a simple parabolic model to relate I_{th} to temperature, i.e, $I_{th}=I_{th,min}(1+\alpha(T-T_{min})^2)$, and extract $I_{th,min}$, α, and T_{min}. $I_{th,min}$ is the minimum threshold current which occurs at $T=T_{min}$ and α is an indication of the $I_{th}(T)$ function curvature and thus temperature sensitivity of lasers [15]. It is useful to plot extracted T_{min} and α for devices with different plating sizes as functions of their R_{th} to find a correlation between plating and device stress by comparing the experimental result with the no stress model. Plotting these parameters as functions of R_{th} rather than d_{norm} eliminates the effect of possible deviations in the real d_{norm} from its nominal value. Figure 5.24 shows that both T_{min} and α are anti-correlated with R_{th}.

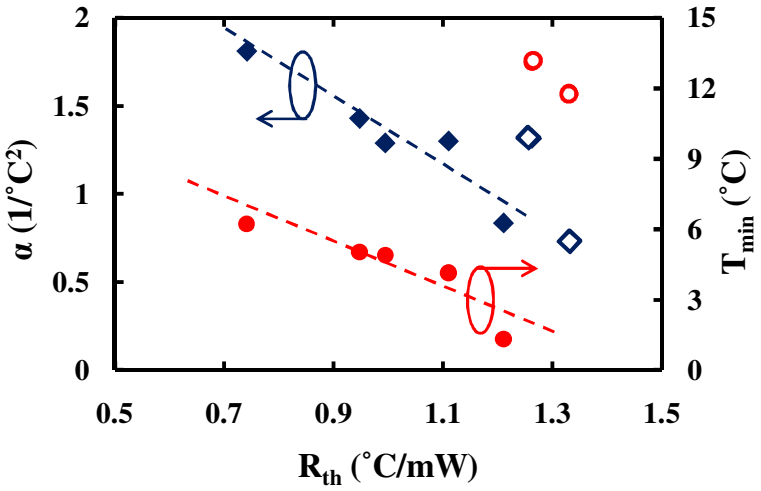


Figure 5.24 α and T_{min} versus R_{th}. Dashed lines represent the fits to the solid circles and diamonds.

Expected behavior of $T_{min}(R_{th})$ and $\alpha(R_{th})$ functions with no stress differs from what is experimentally observed for the sample. If there are purely thermal effects in the plated

devices, for the same amount of heat flux in the structure, the active region temperature or operating wavelength change in a VCSEL with smaller R_{th} is less than that with a larger R_{th}. Difference in thermal resistance alone should not affect zero-bias gain-mode offset or the rate of wavelength change in gain spectrum and cavity mode with temperature. In other words, T_{min} and α should be independent of R_{th}. Data presented in Figure 5.23 contradicts the no stress model indicating that this data needs to be explained by additional factors that may be attributed to stress. R_{th} dependence of both T_{min} and α can be explained by assuming that the copper puts the mesa under stress and thus changes the gain mode offset of the structure. Decreasing T_{min} with R_{th} is an indication of a shift in the gain peak wavelength due to stress caused by plating. Applying Cu on the mesas increases the compressive stress of the semiconductor and thus increases the E_g as also presented in [16]. Increased E_g of the quantum well material causes a blue shift in gain spectrum resulting in a smaller gain mode offset for the VCSELs with positive zero-bias gain-mode offset at room temperature. Smaller gain mode offset reduces the temperature change required to reach $I_{th,min}$, and thus makes T_{min} larger for lasers with more stress, i.e. less R_{th}, as seen in the presented data. Increases in the α parameter for 980 nm VCSELs under strain in epitaxial has also been reported in literature [15].

Parameter T_{min} is used to estimate the bandgap expansion for the VCSELs under stress. To compare the amount of expansion, the gain-mode offsets of two 22 μm mesa diameter VCSELs one without Cu (d_{norm}=0) and one with largest d_{norm} (d_{norm}=1.625) are estimated using the equation below

$$\lambda_{gain}(T=T_{room}) - \lambda_{mode}(T=T_{room}) = \left(\frac{\partial \lambda_{gain}}{\partial T} - \frac{\partial \lambda_{mode}}{\partial T}\right)(T_{room} - T_{min}) \qquad (5.3)$$

where λ_{gain} (λ_{mode}) and $\partial\lambda_{gain}/\partial T$ ($\partial\lambda_{mode}/\partial T$) are corresponding the gain peak (mode) wavelengths and their rate of change with temperature. Assuming $\partial\lambda_{gain}/\partial T$=0.2 nm/˚C, T_{room}=25 ˚C, and using the measured values for $\partial\lambda_{mode}/\partial T$ and T_{min} for each device, one can estimate gain-mode offsets as 3.6 nm and 2.9 nm for VCSELs with d_{norm}=0 and d_{norm}=1.625, respectively. Since the mode wavelength shift with stress can be considered to be much less than the gain spectrum shift, the gain peak wavelength shift with stress after plating, $\Delta\lambda_{gain}$ equals 0.7 nm with neglecting the mode wavelength shift. Energy gap expansion due to stress can be expressed as

$$\Delta E_g = -\frac{hc}{\lambda_{gain}^2}\Delta\lambda_{gain} \tag{5.4}$$

where h is Planck constant and c is speed of light. With λ_{gain}=670 nm, ΔE_g is approximated as 2 meV. This value can quantify the amount of compressive stress induced by Cu on the mesa. The rate of energy gap change with pressure, $\partial E_g/\partial P$ for GaInP has already been reported to be in the range of 70-80 meV/GPa [17, 18]. Use of the reported values for $\partial E_g/\partial P$ in conjunction with the estimated ΔE_g=2 meV gives rise to ~ 30 MPa pressure on the mesa which is in agreement with the reports on the internal stress in electroplated Cu films [19].

Next section will discuss some results on the thermal modeling of VCSELs with different plating sizes to better understand how thermal resistance changes with plating size with absence of any stress.

5.6. VCSEL thermal modeling

In this section, the effect of Cu on the temperature distribution and thermal resistance in a typical top-emitting oxide-confined red VCSEL is numerically simulated

using COMSOL Multiphysics software. The program utilizes a finite element method (FEM) to simulate a variety of physical problems such as heat transfer, Joule heating, and solid mechanics. The heat transfer module is employed in this section to study the heat distribution in a typical VCSEL structure, which is mainly due to generated heat flux in the VCSEL active region by applying the electric current to it. The heat equation as the mathematical model for heat transfer in solids can be expressed by [20]

$$\rho C_p \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q \tag{5.5}$$

where ρ is the mass density of material, C_p is the heat capacity, k is the thermal conductivity, and Q is the heat generated per unit volume. In steady state the first term in Equation 5.5 disappears and the equation reduces to

$$\nabla \cdot (k \nabla T) + Q = 0 \tag{5.6}$$

which is similar to the heat transfer in fluids at steady state with no fluid velocity field. The VCSEL mesa was surrounded by air in these simulations.

The heat transfer problem was solved by defining an initial value of room temperature (20 ˚C) for all domains and temperature boundary condition for keeping all outer sides of the device at room temperature at any time.

5.6.1. Device structure

The VCSEL studied here has a 22 μm mesa diameter with 6 μm oxidation length similar to the fabricated and characterized red VCSELs discussed earlier in this chapter. Since VCSELs are symmetric with respect to the z-axis in the cylindrical coordinate system with three curvilinear coordinates (r, φ, z), the axis symmetry option in COMSOL

was chosen to simplify the problem. Therefore, this model performs a 2D simulation in the **r** and **z** directions for an arbitrary azimuth angle **φ**. The VCSEL consists of 6 µm and 4 µm thick n-type and p-type DBRs, respectively, both with alternating quarter wave layers of ($Al_{0.5}Ga_{0.5}As$/ $Al_{0.92}Ga_{0.08}As$) above a GaAs substrate. A 6 µm long, 100 nm thick oxide layer was placed 1.5 µm above the bottom of the p-type DBR. The active region is formed below the oxide layer right at the junction of p- and n-type DBRs with a length of 6.5 µm and thickness of 200 nm. Copper layers with a variety of inner and outer diameters and thicknesses were formed on and around mesas and extended outside the mesas on the surface of n-type DBR, while the VCSEL aperture is not covered by Cu. A cross section of the simulated device is shown in Figure 5.25.

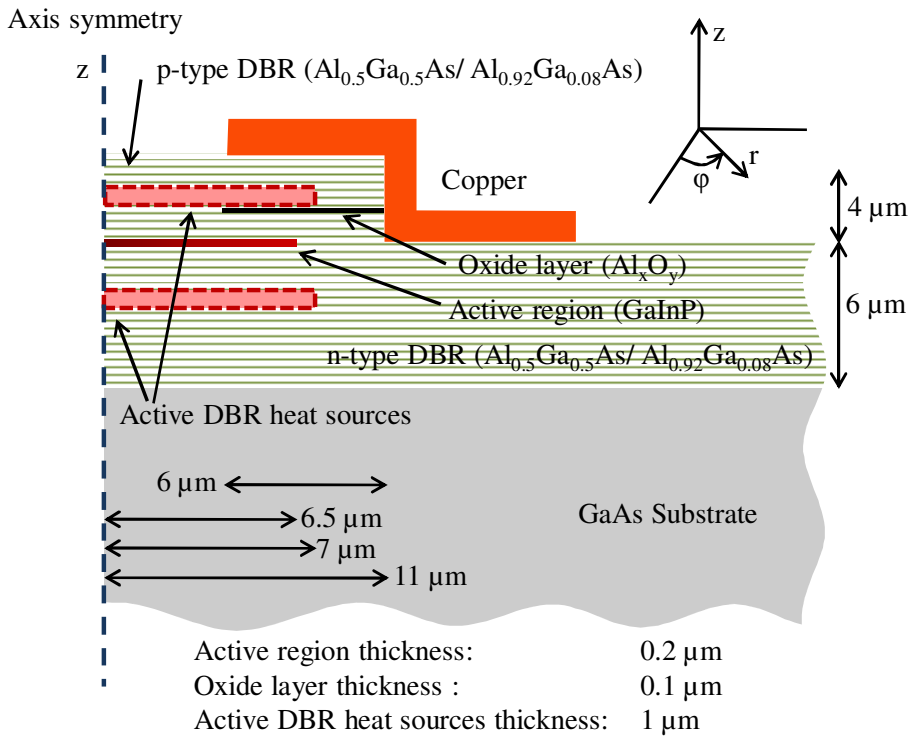


Figure 5.25 Cross section of the simulated red VCSEL.

In order to better model the effect of temperature on the structure, two active DBR heat sources are placed in the p- and n-type DBRs to mimic the Joule heating effects in the DBR mirrors. Although the software is capable of coupling the Joule heating and heat transfer problems, these two effects could not be properly coupled and used at the time of writing this dissertation. Large current density in the Cu resulted in a much larger Joule heating in the Cu than mirrors.

5.6.2. Material parameters

The expression for heat transfer in solids mentioned in Equation 5.5 indicates that three different constants need to be defined for each material in the model. These parameters are density, ρ, heat capacity, C_p, and thermal conductivity, k. Vertical and lateral thermal conductivities (k_v, k_l) for the laminar DBR mirrors were estimated from the k values and thicknesses of $Al_{0.5}Ga_{0.5}As$ and $Al_{0.92}Ga_{0.08}As$ and using equations below [21].

$$k_v = \frac{d_1 + d_2}{d_1/k_1 + d_2/k_2}, \quad k_l = \frac{d_1 k_1 + d_2 k_2}{d_1 + d_2} \tag{5.7}$$

where d_1 (d_2) and k_1 (k_2) are corresponding to the thickness and thermal conductivity of layer 1 (layer 2). The other parameters can be estimated by averaging as was done for estimating k_l. The estimated effective parameters for DBR mirrors in a red VCSEL along with the parameters for other materials used in this simulation are summarized in Table 5.5. It is important to note that the real values for thermal conductivities of the DBR mirrors and active region might be larger than those estimated in Table 5.3. This difference is originated from higher thermal conductivity of superlattices than alloys due

to suppression of alloy scattering in the superlattice as reported in [22] for AlAs/GaAs superlattices and AlGaAs alloys.

Table 5.5 Material parameters used in the red VCSEL simulation.

Material	Density (kg/m^3)	Heat capacity (J/kg.K)	Thermal conductivity (W/m.K)
Air	1.2	1012	0.025
Active region ($Ga_{0.5}In_{0.5}P$)	4470	370	6.36
Al_xO_y	3690	880	0.7 [23]
Copper	8700	385	400
DBR mirrors	4209.3	424.96	k_v=16.22 k_l=20.55
GaAs	5360	334.7	$44.05.(300/T)^{1.25(1)}$

(1) Temperrature dependence of GaAs thermal conductivity from [24]

5.6.3. Simulation results

After setting up the device geometry and defining all required parameters, heat sources need to be applied to the structure. The main heat source in the structure is the active region and is assumed to carry 85% of the total heat flux in the device. The remaining 15% comes from the Joule heating of DBR mirrors with 10% and 5% being associated with p-type and n-type DBR, respectively. The heat flux distribution in the device is related to the voltage drop across the active region and DBRs. the 670 nm wavelength corresponds to ~1.85 V which is approximately 85% less than 2.1-2.2 V, the typical voltage observed in the IV measurement. The total heat flux in the device is assumed to be 20 mW (typical 10 mA current and 2 V device voltage) which results in a

6.4×10^{14} W/m^3 active region heat source and 1.8×10^{13} W/m^3 and 9×10^{12} W/m^3 heat sources corresponding to the p- and n-type DBRs.

5.6.3.1. Effect of Cu thickness

For the first set of simulations the effects of Cu thickness on the temperature distribution of the VCSELs are investigated by varying the Cu thickness on top and around mesas from 1 μm to 5 μm. Contour plots of the temperature distribution in a cross sectional plane (r-z plane) of the VCSEL are given in Figure 5.26 for two cases of no Cu and 2 μm thick Cu. It can be immediately seen from the graphs that the maximum temperature in the device which occurs at the active region is 54.37 ˚C -47.22 ˚C=7.15 ˚C higher in the case of no Cu than the case of 2 μm Cu, indicating Cu is reduces the thermal resistance of the VCSEL.

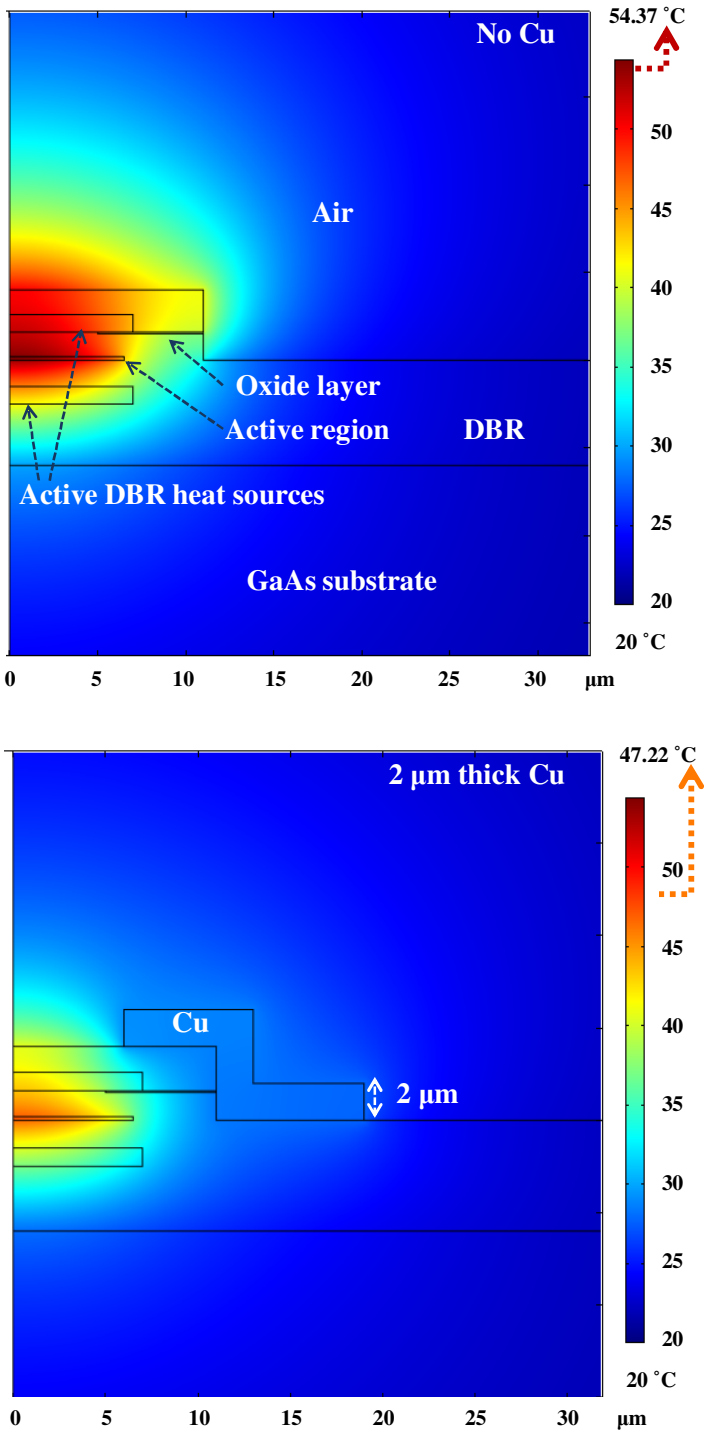


Figure 5.26 Simulated temperature distributions in the VCSEL without Cu (top) and with 2 μm thick Cu (bottom).

Maximum temperature rise in the active region for Cu thicknesses from 1 μm to 5 μm is plotted in Figure 5.27.

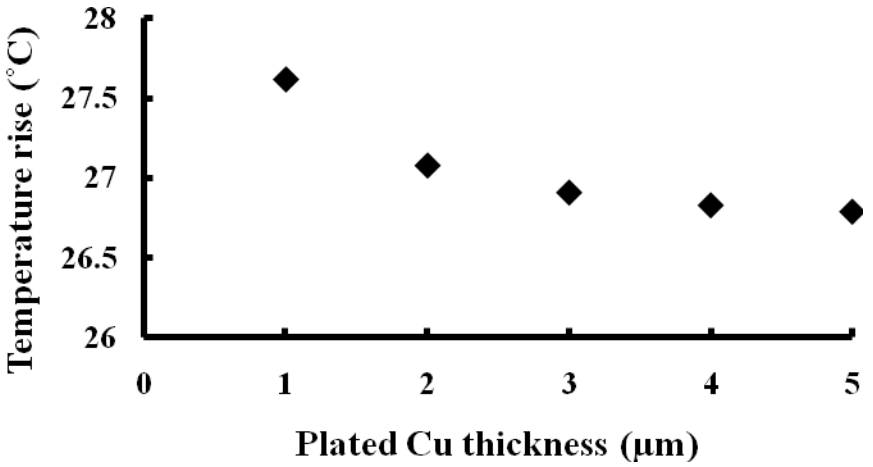


Figure 5.27 Simulated maximum temperature rise in the active region for different Cu thicknesses with d_{inner}=12 μm and d_{outer}=38 μm.

In addition to the fact that the thicker Cu reduces the overall device temperature, it can be also inferred from Figure 5.27 that increasing the Cu thickness to more than 2 μm barely changes the active region temperature. Increasing the Cu thickness from 2 μm to 5 μm improves the thermal resistance only by 1%, while it might significantly increase the stress on the VCSEL mesa. The 2 μm Cu thickness sufficiently reduces the thermal resistance and applies less amount of stress on the VCSEL mesa.

Temperature rise in VCSELs can also be decreased by increasing the mesa diameter. A VCSEL with 40 μm mesa diameter and 10 μm aperture diameter (same as VCSELs presented in Figure 5.26) is simulated and presented in Figure 5.28. This result indicates that the maximum temperature rise in this VCSELs is 50.93 ˚C i.e., smaller than

the simulated VCSEL with 22 µm mesa diameter and no Cu and larger than the one with 22 µm mesa and 2 µm of Cu. This means that using Cu for heatsinking is more effective than fabricating VCSELs with larger mesa diameters.

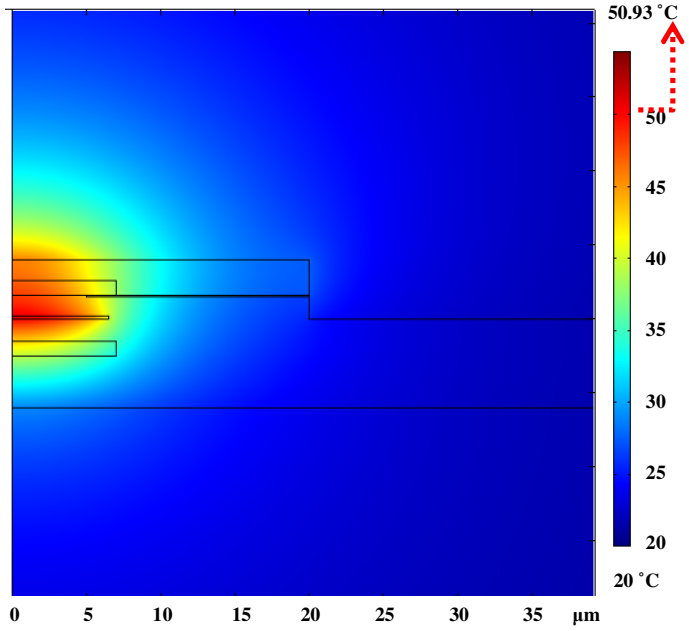


Figure 5.28 Simulated temperature distribution in a VCSEL without Cu, with the same oxide aperture, but a larger mesa than the ones presented in Figure 5.25.

5.6.3.2. Effect of Cu extension on and around mesa

The experimental results presented in the previous chapters indicate that thermal resistance was reduced by increasing d_{norm} and in fact is a function of plating diameter. This thermal resistance reduction was verified by the thermal model. This model indicates that after adding Cu layers to the mesas the effective thermal conductivity of the VCSEL increases, and thus its R_{th} decreases. COMSOL multiphysics is also used to study

the effects of Cu extension on top and bottom of the VCSEL mesas on the device heat distribution and thermal resistance. In this study, the Cu thickness is kept at 2 μm.

For this experiment the 22 μm mesa VCSEL is covered by Cu with different combinations of d_{outer} and d_{inner} as mentioned in Table 5.6.

Table 5.6 different combinations of d_{inner} and d_{outer} used in simulating R_{th}.

d_{outer}/μm	d_{inner}/μm	d_{norm}	R_{th} (˚C/mW)
0	0	0	2.023
22	12	0.833	2.003
22	14	0.571	2.013
22	16	0.375	2.019
22	18	0.222	2.022
28	12	1.333	1.727
28	14	1	1.762
28	16	0.75	1.792
28	18	0.556	1.813
32	12	1.667	1.666
32	14	1.286	1.703
32	16	1	1.734
32	18	0.778	1.757
38	12	2.167	1.602
38	14	1.714	1.641
38	16	1.375	1.674
38	18	1.111	1.699
42	12	2.5	1.571
42	14	2	1.611
42	16	1.625	1.644
42	18	1.333	1.671

The result of R_{th} given by the simulated temperature change and active region heat flux at each case is shown in Figure 5.29 as a function of d_{norm}. VCSELs with no Cu and Cu only on top of the mesas exhibit relatively equal R_{th} regardless of length of Cu on the mesa. These devices also have higher R_{th} than the ones with Cu around mesas. This result is expected because the main role of Cu is to make a high thermal conductivity path to carry the generated heat away from the active region and transfer it to the substrate.

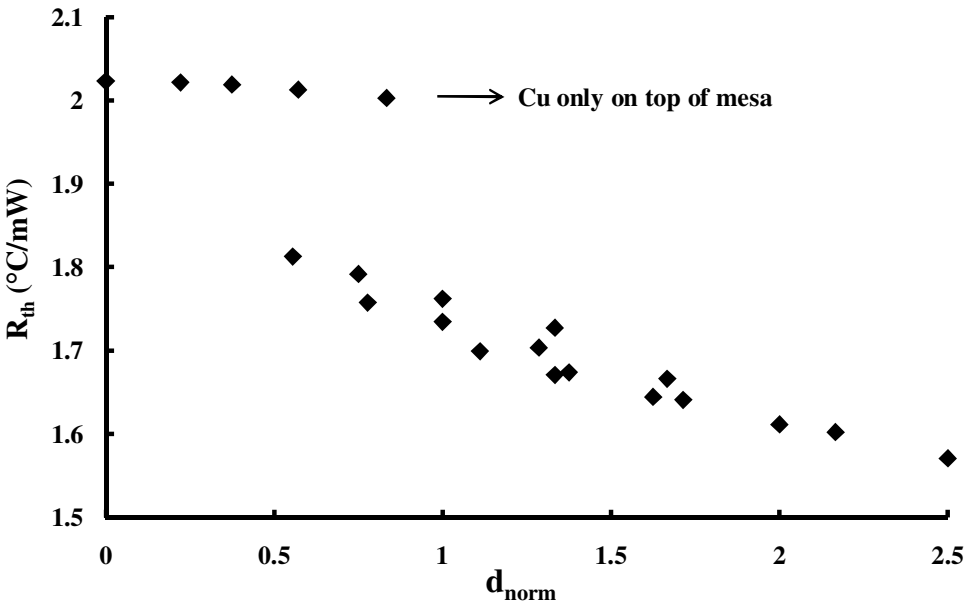


Figure 5.29 Simulated R_{th} as a function of d_{norm} for different combinations of d_{inner} and d_{outer}.

Decreasing R_{th} with increased d_{norm} is another result that can be seen in Figure 5.29 and is also consistent with the experimental results. Although the simulation data falls into a line that follows the trend of decreasing R_{th} with d_{norm}, the data is a little scattered. The scattered simulation result comes from the fact that devices with identical d_{norm} might have different R_{th} because of their different of d_{inner} and d_{outer}. As an example, there are two VCSELs in Figure 5.29 with d_{norm}=1, but slightly different R_{th}. The device with larger d_{outer} exhibits a greater R_{th}. Simulated R_{th} as functions of d_{inner} and d_{outer} Cu is summarized in Figure 5.30 where surface color represents the R_{th}. This graph verifies that R_{th} can be reduced by increasing the d_{outer} and deacresing the d_{inner}.

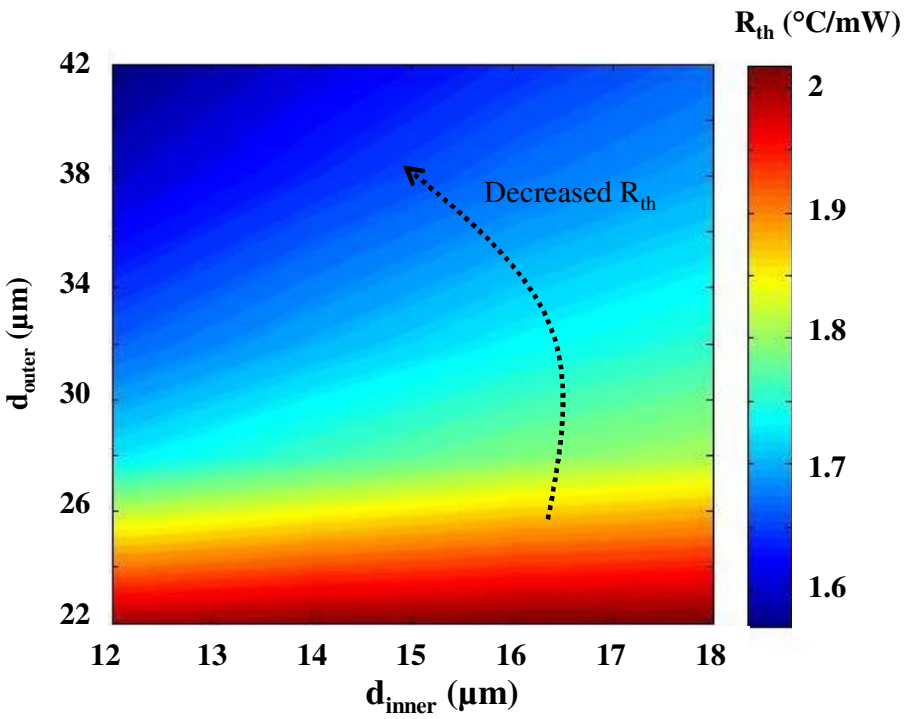


Figure 5.30 Simulated R_{th} for different d_{inner} and d_{outer}.

The experimental results of R_{th} for 22 µm mesa diameter VCSELs as a function of d_{norm} along with the simulation results of the corresponding VCSELs are plotted in Figure 5.31. Simulation 1 employs the typical VCSEL structure used in Section 5.6 and simulation 2 represents the structure with higher thermal conductivity of the n-DBR mirror. The difference in simulation and experimental results can be attributed to the dissimilarities between the real VCSEL structure and the structure used for the simulation.

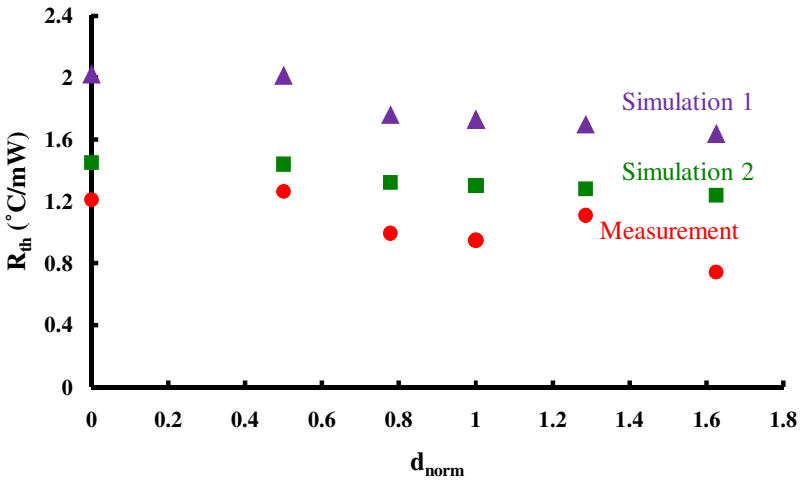


Figure 5.31 Simulated and experimental R_{th} for 22 µm mesa diameter VCSELs vs. d_{norm}. Simulation 1 and simulation 2 results represent different n-mirror definitions.

Some work has been also done on stress modeling of Cu plated red VCSELs by assigning a body load to the Cu film. However, we believe that the results were not quite correct. We need to somehow model the initial stress in the Cu film.

5.7. Conclusions

This chapter described the fabrication and characterization of 670 nm (red) oxide-confined vertical-cavity surface-emitting lasers (VCSELs) that were fabricated and characterized for their DC behavior using thermal management via copper electroplating of mesas. Fabricated VCSELs showed a high output power (>2.5 mW for 15 µm active diameter VCSEL). These VCSELs also had lower thermal resistance than unplated lasers previously fabricated by Vixar from similar material.

VCSELs' R_{th} was shown to decrease with increasing d_{inner} and decreasing d_{outer} of the plated Cu due to reduced effective thermal conductivity of VCSELs by Cu. However,

some unexpected results in I_{th} and output power of VCSELs after plating leaded us to a more complete analysis of the Cu plated mesa and introducing an stress model to explain the unexpected result. In addition to providing better heatsinking, adding more Cu to the mesas by increasing d_{norm} was shown to increase the Cu induced mesa stress.

Thermal and stress modeling of the Cu plated VCSELs were also performed to better understand both thermal and mechanical effects of the Cu on the VCSEL mesas. Some more work is still needed to complete the stress modeling of VCSELs.

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Chapter 6

VCSEL DYNAMICS AND SINGLE MODE OPERATION

6.1. Introduction

As discussed in Chapter 3 there are limiting factors that restrict the VCSEL's modulation bandwidth. One factor that was mainly addressed in the two previous chapters is thermal issues. Excessive junction temperatures may cause a reduction in the differential gain and photon density, both of which decrease the oscillation frequency and thus modulation bandwidth. Two other limiting factors in the VCSEL's frequency response are laser intrinsic bandwidth and optical issues that are discussed in this chapter. VCSEL intrinsic behavior can be investigated by analysis of dynamical parameters for laser diodes and their temperature dependence. This analysis provides some useful information about understanding the limiting factors in laser high frequency operation. This chapter introduces a relatively simple method for estimating VCSEL dynamics and understanding the factors limiting the operating bandwidth of high speed VCSELs. Although different groups have already reported on dynamics of laser diodes [1-4], the work studied here is the first temperature dependence dynamics analysis which has been reported on VCSELs using measurements. Optical mode issues appear in the case of multimode laser operation where the optical power is distributed among all existent modes and reduces the frequency response, which is proportional to square root of optical

power, $P^{1/2}$. In addition to VCSEL dynamics, this chapter reviews the attempts performed in this research towards single mode operation of red and IR VCSELs. Previous reports showed the capability of single mode operation by using a surface relief etch on top of the mesa [5]. The effectiveness of this method is studied in this chapter by fabricating and characterizing red and IR VCSELs with surface relief.

6.2. Temperature dependence of VCSEL dynamics

In this section temperature dependence of a 980 nm vertical cavity surface emitting laser (VCSEL) dynamics is investigated. Resonance frequencies and damping factors of a 7 μm active diameter VCSEL on OB1_7-4_2 chip have been measured at temperatures ranging from 10 °C to 70 °C using noise spectra. The analysis showed that there is no significant change in K-factor as a function of temperature for the laser under study. Measured and calculated values are used to extract photon lifetime, τ_p, and differential gain, $\partial g/\partial n$. relatively constant with temperature with an average value of approximately 12×10^{-16} cm^2.

6.2.1. Experiment

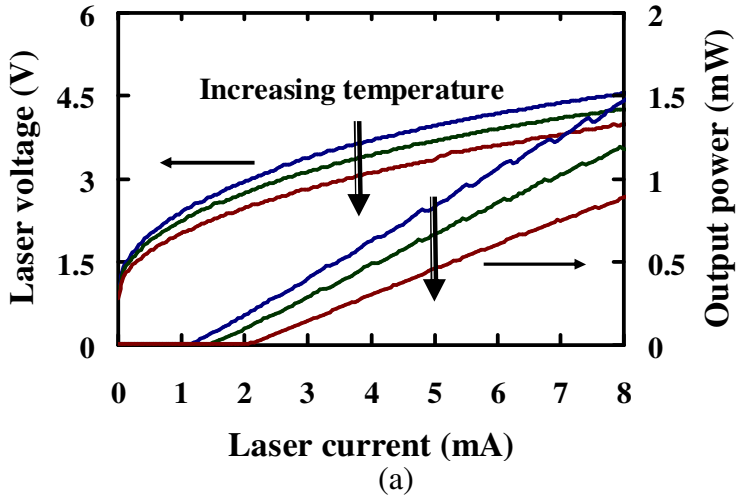
6.2.1.1 VCSEL fabrication

The 980 nm oxide confined VCSELs (OB1_7) were fabricated from molecular beam epitaxy layers grown on an n-type GaAs substrate. The same epitaxial material and processing steps as described in Chapter 4 of this dissertation for VCSEL arrays were used for theses VCSELs. In this section only a summary of design and fabrication will be given.

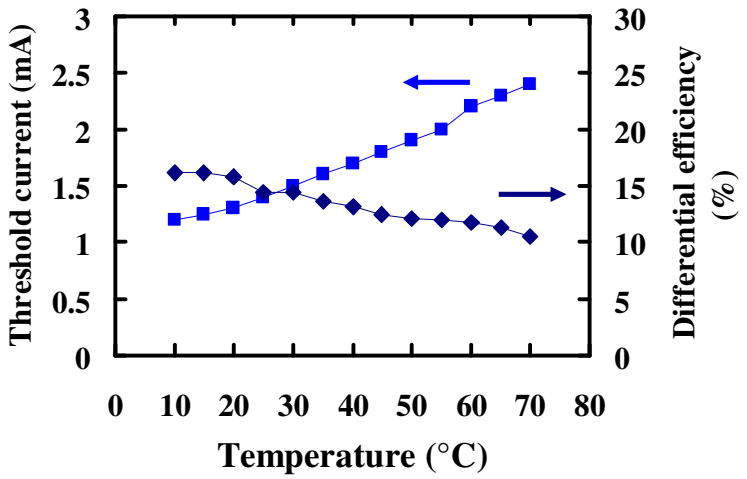
The active region contains three 8-nm $In_{0.18}Ga_{0.82}As$ quantum wells. The n-type lower mirror has been formed with a 23 period Si-doped GaAs-$Al_{0.86}Ga_{0.14}As$ distributed Bragg reflector (DBR) with a calculated reflectivity of 99.59%. The 27 period p-type upper mirror employs a C-doped GaAs-$Al_{0.86}Ga_{0.14}As$ DBR with a calculated reflectivity of 99.67%. The oxide layer is formed by a single low index ~λ/4 layer with 98% Al content adjacent to the cavity. The DBR grading has been described in [6]. The device reported here had a 7 μm diameter oxide aperture in a 10 μm diameter mesa that was coated with silicon nitride and plated over with 2 μm of copper before being flip-chip bonded by indium solder to a copper on GaAs heat spreader. The fabrication flow of bottom-emitting VCSELs is given in Appendix B.

6.2.1.2 VCSEL measurement

The VCSEL LIV curves for temperatures of 15 °C, 35 °C, and 60 °C are plotted in Figure 6.1(a). As depicted in Figure 6.1(b), threshold current, I_{th}, increases and differential efficiency, η_d, decreases with increased temperature from 10 °C to 70 °C.



(a)



(b)

Figure 6.1 (a) LIV of the VCSEL at 15, 35, and 60 °C and (b) threshold current and differential efficiency of the VCSEL at 10 to 70 °C temperature range.

At 25 °C the laser shows a threshold current of 1.3 mA and differential quantum efficiency of 14.5%. The device operated primarily in the fundamental mode but with a limited side-mode suppression ratio of approximately 8 dB at currents up to 4 mA. Biasing the laser at lower currents helps to prevent self-heating effects as well as improve single mode operation which is useful for obtaining well defined resonance frequencies and inhibiting multiple peaks in noise spectra.

The resonance frequencies and damping rates as functions of temperature were obtained from noise spectra under DC bias. The use of noise spectra rather than current modulation response reduces non-linear large signal effects, simplifies electrical probing requirements, and eliminates convolution with electrical effects due to parasitic circuit elements and impedance matching. Figure 6.2 presents the setup used for noise spectra measurements. The HP4145B semiconductor parameter analyzer applies a DC current bias to the laser. The output light of the VCSEL is coupled to a Discovery Semiconductor

DSC30S p-i-n photodiode through a lensed multimode fiber. After boosting the photodiode output signal using a Miteq JSMF4-02K190-35-10P RF amplifier with 35 dB gain, the Agilent 8564EC RF spectrum analyzer detects the noise spectra while an ILX Lightwave temperature controller defines the desired stage temperature using a thermoelectric cooler mounted on a metal chuck.

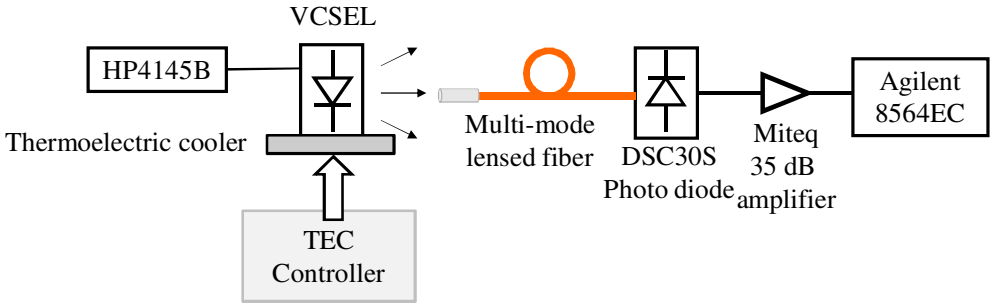


Figure 6.2 Noise spectra measurement setup.

Measured noise spectra at 3mA for 15, 35, and 60 °C are shown in Figure 6.3 along with curve fits described by the magnitude of the conventional damped oscillator response as derived and described in Chapter 2,

$$N(\omega) = \frac{a + b\omega^2}{(\omega^2 - \omega_r^2)^2 + \gamma^2\omega^2}. \tag{6.1}$$

In this equation, a and b are constants, ω is the angular frequency, ω_r is the angular resonance frequency, and γ is the damping factor. Least squares curve fits can be used to extract resonance frequencies and damping factors which are utilized in the next section for VCSEL analysis. There are different tools available for curve fitting purposes such as the "Curve Fitting Tool" in the Matlab toolbox. Another one used here for analyzing the noise spectra was CurveExpert [7]. Both of the tools are capable of fitting a customized model to data points.

6.2.2. Analysis

The resonance angular frequency is given by $\omega_r=[(\partial g/\partial n)s_0 v_g/\tau_{ph}]^{1/2}$, where $\partial g/\partial n$ is the differential gain at threshold, s_0 is the average photon density, v_g is the photon group velocity, and τ_p is the cavity's photon lifetime. The damping factor, which is defined by [8]

$$\gamma = \frac{1}{\tau_n} + \omega_r^2 \tau_p \left[1 + \frac{\varepsilon \Gamma g}{\partial g / \partial n} \right] = \gamma_0 + \mathrm{K} f_r^2 \tag{6.2}$$

represents the rate of energy loss due to the differential carrier lifetime in the absence of stimulated emission, τ_n, as well as optical losses where ε is the gain compression coefficient and Γ is the confinement factor.

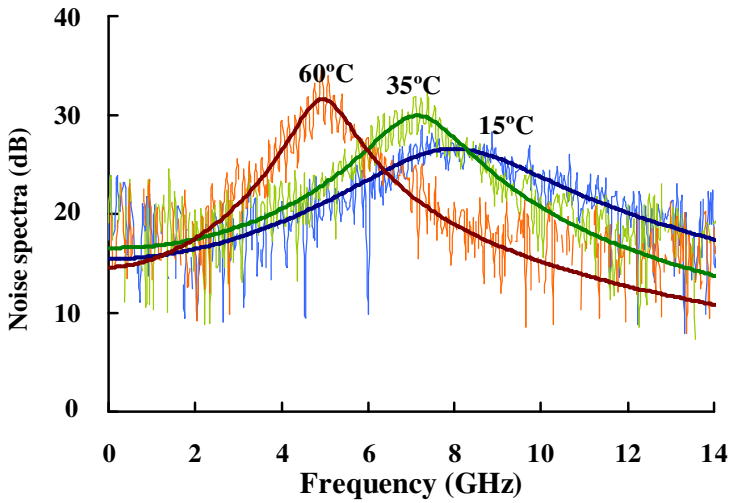
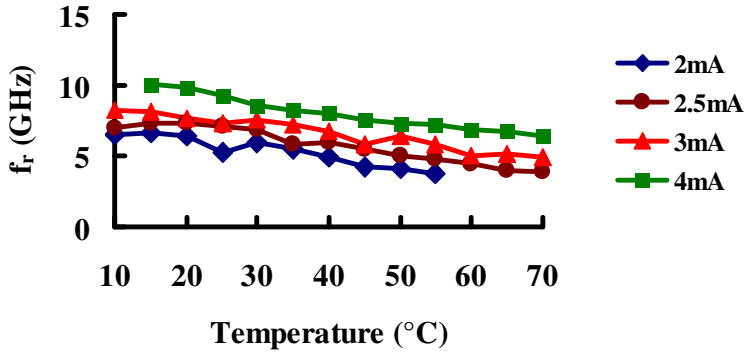


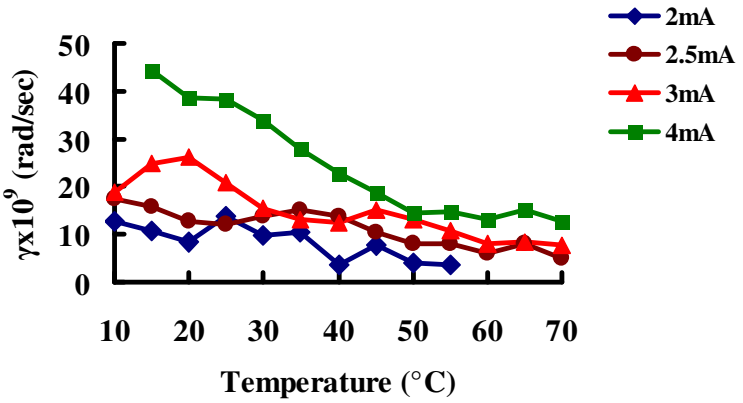
Figure 6.3 Noise spectra along with curve fits at 15 °C, 35 °C, and 60 °C.

The measurement indicates resonance frequency decreases with increasing temperature due to reduced photon density in the gain region. The damping factor also decreases with increasing temperature such that low temperature noise spectra appear

more flattened. Figure 6.4 summarizes the change in resonance frequencies and damping rates with temperature at selected bias currents.



(a)



(b)

Figure 6.4 (a) Resonance frequency and (b) damping of the laser.

Rate equation theory shows resonance frequency is proportional to the square root of optical power [8], $f_r=DP^{1/2}$, where D is a proportionality constant dependent on temperature mainly through the differential gain, $\partial g/\partial n$, and P is the optical output power. D is defined as [9]

$$D = \sqrt{\frac{\partial g}{\partial n}\frac{1}{4\pi^2 V_m \alpha_{T,oc}\tau_{ph}}\frac{\lambda}{hc}} \tag{6.3}$$

where α_{Toc} is output mirror loss including the substrate loss, V_m is the volume of the mode, λ is wavelength, h is Planck's constant, and c is the speed of light. Except $\partial g/\partial n$ all other parameters in (6.3) are expected to be relatively constant with temperature.

Since P decreases with increasing temperature as shown in Figure 6.5 for a range of currents, it is useful to plot the squared resonance frequency normalized by output power, $f_r^2/P=D^2$, in Figure 6.6.

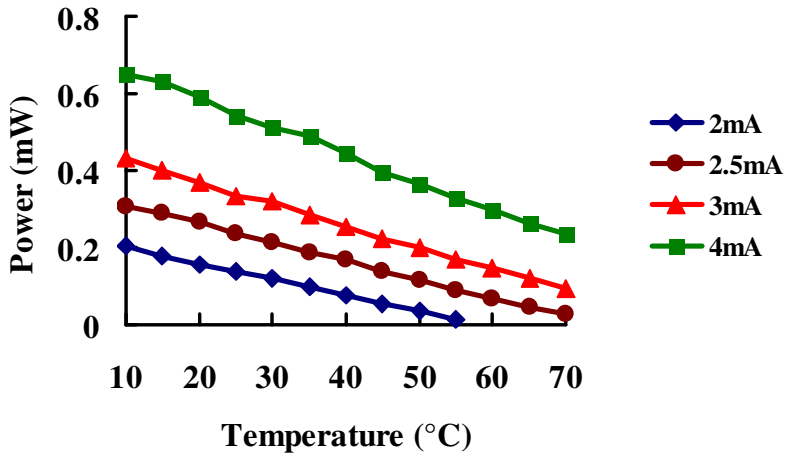


Figure 6.5 Optical power vs. temperature.

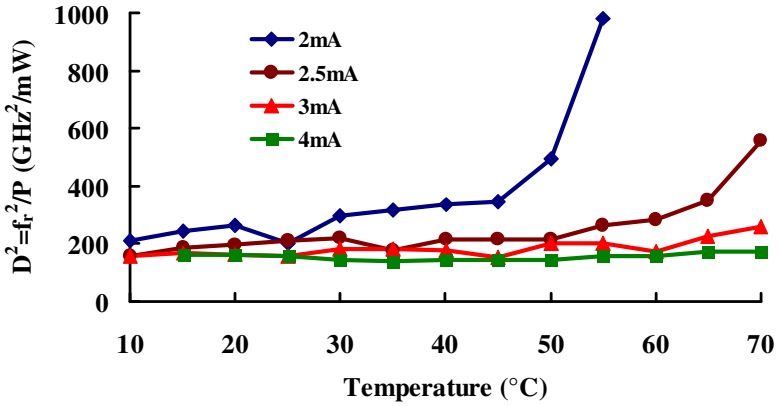


Figure 6.6 Squared resonance frequency normalized by output power for different temperatures.

At higher currents, the plots are flat with temperature indicating that the *D* coefficient and thus differential gain are relatively temperature independent across this range. At lower currents, there is a noticeable increase in *D* at the highest temperatures that may be related to approaching threshold under these conditions. The appearance of constant *D* factor vs. temperature may be due to increasing gain offset balancing decreasing peak $\partial g/\partial n$. As expressed in Equation 6.2, damping factor vs. the resonance frequency squared is a line with the slope of *K*. The γ vs. f_r^2 data plotted in Figure 6.7 can be fit to extract *K*-factors used to estimate maximum intrinsic 3dB frequency. While the data in Figure 6.7 contains some scatter, fits indicate that the *K*-factor for this device is relatively temperature independent. *K*-factors are plotted in Figure 6.8 for temperatures from 10 °C to 70 °C. Neglecting the γ_0 term, the maximum intrinsic 3dB frequency of this device, given by $f_{3dB,max}=2\pi\sqrt{2}/K$, ranges from 22.8 GHz to 37.6 GHz but without a clear trend from 10 °C to 70 °C.

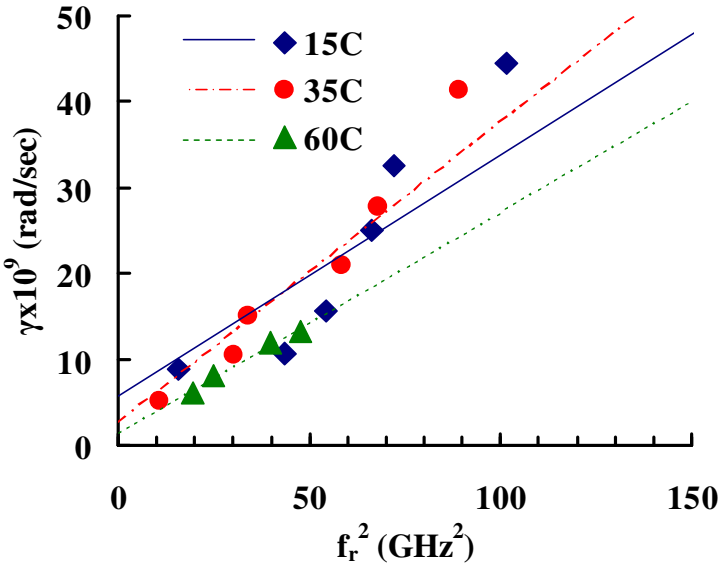


Figure 6.7 Damping versus squared resonance frequency along with linear fits.

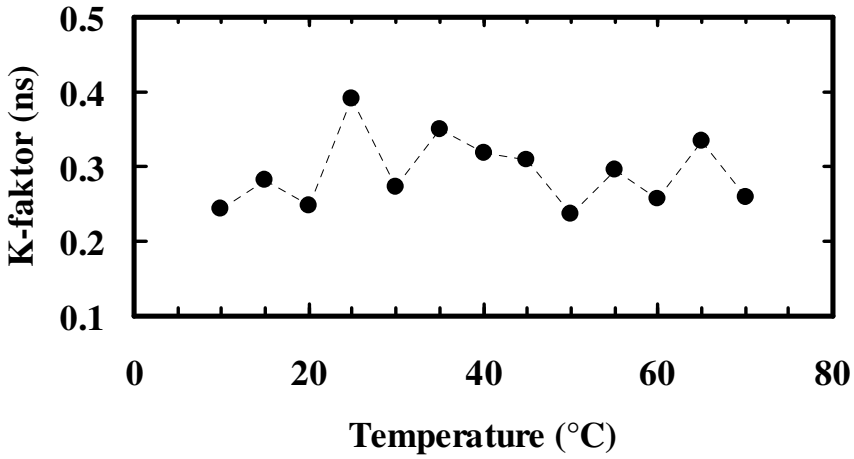


Figure 6.8 *K*-factor extracted from measurement versus temperature.

It might be more useful to write Equation 6.3 as a function of η_i/η_d and substitute $\alpha_{Toc}\tau_p=\eta_d/(\eta_i v_g)$ in Equation 6.3 to give

$$D = \frac{1}{2\pi}\sqrt{\frac{\partial g}{\partial n}\frac{\eta_i}{\eta_d}\frac{v_g}{V_m}\frac{\lambda}{hc}} \tag{6.4}$$

The measured $D(T)$ in conjunction with slope efficiency can quantify the temperature dependent differential gain using Equation 6.4. An effective cavity length of L_{eff}=1.3 μm defined as the length of the cavity plus the penetration depths into the DBRs, gives a mode volume of V_m=50 μm^3. Penetration depth, L_p is defined as $L_p=tanh(\kappa l)/2\kappa$ where l is the thickness of the mirror and κ is the coupling coefficient which, for a stack of mirror layers with high and low refractive index difference Δn, is given by $\kappa=2\Delta n/\lambda_0$ [10]. The calculated group velocity is $v_g=c/N=1.05\times10^{10}$ cm/s where N is the group refractive index of the laser and is given by $N=n-\lambda(dn/d\lambda)$ where n is the effective refractive index of the cavity. The temperature dependence of $\eta_d(T)$ is assumed to be due

entirely to η_i which is taken as unity at the lowest temperature, i.e. 10 °C so that η_d/η_i=0.16 at all temperatures. Note that the constancy of this ratio is consistent with the expectation of a temperature independent cavity lifetime, $\tau_p=\eta_d /(\eta_i \alpha_{Toc} v_g)$, which is 1.13 ps using a calculated value of collected output coupling loss of α_{Toc}=10.6 cm^{-1}. *D(T)* is obtained from a least squares, zero intercept linear fit of f_r vs. $\sqrt{P}$ for varying current biases, and used to determine $\partial g/\partial n$ as shown in Figure 6.9. Differential gain decreases slightly over the working temperature range with an average value of 11.6×10^{-16} cm^2 which agrees well with a theoretical value reported in [11].

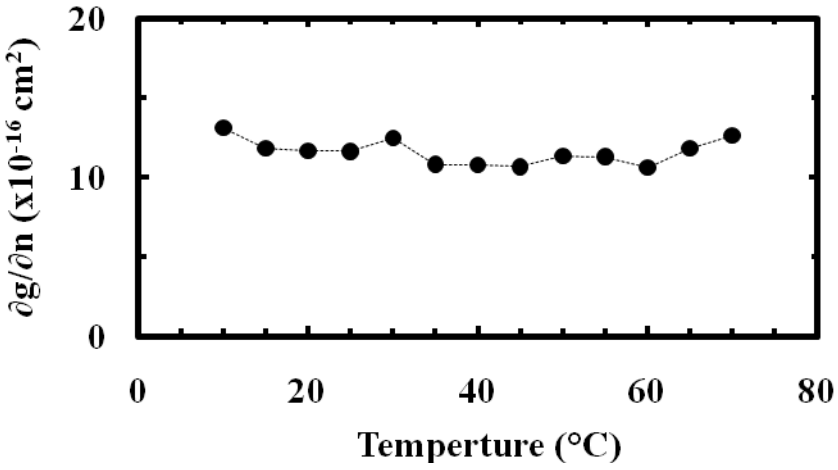


Figure 6.9 Estimated differential gain versus temperature.

6.3. Single mode operation of VCSELs

This section reviews the experimental attempts at surface relief etch on top of red and IR VCSEL mesas to achieve single mode operation. Red VCSELs studied here are fabricated from sample 6538C which was discussed in Chapter 5. IR VCSELs were fabricated from our newest bottom-emitting VCSEL design grown by Opticomp

Corporation. There are two wafers grown by Opticomp: the first one follows our design which is detailed in Appendix A (OB21), and the second one has a few mirror pairs less than the original design for higher power operation (OB22). Fabrication steps follow the bottom-emitting process flow given in Appendix B, except adding a step for single mode surface relief.

6.3.1. Surface relief principles

One of the many approaches for attaining single mode operation in VCSELs is surface relief etch that was shown to be very effective for VCSELs [5], [12-14]. This method is based on removing a certain thickness of top DBR mirror resulting in lower mirror reflectivity and thus higher mirror loss and threshold gain. This concept is simulated by using the transfer matrix method introduced in Chapter 2 for reflectivity of multilayer films and plotting the mirror reflectivity and loss for a typical red VCSEL top DBR mirror as a function of etch depth through the mesa, as shown in Figure 6.10. The top-emitting structure is made up of 32 pairs of alternating layers of quarter wave thick (λ=670 nm) $Al_{0.5}Ga_{0.5}As/Al_{0.92}Ga_{0.08}As$ films. The cavity length in this simulation is assumed to be approximately 191 nm (1-λ). This plot implies that removing a thickness of half-wavelength causes a local minimum in the mirror loss, while taking a quarter-wavelength thick layer off the top mirror results in a maximum mirror loss.

This concept can be used to suppress higher order transfer modes in a VCSEL while the center of mesa that guides the fundamental mode is kept unchanged. Increasing the mirror loss for high order modes can be performed by etching a quarter-wavelength deep donut-happed pattern on top of the VCSEL mesa. This structure is shown in Figure 6.11

and has been already reported in literature [12].

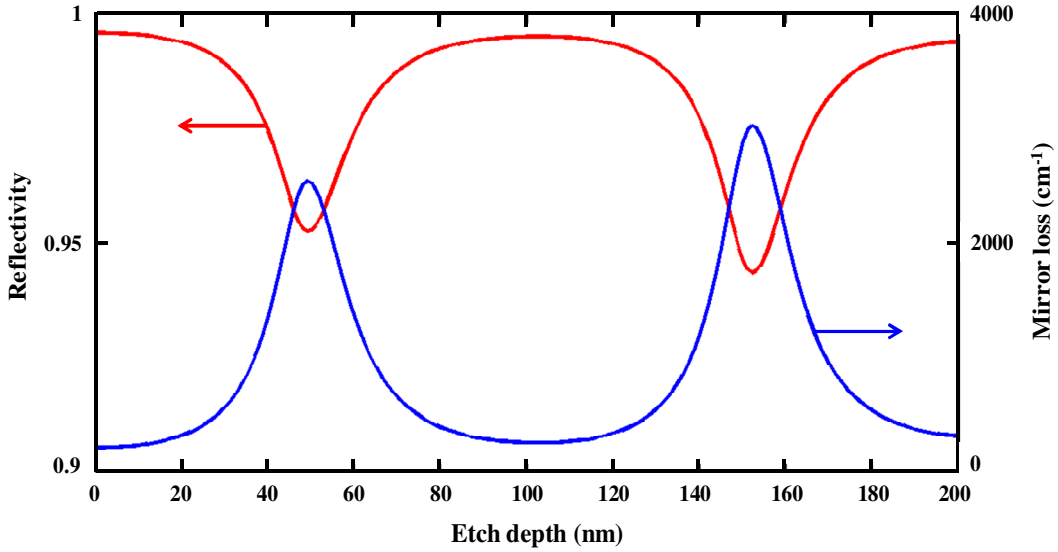


Figure 6.10 Simulated R and α_m as functions of etch depth for a typical top DBR in a top-emitting red VCSEL.

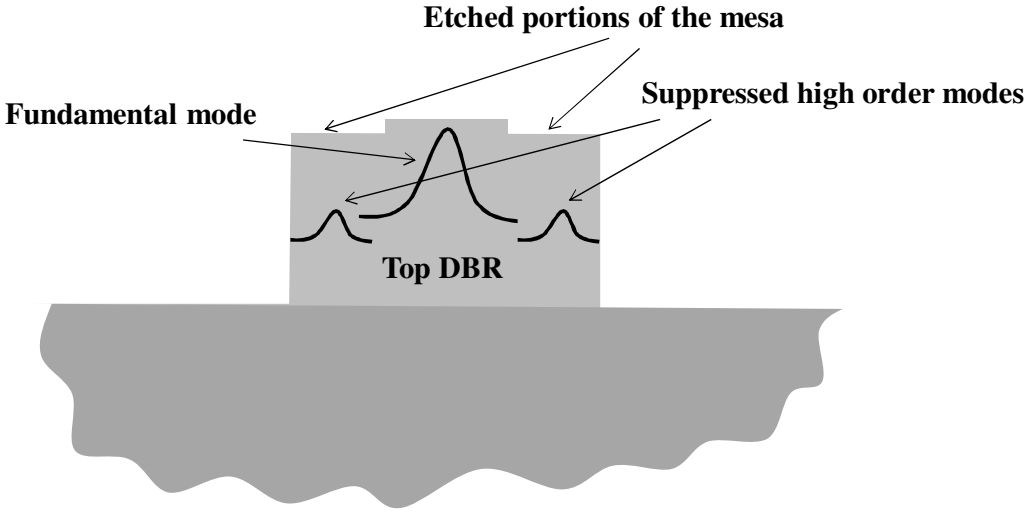


Figure 6.11 Higher order mode suppression by using the surface relief etch.

Another method that was shown to be successful in achieving single mode VCSELs is inverted surface relief that follows the same principle as the ordinary surface relief [5]. An inverted surface relief utilizes a λ/4 thick layer such as GaAs with higher refractive index than the underlying layer. This helps to create reflections from the underlying-topmost layer and topmost-air interfaces that are out of phase with the reflections further down to the mirror stack. Now, to decrease the mirror loss for the fundamental mode, a circular shape pattern is removed from the center of the VCSEL. This approach facilitates the use of precise epitaxial growth to reach the narrow local maxima in the mirror loss curve. This will eliminate the precise etching required in the ordinary surface relief method; because, now there is a wider etching window due to the broader mirror loss spectrum in the local minima as shown in Figure 6.10 [5].

6.3.2. Experiment

Effects of surface relief on single mode operation of 670 nm and 980 nm VCSELs are studied in this section. After introducing the mask set used for each 670 nm and 980 nm VCSELs the results and conclusions of this experiment will be presented.

6.3.2.1. 670 nm VCSELs

Before fabricating the single mode VCSELs, a simulation is performed to understand the options we have for applying surface relief to top-emitting red VCSELs. As mentioned in Chapter 5, a layer of SiN_x film is deposited on the entire red VCSEL sample before starting fabrication to protect VCSEL facets from damage. This layer can be chosen in a way that behaves as an antiphase layer to suppress higher order modes.

Figure 6.12 presents the simulation result of reflectivity of the arbitrary mirror structure as functions of SiN_x and highly doped GaAs cap layer thicknesses, d_{SiN} and d_{cap} respectively. This simulation result proposes that in addition to removing a λ/4 thick layer from the mirror, certain thicknesses of SiN_x and GaAs cap layer can be removed or added to the mirror structure to maximize the reflectivity. Nonetheless, there are difficulties in altering cap layer thickness. Since we were working with red VCSEL epitaxial wafers that were provided to us, we could not add any epitaxial GaAs on the surface. Moreover, it was hard to control the epitaxial material etch depth with our system that can only monitor etch depths of relatively big spots (~1 mm to 2 mm) by measuring the surface reflectivity.

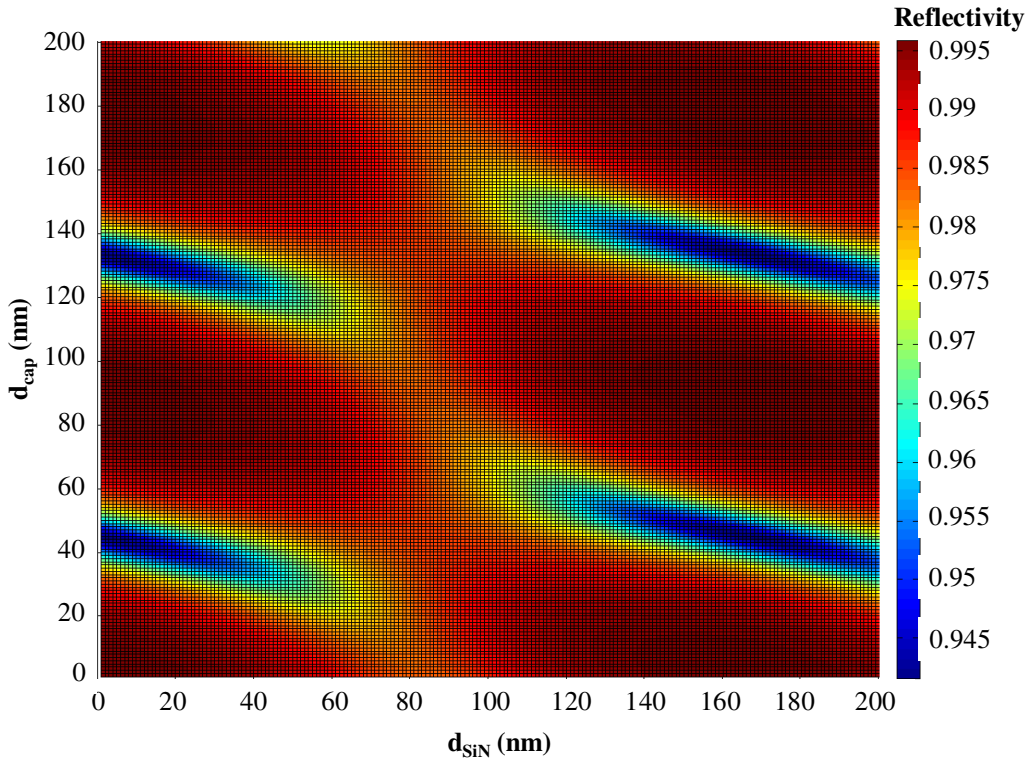


Figure 6.12 Simulated reflectivity as functions of cap layer and SiN_x thicknesses.

However monitoring the etch depth of a calibration piece, while simultaneously etching the main sample, might solve this problem; this method could not be tested due to time constraints of this dissertation. However, there may be some nonuniformities in the etch rate of different pieces with different sizes in our dry etch Trion system that weaken the effectiveness of this method. As mentioned in Section 6.3.1 this is critical to etch down to a very accurate thickness that gives the minimum local reflectivity at a narrow portion of the reflectivity curve. SiN_x can be easily deposited in our cleanroom and etched down to a relatively precise thickness.

One quick conclusion of the simulation result from Figure 6.12 is the strong dependency of the cap layer thickness on the mirror reflectivity altered by SiN_x thickness. The wafers grown by Vixar employ a thin (<20 nm) highly doped cap layer to decrease absorption. This means that the highest reflectivity occurs at 0 and ~$\lambda/2$ thick SiN_x films (see Figure 6.12). However, the mirror loss show less than 80% change at this range of cap layer thickness, while it can approach 90% with other cap layer thicknesses.

Experimentally, we have seen a significant increase in output power when there is no SiN_x on the VCSEL facet. This observation is used for single mode operation of the red VCSELs. Donut shape single mode features were designed for VCSELs with mesa diameters of 18, 20, 22, 27, and 32 µm with corresponding inner and outer diameters of 2, 3, 3.5, 4, and 5 µm and 6, 8, 10, 15, and 20 µm, respectively. Since the sample (6538C_3) had already ~170 nm ($\lambda/2$) of SiN_x before starting the fabrication, a 11 nm thick layer is added on top of the sample to alter the phase matching condition. The SiN_x on center of the pattern was then completely etched away using dry etching in the µ-RIE system with a gas mixture of CF4+8% O2, while the other portions of the mesa were kept

unetched. The LIV measurement of these VCSELs shows that they could not reach threshold and thus there was no laser operation.

Next attempt to achieve single mode operation in the red VCSELs is using the conventional surface relief etch. The whole SiN_x is removed from the mesas and then the single mode mask is used to pattern the features on the sample. This step needs a positive tone photoresist to protect the centers and open up everywhere else on the VCSEL mesas. This step is followed by dry etching the mesas in the Trion system with Cl_2+BCl_3 (1:3) gas mixture. The sample was etched for approximately 10 s to remove the first λ/4 thick layer from the top DBR mirror as shown by the etch trace of a typical 6538C sample and presented in Figure 6.13. Again, it is worthwhile to mention that the etch rate can vary from sample to sample.

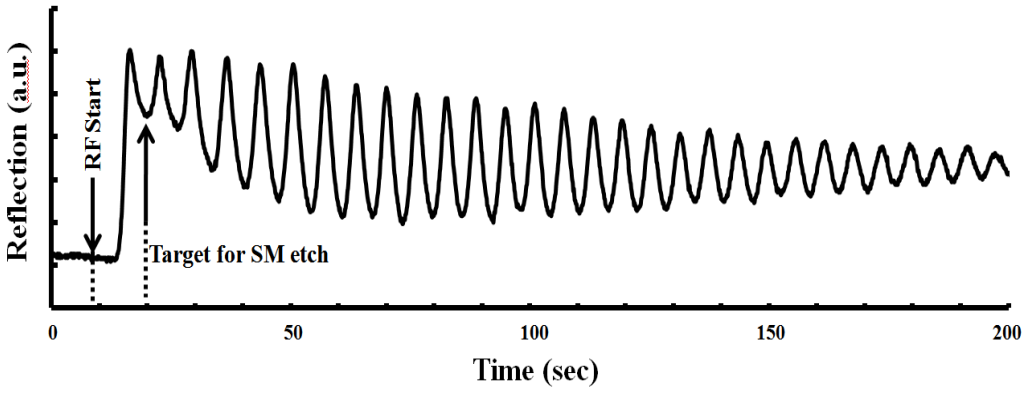


Figure 6.13 Etch trace of a typical sample from wafer 6538C.

After etching and testing the sample none of the measured VCSELs could reach to threshold and thus again there was no laser.

Due to the time limitations for this dissertation this part was not repeated with other epitaxial material and modified fabrication steps. The next section presents the attempts for achieving single mode operation for bottom emitting VCSELs.

6.3.2.2. 980 nm VCSELs

The surface relief method used for top-emitting VCSELs is also applied to bottom-emitting lasers. VCSELs are fabricated from wafer OB21 and mask set "VCSEL_BE_JJ2" with the processing steps that follow the bottom-emitting process flow in Appendix B and include mesa etch, single mode etch, oxidation, and n- and p-metal deposition.

The reflectivity and mirror loss of a typical top DBR with 26 pairs of quarter wave thick layers of GaAs/$Al_{0.86}Ga_{0.14}As$ for a bottom-emitting IR (980 nm) VCSEL is simulated and plotted in Figure 6.14 as functions of etch depth. Higher minimum reflectivity in the case of IR than red VCSELs predicts that surface relief etch for a bottom-emitting IR VCSEL should not be as effective as the one for a top-emitting red VCSEL (compare with Figure 6.10). This difference may arise from the fact that there is a metal contact on top of the mesa in the case of bottom-emitting VCSELs and also differences in the IR and red structures such as mirror compositions.

Due to some design mistakes, there is no donut shape feature on the photo mask for bottom-emitting VCSELs. Single mode pattern in this bright field mask is only a dark circle at the center of VCSELs. There were 2 possible cases by using positive or negative photoresist. Use of positive photoresist can result in the desired mode control etch, but it also etches the mesas without single mode control since there is no pattern on the VCSELs to cover them. This means that there is not a way to compare the results of single mode etch with a VCSEL without surface relief.

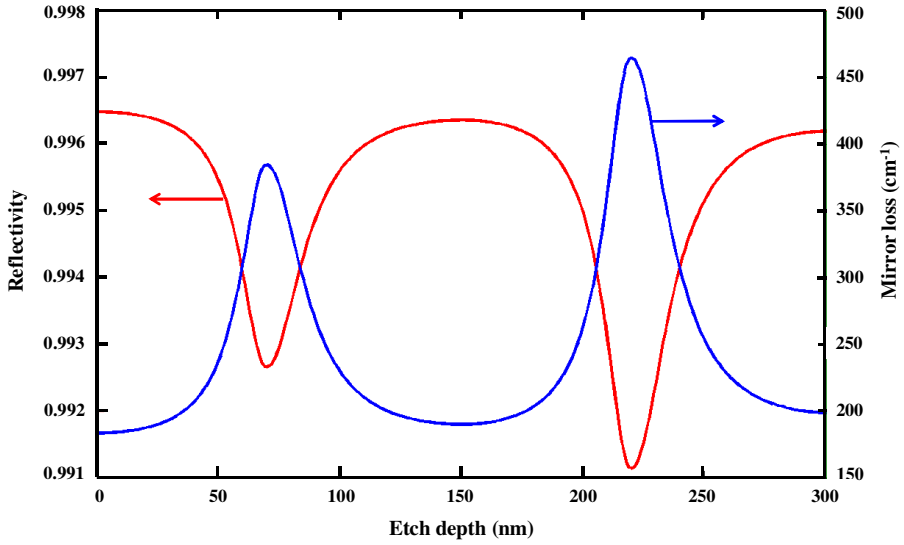


Figure 6.14 Simulated R and α_m as functions of etch depth for a typical top DBR in a bottom-emitting IR VCSEL.

Using a negative photoresist facilitates having unetched VCSELs for comparison purposes but with the cost of etching the center of a VCSEL mesa instead of other portions of it. Since it is really important to compare the results of surface relief with the VCSELs without single mode features, negative photoresist was used to test single mode operation of the bottom-emitting VCSELs. However, the single mode feature becomes inverted with respect to the conventional surface relief. Using this type of surface relief for suppressing lower order modes has already been reported for controlling the spectral width in VCSELs [15]. After patterning the single mode feature, a portion of GaAs cap layer is removed in the Trion system by etching for approximately 8 s.

Typical LIV characteristics of the fabricated VCSELs are presented in Figure 6.15 for a 10 µm and 18 µm diameter apertures in corresponding 16 µm and 24 µm diameter mesas. After performing the LIV measurement, the optical spectra measurement was

carried out for the devices with and without single mode etches.

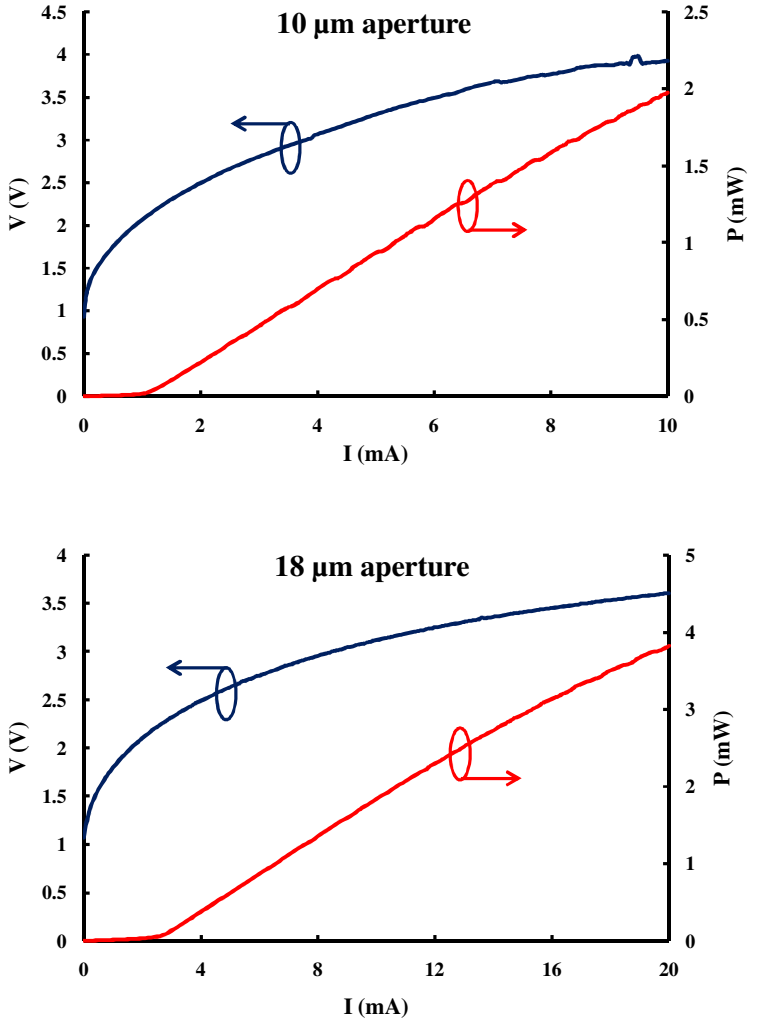


Figure 6.15 LIV measurements for typical VCSELs from sample OB21_4 without mode control feature.

Optical spectra for a 10 µm and 18 µm diameter aperture VCSEL at corresponding bias currents of 3 mA and 4 mA are shown respectively in Figures 6.16 and 6.17 with and without single mode etch. As can be seen from the graphs, single mode etch does not show any significant effect on altering the modal behavior and L-I-V characteristics of

the VCSELs under test. This may be attributed to insufficient etch depth of surface relief on the mesa. Performing a deeper etch required starting a fabrication run from beginning with a new sample. Due to time limitations of this project, this part is left as the future work.

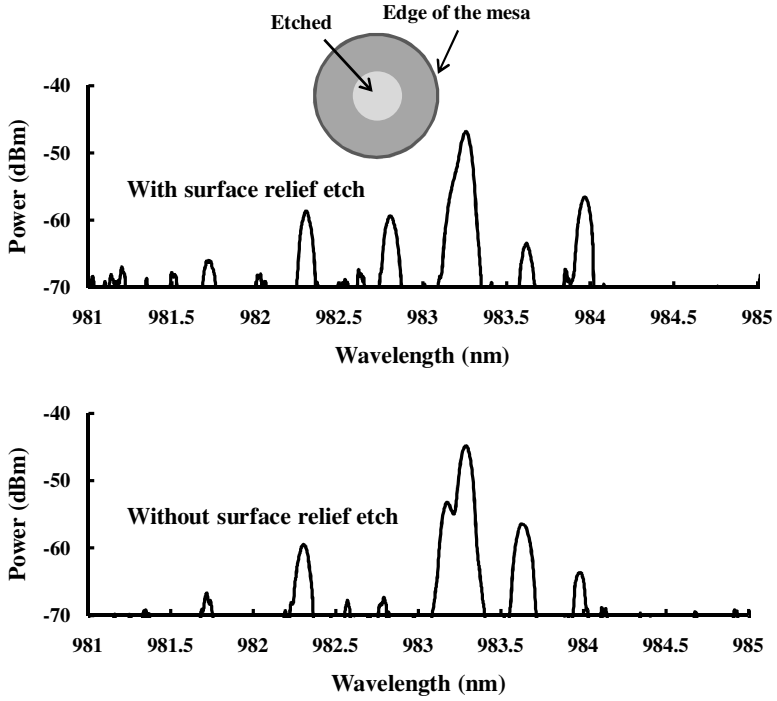


Figure 6.16 Optical spectra for typical 10 μm aperture VCSELs with and without surface relief at 3 mA bias current.

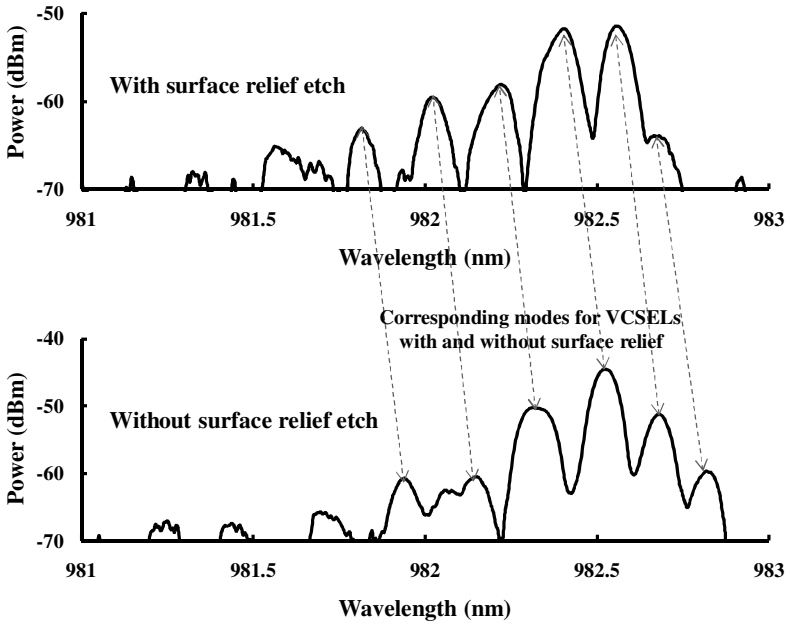


Figure 6.17 Optical spectra for typical 18 μm aperture VCSELs with and without surface relief at 4 mA bias current.

6.4. Conclusions

In the first part of this chapter, temperature dependent dynamics were extracted from the resonance frequency and damping factor by noise measurements for a 7 μm active diameter VCSEL up to $3I_{th}$. This measurement indicates that the temperature dependence of VCSEL dynamics for the device under test is mainly related to the output power although other effects may occur at higher currents. Modifying the power response of the laser to be more constant with temperature should yield better frequency response. For example, the use of higher bandgap energy confinement layers and larger gain offset should yield better high temperature operation and increased bandwidth. However, using larger gain offsets will decrease differential gain. The relatively constant differential gain with temperature indicates a small amount of gain-mode offset at low temperatures for

the laser considered here.

The Second part of this chapter reviewed the attempts of achieving single mode operation in the top-emitting red and bottom-emitting IR VCSELs. The experimental results showed that red devices with surface-relief etches could not reach threshold and single mode etch had no significant effect on the modal behavior of IR VCSELs. Due to time constraints of this dissertation, the experiment was ended and the rest of this work was left as a future work discussed in the next chapter.

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Chapter 7

CONCLUSIONS AND FUTURE WORK

This chapter concludes the research discussed in this dissertation. It also proposes future work based on the research milestones and achievements.

Section 7.1 summarizes the work done on fabrication and characterization of 980 nm bottom-emitting and 670 nm top-emitting oxide-confined vertical-cavity surface-emitting lasers (VCSELs). The future work based on the research goals will be given in Section 7.2.

7.1. Summary of achievements

The main objective of this research is to reduce the effects of the main factors which reduce the modulation speed of VCSELs as mentioned in Chapter 3. Laser intrinsic bandwidth, external parasitic circuit elements, thermal issues, and optical issues are the main limiting factors on VCSEL modulation frequency. The project goals were mainly focused on thermal management techniques which reduce the junction temperature and improve laser DC and AC behavior such as copper electroplating and flip-chip bonding. Analysis was also performed to extract different VCSEL parameters and dynamics at different temperatures to understand the intrinsic limitations on laser

frequency response. Since addressing optical issues was expected to allow higher frequency response, single mode operation of VCSELs was also investigated.

In this section I will summarize all accomplishments of the research on 980 nm bottom-emitting and 670 nm top-emitting VCSELs as well as VCSEL modeling and simulation.

7.1.1. 980 nm oxide-confined bottom-emitting VCSELs

a. Design

A new VCSEL structure has been designed to improve the laser performance and frequency response. Modifications to the previous design include mirror grading, oxide layer tapering as well as placing a high doping thick GaAs layer as an n-contact layer in the bottom n-DBR to lower the contact resistivity. Opticomp Corporation has grown this design for us.

A new mask set was designed by John Joseph with a variety of parameters such as VCSEL mesa diameters, mesa plating overlap sizes (inner and outer diameter), and single mode etch for individual VCSELs. In order to have as many possible variations in the above mentioned parameters, four types of VCSEL chip have been laid out on the mask. Different types of VCSEL arrays with different configurations, number of elements, and element mesa diameter have also been included on the mask for high speed and high power operation. The heatsink was also designed to have impedance matched co-planar waveguides for high speed operation.

b. Fabrication

High speed individual VCSELs with a variety of mesa sizes and several types of high speed, high power VCSEL arrays were simultaneously fabricated with similar processing steps. Two circularly shaped VCSEL arrays, one with 24 μm and the other one with 12 μm mesa diameter single elements were formed. Both arrays contain 28 individual lasers with 70 μm device pitch. Current VCSEL process flow was modified and a new process flow was designed and evaluated to better fit our cleanroom equipment for the best result. Cu electroplating and flip-chip bonding were also performed on both individual and VCSEL arrays.

c. Measurement

DC characterization including LIV measurement, optical spectra and thermal resistance analysis were carried out for 980 nm VCSELs. Some of the data showed improved laser output power and thermal resistance with more efficient thermal management. Measured arrays with small and large single element mesas exhibit over 90 mW and 200 mW CW output powers, respectively. Cu plating and flip-chip bonding were capable of reducing the thermal resistance. As an example, R_{th}=0.23 ˚C/mW and 0.93 ˚C/mW are achieved for 21 μm and 7 μm aperture VCSELs, respectively after better heat management.

Noise measurement and analysis was another type of characterization performed on high speed 980 nm VCSELs. A VCSEL with 7 μm active diameter in a 10 μm diameter mesa was biased at different DC currents and the noise spectra of the device were measured using a spectrum analyzer at various temperatures. Then, the resultant spectra were analyzed and resonance frequencies and damping factors at each current and

temperature were extracted. The temperature dependence of laser dynamics performed on this device indicated that the primary cause of reduced bandwidth is reduced photon density at elevated temperatures.

AC measurement of fabricated 980 nm VCSELs from previous step using a vector network analyzer (VNA) showed a 14 GHz 3dB modulation frequency for a 7 μm aperture VCSEL and 8 GHz 3dB bandwidth for VCSEL arrays. The array frequency bandwidths are capable of approaching 10 GHz at high output powers. AC and DC measurement and uniformity analysis showed that the arrays are uniform in bandwidth and wavelength and are potentially scalable to higher powers with larger number of constituent single VCSELs.

A pulsed measurement was performed on arrays in order to evaluate their ability in generating short pulses which is very important in applications such as LADAR systems. Gain-switched short pulses with smaller than 60 ps FWHM were generated by applying 100 ps FWHM electrical drive pulses to the arrays.

The last part of the work on 980 nm VCSELs studied the effects of surface relief on obtaining VCSELs with single mode operation that can improve their frequency response. However, we were not able to reproduce published results on single mode control using surface relief. This may be due to insufficient etching depth for the surface relief. To do a deeper etch, single mode features need to be precisely aligned with the first etch. This implies that starting a new fabrication run is a better idea than trying to pattern another single mode feature on top of the first one.

d. Publications

Following journal and conference papers related to Section 7.1.1 have been published.

1) R. Safaisini et al., *IEEE J. Quantum Electron.*, **46**, 1590 (2010).
2) R. Safaisini et al., *Electron. Lett.* **45**, 414 (2009).
3) R. Safaisini et al., *IEEE Photon Technol. Lett.* **20**, 1273 (2008).
4) J.R. Joseph et al., *Photonics West (SPIE),* paper 7615-20, (2010).
5) R. Safaisini et al., *CLEO/QELS,* paper CMSS4, (2009).
6) R. Safaisini et al., *LEOS Annual Meeting,* paper 10.1109, (2007).
7) R. Safaisini et al., *APS March Meeting,* paper X39.00011, (2007).

There are also some other publications related to the work I did to support other research in our group.

7.1.2. 670 nm oxide-confined top-emitting VCSELs

a. Design

VCSEL structures for this activity were designed by Vixar, Inc.

I designed a new mask set with a variety of parameters such as VCSEL mesa diameters, mesa plating overlap sizes (inner and outer diameter), and single mode etch for individual VCSELs. This design is compatible with Vixar's requirements for automated measurement and characterization. The mask set was designed to decrease the processing steps and also to be robust in reducing the possible errors in different processing steps with defining a required margin for possible processing tolerances.

b. Fabrication

670 nm red VCSEL fabrication has been developed and single mode and high power VCSELs with mesa diameters varying from 14 μm to 32 μm diameter were fabricated. In order to investigate the effect of Cu heatsinking on laser DC parameters

such as output power, threshold current, and thermal resistance, Cu was electroplated on mesas with a variety of inner and outer diameters.

c. Measurement

LIV measurements, optical spectra and thermal resistance analysis on red VCSELs were carried out before and after Cu plating. Before plating, a maximum power of 2.6 mW was observed for a 27 μm mesa diameter (~15 μm aperture) VCSEL. Thermal resistances of 0.4 ˚C/mW to 2.1 ˚C/mW were also measured for VCSELs with 27 μm to 14 μm mesa diameters, respectively. Although the results showed that thermal resistance decreases with increasing plating size, an increase in the threshold current and decrease in the output power in some of the VCSELs were observed. This unexpected result was attributed to the stress applied to VCSEL mesas by plated Cu. The stress on the mesa shifts the gain peak wavelength and alters the gain-mode offset in the VCSELs.

Effect of the surface relief etch on the single mode operation of red VCSELs were also investigated. There was no laser among the devices I measured and therefore I could not take any optical spectra.

d. VCSEL modeling

Temperature profile and Cu induced stress on the mesa in top-emitting red VCSELs were simulated using Comsol Multiphysics package. The simulated thermal resistance for VCSELs with different plating sizes implied that thermal resistance reduces with increasing Cu size and more importantly this reduction follows the trend of measured thermal resistance reduction with plating size. This indicates the measured thermal

resistance is only affected by thermal properties of Cu on the mesa and not by its stress effects. The stress modeling of the VCSELs showed that Cu puts the mesa under compressive stress and larger the Cu size is more the mesa deforms.

Another modeling part of this dissertation focused on DBR modeling and simulating the effects of different types of surface relief on the VCSELs. The effects of SiN_x and cap layer thicknesses and etch depth of the DBR on the mirror loss was presented. This result was used to study the possible options for surface relief in top-emitting red VCSELs.

e. Publications

Following conference papers related to Section 7.1.2 have been published.

1) R. Safaisini et al., *IEEE Photonics Society*, paper TuQ5,(2010).
2) R. Safaisini et al., *Photonics West (SPIE),* paper 7615-10, (2010).

7.2. Future work

Future work of this dissertation is based on the main goals and achievements of this project. This section summarizes the possible improvements that can be made to better address the issues I encountered during this research.

7.2.1. Reducing the Cu stress on the mesa for better device performance

Although Cu plating of VCSEL mesas resulted in an approximately 30% thermal resistance reduction in red VCSELs, plated Cu caused unexpected results in DC

characteristics of VCSELs due to applying stress to the mesas. This stress is highly related to the plating conditions such as bath temperature and plating current. Cu can be electroplated with different conditions to find the parameters with the minimal stress. The effect of compressive stress of Cu on the VCSEL mesa might also be compensated by covering the mesas with another layer with tensile stress such as SiN_x before copper plating.

7.2.2. Effect of single mode operation on VCSELs frequency response and dynamics

As discussed in Chapter 6, surface relief etch is an effective method for attaining single mode operation in VCSELs. Following steps can solve the issues I encountered with surface relief etch for both IR and red VCSELs:

1) Start over the fabrication with a symmetric red sample. Symmetric samples facilitate spinning on photoresist evenly on the sample which results in improved fabrication yield and thus more working devices.
2) It is really critical for surface relief feature to be etched down to a certain layer to guarantee the increased mirror loss for higher order modes. Use of a monitoring piece or designing a large open area for etch monitor on the mask solves the problem of inaccurate etching.
3) Similar to red VCSELs, precise etching for bottom-emitting IR VCSELs are of great importance. A new mask set with a large open area for etch monitor can also be designed for the IR VCSELs.

4) As mentioned in Chapter 6, the single mode features on our current mask set has been designed in a wrong way. A new mask set should be designed to address this issue.

5) After successful surface relief for single mode operation, frequency response or resonance frequency of IR VCSELs and resonance frequency of red VCSELs can be measured.

7.2.3. VCSEL simulation

I translated a Mathcad code originally written by Prof. Kevin Lear in Matlab form and started to modify and test it. This code can optically simulate circularly symmetric VCSELs by calculating electric field reflections and transmissions from mirrors and active region. This model is based on solving an eigenvalue/eigenvector problem for sets of Bessel type solutions for electric field in the cylindrical VCSEL structure. The DBR part of this code was used in simulating mirror reflectivity for single mode operation.

Appendix A

EPITAXIAL DESIGN FOR 980-NM BOTTOM-EMITTING VCSELS

Appendix B

PROCESS FLOW FOR BOTTOM- AND TOP-EMITTING VCSELS

a) Bottom-emitting VCSEL process flow

1. Mesa Etch
   a. Mesa photolithography
      i. Acetone/methanol/ DI rinse / N_2 dry.
      ii. Bake on hotplate at 120 °C for 1 min.
      iii. Spin on AZ4400 at 2000 rpm for 30 sec.
      iv. Bake at 110 °C for 2 min.
      v. Edge bead removal.
      vi. Use BF mesa mask, expose for 42 sec at 10 mW/cm^2.
      vii. Develop in AZ400K (1:4) for ~1.5 min (5 sec after clearing).
      viii. DI rinse / N2 dry.
      ix. Resist bake at 120 °C for 1 min.
      x. O_2 descum 40 sccm, 40 W, 1 min.
   b. Dry Etch Mesa
      i. Mount sample on quartz wafer with fomblin oil and load the wafer.
      ii. Turn on gas, wait 10 sec, turn on RF.
      iii. Watch hi-low signal until reach the desired layer.
      iv. Stop etching by turning off RF.
      v. Acetone soak for 15 min.
      vi. Acetone/methanol/ DI rinse / N2 dry.

vii. Spray with acetone if necessary.

viii. O2 descum 40 sccm, 50 W, 1 min.

2. Single Mode Etch

a. Single Mode Photolithography

i. Acetone/methanol/ DI rinse / N_2 dry.

ii. Bake at 120 °C for 1 min.

iii. Spin on AZ4400 at 4000 rpm for 30 sec.

iv. Bake at 110 °C for 2 min.

v. Edge bead removal.

vi. Use BF SM Mask, expose for 25 sec at 10 mW/cm^2.

vii. Develop in AZ400K (1:4) for ~40 sec (5 sec after clearing).

viii. DI rinse / N_2 dry.

ix. Resist bake at 125 °C for 1 min.

b. Dry Etch Single Mode

i. Mount sample on quartz wafer with fomblin oil and load the wafer.

ii. Turn on gas, wait 10 sec, turn on RF.

iii. Watch hi-low signal until reach the desired layer.

iv. Stop etching by turning off RF.

v. Acetone soak for 15 min.

vi. Acetone/methanol/ DI rinse / N_2 dry.

vii. Spray with acetone if necessary.

viii. O_2 descum 40 sccm, 50 W, 1 min.

3. N-Metal Deposition

a. Photolithography for n-metal

i. Acetone/methanol/ DI rinse / N_2 dry.

ii. Bake at 120 °C 1 min.

iii. Spin on AZ2070 4000 rpm, 30 sec.

iv. Bake at 110 °C for 30 sec.

x. Edge bead removal.

v. Use n-metal BF mask, expose for 48 sec at 10 mW/cm^2.

vi. Postbake at at 110 °C for 75 sec.

vii. Develop in AZ300MIF for ~1 min (5 sec after clearing).

viii. DI rinse / N_2 dry.

ix. O_2 descum 40 sccm, 40 W, 1 min.

b. Metal Deposition

i. HCl:H_2O (1:1) dip 30 sec, DI rinse/N_2 dry.

ii. Deposit metals. (e.g., Ni/Ge/Au (200/425/1360 Å))

iii. Soak in acetone for >15 min.

iv. Acetone/methanol/DI rinse/N_2 dry.

v. O_2 descum 40 sccm, 50 W, 1 min.

4. Oxidation

c. Oxidize at 450 °C set temperature, 400 °C sample temperature and, 82 °C water temperature for desired oxidation length.

5. P-Metal Deposition

a. Photolithography for P-metal

i. Acetone/methanol/DI rinse/N_2 dry.

ii. Bake at 120 °C for 1 min.

iii. Spin on AZ2070 4000 rpm, 30 sec.

iv. Bake at 110 °C for 30 sec.

v. Edge bead removal.

vi. Use p-metal BF mask, expose for 45 sec at 10 mW/cm^2.

vii. Postbake at at 110 °C for 75 sec.

viii. Develop in AZ300MIF for ~40 sec (5 sec after clearing).

ix. DI rinse / N_2 dry.

x. O_2 descum 40 sccm, 40 W, 1 min.

b. P-Metal Deposition

i. HCl:H_2O (1:1) dip 30 sec, DI rinse/N_2 dry.

vi. Deposit metals. (e.g., Ti/Au (100/2000 Å))

vii. Soak in acetone for >15 min.

viii. Acetone/methanol/DI rinse/N_2 dry.

ix. O_2 descum 40 sccm, 50 W, 1 min.

c. Anneal
    i. 400 °C for 1 min

6. Silicon Nitride Deposit

a. Deposit 100 nm of SiN_x.

7. Via Etch

a. Via Photolithography
    i. Acetone/methanol/DI rinse/N_2 dry.
    ii. Bake at 120 °C for 1 min.
    iii. Spin on AZ4400 at 2000 rpm for 30 sec.
    iv. Bake at 110 °C for 2 min.
    v. Edge bead removal.
    vi. Use Via mask, expose for 40 sec at 10 mW/cm^2.
    vii. Develop in AZ400K (1:4) for ~1.5 min (5 sec after clearing).
    viii. DI rinse / N_2 dry.
    ix. O_2 descum 40 sccm, 40 W, 30 sec.
b. Dry Etch SiN_x
    i. Load sample in micro RIE
    ii. Etch SiNx, 40 sccm (CF4+8%O2), 40 W, 100 sec.
    iii. Soak in Acetone for >15 minutes.
    iv. Acetone/methanol/DI rinse/N_2 dry.

8. Plating

a. Photolithography Plating #1
    i. Acetone/methanol/DI rinse/N_2 dry.
    ii. Bake at120 °C for 1 min.
    iii. Spin on LOR at 4000 rpm, 30 sec.
    iv. Bake at 180 °C for 5 min.
    v. Remove back overflow with 400k (1:4) Qtip.
    vi. Spin on AZ4400 at 3000 rpm for 30 sec.
    vii. Bake at 110 °C for 2 min.
    viii. Edge bead removal.

ix. Use Plating mask, expose for 34 sec at 10mW/cm^2.

x. Develop in AZ400K (1:4) for ~1 min (5 sec after clearing).

xi. DI rinse / N_2 dry.

xii. Acetone/methanol/DI rinse/N_2 dry.

xiii. O_2 descum 40 sccm, 40 W, 30 sec.

b. Seed Metal Deposition

i. HCl:H_2O (1:1) dip for 1 min, DI rinse/N_2 dry.

ii. Deposit metals (e.g., Ti/Au (100/800 Å)) using rotation stage for sidewall coverage.

c. Photolithography Plating #2

i. Acetone/methanol/DI rinse/N_2 dry.

ii. Bake at 120 °C 1 min.

iii. Spin on AZ4400 at 2000, 30 sec.

iv. Bake at 110 °C for 5 min.

v. Edge bead removal.

vi. Use Plating Mask, expose for 34 sec at 10mW/cm^2.

vii. Develop in AZ400K (1:4) for ~1 min (5 sec after clearing).

viii. DI rinse / N_2 dry.

ix. O_2 descum 40 sccm, 40 W, 30 sec.

x. Bake at 120 °C 30 sec.

d. Plating

i. Etch Cu metal source.

ii. Plate at 10 mA 20% on 80% off for 6 min. (Etching current and time might vary from sample to sample)

iii. Etch In metal source.

iv. Plate at 10mA 20% on 80% off ~5 min. (Etching current and time might vary from sample to sample)

v. Soak in Acetone for >15 min.

vi. Ace spray if necessary.

vii. Acetone/methanol/DI rinse/N_2 dry.

e. Dry Etch

i. Mount sample on quartz wafer with fomblin oil and load the wafer.
ii. Turn on gas (Ti/Au sputtering), wait 10 sec, turn on RF.
iii. Watch sample clear from Au surface.
iv. Turn off RF, turn off Gas.
v. If necessary, etch Ti using 980 VCSEL file.
vi. Acetone/methanol/DI rinse/N_2 dry.

b) Top-emitting VCSEL process flow

1. Silicon Nitride Deposit
   a. Deposit 100 nm of SiN_x.
2. Mesa Etch
   a. Photolithography
      i. Acetone/methanol/ DI rinse / N_2 dry.
      ii. Bake on hotplate at 120 °C for 1 min.
      iii. Spin on AZ4400 at 2000 rpm for 30 sec.
      iv. Bake at 110 °C for 2 min.
      v. Edge bead removal.
      vi. Use BF mesa mask, expose for 42 sec at 10 mW/cm^2.
      vii. Develop in AZ400K (1:4) for ~1.5 min (5 sec after clearing).
      viii. DI rinse / N2 dry.
      ix. Resist bake at 120 °C for 1 min.
      x. O_2 descum 40 sccm, 40 W, 1 min.

   b. Dry Etch SiN_x
      i. Load sample in micro RIE
      ii. Etch SiNx, 40 sccm (CF4+8%O2), 40 W, 100 sec.
      iii. Soak in Acetone for >15 minutes.
      iv. Acetone/methanol/DI rinse/N_2 dry.
   c. Dry Etch GaAs

i. Mount sample on quartz wafer with fomblin oil and load the wafer.
ii. Turn on gas, wait 10 sec, turn on RF.
iii. Watch hi-low signal until reach the desired layer.
iv. Stop etching by turning off RF.
v. Acetone soak for 15 min.
vi. Acetone/methanol/ DI rinse / N_2 dry.
vii. Spray with acetone if necessary.
viii. O_2 descum 40 sccm, 50 W, 1 min.

3. Oxidation

a. Oxidize at 450 °C set temperature, 400 °C sample temperature and, 82 °C water temperature for desired oxidation length.

4. P-Metal Deposition

a. Photolithography
   i. Acetone/methanol/DI rinse/N_2 dry.
   ii. Bake at 120 °C for 1 min.
   iii. Spin on AZ2070 4000 rpm, 30 sec.
   iv. Bake at 110 °C for 2 min.
   v. Edge bead removal.
   vi. Use p-metal BF mask, expose for 40 sec at 10 mW/cm^2.
   vii. Postbake at at 110 °C for 75 sec.
   viii. Develop in AZ300MIF for ~50 sec.
   ix. DI rinse / N_2 dry.
   x. O_2 descum 40 sccm, 40 W, 30 sec.

b. Dry Etch SiN_x
   i. Load sample in micro RIE
   ii. Etch SiNx, 40 sccm (CF4+8%O2), 40 W, 100 sec.

c. Metal Deposition
   i. HCl:H_2O (1:1) dip 30 sec, DI rinse/N_2 dry.
   ii. Deposit metals. (e.g., Ti/Pt/Au (100/100/2000 Å))
   iii. Soak in acetone for >15 min.
   iv. Acetone/methanol/DI rinse/N_2 dry.

v. O_2 descum 40 sccm, 50 W, 1 min.

5. Silicon Nitride Deposit

a. Deposit $\lambda/2$ of SiN_x.

6. Metal Interconnect Deposition

a. Photolithography

i. Acetone/methanol/DI rinse/N_2 dry.

ii. Bake at 120 °C for 1 min.

iii. Spin on LOR at 3500 rpm for 30 sec.

iv. Bake at 180C for 5 min.

v. Remove back overflow with AZ400k (1:4) Qtip.

vi. Spin on AZ4400 at 2000 rpm for 30 sec.

vii. Bake at 110 °C for 2 min.

viii. Edge bead removal.

ix. DI rinse / N_2 dry.

x. Use Metal Interconnect Mask, expose for 43 sec at 10mW/cm^2.

xi. Develop in AZ400K for ~1.5 min.

xii. DI rinse / N_2 dry.

xiii. O_2 descum 40 sccm, 45 W, 45 sec.

b. Metal Deposition

i. HCl:H_2O (1:1) dip 30 sec, DI rinse/N_2 dry.

ii. Deposit metals. (e.g., Ti/Au (100/2000 Å))

iii. Soak in acetone for >15 min.

iv. Acetone/methanol/DI rinse/N_2 dry.

v. O_2 descum 40 sccm, 40 W, 30 sec.

7. Back side N-Metal Deposition

a. Metal Deposition

i. HCl:H_2O (1:1) dip 30 sec, DI rinse/N_2 dry.

ii. Deposit metals. (e.g., Ni/Ge/Au (150/425/2000 Å)).

b. Anneal

i. 400 °C for 1 min.

8. Plating

a. Photolithography Plating #1

i. Acetone/methanol/DI rinse/N_2 dry.

ii. Bake at120 °C for 1 min.

iii. Spin on AZ4400 at 3000 rpm for 30 sec.

iv. Bake at 110 °C for 2 min.

v. Edge bead removal.

vi. Use Plating mask, expose for 34 sec at 10 mW/cm^2.

vii. Develop in AZ400K (1:4) for ~55 sec.

viii. DI rinse / N_2 dry.

ix. O_2 descum 40 sccm, 40 W, 30 sec.

b. Seed Metal Deposition

i. HCl:H_2O (1:1) dip for 1 min, DI rinse/N_2 dry.

ii. Deposit metals (e.g., Ti/Au (100/800 Å)) using rotation stage for sidewall coverage.

c. Photolithography Plating #2

i. Acetone/methanol/DI rinse/N_2 dry.

ii. Bake at 120 °C 1 min.

iii. Spin on AZ4400 at 3000, 30 sec.

iv. Bake at 110 °C for 5 min.

v. Edge bead removal.

vi. Use Plating Mask, expose for 44 sec at 10 mW/cm^2.

vii. Develop in AZ400K (1:4) for ~1 min.

viii. DI rinse / N_2 dry.

ix. O_2 descum 40 sccm, 40 W, 1 min.

x. Bake at 120 °C 30 sec.

d. Plating

i. Etch Cu metal source.

ii. Plate at 10 mA 20% on 80% off for 6 min. (Etching current and time might vary from sample to sample)

iii. Soak in acetone for >15 min.

iv. Acetone spray if necessary.

v. Acetone/methanol/DI rinse/N_2 dry.

e. Dry Etch

i. Mount sample on quartz wafer with fomblin oil and load the wafer.

ii. Turn on gas (Ti/Au sputtering file), wait 10 sec, turn on RF.

iii. Watch sample clear from Au surface.

iv. Turn off RF, turn off Gas.

v. If necessary, etch Ti using 980 VCSEL file.

vi. Acetone/methanol/DI rinse/N_2 dry.

Appendix C

SAVE/RECALL STATE FILES FOR CASCADE MICROTECH HIGH SPEED GSG PROBE

In order to calibrate the vector network analyzer (VNA) using the Cascade Microtech GSG125 high speed probe and the standard substrate, we first need to have 4 state files for the GSG probe. These files are: “FILE00.CK”, “FILE00.I”, “FILE00.P”, and “FILE00.W”. The steps for save/recall the state files are as follows:

- Copy the state files onto a floppy disc
- Insert the floppy disk into the VNA
- Press SAVE/RECALL button
- SELECT DISC
- RECALL STATE (from the floppy)
- Press CAL

At this point we should see CalKIT [GSG125] on the right side of the VNA screen. Now, the short, open, and load calibrations can be performed using the standard substrate.

Appendix D

COMBINATIONS OF FEATURE SIZES ON RED VCSEL MASK "VCSEL_TE_RS"

Mesa diameter/ µm	Annular p-contact inner dia./µm	Annular p-contact outer dia./µm	Plating outer dia. (d_{outer})/µm	Plating inner dia. (d_{inner})/µm	Mormalized plating size (d_{norm})
14	4	11	none	none	none
14	4	11	10	4	1.5
14	4	11	12	4	2
14	4	11	16	4	3
14	4	11	20	4	4
14	4	11	24	4	5
14	4	11	34	4	7.5
14	4	11	12	5	1.4
14	4	12	20	5	3
14	4	12	24	5	3.8
14	4	12	34	5	5.8
14	4	12	20	6	2.333333
14	4	12	24	6	3
14	4	12	24	8	2
14	4	12	34	8	3.25
14	2	12	24	8	2
14	6	12	24	8	2
14	6	12	24	10	1.4
16	6	14	none	none	none
16	6	14	12	6	1
16	6	14	14	6	1.333333
16	6	14	18	6	2
16	6	14	22	6	2.666667
16	6	14	26	6	3.333333
16	6	14	36	6	5

16	6	14	14	7	1
16	6	14	22	7	2.142857
16	6	14	26	7	2.714286
16	6	14	36	7	4.142857
16	6	14	22	8	1.75
16	6	14	26	8	2.25
16	6	14	26	10	1.6
16	6	14	36	10	2.6
16	4	14	26	10	1.6
16	8	14	26	10	1.6
16	8	14	26	12	1.166667
17	7	15	none	none	none
17	7	15	13	7	0.857143
17	7	15	15	7	1.142857
17	7	15	19	7	1.714286
17	7	15	23	7	2.285714
17	7	15	27	7	2.857143
17	7	15	37	7	4.285714
17	7	15	15	8	0.875
17	7	15	23	8	1.875
17	7	15	27	8	2.375
17	7	15	37	8	3.625
17	7	15	23	9	1.555556
17	7	15	27	9	2
17	7	15	27	11	1.454545
17	7	15	37	11	2.363636
17	5	15	27	11	1.454545
17	9	15	27	11	1.454545
17	9	15	27	13	1.076923
18	8	16	none	none	none
18	8	16	14	8	0.75
18	8	16	16	8	1
18	8	16	20	8	1.5
18	8	16	24	8	2
18	8	16	28	8	2.5
18	8	16	38	8	3.75
18	8	16	16	9	0.777778
18	8	16	24	9	1.666667
18	8	16	28	9	2.111111
18	8	16	38	9	3.222222
18	8	16	24	10	1.4
18	8	16	28	10	1.8
18	8	16	28	12	1.333333

18	8	16	38	12	2.166667
18	6	16	28	12	1.333333
18	10	16	28	12	1.333333
18	10	16	28	14	1
19	9	17	none	none	none
19	9	17	15	9	0.666667
19	9	17	17	9	0.888889
19	9	17	21	9	1.333333
19	9	17	25	9	1.777778
19	9	17	29	9	2.222222
19	9	17	39	9	3.333333
19	9	17	17	10	0.7
19	9	17	25	10	1.5
19	9	17	29	10	1.9
19	9	17	39	10	2.9
19	9	17	25	11	1.272727
19	9	17	29	11	1.636364
19	9	17	29	13	1.230769
19	9	17	39	13	2
19	7	17	29	13	1.230769
19	11	17	29	13	1.230769
19	11	17	29	15	0.933333
20	10	18	none	none	none
20	10	18	16	10	0.6
20	10	18	18	10	0.8
20	10	18	22	10	1.2
20	10	18	26	10	1.6
20	10	18	30	10	2
20	10	18	40	10	3
20	10	18	18	11	0.636364
20	10	18	26	11	1.363636
20	10	18	30	11	1.727273
20	10	18	40	11	2.636364
20	10	18	26	12	1.166667
20	10	18	30	12	1.5
20	10	18	30	14	1.142857
20	10	18	40	14	1.857143
20	8	18	30	14	1.142857
20	12	18	30	14	1.142857
20	12	18	30	16	0.875
22	12	20	none	none	none
22	12	20	18	12	0.5
22	12	20	20	12	0.666667

22	12	20	24	12	1
22	12	20	28	12	1.333333
22	12	20	32	12	1.666667
22	12	20	42	12	2.5
22	12	20	20	13	0.538462
22	12	20	28	13	1.153846
22	12	20	32	13	1.461538
22	12	20	42	13	2.230769
22	12	20	28	14	1
22	12	20	32	14	1.285714
22	12	20	32	16	1
22	12	20	42	16	1.625
22	10	20	32	16	1
22	14	20	32	16	1
22	14	20	32	18	0.777778
27	17	25	none	none	none
27	17	25	23	17	0.352941
27	17	25	25	17	0.470588
27	17	25	29	17	0.705882
27	17	25	33	17	0.941176
27	17	25	37	17	1.176471
27	17	25	47	17	1.764706
27	17	25	25	18	0.388889
27	17	25	33	18	0.833333
27	17	25	37	18	1.055556
27	17	25	47	18	1.611111
27	17	25	33	19	0.736842
27	17	25	37	19	0.947368
27	17	25	37	21	0.761905
27	17	25	47	21	1.238095
27	15	25	37	21	0.761905
27	19	25	37	21	0.761905
27	19	25	37	23	0.608696
32	22	30	none	none	none
32	22	30	28	22	0.272727
32	22	30	30	22	0.363636
32	22	30	34	22	0.545455
32	22	30	38	22	0.727273
32	22	30	42	22	0.909091
32	22	30	52	22	1.363636
32	22	30	30	23	0.304348
32	22	30	38	23	0.652174
32	22	30	42	23	0.826087

32	22	30	52	23	1.26087
32	22	30	38	24	0.583333
32	22	30	42	24	0.75
32	22	30	42	26	0.615385
32	22	30	52	26	1
32	20	30	42	26	0.615385
32	24	30	42	26	0.615385
32	24	30	42	28	0.5