DISSERTATION

CDTE ALLOYS AND THEIR APPLICATION FOR INCREASING SOLAR CELL PERFORMANCE

Submitted by

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ABSTRACT

CDTE ALLOYS AND THEIR APPLICATION FOR INCREASING SOLAR CELL PERFORMANCE

Cadmium Telluride (CdTe) thin film solar is the largest manufactured solar cell technology in the United States and is responsible for one of the lowest costs of utility scale solar electricity at a purchase agreement of $0.0387/kWh. However, this cost could be further reduced by increasing the cell efficiency. To bridge the gap between the high efficiency technology and low cost manufacturing, a research and development tool and process was built and tested. This fully automated single vacuum PV manufacturing tool utilizes multiple inline close space sublimation (CSS) sources with automated substrate control. This maintains the proven scalability of the CSS technology and CSS source design but with the added versatility of independent substrate motion. This combination of a scalable deposition technology with increased cell fabrication flexibility has allowed for high efficiency cells to be manufactured and studied. The record efficiency of CdTe solar cells is lower than fundamental limitations due to a significant deficit in voltage. It has been modeled that there are two potential methods of decreasing this voltage deficiency.

The first method is the incorporation of a high band gap film at the back contact to induce a conduction-band barrier that can reduce recombination by reflecting electrons from the back surface. The addition of a $Cd_{1-x}Mg_xTe$ (CMT) layer at the back of a CdTe solar cell should induce this desired offset and reflect both photoelectrons and forward-current electrons away

from the rear surface. Higher collection of photoelectrons will increase the cells current and the reduction of forward current will increase the cells voltage. To have the optimal effect, CdTe must have reasonable carrier lifetimes and be fully depleted. To achieve this experimentally, CdTe layers have been grown sufficiently thin to help produce a fully depleted cell. A variety of measurements including performance curves, transmission electron microscopy, x-ray photoelectron spectroscopy, and energy-dispersive x-ray spectroscopy were performed to characterize these cells. Voltage improvements on the order of 50 mV are presented at a thin (1 μm) CdTe absorber condition. However an overall reduction in fill factor (FF) is seen, with a strong reduction in FF as the magnesium incorporation is increased.

Detailed material characterization shows the formation of oxides at the back of CdMgTe during the passivation process. A CdTe capping layer is added to reduce oxidation and help maintain the uniformity of the CdMgTe layer. A tellurium back contact is also added in place of a carbon paint back contact, reducing the impact of the valance band offset (VBO) from the CMT. With the addition of the capping layer and tellurium back contact a consistent 50 mV increase is seen with improved FF. However this voltage increase is well below modeled V_{oc} increases of 150 mV. CMT double hetero-structures are manufactured and analyzed to estimate the interface recombination at the CdTe/CMT interface. The CdTe/CMT interface is approximated at $2*10^5$ cm s^{-1} and modeling is referenced predicting significant reduction in performance based on this interface quality. To improve interface quality by removing the need for a vacuum break, the deposition hardware is incorporated into the primary deposition system.

Second, CdTe has a somewhat higher band gap than optimal for single-junction terrestrial solar-cell power generation. A reduction in the band gap could therefore result in an overall improvement in performance. To reduce the band gap, selenium was alloyed with CdTe using a

novel co-sublimation extension of the close-space-sublimation process. Co-sublimated layers of CdSeTe with various selenium concentrations were characterized for optical absorption and atomic concentrations, as well as to track changes in their morphology and crystallinity. The lower band-gap CdSeTe films were then incorporated into the front of CdTe cells. This two-layer band-gap structure demonstrated higher current collection and increased quantum efficiency at longer wavelengths. Material characterization shows the diffusion of selenium through the CdTe during passivation resulting in improved in lifetime and a reduced voltage deficit at lower band gaps.

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I am very grateful for the help, encouragement, collaborations, and dedication of family, friends, and colleagues. This work would not have been possible without them. It truly is a team effort.

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1. Introduction and Basic Concepts

This dissertation will begin with an introduction about the need for PV electricity and making a reasonable argument for the continued pursuit of research on the topic. This will be followed by several fundamental theories in semiconductor physics to give the reader a basic overview of the concepts covered in the results section. The physics of an electron reflector concept is discussed in detail as it is a major concept throughout the dissertation. Details of the physics, including models showing potential, and other examples in similar technologies are discussed. Section 2 will discuss the platform for which the CdTe baseline solar cell is manufactured and characterized, giving detailed hardware and process development used to establish a repeatable baseline CdTe solar cell. Fundamental steps in CdTe manufacturing, such as $CdCl_2$ passivation and contacting are discussed in detail. Sections 1 & 2 give a foundation for the primary results presented in Sections 3 & 4.

Section 3 discusses the hardware used to manufacture the CdMgTe film, including material and electrical characterization of the film. The CdMgTe layer is added to CdTe to form an electron reflector. Results are characterized and discussed including references to modeling and the demonstrated performance improvements. Detailed material characterization is conducted to assess potential material issues with the CdMgTe layer. The development of the need for a CdTe capping layer is explained. The addition of the capping layer and a new tellurium back contact to further improvements in cell performance are discussed in detail. Double hetero-structures are explored to characterize the interface recombination velocity of the CdTe/CMT interface. TRPL analysis suggests that this interface is less than ideal and may be limiting potential voltage gains. To improve the interface the CMT deposition hardware is

redesigned for the primary deposition chamber, eliminating the need for vacuum breaks at the CdTe/CMT interface.

Section 4 discusses the development of CdSeTe to be used to reduce the band gap of CdTe. Modifications are made to the CdMgTe hardware to controllably deposit CdSeTe at various concentrations. The CdSeTe films are characterized describing material and electrical variations as the concentration is increased. The band bowing concept is demonstrated and explained with increasing selenium. The reduced band gap CdSeTe layer is added to the front of a baseline CdTe cell, demonstrating improvement in the current collected at lower wavelengths and reducing the voltage deficit. Section 5 discusses the conclusions from the various chapters and gives future work suggestions for Sections 3 & 4.

1.1. Energy Overview

1.1.1. Energy Consumption and Sustainability

The United States currently uses ~28,500 terawatt hours (TWh) annually, with ~34% for residential electricity and ~25% for transportation (1). Of this 28,500 TWh, ~80% is generated by fossil fuels including petroleum, natural gas, and coal, as seen in Figure 1 (2). By definition, fossil fuels are a limited resource and will eventually become obsolete. When this will happen is speculation, but most agree we have approximately 40-50 years left at our current consumption of oil (3; 4; 5). Regardless, it is finite and it is going to leave some large power generation needs in its wake.

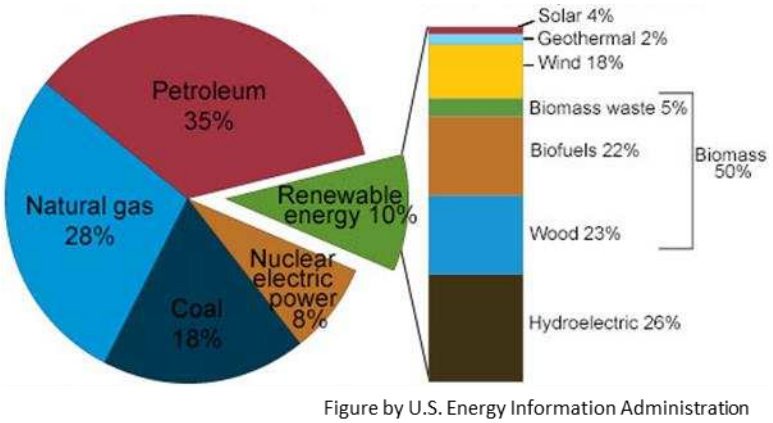


Figure 1: U.S. Energy Consumption by Source 2014 **(2)**

Another concern is the environmental changes this oil consumption is having on our habitat. Chemistry shows us that the burning of fossil fuels generate carbon byproducts, a major portion being CO_2 (6). This CO_2 generation is building up in the atmosphere that we live in and is correlating well with the onset of the industrial revolution of the 20th century and the influx of greenhouse gas emissions (CO_2) represented in Figure 2 (7; 8). These growing greenhouse gas emissions pose a potential health risk. Acceptable CO_2 levels in structural design are <600ppm, OSHA standards are 1000ppm with heath conditions occurring over 1000ppm (9). We are currently at 402 ppm and increasing at about 2.11 ppm per year (10). If we assume no increase in CO_2 production then in approximately 95 years we will be over OSHA standards (11). Thus a child born today could suffer from air quality complications in their lifetime.

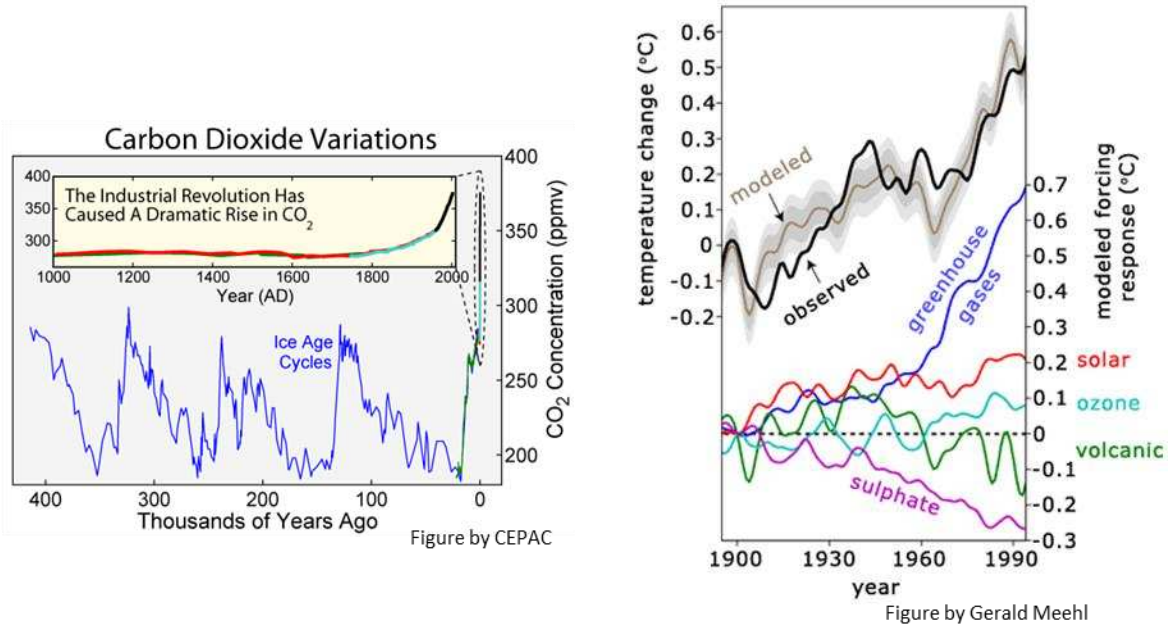


Figure 2: (left) Carbon Dioxide Variations for the last 400,000 years (7), (right) Metric Tons of CO_2 generated by various sources for the last 100 years (8)

Fossil fuels are finite and as they're burned they have an environmental effect which eventually will have a detrimental impact on air quality. This means that our current energy generation model is unsustainable. Technologies need to be developed that can replace our current magnitude of energy production and preferably, without making the environment uninhabitable. Some current renewable technologies may be the answer. Demonstrated in Figure 1, renewables already make up about 10% of energy generation, however only about 5% are going to be directly emissions free or carbon neutral: solar, wind, hydro, and geothermal. There are only two of these current energy sources with the potential of reaching 16TW theoretically: solar and wind (12; 13). Figure 3 shows approximate values (estimated by BP) for what is available in reserve for our fossil fuels globally (Coal, Petroleum, Natural Gas) and the potential per year energy generation of various renewable technologies. The graph puts both fossil fuel reserves and per year renewable potential to scale with the current world energy usage for

reference. Figure 4 demonstrates the basics supply and demand problem for energy consumption in the modern world. Solar has by far the largest potential of filling the energy demand left behind when fossil fuel reserves deplete. The current challenge lies in making solar power generation financially preferred and scaling the manufacturing capacity.

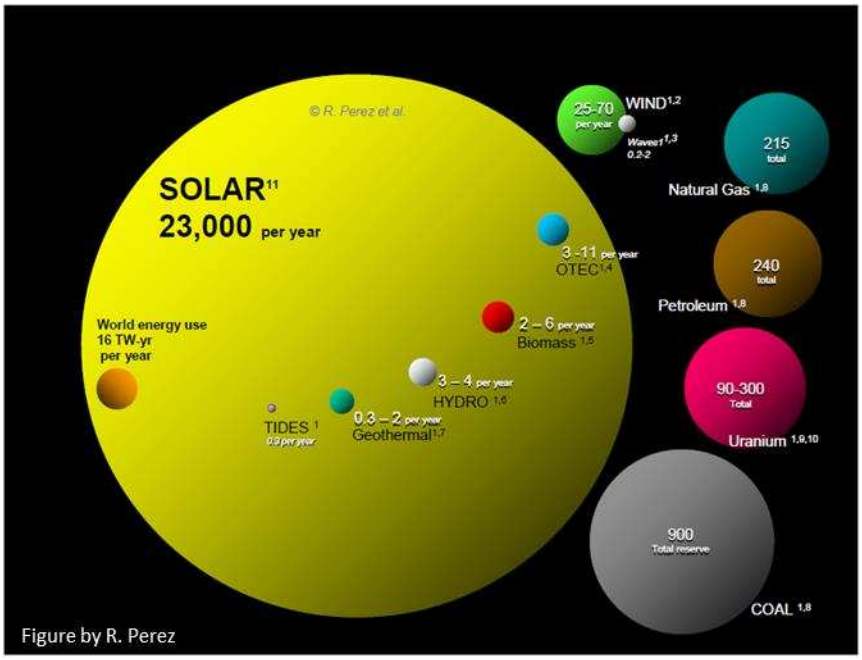


Figure 3: (top) Graph of world extractable and technical potentials for the various renewable energy sources (13)

1.1.2. Solar as a Solution

The growth of photovoltaics has been exponential over the past 10 years and has shown a constant decrease in production cost as the technology scales in manufacturing, shown in Figure 4 (14; 15). This growth is expected to continue with roughly 20 GW of shared solar installed in the U.S. and another 20 GW to come online in the next two years as the government is pursuing its SunShot goal of a $1 per watt installed by 2020, yielding ~0.06 $/kWh energy production (14; 16). That is well below the national average of 0.11 $/kWh. Solar is currently equal to the national average cost and has hit as low as 0.0387 $/kWh (17). This cost is thought to be the

lowest electricity generation price in the USA ever, coming from a 100MW solar plant to Utility Nevada (16; 18; 17).

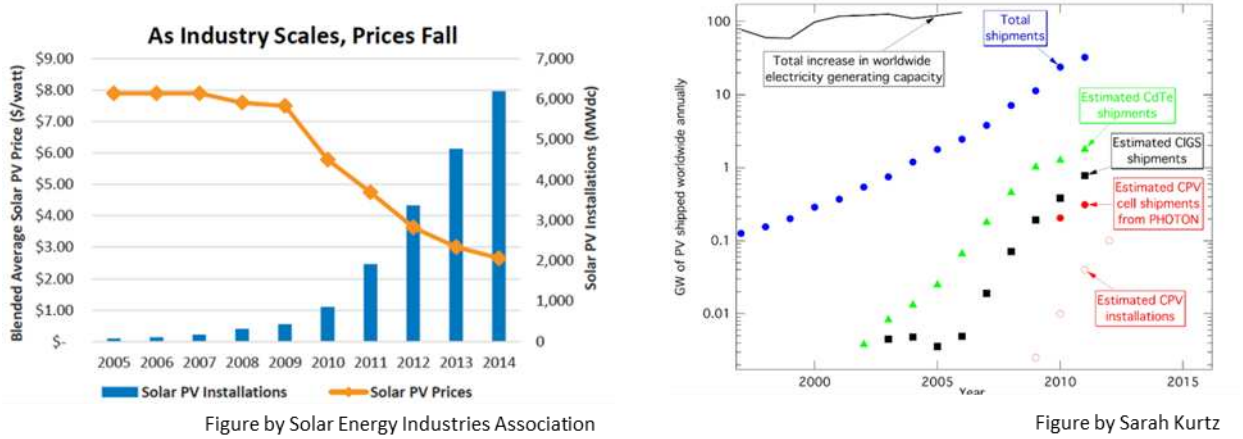


Figure 4: (left) Cost of Solar PV prices and the amount of U.S. PV installations (14), (right) Growth of PV Industry (15)

Module costs were cut in half over the past 3 years from manufacturing and cell performance improvements, representing the majority in cost reduction of utility scale power production, Figure 5 (19). The number one solar cell manufacturer in the U.S. is First Solar, who is responsible for one of the lowest solar power plant to utility cost. This solar power utilizes a thin film technology, Cadmium Telluride (CdTe) as the absorber. CdTe cell performance in the last 5 years has improved dramatically, from ~16% to 21.5%, with module efficiencies over 18% (20; 21). This makes CdTe more efficient and cheaper than the 10 year stagnate multi-crystalline Silicon (multi-si) solar cell technology. With the market share of CdTe at only ~10%, and multi-Si closer to 50%, the improved performance and cost of new CdTe technologies makes it a potential dominate PV technology in years to come, and the favored technology to achieve the SunShot goal (22; 23).

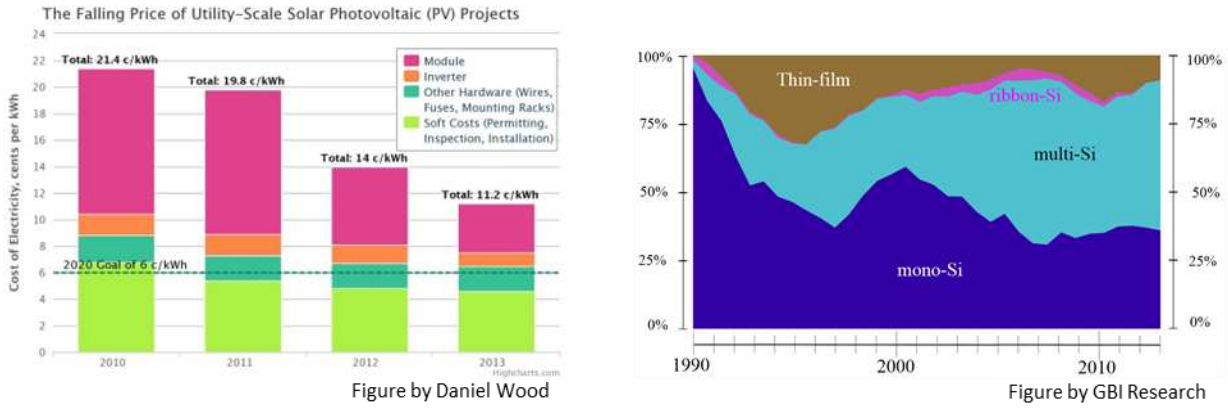


Figure 5: (left) Price of Utility-Scale Photovoltaic Projects (19), (right) Global Market Share by PV Technology (22)

1.2. PV Basics and Characterization:

Photovoltaic solar cells directly convert light from the sun into electricity. The light received from the sun can be broken up into little energy packets called photons and these photons have different energies that we see in the visible range as color. Figure 6 (left) shows the rate at which these photons hit the earth at various energies. As the photons hit our solar cell the photons are absorbed and excite electron and hole pairs, Figure 6 (right). These charge carriers in the solar cell material are swept out by a built-in-field generated by a P-N junction.

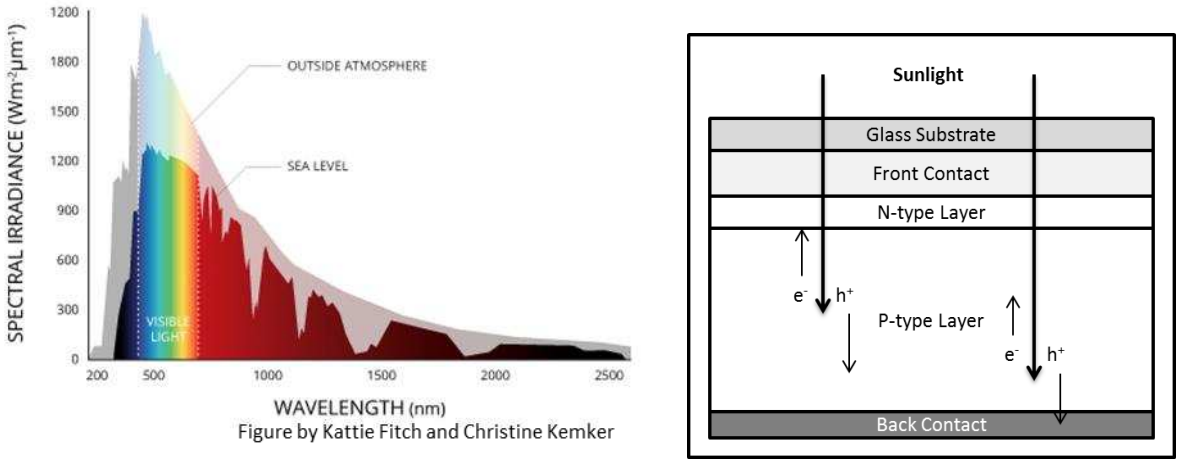


Figure 6: left) The solar spectrum (24) right) A schematic of a simple conventional solar cell, the creation of electron-hole pairs

1.2.1. The Formation of a PN junction

The Formation of the P-N junction comes from the combination of an N-type and P-type semiconductor. P-type semiconductors can be doped to have impurities that are acceptors of electrons and are known as positive type (p-type). Semiconductors doped to have impurities that are donors of electrons are known as negative type (n-type). For example, a common semiconductor like silicon can be doped p-type by adding boron or n-type by adding phosphorus. The Fermi energy level is defined as the energy level with a 50% probability of being occupied. Intrinsic materials have the same number of electrons and holes and so the Fermi level is near the center of the band gap. The position of the Fermi level in extrinsic materials is a function of the concentration of donors and acceptors, their energy level, and the temperature of the material. The Fermi level moves up or down to maintain a charge density balance between the concentrations of free charge carriers and immobile ionized dopants.

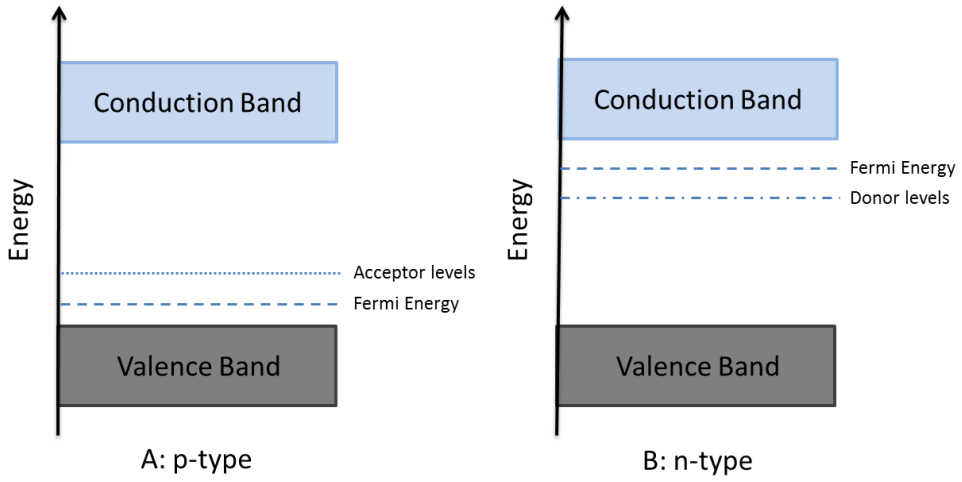


Figure 7: Position of Fermi energy a) p-type b) n-type semiconductors (25)

P-type materials have the Fermi level shifted towards the valence band because of the presence of dopants at the acceptor energy state (Figure 7a). N-type materials have the Fermi level shifted toward the conduction band due to presence of dopants at a donor energy state

(Figure 7b). As separate materials the Fermi levels do not align (Figure 8a), however when the n-type and p-type materials are brought together a p-n junction is formed which is referred to as a diode. At equilibrium and without the presence of photons and temperature gradients, the Fermi levels in the two materials must be the same on each side of the junction causing the bands to bend as shown in Figure 8a. As the bands bend, a net negative charge imbalance sets up in the p-type region adjacent to the junction and a net positive charge imbalance sets up in the n-type region. These charge imbalances are caused by donor and acceptor ions in the n-type and p-type regions respectively. The collective volume of these two space charge regions is called the deletion width of the diode. The magnitude of the space charge in each material must be equal. These adjacent positive and negative space charge regions develop an electric field that retard further diffusion of majority charge carriers and this field is referred to as the built-in-field.

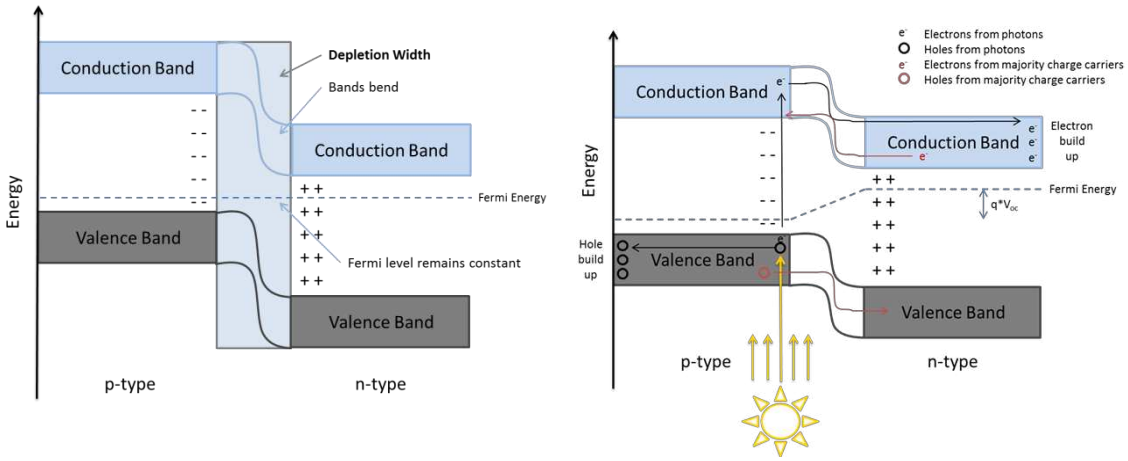


Figure 8: a) The p–n junction b) p-n junction under photon bias.

There are two types of p-n junctions, a homo-junction or a hetero-junction. Homo-junctions use the same semiconductor material, which is doped to form both the p-type and n-type regions. Hetero-junctions are formed using different materials for the n-type and p-type. In general, the interface of a homo-junction device is superior since the same base material is used

on both sides of the junction. This limits the formation of energy barriers and recombination sites that reduce cell efficiency. Hetero-junctions allow for the window layer and absorber layer band gaps to be engineered around the solar spectrum to limit absorption losses and induce barriers to carriers diffusing the wrong direction. However they often suffer from losses due to energy barriers and recombination sites.

As a diode is exposed to light, photons are absorbed and hole-electron pairs are generated within the depleted width region. The built-in-field will push the electron towards the n-type and the hole towards the p-type. The Fermi energy and built-in-field will adjust to allow the flow of electrons and holes from the majority charge carriers to balance the photo-generated current. As the electrons and holes build up, the Fermi level will change across the diode establishing a voltage difference between the front and back contacts (Figure 8b). This voltage difference developed under light illumination at an open circuit condition is known as the open circuit voltage (V_{oc}) of the photodiode. If the photon generated hole-electron pairs are swept out of the diode region and complete the circuit to the back contact under no load, a short circuit current is generated (J_{sc}). This generated current is generally normalized by the area, denoted J (current density). The current density through the diode as a function of voltage can be describe by the diode equation:

$$\boldsymbol{J = J_{sc} - J_o \left(e^{\frac{qV}{nkt}} - 1\right)} \quad (1)$$

J: Current Density

J_{sc}: Short Circuit Current Density

J_o: Dark Saturation Current (Leakage Current) Density

V: Applied Voltage

n: Ideality Factor

q: Electron Charge (absolute)

k: Boltzmann's Constant

t: Absolute Temperature

1.2.2. PV Characterization Techniques

The V_{oc} and J_{sc} conditions are standard parameters used to describe the performance of a photodiode, however neither point will generate power. At the open circuit voltage condition there is no current flow and similarly at the short circuit current condition there is no voltage potential, both result in no power output. As a load resistance is varied between the open circuit and short circuit condition, a current density vs. voltage (J-V) curve is generated (Figure 9). The parameters J_{sc} and V_{oc} are represented by the axis intercepts of the solid line, the dashed line represents the power generation at any given point along the load sweep. The maximum power point (mp) is represented in Figure 9 corresponding to the maximum power voltage (V_{mp}) and maximum power current density (J_{mp}) of the cell. Fill factor (FF) is a characteristic parameter comparing the max power point to the product of open circuit voltage and short circuit current (Equation 2). The higher the FF, the closer the max power point will be to the potential max power point.

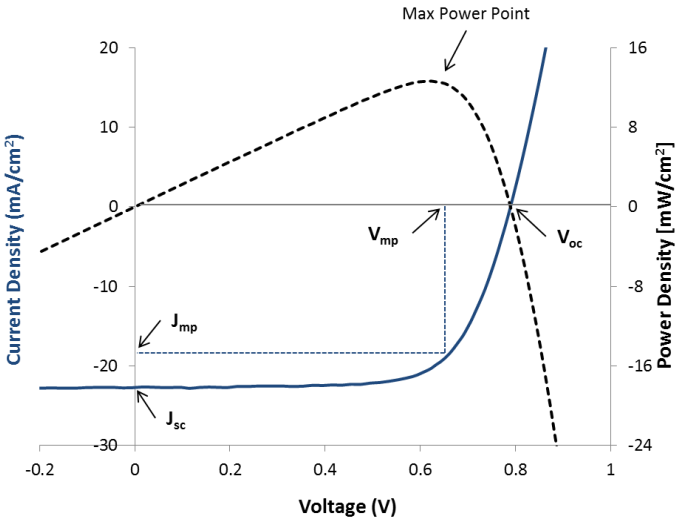


Figure 9: J-V curve of a CdTe cell with overlaid resulting power density, parameters V_{oc}, J_{sc}, V_{mp}, J_{mp} are identified

$$\boldsymbol{FF = \frac{V_{mp} \cdot J_{mp}}{V_{oc} \cdot J_{sc}}} \tag{2}$$

Efficiency (η) of the solar cell is calculated by comparing the power from one sun illumination, to the power generated by the cell at the maximum power point (Equation 3). The input power density is ~100mW/cm^2, and if the cell generates ~12mW/cm^2 the resulting cell efficiency is 12%. The efficiency of a solar cell is directly related to the V_{oc}, J_{sc}, and FF parameters of the cell and these characteristic parameters are commonly used to describe the ability of a photovoltaic cell in converting the solar spectrum to electricity.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{oc} \cdot J_{sc} \cdot FF}{P_{in}} \tag{3}$$

1.3. How does a Electron Reflector Improve Voltage

A possible mechanism for voltage loss in CdTe solar cells has been associated with back surface recombination, between the CdTe and the back contacting material. This interface generally forms a Schottky barrier and due to the poor band matching of common metals a valance band offset is formed (26). If the CdTe/back contact interface has a high recombination velocity, then the V_{oc} and efficiency will be reduced, shown in Figure 10a (27; 28). A potential solution is to induce a conduction band offset at the back to prevent the minority carriers from reaching any high recombination interfaces as shown in Figure 10b. If the cell is fully depleted, any generated carriers would be reflected away from the back interface, effectively decreasing the back-surface recombination. Thus this CBO offset is reflecting both photoelectrons and forward-current electrons away from the rear surface. Higher collection of photoelectrons will increase the cell's current, and reduction of forward current will increase its voltage. This concept is referred to as an electron reflector.

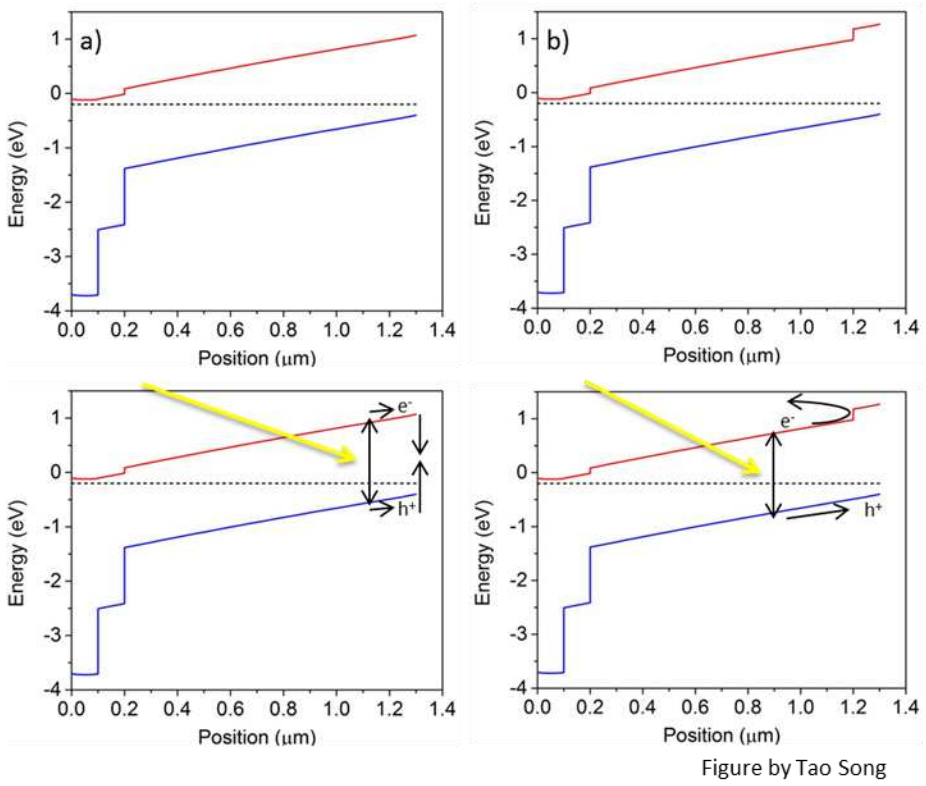


Figure 10: Electron Reflector Concept a) No CBO, b) With a CBO

1.3.1. Mechanisms to make an Electron Reflector

There have been three mechanisms proposed to make an electron reflector (ER) in CdTe (27). Figure 11 shows the band diagrams for the three structures proposed. Type A, the expanded-band-gap structure, utilizes an additional film where the ER layer has an increased band gap in comparison to the bulk absorber. This Type A layer also needs to have an electron affinity that allows the increase in band gap to be in the conduction band. This concept was studied in Section 3 using CdMgTe. The next option is a Type B reversed back barrier, where the bulk absorber band gap is reduced and the band gap at the back remains the same, generating the desired offsets. This method is studied in Section 4 of this manuscript using CdSeTe. Finally Type C where the material is doped heavily p-type at the back surface causing the conduction and valance band to increase. This doping effect already occurs in the CdTe to some degree, the

back surface is either etched leaving a tellurium rich layer or a tellurium layer is added, followed by a copper doping process forming p^+ Cu_xTe. Type C is not studied as an electron reflector concept in this manuscript

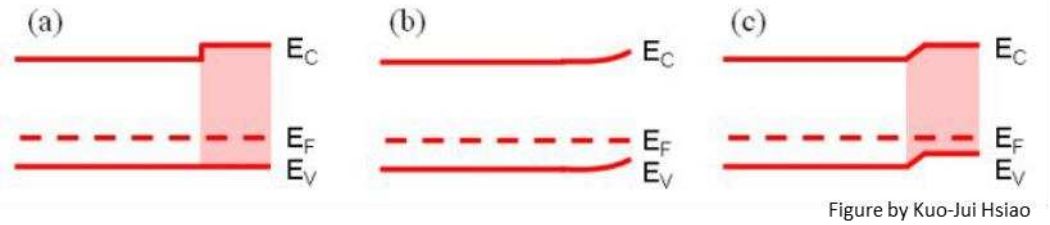


Figure 11: Band diagrams of the three prosed ER structures: a) expanded band gap layer, b) reversed back barrier, and c) heavily doped back surface (27)

A modeled comparison of these three ER structures was conducted by K. J. Hsiao in his Ph.D Thesis and is shown in Figure 12 (27). This figure shows the JV performance parameters (V_{oc}, J_{sc}, FF, and η) for all three ER structures against their respective parameters: ϕ_e for type A increased back barrier in the conduction band, ϕ_b for a revered back barrier where the bulk band gap is lowered, and ρ_{ER}/ρ_{bulk} for a heavily doped back surface. All three structures can increase the overall efficiency of the cell, however type A and B appear to help V_{oc} most significantly. Type C according to the model would require an increase of ~10^5 compared to the bulk doping, to get a similar effect to type A and B. With a bulk doping of ~10^{14} in CdTe, and current work in the field to increase this to 10^{16}, this would mean a back contact doping of 10^{19}-10^{21}. This would be difficult for CdTe due to its compensating tendencies in polycrystalline growth (29).

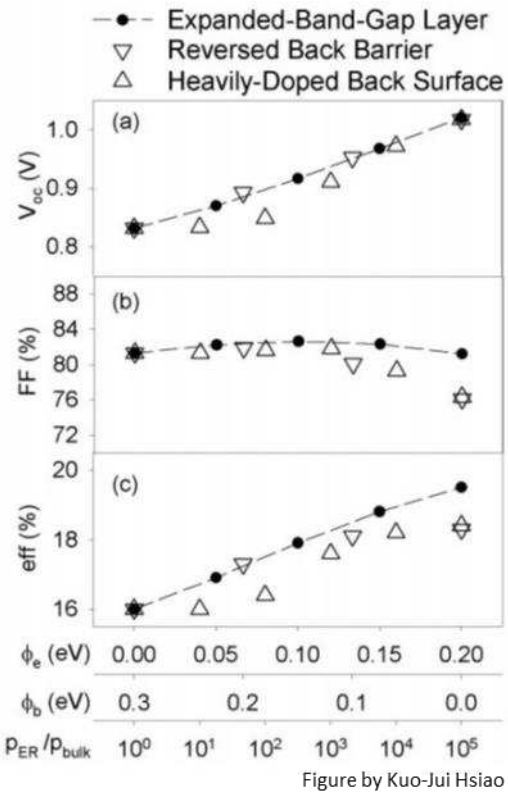


Figure 12: Comparison of the ER structures Type A, B, and C as a function of their respective parameters (27)

1.3.2. Electron Reflector Concept in other Technologies

1.3.2.1. Silicon HIT Cell

The original hetero-junction solar cell, the HIT cell, is an intrinsic thin-layer structure which is composed of monocrystalline and amorphous silicon (a-si) layers. The monocrystalline layer acts as the absorber and the capping amorphous layers passivate and induce the desired barrier heights to block minority carriers as depicted in Figure 13. By heavily doping a higher band gap material (a-si) P and N-type, an ideal double hetero-junction is formed, Figure 13a. The HIT cell also uses the intrinsic a-Si layers between the heavily doped p^+ and n^+ layers as a type of buffer. The formation of these barriers and passive interfaces has been the key to the improved voltage and efficiency of c-Si solar cells (30; 31).

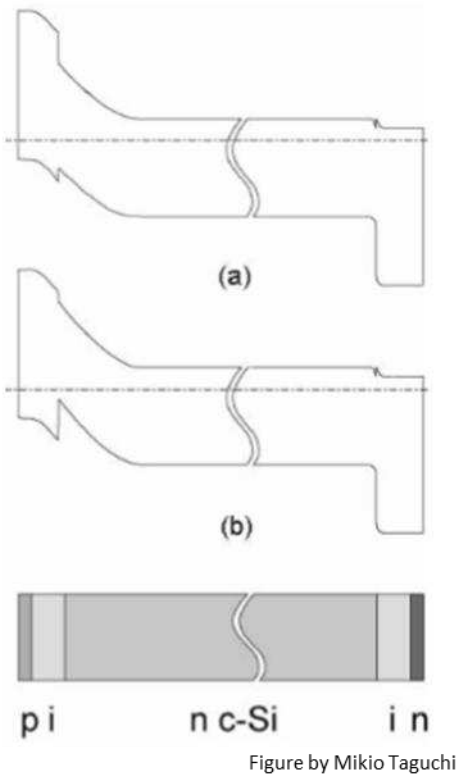


Figure 13: Schematic Diagram of the HIT cell a) Ideal double hetero-junction b) Estimated (30)

1.3.2.2. CMT Double-Hetero-Structure

Similar to the HIT cell previously described, a CMT double hereto-structure has been deposited and characterized by Arizona State University (ASU) with lifetimes measured over 3 μs and an open circuit voltage of 1.096 V (32). To achieve a high carrier lifetime and voltage the cell is grown on InSb (001) substrates using molecular beam epitaxy consisting of a CdTe absorber with CdMgTe layers on both sides forming a CdTe/CMT double hetero-structure (DHS). This CMT DHS design offers optimal confinement for minority carriers and excellent passivation of the surfaces of the CdTe absorber interface. Figure 14 outlines the cell structure and layer details. Note the CMT develops a CBO and VBO on each side of the cell similar to the HIT cell. One significant difference from the HIT cell is the front contact junction should be as transparent as possible to minimize parasitic losses. A significant difference from polycrystalline

work is the doping ($10^{16\text{-}18}$ cm^{-3}) of various layers and low interface recombination velocity (IRV) of the interfaces. These devices were made by MBE and were single crystal devices.

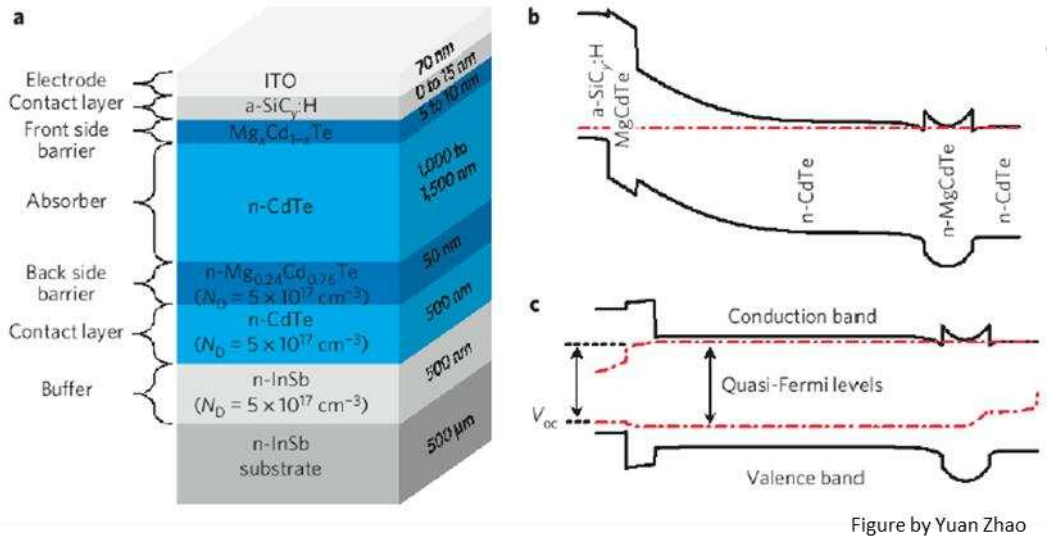


Figure 14: Device design and band diagram, a) layer structure of the CdTe/CMT DHS solar cell. Schematic band diagrams at b) equilibrium c) open circuit (32).

1.3.2.3. CIGS

Copper Indium Gallium Selenide ($CuIn_{(1-x)}Ga_xS$) solar cells utilize a version of the Type B ER structure. By varying the gallium content (x=0-1) in CIGS cells the band gap can be altered from CIS ~1.0 eV to 1.7 eV (CGS). Figure 15 shows the change in the band structure of a CIGS cell as the gallium content is increased towards the back of the cell. A conduction band offset is induced and helps prevent any flow of minority carriers to the back, also reducing back-contact recombination. This improves the performance of the cell, increasing V_{oc} by ~90mV (28). This has allowed CIGS to be able to generate more voltage at a given band gap than any other thin film technology (33), with a record cell efficiency of 21.0% (34).

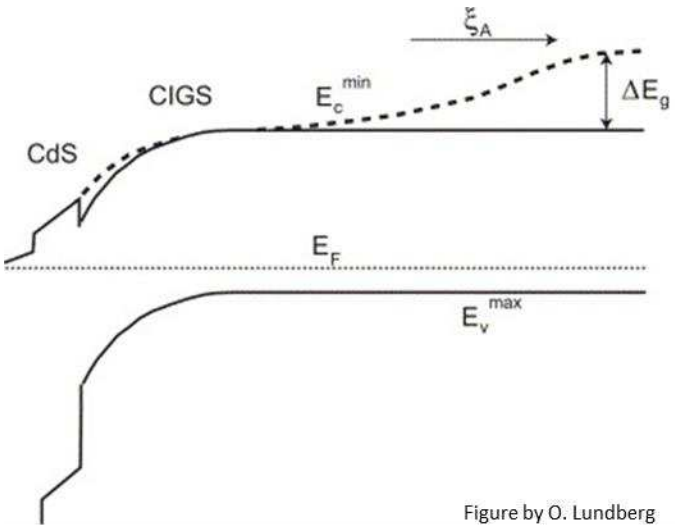


Figure 15: Band diagram of a CIGS cell, dotted line shows the change in the CBO as the Ga content is increased (35)

1.3.2.4. III-V

Solar cells comprised of elements from group III (aluminum, gallium, and indium) alloyed with group V (phosphorous, arsenic, antimony) can be band gap graded with induced offsets at the front and back of the cell. This has allowed GaAs cells to reach single band gap efficiency of 28.8% and multi-junction cells achieving efficiencies of ~37.9% with a InGaP/GaAs/InGaAs structure (34). Figure 16 demonstrates the versatility in the III-V group in regards to the induction of offsets. Figure 16 shows the formation of conduction and valance band offsets of AlGaAs and GaInP layers on p-type GaAs absorbers. In both cases these films passivate the back contact and prevent recombination and a barrier to minority carriers with a desired band offset.

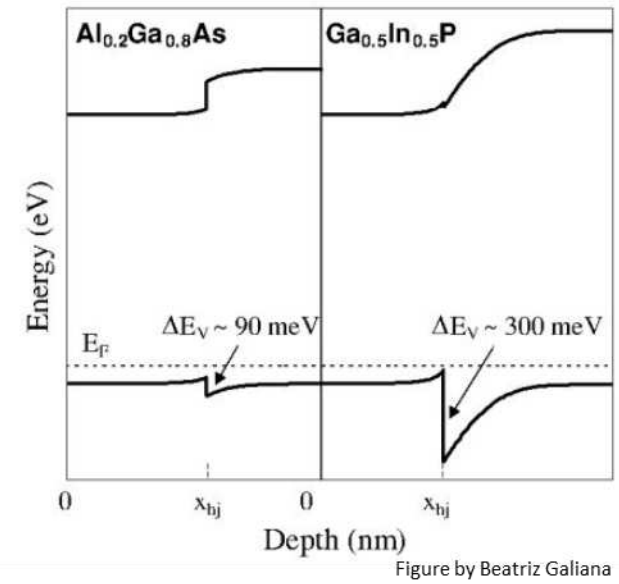


Figure 16: (Left) Band diagrams of a p-GaAs/$Al_{0.2}Ga_{0.8}As$ hetero-junction and (right) band diagram of a p-GaAs/$Ga_{0.5}In_{0.5}P$. Doping level held constant 3 x 10^{17} cm^{-3} (36)

2. CdTe Solar Cells

As mentioned previously, CdTe is the number one manufactured solar cell technology in the United States (37). It currently has the highest module efficiency among all thin film technology and multi-crystalline silicon (20; 34; 21). It also is the technology used in the cheapest cost per watt utility scale solar generation in the USA to date (17).

2.1. CdTe Manufacturing at CSU

Section 2.1 is based on published work in the Journal of Vacuum Science and Technology A (38). It was written in collaboration with Jason M. Kephart, Pavel S. Kobyakov, Kevin Walters, Kevan C. Cameron, Jennifer Drayton, James R. Sites, Kurt L. Barth, W.S. Sampath. I'm thankful for funding support from NSF's Accelerating Innovation Research, DOE's SunShot, and NSF's Industry/University Cooperative Research Center programs. Assistance with the research from Amit Munshi, Tushar Shimpi, Keegan Barricklow, Andrew Moore, Russell Geisthardt, John Raguse, Marina D'Ambrosio, Christina Moffett, Carey Reich, and Lauren Swanson are gratefully acknowledged.

Photovoltaic technologies have shown efficiencies of over 40% on MBE grown single crystal cells, however manufacturing costs have prevented a more significant energy market penetration. To bridge the gap between the high efficiency technology and low cost manufacturing a research and development tool and process was built and tested. This fully automated single vacuum PV manufacturing tool utilizes multiple inline close space sublimation (CSS) sources with automated substrate control. This maintains the proven scalability of the CSS technology and CSS source design but with the added versatility of independent substrate motion. This combination of a scalable deposition technology with increased cell fabrication

flexibility has allowed for high efficiency cells to be manufactured and studied. The single vacuum system is capable of fabricating a 3.1 x 3.6 inch substrate every 45 minutes with a cell efficiency of 12% with a standard deviation of 0.6% as measured over 36 months. The substrate is generally scribed into 25 small area devices allowing for over 250 small area devices to be fabricated each day. The system can operate uninterrupted for maintenance for over 21 days.

2.1.1. CdTe Manufacturing Introduction

The growing photovoltaic (PV) market requires technologies that utilize economic large-scale manufacturing with high device efficiency. Cadmium telluride (CdTe) has been expanding in the PV market because of its proven low cost manufacturing and a band gap that is ideal for the Shockley-Queisser limit (39). Using the CdTe technology, First Solar Inc. has made a power purchase agreement (17) at 0.038 $/kWhr and has developed small-area CdTe cells with efficiencies up to 21.5% (34).

Previously, the Colorado State University PV Manufacturing Lab developed a belt driven close space sublimation (CSS) technology for continuous in-line processing of CdTe solar cells (40; 41). This technology was scaled up to where a former company, Abound Solar, was able to produce CdTe solar cells at a production capacity (42) of 200 MW/Yr, at ~0.75 $/W. However the CdTe PV technology is still well below the projected cell efficiency (33; 43). To develop efficiency-improving technologies for the CdTe technology without losing the scalability of manufacturing, the belt-driven continuous in-line processing technology was modified to incorporate more versatility in processing.

As many new theories are being generated to improve CdTe solar cells (44; 45; 46; 47; 48) a more flexible R&D system was needed for scientific studies of these new performance

enhancing ideas. The new system maintained the in-line fabrication heritage of the previous scalable belt CSS system but eliminates the restriction of a single pre-defined process sequence with equal dwell times. This increased versatility of the deposition order and time allows for each substrate to have a unique deposition process. This manufacturing tool has been referred to as the Advanced Research and Development System (ARDS), but is more commonly known as the Single-Vacuum Close Space Sublimation Chamber. With demonstrated CdTe solar cells efficiencies of ~12% from the previous belt driven system, the new system was designed to mimic historical performance results but with increased versatility, reliability, and repeatability. To meet these criteria, finite element analysis and computational fluid dynamics modeling techniques where used in all design and development stages of the project (49; 50; 51).

2.1.2. CSS Deposition Chamber

2.1.2.1. The R&D Manufacturing Tool:

The baseline CdTe cell manufactured in the CSS deposition chamber begins with a TEC12D substrate commercially available from Pilkington. Glass substrates are purchased pre-cut to the standard 3.1 x 3.6 inch size (Hartford Glass). The substrate is cleaned using a 30 min IPA rinse, then a 1 hour 50^{o} C heated sonication in 1% Micro-90 and deionized water. This is followed by a 30 min heated deionized water sonication rinse. The substrates are dried using Marangoni drying (52) in which the water is slowly drained while nitrogen saturated with isopropyl alcohol flows over the surface. This creates a surface tension gradient that reduces the amount of water residue which can dry and contaminate the surface.

A single piece of glass is inserted into the chamber where the TCO is plasma cleaned in a hollow cathode plasma reactor (53). A 100-nm CdS window layer is deposited, followed by a

2.0-μm CdTe absorber layer. The CdTe layer is then passivated with a $CdCl_2$ treatment and doped using copper. The glass substrate is removed from the chamber and carbon and nickel paint are sprayed on for back contacting. This forms what is known as the baseline cell structure depicted in Figure 17.

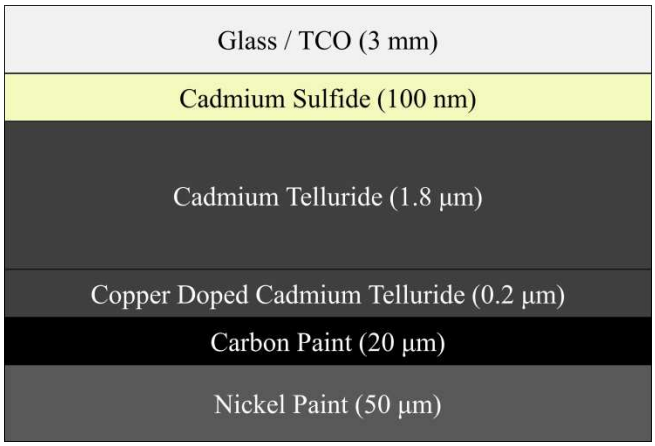


Figure 17: A diagram depicting the various layers that comprise the baseline cell structure of a typical CdS/CdTe cell manufactured in the single vacuum CSS chamber.

From plasma cleaning the glass through the final step of copper doping, all cell manufacturing is performed in this single-vacuum CSS deposition chamber. Figure 18 shows a diagram of the key components of the system. To enable multiple deposition and passivation stations, the chamber utilizes a series of inline CSS sources. A load-lock is incorporated for inserting and removing samples, increasing the throughput of the system. Finally, a magnetic transfer arm is used to move the substrate through the chamber. The system uses two Leybold D65 mechanical pumps to cycle the load lock and back the Varian VHS4 diffusion pump with a cold water baffle which gives a base pressure of $8*10^{-7}$ mTorr.

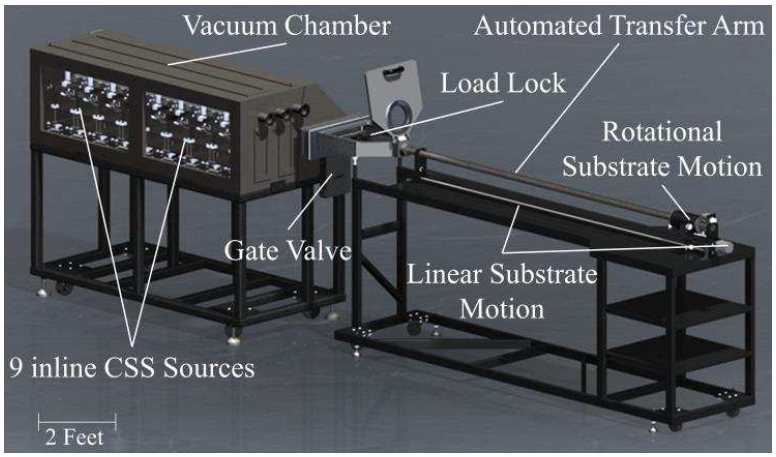


Figure 18: A diagram of the Single Vacuum Closed Space Sublimation Chamber with various key components being identified.

2.1.2.2. The CSS Sources

An illustration of 1 of the 9 deposition sources is shown in Figure 19A. It is comprised of two DFP grade graphite sources; a top substrate heater and a bottom CSS deposition source. The bottom source holds the desired material to be deposited and the top source is used to maintain substrate temperature during deposition. A counterweight shutter system is utilized to move a shutter over the CSS deposition source to contain the vapor pressure of the sublimating material when not in use. This prevents source-to-source contamination and material deposition outside the source. The substrate motion into the deposition source pushes the shutter open allowing for thin film deposition.

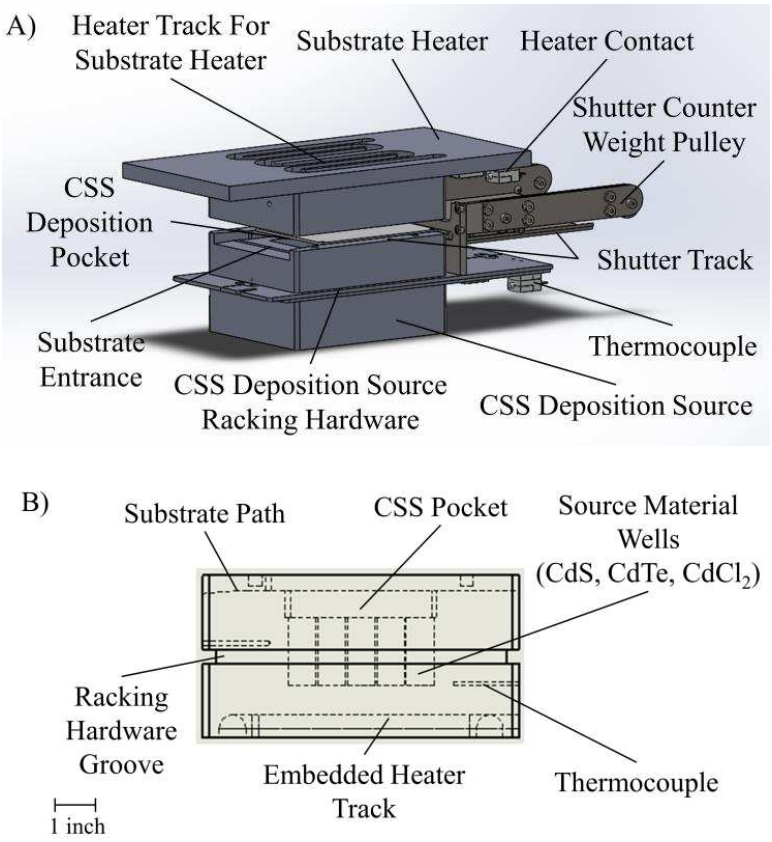


Figure 19 A) CAD of a full CSS source of 1 of 9 typical deposition stations highlighting key components B) A cross-sectional CAD drawing of the bottom deposition source identifying notable features.

During processing, the deposition source is maintained at sublimation temperatures using an embedded 80/20 Ni-Cr resistive heater which is potted into the graphite CSS deposition source using a Cotronics Resbond 920 ceramic paste (54). Above the embedded heater are 20 wells spread across the interior of the pocket for the sublimation material, depicted in Figure 19B. The temperature set point of each source is dependent on the material being sublimated. A channel on the front of the source guides the end effector and glass substrate into the source and a groove is milled around each source for racking hardware to hold the sources in place. This allows for easy insertion and extraction of each individual source enabling the system to be changed or maintenance in less than a work day. The system receives a bi-weekly preventative

maintenance in which deposition material is added and excess buildup is removed. This keeps the system at a more consistent state rather than maintenance after failure.

2.1.2.3. The End Effector (Substrate Motion)

To allow for variation in fabrication sequence and timing an automated transfer arm with a 718 Inconel end effector design is utilized. The end effector is used to hold the substrate throughout the deposition process. The magnetic transfer arm is a custom magnetic manipulator from Transfer Engineering based of the DBLRP and DBLOP models allowing two-dimensional motion of the end effector and substrate to each deposition source. As depicted in Figure 18 and Figure 20, the end effector moves from source to source using a lead screw and in and out of each source using a rack-pinion gear. This allows the substrate to enter all deposition sources in any sequence. The automation is controlled by LabVIEW™ software, allowing for a custom user interface and real time motion control. This automation is capable of manufacturing ~250 small-area devices (SADs) over 10 substrates within a single work day.

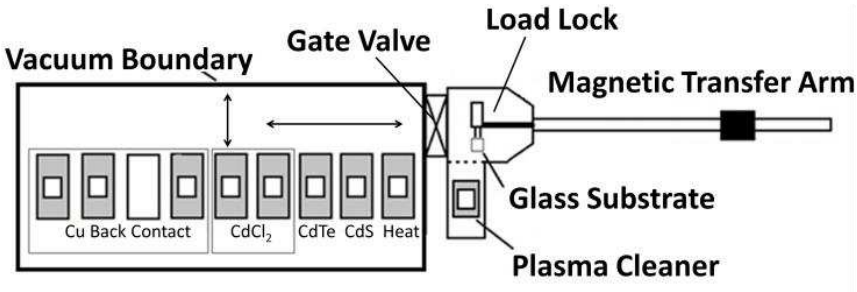


Figure 20: A diagram depicting the 2 dimensional motion of the end effector and substrate through the deposition chamber.

2.1.3. Cell Fabrication Process

2.1.3.1. Process Temperature and Times

The deposition of each layer and the corresponding passivation and doping treatments are all completed in the CSS chamber. The chamber is maintained at 40 mTorr with a 100 sccm MFC flow controller allowing various gases to be used but the standard process uses a mixed gas of 98% N_2 and 2% O_2. Prior to each run the end effector is thermally cleaned before every substrate at 620^o C for 440 s to remove possible contamination from the previous deposition. The substrate, Pilkington TEC12D for the baseline, is plasma cleaned in an oxygen environment for 30 s at 200 mTorr[16]. The glass is heated to 465^o C in 110 s in a 620^o C environment and then transferred to the CdS source in < 5 s using the automated transfer arm. A 100 nm layer of CdS is deposited in 110 s at a substrate temperature of 465^o C. Then a 2.0-μm CdTe layer is deposited at a substrate temperature of 480^o C in 110 s. The CdTe film is then passivated with a 180 s $CdCl_2$ treatment followed by a 180 s anneal at 400^o C. The sample is cooled for 500 s to 150^o C and then doped using a 190^o C CuCl treatment with a 200^o C anneal for 220 s. The substrate is cooled to room temperature and rinsed with DI water to remove any residual $CdCl_2$. Each source operates at an optimized temperature for the substrate, substrate heater, and source heater. Table 1 shows the source and substrate temperatures for each source as well as the deposition time for each station as measured by Pyrometry.

Table 1: Process time and temperatures for each CSS station from left to right in sequential order for the baseline cell

Source	**Heater**	**CdS**	**CdTe**	**$CdCl_2$**	**$CdCl_2$ Anneal**	**Cool**	**Cu**	**Cu Anneal**
Time (s)	110	110	110	180	180	500	110	220
Substrate Temp In (^oC)	20	465	480	460	430	405	150	170
Substrate Temp Out (^oC)	465	480	460	430	405	150	170	195
Substrate Heater (^oC)	620	480	360	387	400	50	170	210
CSS Deposition Source (^oC)	620	620	555	435	400	50	200	210

2.1.3.2. $CdCl_2$ Treatment

The $CdCl_2$ treatment is a combination of both a vapor and sublimation treatment. As the $CdCl_2$ passivation begins, the substrate is at 460^o C resulting in a purely vapor $CdCl_2$ treatment. The substrate heater is at 387^o C thus causing the substrate to cool to 430^o C during the 180 s treatment this reduction in substrate temperature results in the deposition of a $CdCl_2$ film at the end of the treatment. This $CdCl_2$ film is then inserted into an anneal station for an additional 180 s at 400^o C. Additional analysis and details of this $CdCl_2$ process is discussed in (55).

2.1.3.3. Cu Doping

The copper doping process is performed by exposing the CdTe surface to a CuCl vapor. This is believed to be primarily a reaction based mechanism opposed to a deposited layer as less than 1-nm of copper is incorporated into the CdTe (56). Doping of the CdTe is required to limit the effect of a back barrier that can form when CdTe is contacted. Due to the natural high work function of CdTe, a high work function material is required to limit the formation of an opposing

diode, forming a barrier in the valance band restricting the flow of holes (57) as shown in Figure 21.

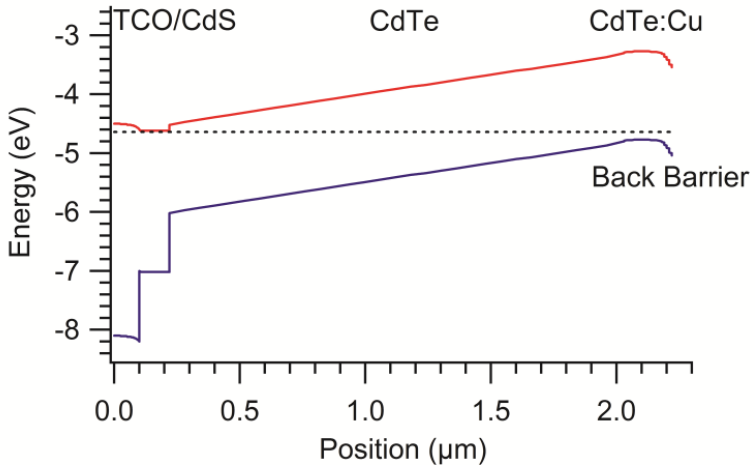


Figure 21: A band diagram of a CdS/CdTe with a low work function back contact and copper doping. Back barrier is an approximation (not to scale).

Copper dopes the back of the CdTe, which lowers and narrows the depletion width of the opposing diode, reducing the barrier effects. Figure 22 and Table 2 show a CdS/CdTe cell with and without any intentional copper doping. Copper has been shown to diffuse into the CdTe doping the bulk of the absorber layer, however too much copper diffusion can cause meta-stabilities in performance issues (56; 57; 58). The influence and mobility of copper has been and continues to be a topic of study and controversy.

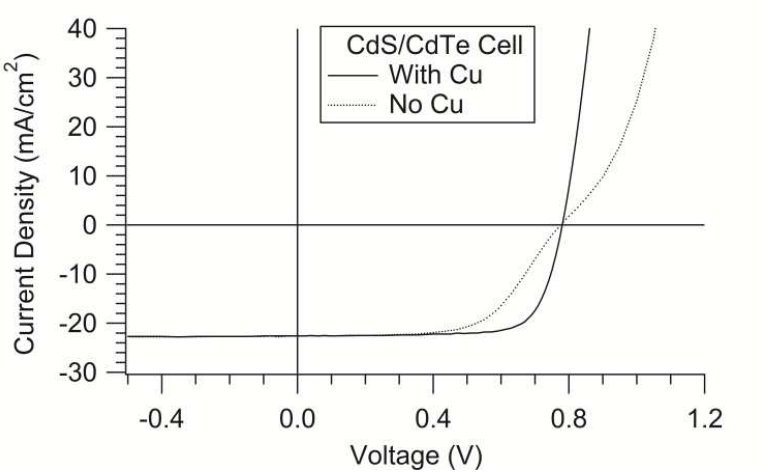


Figure 22: Current density verse voltage curves of a baseline CdS/CdTe cells.

Table 2: Figure 22 Performance Parameters

Structure	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
With Cu	780	22.6	75.2	13.3
No Cu	776	22.6	60.5	10.6

2.1.3.4. Back Contact

Carbon paint is used to contact the baseline CdS/CdTe device. The Carbon paint is purchased from Henkel (Loctite), identified as DAG 1098. It is carbon suspended in MEK with an acrylic binder. The as-purchased carbon paint is diluted with MEK at a 1:4 carbon paint to MEK ratio. It is deposited using a commercially available spray gun at 30psi in one pass making a 20-µm carbon paint layer.

Cells are finished with a nickel paint layer for a thicker, lower resistance electrode to minimize lateral series resistance. The paint also provides a mechanically robust cover for the cell as it is transferred and numerous measurements are taken. It is purchased from Henkel (Loctite) and is identified as EDAG 440AS. It is diluted with MEK at a 1:1 ratio with MEK. It is spray deposited in 3 thin coats for a 50 µm layer.

To form small area devices (SAD) of approximately 0.6 cm^2 the excess CdTe material is removed using urea blasting media (40-60 mesh, Kramer Industries). This process uses a 60 psi syphon type bead blaster and a stainless steel mask to protect the active CdTe area. To improve contacting the front contact (TCO), indium is soldered around the CdTe cell.

2.1.4. Repeatability and Performance

2.1.4.1. Repeatability

CdS/CdTe baseline cells have been fabricated over the past 36 months utilizing nearly identical process parameters to maintain a baseline performance standard of the tool. Between 27 and 54 CdS/CdTe small area devices have been manufactured in a day consistently over those 36 months. Figure 23 shows the average performance and a standard deviation for each sample set of cells over the past 3 years.

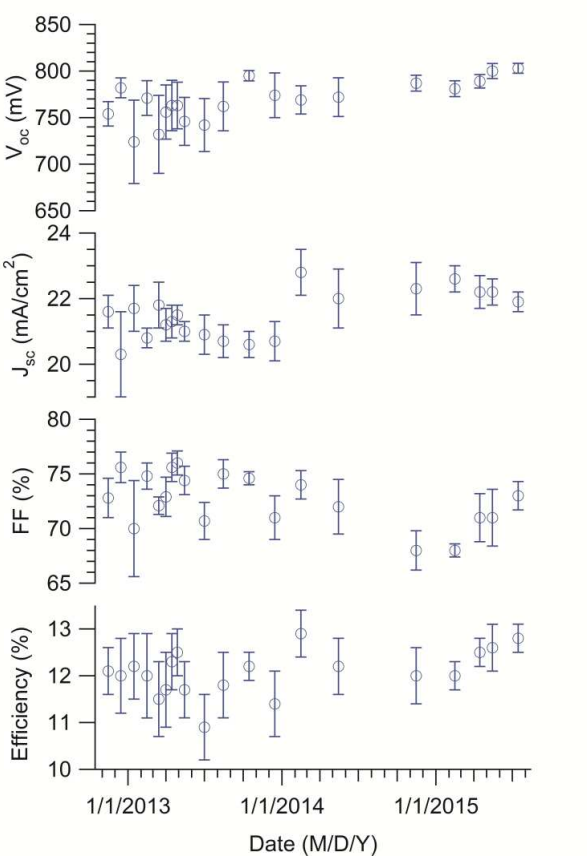


Figure 23: The average performance (± a standard deviation) for each sample set over the past 3 years.

Figure 23 shows a fairly consistent capability to manufacture a baseline CdTe solar cell. There is a reduction in spread over the past 36 months which is attributed to minimizing the time the chamber sits at atmosphere by changing weekly preventative maintenance to a bi-weekly schedule and only adding CdS and CdTe source material when the 240gram material load drops below 50% which is approximately monthly. Table 3 gives the overall average and a standard deviation of each of the performance parameters over the 36 months. This statistically significant data set gives users of the tool the ability to confidently conduct statistically relevant scientific studies.

Table 3. Average JV performance over 36 months.

V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
762 ± 23	21.3 ± 0.6	73 ± 2	12 ± 0.6

2.1.4.2. Enabled Research

The development of this chamber and process has allowed for various studies to be conducted with an over 20,000 SAD's having been manufactured to date. Fundamental characterization of $CdCl_2$ passivation, copper doping, increased CdTe deposition temperatures, and the post-annealing of CdTe cells have been studied to develop a deeper understanding of the fundamental physics (55; 59; 60; 61; 62).

To improve cell performance, novel front contacts have been developed using various TCO and buffer layers to improve current collection and band alignment (45; 63; 64). Back contacts were studied using MoO_3, MoO_xN_y, and tellurium to reduce barriers to hole collection (65). It has also enabled the development of an electron reflection concept for CdTe using a $Cd_{1-x}Mg_xTe$ layer to improve minority carrier lifetime (47; 28).

Advanced PV characterization techniques have been developed including electroluminescence (EL) and light-beam-induced-current (LBIC) (66; 67; 68; 69). These uniformity measurements have increased the characterization capabilities and improved the understanding of the technology. All of this work has been possible due to the reliable and high output cell manufacturing of this single-vacuum CSS chamber. It has allowed for almost every part of the CdTe cell to be studied and has enabled the development of a next generation high efficiency cell structure.

An example of efficiency improving enabled research is in the next generation cell structure that uses an MZO (Magnesium Zinc Oxide) buffer layer as an alternative to the CdS

layer (45). This is deposited in a separate RF sputter deposition chamber, where the film is deposited onto TEC10 glass, replacing the SnO_2 buffer layer in TEC12D and the CdS window layer. This tool has allowed for the direct comparison of MZO devices with CdS devices which are fabricated the same day. Highlighting the flexibility of the CSS chamber as no retooling was required. This new MZO layer has been optimized to improve transmission below 500 nm thereby improving current as well as an improved band alignment for improved voltage (45). As shown in Table 4, this next generation cell structure resulted in an absolute increase in efficiency of ~3% without an AR coating. This was the direct result of research facilitated by the development of this system and demonstrates its capability.

Table 4: Enabled research resulting in high efficiency cells

Structure	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
CdS/CdTe	799	22.9	73.6	13.5
MZO/CdTe (45)	832	25.5	77.6	16.5
MZO/HT CdTe (70)	863	26.8	79.2	18.3

2.1.5. Conclusions

This Section has outlined the development of a single vacuum CSS deposition system and process for the manufacturing of CdTe solar cells. By utilizing manufacturing technologies with proven scalability, advancement in CdTe can be made and transferred to large scale manufacturing. This hardware and process has been optimized to make over 13% efficient CdS/CdTe cells with documented performance over the past 36 months. It is capable of manufacturing approximately 250 SAD's over 10 substrates within a single work day allowing statistical experiments to be performed and has enabled the development of next generation cells

with efficiencies over 16%. By retaining the scalability of the technology but increasing the versatility of manufacturing, this developed R&D tool and process has allowed for continued success of the transfer of efficiency improving technologies to large scale manufacturing processes.

2.2. Tellurium Back Contact

Section 2.2 is based on work with co-authors Jason M. Kephart, Andrew Moore, Jennifer A. Drayton, and W.S. Sampath. I'm thankful for funding support from NSF I/UCRC, DOE FPACE I & II, NSF AIR, and assistance from Amit Munshi, Tushar Shimpi, Russell Geisthardt, John Raguse, Marina D'Ambrosio, Christina. Moffett, Carrey. Reich, Kurt Barth, Kevan Cameron, and Lauren Swanson.

The CdTe technology currently uses a hetero-junction design allowing for ideal band alignment engineering. Tellurium has been studied as a possible back contact to CdTe and compared directly to carbon paint contacts used at CSU. The comparison of the two contacts was performed by assessing changes in J-V performance, C-V profiles, and accelerated life testing of the two contacts. As well as developing band diagrams from temperature dependent JV measurements and modeling to explain the change in the proposed barriers developed for the different contacts and how copper is used to mitigate different effects.

2.2.1. Back Contact Introduction

The growing PV market requires technologies that utilize economic large scale manufacturing with high device efficiency. Cadmium Telluride (CdTe) has been expanding in the US PV market because of an ideal band gap for the Shockley-Queisser limit and a large

absorption coefficient that allows nearly complete absorption at 1 μm (39). Companies such as First Solar Inc. have demonstrated the ability to manufacture CdTe thin film solar cells at record low PV energy distribution costs of 0.038 $/kWhr and have developed small area CdTe cells with efficiencies up to 21.5% (34; 17).

The development of high quality contacts is essential to improving cell performance and stability in order to increase further market penetration of the technology (58). The back contact has been a source of uncertainty and instability in the CdTe technology (58; 56). Tellurium has been proposed to make a passivated, low barrier back contact in CdTe (71). This is generally achieved through an etching process of the CdTe absorber leaving a tellurium rich layer (72; 73), however tellurium can be deposited directly as well (74; 75).

In this work a tellurium layer is evaporated and compared to a well characterized laboratory standard carbon paint back contact (38). The tellurium is deposited at various thicknesses showing the change in cell performance and stability of the contact. The two contacts are compared directly with proposed band diagrams, and J-V modeling is used to explain the tellurium contact properties.

2.2.2. Materials and Methods

The CdTe solar cells manufactured at CSU utilize a fully-automated, single vacuum deposition chamber with integrated close space sublimation sources. The well characterized and statistically reproducible baseline structure is shown in Figure 24 left. An explanation of the hardware and processing details for the CdS, CdTe, $CdCl_2$, copper doping, back contacting layers, and cell fabrication are described in detail in Section 2.1. (38).

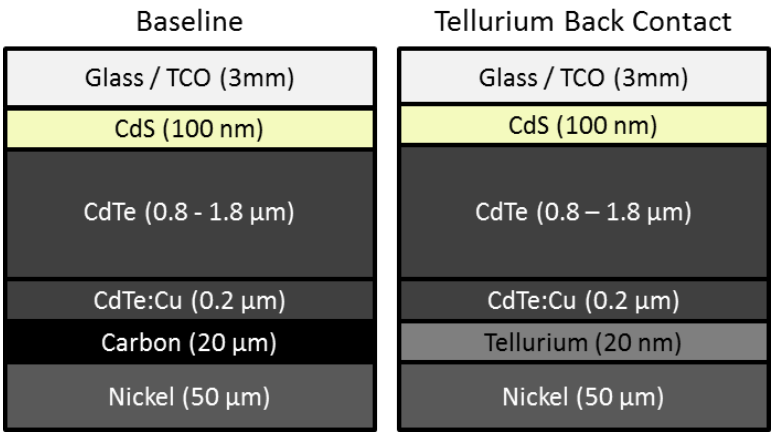


Figure 24: Baseline CdS/CdTe cell manufactured at CSU (Left) CSU baseline cell with a tellurium back contact (Right)

To better assess the quality of the back contacts, a thinner 1.0-µm CdTe thickness is used compared to the standard process (38). It has been theorized that by reducing the CdTe thickness and bringing the back interface towards the carrier generation region negative effects to performance can be accentuated (47). The CdTe thickness is controlled by changing the sublimation source temperature resulting in a lower vapor pressure and thus a reduced growth rate. A two-minute deposition time is maintained for all CdTe deposition regardless of thickness. After the cell is copper doped the tellurium layer is deposited at room temperature using evaporation. It is deposited at 10^{-5} Torr in an environment that is flushed with argon to minimize oxygen. The material is held and heated in a tungsten boat. The thickness and deposition rate is measured using a R. D. Mathis quartz crystal monitor. The deposition rate is held constant at 1 nm/s and time is used to vary thickness. Figure 25 shows a cross section TEM and EDS map of a device with the evaporated tellurium back contact.

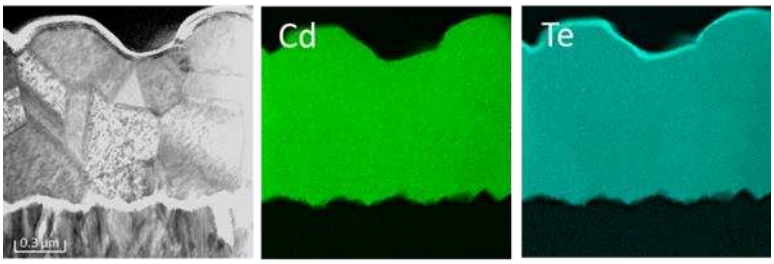
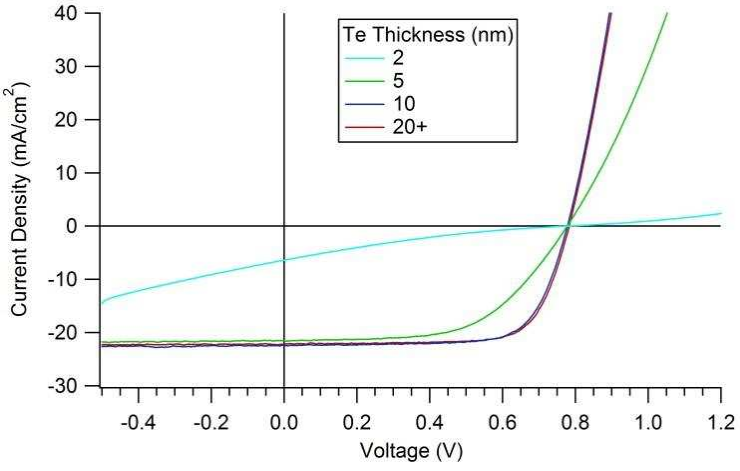


Figure 25: Cross section TEM and EDS of a 50-nm tellurium back contact, showing uniform and conformal coverage of the tellurium.

2.2.3. Tellurium Back Contact Results

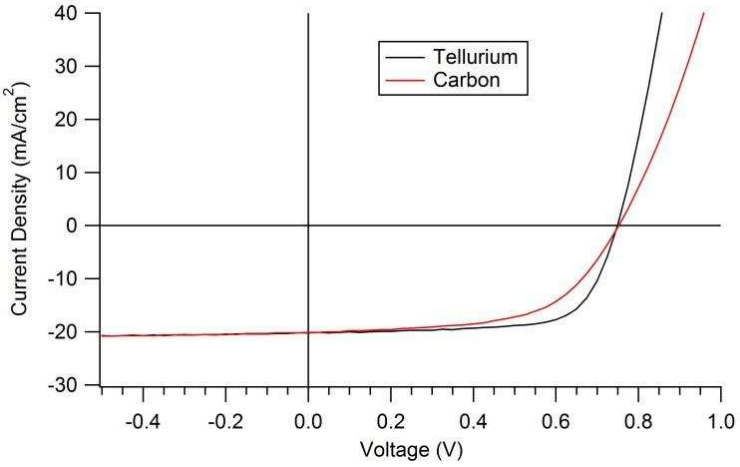
Figure 26 compares experimental J-V curves for CdS/CdTe cells with varying tellurium thicknesses at the back. Below 10 nm there is a significant reduction in the efficiency (η), fill factor (FF), and short circuit current density (J_{sc}) of the cell. This is attributed to an insignificant amount of the tellurium present to get complete coverage or obtain its bulk properties. This is in agreement with work that shows the thicknesses of the tellurium will substantially change the electronic effects up to 10 nm (73).



Tellurium Thickness [nm]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
2	778	6.4	18.2	0.9
5	778	21.5	57	9.5
10	778	22.4	71.8	12.5
20+	783	22.1	73.5	12.7

Figure 26: J-V of CdS/CdTe cells with various tellurium thicknesses, assessing the electronic changes as the tellurium layer thickness is increased.

Figure 27 gives a direct comparison of a 1-µm CdS/CdTe cells made on the same substrate with the two different back contacts. One side of the substrate was completed with tellurium and the other is completed with a carbon paint back contact (38). The tellurium contact shows an improvement in FF with little difference in V_{oc} and J_{sc}. All cells were finished with a nickel paint layer for a thicker, lower resistance electrode to minimize lateral series resistance.



Back Contact	V_{oc} [mV]	FF [%]	J_{sc} [mA/cm^2]	η [%]:
Tellurium	749	70.4	20.2	10.6
Carbon	753	58.6	20.1	8.9

Figure 27: J-V of a CdS/CdTe baseline device with tellurium vs carbon back contacts

Figure 28 shows room temperature capacitance vs frequency (C-F) curves for the devices shown in Figure 27, comparing the two back contacts. The C-F is measured at 4 different biases: -2.0, -1.0, 0.0, and 0.2, to change the depletion width of the cell. The carbon back contact shows significantly more dispersion at all biases, indicative of a cell with a greatly increased unfavorable defect density.

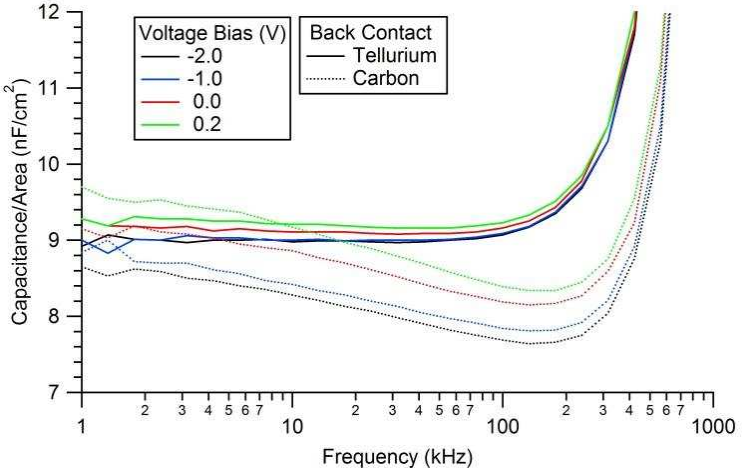


Figure 28: C-F of a CdS/CdTe baseline cells with tellurium vs carbon back contacts, showing a significant improvement in dispersion with the tellurium back contact.

Figure 29 shows the room temperature capacitance vs voltage (C-V) of the same devices from Figure 27. With the substitution of tellurium for carbon there is a slight increase in doping as seen by the increase in the belly of the curve (76). In addition there is also a much steeper transition at the back contact, indicative of a higher quality back contact (77).

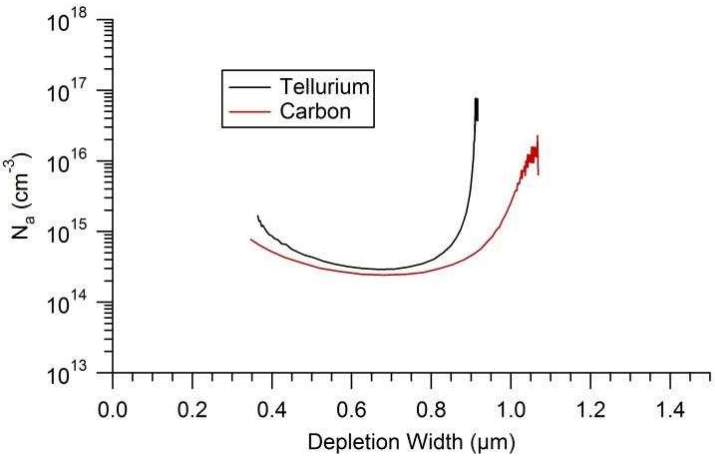


Figure 29: C-V of a CdS/CdTe cells with tellurium vs carbon back contacts

Temperature-dependent-current vs voltage measurements (J-V-T) data for the 1-μm CdS/CdTe cells with both back contacts are presented in Figure 30. As the temperature is reduced from 25 to -75^{o} C, the diode behavior changes significantly, as the contact barrier has a progressively larger impact on carrier transport with decreasing temperature. At these lower temperatures there is a major degradation of fill factor with the carbon back contact as seen in Figure 30a. However when the carbon is replaced with tellurium the FF remains constant to lower temperatures, but eventually roll-over develops at the lowest temperature forming a barrier. However, this implies a different barrier is formed with the tellurium compared to the carbon. These behaviors are similar to those seen in 2-μm CdS/CdTe cells.

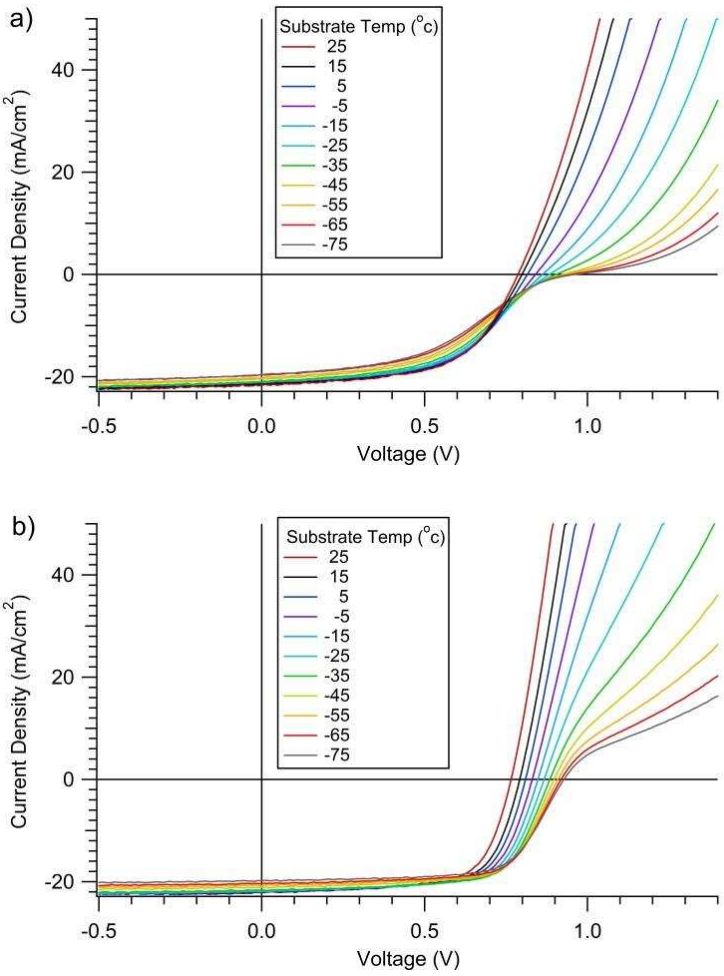
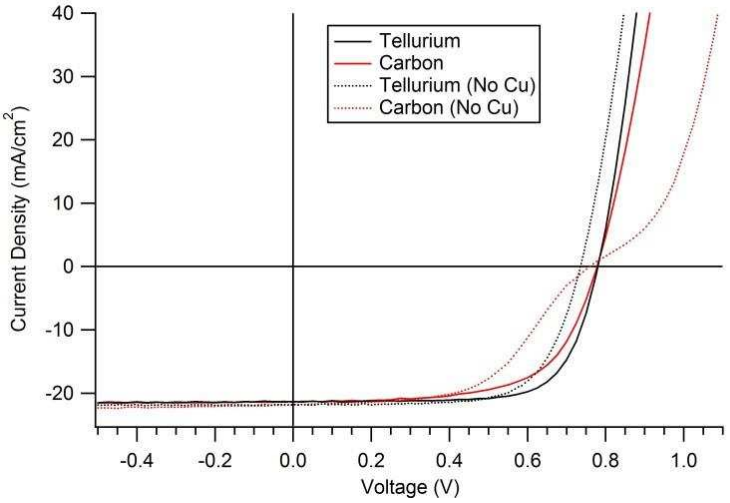


Figure 30: J-V-T of a CdS/CdTe cells with a) carbon paint and b) tellurium.

Figure 31 shows J-V of CdS/CdTe cells with both back contacts, with and without the copper doping process. The tellurium back contact without intentional copper shows less FF reduction, but a larger reduction in V_{oc}. The two materials appear to be forming different junctions with the CdTe. Copper doping, however, improves the J-V performance of both contacts.



Back Contact	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
Tellurium	781	21.3	72.0	12.0
Carbon	779	21.4	63.2	10.5
Tellurium (No Cu)	737	21.8	68.8	11.1
Carbon (No Cu)	759	21.8	53.5	8.9

Figure 31: JV of a CdS/CdTe with tellurium and carbon back contacts, each with and without copper doping.

2.2.4. Discussion

2.2.4.1. Band Diagrams

This large reduction in FF with the carbon back contact is associated with a barrier to reverse current. It is unlikely that CdS forms a conduction band barrier to reverse current at the front of CdS/CdTe cells (63). Thus it is more likely that the carbon paint maintains the large valance band offset (VBO) at the back of the cell opposing the flow of holes, as depicted in Figure 32. The carbon paint electronically relies on the copper doping at the back to keep the formation of a VBO low. This VBO is formed due to the low work function of the carbon compared to the CdTe. As the temperature is reduced the holes in the reverse current direction lack enough energy to overcome the VBO barrier and reduce the cells ability to collect current, leading to the reduction in FF seen in Figure 30a.

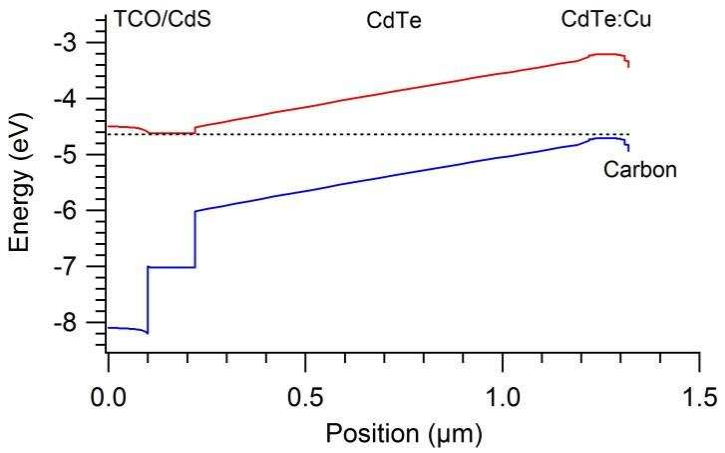


Figure 32: Band diagram of a CdS/CdTe cell with a carbon back contact, showing the formation of a VBO with the low work function back contact.

Figure 30 indicates that the tellurium forms a different interface with CdTe. As holes are injected into the CdTe in the forward direction the holes are unable to overcome that barrier as the thermal energy is reduced. In both cases, at lower temperatures more of a voltage bias is required to achieve the same forward current but the effect is significantly reduced with the tellurium layer. Figure 33 shows the proposed change in the band diagram as the tellurium is used instead of the carbon paint. Due to the small band gap of tellurium and its low electron affinity, the Fermi level is likely pinned forming a forward current barrier (71). The barrier formed using tellurium as the back contact is in the opposite direction compared to the carbon paint.

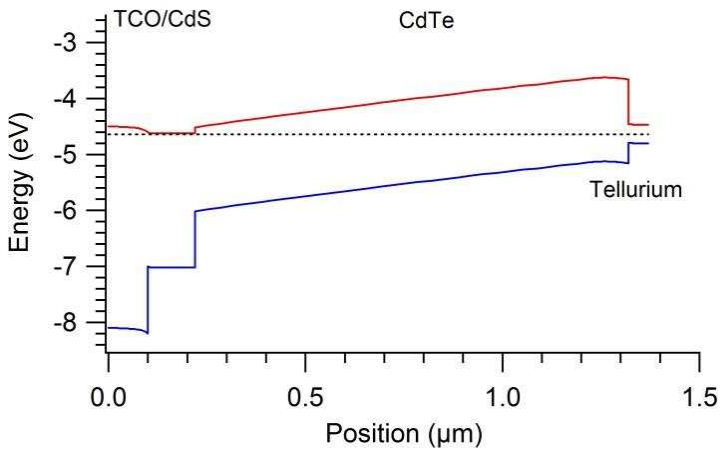


Figure 33: Band diagram of a CdS/CdTe cells with a tellurium back contact, the barrier is formed in the opposite direction of the carbon back contact cell.

This forward current barrier is a result of a low electron affinity of the tellurium. This results in the removal of the VBO seen in the carbon back contact (Figure 32) and thus improves the FF in the no copper tellurium cell. However the Fermi level is pinned higher, lowering the V_{oc} as shown in Figure 31 and Figure 33. To recover this V_{oc} loss with tellurium, copper is used to dope the back of the CdTe and pin the Fermi lower. This improves the V_{oc} and develops a small VBO. Figure 34 shows the theoretical band diagram of a tellurium back contact with copper doping. This makes a low barrier back contact that does not impede reverse current but is still dependent on copper similar to the carbon paint, however for different reasons.

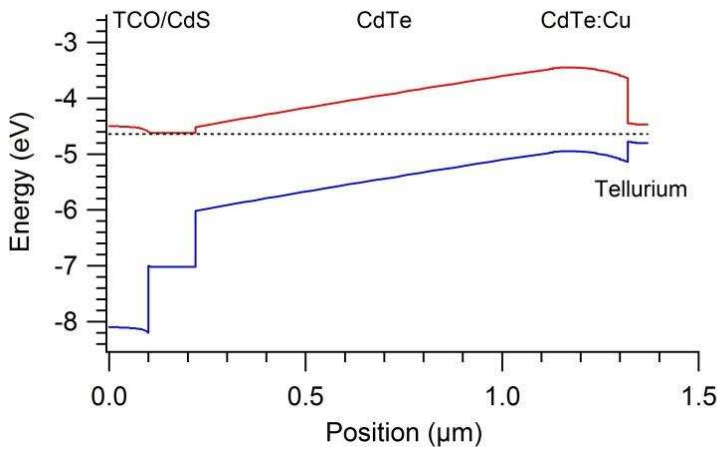


Figure 34: Band diagram of a CdS/CdTe cells with a tellurium back contact with copper doping, the increased carrier concentration at the back reduces the voltage loss.

2.2.4.2. Accelerated Life Testing

Figure 35 shows accelerated life (ALT) testing at 85^{o}C for almost 1000 hours under open-circuit bias for the copper doped carbon and tellurium back contacts. The carbon back contact shows a significant degradation in the FF over the 1000 hours, likely associated with the migration of copper from the back contact and leaving a low work function back contact. Figure 35b shows the same ALT but with the tellurium contact, there is no significant change in FF but a larger loss in voltage. As the cells are stresses in ALT the cells performance shifts towards the no intentional copper condition. This is in agreement with the migration of copper that is typically seen during ALT (56). It has also been hypothesized that tellurium may react with oxygen and under ALT conditions a tellurium oxide may form, further material characterization is required.

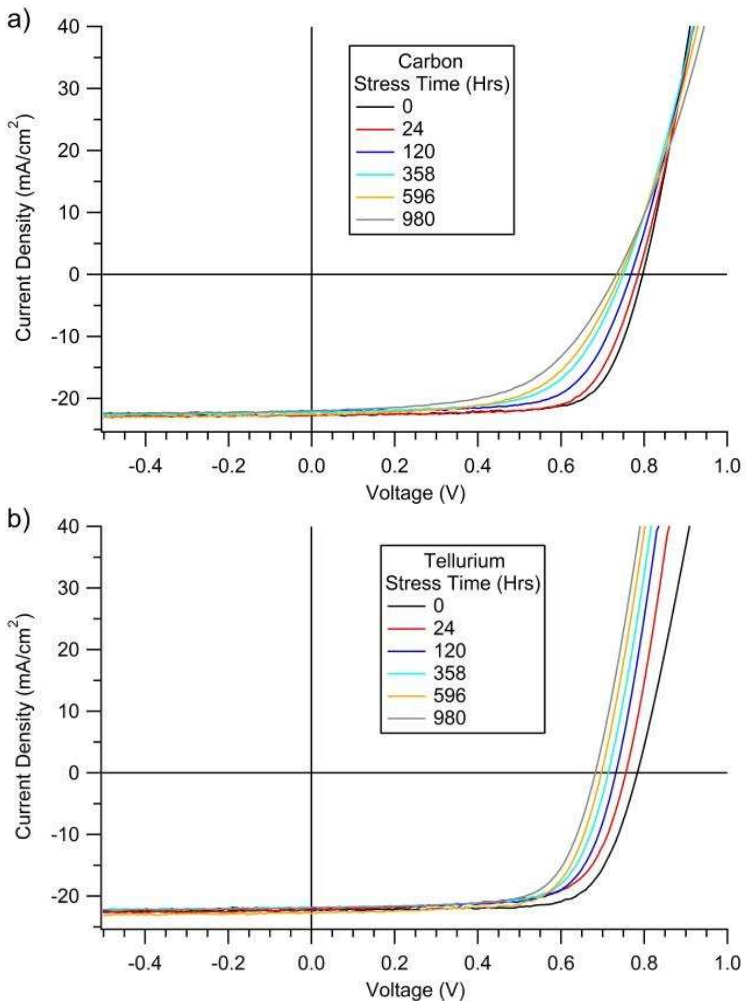


Figure 35: Accelerated Life Testing of CdS/CdTe cell with a) carbon and b) tellurium back contacts (with copper doping).

The migration of copper doping away from the back contact causes a reduction in the doping at the CdTe/Te interface as modeled in Figure 36. This model uses the same parameters as previous work (27; 28). Figure 36 uses the same band diagram from Figure 34 but the doping concentration is varied to simulate the migration of copper from the back. With a reduction in back contact doping, the model (Figure 36) shows a similar trend to the experimental ALT (Figure 35b). Similar to Figure 35 there is a constant FF and J_{sc} but a decreasing V_{oc}. The copper doping was used to help pin the Fermi closer to the valance band at the CdTe/Te interface

(Figure 34), but as the copper migrates due to ALT the doping is reduced at the back and the bands shift back to Figure 33 and the voltage is reduced. This is in agreement with previous copper migration work.

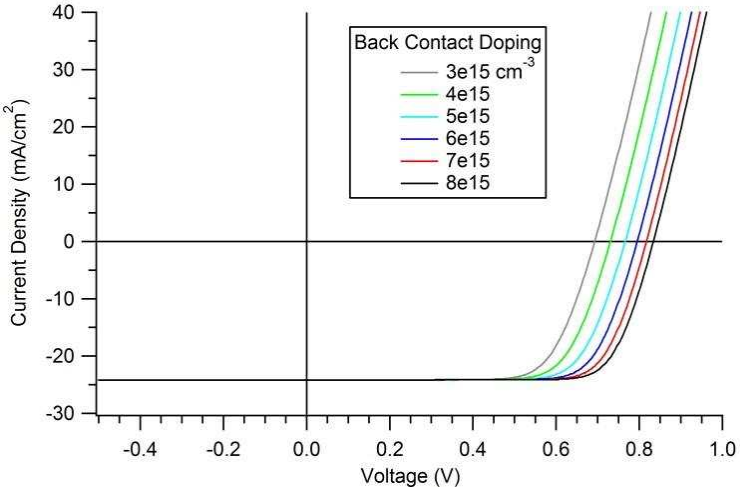


Figure 36: Modeled J-V performance of CdS/CdTe/Telluride cell with various back contact doping (emulating copper migration in ALT)

2.2.5. Tellurium Back Contact Conclusions

Tellurium has been compared directly with carbon paint as a back contact in CdTe cells. Both contacts without intentional copper doping appear to develop barriers, however through different mechanisms. J-V-T measurements have shown the carbon back contact develops a VBO blocking the flow of reverse current out of the cell. It is theorized that the tellurium back contact pins the Fermi level above the valance band developing a forward current barrier from injected holes. Both contacts rely on copper doping to mitigate the corresponding negative effects of the barriers. The VBO causes FF reduction with carbon contacting and the tellurium's low electron affinity causes V_{oc} loss. This is in agreement with ALT of the contacts, as the copper migrates away from the back contact the cells approach there no copper conditions. As the back contact doping density is reduced the V_{oc} decreases, thus showing agreement between

modeling and the experimental results. Both contacts appear dependent on copper for optimal performance but the change in barrier formation of the tellurium back contact may prove ideal for VBO prone back contacts such as $Cd_{1-x}Mg_xTe$, this is discussed in detail in Section 3.

3. $Cd_{1-x}Mg_xTe$

3.1. Type A CdMgTe Electron Reflector

In Section 1.3 a Type A ER structure was theorized to improve cell performance by increasing the conduction band offset. This was achieved by adding a high band gap material. To keep the offset in the conduction band, the material needs a low electron affinity and it is preferred that this material have a similar lattice constant to limit defect growth at the interface as shown critical in III-V materials (78; 79). Two potential group II elements to use are zinc and magnesium, both replacing the cadmium cation forming $Cd_{1-x}Mg_xTe$ and $Cd_{1-x}Zn_xTe$. Each material has advantages and disadvantages over the other. The CMT layer has a more closely matched lattice constant to CdTe as shown in Figure 37, however CZT has a lower electron affinity which would minimize potential negative VBO effects. Since there is a hypothesized significant dependence on interface quality and there has been passivation of CMT in literature (80; 81; 48), CMT was the material studied.

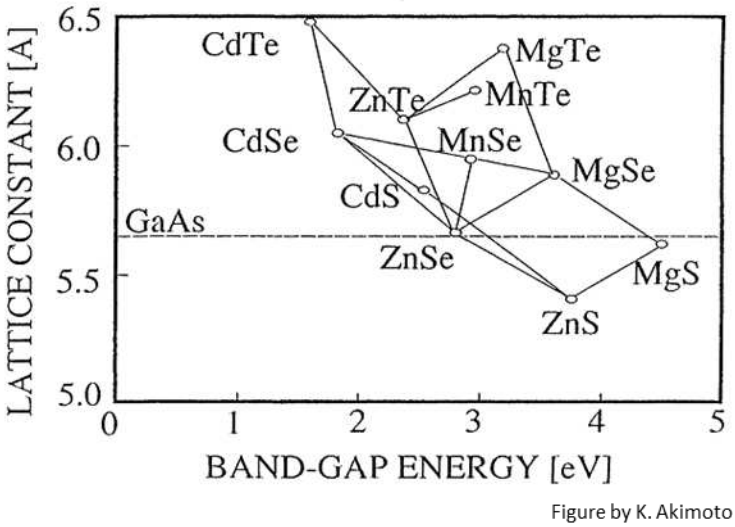


Figure 37: Lattice Constant vs Band-Gap (28)

The modeled ideal Type A ER structure would have a barrier only in the conduction band to repel the minority carriers away from the back (82). The formation of a valance band offset at the back of this device would repel holes and reduce the power generation of the cell. This would cause a decrease in performance as demonstrated in the predicted JV in Figure 39 of the four structures proposed in Figure 38.

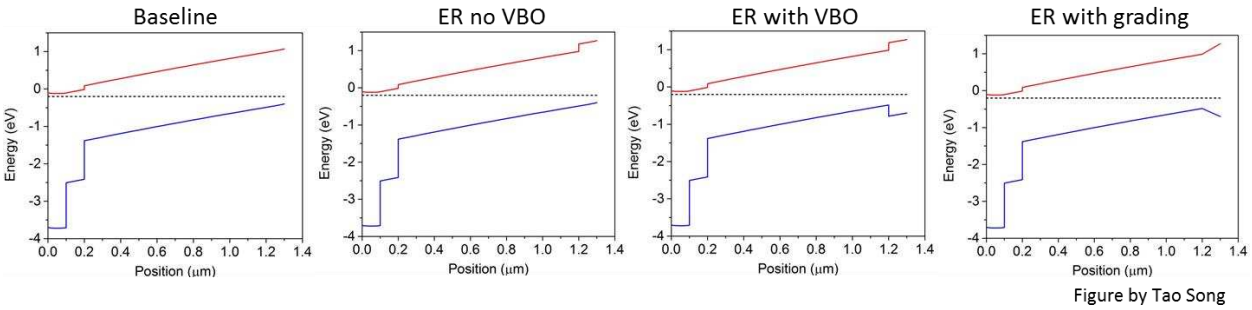
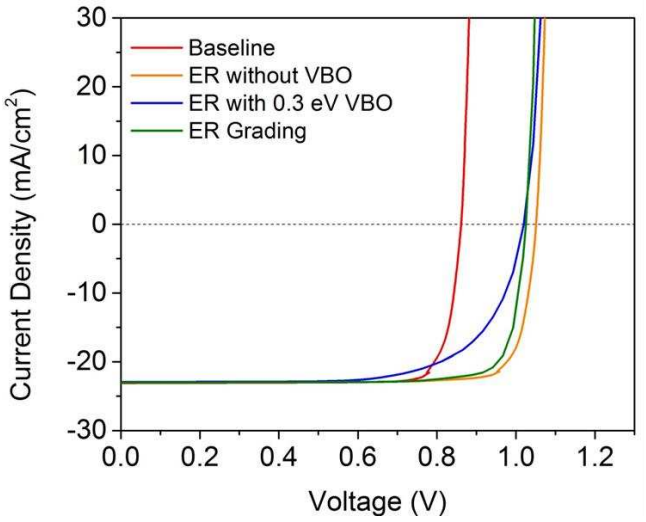


Figure 38: CMT Band diagrams a) Baseline, b) ER no VBO, c) ER with 0.3eV VBO, ER with graded 0.3eV VBO (82)

The loss in performance from a 0.3eV VBO is in FF. Even with the formation of a substantial VBO of 0.3eV there is a V_{oc} increase of ~200mV. This is in agreement with the HIT cell results. In the HIT cell technology the formation of a VBO primarily affects FF (83; 84). To elevate this loss in FF from the VBO is has been proposed to grade the barrier. It is theorized an abrupt VBO leads to more hole recombination current, resulting in more forward current and thus FF is reduced, a graded VBO can mitigate the hole recombination at the CdTe/CMT interface at forward bias and thus benefit FF (82).



Cell Structure	$V_{oc}(mV)$	$J_{sc}(mA/cm^2)$	FF (%)	η (%)
Baseline	860	23.1	85.2	17.0
ER, no VBO	1050	23.0	85.2	20.6
ER with 0.3 eV VBO	1020	22.9	69.2	16.2
ER grading	1030	23.0	83.7	19.7

Figure by Tao Song

Figure 39: Modeled JV performance for the various CMT cell structures

The ER structure operates on the premise that the electrons are diffusing to the back interface, if the cell is heavily doped or significantly thick the cell is not fully depleted. The built-in electric field in the depletion region (drift field) is used to collect generated carriers and reduce bulk recombination. A fully depletion cell occurs when the drift field spans the entire thickness of the cell. Thus in a non-fully depleted cell the generated electron current will not reach the back of the cell to be reflected and instead will recombine in the CdTe, this is demonstrated in Figure 40. Note, as the cell is put into forward bias the depletion width narrows, thus a cell may be fully depleted at open circuit condition but not when under forward bias. To promote full depletion the CdTe absorber must either be very poorly doped or the CdTe thickness must be reduced.

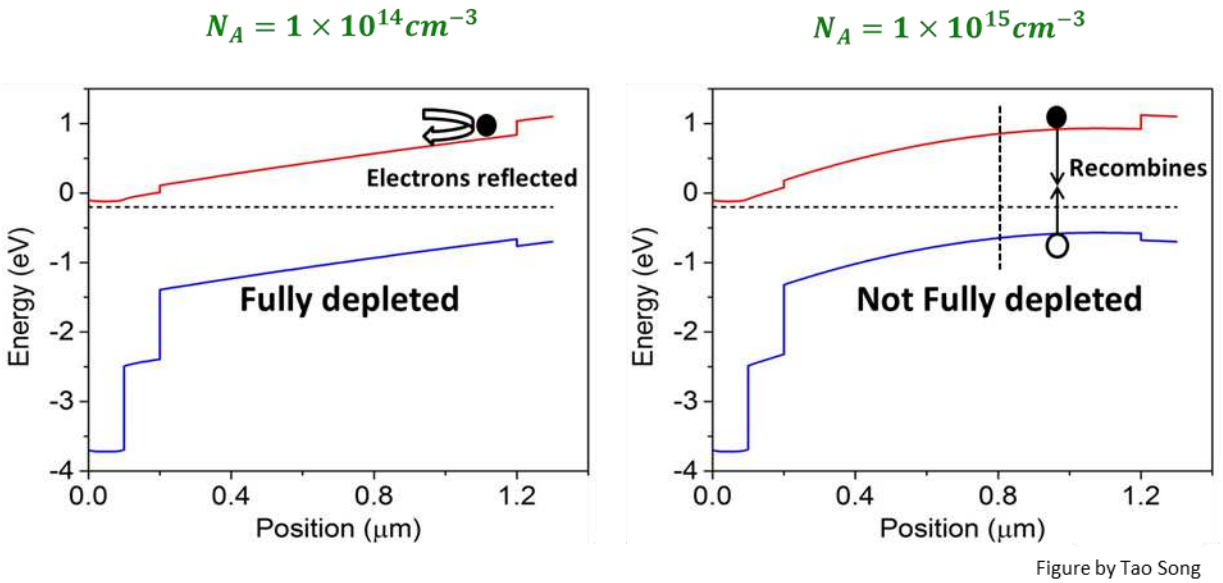


Figure 40: Depleted vs Not Depleted CdTe with Type A CMT ER

Figure 41 shows the connection between CdTe thickness and the doping density of CdTe in respect to V_{oc} changes in a Type A ER structure using CMT. Typical doping density of CdTe is ~$2*10^{14}$ cm^{-3} (46), there has not been a significant development in CdTe doping technology making it difficult to use carrier concentration as the controlling parameter. At this carrier concentration it is modeled that moving towards full depletion by thinning the CdTe down to ~0.5μm would increase V_{oc} performance. Thinning CdTe is more controllable as the deposition thickness can be controlled with deposition time and temperature.

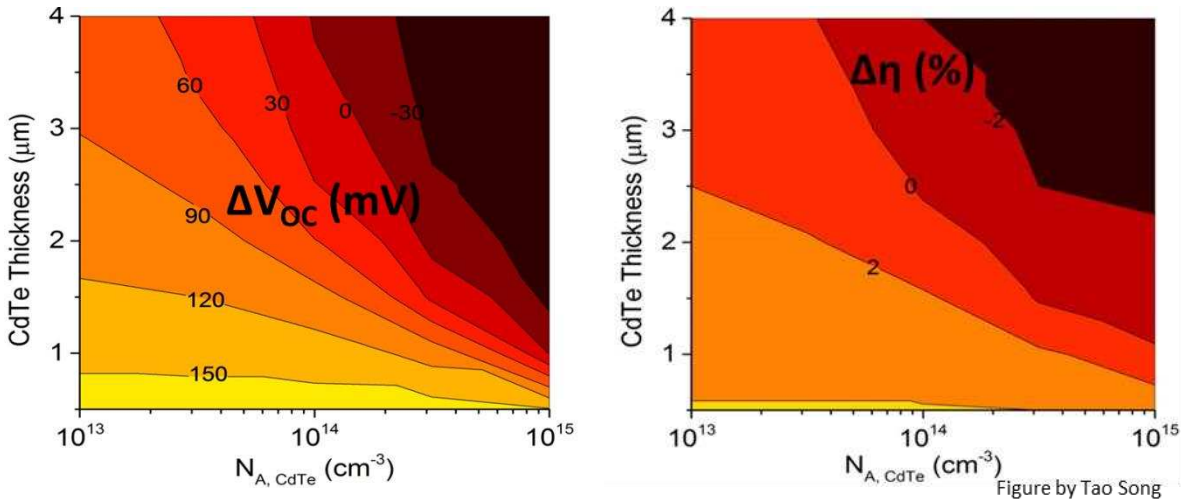


Figure 41: Modeled V_{oc} vs CdTe doping (82)

Due to the favorable lattice mismatch, the lower required alloying to achieve a higher band gap, and the published literature available on passivation, CMT was selected as the best candidate for a Type A ER structure.

3.2. CdMgTe Hardware and Manufacturing

The original source development for CMT deposition was developed by P. S. Kobyakov, who developed the source geometry identified as co-sublimation Generation I (Gen I). Gen I geometry is depicted in Figure 43 and significant characterization of the ability to controllably deposit CMT was performed (28).

The first improvement to this work was the reduction in oxygen in the chamber. The base pressure was lowered from 10^{-5} to 10^{-7} Torr by identify and fixing leaks with a helium leak detector. This lowered the partial pressure of oxygen in the chamber from 10^{-9} to 10^{-11}, or from ~0.08% to 0.0001%. Since magnesium is prone to react with oxygen, it is important to minimize the presence of oxygen during processing. Oxygen effects on performance is discussed in detail in Section 3.4.

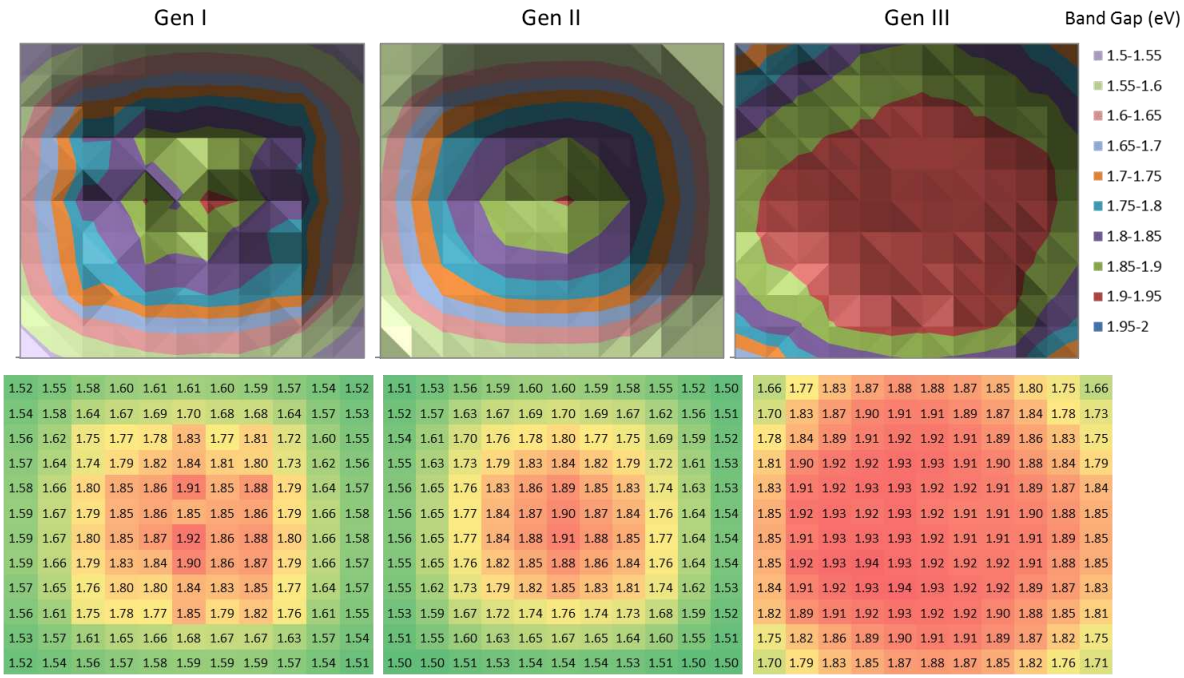


Figure 42: Co-Sublimation Source Generation I, II, and III showing band gap uniformity

The Gen I hardware had strong non-uniformities during deposition as shown in Figure 42, having a standard deviation across the substrate of 0.118 eV. With Gen II hardware the pocket depth was increased from 0.5 to 1.0 inch, this improved the central uniformity as shown in Figure 42 but the standard deviation did not significantly change (0.12 eV). In Gen III additional holes where added to allow for an increase in magnesium vapor flux across the pocket as shown in Figure 43. This improved band gap uniformity across the cell, with a standard deviation of 0.061 eV an improvement from 0.118 with Gen I.

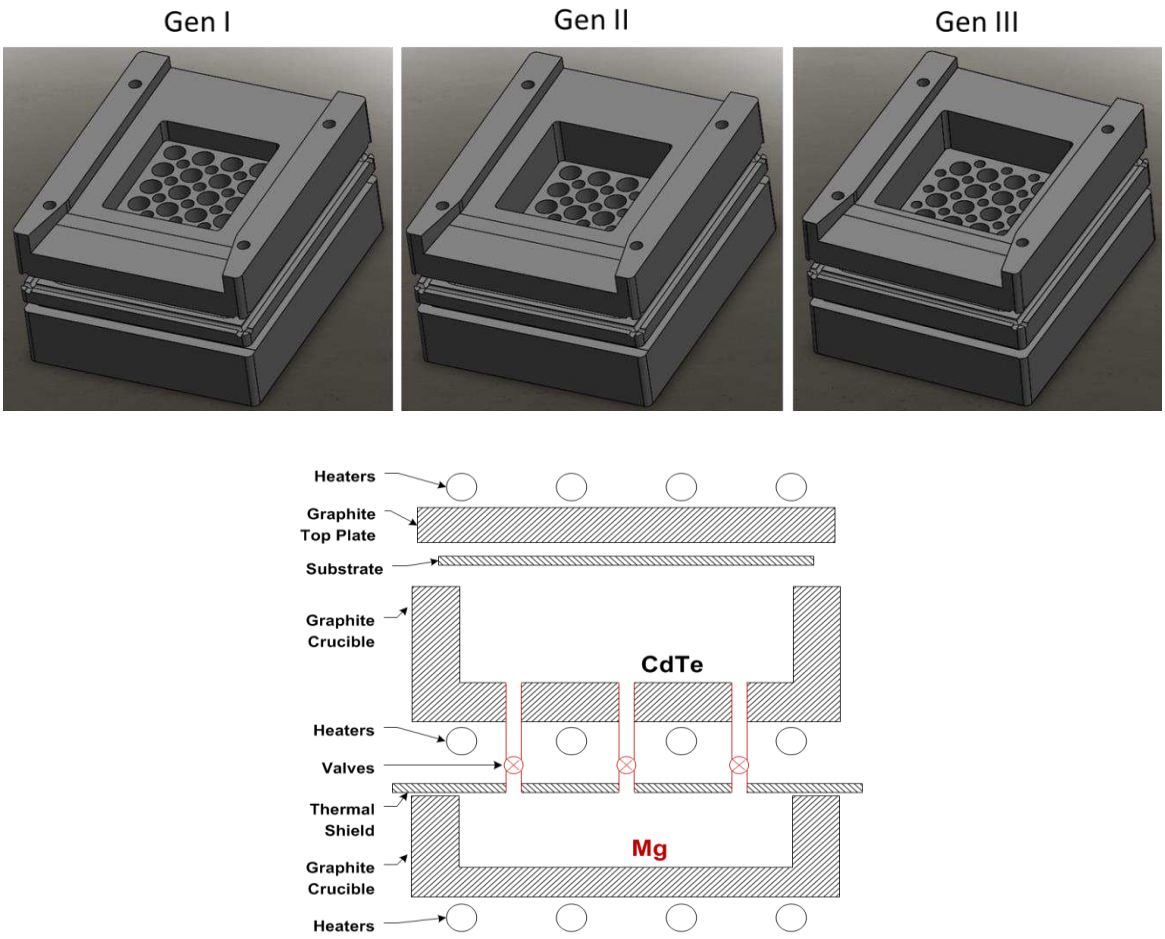


Figure 43: (top) CAD drawings of Generation I, II, and III of the CdTe Co-Sublimation Source (bottom) Schematic of Co-Sublimation Sources

3.3. Development of Type A CdTe/CdMgTe Solar Cells

The following section was published in the 40th IEEE PVSC (47), in collaboration with Russell Geisthardt, Pavel Kobyakov, John Raguse, Jennifer Drayton, Jim Sites, and W.S. Sampath. Primary funding for this work came from the Department of Energy's SunShot program (FPACE Award DE-EE0005399). Additional funding was supplied by NSF's I/UCRC and AIR programs and by NREL's NPO program. I am particularly grateful to Helio Moutino and Darius Kuciauskis at NREL for their assistance through the NPO program. I also acknowledge several colleagues at CSU, Katherine Zaunbrecher, Jason Kephart, Kevan

Cameron, Patrick McCurdy, Carey Reich, Andy Moore, Amit Munshi, Tushar Shimpi, and Lauren Swanson, for their support with the research.

The record efficiency of CdS/CdTe solar cells is lower than the theoretical Shockley-Queisser limit (34; 39). The current record cell has a V_{oc} of 876 mV (34), significantly below optimal for the 1.5 eV band gap of poly-crystalline CdTe. A detailed loss analysis of these record cells show a majority of the losses of the CdTe technology are electronic losses, primarily the low V_{oc} and reduced FF related to high diode quality factor (85). A back surface field (BSF) or electron reflector (ER) has been proposed to mitigate these electronic losses (27).

When minority carriers are able to diffuse to the back contact, back-surface recombination may become a primary mechanism for performance loss. The ER increases the collection of carriers generated near the back surface from low energy photons and it reduces forward-current loss. The result should be an increase in both voltage and current as this back surface recombination is reduced. To incorporate an electron reflector at the back contact of CdTe, a high-band-gap film has been produced (86).

Deposition of $Cd_{1-x}Mg_xTe$ (CMT) by sublimation has been developed to manufacture high-band-gap CMT films (86). CMT was chosen because its lattice constant is close to CdTe and the amount of Mg required is modest. CMT films have been shown to grow epitaxial on CdTe making it a primary candidate to reduce recombination at the back surface interface and to promote reflection of electrons towards the charged collection region (28). To minimize the quasi-neutral region, the CdTe absorber thickness was reduced. Devices were then characterized with and without the ER present.

The CdS/CdTe solar cells studied here are manufactured by sublimating films using close space sublimated (CSS) sources integrated into a single-vacuum deposition system (40; 50). The

baseline CdS/CdTe fabrication process is described in detail in Section 2.1. The passivated CdS/CdTe film stacks are then transferred to a separate chamber where the ~120 nm, 1.75 eV CMT film is deposited, reference cells are subjected to the same heat cycles without deposition (86). The CdS/CdTe/CMT film stack is then returned to the primary deposition system for a second $CdCl_2$ passivation, which is performed in a <0.01% O_2 environment to minimize Mg loss (87). A second passivation is used because at the reheat substrate temperatures of 470 ^oC during CMT deposition removes the chlorine and makes stacking faults reappear (55). Note, there is no CdTe capping layer used. The cell is then finished with Cu back contact doping. Finally acrylic carbon and nickel paint is sprayed on for a back contact and the films are mechanically abraded into ~0.60 cm^2 small-area devices as described in Section 2.1.

3.3.1. CdTe/CdMgTe Cell Results

To minimize bulk recombination and attain the optimal effect from the addition of an ER, the cell must be close to or fully depleted (27). To achieve this, a thin 1 µm CdTe absorber layer is used. Without the ER present, this layer can bring the back surface recombination into the carrier generation region of the cell. Other groups have shown that for absorbers of thickness below ~2.5 µm, and especially between ~1.2 µm to 0.5 µm, there is substantial reduction in V_{oc}, FF, and J_{sc} (88; 89). Similar results have been shown with CdTe cells at CSU, as seen in Figure 36a. This reduction in V_{oc} and J_{sc} is attributed to this back surface recombination. By adding the 100 nm CMT film to the back of the cell and inducing the ER, the V_{oc} and J_{sc} losses are significantly reduced and display a different trend in the data as shown in Figure 44b.

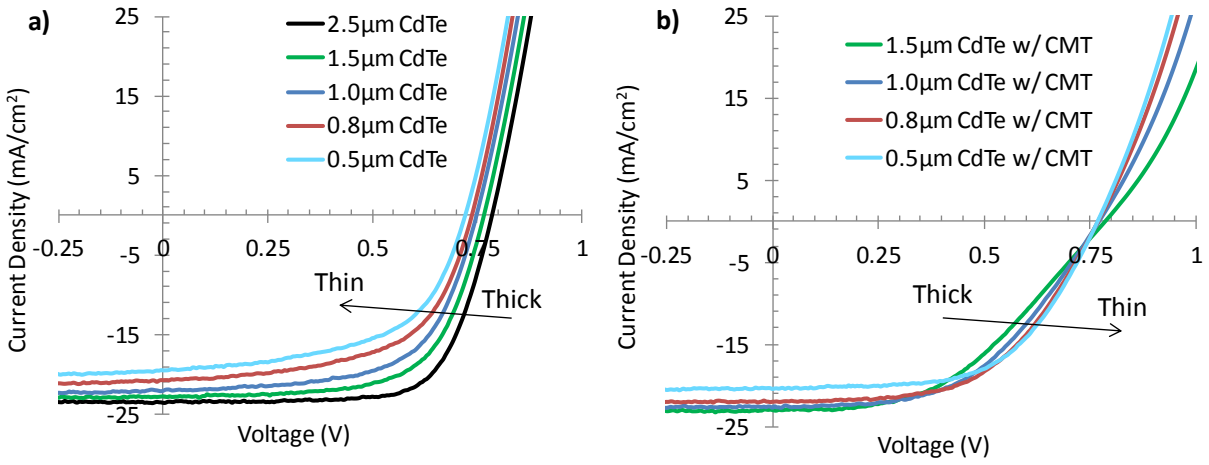


Figure 44: J-V Curves of a) CdS/CdTe and b) CdS/CdTe/CMT cells with various CdTe thicknesses

As the CdTe thickness (Figure 44a) is decreased there is, as expected, a decrease in J_{sc} with reduced optical absorption. Figure 45 depicts the quantium efficiency (QE) and associated loss mechanisms of a 0.6 µm CdTe cell. As the CdTe is reduced in thickness, there is a reduction in absorption above the CdTe band gap, but this reduction only partially accounts for the decreases seen in J_{sc}. The current losses due to non-absorption (blue region in Figure 45) and non-collection (green region in Figure 45) are calculated by integration of the respective regions weighted by the solar spectrum and are shown in Figure 45. The other photon losses are essentially independent of CdTe thickness.

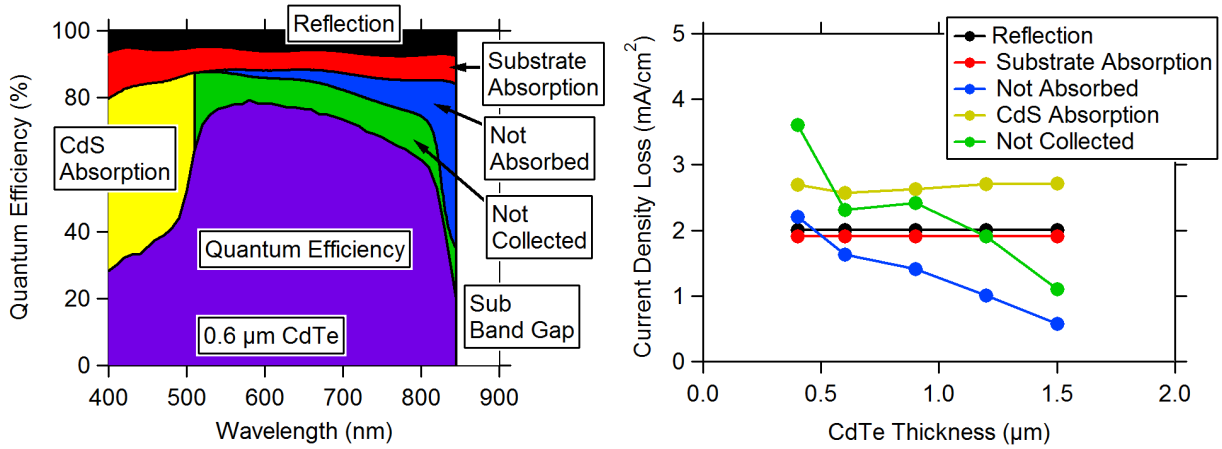


Figure 45: (left) Quantum efficiency of a 0.6 µm CdTe cell (without a CMT layer) illustrating the individual loss mechanisms, (right) Integrated current densities for each category of loss mechanism as a function of CdTe thickness

Incomplete collection of photo-generated carriers is mitigated with the presence of the CMT film, as shown in the solid and dashed QE curves of Figure 46. There is a substantial increase in current from 550 to 850 nm. The additional 120 nm higher-band-gap (1.75 eV) material cannot account for the increased current from optical absorption alone. The current increase across the spectrum is assumed to be from the reduction in carrier recombination at the back interface and is consistent with earlier modeling (90). Furthermore, as one would expect, the improvement in QE as a result of adding the CMT layer is greater at the thinner absorber conditions.

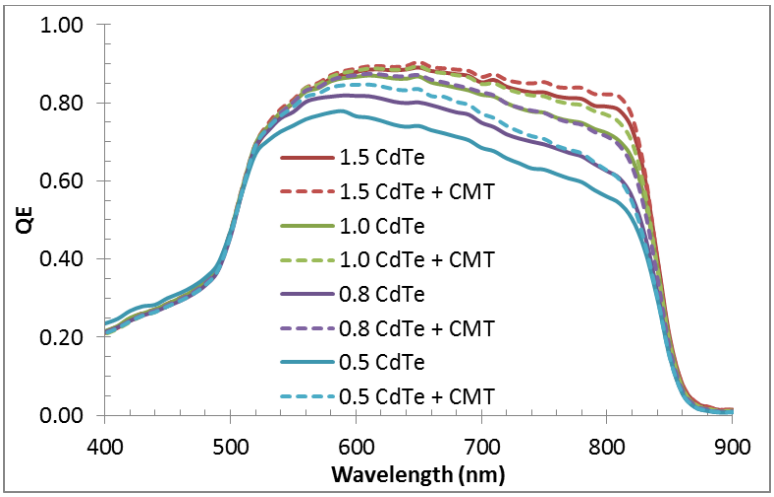


Figure 46: Quantum efficiency at various CdTe thicknesses with and without a 1.75 eV CMT layer

Figure 47 shows the measured V_{oc} and J_{sc} at various CdTe thicknesses with and without the addition of a CMT film. V_{oc} is maintained as the CdTe cell thickness is reduced with a CMT film present. The loss in J_{sc} is reduced, but as discussed below FF displays an increase. Modeling has been presented to predict and begin to account for these losses (27; 90). The overall performance of the CdTe cell becomes increasingly dependent on the extent of recombination at the CdTe/carbon back-surface interface as the CdTe thickness is reduced.

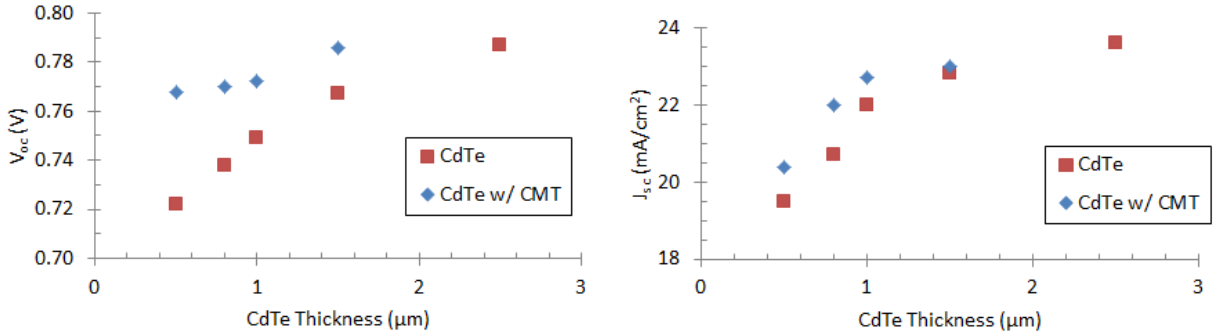


Figure 47: V_{oc} and J_{sc} of CdS/CdTe cells at various CdTe thicknesses; with (Blue Diamonds) and without (Red Squares) a 1.75 eV CMT film

The improving FF with reducing CdTe thickness is shown in Figure 48. This is thought to be associated with the reduction of the quasi-neutral region of the cell. Carriers are generated and collected more efficiently, with a reduction of bulk resistance of the CdTe material (91). This is not observed without the CMT due to the high recombination velocity of the CdTe/Carbon back contact interface.

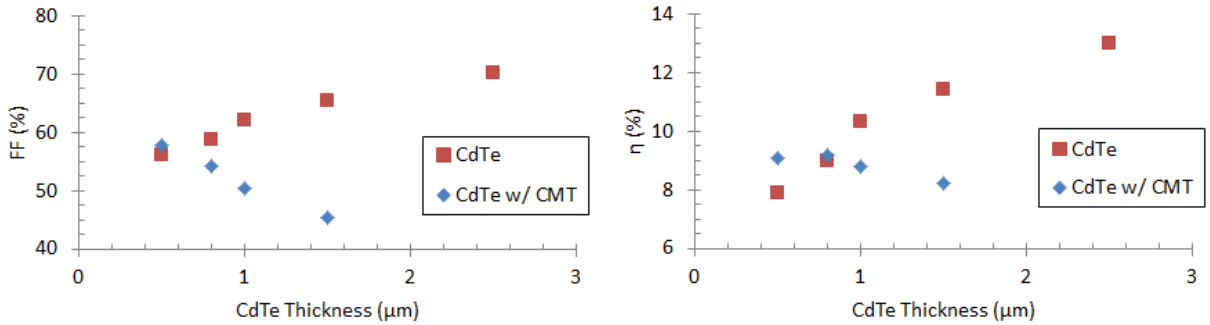


Figure 48: FF and Efficiency (η) of CdS/CdTe cells at various CdTe thicknesses; with (Blue Diamonds) and without (Red Squares) a 1.75 eV CMT film

Comparative time-resolved-photoluminescence (TRPL) (92; 93) measurements of the CdS/CdTe cells were performed with a wavelength of 760 nm thorough the glass/TCO interface. Figure 49a shows that the decay times are decreasing as the thickness of the CdTe absorber is decreased and the back interface is brought into the carrier generation region. This implies that the recombination velocity of the back surface is reducing the minority carrier lifetime, in agreement with V_{oc} and J_{sc} losses. Figure 49b shows the TRPL decay times of CdTe with a CMT film. The decay times for the thin cells are now significantly longer which suggests that the recombination at the back interface is significantly reduced.

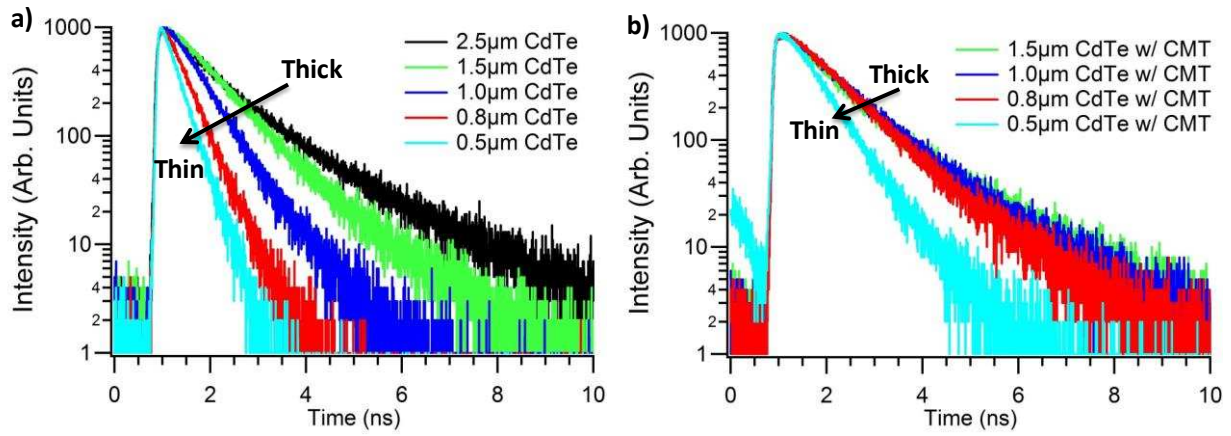


Figure 49: TRPL from a) CdS/CdTe and b) CdS/CdTe/CMT cells as a function of the CdTe absorber thickness

Additional evidence for the effectiveness of the CMT layer is provided by electron-beam-induced current (EBIC) (94; 95) measurements from cells with and without the CMT layer. Figure 50a shows the EBIC signal is relatively uniform over about half the CdTe thickness, but decreases significantly near the back interface. In contrast, Figure 50b, with the same absorber thickness of CdTe plus a CMT layer, shows uniform response throughout the CdTe, again strongly suggesting a beneficial effect from the CMT layer. The line cuts in Figure 50 quantify the EBIC information and give support to the explanation of the quantum efficiency differences seen in Figure 46.

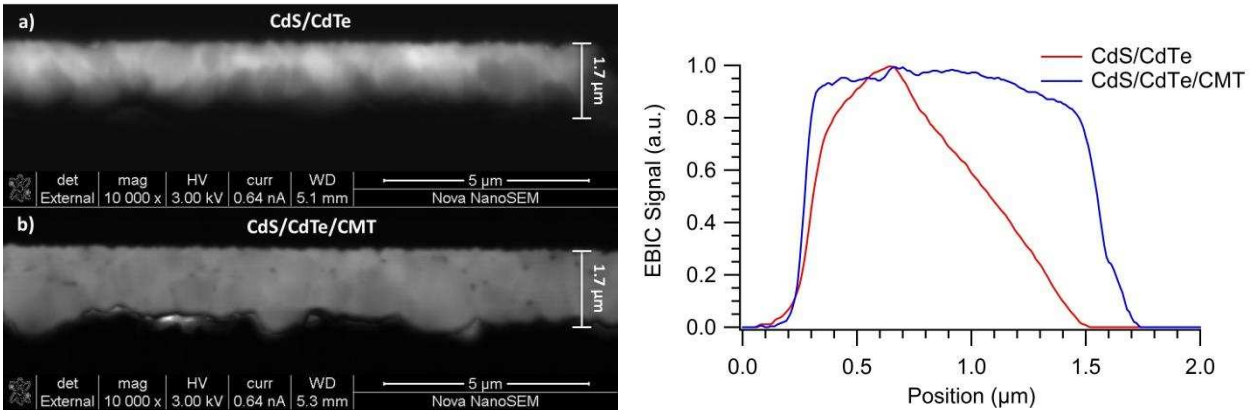


Figure 50: EBIC Maps and line profiles of a) CdS/CdTe (red) and b) CdS/CdTe/CMT) (blue)

3.3.2. CdTe/CdMgTe Cells Results with no Intentional Copper Doping

Copper can have a significant effect on lifetime, and the ability for CMT to be doped and how copper diffuses through the CMT could be in question. To separate potential copper effects from CMT effects, TRPL and performance parameters are studied with any intentional copper doping. With the addition of CMT a similar trend is present for V_{oc} with the addition of a constant V_{oc} shift over the CdTe reference sample. However the change in J_{sc} becomes less consistent, QE is presented in Figure 52 showing a significant reduction in QE change with and without CMT. A similar FF gain is shown in Figure 51, increasing with decreasing CdTe thickness as seen with Cu and a similar result with efficiency. It appears the only parameter significantly affected by the removal of copper was J_{sc}.

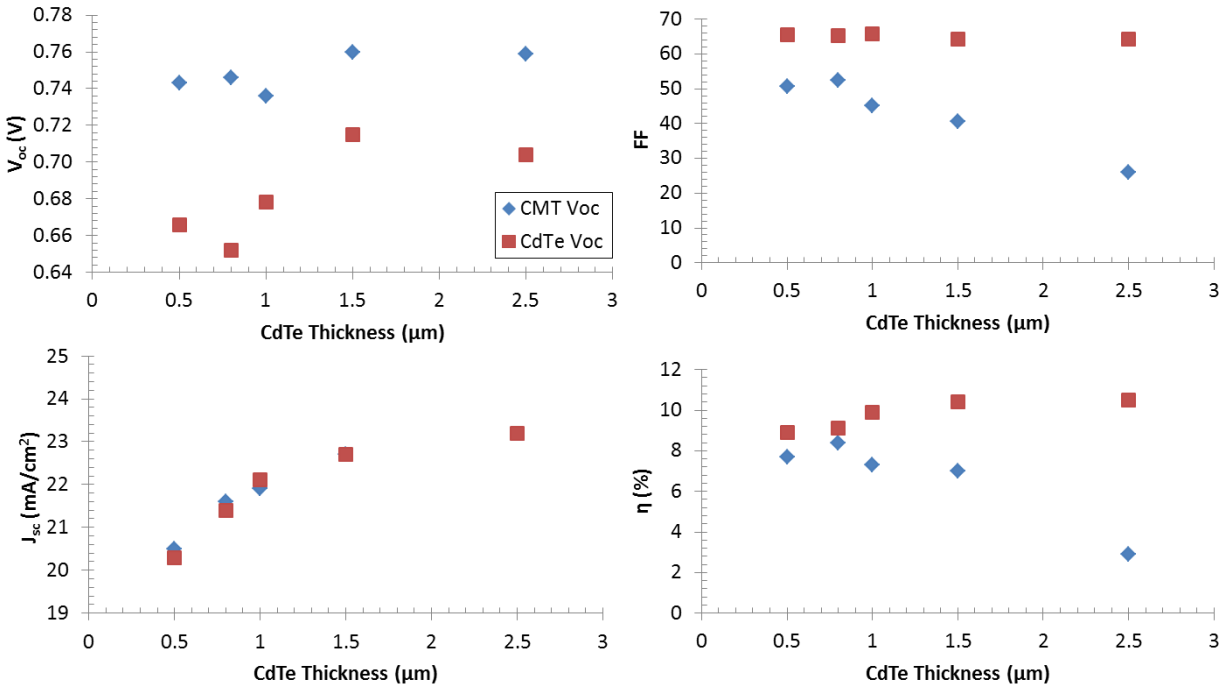


Figure 51: Performance parameters for CdTe/CMT Type cells without Cu

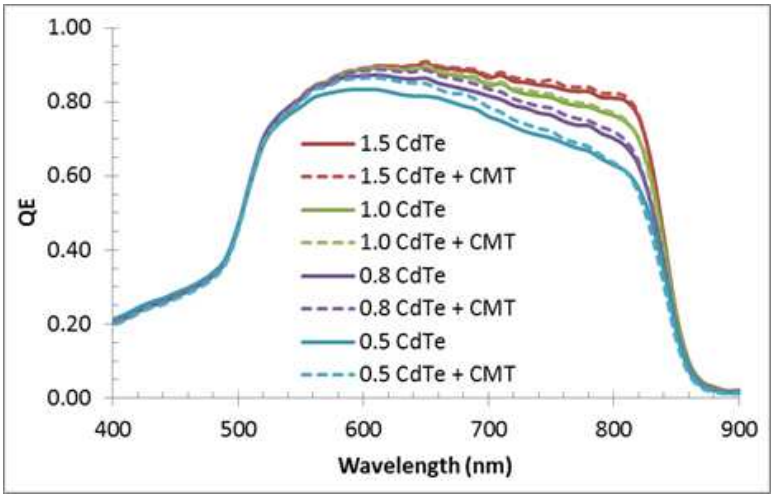


Figure 52: QE w and w/o CMT no Copper treatment

The improvements seen with and without copper appear to be similar but with the copper present the effect is more drastic. It is theorized that as the copper increases the doping at the back of the cell it reduces the mobility of the carriers. As the carriers are generated in this low mobility region the presence of a more passivated interface between CdTe and CMT shows an increased improvement. When the copper doping is removed the improvement remains but to a lesser degree because the localized mobility at the back is improved.

3.3.3. Higher Band gap CdMgTe

The results shown so far are for a relatively modest expansion of the CdTe band gap corresponding to a Mg fraction of about 15% compared to Cd (~1.75 eV). Modeling has suggested that further increase in the band gap of CMT would further increase V_{oc} (27). This is explored in Figure 53a, with increased band gap of the CMT layer there is no increase in V_{oc} improvement. However Figure 53b shows a loss in FF as the band gap is increased to 1.82 eV. The increase in CMT band gap is not resulting in further V_{oc} improvement but is producing a dominating reduction in FF.

One possible cause is the high electron affinity of the CMT film, causing part of the increased band gap to develop barriers not only in the conduction band but also in the valance band. The valance-band offset (VBO) generates a barrier to holes resulting in reduced current in the power generation region, presenting as a loss in FF.

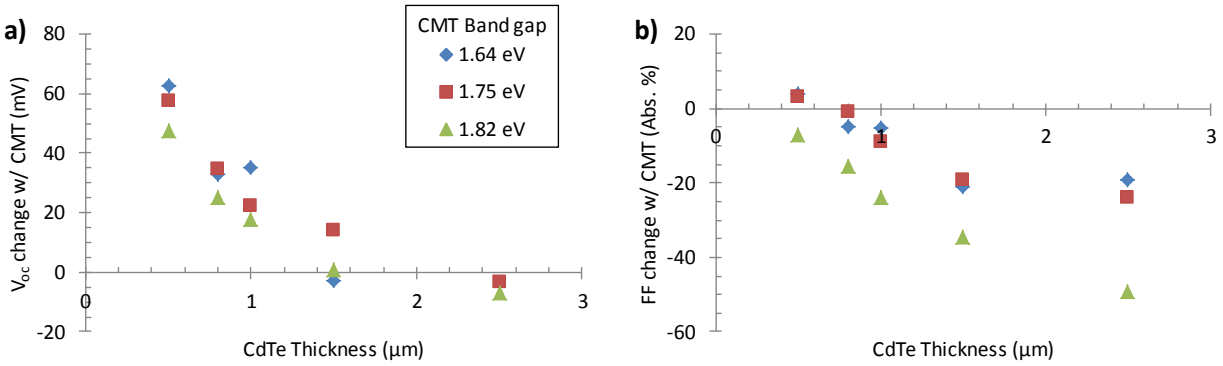


Figure 53: a) V_{oc} and b) FF change with the addition of the CMT layer at three different CMT band gaps, as a function of CdTe thickness

Figure 54a shows that the combination of the CdTe/CMT VBO and the CMT/metal electrode could further limit the transport of holes. Future work will include possible mitigation of this problem by adding a CdTe "cap" layer at the back of the CMT (Figure 54b) so that the benefit of the electron reflector can be realized without necessarily compromising the hole transport. AFORS-HET modeling is used for all band diagrams and are to scale.

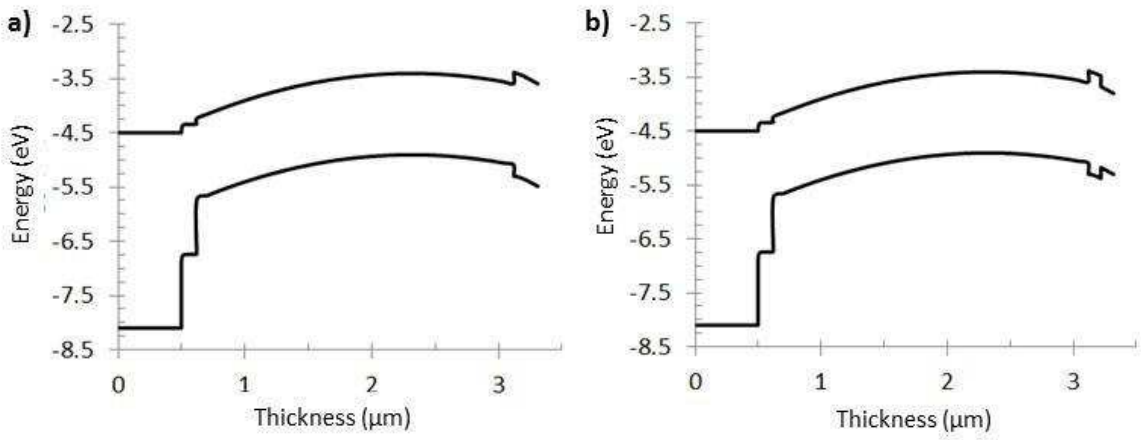


Figure 54: Band Diagram of a) TCO/CdS/CdTe/CMT/Carbon and b): TCO/CdS/CdTe/CMT/CdTe Cap/Carbon

3.3.4. Type A CdMgTe Cell Conclusions

The addition of a $Cd_{1-x}Mg_xTe$ layer to the back of the absorber of a CdTe solar cell is shown to improve both the current and the voltage of the cell. Furthermore, the improvements become greater for absorber thicknesses of 1 μm and less. The explanation, consistent with earlier simulations, is that the higher conduction band of the additional layer is reflecting electrons in the CdTe absorber and preventing them from reaching the high-recombination region near the metallic back contact. Also consistent with simulations, band-gap expansion of 0.2-0.3 eV appears to be sufficient, and larger expansions are not helpful. Supporting evidence for the effectiveness of the CMT layer comes from high-quality growth, longer decay time seen in TRPL, and collection throughout the CdTe seen in EBIC. A problem that needs to be addressed is that the fill-factor appears to be compromised due to a significant fraction of the band-gap expansion occurring in the valence direction, which can degrade hole collection. The proposed solution is to cap the CMT layer with an additional CdTe layer.

3.4. Material Issues Associated with Type A CdMgTe ER Structure

The following work was published in the 2015 MRS Spring Meeting in collaboration with Ali Abbas, Amit Munshi, Jennifer Drayton, John Raguse, Russell Geisthardt, Jim Sites, and W.S. Sampath (96). Primary funding for this work came from the Department of Energy's SunShot program (FPACE Award DE-EE0005399). Additional funding was supplied by NSF's I/UCRC and AIR programs. I am particularly grateful to Jason Kephart, Kevan Cameron, Carey Reich, Andy Moore, Tushar Shimpi, and Lauren Swanson for their support with the research.

Experimental results have shown an improvement in lifetime and voltage at a thin (1μm) CdTe thickness. However, the voltage improvements have been smaller than predicted (27; 28; 47). This may be due to the challenges in the $CdCl_2$ passivation process for the CdTe/CMT stack. Passivation is a critical step in CdTe fabrication that can typically convert cells from ~2% to ~13% efficiency (55). In this work, we examine some of the challenges in the passivation of the CdS/CdTe/CMT stack.

3.4.1. Manufacturing and Characterization Overview

The CdTe solar cells studied here were manufactured by sublimating the key layers using CSS deposition from sources integrated into a single-vacuum deposition system (ARDS) (47; 63). The cells were processed through the ARDS chamber where the CdS (120 nm) and CdTe (2.0 μm) layers were deposited as described in Section 2.1. The CdS/CdTe stack was then transferred to a separate chamber where a 120-nm, 1.8-eV CMT film was deposited (86). This deposition was performed in an argon environment with <0.01% O_2 to minimize oxidation. The deposition rate was ~4 nm/s for ~30s at 470°C. Due to the substrate temperature during

deposition, any passivation of the stack must come after CMT deposition (97). The sample was cooled below 120^{o}C prior to exposure to atmosphere. After CMT was deposited onto the CdTe stack the entire CdS/CdTe/CMT stack was then returned to the ARDS system for a $CdCl_2$ passivation process. The $CdCl_2$ process described in (63) was performed but in a <0.01% O_2 environment to minimize magnesium reactions (87). The cell was finished with a copper doping back contact process (63). The final back electrode is painted on with acrylic carbon (20 μm) and nickel paint (50 μm), and the cell structures were mechanically abraded to form ~0.60 cm^2 small-area devices.

In-depth microstructure characterization of the CdTe film stacks was carried out using Transmission Electron Microscopy (TEM), Energy-dispersive X-ray spectroscopy (EDX), and X-ray Photoelectron Spectroscopy (XPS). TEM samples were prepared by Focused Ion Beam (FIB) milling using a dual beam FEI Nova 600 Nanolab. A standard in-situ lift-off method was used to prepare cross-sectional samples. A platinum over-layer was deposited to define the surface and homogenize the final thinning of the samples down to 100 nm. Transmission Electron Microscopy (TEM) was undertaken using a Tecnai F20 operating at 200 kV to investigate the detailed microstructures of the cell cross sections. The system was equipped with an Oxford instruments X-max N80 TLE SDD EDX detector, and this was used in STEM mode to collect elemental distribution maps. These maps were collected in a single frame using a long dwell time, as well as a small condenser aperture (70 μm) to minimize drift and beam spread during collection. Additional elemental characterization was performed using a Phi-5800 XPS which utilized a monochromatized Al K_α x-ray source and a neutralizing electron shower to reduce charging. The films were sputtered with a rastering Argon ion beam at a voltage of 5 kV over an area of 9 mm^2.

3.4.2. Type A CdMgTe ER Issues

When CdTe was passivated with $CdCl_2$, the cell efficiency improved from ~2% to 13%. The primary effects observed were the removal of stacking faults, the addition of chlorine at the grain boundaries of the CdTe, and sulfur diffusion at the CdS/CdTe interface (97; 55). When passivating the CdS/CdTe/CMT stack, chlorine must travel through the CMT film and down the CdTe grain boundaries. The CMT film has been shown to be epitaxial with the underlying CdTe cell (28). Thus the grain boundaries of the two films are aligned. Cross-section TEM and EDX are presented in Figure 55 of an un-passivated CdS/CdTe/CMT stack. The magnesium film appears to be continuous along the back of the CdTe cell, conforming to the shape of the CdTe morphology and maintaining epitaxial growth. There is little to no sulfur diffusion from the CdS, and no chlorine signature. Tellurium images were uniform in all cases and not shown.

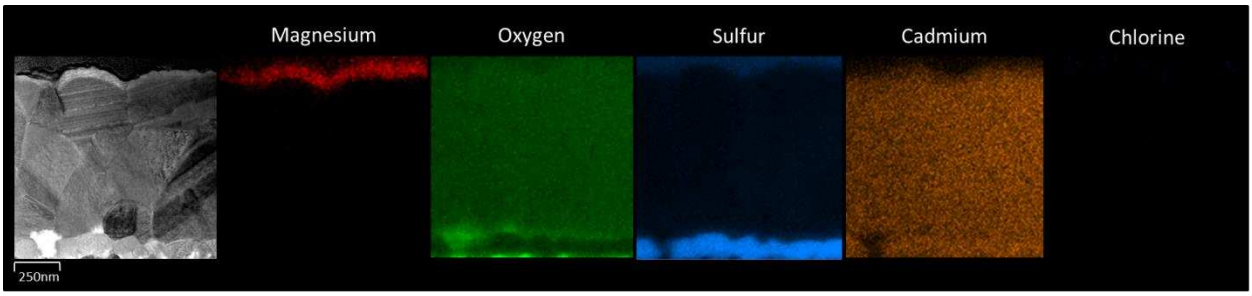


Figure 55: Cross Section TEM and EDX of CdS/CdTe/CMT stack without passivation

Figure 56 is of the same film stack as Figure 55 following a standard $CdCl_2$ treatment (63). Cell performance is improved, and chlorine is seen to decorate the grain boundaries. There is no apparent presence of stacking faults, and there is minimal sulfur diffusion. However, the CMT film no longer looks continuous, and it appears that during the passivation step the CMT film is degraded by substantial magnesium loss. If any oxygen or water is present, the Gibbs free energy is favorable for MgTe to react and reduce to MgO (28). There is a strong oxygen and chlorine signature at the CMT layer, suggesting that some of the magnesium may have reacted

and formed an oxide or chloride. Figure 57 shows the response from the XPS KLL magnesium peak as a function of depth into the film. The MgTe has a peak that corresponds to ~303 eV and MgO has a peak that corresponds to ~306 eV. After passivation the MgO signature at 306 eV is apparent on the surface, and as we sputter into the device, the peak shifts towards a MgTe signature at 303 eV. This suggests that the back of the cell has reacted from MgTe to MgO.

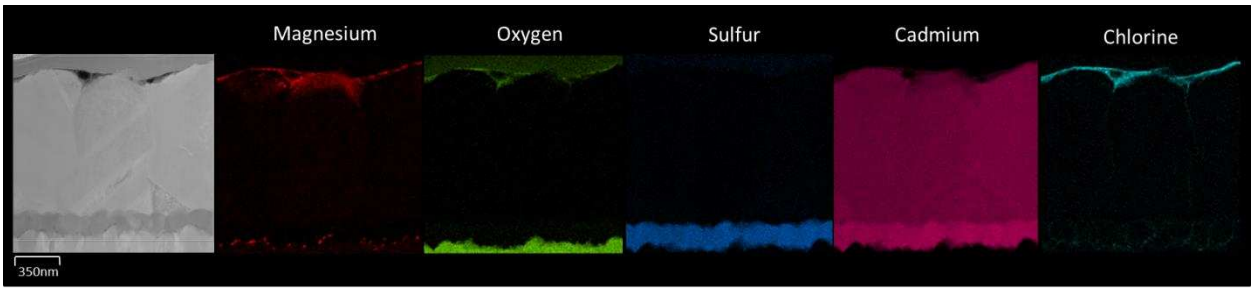


Figure 56: Cross Section TEM and EDX of CdS/CdTe/CMT stack passivated with $CdCl_2$

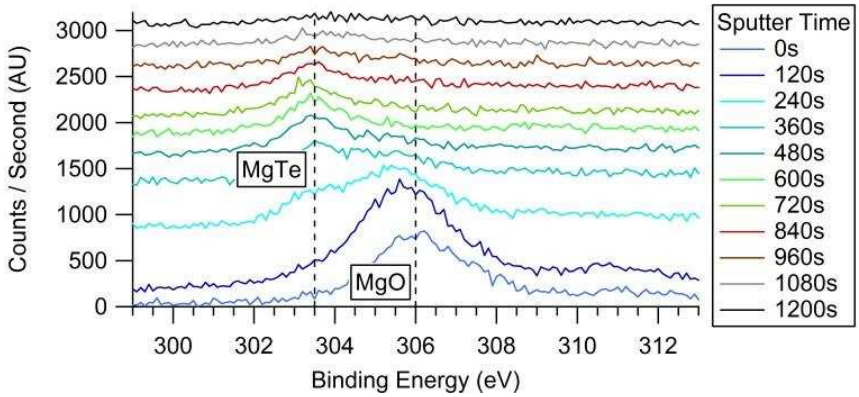


Figure 57: XPS of the Magnesium KLL peak, (Sputtered from bottom to top)

3.4.3. CdTe Capping Layer

In order to minimize the formation of MgO, a thin CdTe capping layer was deposited on top of the CMT layer to limit exposer of the film to atmosphere with the intention of reducing oxidation and magnesium loss. This CdTe layer was deposited immediately after the CMT deposition and was controlled by shuttering off the magnesium vapor flux in situ. With the

addition of the CdTe capping layer there is an improvement in cell performance, primarily an improvement in FF. Since MgO has a large band gap (~6.72 eV) and an electron affinity of 2.8 eV, this would induce a large valance band offset at the back of the device and likely cause this reduction in FF (28; 98).

Figure 58 shows cross section TEM and EDX of the passivated CdS/CdTe/CMT/CdTe Cap stack. The addition of a 100nm CdTe Cap has removed the previously seen oxygen signature at the back of the cell, indicating that the cap has helped prevent MgO formation. However, localized magnesium loss is present and appears more significantly at the grain boundaries.

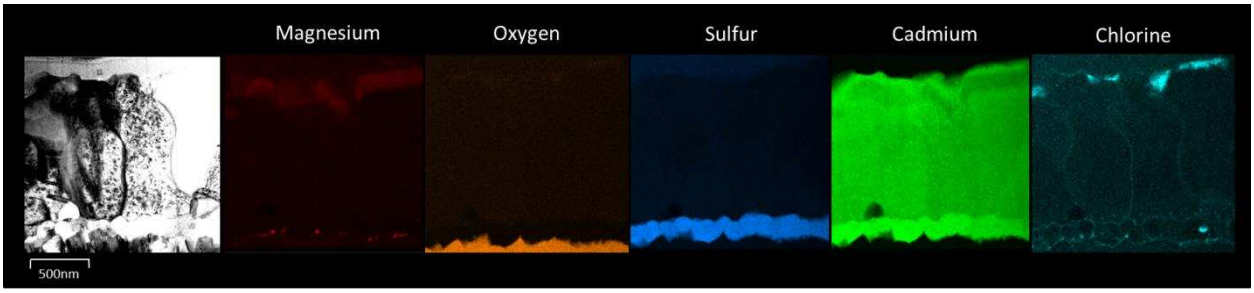


Figure 58: TEM and EDX of CdS/CdTe/CMTe/CdTe Cap stack passivated with $CdCl_2$

$MgCl_2$ has been shown by some to be as effective as $CdCl_2$ in passivating CdTe cells (99). The Gibbs free energy is favorable for MgTe to react with $CdCl_2$ and form CdTe + $MgCl_2$. However, if the cells were passivated with $MgCl_2$ instead of $CdCl_2$, the localized magnesium loss could be reduced (28). Figure 59 shows the cross section TEM and EDX of a CdS/CdTe/CMT/CdTe Cap cell passivated with $MgCl_2$ instead of $CdCl_2$. The cell performance did not improve, and the localized magnesium loss was still present and similar to Figure 58 with the $CdCl_2$ passivation. This may suggest that the loss mechanism is not a reaction with $CdCl_2$ but

with chlorine, since if chlorine is moving down the grain boundaries and not $CdCl_2$, the loss mechanism would likely not be the same between $CdCl_2$ and $MgCl_2$.

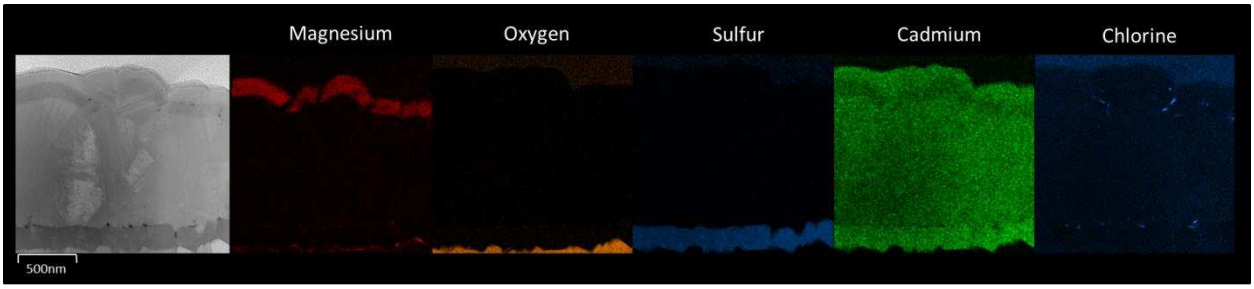


Figure 59: TEM and EDX of CdS/CdTe/CMT/CdTe Cap stack passivated with $MgCl_2$

As seen in Figure 58 and Figure 59, the localized magnesium loss is highest at the grain boundaries for cells with a capping layer. Figure 60 shows a line scan taken from EDX across a grain boundary of a post-passivated CdTe cell at a grain boundary. There is a significant decrease in magnesium content and an increase in cadmium content, implying that the CMT has reacted and is now CdTe. There is also an increase in oxygen and a decrease in tellurium suggesting that some magnesium may have reacted to form MgO.

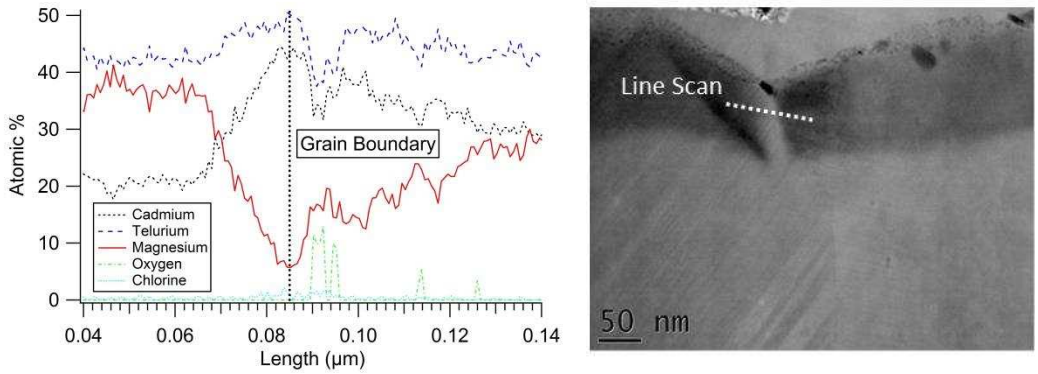


Figure 60: Line scan of a CdS/CdTe/CMT/CdTe Cap stack grain boundary passivated with $CdCl_2$

Figure 61 shows a magnified view of the CdS/CdTe interface of a CdS/CdTe/CMT/CdTe Cap stack passivated with $CdCl_2$. It appears that the magnesium has diffused down the grain boundaries and has begun collecting at the junction and window layer interfaces. With no substantial oxygen or chlorine concentration to correlate with the magnesium, it is unclear if it is strongly bonded. It is possible that this is the magnesium that was lost from the CMT film during passivation and has traveled down the grain boundaries and collected at the front interfaces.

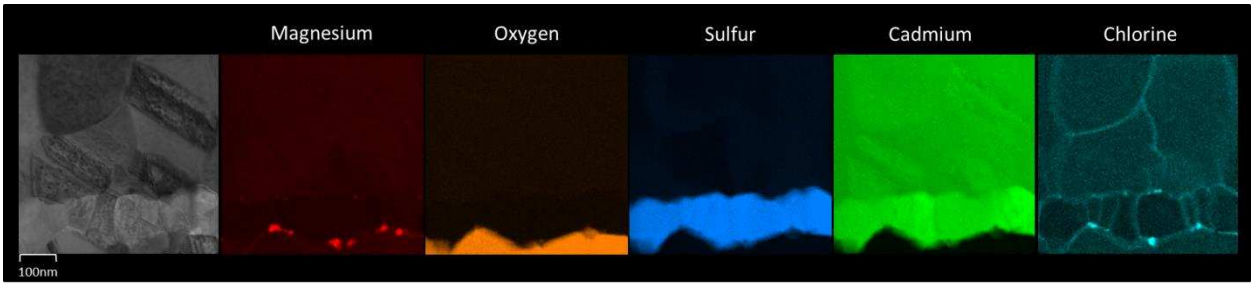


Figure 61: TEM and EDX of the CdS interface of a passivated CdS/CdTe/CMT/CdTe Cap stack.

The accumulation of magnesium also affects the electrical characterization of the cells. Figure 49 shows QE curves of two cells, one with and one without CMT. Both cells have the same initial CdS thicknesses and received the same passivation treatment but it has consistently been that the cells with magnesium diffusion show decreases in QE between 300 and 500 nm. Since this magnesium diffusion does not affect the whole spectrum, it is thought that the magnesium must be affecting the CdS and not simply scattering incoming light.

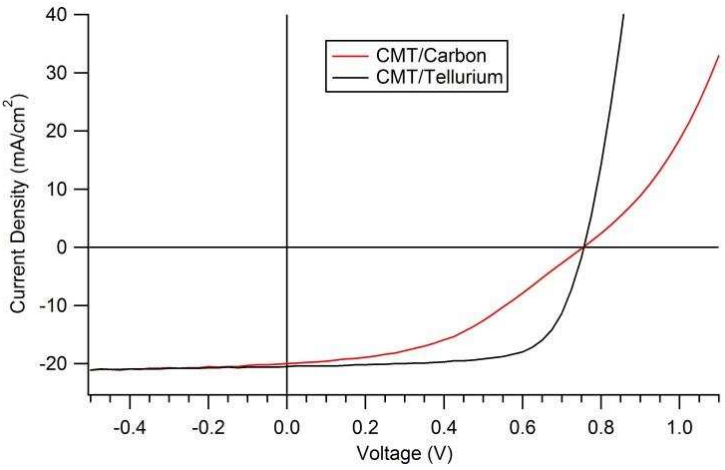
3.4.4. Type A CdMgTe ER Material Characterization Conclusions

Conformal layers of CMT were deposited at the back the of CdTe solar cells. After the CdS/CdTe/CMT stack was passivated with a standard $CdCl_2$ treatment, there was significant degradation to the CMT film. It appeared that the CMT layer was partially oxidized to form MgO on the CMT surface as seen in the XPS peaks and EDX images. This oxide formation had

an electron effect as well, reducing the cell's FF and overall performance. With the addition of a CdTe capping layer, the oxygen signature was significantly reduced, and cell performance was improved. EDX showed however that even with the CdTe capping layer there was localized magnesium loss at the shared grain boundaries. A $MgCl_2$ treatment was explored to minimize this effect, but localized magnesium loss was present with the $MgCl_2$ passivation as well. The lost magnesium appears to be traveling down the grain boundaries to the CdS and TCO interfaces and collecting as evidenced by the reduced 300-500 nm (CdS region) QE response.

3.4.5. Contacting CdMgTe with Tellurium

As shown in Figure 54, due to the non-ideal electron affinity of the CMT material a larger VBO can form blocking the holes and reducing the FF of the device. A back contact with a higher electron affinity and doping is needed to minimize the VBO formation. Tellurium has been used to minimize VBO formation in CdTe as discussed in Section 2.3. Figure 62 shows a comparison of tellurium and carbon in contacting the CMT at the back of a CdTe cell. The tellurium improves the FF of the cell and is a potentially ideal contact for CMT cells. It is theorized that the holes may diffuse from the tellurium layer into the CMT layer moving the bands and minimizing the VBO (32).



Cell Structure	V_{oc} [mV]	J_{sc} [mA/cm^2]	Fill Factor [%]	Efficiency [%]
CMT/Te	757	20.5	69.7	10.8
CMT/C	755	20.0	43.3	6.5

Figure 62: JV of CdS/CdTe/CMT with carbon and tellurium back contacts

3.5. Type A ER Structure with CdTe Cap and Tellurium Back Contact

With the addition of a CdTe cap to reduce oxidation and the tellurium back contact for improved band alignment the CdTe/CMT ER structure was re-swept across various CdTe thickness, shown in Figure 63. A baseline cell without the CMT layer is used for reference, both intentional and non-intentional copper is processed. Figure 63a show a consistent offset in V_{oc} of ~50 mV with the addition of CMT layer, this is consistent with previous ER work, however under ideal conditions the V_{oc} increase is estimated at 200 mV. The FF remains primarily flat for the reference cell around 65-70 % for the baseline structure while the ER structure shows an increase of ~10% with the thinning CdTe to 0.8 μm where it flattens out slightly above baseline cells. This is consistent with prior work and models described above. J_{sc} remains fairly constant for both structures. Overall there is ~0.8 - 1.0% increase in efficiency with the addition of the ER layer when the absorber is below 1 μm thick.

Figure 63b with copper doping shows more degradation in voltage as the baseline cell is thinned down while the voltage for the ER structure remains flat, this is similar to results in Section 3.3. Copper may help dope the CMT but may also reduce mobility at the CdTe/CMT interface possibly increasing interface recombination velocity and reducing the ER effect. Both the baseline and ER structure show substantial reduction in FF, likely associated with excess copper getting to the front junction. It appears CMT may prevent copper diffusion as the FF loss is about half compared to the baseline cells. There is significantly more J_{sc} loss with both structures as compared to the no copper condition. With possible increased interface

recombination velocity and narrowed depletion width, the carrier collection efficiency at longer wave lengths is likely affected. Over all the ER structure improves efficiency as the CdTe is thinned, however the cells appear to be dominated by copper migration at the thin CdTe conditions. This masks whether the ER effect is helping or the reduction in copper diffusion with CMT is dominating. The assumption that the interface between CdTe and CMT may not be as ideal as TEM images have implied (28). Further analysis of this interface may be required as substantial interface recombination velocity at the CdTe/CMT interface would significantly reduce the effectiveness of an ER concept.

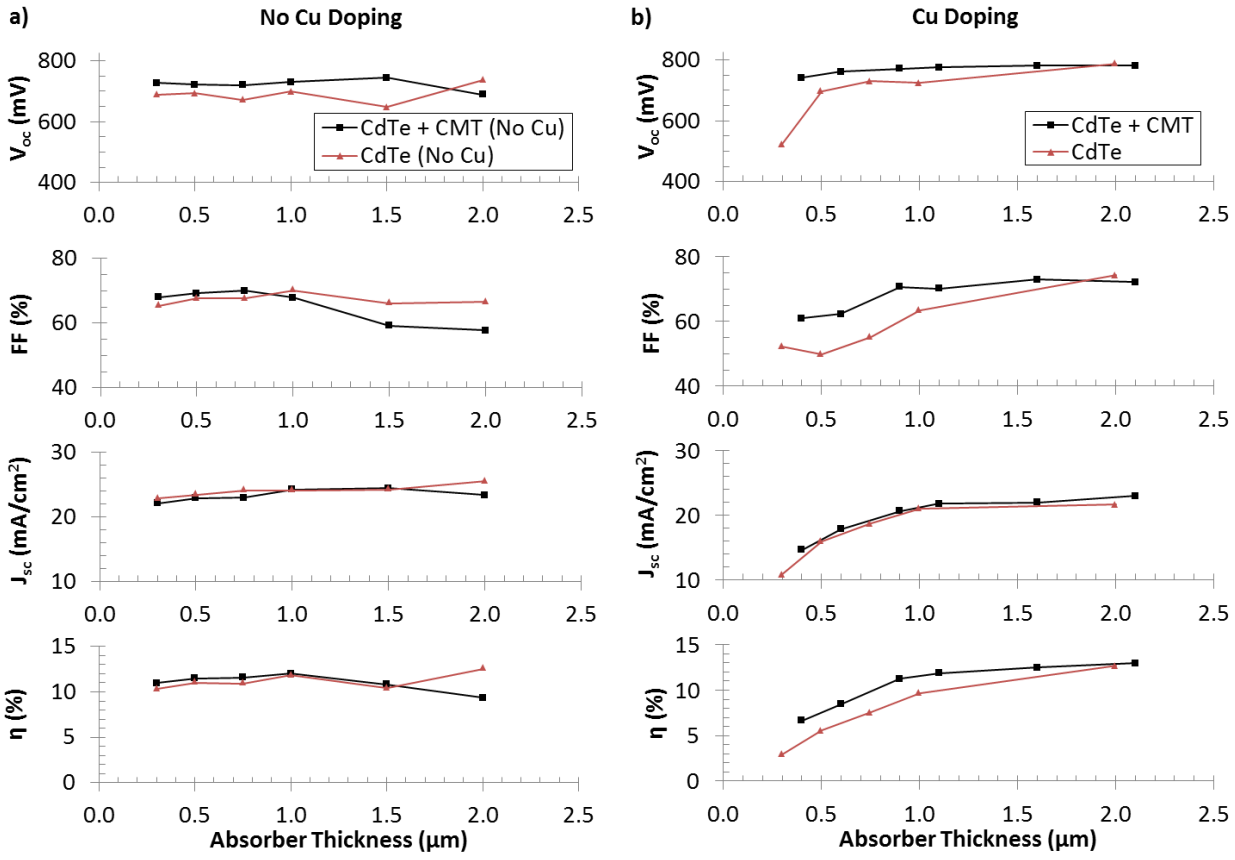


Figure 63: JV parameters of a CdTe/CMT ER structure with CdTe cap and Tellurium back contact at various CdTe thicknesses, with and without copper. Reference cells have identical structure but with CMT removed.

3.6. Using Double Hetero-Structures to Assess CdMgTe Type A ER

The improvement seen with the presence of CMT has been significantly less than what modeling has predicted, 50 mV compared to 200 mV. Potential reasons shown in Section 3.4 are possibly the localized loss of CMT from the grain boundaries. Another possibility is that the interface between the CMT and CdTe has too high of recombination, which can be detrimental to performance. Or finally that the bulk lifetime of the material is low and the minority carriers cannot reach the back interface to be reflected. To address these concerns and limit any potential influence from the rest of the cell structure a double hetero structure shown in Figure 64 was fabricated and TRPL lifetime was measured to see if significant lifetime improvements can be measured.

Single crystal CdTe growth has shown a significant improvement in lifetime with the addition of CMT on both sides of the crystal (100; 32). This tells us that the CdTe material is capable of having high lifetimes. Replicating this work in polycrystalline CdTe should show if the grain boundaries, interfaces, and localized magnesium loss are detrimental to lifetime.

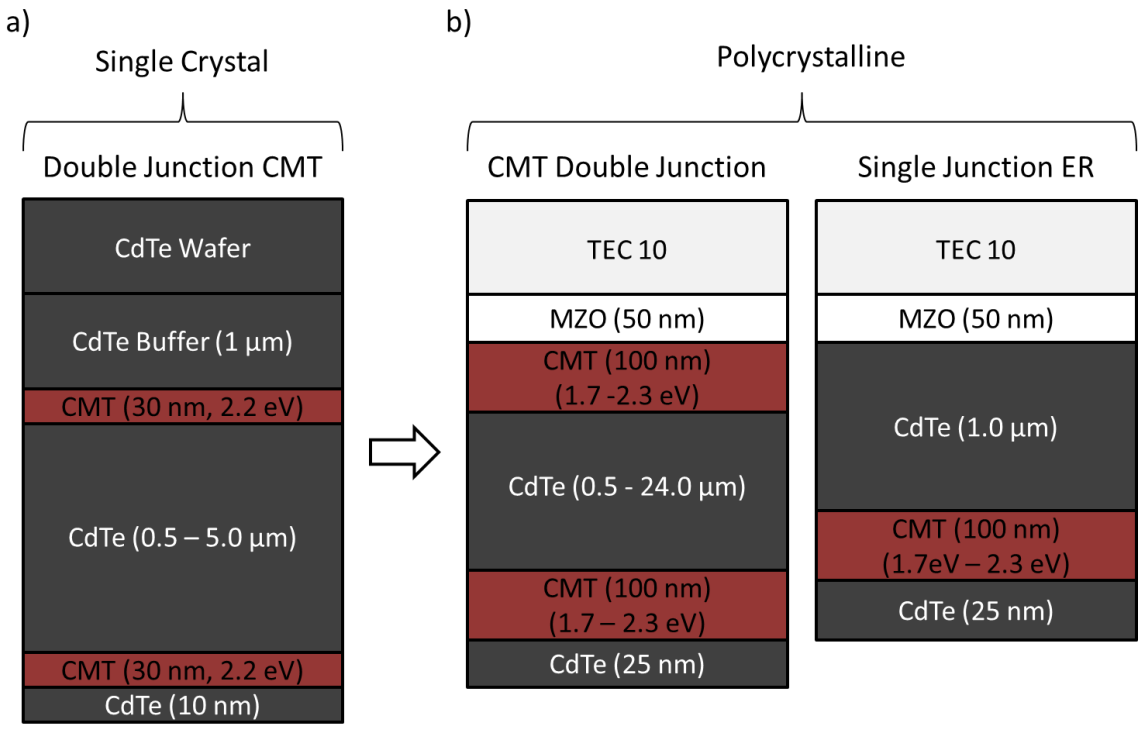


Figure 64: Double hetero-structure CMT/CdTe/CMT a) Single Crystal b) Polycrystalline

3.6.1. CdMgTe Double Hetero-Structure Fabrication

CMT double hetero-structure (DHS) depicted in Figure 64 were manufactured using the ARDS described in Section 2.1 and the RTC described in Section 3.3 (38; 47). The CMT DHS used a Tec 10 substrate with a 100 nm MZO buffer layer (45). CMT was deposited in the RTC as described in Section 3.3 (86; 47). The CMT film was transported to the ARDS in atmosphere for >10s. The film was heated to 470 ^{o}C and CdTe was deposited in a 40 mTorr Nitrogen environment. The CdTe thickness was swept from 0.5 – 24.0 µm using increasing deposition time. The MZO/CMT/CdTe cell was then transferred back to the RTC where, under identical process conditions, the second CMT layer was deposited. CMT layers were deposited at three band gaps: 1.8, 2.0, 2.2 eV, all at 100 nm thick. The cell was then vented and transferred to the ARDS where the MZO/CMT/CdTe/CMT cell was then heated to 470 ^{o}C and a CdTe cap was

deposited at 25 nm thickness. Note this is a reduced CdTe cap thickness than what was previously optimized. This was done to minimize any potential TRPL signal from the capping layer. This reduced capping thickness may not fully protect the CMT layer during passivation and should be further characterized. The cell then went through the standard passivation treatment with no copper doping (38). The passivation time in both the $CdCl_2$ source and strip source was doubled for samples 6.0, 12.0, 24.0 µm CdTe. Half the cell received a Tellurium back contact as described in Section 2.2 while the other half was saved for TRPL analysis. Note there were atmospheric vacuum breaks at every interface of the structure. Reference cells were fabricated for each band gap CMT. The reference cell consisted of a MZO/CMT/CdTe structure at a CdTe thickness of 1.5 µm.

3.6.2. CdMgTe Double Hetero-Structure JV Cell Performance

Figure 65 shows JV parameters for all three CMT DHS structures with varying thickness. There is a slight increase in V_{oc} at the thin condition similar to results shown in Section 3.3. As the CdTe thickness increases past 2.0 µm the V_{oc} performance stabilizes and reduces in the 2.2 eV. This may be associated with oxide formation in the higher 2.2 eV CMT case. J_{sc} is fairly consistent with possible minor improvements at the thin conditions. There is substantial degradation in J_{sc} at 12 and 24 µm likely due to the poor passivation quality for those thicknesses. FF correlates well with CMT band gap, as the CMT band gap is increased the FF reduces at all CdTe thicknesses. This is likely associated with the formation of a CBO at the front blocking electrons, similar to the MZO work by Kephart (45) and the formation of a VBO at the back of the device as described in Section 3.4. This is likely the dominate effect as the reference cells with CMT only at the front did not show a significant FF/CMT band gap

correlation. Efficiency showed a peak around 6 μm, this is likely associated with preferred process conditions as that is near the current record performance set point of the ARDS tool (70).

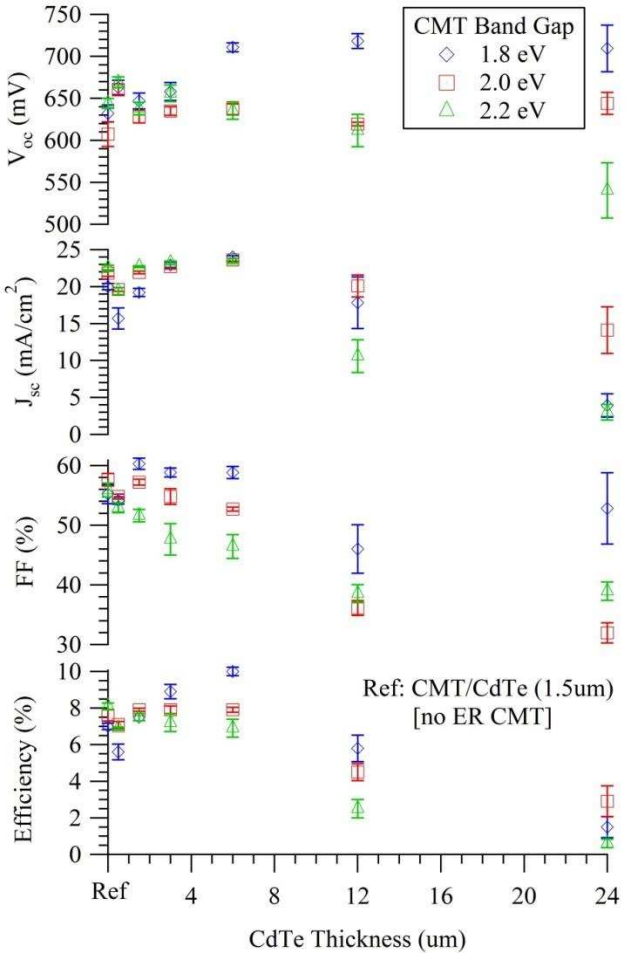


Figure 65: JV of CMT Double-Hetero-Structures at 1.8, 2.0, 2.2 eV band gaps and various thicknesses.

3.6.3. Time Resolved Photolumination Analysis

3.6.3.1. Characterizing the Polycrystalline CdTe/CdMgTe Interface

The samples underwent TRPL analysis similar to Section 3.3. The TRPL was performed using a Horiba Deltamyc system. It utilized a 640 nm (1.93 eV) excitation source at an average diode power of 0.4 mW. The samples were measured till a peak total of 10,000 points were

collected. Curves were analyzed using DecayFit software to approximate bi-exponential fits. The CMT band gap is above the excitation wavelength of 640 nm (1.93 eV) then the excitation would occur in the CdTe layer. Letting the CMT/CdTe interface be probed as over 90% of the light would be absorbed in the first 400 nm of the CdTe layer at 640 nm (101).

Figure 66 shows the bi-exponential fit, τ_1 and τ_2 as measured from the front and back of the CMT DHS at 2.0 and 2.2 eV CMT band gaps with various CdTe thicknesses. There is a strong correlation with CdTe thickness amongst all of the parameters. This is indicative of strong interface recombination dependence. Similar trends are seen when TRPL is measured from the back and the front. This indicates that both interfaces are behaving in a similar capacity. The 2.2 eV band gap shows slightly higher performance than the 2.0 eV band gap which is consistent with a larger CBO reflecting carriers away from the interface. Samples measures from the front show slightly higher lifetimes than those from the backs, believed to be correlated with field effects in the front. This however is a subtle behavior with the CdTe thickness dominating the trend in all cases.

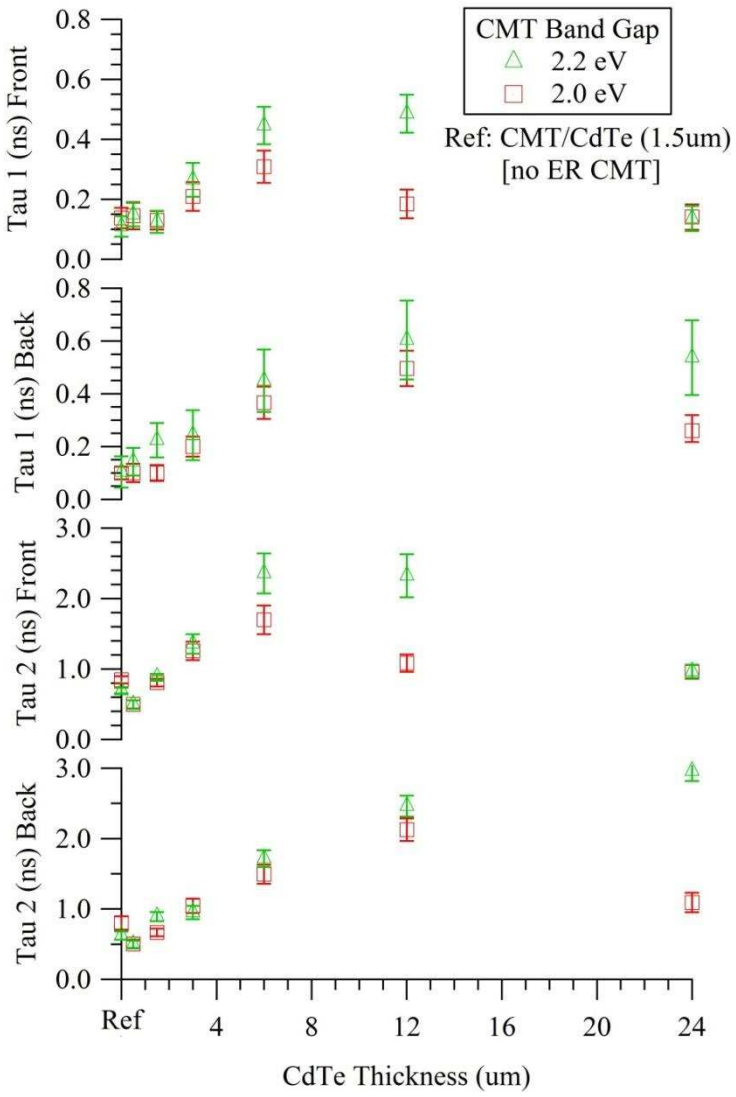


Figure 66: TRPL approximated Tau1 and Tau2 for 2.0 and 2.2 eV CMT DHT at various thicknesses.

Zhao et. al. has demonstrated 1.1 V CMT DHT cells with 3600 ns lifetimes on molecular beam epitaxial grown cells using a InSb (001) substrate (32). The interface recombination can be analyzed by varying the thickness of the bulk CdTe layer. The measured effective lifetime τ_{eff} is related to the radiative (τ_{rad}) and non-radiative (τ_{non}) lifetimes of the cell described by Equation 3 (32). Radiative lifetimes are fairly low for CdTe as compared with higher performing technologies (68; 34). The radiative lifetimes have been correlated to the photon recycling factor

(ϒ) (102), materials radiative recombination coefficient (B), and the doping concentration (N_D). Photon recycling increases with CdTe thickness, thus the radiative lifetimes increase for CMT DHS with thicker CdTe absorption layers. The non-radiative lifetimes are associated with the bulk Shockley-Read-Hall (SRH) lifetimes (τ_{SRH}) and the interface recombination velocity (IRV) described in Equation 3.0 as the effective IRV (S_{eff}) and CdTe absorber thickness (d).

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{non}} = (1-\gamma)BN_D + \frac{1}{\tau_{SRH}} + \frac{2S_{eff}}{d} \tag{3}$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_1} + \frac{1}{\tau_2} \tag{4}$$

The τ_1 and τ_2 are converted to an effective lifetime using Equation 4. Since radiative recombination is dependent on sample thickness, the non-radiative lifetimes are used to extrapolate effective IRV. Radiative lifetimes were calculated assuming B = $4.3*10^{-9}$ cm^3 s^{-1}, N_D = $1.5*10^{14}$ cm^{-3}. Note that in the polycrystalline CMT DHS cells, the non-radiative recombination values dominate the equation by over 4 orders of magnitude, implying that the bulk lifetime effects are being washed-out by interface effects. This is not the case in the single crystal cells presented by ASU (32). Figure 67 shows the inverse of the non-radiative lifetime ($1/\tau_{non}$) plotted against 2/d for a characteristic cell. A linear correlation can be fit to the data giving an approximation for the effective IRV from the slope and the bulk SRH lifetime from the y-axis intercept. Excels statistics package allowed the LINEST function to give slope and intercept approximations of the data, along with standard deviations of the fit for error bar approximations.

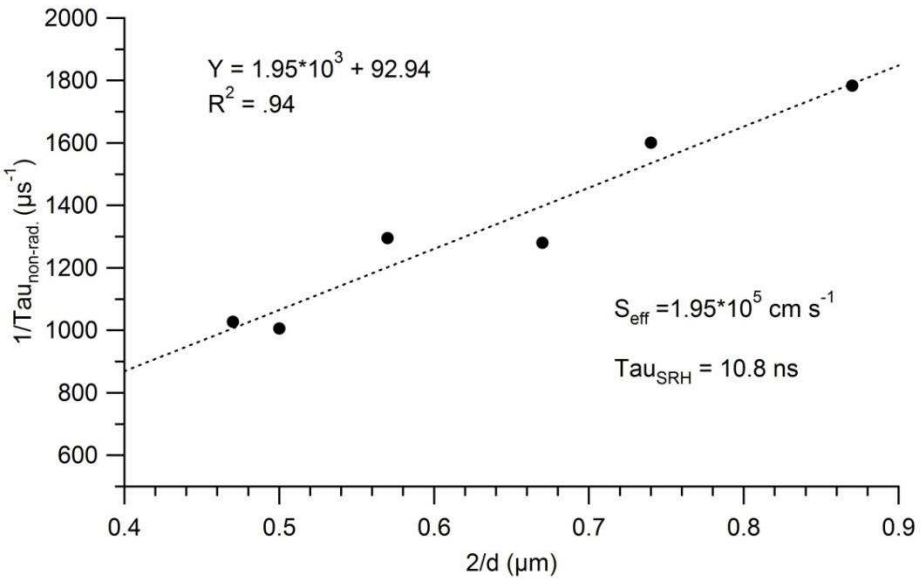


Figure 67: Inverse of the non-radiative lifetime vs 2/d (Bulk CdTe absorber thickness). A linear fit is used to approximate the interface recombination and bulk SRH lifetime.

This technique is used on all CMT DHT devices described above as well as MZO DHT structures where an MZO cell is deposited as described by Kephart (45) with an addition MZO layer deposited after the $CdCl_2$ step. For reference MZO baseline cells are characterized with process condition described by Swanson and Munshi (38; 47). Cells described in Section 3.0 are also characterized for comparison. Table 5 outlines the approximated effective IRV (S_{eff}) with a standard deviation reference (S_{eff} Std. Dev.), bulk SRH lifetimes (τ_{SRH}) with stand deviation, and R^2 values to give insight to the linear fit.

Table 5: Approximation of effective IRV and bulk SRH lifetimes with standard deviations using the technique described in Section 3.3.3.

Sample Details		Fitted Parameters				
(CMT Band Gap (eV)	Measured	S_{eff} (cm s^{-1})	S_{eff} Std Dev (cm s^{-1})	τ_{SRH} (ns)	τ_{SRH} Std Dev (ns)	R^2
CMT DHT 1.8 eV	Back	9.77E+04	5.96E+04	0.19	0.92	0.44
CMT DHT 2.0 eV	Back	2.32E+05	1.01E+05	0.21	0.54	0.68
CMT DHT 2.2 eV	Back	1.65E+05	9.58E+04	0.26	0.57	0.89
CMT DHT 1.8 eV	Front	1.78E+05	6.83E+04	0.26	0.8	0.66
CMT DHT 2.0 eV	Front	1.01E+05	5.53E+04	0.18	0.99	0.51
CMT DHT 2.2 eV	Front	1.59E+05	8.60E+04	0.26	0.63	0.89
MZO/CdTe/Te	Front	1.28E+05	2.29E+04	2.8	1.3	0.89
MZO/CdTe HT/Cu/Te	Front	1.95E+05	2.48E+04	10.76	6.2	0.94
MZO DHT	Front	1.73E+05	5.38E+04	0.7	0.56	0.72
	Back	2.01E+05	7.14E+04	0.09	0.42	0.67
CdS/CdTe/Cu/C	Front	8.13E+04	1.40E+04	4.89	2.99	0.87
CdS/CdTe/CMT/Cu/C	Front	6.88E+03	5.76E+03	0.87	6.55	0.41
CdS/CdTe/C	Front	6.84E+04	1.27E+04	1.48	3.3	0.91
CdS/CdTe/CMT/C	Front	1.15E+04	1.06E+04	0.94	3.57	0.38

The CMT DHT structures show similar results for all band gaps. The interface recombination is dominating the structure, this is in agreement with the strong correlation between lifetime and CdTe thickness. The approximated lifetime of all CMT/CdTe interfaces in the DHS are ~$2*10^5$ cm s^{-1}. Previous work has suggested the CdTe/CMT interface was epitaxial with low IRV (28). This was based off of high resolution TEM images of the interface showing similar lattice correlation and lattice constants. This is in contradiction with the JV and TRPL analysis. Modeling done by Toa Song is presented in Figure 68, showing predicted performance of an ER structure at various IRV between the ER layer and CdTe layer. This model uses CdZnTe in place of CMT, the differences are described in Section 3.1 but for modeling purposes is assumed to be a more ideal ER structure as it has no inherent VBO issue. Modeling predicts that an ER/CdTe interface with IRV of ~$2*10^5$ cm s^{-1} will not yield a substantial voltage

increase. The model predicts the IRV must be ~10 cm s^{-1} for a voltage of ~1100 mV to be seen. The 1100 mV cell demonstrated by Zhao had an effective IRV of ~2 cm s^{-1}, consistent with Tao's model (32).

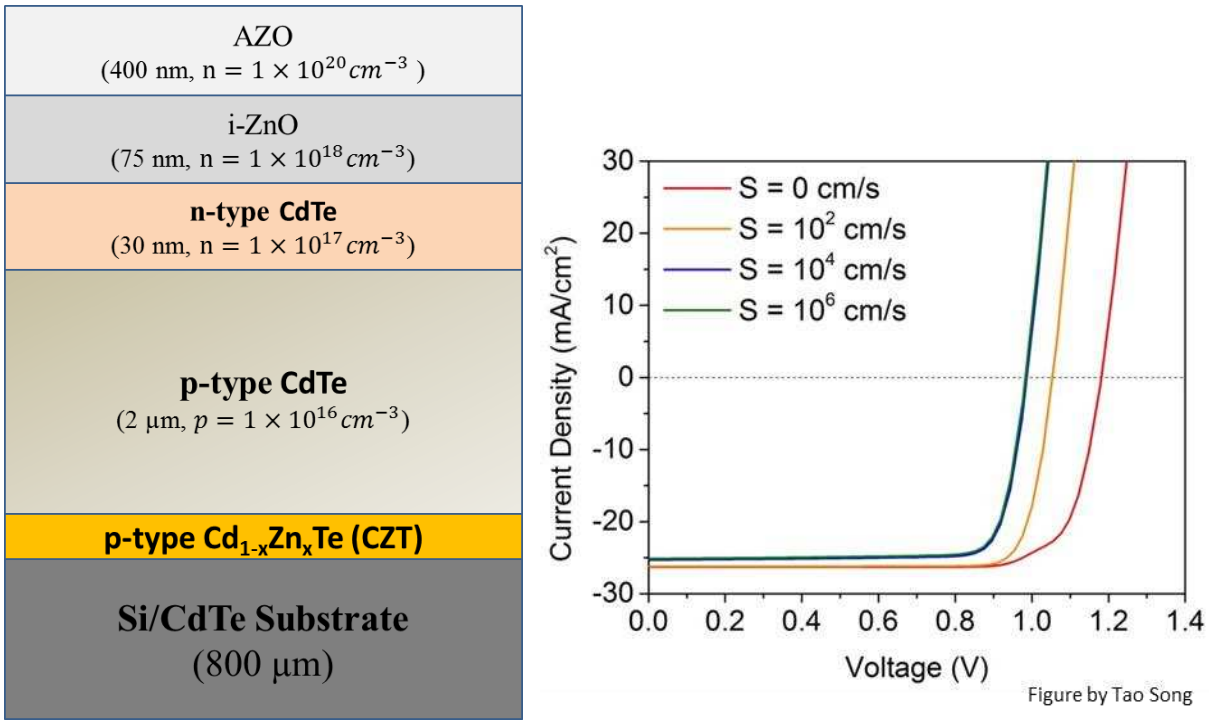


Figure 68: a) Structural diagram of ER Cell b) Modeled JV performance as a function of varying ER/CdTe IRV.

3.6.3.2. Characterizing the MZO and CdS interface with Polycrystalline CdTe

The addition of MZO has experimentally been shown to improvement both J_{sc} and V_{oc} (45). The improvement is attributed to the development of a CBO being formed at the front CdTe interface and reduces the impact of high interface recombination. This was modeled in detail by Song (103). Figure 69 is showing a modeled comparison of CdS and MZO as buffer/emmiter layers. The improvements in V_{oc} from CdS to MZO is present only when the emitter/CdTe interface has IRV < 10^4cm s^{-1}. Experimentally shown there is a ~50 mV increase in

V_{oc} using MZO compared to CdS (38; 45). Base on modeled results in Table 5, this implies an IRV of 10^5cm s^{-1}. Table 5 shows TRPL analysis of the MZO/CdTe interface both in a baseline cell structure and a DHS. Using the TRPL analysis as described in section 3.3.3.1 the effective IRV from the MZO/CdTe interface is ~1.5*10^5 cm s^{-1}. This is in agreement with experimental, modeling, and literature of polycrystalline CdTe interfaces (45; 38; 103; 104; 105). MZO DHS show no change in IRV or SRH when measured from the front or the back, implying field effects are marginal and IRV is dominating. Table 5 shows a small improvement with CdS compared to MZO, potential 8.1*10^4 cm s^{-1} with copper and 6.8*10^4 cm s^{-1} without copper.

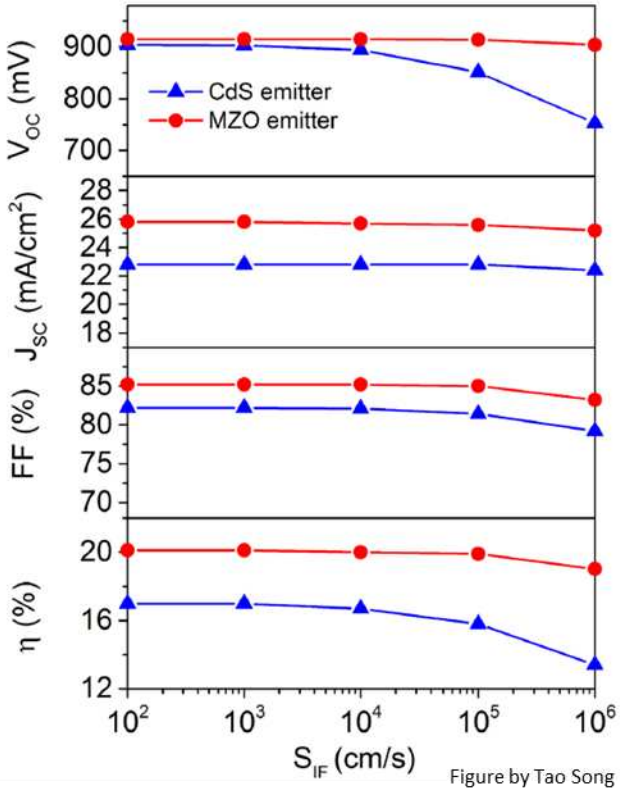


Figure 69: Calculated performance parameters as a function of interface recombination velocity with two practical emitters: CdS (E_g=2.4 eV, ΔE_c = -0.1eV) and MZO (E_g=3.7eV, ΔE_c = +0.2 eV). Figure 69 is Figure 10 from reference (103).

3.6.3.3. MZO/CdTe IRV effects on ER concept

TRPL analysis, modeling, and experimental results suggest that polycrystalline CdTe cells have inherently high (10^5 cm s^{-1}) IRV. Modeling and experimental results suggest that this may be detrimental to the ER effect and limit voltage gains. Figure 70 shows modeling done by Tao Song of an ER structure with and without ~$2*10^5$ cm s^{-1} IRV at the front interface. The CBO spike associated with MZO reduces the IRV effects compared to CdS. Assuming the bulk lifetime is sufficiently high (>10 ns), the MZO/CdTe interface (with ~$2*10^5$ cm s^{-1} IRV) shows a 100 mV improvement in V_{oc}. Suggesting that if the CdTe/CMT interface was improved the ER effect could partially be seen even with ~$2*10^5$ cm s^{-1} IRV at the front MZO/CdTe interface.

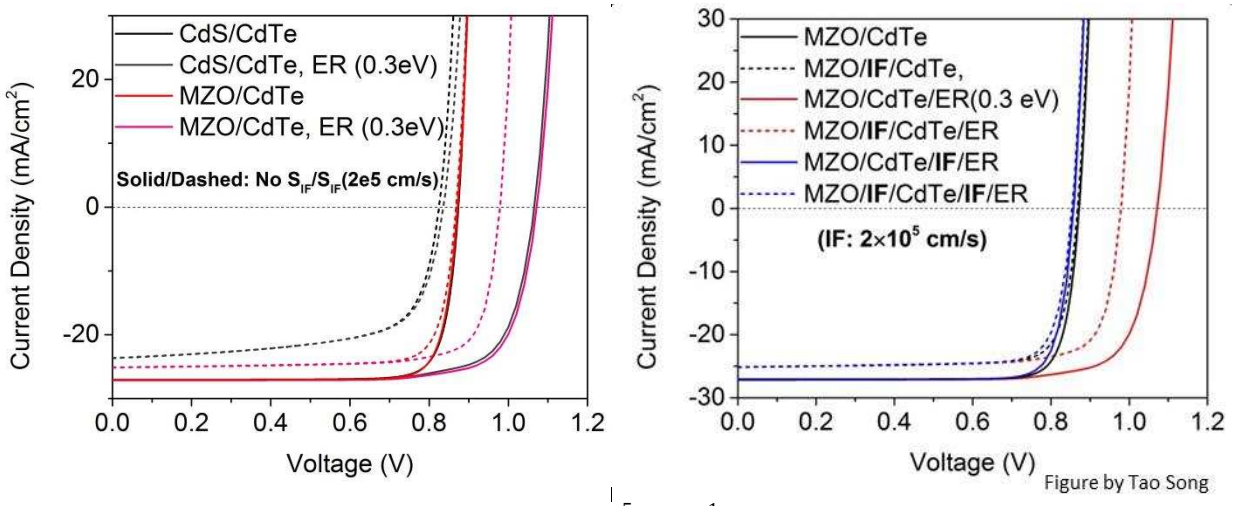


Figure 70: Modeling predicting the effects of 10^5 cm s^{-1} IRV at various key interfaces with CdS and MZO window layers. No performance improvement is predicted with 10^5 cm s^{-1} IRV at the CdTe/CMT interface.

3.7. Co-Sublimation Integrated into the ARDS

The integration of co-sublimation technology into the ARDS was in collaboration with Davis Hemengway, Jason Kephart, Kevan Cameron, Carey Reich, Kurt Bath, and W.S. Sampath, a specific thanks to Davis for design and CAD work and Jason for the magnesium shutter and controls development.

Section 3.5.3.3 hypothesized that if the CMT/CdTe IRV was significantly reduced, similar to what was shown by ASU (32), an improved ER effect could still be seen despite the high IRV of the MZO/CdTe interface. To improve the CMT/CdTe interface removing the need for vacuum breaks at critical interfaces can be achieved by integrating the co-sublimation (co-sub) technology into the ARDS described in Section 2.1. This would allow the CMT layer to be deposited directly after the CdTe layer without breaking vacuum. Figure 71 shows the completed ARDS Co-Sub source.

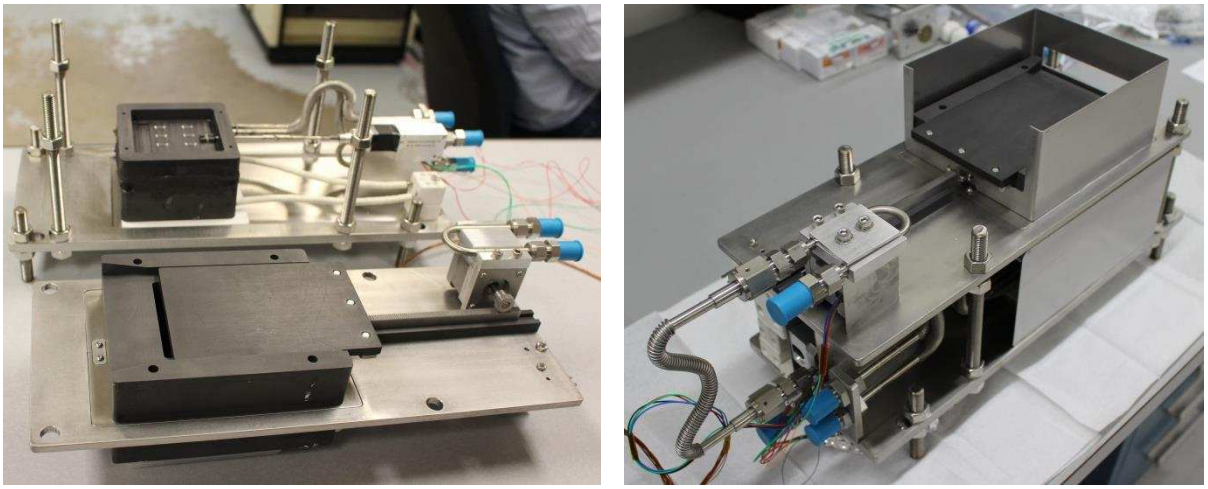


Figure 71: Images of ARDS Co-Sub design, (left) Magnesium and CdTe sources shown separately (right) the completed co-sub source.

Several changes were incorporated into the co-sub for incorporation to the ARDS. The CdTe will react with magnesium and cease to sublimate if the magnesium flux is present and the top shutter is closed. Thus the top shutter was independently controlled using a rack and pinion design. The magnesium shutter was imbedded into the magnesium pocket with a Zaber linear actuator (T-NA08A25-SV2) controlling the small movements of the magnesium shutter depicted in Figure 72. The shutter base (Figure 71 in orange) with machined slots is fixed inside the magnesium pocket. The shutter slide (Figure 71 in green) moves in and out of the page relative

to the base. This motion opens and closes the slots relative to each other, effectively shuttering the magnesium flux.

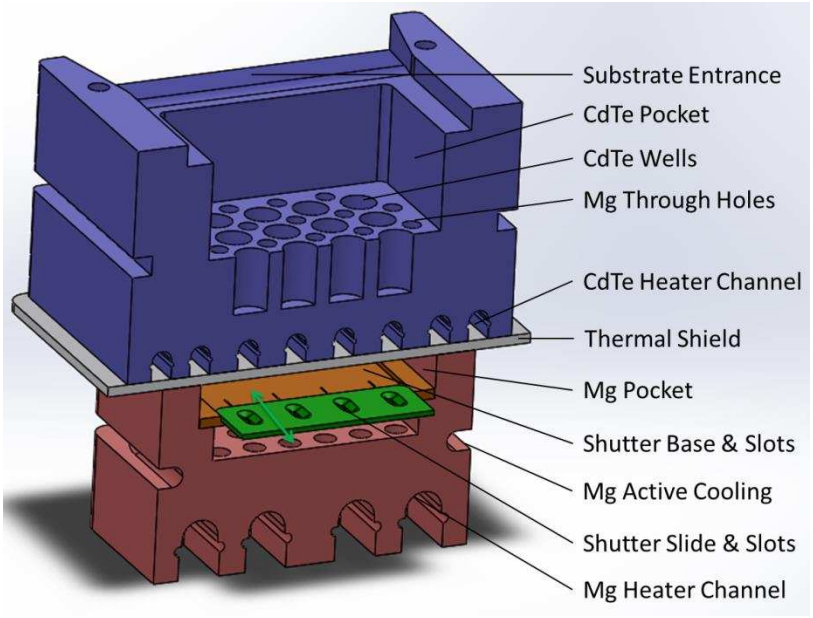


Figure 72: CAD of ARDS Co-Sublimation design with the magnesium shutter design in orange and green.

Figure 73 shows experimental data from the ARDS co-sublimation hardware. The co-sub source was loaded with magnesium for deposition of CdMgTe films. The source was calibrated with the shutter at the 100% open position to a band gap of 2.3 (red) and 2.05 (blue). Since the magnesium flux is a function of the bottom source temperature and the shutter position, Figure 73 (right) normalizes the data by plotting the percent change from 1.5 to the calibrated band gap at 100% open shutter position. Set points were swept in both directions showing no significant signs of hysteresis. The ARDS Co-Sub hardware shows a reliable and consistent ability to deposit various band gaps of CdMgTe between 1.5 and 2.3 eV, similar to previous work.

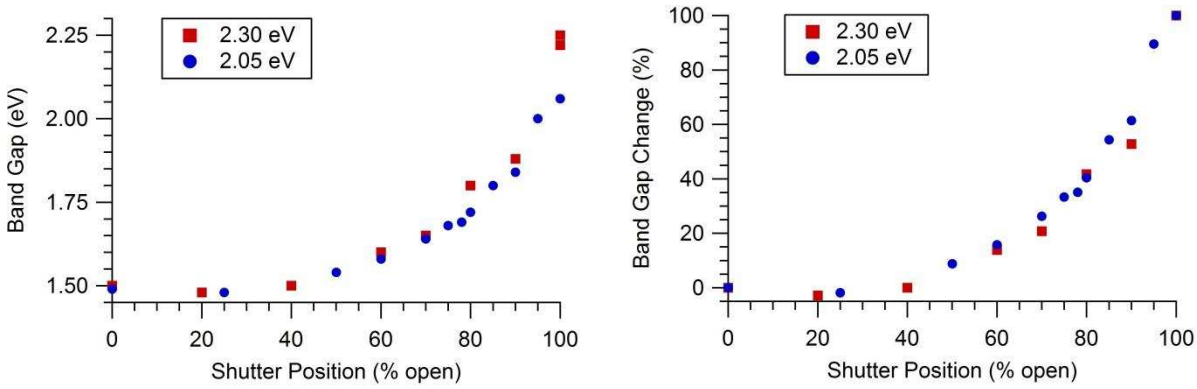


Figure 73: (left) Band gap vs. shutter position, (right) Band gap percent change vs shutter position. (Legend refers to band gap at 100% open shutter position)

4. $CdSe_xTe_{1-x}$

As described in Section 1.3.1, there is an alternative structure to achieve an electron reflector effect. By reducing the band gap of the bulk absorber while keeping the band gap of the back contact unchanged. Thus reduce the CdTe band gap and leave CdTe as the back contact, a Type ER structure. Reducing the band gap of the CdTe absorber can be achieved by alloying with group II and VI elements: Mercury, Sulfur, and Selenium (106; 107; 108; 109; 110). Sulfur alloying is commonly seen in our CdTe manufacturing process, sulfur will diffuse from the CdS to the CdTe during the $CdCl_2$ process, as described in Section 2.2. This sulfur diffusion decreases the band gap, leading to a reduction in bulk band gap of ~0.03 eV, Figure 74. This reduction needs to be increased, to do this other elements such as selenium and mercury can be used.

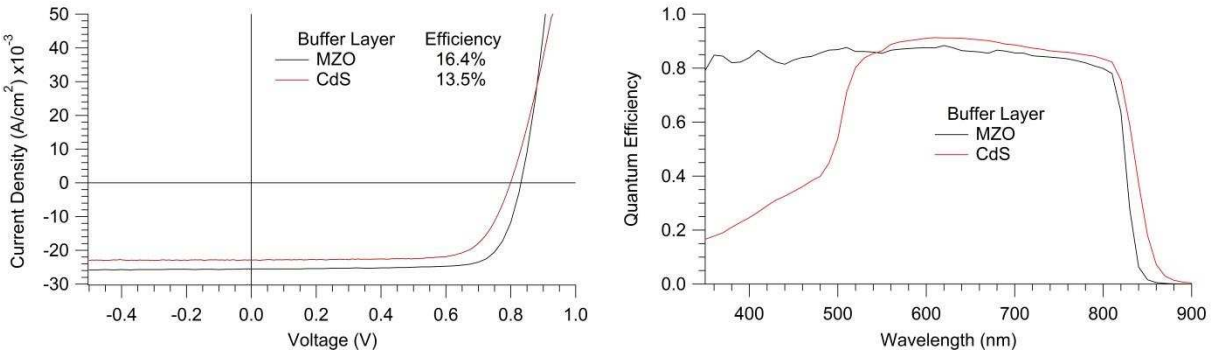


Figure 74: QE of a CdS/CdTe and MZO/CdTe cell

4.1. Sputtered CdSe (Annealed CdSeTe)

It has been proposed by the University of Toledo to use sputtered CdSe as a buffer layer between the front contact/n-type layer and the CdTe absorber (111). This buffer will diffuse selenium into the CdTe layer lowering the band gap of the front absorber and building our Type B structure with $CdSe_xTe_{1-x}$. Figure 75 shows the material structure for this sputtered CdSe cell.

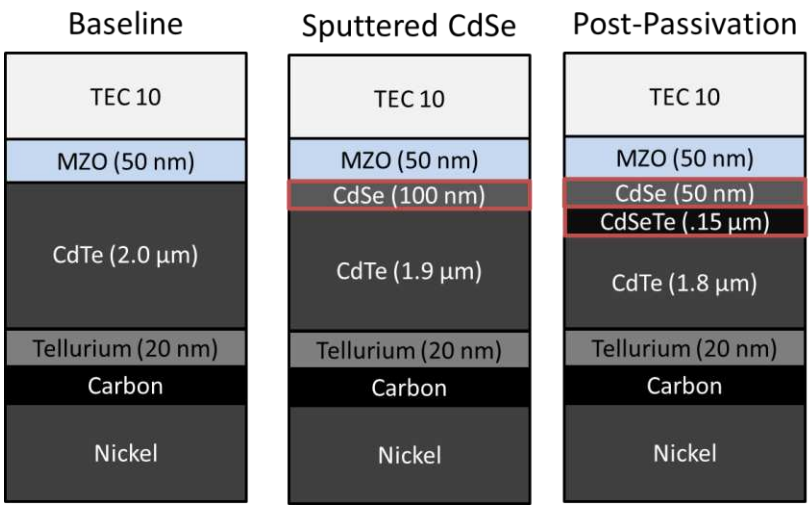


Figure 75: Baseline and Sputtered CdSe Structures

Similar to UT's work (111) an optimization sweep of this CdSe layer was performed. The CdSe was sputtered at 15 mTorr, in Ar gas at 80W RF power, sweeping from 0 to 300nm of sputtered CdSe. The cells then went through the standard deposition, passivation and doping processes utilized at CSU (63). As Figure 76 shows, as the CdSe thickness increases from 0-300 nm the band edge sweeps out at the low energy region, decreasing the band gap of the absorber. At 75 nm CdSe thickness the V_{oc} increases and continues to increase up to 300 nm. This effect is hypothesized to be due to a passivation effect at the front. However there is an abrupt drop in J_{sc} as the CdSe thickness reaches 100 nm and continues to drop through 300 nm. This is hypothesized to be due to incomplete diffusion of the CdSe layer at the front interface, described below this is likely a non-ideal interface. As the CdSe layer gets thicker only so much selenium can diffuse through the CdTe during the passivation process. As the CdSe gets progressively thicker the bulk properties of the CdSe layer begin to dominate at the front.

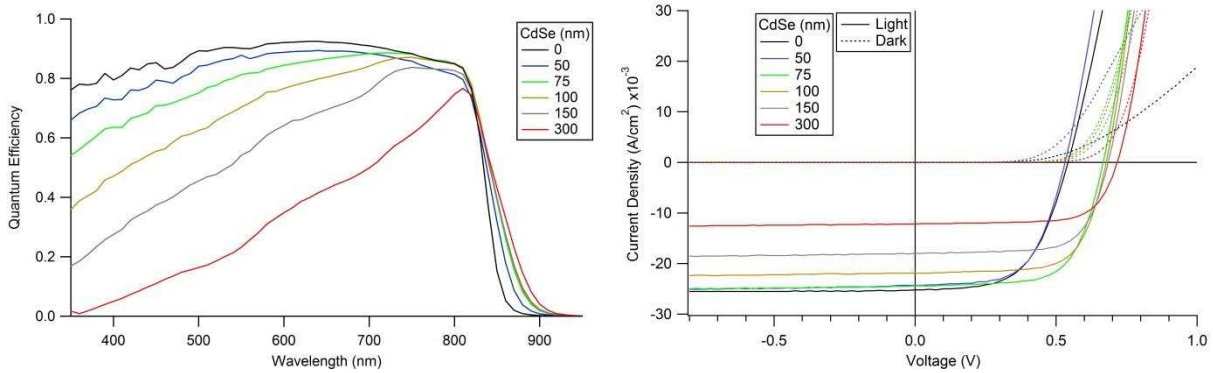


Figure 76: JV and QE of Sputtered CdSe structure with various CdSe thicknesses

With the addition of the CdSe layer a shift in the band edge can be seen in both Figure 76 and Figure 77, this is similar to reported effects by UT. This shift is not consistent, the bottom of the curve shifts more than the top giving a washed out effect, this is associated with a graded band gap. Figure 77b gives the derivative of QE used to establish the band gap of the cell, assuming the max slope point corresponds to the band gap of the cell (112). When using this sputtered CdSe diffusion method, the grading of the material is dependent on the initial concentration of Selenium (the CdSe thickness) and the diffusion time during the $CdCl_2$ treatment. This gives very limited control over band gap and how this band gap is graded.

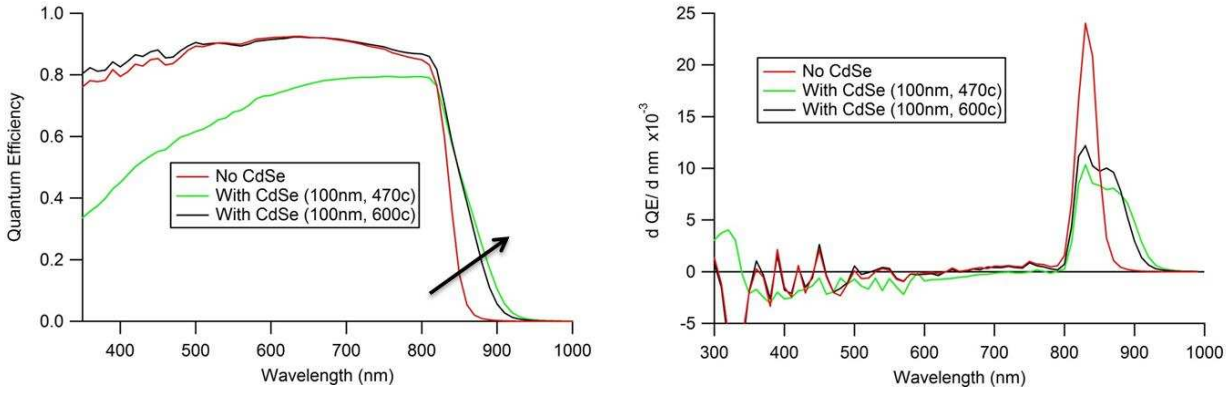


Figure 77: QE and dQE/dnm of CdSe buffered cells

4.2. Co-Sublimation of CdSeTe

The work presented in section 3.3.2. is based on work published in Solar Energy Materials and Solar Cells in collaboration with Jim R. Sites and W. S. Sampath. I'm thankful for funding support from NSF's Accelerating Innovation Research, DOE's SunShot, and NSF's Industry/University Cooperatieve Research Center programs. Assistance with the research from A. Munshi, T. Shimpi, A. Moore, R. Geisthardt, J. Raguse, Kurt Barth, M. D'Ambrosio, C. Moffett, C. Reich, and Lauren Swanson are gratefully acknowledged.

CdTe thin film solar cells have demonstrated efficiencies over 20%, but CdTe has a somewhat higher band gap than optimal for single-junction terrestrial solar-cell power generation. A reduction in the band gap could therefore result in an overall improvement in performance. To reduce the band gap, selenium was alloyed with CdTe using a novel co-sublimation extension of the close-space-sublimation process. Co-sublimated layers of CdSeTe with various selenium concentrations were characterized for optical absorption and atomic concentrations, as well as to track changes in their morphology and crystallinity. The lower band-gap CdSeTe films were then incorporated into the front of CdTe cells. This two-layer band-gap structure demonstrated higher current collection and increased quantum efficiency at longer wavelengths.

4.2.1. Introduction to CSS of CdSeTe

Geisthardt et al., further characterized the potential of the CdTe technology with an analysis of performance limits under various real world conditions theorizing fundamental limits of the technology (43). This model projected that if the CdTe band gap were reduced from 1.5

eV to 1.38 eV, the increase in current would more than compensate for the voltage and fill-factor reductions and result in a net increase in efficiency.

A reduction in the CdTe band gap has been demonstrated through selenium alloying (113; 110), reducing the band gap of CdTe to 1.39 eV (114). Paudel and Yan showed that by sputtering CdSe between the front contact and CdTe layers a cadmium selenium telluride (CdSeTe) layer was formed during the $CdCl_2$ process (111). The addition of this CdSeTe layer resulted in improved current collection at long wavelengths. The sputtered CdSe technique was dependent on diffusion of selenium from the CdSe sputtered layer. Since CdSe likely causes poor cell performance in this structure, the sputtered CdSe layer must be fully defused into CdTe forming CdSeTe. Thus the sputtered CdSe layer acted as a selenium reservoir while the $CdCl_2$ passivation drove the diffusion of selenium into the CdTe layer. This method makes more complicated band gap gradings or the formation of uniform single band gaps below 1.5 eV difficult.

This paper will study the material and electrical properties of as-deposited CdSeTe alloys, demonstrating control over the selenium alloying. As-deposited single band-gap CdSeTe alloys will be used for characterization to assess material changes as the selenium incorporation is increased. Finally the single band gap CdSeTe layer will be deposited at the front of a CdTe cell to assess increased current collection at longer wavelengths.

4.2.2. Co-Sublimation Hardware and Characterization

Co-sublimation technology has been developed at Colorado State University to allow CdTe to be alloyed with magnesium (86). This technology has now been further developed to incorporate selenium in place of magnesium to allow for the controllable deposition of CdSeTe.

This enhanced hardware (Figure 78) includes additional transfer holes around the perimeter of the CdTe source to improve band gap uniformity across the film. Due to the increased vapor pressure of selenium (38) active water cooling was added to the selenium bottom source to maintain a reduced operating temperature. To allow the selenium flux to be quickly turned on or off, a shutter was added above the selenium source. All CdSeTe films were deposited on Pilkington Tec10 substrates with a magnesium zinc oxide (MZO) buffer layer (38; 45). This 100-nm buffer layer was RF-sputtered onto the substrate at room temperature with a magnesium composition of x=0.25 in the film. The MZO was used in place of CdS for increased current collection and improved band alignment in CdTe cells (45). These substrates with the 100-nm MZO buffer layers were used for all characterization films and device.

Optical properties of the CdSeTe films were analyzed with a Mikropack DH-2000-BAL UV-VIS-NIR light source and an Ocean Optics USB4000-VIS-NIR spectrometer. Band gaps were calculated using the Tauc plot method, where $(\alpha h\lambda)^2$ was plotted against photon energy, $h\nu$, and the linear portion of $(\alpha h\lambda)^2$ was extrapolated to where $\alpha=0$ cm^{-1} (i.e., the x-axis). A JOEL JSM-6500F field emission scanning electron microscope (SEM) and a Nanoscience atomic-force microscope (AFM) were used for morphology and imaging. Film composition was derived from energy dispersive x-ray spectroscopy (EDS) and a PE-5800 x-ray photoelectron spectroscopy (XPS). XPS samples received a 120 second, 5kV sputter cleaning treatment to remove carbon and oxide peaks typical of surface contamination. Glancing angle x-ray diffraction (GAXRD) was performed at an incidence of 1.5^o with a Bruker D-8 Discover utilizing Cu K_α radiation (λ=1.542 Å). Standard current-voltage and quantum efficiency facilities were used for cell-performance and characterization

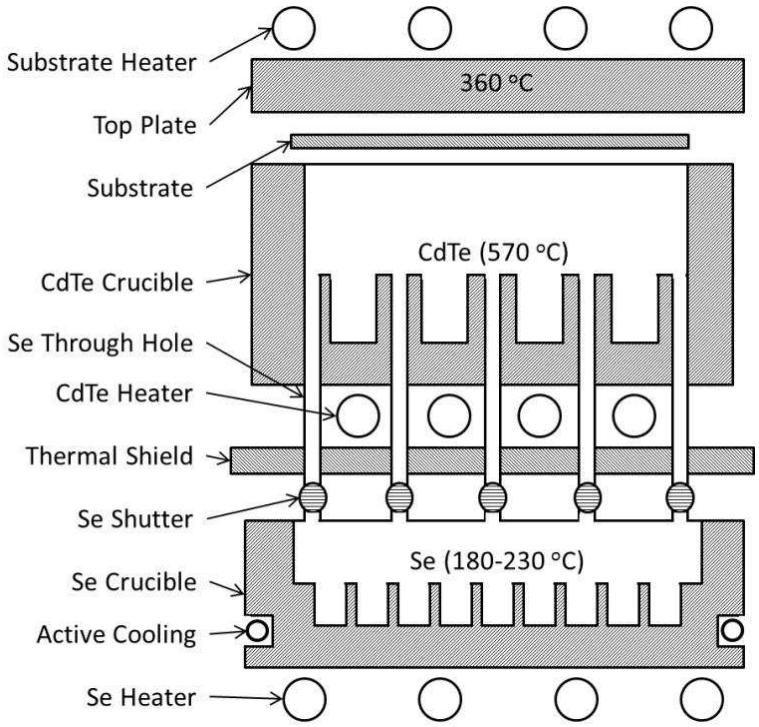


Figure 78: Co-sublimation hardware for alloying CdTe and selenium (Gen IV). The selenium vapor pressure is directed into the CdTe pocket to allow sublimation of the alloy.

4.2.3. CdSeTe Films

4.2.3.1. Composition

The co-sublimation source in Figure 78 allows the band gap of the CdSeTe film to be controlled though the amount of selenium flux from the bottom source by controlling its temperature. Figure 79a shows a set of transmission curves for ~1.0 µm thick CdSeTe films deposited at various selenium source temperatures. As the selenium source temperature is increased, the transmission curves shift to the right, which indicates a decrease in band gap by as much as 80 meV. Tauc-plot analysis was conducted on these curves over a selenium-source temperature range from 180 ^{o}C to 227.5 ^{o}C. Figure 79b gives the resulting band gap vs. selenium source temperature, demonstrating the controllably of the co-sublimation hardware for CdSeTe deposition. The band gaps deduced from the transmission curves decreased CdTe at 1.5 eV to

approximately 1.4 eV, then rose sharply towards the CdSe band gap at 1.7 eV. This change in band gap with increasing selenium concentration is consistent with previous CdSeTe materials reported in the literature (114).

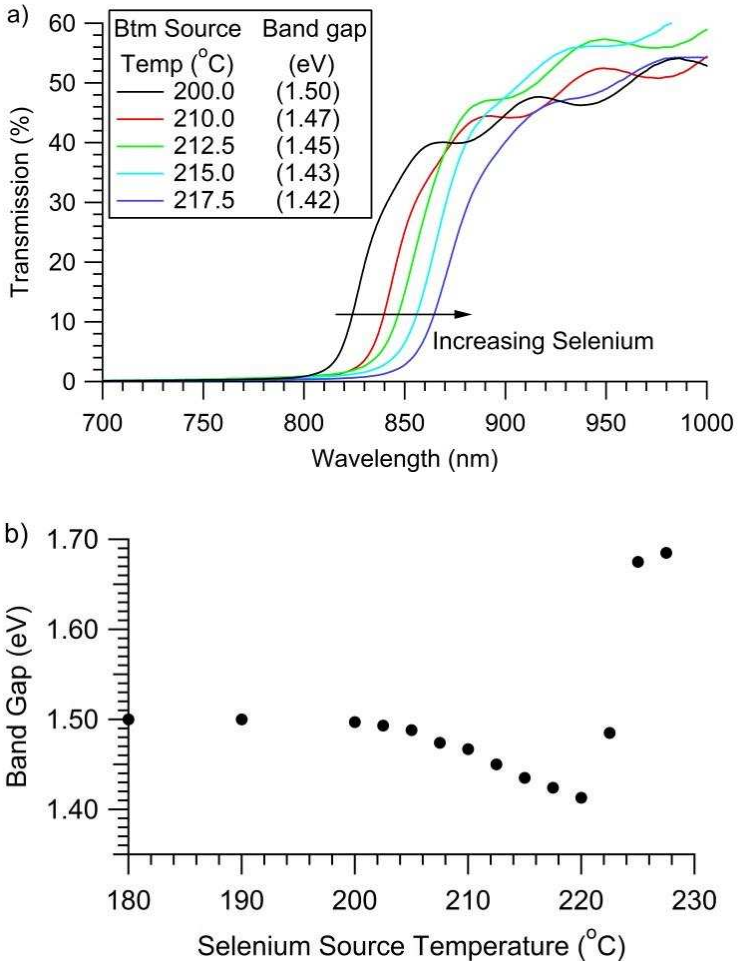


Figure 79: a) Optical transmission of CdSeTe films at various selenium bottom source temperatures b) Tauc-plot-calculated band gaps vs. selenium source temperatures. As the selenium source temperature is increased, the selenium vapor flux is increased and the CdSeTe band gap first decreases, than rises sharply.

The reduction in band gap of CdSeTe compared to 1.5 eV CdTe or 1.7 eV CdSe is due to band gap-bowing (113). X-ray photoelectron spectroscopy (XPS) and electron-diffraction spectroscopy (EDS) were performed for elemental analysis, which allowed the cadmium, tellurium and selenium atomic concentrations to be determined. Figure 80a shows the XPS

atomic concentrations for Cd, Te, and Se at various selenium bottom source temperatures. The 3d5 peak was used to approximate the atomic concentration for Cd and Te, and the 3d peak for selenium. Figure 80b shows the atomic concentrations measured by EDS, which are consistent with the XPS measurements.

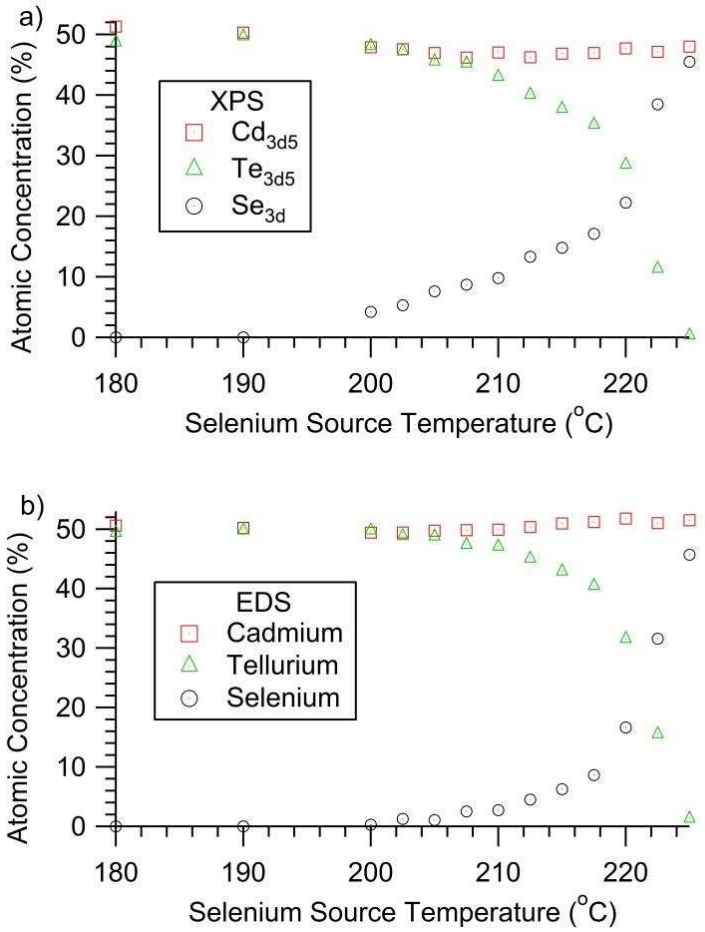


Figure 80: Atomic concentrations of Cd, Te, and Se as measured by a) XPS and b) EDS show increased selenium incorporation at higher temperatures.

Figure 81 combines the band gaps calculated from the absorption curves with the selenium concentrations determined from XPS and EDS. The minimum band gap observed was 1.41 eV at a selenium concentration of x = 0.35 as measured by EDS and x = 0.45 as measured by XPS. These values are consistent with those from hot-wall-deposited and MBE-grown

CdSeTe films (110; 114). The EDS values are believed to be a better representation of the bulk properties, since XPS is more sensitive to surface contamination and subjective to preferential sputtering. The EDS data, which utilized a 15 kV electron excitation beam, should therefore be close to the bulk characterization, and further analysis below will use the EDS concentrations. Note that the CdSeTe concentrations become highly sensitive to source temperatures above 220 ^{o}C.

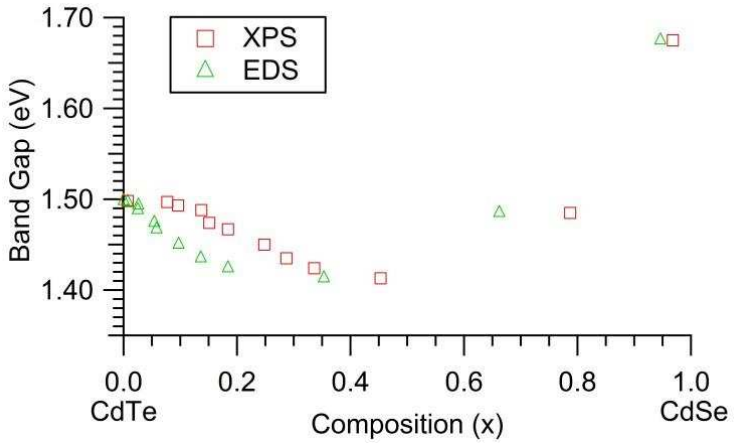


Figure 81: CdSeTe band gap as a function of selenium concentration as measured by XPS and EDS.

4.2.3.2. Morphology

The surface morphology of the CdSeTe film changes as the selenium concentration is increased. Figure 82 shows scanning electron microscope images of the CdSeTe deposited film with varying selenium concentrations. At x = 0.14 the grains become more faceted and tightly packed, and as x is increased to 0.36, the faceted nature of the grains remains with a minor reduction in grain size. Note x = 0.36 should be approaching the optimal band gap for a single junction solar cell. As the selenium concentration is increased to x = 0.66 the grains appear to further reduce in size and begin losing the faceted feature. AFM measurements show similar

morphology changes to SEM with an increase in the RMS roughness from x = 0.4 to 1.0 as presented in Table 6.

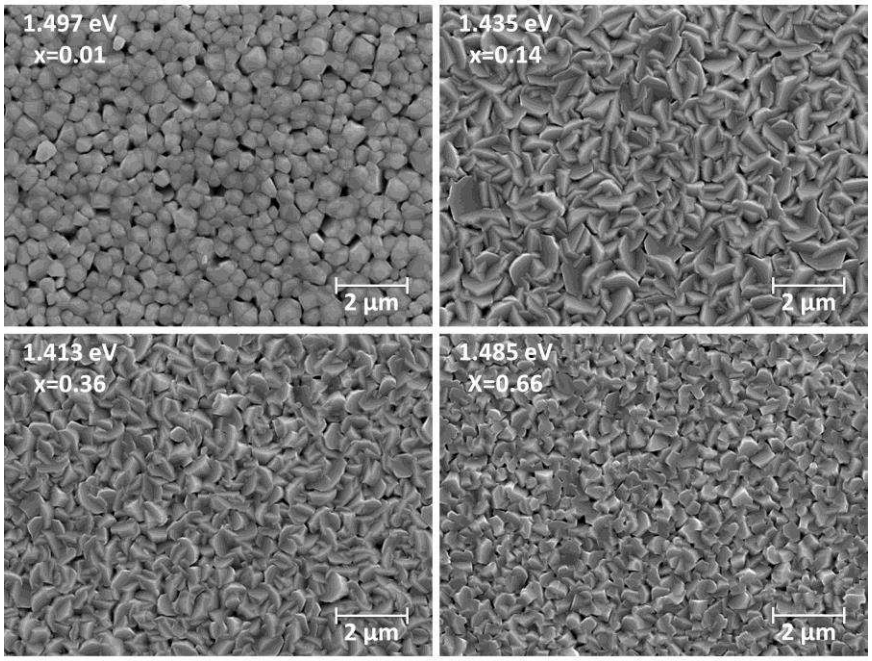


Figure 82: SEM images at x= 0.01, 0.14, 0.36, and 0.66. A clear change in morphology is seen as the selenium concentration is increased. Se concentration x is estimated from EDS.

Table 6: RMS Roughness vs Selenium concentration (x)

Se (x)	*0.01 - 0.37*	*0.54*	*0.72*	*0.95*	*0.97*
RMS (nm)	38 - 43	51	62	102	125

4.2.3.3. Crystallinity

Figure 83 gives glancing angle XRD of films with a varying selenium concentrations over the full range from x = 0 to 1. Key peaks are identified, and it is seen that the dominant orientation of the CdTe grown on MZO is 111 with very small peaks at 220 and 311. Figure 84 shows an expanded view of the 111 peak as a function of selenium concentration. As the selenium alloying is increased from x = 0 to 0.35, the 111 peak shifts to the right, indicative of band bowing as the lattice constant for the CdSeTe material moves towards the CdSe zinc-blend

limit. At x near 0.6, however, the material shifts structure from cubic zinc-blende to hexagonal wurtzite (44). This is identified by the development of the peak at $2\theta = 45.6^{o}$, which corresponds to the CdSe 103 peak. The 111 peak intensity decreases up to x = 0.35, and when the material becomes hexagonal, the CdTe 111 peak is replaced by a CdSe 002 peak near the previous CdTe 111 location. The CdSe 103 peak then increases in intensity as the material approaches CdSe. At x = 0.35, the material has the lowest band gap seen in this study, and the CdSe 103 and 112 peaks have begun to appear suggesting that the structural phase transition is under way. Theoretically a band gap of 1.38 eV is desired (43), but mixing of CdTe cubic zinc-blende and CdSeTe hexagonal wurtzite interface may limit the band-gap decrease.

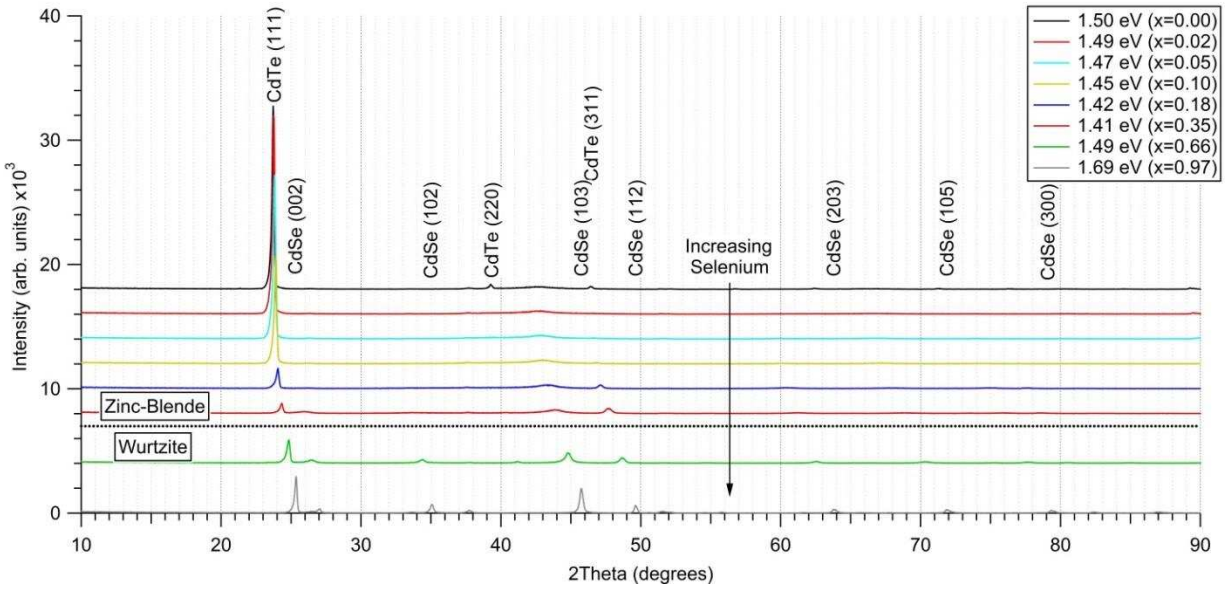


Figure 83: Glancing Angle (1.5^{o}) XRD at varying selenium concentrations, showing the shift from a cubic to hexagonal structure.

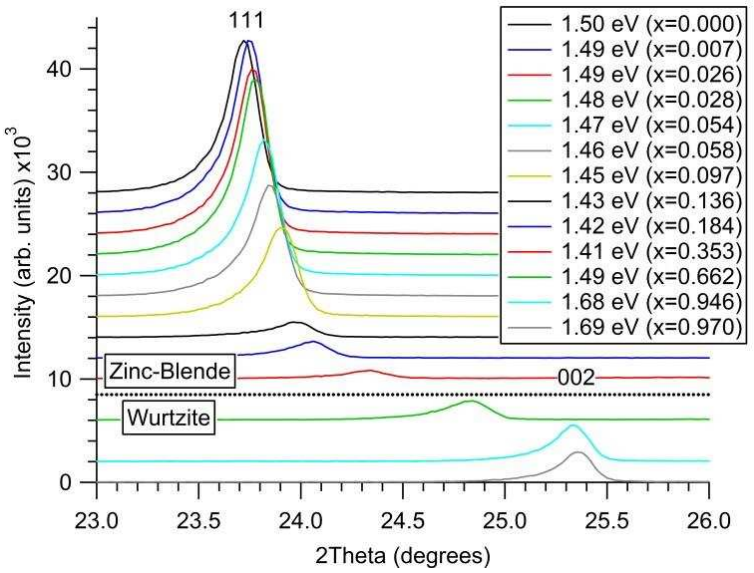


Figure 84: 111 XRD peak with varying selenium concentration. The 111 peak shifts to the right as the selenium concentration is increased, then disappears at the structural transition.

The lattice constant a_o for the cubic structure is calculated using Equation 5 and lattice constants a_o and c_o for the hexagonal structure using Equation 6. The lattice constants are calculated using the miller indices (hkl), peak location θ, and the wavelength of the incident x-ray beam ($\lambda_{K\alpha 1,cu}$ = 1.5405Å). Figure 85 gives the calculated lattice constant of CdSeTe films from x = 0 to 0.35, where the film is believed to be cubic. The lattice constant decreases from CdTe at 6.48Å (zinc-blende) towards CdSe at 6.08Å (zinc-blende) until the film becomes hexagonal (115; 55). Table **7** gives the calculated lattice constants above x = 0.60 with literature values for hexagonal CdSe.

$$Sin^2(\theta) = \frac{\lambda^2}{4a_o^2}(h^2 + k^2 + l^2) \quad (5)$$

$$Sin^2(\theta) = \frac{\lambda^2}{4}\left(\frac{4}{3}\left(\frac{h^2+hk+k^2}{a_o^2}\right) + \frac{l^2}{c_o^2}\right) \quad (6)$$

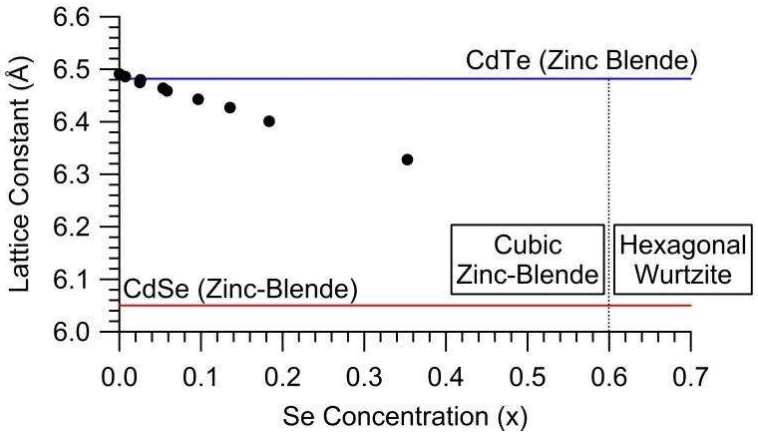


Figure 85: Lattice constant (a_o) calculated from XRD as a function of selenium concentration (x) with CdTe (Zinc-Blende) and CdSe (Zinc-Blende) referenced (116)

Table 7: XRD lattice constants calculated after material shifts to wurtzite, *literature given values **(116)**.

x	*2θ (deg)*	*d(103)*	a_o	*d(002)*	c_o
0.66	24.8	2.021	4.385	3.581	7.162
0.94	25.3	1.983	4.305	3.512	7.023
0.96	25.4	1.981	4.301	3.509	7.018
1.0*	-	-	**4.300**	-	**7.010**

4.2.4. CdSeTe Cell Performance

4.2.4.1. CdSeTe/CdTe Device Fabrication

The co-sublimated hardware has demonstrated an ability to deposit CdSeTe films at various band gaps with a high level of control. To demonstrate increased current collection at higher wavelengths, these lower band gap CdSeTe films were incorporated between the Tec10/MZO and CdTe layers, similar to the sputter CdSe process (111). The CdSeTe/CdTe cells were then processed using CSU's standard techniques (38). No re-optimization of the process conditions, including the Cl passivation, was performed. Figure 86 shows the CdSeTe/CdTe cell structure that was fabricated. The baseline CdTe solar cell was deposited at CSU using its

standard inline close-space-sublimation technology (38). In this research, a MZO front contact was used instead of the traditional CdS layer to improve the current collection and a tellurium back contact is used in place of carbon paint (38; 44; 74). The tellurium back contact was evaporated at 10^{-5} Torr at 1 nm/s. CdSeTe layers were co-sublimated at 10 nm/s onto the Tec 10/MZO substrate at a temperature of 470 ^{o}C in a 40 mTorr argon environment. The thickness of the CdSeTe layer was varied from 0 to 400 nm for each of the three discrete band gaps: 1.47, 1.45, and 1.41 eV. The MZO/CdSeTe film was then re-inserted in the primary chamber, where it was heated to 470 ^{o}C and the CdTe, $CdCl_2$ and copper doping steps were completed, as described previously (38).

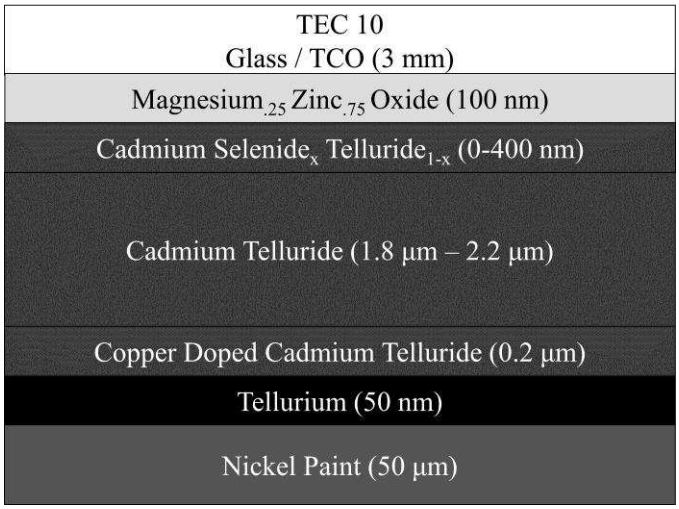


Figure 86: CdSeTe/CdTe structure to assess the CdSeTe ability to collect photons below 820 nm.

Cross section TEM and EDS is performed on the CdSeTe/CdTe structure with a 400 nm 1.45 eV CdSeTe layer. Figure 87 shows a cross section TEM images using methods described in Section 2.2 and 3.4, the images were collected by Ali Abbas at Loughborough University. The grain size is ~0.5 - 1.0 μm in size, which has been shown to be small for this described manufacturing process (70). Fill factor may be increased by increasing grain size through increased substrate temperature (~470 to 600 ^{o}C). There is no abrupt interface between the

CdSeTe and CdTe layers. A white line is marked in Figure 87 to show the CdSeTe/CdTe approximate interface, the CdTe appears to grow epitaxial, with twins and grains spread cross the interface. Figure 88 shows cross section EDS of Figure 87 with elements cadmium, tellurium, selenium, chlorine, and oxygen. There is selenium diffusion from the CdSeTe layer to the CdTe likely during the reheat or $CdCl_2$ step. The selenium appears to be diffusing down in the bulk of the material as well as down the grain boundaries. The selenium diffusion appears enhanced at the grains boundaries in comparison to the bulk. The chlorine signature is significantly reduced compared to previous work (55). There may be opposing diffusion effects between the Chlorine and Selenium.

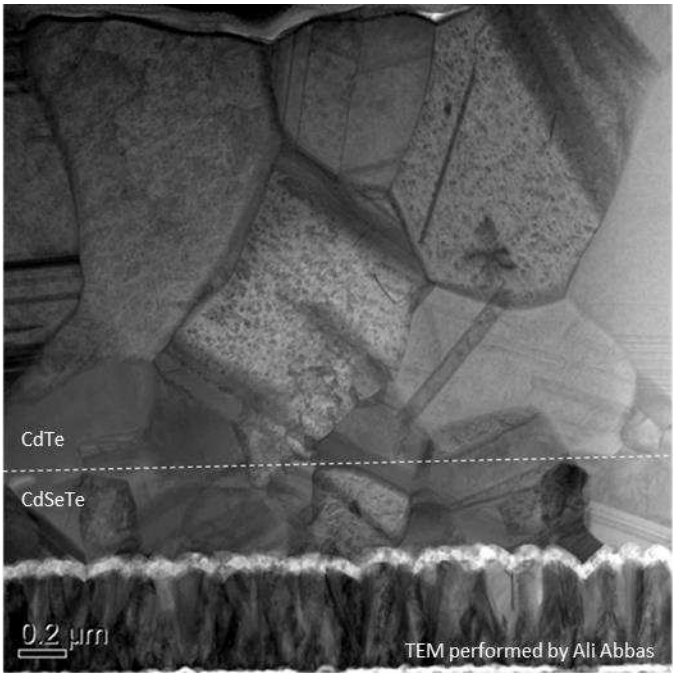


Figure 87 Cross section TEM of a 400 nm 1.45 eV CdSeTe/CdTe device using standard process conditions described in Section 2. A dashed white line represents the approximate CdSeTe/CdTe interface.

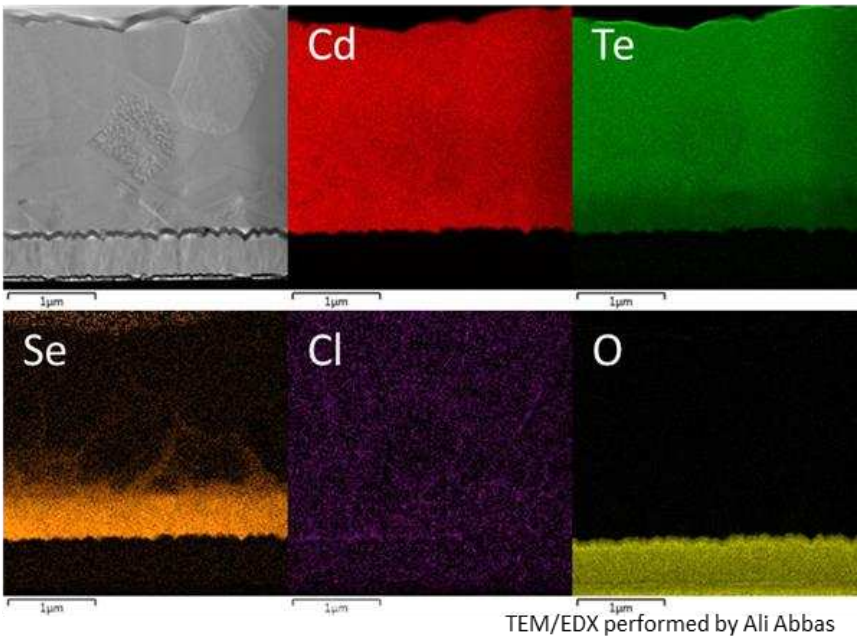


Figure 88 Cross section EDS of a 400 nm 1.45 eV CdSeTe/CdTe device.

4.2.4.2. CdSeTe/CdTe Cell Performance

Figure 89 shows the average J-V performance parameters and their standard deviations for cells with three CdSeTe band gaps: 1.47, 1.45, and 1.41 eV at various thicknesses in each case from 0 (a reference cell of CdTe without any CdSeTe layer) to 400 nm. The standard deviation is calculated over the 25 devices measured per substrate. Figure 90 shows representative J-V curves for 1.47, 1.45, and 1.41 eV CdSeTe/CdTe devices with a 200-nm thick CdSeTe layer.

There is a V_{oc} reduction for all band gaps of CdSeTe compared to absorbers with CdTe only, as expected when the front-junction band gap is reduced (43). The V_{oc} was slightly larger at 1.45 eV (810 mV) compared to 1.47 eV (795 mV) or 1.41 eV (750 mV), probably due to a process factor that was not identified. All three band gaps show a consistent increase in performance as the CdSeTe thickness is increased from 25 to 200 nm. This may be associated

with different process optimizations for each set point including $CdCl_2$ passivation and copper doping.

The MZO band alignment can be turned by changing the magnesium content in the MZO film (45). The CdSeTe layer likely has a slightly different band alignment compared to CdTe and may require a new optimization of the magnesium content in the MZO for a MZO/CdSeTe interface (45). The lattice mismatch between layers may also be affecting the overall performance. The CdSeTe layer could act as a buffer between the lattice mismatched MZO/CdTe interface. The fill-factor (FF) shows a similar trend to V_{oc}, and reaches values similar to the reference cells when it is at 200 nm and 1.45 eV.

The short circuit current shows an increase from 24.5 to 26.0 mA/cm^2 as CdSeTe thickness increases from 0 to 400 nm at 1.45 eV and similarly for 1.47 eV. This is consistent with an increased absorption of the reduced band-gap CdSeTe layer and is evidence that the collection efficiency of the CdSeTe is reasonably good. The cells with 1.41eV CdSeTe began to show comparable current collection (24.0 mA/cm^2) at 100 nm, but decreased dramatically (to 15.4 mA/cm^2) at 400 nm.

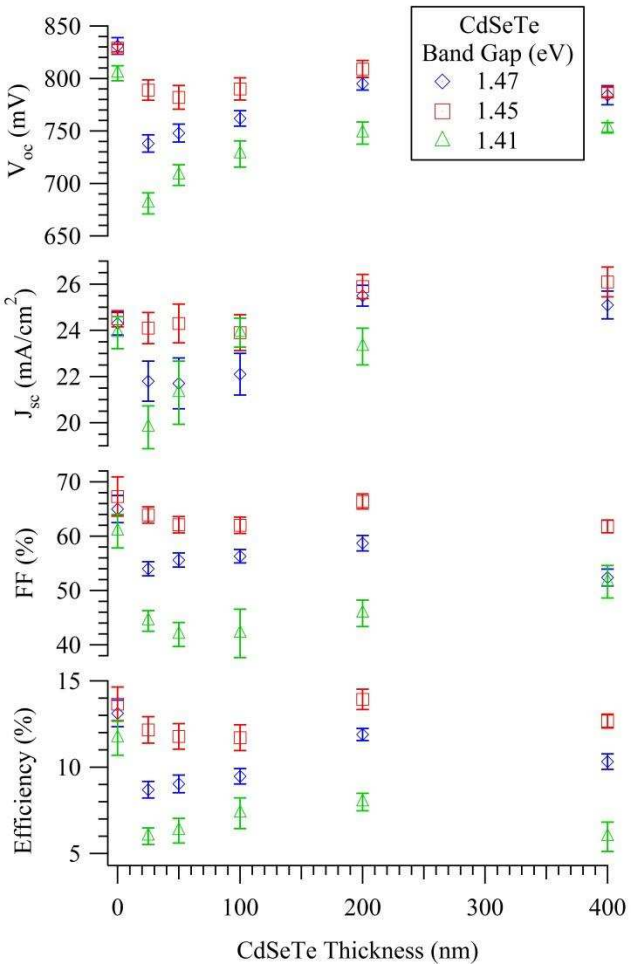


Figure 89: JV performance parameters of MZO/CdSeTe/CdTe devices with the CdSeTe layer at1.47, 1.45, and 1.41 eV. The CdSeTe thickness is swept from 0 – 400nm. Average device values are used with a plus/minus one standard deviation error bar. J_{sc} at 1.41 eV and 400 nm is 15.4 mA/cm^2.

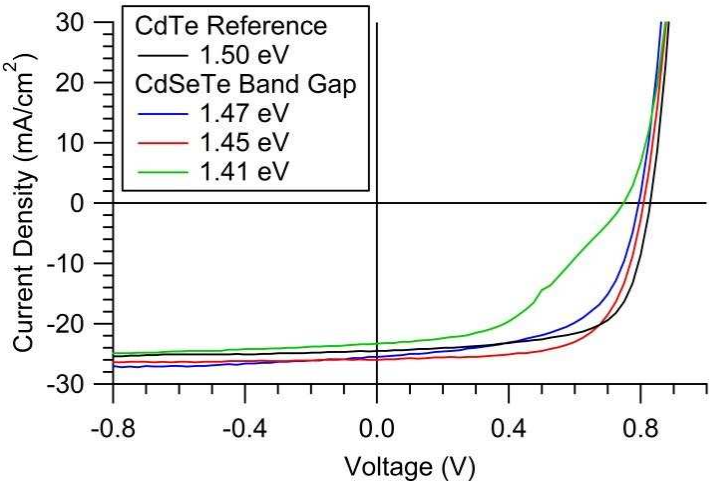


Figure 90: JV of 1.47, 1.45, and 1.41 eV CdSeTe/CdTe cells at 200 nm CdSeTe thicknesses.

The 1.41 eV CdSeTe cells showed inferior performance to the others with reductions in V_{oc}, FF and J_{sc}. This may be because as the CdSeTe material approaches 1.41 eV, the film is starting to transition from the cubic zinc-blende structure to the hexagonal wurtzite structure as shown by XRD, which is likely not ideal for an interface with the cubic zinc-blende CdTe. Increased CdTe/CdSeTe interface recombination may potentially reduce the performance at 1.41 eV as the materials crystallinity changes. Maintaining a cubic structure as the CdSeTe band gap is minimized may prove critical for maintaining performance improvement.

Figure 91 shows the quantum efficiency (QE) of the cells with 1.45-eV band-gap CdSeTe layers at various thicknesses from 0 to 400 nm. As the CdSeTe layer thickness is increased, a shift in the absorbed band edge can be seen at ~850 nm. The increased absorption of the CdSeTe layers at lower wavelengths is indicative of a lower absorber material. The integrity of the lower band-gap CdSeTe was maintained through the passivation process and it clearly contributes to current collection. The QE derived band gaps are calculated by taking the max negative derivative of the QE curves (112). The QE derived band gaps are tabulated in Table 8 with the band gaps from optical absorption as reference. The Tauc plot measurements and derived QE

band gaps give similar values. Tauc plots are measured prior to CdTe deposition and $CdCl_2$ passivation while QE derived band gaps are measured on completed devices. The agreement between the two implies that the reduced band gap of the CdSeTe layers is maintained.

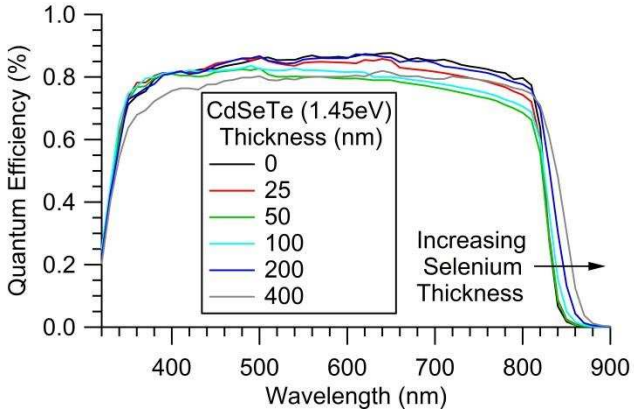


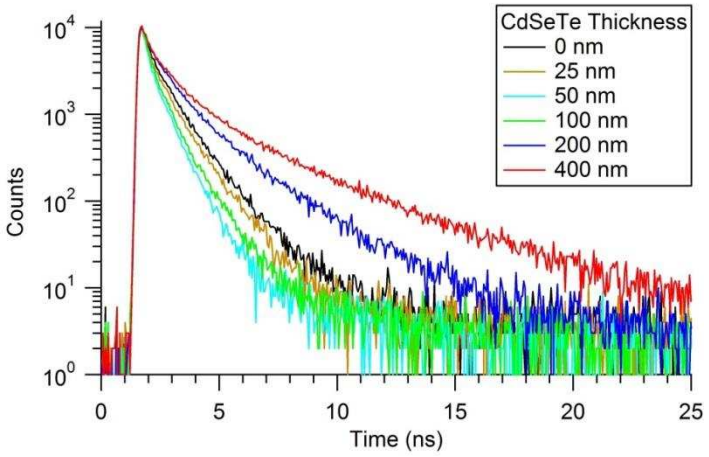
Figure 91: QE of 1.45eV CdSeTe/CdTe cells at various CdSeTe thicknesses. Greater photon collection above 840 nm is seen with increasing CdSeTe thickness.

Table 8: Calculated band gaps (eV) of the minimum bulk absorber from integrating the QE at various CdSeTe thickness (nm) **(112)**. The measured tauc plot band gaps are listed for reference and the max J_{sc} measured from JV and QE integration.

	QE Derived Band Gaps (eV)							*J_{sc} (mA/cm^2)*		
	CdSeTe Thickness (nm)							QE	JV	JV
Se (x)	**0 nm**	**25 nm**	**50 nm**	**100 nm**	**200 nm**	**400 nm**	Tauc	**200 nm**		**0 nm**
0.05	1.51	1.51	1.51	1.51	1.50	1.47	1.47	25.0	25.5	24.3
0.10	1.51	1.50	1.50	1.50	1.48	1.46	1.45	25.7	26.0	24.5
0.36	1.51	1.49	1.49	1.49	1.43	1.41	1.41	23.4	23.3	23.9

Time Resolved Photo-luminesces (TRPL) at conditions described in Section 3.6 was performed to characterize changes in lifetime of the 1.45 eV CdSeTe/CdTe cells. Figure 92 shows the TRPL with increasing CdSeTe (CST) thickness. The reference cell and 25 nm CST cell appear to be comparable, likely not substantially affecting the band diagram or interface

recombination velocity. There is a drop in performance at 50 and 100 nm, believed to be due to non-ideal process condition, likely the passivation process. This lifetime reduction correlates with the JV performance parameters shown in Figure 89. At a CST thickness of 200 and 400 nm, there is a substantial increase in lifetime as compared to the 0 nm reference. The increase in lifetime does not correlate with voltage. The similar structure of CST and CdTe along with the lack of performance increase till 200 nm CST thickness implies the lifetime improvement may not be because of the interface. Similar to the increased substrate temperature work (70) the increase in lifetime with marginal improvement in voltage may be indicative of a bulk lifetime improvement opposed to an interface recombination velocity improvement. CST double-hetero structures, similar to cells analyzed in Section 3.5 may give a more complete understanding. Note that the V_{oc} may be comparable between the CdSeTe device and CdTe reference but the voltage deficit is reduced. With the voltages remaining the same but the band gap dropping ~.08 eV, that is an 80 mV reduction in the voltage deficit constant with increasing lifetime.



CdSeTe	Bi-Exponential Fit	
Thickness (nm)	Tau 1 (ns)	Tau 2 (ns)
0 (ref)	0.10	1.04
25	0.10	0.96
50	0.10	0.72
100	0.10	0.78
200	0.53	2.17
400	0.68	3.67

Figure 92: TRPL of 1.45eV CdSeTe/CdTe cells at various CdSeTe thicknesses. Improvements in lifetime can be seen as the CdSeTe thickness is increased.

Figure 93 shows temperature dependent J-V on 1.45 eV CdSeTe cells with varying CdSeTe thickness. The reference cell has a slope of -0.002 mV/C consistent with previous work

(112). The x-axis intercept is an approximation of the band gap of the cell. As the CdSeTe thickness increases the x-intercept is increasing and approaching the reference cell. This is in contradiction with the trend shown optically and in QE (Table 8). The contradiction may be connected to the improvement in the voltage deficit. If the x-intercept is viewed as the field strength opposed to band gap the defect density may be affecting the x-intercept. As seen in Figure 92 the addition of CdSeTe passivates the front, improves lifetime of the cell, and reduces the voltage deficit. Figure 93 gives further evidence that the selenium may be acting as a passivation technique.

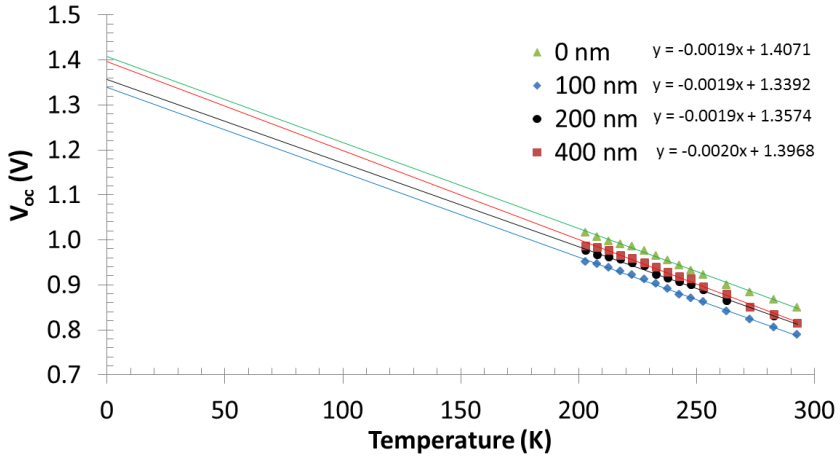


Figure 93: Temperature dependent JV for 1.45 eV CdSeTe cells with varying CdSeTe thickness.

With the incorporation of CdSeTe at the front of a CdTe device changes in doping can affect the performance of the device. C-V measurements were taken to assess potential changes in doping with the incorporation of selenium. Figure 94 shows CV of a 1.45 eV CdSeTe / CdTe cell at various thicknesses of CdSeTe. The bulk absorber thickness was maintained at 2.0 µm. Doping is approximated by assessing the belly of the curve, there appears to be no significant change in doping as the CdSeTe thickness changes. A similar trend was seen for 1.41 and 1.47 eV.

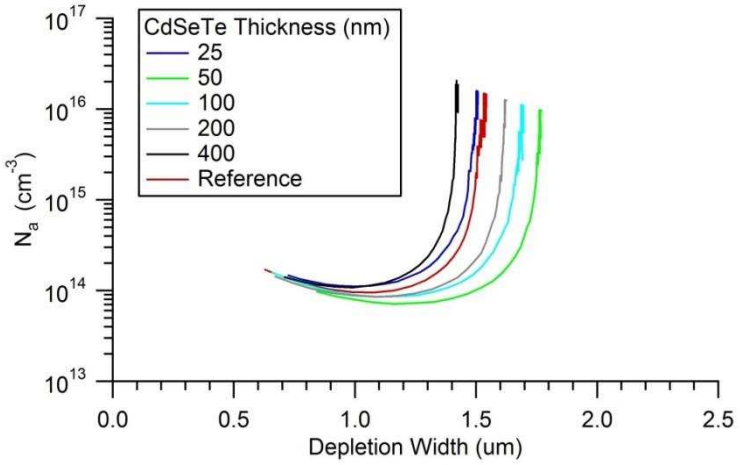


Figure 94: CV of 1.45eV CdSeTe/CdTe cells at various CdSeTe thicknesses.

4.2.5. CSS Deposited CdSeTe Conclusion

Since a reduction in the CdTe band gap from 1.5 to 1.38 eV should result in increased cell current and performance, a new co-sublimation deposition source was developed to manufacture selenium-alloyed CdTe films. Controllable alloying of CdSeTe films was demonstrated and achieved a minimum band gap of 1.41 eV with notable changes to morphology and crystallinity with increasing selenium concentration. Various thickness and selenium concentrations of CdSeTe films were deposited at the front of CdTe solar cells. The lower band-gap CdSeTe/CdTe cells showed a shift in the QE cutoff to longer wavelengths, consistent with measured transmissions curves and demonstrated larger currents with thicker alloy layers. Selenium diffused from the CdSeTe layer into the CdTe grading the CdSeTe/CdTe interface during the passivation process. The addition of the CdSeTe layer shows increases in lifetime as measured with TRPL as well as a reduction in the voltage deficit.

With process optimization efficiency gains are believed to be possible through the integration of CdSeTe films. This layer can be one fixed band gap or further complexity can be

added by grading the selenium content similar to CIGS technology (35). This is possible with the new ARDS Co-Sublimation hardware described in Section 3.7.

5. Conclusions and Future Work

5.1. CdTe Solar Cell Conclusions

5.1.1. CdTe Manufacturing

Section 2.1 outlined the development of a single vacuum CSS deposition system and process for the manufacturing of CdTe solar cells. By utilizing manufacturing technologies with proven scalability, advancement in CdTe can be made and transferred to large scale manufacturing. This hardware and process has been optimized to make over 13% efficient CdS/CdTe cells with documented performance over the past 36 months. It is capable of manufacturing approximately 250 SAD's over 10 substrates within a single work day allowing statistical experiments to be performed and has enabled the development of next generation cells with efficiencies over 18%. By retaining the scalability of the technology but increasing the versatility of manufacturing, this developed R&D tool and process has allowed for continued success of the transfer of efficiency improving technologies to large scale manufacturing processes.

5.1.2. Tellurium Back Contact

In Section 2.2, tellurium has been compared directly with carbon paint as a back contact in CdTe cells. Both contacts without intentional copper doping appear to develop barriers, however through different mechanisms. J-V-T measurements have shown the carbon back contact develops a VBO, blocking the flow of reverse current out of the cell. It is theorized that the tellurium back contact pins the Fermi level above the valance band developing a forward current barrier from injected holes. Both contacts rely on copper to mitigate there barriers corresponding negative effects. The VBO causes FF reduction with carbon contacting and the tellurium's low electron affinity causes V_{oc} loss. This is in agreement with ALT of the contacts,

as the copper migrates away from the back contact the cells approach their no copper conditions. This is in agreement with modeling as the back contact doping density is reduced V_{oc} decreases mimicking experimental ALT results. Both contacts appear dependent on copper for optimal performance but the change in barrier formation of the tellurium back contact may prove ideal for VBO prone back contacts such as $Cd_{1-x}Mg_xTe$.

5.2. CdMgTe

5.2.1. CdMgTe Conclusions

The addition of a $Cd_{1-x}Mg_xTe$ layer to the back of the absorber of a CdTe solar cell is shown to improve both the current and the voltage of the cell. Furthermore, the improvements become greater for absorber thicknesses of 1 μm and less. The explanation, consistent with earlier simulations, is that the higher conduction band of the additional layer is reflecting electrons in the CdTe absorber and preventing them from reaching the high-recombination region near the carbon paint back contact. Also consistent with simulations, band-gap expansion of 0.2-0.3 eV appears to be sufficient, and larger expansions are not helpful. Supporting evidence for the effectiveness of the CMT layer comes from high-quality growth, longer decay time seen in TRPL, and collection throughout the CdTe seen in EBIC. A problem that needs to be addressed is that the fill-factor appears to be compromised due to a significant fraction of the band-gap expansion occurring in the valence direction, which can degrade hole collection. The proposed solution is to cap the CMT layer with an additional CdTe layer.

After the CdS/CdTe/CMT stack was passivated with a standard $CdCl_2$ treatment, there was significant degradation to the CMT film. It appeared that the CMT layer was partially oxidized to form MgO on the CMT surface as seen in the XPS peaks and EDX images. This

oxide formation had an electron effect as well, reducing the cell's FF and overall performance. With the addition of a CdTe capping layer, the oxygen signature was significantly reduced, and cell performance was improved. EDX showed however that even with the CdTe capping layer there was localized magnesium loss at the shared grain boundaries. A $MgCl_2$ treatment was explored to minimize this effect, but localized magnesium loss was present with the $MgCl_2$ passivation as well. The lost magnesium appears to be traveling down the grain boundaries to the CdS and TCO interfaces and collecting as evidenced by the reduced 300-500 nm (CdS region) QE response.

With the addition of a CdTe cap to reduce oxidation and the tellurium back contact for improved band alignment the CdTe/CMT ER structure was re-swept across various CdTe thickness. The FF remains primarily flat for the reference cell for the baseline structure while the ER structure shows an increase of ~10% with the thinning CdTe to 0.8um, this is consistent with previous work and models described above. J_{sc} remains fairly constant for both structures. Overall there is 0.8 - 1.0% increase in efficiency with the addition of the ER layer when the absorber is below 1 μm thick. This is primarily from the in V_{oc} increase of 50 mV with the addition of the CMT layer. The trends are consistent with modeling of an ER effect, however under ideal conditions the V_{oc} increase is estimated to be much larger, closer to ~200 mV. The CdTe/CMT interface quality may be limiting the voltage improvement.

To assess the interface recombination quality of the CMT/CdTe interface, double heter-junction cells were fabricated and analyzed comparable to work done by ASU (32). Similar to earlier results, improvements in performance were seen with the addition of CMT but predominantly at a thin absorber condition. TRPL analysis gives an approximation of the CdTe/CMT interface to be ~10^5 cm s^{-1}. Modeling predicts that an interface recombination

velocity of 10^5 cm s^{-1} will prevent any substantial performance increase even under ideal conditions (no valance band off set, favorable CMT doping, and ideal back contacting).

5.2.2. CdMgTe Future Work

The primary obstacle to improving the voltage using the CMT ER structure is the CMT/CdTe interface quality. TRPL analysis predicts this interface recombination velocity to be ~10^5 cm s^{-1}, this is modeled to be too large for any significant V_{oc} improvement. To address this, the co-sublimation technology was re-designed to be incorporated into the primary single vacuum deposition system (ARDS) described in Section 2.0. This allows the CdTe/CMT interface to be deposited without breaking vacuum which should limit interface defects and reduce the interface recombination velocity allowing for more significant V_{oc} improvements. The new co-sublimation technology has an advanced shutter design which allows the magnesium (or band gap) to be graded across the interface for potential further improvement to the interface recombination velocity.

5.3. CdSeTe

5.3.1. CdSeTe Conclusions

Since a reduction in the CdTe band gap from 1.5 to 1.38 eV should result in increased cell current and performance, a new co-sublimation deposition source was developed to manufacture selenium-alloyed CdTe films. Controllable alloying of CdSeTe films was demonstrated and achieved a minimum band gap of 1.41 eV with notable changes to morphology and crystallinity with increasing selenium concentration. Various thickness and selenium concentrations of CdSeTe films were deposited at the front of CdTe solar cells. The lower band-

gap CdSeTe/CdTe cells showed a shift in the QE cutoff to longer wavelengths, consistent with measured transmissions curves and demonstrated larger currents with thicker alloy layers. No significant change was seen in CV measurements suggesting the CdSeTe layer has similar doping concentrations to CdTe. Lifetime was improved and the JVT voltage intercept increased with increasing selenium concentration suggesting the CdSeTe layer is passivating the CdTe improving the interface recombination velocity at the front and bulk.

5.3.2. Future work

With the addition of the new co-sublimation technology into the ARDS a complete optimization of selenium incorporation into the CdTe at the front can be performed. With improved passivation parameters to assess selenium diffusion, increased substrate temperature to increase grain size, and grading of the selenium content for ideal band bending. I'm confident significant improvements to current and voltage deficit can be made resulting in new record efficiencies. Double hetero-structures with CST at various CdTe thicknesses should be performed to approximate the improvement in the front interface recombination velocity and bulk lifetimes.

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