Modelling Thin-Film Transistors for Understanding Material Properties and Improving Electronic Device Performance

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***Abstract*—As new materials continue to develop through theoretical and experimental findings, it is desirable to have a reliable method of testing the materials to better understand their unique properties. Reliable computer modelling of electronic devices composed of these materials provides an inexpensive means of determining how a material will perform. Here we demonstrate the use of a computer software to accurately model electronic devices. We focus on amorphous silicon thin-film transistors and relate what is observed computationally to published experimental and theoretical results. We show that the computer models can be used to accurately study materials for applications in advanced electronic devices. We then discuss opportunities in new materials discovery that this type of modelling might permit.**

I. Introduction

The low cost, abundance, and device performance of amorphous silicon (a-Si) make it a very popular material in modern electronic devices. Thin film transistors (TFTs) using a-Si and related materials represent an important class of silicon-based devices. How these devices operate has much to show about the properties of the materials they're composed of. Accurate modelling and simulation of a-Si TFTs allows for more effective and efficient ways of optimizing adjustable parameters and extracting useful information not easily obtainable through experimentation.

In this paper, we describe how properties of a material - specifically of a-Si - affect the performance of a computer modelled a-Si TFT, and how the performance is affected by the relevant parameters in the material. Here, the relevant parameters include qualitative descriptions of the amount of disorder in the amorphous material and the temperature of the device. We discuss how this method of modelling a-Si TFTs agrees well with published experimental data and previous theoretical arguments, and is hence a viable means of predicting how the properties of constituent materials influence devices and, alternatively, how to extract materials properties from device characteristics.

The a-Si TFTs were modeled using the microelectronic device simulation program Silvaco Atlas [1]. This program uses finite element analysis to solve equations relating the microscopic parameters of the material and geometry of the device to its macroscopic performance and properties. Basic physical relationships, such as charge carrier distribution functions and drift-diffusion equations, are solved numerically. The numerical solutions give rise to macroscopic data such as current-voltage (IV) curves. This type of modelling gives an explicit relationship between device and material parameters and macroscopic data without introducing unwanted experimental difficulties.

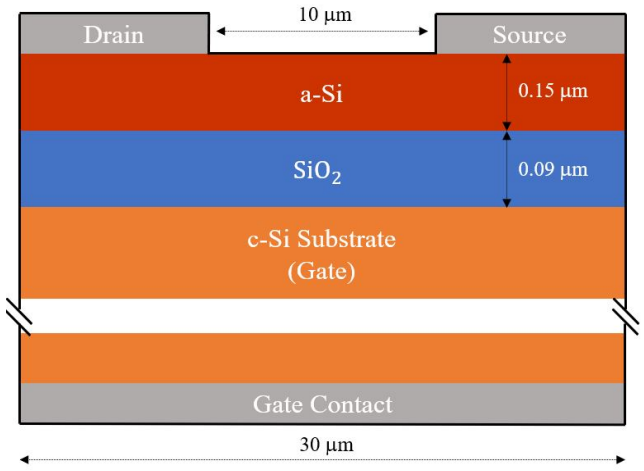

Fig. 1. Structure of the simulated TFT.

II. Computer Model

A. Device Structure

The device structure that was used in this report is displayed in Fig. 1. The device was modelled in two dimensions to minimize the time for computation while retaining the desired physical properties of the device (the actual model assumed a 1 μm thickness - into and out of the page in Fig. 1 - in solving the physical 3-dimensional equations, but the device was treated as 2-dimensional to simplify the analysis). The mesh (or individual elements where the finite element method solved for numbers of interest) was defined to have the highest density of elements in areas of higher importance, such as at the interface of the contacts with the current carrying layer (or active layer) in the TFT, and a lower density in regions of less importance, such as deep in the substrate. The densities were varied until the model's output converged, while also looking to minimize the time needed to perform the computation.

The TFT consists of a 0.15 μm thick undoped a-Si active layer, a 0.09 μm thick SiO_2 insulating layer, and a crystalline

silicon (c-Si) substrate doped n-type at 10^{18} cm^{-3}. The length of the TFT was 30 μm. The doped substrate acted as the gate. Electrical contacts (drain and source, between which current will flow) were placed on the top of the device as shown. Both the drain and source contacts had a length of 10 μm, and the channel had a length of 10 μm. A gate contact was placed underneath the device. The gate will control the current between the source and drain as a field-effect transistor, and little current will flow through the gate due to the insulating oxide layer.

Different drain and source contacts were used depending on whether the primary charge carriers were electrons or holes. The drain and source contacts were specified as metals with a custom workfunction to match either the conduction or valence band energy for electron or hole devices, respectively. In this way, there were no issues with energy barriers (Schottky barriers) at the contacts, otherwise commonly encountered in experimental measurements of this kind. The device was a bottom gate transistor, and the gate contact was aluminum for both electron and hole devices.

B. Material Properties

Silvaco Atlas uses c-Si as the default form of silicon in all simulations. Therefore, to appropriately model a-Si, it was necessary to modify c-Si to match the properties of a-Si. Here, we give a brief comparison of c-Si to a-Si and an overview of the properties of a-Si which we wish to incorporate into our model.

In crystalline silicon, there is a well-defined, periodic, long-range structure. A relatively simple model of one-dimensional crystalline solids of periodic delta functions representing the potential of the atomic nucleus (the Kronig-Penny model) shows that the allowed energy states of a material form energy bands with a well-defined band gap. Charge carriers in the mobile energy states can be represented by a Bloch wavefunction, extending with the periodicity of the crystal. The extended wavefunction is what allows for the conduction of charge carriers in the conduction band of c-Si.

Amorphous silicon, on the other hand, has no such periodicity and is essentially defined by the random network of bond lengths and bond angles. At the same time, a-Si behaves as a semiconductor despite missing the long-range order present in c-Si. The reason for its semiconducting behavior is due to its short-range order (the length-scale of a few atoms) resembling that of a crystalline material. The short-range order allows for the existence of allowed energy bands. The order of a-Si breaks down at longer and longer distances - the slightly varying bond angles, varying bond lengths, and missing atoms become apparent at larger length scales.

Because of the distribution of bond lengths and bond angles, there will be a distribution of localized electronic states between the conduction and valence bands [2]. The density of states decreases exponentially as you move into the band gap, or more appropriately, the mobility gap. These exponential distributions are termed "band tails" or "Urbach tails". In addition to band tail states, additional states are created in the middle of the band gap through unbonded Si atoms called "defects". An energy-level diagram showing qualitative features of the density of states at a given energy for a-Si is shown in Fig. 2.

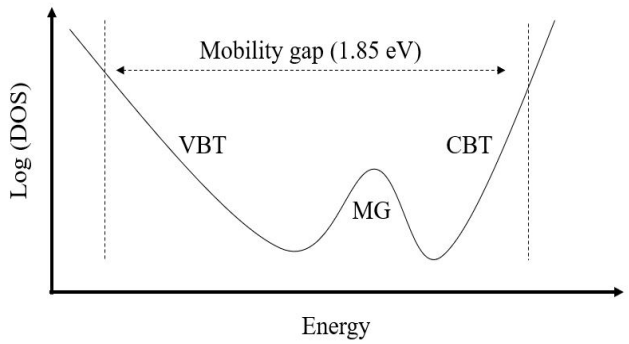

Fig. 2. Qualitative features of the density of electronic states (DOS) as a function of energy in the band gap of amorphous silicon. Shown is the valence band tail (VBT), conduction band tail (CBT), and mid-gap states (MG). Image adapted from Ref. [3].

The band structure of a-Si presented here can be verified experimentally by looking at its optical absorption spectra [4], [5]. In these spectra, we see a large absorption when the energy of the incident photons matches the band gap. As we decrease the energy of the photons, the absorption decreases exponentially in accordance with the exponential decrease in the density of states at each band tail.

The tail states consist of mobile states at higher energies closer to the bands and immobile states deeper within the band gap. The extra time spent in the immobile states as compared to mobile states thus decreases mobility of the charge carriers. The non-periodicity of the material also has the effect of lowering the carrier mobility as there is no well-defined, long-range path for the carriers to travel. Thus there is an increase in scattering, increasing the time it takes for a carrier to travel a given distance in a material. We can define a free carrier mobility, μ_0, which is the theoretical mobility of a carrier in the mobile states without being trapped in immobile states. Drift mobility, μ_d, is the "effective mobility" which takes into account the trapping of charge carriers and is what is measured experimentally. We can also define a "mobility edge" as the transition energy from mobile states to states that are effectively immobile. The energy difference between the mobility edges for electrons and holes is the mobility gap, and the density of states at the mobility edge is called the band tail intercept density. How the mobility is defined in the simulations is discussed further below.

The models constructed in Silvaco Atlas were thus made to simulate the features of a-Si described above. The a-Si was modelled primarily in terms of the band structure, carrier mobility, and temperature dependence of the mobility. The free-carrier mobility μ_0 was set as 7 cm^2/Vs for electrons and 0.2 cm^2/Vs for holes (compare to 1400 and 450, respectively, in c-Si [1], [6]). Both are on the same order of values recorded

in previous experiments and, as will be shown later in this report, resulted in drift mobilities on the same order of those recorded previously [4], [7]. The temperature dependence of the mobility takes into account scattering and excitation of charge carriers, and is discussed further below in terms of the computer model.

The band structure of the a-Si was described by the mobility gap, the slope of the band tails, and a Gaussian distribution of defects within the band gap. The mobility gap of a-Si was entered as 1.82 eV [2], [5]; slightly larger than that of c-Si (1.1 eV) due to the altered density of states near the band edge. The equations describing the density of states of the band tails and of the defects are given in equations 1 and 2, respectively.

$$N_{bt}(E) = N_{bt} \exp\left(\frac{-\Delta E}{kT_{bt}}\right) \tag{1}$$

$$N_{mg}(E) = N_{mg} \exp\left[-\left(\frac{\Delta E}{kT_{mg}}\right)^2\right] \tag{2}$$

In equation 1, N_{bt} represents the band tail intercept density, ΔE represents the difference in energy from the respective band (such that each tail decays as you move into the gap away from the respective band), and kT_{bt} represents the characteristic decay energy or slope of the band tail. In equation 2, N_{mg} represents the maximum density of states in the Gaussian distribution, ΔE represents the difference in energy from the location of the maximum, and kT_{mg} represents the characteristic energy width of the Gaussian distribution.

The default values used for N_{bt} was 1×10^{21} cm^{-3} for both the conduction and valence bands. The default slopes of the band tails was 30 meV and 50 meV for the conduction and valence band, respectively. The lower slope of the valence band (and thus larger extension into the band gap) can be better understood by considering the geometry of the anti-bonding and bonding states of silicon [4]. Anti-bonding states in the conduction band are spherically symmetric, meaning that a deviation from the typical bonding angle will not cause a major change in the band structure. On the other hand, bonding states in the valence band do not posses this symmetry, and thus a deviation from the typical bonding angle will have a more noticeable effect on the band structure.

As shown later in the paper, mid-gap defects were found to have a negligible effect on the carrier mobility. They did, however, have an effect on the Fermi level of the material. Defects tended to cause difficulties in the numerical calculations. We spend one section looking at the effects of defects on device performance. After this section, the defect density was set to zero on all calculations unless noted otherwise to keep calculations as simple as possible when looking at how other parameters affected device performance.

The TFTs can operate with an electron channel, which uses positive gate voltages to attract electrons to the a-Si/SiO_2 interface, or a hole channel, which uses negative gate voltages to repel electrons from (or attract holes to) the interface. The accumulation of charge carriers near the interface allows

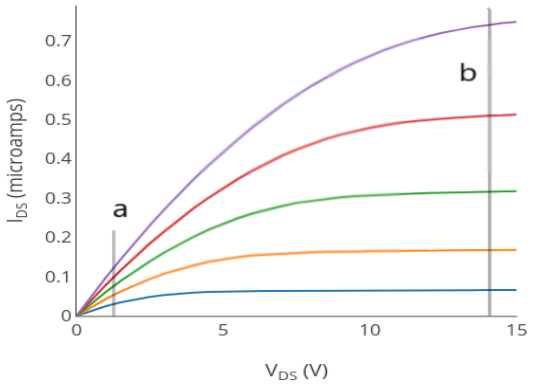

Fig. 3. I_{DS} versus V_{DS} at various constant gate voltages. Blue shows a gate voltage 5V, orange 7.5V, green 10V, red 12.5V, and purple 15V. Line *a* shows a given V_{DS} at which the device operates in the linear regime, and *b* shows the saturation regime.

that region to conduct between the drain and source contacts. Henceforth, a device that uses an electron channel to carry current will be referred to as simply an "electron device", and one that uses holes to conduct will be referred to as a "hole device".

III. Simulation Results

The simulations produced the well-known IV curves of drain-to-source current, I_{DS} as a function of drain-to-source voltage, V_{DS}. A plot of I_{DS} versus V_{DS} at various fixed gate voltages is shown in Fig. 3 for an electron device. Subsequent simulations extracting properties of the material were done of I_{DS} versus gate-to-source voltage, V_{GS}, at a fixed V_{DS}. In Fig. 3, line *a* at low V_{DS} shows where I_{DS} is roughly proportional to V_{GS} and is called the linear regime of the TFT. At line *b* at high V_{DS}, I_{DS} is roughly proportional to the square of V_{GS} and is called the saturation regime of the TFT. All subsequent results were obtained in the saturation regime.

Since I_{DS} is proportional to the square of V_{GS} in the saturation region, plotting the square root of I_{DS} versus V_G results in a linear plot. From this plot, the carrier mobility can be extracted [8] from the equation

$$\mu_d = m_{sat}^2 \frac{2L}{WC_{ox}} \tag{3}$$

where m_{sat} refers to the slope of $I_{DS}^{1/2}$ versus V_{GS}, L is the length of the channel, W is the width of the channel, and C_{ox} is the capacitance of the insulating oxide layer. Equation 3 was used to determine the mobility of both electrons and holes as the defect density, band tail slope, band tail intercept density, and temperature were varied.

A. Dangling Bonds

The disorder in a-Si results in some valence electrons in the material not bonding to their neighbors, resulting in what is termed a "dangling bond". Each dangling bond consists of a single electron, giving each dangling bond a net spin. Because of their spin, dangling bonds can be confirmed

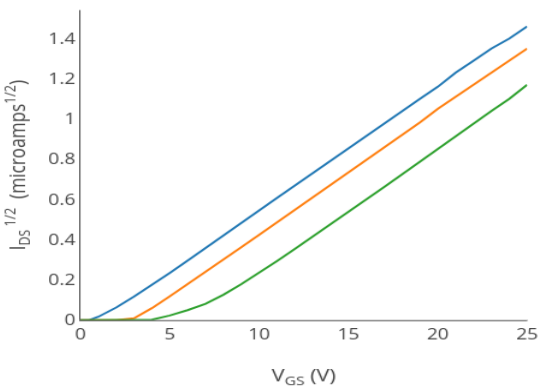

Fig. 4. I_{DS} versus V_{GS} for a-Si consisting of various levels of defects. Blue shows a defect density of 8×10^{15} cm^{-3}, orange 4×10^{16} cm^{-3}, green 8×10^{16} cm^{-3}.

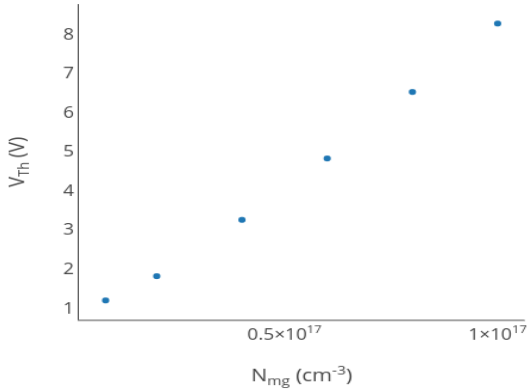

Fig. 5. Threshold voltage (V_{th}) as a function of defect density in an electron device.

through observations with electron spin resonance. Their effect on the carrier mobility has been tested experimentally through the use of time-of-flight experiments [7]. The results show that the mobility stays roughly constant as the level of defects are varied. Here, we demonstrate the same result through the simulations of TFTs.

Fig. 4 shows a plot of $I_{DS}^{1/2}$ versus V_{GS} in the saturation regime (each curve with a constant drain to source voltage of 20V) with the active a-Si layer having a varying level of defects. Clearly, once the carrier channel has been saturated (i.e., once the curve becomes roughly linear), each curve displays the same slope, and thus each material has the same carrier mobility by equation 3.

One clear difference between the curves in Fig. 4 is how the "turn-on voltage" or "threshold voltage" changes with changing defect densities. This was determined by extrapolating the linear portion of the curve to find its x-intercept, which we define as the threshold voltage. The change in threshold voltage implies a change in the Fermi level of the a-Si, as a higher energy is required for the device to form an accumulation layer [8]. In other words, a higher voltage is required to attract carriers to the a-Si/SiO_2 interface to create a conducting channel. Fig. 5 shows there to be a roughly linear dependence of the threshold voltage as a function of defect density, signifying a linear relationship between the Fermi level of the a-Si and the density of defects.

B. Band Tails and Shallow Localized States

Shallow localized states located in the band tail are present in much higher densities than dangling bonds in amorphous silicon, and should therefore have a much higher impact on the carrier mobility. To see this, we look at how the drift mobility is related to the free carrier mobility. The drift mobility is related to the free carrier mobility by the time the charge carriers spend in immobile, localized states compared to the time spent in mobile states. This model can be written explicitly as [4]

$$\mu_d = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{loc}} \tag{4}$$

where τ_{free} is the average time spent in mobile states and τ_{loc} is the average time spent in immobile, localized states. If we restrict our view to how the mobility is effected by localized states at a single energy level, we can rewrite equation 4 as

$$\mu_d = \frac{\mu_0}{1 + f_{loc}} \tag{5}$$

where

$$f_{loc} = \frac{N_{loc}}{N_{free}(E_c)kT} \exp\left(E_{loc}/kT\right) \tag{6}$$

is the ratio of time spent in immobile states to mobile states for a single localized state energy level [4]. Here, N_{loc} is the density of localized states evaluated at the energy E_{loc} and N_{free} is the density of states per unit energy at the conduction band energy E_c. We can then use equation 5 to obtain the drift mobility.

Notice that when the density of conducting states is much larger than the density of localized states, or at sufficiently high temperature, f_{loc} becomes very small and the drift mobility approaches the free carrier mobility. Therefore, in our model we expect to see the drift mobility decrease as the density of localized states is increased or the temperature is decreased in accordance with equation 5.

Fig. 6 shows the dependence of mobility on the slope of the band tail for the computer model. Note that the slope of the conduction band was varied for electrons, while the slope of the valence band was varied for holes. A similar trend was found between the mobility and the band tail intercept density, and is shown in Fig. 7. Both figures show that as the density of localized states is increased, the simulations were able reproduce the macroscopic properties in the mobility in accordance with equation 5, as expected.

Like dangling bonds, the level of disorder represented by the band tails also has an effect on the threshold voltage, though the effect is not as dramatic. Fig. 8 shows a log plot of the threshold voltage as a function of the band tail intercept density. The data shown is from a-Si with zero defects. Even

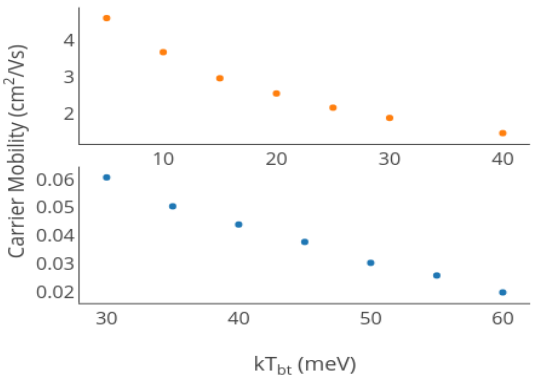

Fig. 6. Electron (top) and hole (bottom) mobilities versus the decay energy of the respective band tail.

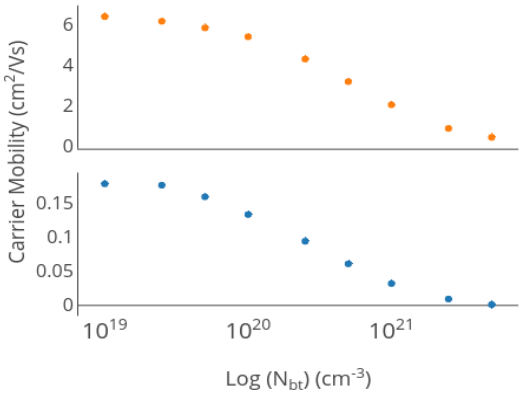

Fig. 7. Log plot of the dependence of electron (top) and hole (bottom) mobility on the band tail intercept density.

on the logarithmic scale, the threshold voltage changes only by a few volts.

C. Temperature Dependence of Mobility

In an amorphous material, temperature changes the dynamics of the carriers in two main ways. The first is that an increase in temperature corresponds to more charge carriers

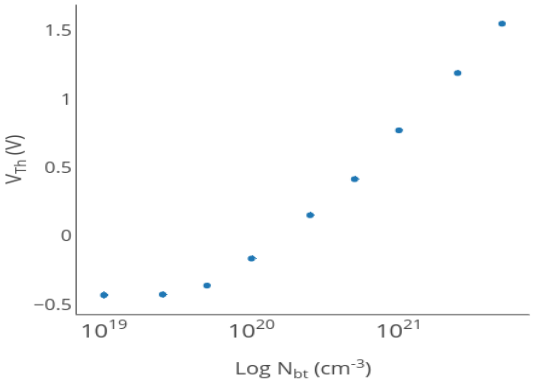

Fig. 8. Log plot of the band tail intercept density versus threshold voltage in an electron device.

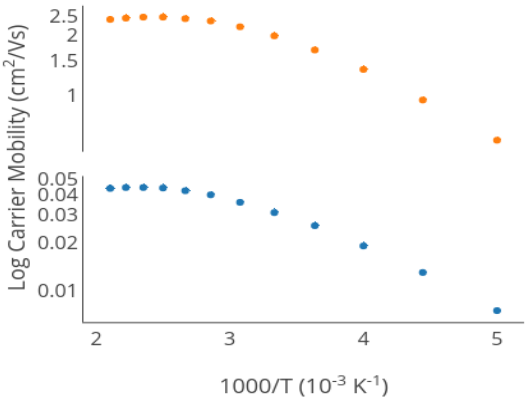

Fig. 9. Arrhenius plot of the dependence of Electron (top) and hole (bottom) mobility on temperature.

being excited into conducting states from localized states. Thus carriers spend more time in mobile states, resulting in an increased drift mobility. This trend can be seen in equation 5, where the drift mobility increases with increasing temperature. The second effect is the increased scattering of charge carriers by phonons at higher temperatures, which lowers the drift mobility.

When the total density of localized states is much greater than the density of free states such that the time a carrier spends in localized states is much greater than that spent in mobile states (i.e., $\mu_d \ll \mu_0$), equation 5 displays Arrhenius behavior. This behavior is seen in Fig. 9, where the log of mobility versus inverse temperature is roughly linear. This only applies at very low temperatures, where phonon scattering is minimal and equation 5 can be treated as a good approximation to the drift mobility based on the density of electronic states. At higher temperatures, it is also necessary to take into account the added scattering by phonons, which equation 5 does not. Therefore, another equation is needed to fully model the temperature dependence of the mobility. A common way to model the temperature dependence of scattering is to relate the increased cross-sectional scattering area and increased velocity of carriers to the mobility as in equation 7. This was the model used in this report, where the phonon scattering effects μ_d by the relation

$$\mu_d = \mu_0 \left(\frac{T}{300K} \right)^{-3/2} . \tag{7}$$

The competing effects of temperature on mobility in equations 5 and 7 result in the curve shown in Fig. 9. It is clear that the effect of added excitation of the charge carriers plays a dominant role on the mobility up to around 420K, at which point the increase in scattering begins to dominate and decrease the mobility as temperatures increase even more. These results are supported through previous experimental findings [9], [10].

IV. Conclusions

Through the simulation of a-Si TFTs, we have looked at four major parameters that affect its performance using the device simulation software, Silvaco Atlas. The full numerical simulations match the trends reported in previous theoretical arguments and published experimental data. These ideas and their application to the simulation of amorphous materials in microelectronic devices can be summarized as follows. First, dangling bond defect states have little to no effect on the mobility of charge carriers, but have a large effect on the threshold voltage of the TFT and thus affect the Fermi level of the material. Second, the density of localized states near each band displays a negative relationship with the mobility. Third, the mobility displays a positive, Arrhenius behavior at lower temperatures in amorphous materials. At higher temperatures (over approximately 420K) the carrier mobility begins to decrease due to scattering dominating the transport process.

The results demonstrated in this report show that the computer modelling of TFTs is a viable means of both studying how material properties effect devices and of improving device performance. While the studies here focused on the properties of a-Si, the work can be extended to more exotic materials; for example, experimental data from TFTs made of an exotic material can be matched to the computer model to learn more about the microscopic properties governing the bulk behavior [3]. Moreover, the computer models can be used to indirectly confirm existing theories of material properties through direct computation of microscopic properties, supporting evidence obtained through macroscopic experimental data.

Acknowledgments

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References

[1] Silvaco Atlas Device Simulation User's Manual, Silvaco, Inc., 4701 Patrick Henry Drive, Bldg. 2, Santa Clara, CA 95054, 2015.
[2] N. F. Mott, "States in the gap in non-crystalline semiconductors", Journal of Physics C: Solid State Physics, Vol. 13, pp. 5433–5471, 1980.
[3] I. Airuoyo, "The Field Effect in Co-Deposited Quantum Confined a/nc-Si:H", Ph.D. Thesis, Colorado School of Mines, 2018.
[4] R. A. Street, "Hydrogenated Amorphous Silicon", Cambridge University Press, 1991.
[5] M. Vaněček, J. Kočka, J. Stuchlík, and A. Tříska, "Direct measurement of the gap states and band tail absorption by constant photocurrent method in amorphous silicon", Solid State Communications, Vol. 39, pp. 1199–1202, 1981.
[6] Electrical Properties of Silicon, Ioffe Institute Database.
[7] R. A. Street, "Trapping parameters of dangling bonds in hydrogenated amorphous silicon", Applied Physics Letters, Vol. 41, pp. 1060-1062, 1982.
[8] B. V. Zeghbroeck, "Principles of Semiconducting Devices", 2004.
[9] R. A. Street, J. Kakalios, and M. Hack, "Electron drift mobility in doped amorphous silicon", Physical Review B, Vol. 38, pp. 5603–5609, 1988.
[10] W. Fuhs, M. Milleville, and J. Stuke, "Drift Mobility and Photoconductivity in Amorphous Silicon", Physica Status Solidi (B), Vol. 89, pp. 495–502, 1978.