ADVANCED CONTROL OF CONVERTERS WITH MULTITASK FUNCTIONALITIES IN DISTRIBUTION GRID SYSTEMS BASED ON CONSERVATIVE POWER THEORY

by

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ii
ABSTRACT

Distributed generation (DG) play a very important role in the modernization of electric power systems, it is estimated their increasing share of operation in the near future. In addition, there is growing concern on the environmental issues, lack of transmission capacity and limitation in constructing new lines, and increasing demand of energy, that would support a more flexible inverter control, capable of interacting users with the utility grid. The main objective of such a system is providing active power, which is the primary use to balance loads. However, power electronic systems can provide power quality improvement and DG systems would then be used as multi-functional compensators for improving power quality, instead of only balancing or selling active power to the grids. In this context, this dissertation first studies the well-known instantaneous current decomposition theories highlighting the important contributions based on the Instantaneous Power (PQ) theory and the Conservative Power Theory (CPT) and presents a comprehensive comparison from performance and computational complexity perspectives. Although these theories are quite distinct in their formulations, the central idea is to make a comparative study between the current portions and their respective portions of power, in order to show the similarities and divergences between them in terms of characterization of the physical phenomena and in terms of disturbing current compensation. The studied instantaneous current decomposition techniques are then used to provide selective functionalities in distribution systems. Therefore, it is possible to inject active power plus compensate selectively unwanted current terms (reactive, unbalance, and distortion), enabling full exploitation of the inverter capability and increasing its overall cost-benefit and efficiency. Afterwards, control structures with multitask functionality to the grid side converter of the renewables to carry out the power quality ancillary services in the distribution system are developed. The key diversity of the methodologies we proposed in this project with respect to others in the literature is that the developed control structures on the grid side converters are based on the CPT theory. This choice provides decoupled power and current references for the grid side inverter control, which offers very flexible, selective and powerful functionalities. These qualities make the system to be the benchmark for achieving 100% renewable and sustainable grid with multifunctional capabilities. This thesis then proposes the coordinated control of the aforementioned multifunctional interfacing DG systems to enhance the operation of microgrid systems. Based on our proposed method, a hybrid cooperative strategy
is developed that overcomes limitations in communication-based and non-communication-based approaches for the coordinated operation of multifunctional distributed generators in islanded microgrid systems. Two important issues that are addressed are the power quality and undesirable current sharing, particularly in the low-voltage distribution network, where electronic devices are drawing distorted and unbalanced currents. The interactions of such current disturbances with high feeder/line impedances, in a low voltage system cause considerable voltage deterioration and possibly affect sensitive loads showing the requirement for power quality enhancement. Finally, this thesis explores the study and implementation of cascaded multilevel converters, in which the primary concepts relating to modulation, structure, and control schemes are detailed. These topologies are composed of series-connected H-bridge converters with isolated DC links. Therefore, it is possible to integrate renewable energy and storage resources to power grids. The experimental findings validate the applicability and performance of the proposed control strategies in distribution grid systems.
TABLE OF CONTENTS

ABSTRACT ......................................................................................................................... iii
LIST OF FIGURES .............................................................................................................. viii
LIST OF TABLES ................................................................................................................ xiii
ACKNOWLEDGMENTS ..................................................................................................... xiv

CHAPTER 1  INTRODUCTION .............................................................................................. 1
  1.1  Research Objectives ................................................................................................. 3
  1.2  Organization of the Thesis ....................................................................................... 4

CHAPTER 2  POWER THEORIES FOR CURRENT DECOMPOSITIONS AND
RELATED DEFINITIONS ...................................................................................................... 6
  2.1  Instantaneous Power Theory (PQ) ............................................................................ 7
    2.1.1  The Clarke Transformation ................................................................................. 8
    2.1.2  The Instantaneous Powers of the PQ Theory ....................................................... 9
    2.1.3  Power Terms based on PQ theory ..................................................................... 14
  2.2  Conservative Power Theory .................................................................................... 15
    2.2.1  Conservative Power Terms under Periodic Non-sinusoidal Operation ......... 15
    2.2.2  Current Terms under Periodic Non-Sinusoidal Operation .............................. 17
    2.2.3  Power Terms under Periodic, Non-sinusoidal Operation .............................. 21
    2.2.4  Load Conformity Factors ................................................................................. 22
  2.3  Analysis of Different Compensation Strategies by Means Of Ideal Current
Source Models .................................................................................................................. 24
    2.3.1  Symmetrical and Sinusoidal Voltage Source ..................................................... 25
    2.3.2  Asymmetrical and Sinusoidal Voltage Source .................................................. 30
    2.3.3  Symmetrical and Non-sinusoidal Voltage Source ........................................... 33
  2.4  Analysis of Different Compensation Strategies by Means of Three-Phase
Three-Wire Inverter .......................................................................................................... 35
    2.4.1  Compensating Load Current Components Based on CPT: ............................ 38
    2.4.2  Compensating Load Current Components Based on PQ: .............................. 41
  2.5  Computational Complexity and Dynamic Response for each Control Method.... 44
2.6 Discussions

CHAPTER 3
STUDY OF FOUR-LEG GRID-TIED INVERTER WITH LOCAL POWER SOURCE AND SIMULTANEOUS FUNCTIONALITY

3.1 Fundamental Formulas

3.2 The Current Decomposition of the CPT in Single-Phase System

3.2.1 The Active Current

3.2.2 Reactive Current

3.2.3 Void Current

3.3 Current Decomposition of the CPT in Three-Phase Systems

3.3.1 Three-Phase Active Current

3.3.2 Three-Phase Reactive Current

3.3.3 Three-Phase Void Current

3.3.4 Three-Phase Balanced Active Current

3.3.5 Three-Phase Unbalanced Active Current

3.3.6 Three-Phase Balanced Reactive Current

3.3.7 Three-Phase Unbalanced Reactive Current

3.3.8 Compensation of Unbalanced Load

3.4 Three-Phase Four-Leg Grid-Tied Inverter Structure and Control

3.4.1 Four-Wire DG Inverter Control Strategy

3.4.2 Analysis of Different Compensation Strategies by Means of Three-Phase Four-Leg Inverter

3.5 Discussions

CHAPTER 4
COORDINATED OPERATION OF MULTIFUNCTIONAL DISTRIBUTED GENERATORS IN A MULTI-INVERTER BASED ISLANDED MICROGRID

4.1 Cooperative Control of Four-Leg Interfacing Converters in Islanded Microgrid with Power Quality Enhancement Based on CPT Theory

4.1.1 Microgrid Structure with Four-Leg Interfacing Converters

4.1.2 Load Current Sharing Strategy among DG Inverter Units

4.1.3 Application Example by Means of Three-Phase Four-Wire Inverters
4.2 Participation of Single-Phase Interfacing Converters in Three-Phase Islanded Microgrids with Power Quality Enhancement Based on CPT Theory .................. 98

4.2.1 Microgrid Structure with Participation of Single-phase Interfacing Converters ....................................................................................................................... 98

4.2.2 Load Current Components Sharing among Single-Phase and Three-Phase DG Inverters .............................................................................................................. 101

4.2.3 Application Examples by Means of Single-Phase and Three-Phase Inverters ......................................................................................................................... 102

4.3 Discussions.......................................................................................................................... 108

CHAPTER 5 CASCADED MULTILEVEL CONVERTER FOR POWER QUALITY IMPROVEMENT IN SMARTGRID APPLICATIONS ........................................ 110

5.1 Cascaded H-bridge Multilevel Converter Topology ............................................................ 111

5.2 SAPF CHMI Modulation and Control ................................................................................. 113

5.2.1 Control Strategy ............................................................................................................. 116

5.2.2 Analysis of Different Compensation Strategies by Means of Experimental Results ........................................................................................................... 123

5.3 Discussions.......................................................................................................................... 134

CHAPTER 6 CONCLUSIONS AND FUTURE WORK ............................................................... 136

6.1 Conclusions.......................................................................................................................... 136

6.2 Future Work.......................................................................................................................... 138

6.2.1 Development of Cooperative Control Strategies for Maintenance of Power Quality Indexes in Microgrids with Multiple Bus Considerations ............ 138

6.2.2 Development of Bidirectional Electric Vehicle (EV) Charging System for Smart Grid Applications ................................................................................. 139

6.2.3 Study of Energy Management System for Smart Microgrids ...................................... 139

REFERENCES CITED.............................................................................................................. 140
LIST OF FIGURES

Figure 2-1  Three-phase three-wire circuit with nonlinear and unbalanced load. ....................... 24
Figure 2-2  PCC voltages and currents before compensation with symmetrical and sinusoidal voltage sources ................................................................. 25
Figure 2-3  Unbalanced currents compensation using CPT .......................................................... 26
Figure 2-4  Void currents compensation using CPT ................................................................. 27
Figure 2-5  Unbalanced and void currents compensation using CPT ........................................... 28
Figure 2-6  Non active currents compensation using CPT ......................................................... 28
Figure 2-7  Load oscillating active current compensation using PQ ............................................ 29
Figure 2-8  Load oscillating reactive current compensation using PQ ........................................ 30
Figure 2-9  PCC voltages and currents before compensation with unbalanced voltage source ........................................................................................................... 31
Figure 2-10  Non active currents compensation (CPT) ............................................................... 31
Figure 2-11  Compensation of oscillating active and total reactive currents (PQ) ......................... 32
Figure 2-12  PCC voltages and currents before compensation with symmetrical non-sinusoidal voltage sources ................................................................. 33
Figure 2-13  Non active currents compensation (CPT) ............................................................... 33
Figure 2-14  Non active currents compensation (CPT) ............................................................... 34
Figure 2-15  Compensation of oscillating active current and the total reactive current (PQ) ....... 35
Figure 2-16  Prototype hardware implementation ....................................................................... 36
Figure 2-17  Three-phase inverter configuration ....................................................................... 37
Figure 2-18  Before implementing any compensation strategy: PCC voltage (85 V/div) and load current (5 A/div) of phases a and b ......................................................... 38
Figure 2-19  Compensation of balanced reactive current component: PCC voltage (85 V/div) and inverter current (0.5 A/div) of phases a and b .............................................. 39
Figure 2-20  Compensation of unbalance current component: PCC voltage (85 V/div) and inverter current (0.5 A/div) of phases a and b ......................................................... 39
Figure 2-21  Compensation of void current component: PCC voltage (85 V/div) and inverter current (2 A/div) of phases a and b ................................................................. 40
Figure 2-22  Compensation of unbalance and void current components: PCC voltage (85 V/div) and inverter current (2 A/div) of phases a and b ............................................. 41
Figure 2-23  Compensation of balanced reactive, unbalance, and void current components: 
PCC voltage (85 V/div) and grid current (5 A/div) of phases a and b. ...................... 41

Figure 2-24  Compensation of load constant reactive current component: PCC voltage 
(85 V/div) and inverter current (0.5 A/div) of phases a and b. ............................... 42

Figure 2-25  Compensation of oscillatory active current component: PCC voltage (85 V/div) 
and inverter current (2 A/div) of phases a and b. ................................................. 42

Figure 2-26  Compensation of oscillatory reactive current component: PCC voltage 
(85 V/div) and inverter current (2 A/div) of phases a and b. ................................. 43

Figure 2-27  Compensation of oscillatory active and reactive current components: PCC 
voltage (85 V/div) and inverter current (2 A/div) of phases a and b. ..................... 43

Figure 3-1   Implementation of active current given by (3.8). ............................................... 49

Figure 3-2   Implementation of reactive current given by (3.9). ............................................. 50

Figure 3-3   Implementation of void current given by (3.10). ................................................... 50

Figure 3-4   Implementation of balanced active current given by (3.15). ............................... 52

Figure 3-5   Implementation of unbalanced active current given by (3.16). ............................. 53

Figure 3-6   Considered grid-tied four-leg inverter with a current source modeled as DG..... 54

Figure 3-7   Four-wire four-leg grid-tied PEI. ........................................................................... 56

Figure 3-8   Block diagram of the current control loop. ............................................................. 57

Figure 3-9   Bode diagram of the current control plant in both “s” and “w” planes: 
(a) Magnitude response, (b) Phase response.............................................................. 58

Figure 3-10  Bode plot of the open loop current transfer function. ........................................... 60

Figure 3-11  Block diagram of the DC voltage control loop. ..................................................... 62

Figure 3-12  Bode plot of the open loop DC-link voltage transfer function. ............................. 64

Figure 3-13  Active power delivery: (a) PCC voltage and inverter current, (b) PCC voltage 
and grid current, (c) grid neutral current and inverter neutral current. ..................... 66

Figure 3-14  Active and reactive power delivery: (a) PCC voltage and inverter current, 
(b) PCC voltage and grid current, (c) grid neutral current and inverter neutral current. ......................................................... 68

Figure 3-15  Active power delivery and reactive and unbalance compensation: (a) PCC 
voltage and inverter currents, (b) PCC voltage and grid current, (c) grid neutral 
current and inverter neutral current................................................................. 69

Figure 3-16  Active power delivery and non-active compensation: (a) PCC voltage and 
inverter currents, (b) PCC voltage and grid current, (c) grid neutral current and 
inverter neutral current................................................................. 70
Figure 4-22 Group A and B master inverters voltage waveforms before and after compensation of load non-active current components (t=0.6s) ................. 106
Figure 4-23 Groups A and B load buses voltage waveforms before and after compensation of load non-active current components (t=0.6s) ................................................. 106
Figure 4-24 Active power sharing among VSI units ................................................................. 107
Figure 5-1 CHMI Topology ........................................................................................................ 111
Figure 5-2 Block diagram of the power circuit, control scheme, and loads to the power grid .......................................................................................................................... 114
Figure 5-3 Reference and carrier signals for one phase of the 7-level CHMI. ......................... 115
Figure 5-4 DSP implementation of the PS-PWM for the 7-level CHMI .................................... 115
Figure 5-5 Block diagram of the proposed control scheme with DC voltage controllers of H-bridge cells in phase a ................................................................. 117
Figure 5-6 Bode plot of the open-loop current transfer function ............................................. 120
Figure 5-7 Bode plot of the open loop DC-link voltage transfer function ............................... 123
Figure 5-8 Before implementing any compensation strategy: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b ................................................................. 124
Figure 5-9 Compensation of balanced reactive current component: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b, (b) Compensation of balanced reactive current component: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b .................................................................... 125
Figure 5-10 (a) Compensation of unbalance current component: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b, (b) Compensation of unbalance current component: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b ................................................................. 126
Figure 5-11 (a) Compensation of void current component: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b, (f) Compensation of void current component: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b .............................................................................. 127
Figure 5-12 Compensation of non-active current component under symmetrical and sinusoidal voltage sourc: (a) PCC voltage (90 V/div) and grid current (40 A/div), (b) CHMI terminal voltages (110 V/div), (c) H-bridge DC-link regulated voltages (25 V/div) of phase a and DC-link current (12 A/div) of H-bridge a1 ................................................................. 129
Figure 5-13 Compensation of non-active current component under asymmetrical and sinusoidal voltage source: (a) PCC voltage (90 V/div) and grid current (40 A/div), (b) CHMI terminal voltages (110 V/div), (c) H-bridge DC-link
regulated voltages (25 V/div) of phase a and DC-link current (12 A/div) of H-bridge a1. ........................................................................................................ 131

Figure 5-14 Compensation of non-active current component under symmetrical and non-sinusoidal voltage source: (a) PCC voltage (90 V/div) and grid current (40 A/div), (b) CHMI terminal voltages (110 V/div), (c) H-bridge DC-link regulated voltages (25 V/div) of phase a and DC-link current (12 A/div) of H-bridge a1. ........................................................................................................ 133
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table 2-1</th>
<th>Source voltages, line impedance and load parameters. .................................................. 25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 2-2</td>
<td>Three-phase Inverter and load parameters. ........................................................................ 37</td>
</tr>
<tr>
<td>Table 2-3</td>
<td>Required mathematical operations and dynamic response for each control method. .................. 44</td>
</tr>
<tr>
<td>Table 3-1</td>
<td>Three-phase Four-leg Inverter and load parameters. ........................................................... 55</td>
</tr>
<tr>
<td>Table 3-2</td>
<td>Requirements chosen for current control scheme. ................................................................. 59</td>
</tr>
<tr>
<td>Table 3-3</td>
<td>Requirements chosen for DC voltage control scheme. .......................................................... 63</td>
</tr>
<tr>
<td>Table 4-1</td>
<td>Microgrid Inverters Parameters. ............................................................................................. 79</td>
</tr>
<tr>
<td>Table 4-2</td>
<td>Requirements chosen for current control scheme. ................................................................. 81</td>
</tr>
<tr>
<td>Table 4-3</td>
<td>Requirements chosen for voltage control scheme. ................................................................... 85</td>
</tr>
<tr>
<td>Table 4-4</td>
<td>Load and Line Impedance parameters. ....................................................................................... 89</td>
</tr>
<tr>
<td>Table 4-5</td>
<td>Load and Line Impedance parameters. ....................................................................................... 100</td>
</tr>
<tr>
<td>Table 5-1</td>
<td>CHMI parameters. .................................................................................................................... 117</td>
</tr>
<tr>
<td>Table 5-2</td>
<td>Requirements chosen for current control scheme. ................................................................... 119</td>
</tr>
<tr>
<td>Table 5-3</td>
<td>Requirements chosen for DC voltage control scheme. ............................................................ 122</td>
</tr>
<tr>
<td>Table 5-4</td>
<td>Load parameters. ...................................................................................................................... 123</td>
</tr>
<tr>
<td>Table 5-5</td>
<td>PCC Power Components, Inverter and Grid Currents, and Power Factor under possible selective compensation strategies. .......................................................... 127</td>
</tr>
<tr>
<td>Table 5-6</td>
<td>PCC Power Components, Inverter and Grid Currents and Power Factor through the non-active compensation - Case 1. ................................................................. 130</td>
</tr>
<tr>
<td>Table 5-7</td>
<td>PCC Power Components, Inverter and Grid Currents and Power Factor through the non-active compensation - Case 2. ................................................................. 132</td>
</tr>
<tr>
<td>Table 5-8</td>
<td>PCC Power Components, Inverter and Grid Currents and Power Factor through the non-active compensation - Case 3. ................................................................. 134</td>
</tr>
</tbody>
</table>
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My family,
My dear Mom and Dad,
for their boundless support and love
CHAPTER 1 INTRODUCTION

The world is at the edge of a major shift in the paradigm of electrical energy generation, transmission, distribution and storage, by moving from existing, centralized generation towards distribution energy resources (DER). The new paradigm has the potential to result in higher stability margins and better reliability, reduction of transmission lines power loss, power quality increase, ability to shift peak loads, etc. Smart grid technologies help utilities to operate, control, and maintain DER as well as interconnect them to the main grid. In the new paradigm of the grid, the complexity of technical tasks have changed from dealing with local SCADA data into a variety of massive field data collection, that allows a more comprehensive view of the power system status, energy flows, hierarchical control, asset management, equipment conditions etc. A Microgrid is a localized grouping of DER and loads that has the capability of islanding and operating independently from the grid as well as grid-connected mode of operation. As long as a microgrid is connected to a large grid, the voltage is supported by the main grid and power source connected to the microgrid could generate independently. In contrast, in the islanded operation of microgrids and in electrical islands such as shipboard distribution systems, dynamics are strongly dependent on the connected sources and on the power regulation control of the grid interfacing converters. This may affect control accuracy and stability of the system. Furthermore, load variation has an adverse impact on the quality of voltage. While any load step generally affects the magnitude of voltages at the load bus, nonlinear and unbalanced loads cause distortion and imbalance of the load voltage.

Smart technologies bring about the possibility of a smart microgrid. A smart microgrid typically integrates the following components [1], [2].

1) Renewable energy resources capable of supplying local demand as well as feeding the unused energy back to the electric grid.
2) A variety of loads, including residential, office and industrial loads.
3) Local and distributed power storage units to smooth out the intermittent performance of renewable energy sources.
4) Smart meters and sensors capable of measuring electric parameters such as active power, reactive power, voltage, current, harmonics, unbalanced current, and so on with acceptable precision and accuracy.

5) Communication infrastructure that enables system components to exchange information and commands securely and reliably.

6) Smart terminations, loads, and appliances capable of communicating their status and accepting commands to adjust and control their performance and service level based on user and/or utility requirements.

7) A supervisory control, composed of integrated networking, computing, and communication infrastructure elements, that appears to users in the form of an Energy Management System that allows command and control on all nodes of the network.

In many cases the energy sources in a microgrid are interfaced through power electronic converters feeding harvested power to grid. The loads are also connected to the microgrid. Most of the loads are non-linear in nature which draws non-sinusoidal currents distorting the voltage at the point of common coupling (PCC). To solve this problem, another converter is connected in parallel to the load to reduce the harmonic distortion in the grid currents. This extra inverter circuit is called Power Factor Correction (PFC) circuits. Such PFC circuits are referred as typical active power filters. For a typical user, who has his/her own renewable energy sources and his/her own residential loads, needs two parallel connected inverter for the operation of overall system and the cost of the overall system increases. A higher degree of controllability of converters allows for the possibility of ancillary functions for power quality improvement when converters have unused capacity. This calls for a multi-task converter to supplying the load components and mitigating the electrical disturbances existing on the load currents. This work presents flexible control strategies for Distributed generation (DG) units in microgrids to supply selectively the load current components allowing the DG system to inject its available energy, as well as to work as an active power filter, mitigating load current disturbances and improving power quality. In order to avoid instability in the system and to increase the efficiency of the microgrid operation, a coordinated operation between converters in a microgrid is required. Several methods for DGs power control have been proposed, which can be mainly classified as two types: communication-based and non-communication-based control strategies. In case of short distances, it is reasonable to use a communication link among DG inverters with potential improvement in controllability and
dynamic response and, consequently, in PCC voltage regulation and proper power sharing [3]. However, there are some drawbacks in communication-based approach, such as the requirement for high-bandwidth communication links, which can be an unfeasible and costly solution for microgrids with long distances among the inverters. Long distance communication lines get interfered easier, therefore, reducing system reliability and expandability [3]. However, communication links should be always an enhanced technical solution, since they have the potential to provide better controllability and better load sharing response [4]. Therefore, a proper coordination scheme should be developed in order to meet the operating criteria of the microgrid such as power flow control, voltage support and harmonic mitigation and unbalance compensation.

1.1 Research Objectives

This project aims at broadly developing an advance control technique of DC/AC converters for integration of DG resources as microgrid system. The proposed control technique can:

1) Connect DG resources to the ac grid via two-level and multilevel converters.
2) Supply load power components with accurate and fast dynamic response.
3) Inject the available active power of DG resources to the microgrid continuously.
4) Mitigate load reactive power and increase the power factor of power grid.
5) Mitigate load harmonic current components.
6) Guarantee balanced overall grid currents of unbalanced load.
7) Provide fast dynamic response in tracking rapid variations in load.
8) Regulate load voltage/frequency in a wide range of load conditions in islanded mode of operation.
9) Control distributed power sources in a microgrid in coordination with each other in order to meet the requirements for the electrical network and overcome these challenges.

Note that in AC microgrids, there are four major power components, i.e. active, reactive, harmonic, and unbalance components that need to be coordinated. For DC microgrids, there is only one power component to control i.e. active component which results in simplicity of the control system compared with the AC microgrid case. Therefore, a power sharing scheme should be developed so that the potential of each DG could be exploited at most.
To be fulfilled, the above objectives need to evolve and builds upon a number of tasks. Key tasks are:

1) Development of a supervisory control system for monitoring and measuring loads currents and voltages at PCCs.
2) Development of power electronic interfaces for injection of current/power components under the connection of DG resources to the microgrid.
3) Development of novel reference generation methods for the DG interfacing unit for setting appropriate references of DG control loop circuit.
4) Development of novel current control methods for the DG electronic interface system capable of high power quality current injection of the grid under the presence of grid current distortion, interfacing parameter variation, and converter system delays.
5) Development of novel voltage control methods for the DG electronic interface system capable of fast voltage regulation and effective mitigation of dynamic voltage disturbances.
6) Development of a coordinated operation system for controlling power components among power electronic interfaces for comprehensive duty sharing in the microgrid.

1.2 Organization of the Thesis

This thesis presents a multi-objective control technique of two level and multilevel converter topologies for microgrid operation of distributed generation resources based on renewable energy (and non-renewable energy) resources. The proposed control technique of DG interfacing system is used to improve the quality of power by injection of different current components during integration of DG resources.

Chapter 2 investigates the main similarities and discrepancies among important current decompositions proposed for the compensation of disturbances such as reactive current, asymmetry, unbalances or nonlinearities. Such decompositions and related definitions may influence the power measurement techniques, revenue metering, instrumentation technology and also power conditioning strategies.

Chapter 3 investigates control strategies on the grid side converters of renewable to compensate disturbances caused in presence of reactive, non-linear and/or unbalanced single- and intra-phase loads, in addition to providing active/real power from energy sources. The proposed control
methodology provides decoupled power and current references based on the Conservative Power Theory concept to perform power injection and power conditioning simultaneously offering very flexible, selective and powerful functionalities.

Chapter 4 proposes a platform that enables the coordinated operation of multifunctional distributed generators, aiming at making proper use of DG inverter units’ capability to improve power quality indices at microgrid load buses. In this platform, a multi-master-slave-based control of DGs is proposed in which slaves inject the available energy and compensate selectively unwanted current components of local loads with the secondary effect of having enhanced voltage waveforms while masters share the remaining load power autonomously with distant groups using frequency droop.

Chapters 5 investigate the cascaded multilevel converter topology to provide flexible power conditioning for selective compensation or minimization of particular load disturbances in medium voltage systems. The feature of modularity increases the reliability of the device, making this topology an attractive choice for new applications with enhanced energy efficiency and system reliability.
CHAPTER 2 POWER THEORIES FOR CURRENT DECOMPOSITIONS AND RELATED DEFINITIONS

Electronic systems and several nonlinear loads are being increasingly used since the advent of power electronics. Such devices are usually more efficient and flexible in a wide range of applications, such as AC and DC motor drives, battery chargers, power supplies, UPS, rectifiers and so on. However, the current quality deterioration due to harmonic pollution of switching devices has been increasingly penetrating the utility grid and causing great concerns for the utility companies, operators, and even regular consumers in the local grid [5], [6].

In order to eliminate these harmonics in the electric system, a variety of compensation algorithms were proposed by researchers for switching compensators over the last two decades. These compensation algorithms are derived from electric-power theories that are defined in the frequency domain or in the time domain. The conventional active (P), reactive (Q) and apparent (S) powers, defined in the frequency domain [7]–[9], originally in single-phase circuits and then expanded for three-phase circuits, and several other power quality indices that are derived from them are precise only for off-line calculation and analysis of power quality issues. In general, power definitions in the time domain offer a more appropriate basis for the use in controllers for power electronic devices, because they are also valid during transients. This is especially true if the definitions are done considering already a three-phase circuit instead of considering single-phase circuits and then summing up to have a three-phase system [7].

At the beginning [10], two important approaches to power definitions under non-sinusoidal conditions were introduced by Budeanu in 1927 [9], and Fryze in 1932 [11]. Budeanu worked in the frequency domain, whereas Fryze defined the power in the time domain. In 1983 Akagi, Kanazawa and Nabae proposed a time domain power theory for three-phase circuit for the control of active filters connected to three-phase three-wire systems [12]. This theory is known today as PQ theory [7], [10]. In the literature it can be found other power definitions defined in the time domain. The most important are the Fryze-Buchholz-Depenbrock (FBD) proposed by Depenbrock, [13], the Conservative Power Theory (CPT) proposed by Tenti [14], and the CPC (Current’s Physical Components) proposed by Czarnecki, [15], [16]. Also in the literature we can find p-q theory inspired control algorithms for switching compensators as, for example, the p-q-r theory [17]–[19], which is also defined in the $\alpha\beta0$ reference frame. A comparison involving the
p-q-r and the p-q theories is provided in [19]. The control method denominated as Synchronous Reference Frame (SRF) [20] also presents similar aspects related with the p-q-r and the p-q theories. The SRF method is defined in the $dq0$ reference frame. All of these control algorithms and methods can be applied to control switching compensators connected in three-phase systems, with or without neutral wire. Control algorithms derived from the p-q theory have been widely applied to control switching compensators, and their control algorithms, are well established in the electrical engineering community involved in switching compensators design [7], [10]. However, the PQ theory faces some conceptual problems when it is considered as a power theory for understanding the power properties of the load under non sinusoidal and unbalanced conditions [7], [14], [15], [21]–[24]. It occurs when the real and imaginary currents, derived from the p-q theory, are compared with the active and non-active currents defined by Fryze in 1932 [11].

In this chapter, the main similarities and discrepancies among two important time domain power theories named the instantaneous power (PQ) theory and Conservative Power Theory (CPT) control methods for the compensation of disturbances such as reactive current, asymmetry, unbalances or nonlinearities in the three-phase circuits are studied and a comprehensive comparison from performance and computational complexity perspectives is presented. Although these theories are quite distinct in their formulations, the central idea is to make a comparative study between the current portions and their respective portions of power, in order to show the similarities and divergences between them in terms of characterization of the physical phenomena and in terms of disturbing current compensation. In addition to analyzing performance of different compensation techniques, the computational burden related to the mathematical structure of each technique is also evaluated. A clear understanding of computation burden of each technique helps to choose a technique over another when the computational resources are limited, or select a proper microcontroller for a certain application. Next sections present a concise review of the investigated power theories and related current decompositions. Simulation and experimental results for several cases are discussed and compared in order to point out the major similarities and divergences under different voltage conditions.

2.1 Instantaneous Power Theory (PQ)

The instantaneous real and imaginary power theory (PQ Theory) was published in the IEEE Transactions on Industry Applications in 1984 [25]. The PQ Theory defines a set of instantaneous
powers in time domain. Since no restrictions are imposed on voltage or current behaviors, it is applicable to three-phase systems with or without neutral conductor, as well as to generic voltage and current waveforms. Thus, it is valid for steady and transient states.

Other traditional concepts of powers are characterized by treating a three-phase system as three single-phase circuits. The PQ theory firstly transforms voltages and currents from the \( abc \) to \( \alpha\beta0 \) coordinates, and then defines instantaneous powers on these coordinates. Hence, this theory always considers the three-phase system as a unity, and has the advantage of instantaneously separating homopolar (zero-sequence) from nonhomopolar (positive and negative-sequence) components, which may be present in the instantaneous three-phase four-wire voltages and currents. Indeed, since their instantaneous powers are defined in the \( \alpha\beta0 \) reference frame, it is possible to extract, separately, the homopolar (zero-sequence) component. The PQ theory also allows a comprehensible explanation as to why imaginary power can be compensated without the need of energy storage elements [10], [26]. Besides, it also allows determining the amount of energy that must be stored in a compensation device, in order to compensate oscillating powers that are exchanged between source and load [25], [27].

2.1.1 The Clarke Transformation

The \( \alpha\beta0 \) transformation or the Clarke transformation maps the three-phase instantaneous voltages in the \( abc \) phases, \( v_a, v_b, \) and \( v_c \), into the instantaneous voltages on the \( \alpha\beta0 \) axes \( v_\alpha, v_\beta, \) and \( v_0 \). The Clarke Transformation and its inverse transformation of three-phase generic voltages are given by:

\[
\begin{bmatrix}
v_0 \\
v_\alpha \\
v_\beta
\end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{1}{\sqrt{2}} \\
\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\
0 & -\frac{1}{\sqrt{2}} & \frac{1}{2}
\end{bmatrix} \begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix}
\]

\[
\begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & 1 & 0 \\
\frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\
\frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
v_0 \\
v_\alpha \\
v_\beta
\end{bmatrix}
\]

Similarly, The Clarke Transformation and its inverse transformation of three-phase generic instantaneous line currents, \( i_a, i_b, \) and \( i_c \) are given by (2.2). One advantage of applying the \( \alpha\beta0 \) transformation is to separate zero-sequence components from the \( abc \) phase components. The \( \alpha \) and \( \beta \) axes make no contribution to zero-sequence components.
\[
\begin{bmatrix}
    i_0 \\
i_\alpha \\
i_\beta
\end{bmatrix}
= \sqrt{\frac{2}{3}} \begin{bmatrix}
    \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\
    1 & -\frac{1}{2} & -\frac{1}{2} \\
    \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0
\end{bmatrix}
\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix}
\]

\[
\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix}
= \sqrt{\frac{2}{3}} \begin{bmatrix}
    \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\
    1 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\
    \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix}
\begin{bmatrix}
i_0 \\
i_\alpha \\
i_\beta
\end{bmatrix}
\] (2.2)

No zero-sequence current exists in a three phase, three-wire system, so that \( i_0 \) can be eliminated from the above equations, thus resulting in simplification. If the three-phase voltages are balanced in a four wire system, no zero-sequence voltage is present, so that \( v_0 \) can be eliminated. However, when zero-sequence voltage and current components are present, the complete transformation has to be considered.

If \( v_0 \) can be eliminated from the transformation matrices, the Clarke transformation and its inverse transformation become:

\[
\begin{bmatrix}
v_\alpha \\
v_\beta
\end{bmatrix}
= \sqrt{\frac{2}{3}} \begin{bmatrix}
    1 & -\frac{1}{2} & -\frac{1}{2} \\
    \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0
\end{bmatrix}
\begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix}
\]

\[
\begin{bmatrix}
v_\alpha \\
v_\beta
\end{bmatrix}
= \sqrt{\frac{2}{3}} \begin{bmatrix}
    1 & 0 \\
    -\frac{1}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix}
\begin{bmatrix}
v_a \\
v_\beta
\end{bmatrix}
\] (2.3)

Similar equations hold in the line currents.

2.1.2 The Instantaneous Powers of the PQ Theory

The PQ Theory is defined in three-phase systems with or without a neutral conductor. Three instantaneous powers—the instantaneous zero-sequence power \( (p_0) \), the instantaneous real power \( (p) \), and the instantaneous imaginary power \( (q) \) are defined from the instantaneous phase voltages and line currents on the \( \alpha\beta0 \) axes as [7]:

\[
\begin{bmatrix}
p_0 \\
p \\
q
\end{bmatrix}
= \begin{bmatrix}
v_0 & 0 & 0 \\
0 & v_\alpha & v_\beta \\
0 & v_\beta & -v_\alpha
\end{bmatrix}
\begin{bmatrix}
i_0 \\
i_\alpha \\
i_\beta
\end{bmatrix}
\]

\[
p = v_\alpha i_\alpha + v_\beta i_\beta = \bar{p} + \tilde{p}
\]

\[
q = v_\beta i_\alpha - v_\alpha i_\beta = \bar{q} + \tilde{q}
\]

\[
p_0 = v_0 i_0 = \bar{p}_0 + \tilde{p}_0
\]

(2.4)

where, “−” represents the average and “~” represents the oscillating components of each power.

It is important to point out that differently from other power definitions, the powers defined in (2.4) considers all three-phase voltages and currents. In theories presented in [7], [13]–[16], the definitions are based on single phase voltage and current and therefore do not allow the understanding of what is possible to have with definitions in three-phases voltages and currents as in the PQ theory.
The physical meanings of the instantaneous powers defined in the $\alpha\beta0$ reference frame, including their average and oscillating components are described as follow. The instantaneous real power ($p$) represents the energy, per time unity, that flows from the source to the load (or from the load to the source, if negative) through the three phase wires [10], [28]. The average component of the real power ($\bar{p}$), if positive, constitutes the energy, per time unity, that is transferred from the source to the load. The oscillating component ($\tilde{p}$) corresponds to the energy, per time unit, that is exchanged between the source and the load.

In three-phase electrical circuits (with or without neutral wire) where voltages and currents are only comprised by their fundamental positive-sequence components, the energy transfer is unidirectional, normally from the source to the load. In this case, the instantaneous real power ($p$) contains only its average component ($\bar{p}$). There are also others particular situations in which energy can present a unidirectional transfer from the source to the load as, for example, when voltages and currents present the same harmonic components and; moreover, present the same symmetrical components (positive, negative or zero components). In any other situations, where the voltages and currents are composed by distorted or unbalanced components, the instantaneous real power presents average and oscillating components.

The instantaneous zero-sequence power ($p_0$) results from zero-sequence components of voltages and currents ($v_0$) and ($i_0$). It is important to comment that this power only exists in three-phase circuits with neutral wire. The average component ($\bar{p}_0$) corresponds to the energy, per time unity, that flows from the source to the load using the neutral wire. The oscillating component ($\tilde{p}_0$) corresponds to the energy flow, per time unity, that is exchanged between source and load through the neutral wire. It is important to notice that the average component cannot exist without the presence of oscillating one [10].

The instantaneous three-phase active power ($p_{3\phi}$), determined in $abc$ coordinates, and the instantaneous real power ($p$) and instantaneous zero-sequence power ($p_0$), determined in $\alpha\beta0$ coordinates, can be associated as follows [7]:

$$p_{3\phi} = v_a i_a + v_b i_b + v_c i_c = v_{\alpha} i_{\alpha} + v_{\beta} i_{\beta} + v_0 i_0 = p + p_0$$ (2.5)

There are no zero-sequence current components in three phase three-wire systems, that is $i_0 = 0$. In this case, only the instantaneous powers defined on the $\alpha\beta$ axes exist, because the product
$v_0i_0$ is zero. Hence, in three-phase three wire systems, the instantaneous real power represents the total energy flow per time unity, in terms of $\alpha\beta$ components. In this case, $(p_{3\phi} = p)$. In an electrical system composed by voltages and currents with fundamental positive-sequence components only, it is possible to assure that the instantaneous three-phase active power $(p_{3\phi})$ and the instantaneous real power $(p)$ are equal, presenting only average component $(\bar{p})$. Moreover, as described in [10], [28], [29], in this condition is also possible to affirm that the conventional active power $(P)$ is equal to the instantaneous powers $(p_{3\phi})$ and $(p)$. In any other condition, the active power $(P)$ corresponds only to the average component of the instantaneous active power $(p_{3\phi})$.

It is important to note that the conventional power theory defined reactive power as a component of the instantaneous (active) power, which has an average value equal to zero. Here, the instantaneous imaginary power $(q)$ can be understood as responsible for the energy, per time unit, that is exchanged between the three-phase wires of the electrical system. Therefore, the power that flows in each phase and depends on $(q)$ does not contribute to the energy that flows from the source to the load or vice-versa. The instantaneous three phase reactive power $(q_{3\phi})$, determined in $abc$ coordinates, and the imaginary power can be associated as follows [7]:

$$q_{3\phi} = (v_a - v_b)i_c + (v_b - v_c)i_a + (v_c - v_a)i_b = \sqrt{3}(v\beta i_\alpha - v_\alpha i_\beta) = \sqrt{3} q$$ (2.6)

The instantaneous reactive power $(q_{3\phi})$ is similar to the conventional reactive power $(Q)$ only when the fundamental positive-sequence components of the voltages and currents are considered. When the currents or voltages present harmonic or unbalanced components, the instantaneous power $(q_{3\phi})$ contains average and oscillating components, which makes impossible to compare $(q_{3\phi})$ with $(Q)$.

Based on the aforementioned explanations involving the real, imaginary and zero-sequence powers, the authors of PQ theory conclude that [7]:

- The total energy that flows per time unity, that is, the instantaneous three-phase active power is always equal to the sum of the real and zero-sequence powers.
- In three-phase circuits, with or without neutral wire, it is possible to affirm that the three-phase active power $(p_{3\phi})$ is equal to the conventional active power $(P)$, if the voltages and
currents are only comprised by their fundamental positive-sequence (or only negative-sequence) components.

- The instantaneous imaginary power is only derived from the nonhomopolar components of the voltages and currents. Moreover, there is a power in each phase that depends on the imaginary power, but their three-phase instantaneous sum is always equal to zero.

Based on the real and imaginary powers, together with the phase voltages transformed to $\alpha$ and $\beta$ components, it is possible to determine a set of real and imaginary current components corresponding to these powers. This is very suitable for better explaining the meaning of the powers defined in the PQ Theory. From (2.4), it is possible to write [7]:

\[
\begin{bmatrix}
i_{\alpha} \\
i_{\beta}
\end{bmatrix} = \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \begin{bmatrix} v_{\alpha} & v_{\beta} \\
v_{\beta} & -v_{\alpha}
\end{bmatrix} \begin{bmatrix} p \\
q
\end{bmatrix} = \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \begin{bmatrix} v_{\alpha} & v_{\beta} \\
v_{\beta} & -v_{\alpha}
\end{bmatrix} \begin{bmatrix} p \\
0
\end{bmatrix} + \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \begin{bmatrix} v_{\alpha} & v_{\beta} \\
v_{\beta} & -v_{\alpha}
\end{bmatrix} \begin{bmatrix} 0 \\
i_{\alpha p}
\end{bmatrix} + \begin{bmatrix} 0 \\
i_{\alpha q}
\end{bmatrix} \quad (2.7)
\]

The above current components can be defined as shown below.

Instantaneous real current on the $\alpha$ axis $i_{\alpha p}$:

\[
i_{\alpha p} = \frac{v_{\alpha}}{v_{\alpha}^2 + v_{\beta}^2} p \quad (2.8)
\]

Instantaneous imaginary current on the $\alpha$ axis $i_{\alpha q}$:

\[
i_{\alpha q} = \frac{v_{\beta}}{v_{\alpha}^2 + v_{\beta}^2} q \quad (2.9)
\]

Instantaneous real current on the $\beta$ axis $i_{\beta p}$:

\[
i_{\beta p} = \frac{v_{\beta}}{v_{\alpha}^2 + v_{\beta}^2} p \quad (2.10)
\]

Instantaneous imaginary current on the $\beta$ axis $i_{\beta q}$:

\[
i_{\beta q} = \frac{-v_{\alpha}}{v_{\alpha}^2 + v_{\beta}^2} q \quad (2.11)
\]

Accordingly, the $abc$ real currents, the $abc$ imaginary currents, and zero-sequence currents can be determined by using the same procedure as the below:
The \( abc \) real currents can be determined applying the appropriate inverse Clarke transformation on the real currents as follow:

\[
\begin{bmatrix}
i_{ap} \\
i_{bp} \\
i_{cp}
\end{bmatrix} = \sqrt{2} \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & 1 & 0 \\
\frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\
1 & -\frac{1}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
0 \\
i_{ap} \\
i_{bp}
\end{bmatrix} = \sqrt{2} \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{2} & \frac{\sqrt{3}}{2} \\
\frac{1}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
i_{ap} \\
i_{bp}
\end{bmatrix}
\]

The \( abc \) imaginary currents can be determined applying the appropriate inverse Clarke transformation on the real currents as follow:

\[
\begin{bmatrix}
i_{aq} \\
i_{bq} \\
i_{cq}
\end{bmatrix} = \sqrt{2} \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & 1 & 0 \\
\frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\
1 & -\frac{1}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
0 \\
i_{aq} \\
i_{bq}
\end{bmatrix} = \sqrt{2} \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{2} & \frac{\sqrt{3}}{2} \\
\frac{1}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
i_{aq} \\
i_{bq}
\end{bmatrix}
\]

The \( abc \) zero-sequence currents can be determined applying the appropriate inverse Clarke transformation on the real currents as follow:

\[
\begin{bmatrix}
i_{a0} \\
i_{b0} \\
i_{c0}
\end{bmatrix} = \sqrt{2} \frac{1}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & 1 & 0 \\
\frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\
1 & -\frac{1}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
i_0 \\
0 \\
0
\end{bmatrix} = \sqrt{2} \frac{1}{\sqrt{3}} \begin{bmatrix}
i_0 \\
0 \\
0
\end{bmatrix}
\]

So, the instantaneous three-phase currents (a, b and c) can be decomposed on the following components:

\[
\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} = \begin{bmatrix}
i_{a0} \\
i_{b0} \\
i_{c0}
\end{bmatrix} + \begin{bmatrix}
i_{ap} \\
i_{bp} \\
i_{cp}
\end{bmatrix} + \begin{bmatrix}
i_{aq} \\
i_{bq} \\
i_{cq}
\end{bmatrix}
\]
2.1.3 Power Terms based on PQ theory

The instantaneous power on the α and β coordinates are defined as \( p_\alpha \) and \( p_\beta \), respectively, and are calculated from the instantaneous voltages and currents on the \( \alpha \beta \) axes as follows [7]:

\[
\begin{bmatrix}
p_\alpha \\
p_\beta 
\end{bmatrix} = \begin{bmatrix}
v_\alpha i_\alpha \\
v_\beta i_\beta 
\end{bmatrix} = \begin{bmatrix}
n v_\alpha i_{\alpha p} \\
n v_\beta i_{\beta p} 
\end{bmatrix} + \begin{bmatrix}
n v_\alpha i_{\alpha q} \\
n v_\beta i_{\beta q} 
\end{bmatrix}
\] (2.16)

It was mentioned that in the three-phase, three-wire system, the three-phase instantaneous active power \( (p_{3\phi}) \) in terms of Clarke components is equal to the instantaneous real power \( (p) \). The instantaneous real power can be given by the sum of \( p_\alpha \) and \( p_\beta \). Therefore, rewriting this sum yields the following equation:

\[
p = v_\alpha i_{\alpha p} + v_\beta i_{\beta p} + v_\alpha i_{\alpha q} + v_\beta i_{\beta q}
\] (2.17)

In the above equation, there are two important points. One is that the instantaneous real power is given only by:

\[
v_\alpha i_{\alpha p} + v_\beta i_{\beta p} = p_{\alpha p} + p_{\beta p} = p
\] (2.18)

The other is that the following relation exists for the terms dependent on \( q \):

\[
v_\alpha i_{\alpha q} + v_\beta i_{\beta q} = p_{\alpha q} + p_{\beta q} = 0
\] (2.19)

The above equations suggest the separation of the powers in the following types:

Instantaneous real power on the α axis \( p_{\alpha p} \):

\[
p_{\alpha p} = v_\alpha i_{\alpha p} = \frac{v_\alpha^2}{v_\alpha^2 + v_\beta^2} p
\] (2.20)

Instantaneous imaginary power on the α axis \( p_{\alpha q} \):

\[
p_{\alpha q} = v_\alpha i_{\alpha q} = \frac{v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2} q
\] (2.21)
Instantaneous real power on the β axis $p_{\beta p}$:

$$p_{\beta p} = v_{\beta} i_{\beta p} = \frac{v_{\beta}^2}{v_{\alpha}^2 + v_{\beta}^2} p$$

(2.22)

Instantaneous imaginary power on the β axis $p_{\beta q}$:

$$p_{\beta q} = v_{\beta} i_{\beta q} = \frac{-v_{\alpha} v_{\beta}}{v_{\alpha}^2 + v_{\beta}^2} q$$

(2.23)

The above equations lead to the following important conclusions [7]:

- The sum of the α axis instantaneous real power $p_{\alpha p}$ and the β axis instantaneous real power $p_{\beta p}$ corresponds to the instantaneous real power $p$.
- The sum of $p_{\alpha q}$ and $p_{\beta q}$ is always zero. Therefore, they do not contribute to the instantaneous nor average energy flow between the source and the load in a three phase circuit. This is the reason that they were named instantaneous imaginary power on the α and β axes. The instantaneous imaginary power $q$ gives the magnitude of the powers $p_{\alpha q}$ and $p_{\beta q}$.
- Because the sum of $p_{\alpha q}$ and $p_{\beta q}$ is always zero, their compensation do not need any energy storage element.

2.2 Conservative Power Theory

The Conservative Power Theory (CPT), proposed by Tenti et al. and recently reformulated in [30] is defined in time domain for any operating conditions and it can be applied in polyphase systems, with or without return conductor. The CPT theory proposes power and current’s decomposition in the stationary frame, according to terms which are directly related to electrical characteristics, such as: average power transfer, reactive energy, unbalanced loads and nonlinearities. The basic definitions are recalled hereafter, while additional information can be found in previous publications [30]–[32].

2.2.1 Conservative Power Terms under Periodic Non-sinusoidal Operation

Assuming a generic poly-phase circuit under periodic operation (period $T$), where $(v)$ and $(i)$ are, respectively, the voltage and current vectors and $(\hat{v})$ is the unbiased integral of the voltage vector measured at a given network port (phase variables are indicated with subscript “m”), the following terms were defined:
Active power:

\[ P = \bar{p} = \langle v, i \rangle = \frac{1}{T} \int_{0}^{T} v \cdot i \, dt = \sum_{m=1}^{M} P_m \]  

(2.24)

Instantaneous active power:

\[ p = v \cdot i = \sum_{m=1}^{M} v_m i_m \]  

(2.25)

The active power equals to the average value of the instantaneous active power and represents the average power flowing through the port and it coincides with the conventional definitions. As known, the value of \( P \) does not depend on the voltage reference. Moreover, the active power is a conservative quantity, i.e., it is additive over all network components.

The active power, which corresponds to the average power consumption, is not enough to characterize the network operation, not even in case of passive linear circuits. Power fluctuations and current flows caused by energy storage elements must be also taken into account, and under sinusoidal conditions, this phenomenon is accounted by reactive power \( Q \), which is also conservative and independent of voltage reference.

Extending the reactive power concept to periodic non-sinusoidal operation, the CPT makes reference to reactive energy \( W \) in the following form [30]:

Reactive energy:

\[ W = \bar{w} = \langle \hat{\varnothing}, i \rangle = \frac{1}{T} \int_{0}^{T} \hat{\varnothing} \cdot i \, dt = \sum_{m=1}^{M} W_m \]  

(2.26)

Instantaneous reactive energy:

\[ w = \hat{\varnothing} \cdot i = \sum_{m=1}^{M} \hat{\varnothing}_m i_m \]  

(2.27)

Reactive energy is the average value of Instantaneous reactive energy. It is a new quantity which is related to the average energy conveyed through the port. Moreover, the instantaneous reactive energy is a time function, which requires the integration of the phase voltages. In here, \( \langle \hat{\varnothing} \rangle \) is the vector of unbiased integral of the port voltages. Reactive energy \( W \) is a conservative quantity for
every voltage and current waveform. It can be shown that, due to the Tellegen’s Theorem, the
instantaneous quantities and their average values are conservative for whichever network and
irrespective of voltage and current waveforms [30], [32]. This is not generally true for conventional
reactive power definitions.

It is worth noting that definitions (2.24) to (2.27) hold irrespective of voltage and current
waveforms provided that they are periodic. Moreover, computation of the quantities defined by
(2.24) to (2.27) is directly done in the time domain and requires integration and low-pass filtering
only. Finally, since the conservation property holds in general, active power and reactive energy
are additive quantities in every electrical network. It is important to highlight that under sinusoidal
conditions the terms $p$ and $w$ coincides at any time with the conventional active
($P_{conv} = VI \cos \phi$) and reactive powers ($Q_{conv} = \omega W = VI \sin \phi$), with $\phi$ being the displacement angle
and $\omega$ being the grid frequency [30], [32].

Another relevant, though not conservative, power term characterizing the network operation at
a given port is the apparent power $A = VI$ where $V$ and $I$ are the collective RMS values of phase
voltages and currents and are expressed by the following equations where $M$ is the number of
phases and the summation does not include the neutral wire.

$$V = \sqrt{\langle v, v \rangle} = \sqrt{\sum_{m=1}^{M} V_m^2}, \quad I = \sqrt{\langle i, i \rangle} = \sqrt{\sum_{m=1}^{M} I_m^2} \quad (2.28)$$

2.2.2 Current Terms under Periodic Non-Sinusoidal Operation

The phase currents are decomposed into three basic current components explained below.

2.2.2.1 Basic Current Terms

Consider a generic port of a $M$-phase network and let $v_m$ and $i_m$ be the voltage and current
measured at phase $m$ terminals. We decompose current in order to identify the terms related to
active power $P_m$ and reactive energy $W_m$ absorbed by phase $m$ at the given port [30].

2.2.2.1.1 Active Current

The active current is the minimum phase current (i.e., with minimum RMS value) needed to
convey active power $P_m$. It is expressed by:
\[ i_{am} = \frac{(v_m, i_m)}{\|v_m\|^2} v_m = \frac{P_m}{V_m^2} v_m = G_m v_m, m = 1,2, ... M \rightarrow \] (2.29)

\[ I_a = \sqrt{\sum_{m=1}^{M} I_{am}^2} = \sqrt{\sum_{m=1}^{M} \left( \frac{P_m}{V_m} \right)^2} \]

In (2.29), term \( G_m = \frac{P_m}{V_m^2} \) is the equivalent conductance of phase \( m \). The active current has no impact on reactive energy, as it can easily be shown from (2.29).

### 2.2.2.1.2 Reactive Current

The reactive current is the minimum phase current needed to convey reactive energy \( W_m \). It is expressed by:

\[ i_{rm} = \frac{\langle \hat{v}_m, i_m \rangle}{\|\hat{v}_m\|^2} \hat{v}_m = \frac{W_m}{\hat{V}_m^2} \hat{v}_m = B_m \hat{v}_m, m = 1,2, ... M \rightarrow \] (2.30)

\[ I_r = \sqrt{\sum_{m=1}^{M} I_{rm}^2} = \sqrt{\sum_{m=1}^{M} \left( \frac{W_m}{\hat{V}_m} \right)^2} \]

In (2.30), term \( B_m = \frac{W_m}{\hat{V}_m^2} \) is the equivalent reactivity of phase \( m \). The reactive current has no impact on active power, as it can easily be shown from (2.30).

### 2.2.2.1.3 Void Current

The remaining current term is called void current and is not conveying active power and reactive energy. It is defined by:

\[ i_{vm} = i_m - i_{am} - i_{rm}, m = 1,2, ... M \] (2.31)

### 2.2.2.1.4 Orthogonality

All the aforementioned current terms are orthogonal, thus:

\[ I_m = \sqrt{I_{am}^2 + I_{rm}^2 + I_{vm}^2} \rightarrow I = \sqrt{I_a^2 + I_r^2 + I_v^2} \] (2.32)
Note that active and reactive currents refer to power and energy terms that are conservative in every network and also keep their meaning in presence of distortion, voltage asymmetry, and load unbalance.

2.2.2.2 Balanced Current Terms

As for conventional networks under sinusoidal operation, it makes sense to identify the effects of supply voltage asymmetry and load unbalance, because they both affect power quality. Of course, under non-sinusoidal operation, the traditional approach must be revised and this can easily be done based on the earlier definitions. Notice, first of all, that we use term “unbalance” to characterize the load attitude to perform asymmetrically in the different phases. Instead, term “asymmetry” is associated to an asymmetrical behavior of the supply seen from load terminals. Irrespective of supply asymmetry, load unbalance, and waveform distortion, the following current terms is defined.

2.2.2.2.1 Balanced Active Currents

The balanced active currents are the minimum currents (i.e., with minimum collective RMS value) needed to convey total active power $P = \sum_{m=1}^{M} P_m$ absorbed at the network port. They are given by:

$$i_a^b = \frac{\langle v, i \rangle}{\|v\|^2} v = \frac{P}{V^2} v = G^b v \rightarrow I_a^b = \frac{P}{V^2}$$ (2.33)

In (2.33), coefficient $G^b = P/V^2$ is the equivalent balanced conductance. Note that these currents are the same that would be absorbed by a symmetrical resistive load with same active power consumption as the actual load. Also, note that the balanced active currents track phase voltages ($v$) irrespective of their waveform. Thus, these currents are symmetrical only if the phase voltages are symmetrical. The term “balanced” therefore refers to load symmetry, not to current symmetry.

2.2.2.2.2 Balanced Reactive Currents

Similarly, the balanced reactive currents are the currents with minimum collective RMS value needed to convey total reactive energy $W = \sum_{m=1}^{M} W_m$ absorbed at the port. They are given by:
\[ i^b_j = \frac{\langle \hat{V}, i \rangle}{\|\hat{V}\|^2} \hat{V} = \frac{W}{V^2} \hat{V} = B^b \hat{V} \rightarrow I^b_r = \frac{W}{V^2} \]

In (2.34), coefficient \( B^b = W/\hat{V}^2 \) is the equivalent balanced reactivity. Note that these currents are the same that would be absorbed by a symmetrical reactive load taking same reactive energy as the actual load. Also, note that the balanced reactive currents track voltage integrals \( \langle \hat{V} \rangle \) irrespective of their waveform. Thus, these currents are symmetrical only if the phase voltages are symmetrical. Additionally, in this case, the term “balanced” therefore refers to load symmetry, not to current symmetry.

2.2.2.3 Unbalanced Current Terms

2.2.2.3.1 Unbalanced Active Currents

Unbalanced active currents are defined by:
\[ i^u_a = i_a - i^b_a \rightarrow i^u_{am} = i_{am} - i^b_{am} = (G_m - G^b) v_m, m = 1, 2, \ldots, M \rightarrow \]
\[ I^u_a = \sqrt{\sum_{m=1}^{M} \left( \frac{P_m}{V_m} \right)^2 - \left( \frac{P}{V} \right)^2} \]

Clearly, these currents exist only if the load is unbalanced, i.e., if the equivalent phase conductances differ from each other. Note that the balanced and unbalanced active currents are collectively orthogonal, i.e.
\[ \langle I^u_a, I^b_a \rangle = 0 \rightarrow I^u_a = \sqrt{I^2_a - I^b_a} \]

2.2.2.3.2 Unbalanced Reactive Currents

Similarly, the unbalanced reactive currents are defined by:
\[ i^u_r = i_r - i^b_r \rightarrow i^u_{rm} = i_{rm} - i^b_{rm} = (B_m - B^b) \hat{v}_m, m = 1, 2, \ldots, M \rightarrow \]
\[ I_r^u = \sqrt{\sum_{m=1}^{M} \left( \frac{W_m}{\bar{v}_m} \right)^2 - \left( \frac{W}{\bar{v}} \right)^2} \]

These currents exist only if the equivalent phase reactivities differ from each other. The balanced and unbalanced reactive currents are collectively orthogonal, thus,

\[ \langle i_r^u, i_r^b \rangle = 0 \rightarrow I_r^u = \sqrt{I_r^2 - I_r^b^2} \]

(2.38)

We collectively refer to unbalance currents as the sum of active and reactive unbalance terms, which are orthogonal each other. Thus,

\[ i_u^u = i_u^a + i_u^b \rightarrow I_u^u = \sqrt{I_u^a^2 + I_u^b^2} \]

(2.39)

2.2.2.3.3 Complete Current Decomposition

In conclusion, the phase currents can be split as follows:

\[ i = i_a^b + i_a^b + i_u^a + i_u^b + i_r = i_a^b + i_{na} \]

(2.40)

such that \( i_a^b \) is the balanced active current, \( i_a^b \) is the balanced reactive current, \( i_u^u \) is the unbalance current, \( i_r \) is the void current, and \( i_{na} \) is the non-active current. All terms are orthogonal, thus,

\[ I = \sqrt{I_a^b^2 + I_b^b^2 + I_u^a^2 + I_u^b^2} = \sqrt{I_a^b^2 + I_{na}^2} \]

(2.41)

It should be emphasized once more that the earlier definitions are valid, and keep their physical meaning, for whichever voltage and current waveform, supply asymmetry and load unbalance.

2.2.3 Power Terms under Periodic, Non-sinusoidal Operation

From (2.41), the apparent power defined earlier is decomposed as follows [30]:

\[ A = \sqrt{V^2 I_a^b^2 + V^2 I_r^b^2 + V^2 I_u^a^2 + V^2 I_u^b^2} = \sqrt{P^2 + Q^2 + N^2 + D^2} \]

(2.42)

where,

- \( P = V I_a^b \) is the active power

(2.42.a)
• \( Q = VI_b \) is the reactive power \( (2.42.b) \)
• \( N = VI^u \) is the unbalance power \( (2.42.c) \)
• \( D = VI_v \) is the void power \( (2.42.d) \)

The reactive power is related to the balanced reactive currents and consequently to the reactive energy, but the reactive power can be affected by the grid frequency and voltage distortions, as discussed in [30]–[32]. The unbalance power \( (N = \sqrt{N_a^2 + N_r^2}) \) is associated to imbalances on the phase conductances and reactivities. In the case of single phase circuits, such component vanishes. The distortion power is related to the existence of nonlinear elements or conditions. Additional details can be found in [30]–[32].

2.2.4 Load Conformity Factors

By means of the CPT theory, a set of performance indices based on the orthogonal current/power decomposition can be defined to characterize different aspects of load operation [33], [34]. The general conformity factor is the power factor \( (\lambda) \), which can be calculated in any generic circuit, independently to the waveform distortions or asymmetries and represents the global efficiency of the load, under certain voltage supplying conditions. This power factor definition is affected not only by voltage and current displacement, but also by unbalanced and nonlinear loads. Unit power factor represents current waveforms proportional to voltage waveforms (as in case of balanced resistive loads).

\[
\lambda = \frac{I_a^b}{\sqrt{I_a^b \cdot I_a^b + I_r^b \cdot I_r^b}} = \frac{P}{A} = \frac{P}{\sqrt{P^2 + Q^2 + N^2 + D^2}}
\]

(2.43)

Of course, under sinusoidal and symmetrical (or single-phase) voltage and current conditions, \( (\lambda) \) is equal to the traditional fundamental displacement factor (\( \cos \phi \)), where \( \phi \) is the phase angle between fundamental phase voltage and current. However, this relation is not correct if the grid voltages and/or currents are distorted and/or unbalanced.

The reactivity factor \( (\lambda_Q) \) has been defined as:

\[
\lambda_Q = \frac{I_r^b}{\sqrt{I_r^b \cdot I_r^b + I_r^b \cdot I_r^b}} = \frac{Q}{\sqrt{P^2 + Q^2}}
\]

(2.44)
and it reveals the presence of reactive energy in linear inductors and capacitors, or even fundamental phase shifting caused by non-linear loads (e.g. thyristor rectifiers). For single-phase or balanced three-phase circuits, with sinusoidal supply voltages, $\lambda_Q$ is calculated as $\lambda_Q = (\sin \varphi)$.

The unbalance factor ($\lambda_N$) has been defined as:

$$\lambda_N = \frac{I^u}{\sqrt{I_r^b + I^b + I^u}} = \frac{N}{\sqrt{P^2 + Q^2 + N^2}} \quad (2.45)$$

which indicates possible unbalances on the load equivalent phase impedances (conductances and reactivities). Such factor results zero only if the load is balanced, independently of voltage symmetry or distortion.

In case of sinusoidal and symmetrical supply voltages, the unbalance factor can also be related to the traditional positive, negative and zero sequence unbalance factors, calculated by means of Fortescue’s transformation on the fundamental current waveforms.

Finally, the distortion factor ($\lambda_D$) has been defined as:

$$\lambda_D = \frac{I^v}{\sqrt{I_r^b + I^b + I^u + I^v}} = \frac{N}{\sqrt{P^2 + Q^2 + N^2 + D^2}} \quad (2.46)$$

which reveals the presence of load non-linearities (distortion currents). Considering single-phase or balanced three-phase loads, supplied by ideal voltages, such conformity factor may be associated to the conventional current total harmonic distortion ($THD_I$). $\lambda_D = 0$ means that the load is linear and $G_D$ and $B_D$ are constant over time.

On the basis of the previous definitions, the relationship among the initial global power factor and the other factors can be expressed by:

$$\lambda = \sqrt{(1 - \lambda_Q^2)(1 - \lambda_N^2)(1 - \lambda_D^2)} \quad (2.47)$$

which allows us to independently assess the influence of each conformity factor on the global power factor. Under ideal operation, the reactivity, unbalance and distortion factors are equal to zero, since they express the non-idealities of the power circuits, whereas the $\lambda$ results unitary, since it expresses the circuit efficiency.
2.3 Analysis of Different Compensation Strategies by Means Of Ideal Current Source Models

This section illustrates the application of possible selective compensation strategies for a shunt active filter, on compensating the undesirable currents from an unbalanced nonlinear load [5]. Such strategies are found on PQ and CPT approaches. The main goal is to investigate the performance of the shunt compensator, controlled by means of each control method, to compensate harmonic, unbalanced and reactive currents. Figure 2-1 demonstrates the power circuit corresponding to a three phase sinusoidal voltage source connected to three unbalanced non-linear single-phase loads, via line impedances. In this condition, the load currents may create distorted and unbalanced voltage drops over the line impedances.

Figure 2-1 Three-phase three-wire circuit with nonlinear and unbalanced load.

Table 2-1 depicts the line impedances, grid voltages and load specifications. In here, both symmetrical and asymmetrical voltage source have been considered to improve the understanding of the APF performance, under different voltage conditions and assuming each mentioned control method. It is worth point out that the APF has been simulated by means of ideal current source models, in order to avoid the influence of current controllers and switching frequency when comparing the control strategies.
Table 2-1 Source voltages, line impedance and load parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sinusoidal and Symmetrical voltage sources</td>
<td>( v_a = 127^\circ &lt; 0^\circ, v_b = 127^\circ &lt; -120^\circ, v_b )</td>
</tr>
<tr>
<td></td>
<td>= 127&lt; 120° (( V_{rms} ))</td>
</tr>
<tr>
<td>Sinusoidal and Asymmetrical voltage sources</td>
<td>( v_a = 98^\circ &lt; 0^\circ, v_b = 112^\circ &lt; -120^\circ, v_b )</td>
</tr>
<tr>
<td></td>
<td>= 127&lt; 120° (( V_{rms} ))</td>
</tr>
<tr>
<td>Non sinusoidal and Symmetrical voltage sources</td>
<td>5% of 3rd, 5th, 7th and 9th harmonics</td>
</tr>
<tr>
<td>Line Impedances</td>
<td>( L_l = 1\mu H, R_l = 0.4\Omega )</td>
</tr>
<tr>
<td>Rectifier between phases A and B</td>
<td>( L_s = 1mH, R1 = 3\Omega, C1 = 500\mu F )</td>
</tr>
<tr>
<td>Rectifier between phases B and C</td>
<td>( L_s = 1mH, R2 = 5\Omega, C2 = 150\mu F )</td>
</tr>
<tr>
<td>Rectifier between phases C and A</td>
<td>( L_s = 1mH, R3 = 15\Omega, C3 = 220\mu F )</td>
</tr>
</tbody>
</table>

2.3.1 Symmetrical and Sinusoidal Voltage Source

Figure 2-2 shows the waveforms of voltages and currents at the PCC (Point of Common Coupling), prior to compensation and under symmetrical and sinusoidal voltage source (see Table 2-1).

![Figure 2-2 PCC voltages and currents before compensation with symmetrical and sinusoidal voltage sources.](image)
As expected, the voltage and current waveforms are unbalanced and distorted at the PCC. The voltages deterioration is related to the impact of current flowing through the line impedance. Following, the undesirable currents compensation is discussed considering the two mentioned control techniques (PQ and CPT), under possible different compensation strategies applied to the shunt active filter (APF).

2.3.1.1 Compensation of Unbalanced, Void and Reactive Currents Based on CPT

2.3.1.1.1 Unbalanced currents compensation \( i^u = i^u_d + i^u_r = i_{ref} \):

In this case the goal was to compensate only the unbalanced current components.

![Figure 2-3 Unbalanced currents compensation using CPT.](image)

Note from Figure 2-3 that the compensated currents result practically balanced, but their waveforms remain distorted, as the respective phase voltages.

2.3.1.1.2 Void currents compensation \( i_v = i_{ref} \):

Figure 2-4 shows the case on which the active filter was set to compensate just the void (non-linear) current components. The resulting compensated currents are practically sinusoidal, but they are not balanced and nor were they in phase with the voltages. It can also be observed that the
resultant PCC voltages were unbalanced, but sinusoidal after the current compensation. This occurs for the reason that the harmonics from the loads were compensated.

![Figure 2-4 Void currents compensation using CPT.](image)

2.3.1.1.3 Unbalanced and void currents compensation \((i^u + i^v = i_{ref})\):

This compensation strategy eliminates both the unbalanced and harmonic (void) currents. The currents after compensation were sinusoidal and balanced, but not in phase with voltage, as illustrated in Figure 2-5. The phase voltages at the load side became sinusoidal and balanced after compensation.

2.3.1.1.4 Non active currents compensation \((i_{na} = i - i^b + i^u + i^v = i_{ref})\):

In this case the objective was to compensate all the undesirable characteristics of the load current (reactive, unbalances and harmonics). The compensated currents were practically sinusoidal, balanced and in phase with the voltages, such as in the case of an equivalent balanced resistive load, given that the non-active currents were compensated as illustrated in Figure 2-6. Moreover, it can be noticed that the disturbances associated with the phase voltages were also compensated, because they were imposed by the load.
2.3.1.2 Compensation of Oscillating and Reactive Currents Based on PQ Theory

2.3.1.2.1 Compensation of oscillating active currents \( (i_p = i_{ref}) \):

Figure 2-7 shows the compensation of the oscillating active current absorbed by the load. In this case, the resulting currents are distorted and asymmetrical, because of the load characteristics and
the defined strategy. These deteriorated currents produced voltage drops over the line impedances causing deteriorated load voltages.

Figure 2-7 Load oscillating active current compensation using PQ.

2.3.1.2.2 Compensation of oscillating reactive currents \( i_q = i_{ref} \):

The same considerations from the previous case are applicable. Figure 2-8 shows that after compensating the oscillating reactive current, the load currents are still highly deteriorated and, consequently, the load voltages are affected.

2.3.1.2.3 Compensation of oscillating active and reactive currents \( i_p + i_q = i_{ref} \):

This kind of compensation is applicable when harmonics and unbalanced currents elimination are the most important issues. Now the resulting compensated currents are sinusoidal and balanced, but not in phase with the voltages. The load currents and voltages after compensation are the same as those in unbalanced and void compensation strategy using CPT control method (see Figure 2-5).
Figure 2-8 Load oscillating reactive current compensation using PQ.

2.3.1.2.4 Compensation of oscillating active and total reactive currents \( (i_p + i_q = i_{ref}) \):

The resultant compensated currents are sinusoidal, balanced and in phase with the voltages, such as in the case of a linear, purely resistive load. In this strategy, the resulting currents and voltages after compensation are equal to those from non-active currents compensation using the CPT (see Figure 2-6).

2.3.1.3 Observation

The previous subsections clearly demonstrated that even choosing one of the considered control methods (PQ and CPT), the compensated currents could be substantially different if using different selective compensation strategies. On the other hand, similar results could be obtained by a proper choice of the compensation strategy, independently on which control technique is applied. For example, the results of applying \( (i_u + i_p) \) or \( (i_p + i_q) \), respectively from CPT and PQ methods in three-phase three-wire systems, are the same.

2.3.2 Asymmetrical and Sinusoidal Voltage Source

Assuming the asymmetrical voltage condition from Table 2-1, Figure 2-9 depicts the voltages and currents before compensation. Under such extreme condition, if the CPT is applied to compensate the non-active currents, the resulting currents are sinusoidal, unbalanced and in phase
with their corresponding asymmetrical voltages, as in case of a balanced resistive load (see Figure 2-10).

![Figure 2-9 PCC voltages and currents before compensation with unbalanced voltage source.](image)

![Figure 2-10 Non active currents compensation (CPT).](image)

On the other hand, if using the PQ theory for compensating the load oscillatory real power (oscillating active currents) and the total imaginary power (total reactive currents), the resulting compensated currents are distorted, in order to absorb constant real power from the source. In this
condition, the load voltages would result distorted due to the voltage drop through the line impedances, as it is shown in Figure 2-11. So, it is noticeable that the PQ method, with constant real power strategy (average active current), is not suitable for asymmetrical voltages.

Note from (2.8) to (2.11) that under asymmetrical or distorted voltages, the resulting PQ phase current terms (compensated currents) cannot reproduce the respective instantaneous phase voltages, since the denominator on such equation is not constant. In this case, it would be necessary to use the fundamental positive sequence voltages before the alpha-beta transformation. However, its accuracy is highly dependent on a Phase-Locked Loop (PLL), especially under distorted voltages.

Figure 2-11 Compensation of oscillating active and total reactive currents (PQ).

This case shows that under asymmetrical voltages the results from PQ and CPT can be very different, even if considering the compensation of all disturbing components from each method. The compensated currents using the CPT are sinusoidal and in phase with the voltages; however, they are not balanced. It happens because the resulting currents follow the measured (asymmetrical) voltages. If using the PQ theory, the resulting currents are distorted and unbalanced, in order to keep constant real power (average active currents), even if the denominator of (2.8) to (2.11) is not constant.
2.3.3 Symmetrical and Non-sinusoidal Voltage Source

Assuming a symmetrical and non-sinusoidal voltage source (Table 2-1), Figure 2-12 depicts the PCC voltages and currents prior to the compensation. Under such condition, if the CPT is used for non-active currents compensation, a significant improvement in the PCC voltages can be observed, as illustrated in Figure 2-13.

![Figure 2-12 PCC voltages and currents before compensation with symmetrical non-sinusoidal voltage sources.](image1)

![Figure 2-13 Non active currents compensation (CPT).](image2)
The remaining deterioration is only due to the imposed voltage distortion, since the compensation emulates a balanced resistive load. However, if the standard limits for current distortion were applied, this technique could lead to possible charges to the consumers, if the voltage deterioration were significant. Moreover, the compensated system draws active power from the system at non-fundamental frequencies (those imposed by the voltages –Table 2-1).

Using the PQ theory to compensate the load oscillating active current and the total reactive current, the resulting compensated currents are almost the same as those in non-active currents compensation using CPT (Figure 2-13). Conversely, if the THD of source voltages is bigger than 10%, the resulting compensated currents, using the same PQ strategy, are no longer proportional to the shape of the voltage source. As explained before, this can happen because the denominator of from (2.8) to (2.11) is not constant under distorted voltages. Therefore, other harmonic frequencies may appear after compensation, apart from those in the source voltages.

Figure 2-14 and Figure 2-15 illustrate the compensated currents for both CPT and PQ, respectively, with the above mentioned compensation strategies, when the magnitude of each harmonics in Table 2-1 was increased to 15% of the fundamental component. It can be clearly seen that the compensated currents using CPT behave as for resistive loads.

![Figure 2-14 Non active currents compensation (CPT).](image-url)
However, the compensated currents using PQ control method led to more harmonics compared to its corresponding phase voltage, making the load voltages even more distorted due to the voltage drop through the line impedances.

2.4 Analysis of Different Compensation Strategies by Means of Three-Phase Three-Wire Inverter

In this section, a three-phase prototype was used to validate experimentally the comparative control strategies between CPT and PQ under symmetrical and sinusoidal AC grid voltage conditions [6]. This setup is equipped with a PWM inverter, implemented with the three-phase open-emitter 600V, 20A IRAMX20UP60A module, shown in Figure 2-16, operating at a switching and sampling frequency of 12 kHz. The grid AC voltage is 170V, and the DC voltage source connected in parallel with the VSI DC-link capacitor is providing 380V. The voltage and current LEM Hall-effect sensors have interfacing circuitry with the Delfino TMS320F28335 32-bit floating-point microcontroller unit (MCU) from Texas Instruments, which runs the control algorithm in real-time. The results were captured using a HAMEG HMO724 four channel oscilloscope. Current waveforms are measured using isolated current sensors with the scaling of 100 mv per division representing 1 Ampere.
Figure 2-16 Prototype hardware implementation.

Figure 2-17 shows the schematic diagram of the hardware setup, consisting of a two-level three-phase voltage source inverter (VSI), and the network loads that are connected to an autotransformer at the PCC. The parameters of the inverter are illustrated in Table 2-2. The main goal is to compare CPT and PQ power theories under unbalanced and nonlinear loading conditions, in the active current provision, and harmonic, unbalanced and reactive current compensation when each of the techniques above is applied.
Figure 2-17 Three-phase inverter configuration.

Table 2-2 Three-phase Inverter and load parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase peak voltage</td>
<td>$v_p = 170$ V</td>
</tr>
<tr>
<td>Grid frequency</td>
<td>$f = 60$ Hz</td>
</tr>
<tr>
<td>Maximum output capacity</td>
<td>$S_{max} = 1$ kVA</td>
</tr>
<tr>
<td>Output filter inductor</td>
<td>$L_f = 4$ mH</td>
</tr>
<tr>
<td>Output filter resistor</td>
<td>$R_f = 0.72$ Ω</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>$V_{dc} = 380$ V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s = 12$ kHz</td>
</tr>
<tr>
<td>Sampling Period</td>
<td>$T_s = (1/12000)$ s</td>
</tr>
<tr>
<td>Load filter capacitor</td>
<td>$C_{DC} = 880$ μF</td>
</tr>
<tr>
<td>Load filter resistor</td>
<td>$R_{DC} = 120$ Ω</td>
</tr>
<tr>
<td>Phase load resistors</td>
<td>$R_a = 150$ Ω, $R_b = 50$ Ω, $R_c = 150$ Ω</td>
</tr>
</tbody>
</table>

Figure 2-18 shows the voltage and current waveforms at the PCC without any compensation (with the inverter injecting zero current). The nonlinear load is an uncontrolled rectifier with RC filter at the DC side, representing a usual example of harmonic voltage source (HVS) load in low
voltage distribution systems and the unbalanced load is a three-phase resistive load. The HVS type load models equipment typically for residential or commercial use, because most of it comprises electronic devices such as computers, audio and video equipment, fluorescent and compact lamps. The load currents (channel 3 and channel 4) are non-sinusoidal with a THD of 30%.

Figure 2-18 Before implementing any compensation strategy: PCC voltage (85 V/div) and load current (5 A/div) of phases a and b.

2.4.1 Compensating Load Current Components Based on CPT:

Figure 2-19 to Figure 2-23 present the waveforms of the voltages at the PCC and currents at the inverter terminal for some of the more illustrative injection strategies using CPT theory.

2.4.1.1 Compensation of Reactive Current Component

This strategy as explained aims to compensate for the lag between load voltages and currents, which corresponds to mitigating the load reactive current component. Figure 2-19 shows the inverter is compensating only the balanced reactive current component of the load, that is ($i_{ref} = i^b$). Thus the inverter currents are no longer in phase with the voltages and its currents has $90^\circ$ phase lag with the corresponding phase voltages. This indicates the absence of active power and nonlinearities.
Figure 2-19 Compensation of balanced reactive current component: PCC voltage (85 V/div) and inverter current (0.5 A/div) of phases a and b.

2.4.1.2 Compensation of Unbalance Current Component

The goal in Figure 2-20 is to show the compensation of only the unbalance load current component, which is \( i_{\text{ref}} = i^u \). In this case, the inverter current remains sinusoidal but unbalanced.

Figure 2-20 Compensation of unbalance current component: PCC voltage (85 V/div) and inverter current (0.5 A/div) of phases a and b.
2.4.1.3 Compensation of Residual Current Component

Unlike the preceding strategy, this one involves compensation of only load nonlinearity-related disturbance. Thus, the residual current component should be mitigated. The compensation strategy is illustrated in Figure 2-21 in which the PCC voltage and the inverter current waveforms show the inverter compensates only the load nonlinearity-related disturbance ($i_{\text{ref}} = i_v$).

Figure 2-21 Compensation of void current component: PCC voltage (85 V/div) and inverter current (2 A/div) of phases a and b.

2.4.1.4 Compensation of Unbalance and Residual Current Component

The strategy illustrated in Figure 2-22 involves compensation of both load nonlinearity-related disturbance and unbalanced currents. This compensation strategy is compared later with PQ theory to show the similarities and differences between these techniques when the smart inverter is performing power quality conditioning.

Figure 2-23 illustrates that the grid supplies balanced current active component of the load, ($i_a^b$). The resulting currents are sinusoidal and in phase with the PCC voltages showing the inverter is compensating the load non-active current component.
From Figure 2-24, the inverter duty is to compensate the load constant reactive component, therefore, \( i_{\text{ref}} = i_{\bar{q}} \). This implies that the inverter currents are sinusoidal and balanced, but not in phase with the voltages, as in case of CPT \( (i_{\bar{p}}) \).
Figure 2-24 Compensation of load constant reactive current component: PCC voltage (85 V/div) and inverter current (0.5 A/div) of phases a and b.

Figure 2-25 and Figure 2-26 show the compensation of the oscillatory active current ($i_{ref} = i_\rho$) and the oscillatory reactive current ($i_{ref} = i_\varphi$) absorbed by the load, respectively. In these cases, the resulting currents are distorted and asymmetrical.

Figure 2-25 Compensation of oscillatory active current component: PCC voltage (85 V/div) and inverter current (2 A/div) of phases a and b.
Figure 2-26 Compensation of oscillatory reactive current component: PCC voltage (85 V/div) and inverter current (2 A/div) of phases a and b.

From Figure 2-27, the inverter is set to supply the oscillatory active and reactive currents components of the load, thus, \( i_{ref} = i_p + i_q \). With three-phase loads, the inverter currents in Figure 2-27 is similar to compensation of \( (i_u + i_v) \) in Figure 2-22 in which the inverter compensates both load nonlinearity-related disturbance and unbalanced current based on the CPT.

Figure 2-27 Compensation of oscillatory active and reactive current components: PCC voltage (85 V/div) and inverter current (2 A/div) of phases a and b.
2.5 Computational Complexity and Dynamic Response for each Control Method

In this section the number of math operations for each control method is estimated to allow a better understanding of each technique in terms of computational complexity. This could help choosing an appropriate microcontroller for a particular application, or a control method and strategy for situations where processing resources are limited. The estimate of the number of instructions was based on a commercial digital signal processor from Texas Instruments (F2812) and, for comparison; all low pass filters for PQ and CPT were implemented as moving average filters with 200 positions.

Table 2-3 depicts the math estimates using each method. Thus, two major conclusions can be pointed out: 1) the highest number of math operations occurs with CPT, while PQ has fewer operations; 2) different selective strategies with same control method may result in different number of operations. For example, using CPT the number of instructions can vary from 100 to 507 if non active or void current compensation were applied.

<table>
<thead>
<tr>
<th>Parameters Compensation Strategy</th>
<th>CPT</th>
<th>PQ</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$i_u$</td>
<td>$i_v$</td>
</tr>
<tr>
<td>Sums</td>
<td>29</td>
<td>21</td>
</tr>
<tr>
<td>Subtractions</td>
<td>30</td>
<td>18</td>
</tr>
<tr>
<td>Multiplications</td>
<td>50</td>
<td>42</td>
</tr>
<tr>
<td>Divisions</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>Cos &amp; Sin</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Sqrt</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>Total Number of Instructions</td>
<td>461</td>
<td>507</td>
</tr>
</tbody>
</table>
2.6 Discussions

The decomposition techniques would result in different current injections when using selective compensation strategies. This would help the designer choose the appropriate decomposition technique or the disturbances needed to be compensated especially when the inverter has limited capacity. As a few examples from the studied techniques, we found that under symmetrical and sinusoidal voltage conditions, similar steady state performance could be achieved if the objective was only to compensate the total disturbing currents from each technique.

Under asymmetrical and sinusoidal voltage conditions, we noticed that PQ theory with constant power strategy was not a good solution for flexible control of the inverter since PQ phase current terms cannot reproduce the respective instantaneous phase voltages. In this case, it would be necessary to use the fundamental positive sequence voltages. Compensating the total disturbing currents using CPT method, we noticed that CPT currents were asymmetrical and sinusoidal since they followed the shape of the asymmetrical and sinusoidal voltage waveforms. This means that CPT theory separates disturbances imposed by the load from irregularities caused by the supply. Under non-sinusoidal voltage conditions, we noticed that CPT control method is able to provide unity power factor correction currents in the presence of distorted voltages. However, if the objective is sinusoidal, balanced resulting currents in phase with the corresponding voltages, it would be necessary to use the fundamental positive sequence voltages for both PQ and CPT theories. However, its accuracy is highly dependent on the PLL, especially under distorted voltages.

Moreover, the number of mathematical operations required in each technique was estimated in order to compare the computational complexity of each method. The highest number of math operations occurred with CPT while PQ has less operations. However, different selective strategies within same control method may result in different number of operations; for example, using CPT, the number of instructions can vary if two different compensation strategies such as non-active or void current compensation were applied.

From this comparative study, it is noticed that CPT may be considered a novel approach for the design and control of power conditioners. Due to its decoupled nature, it allows selective reduction of load disturbing effects, in any percentage, to meet whichever consumer or utility criteria. This enhancement occurs because CPT terms are related just to the load undesired characteristic, inherently reducing the impact of non-idealities from the voltage source.
CHAPTER 3 STUDY OF FOUR-LEG GRID-TIED INVERTER WITH LOCAL POWER SOURCE AND SIMULTANEOUS FUNCTIONALITY

In recent years, the concept of decentralizing power generation through the deployment of distributed generators (DGs) has been widely accepted and applied, driven by the growing market of renewable energy sources. These DGs are normally equipped with a switching power interface, acting as front end with the grid. In a modern grid scenario with pervasive use of DGs, the power available from primary side of renewable DGs, such as photovoltaic or wind energy sources are often lower than the power rating of their switching power interfaces, due mainly to their intermittent characteristics. This enables the use of the switching power interface in other operating modes, providing ancillary services such as unwanted current compensation [35]–[37]. Such flexibility is particularly important when there is a large number of reactive, nonlinear, and unbalanced loads such as variable speed drives, light emitting diode lamps, compact fluorescent lamps, etc., and in conditions where the grid might be weak, such as in rural power systems, or in remote areas. However, the rated capacity of the converter plays a significant role in this situation. Normally, the injection of full power available from the local power source into the grid is desired. If this power is less than the converter rating, the remaining available rating could be used to compensate for power quality disturbances, like harmonic pollution, unbalances and reactive power. Therefore, some selective compensation strategies could be used, where the compensation level would be directly related to the available switching power interface capability. In this context, a selective compensation strategy should be considered, since it allows to design the active compensator components (switches, inductors, capacitors etc.) based on a minimum amount of particular disturbing effects (harmonics, unbalances and phase-shift) or selected harmonics and also to enhance the operation of DGs, when operating close to their power/current ratings, considering that priority is always given to active power generation.

Hence, this chapter proposes a multi-task control strategy for distributed generation systems that simultaneously allows the DGs to inject the available energy, as well as to work as an active power filter, mitigating load current disturbances and improving power quality of the grid. The control structure is developed for three-phase four-wire systems providing more functionality to the grid side converter of a renewable system, where both single- and three- phase loads are fed. The key diversity of the proposed methodology with respect to others in the literature is that the developed
control structure on the grid side converter is based on the CPT theory. This choice provides decoupled power and current references for the grid side inverter control, which offers very flexible, selective and powerful functionalities. These qualities make the system to be the benchmark for achieving 100% renewable and sustainable grid with multifunctional capabilities. We investigated and conducted real time software benchmarking in order to evaluate the performance of the proposed control algorithm for full real-time implementation. The control methodology are implemented and validated in hardware-in-the-loop (HIL) system based on the Opal-RT and Texas Instrument DSP. The results corroborated the quality enhancement control, and allowed to exclude passive filters, contributing to a more compact, flexible and reliable electronic implementation of a smart-grid based control.

3.1 Fundamental Formulas

The CPT theory makes use of fundamental formulas in order to define the parts of a current which are decomposed. This section presents these formulas [35].

The average value of a variable $x$ is given by:

$$\bar{x} = \frac{1}{T} \int_{0}^{T} x(t) dt$$  \hspace{1cm} (3.1)

The time-integral of a variable $x$ is given by:

$$x(\tau) = \frac{1}{T} \int_{0}^{T} x(\tau) d\tau$$  \hspace{1cm} (3.2)

The unbiased integral of a variable $x$ is given by:

$$\hat{x}(t) = x(\tau) - \bar{x}$$  \hspace{1cm} (3.3)

where the second term of (3.3) is the average value of (3.2). The unbiased term means the integral does not contain average value.

The time-derivative of a variable $x$ is given by:

$$\ddot{x}(t) = \frac{dx(t)}{dt}$$  \hspace{1cm} (3.4)

The unbiased integral and the time-derivative present the following properties:

$$\ddot{x} = \dddot{x} = 0$$  \hspace{1cm} (3.5)
\(\langle x, \bar{x} \rangle = \langle x, \hat{x} \rangle = 0\)
\(\langle x, \bar{y} \rangle = -\langle \bar{x}, y \rangle\)
\(\langle x, \hat{y} \rangle = -\langle \bar{x}, y \rangle\)
\(\langle \bar{x}, \hat{y} \rangle = \langle \hat{x}, \bar{y} \rangle = -\langle x, y \rangle\)

where \(\langle \cdot, \cdot \rangle\) is the inner product.

The root-mean square (RMS) value of a variable \(x\) is represented by:

\[X_{RMS} = \|x(t)\|\]  \hfill (3.6)

3.2 The Current Decomposition of the CPT in Single-Phase System

An important feature of the CPT theory is the current decomposition. It consists of decomposing any current into five parts. In single-phase systems, these parts are named as active current, reactive current, scattered active current, scattered reactive current and generated current. The scattered active current, scattered reactive current and generated current can be grouped into one part named void current. In three-phase systems, the current has also terms associated to the balance and unbalance characteristics of an unbalanced load.

Decomposing a current is interesting for selective compensation in smart-grids. Parts of a nonlinear load current can be set as reference for distributed energy resources (DERs). By doing that, each DER is responsible to supply a part of the current drained by such load. This increases the range of options for a SC to manage a smart-grid in order to achieve specific goals like loss reduction and optimal operation. Moreover, fast response, robustness over impedance mismatch and protection schemes are easily obtained with current controller.

This section presents the definition of the current decomposition of the CPT theory for single-phase systems.

According to the CPT, any AC current can be divided into three parts, as shown below:

\[i(t) = i_a(t) + i_r(t) + i_v(t)\]  \hfill (3.7)

where the right side contains, respectively, active current \(i_a\), reactive current \(i_r\), and void current \(i_v\). The definition, the physical meaning and how to implement each part are described in the following section.
3.2.1 Active Current

The part of the current named as $i_a(t)$ is the active current. This part is responsible to carry the active power from a source to a load. The active current of the load is given by (3.8).

$$i_a(t) = \frac{\langle v(t), i(t) \rangle}{\|v(t)\|^2} v(t) \quad (3.8)$$

Figure 3-1 presents the implementation of (3.8). The instantaneous voltage and current are multiplied and the result passes through the Avg block. This block calculates the average value of the product of the multiplication, resulting the average power. Later, the average power is divided by the squared value of the voltage RMS. At the end, the resulted signal is multiplied by the voltage.

The last multiplication in Figure 3-1 implies that the active current has the same waveform of the voltage. If the voltage has distortion at 3\textsuperscript{rd} harmonic for instance, the active current will also have distortion at 3\textsuperscript{rd} harmonic. This is expected since the active power is processed at the coincident harmonics in voltage and current.

3.2.2 Reactive Current

The part of the current named as $i_r(t)$ is the reactive current. This part is responsible to carry reactive energy from a source to a load, or vice-versa. The reactive current is given by (3.9).

$$i_r(t) = \frac{\langle \hat{\theta}(t), i(t) \rangle}{\|\hat{\theta}(t)\|^2} \hat{\theta}(t) \quad (3.9)$$

Figure 3-2 presents the implementation of (3.9). Initially, it is calculated the time-integral of the voltage. The result of the integral is subtracted by its average value. The result of this initial process is the unbiased integral of the voltage $\hat{\theta}(t)$. This variable is then multiplied by the angular frequency.
of the system. This multiplication is necessary because the integral of \(\sin(\omega t)\) results in \((1/\omega)\cos(\omega t)\). Once the \(\hat{v}(t)\) is obtained, the procedure to get the reactive current is similar to the active current.

Figure 3-2 Implementation of reactive current given by (3.9).

Similarly to the active current, the reactive current follows shape of the voltage unbiased integral.

### 3.2.3 Void Current

The part of the current named as \(i_v(t)\) is the void current. This part does not carry neither active power nor reactive energy. All the harmonic content of nonlinear current is within this part. The void current is given by (3.10).

\[
i_v(t) = i(t) - i_a(t) - i_r(t)
\]

(3.10)

Figure 3-3 presents the implementation of (3.10). The active and reactive currents are subtracted from the load current.

Figure 3-3 Implementation of void current given by (3.10).

### 3.3 Current Decomposition of the CPT in Three-Phase Systems

This section presents the definition of the current decomposition of the CPT for three-phase systems with four wires. In order to avoid misunderstanding, the phases of the three-phase system
are named with capital letters A, B and C.

3.3.1 Three-Phase Active Current

The three-phase active current is given by (3.11). The definition is the same for the active current for single-phase.

\[
i_a(A, B, C) = \frac{\langle \nu(A, B, C), i(A, B, C) \rangle}{\|\nu(A, B, C)\|^2} \nu(A, B, C)
\]  

(3.11)

The implementation of (3.11) is merely the application of Figure 3-1 for phases A, B and C, respectively.

3.3.2 Three-Phase Reactive Current

The three-phase reactive current is given by (3.12). The definition is the same for the reactive current for single-phase.

\[
i_r(A, B, C) = \frac{\langle \hat{\nu}(A, B, C), i(A, B, C) \rangle}{\|\hat{\nu}(A, B, C)\|^2} \hat{\nu}(A, B, C)
\]  

(3.12)

Similarly, the implementation of (3.12) is the application of Figure 3-2 for phases A, B and C.

3.3.3 Three-Phase Void Current

The three-phase void current is given by (3.13).

\[
i_v(A, B, C) = i(A, B, C) - i_a(A, B, C) - i_r(A, B, C)
\]  

(3.13)

The implementation of (3.13) is the application of Figure 3-3 for phases A, B and C.

3.3.4 Three-Phase Balanced Active Current

The three-phase active current can be divided into two parts as given in (3.14), named as balanced and unbalanced active currents.

\[
i_a(A, B, C) = i_a^b(A, B, C) + i_a^u(A, B, C)
\]  

(3.14)

The right side of (3.14) has two terms. The first is the three-phase balanced active current. This current is responsible to carry active power considering a balanced load and it is given by (3.15).

\[
i_a^b(A, B, C) = \frac{\langle \nu_a i_a \rangle + \langle \nu_b i_b \rangle + \langle \nu_c i_c \rangle}{\|\nu_a\|^2 + \|\nu_b\|^2 + \|\nu_c\|^2} \nu(A, B, C)
\]  

(3.15)
Figure 3-4 presents the implementation of (3.15). Initially, the average power of each phase is obtained as well as the RMS value of each voltage. The average powers are summed up and it is divided by the sum of the RMS voltage of all phase. The result is multiplied by each phase voltage and the three-phase active balanced current is achieved.

\[ i_a(t) \times \text{Avg} \downarrow \]
\[ v_A(t) \]
\[ i_B(t) \times \text{Avg} \downarrow \]
\[ v_B(t) \]
\[ i_C(t) \times \text{Avg} \downarrow \]
\[ v_C(t) \]
\[ v_A(t) \rightarrow \text{RMS} \rightarrow (\cdot)^2 \]
\[ v_B(t) \rightarrow \text{RMS} \rightarrow (\cdot)^2 \]
\[ v_C(t) \rightarrow \text{RMS} \rightarrow (\cdot)^2 \]
\[ + \]
\[ \div \]
\[ i_{aA}(t) \rightarrow \times \rightarrow i_{aB}(t) \]
\[ v_A(t) \]
\[ i_{aB}(t) \rightarrow \times \rightarrow i_{aC}(t) \]
\[ v_B(t) \]
\[ v_C(t) \]

Figure 3-4 Implementation of balanced active current given by (3.15).

3.3.5 Three-Phase Unbalanced Active Current

The second term of (3.14) is the three-phase unbalanced active current. This current is responsible to carry the unbalanced active power considering in an unbalanced load and it is given by (3.16).

\[ i^u_a(A, B, C) = i_a(A, B, C) - i^b_a(A, B, C) \] (3.16)

The implementation of (3.16) is merely the subtraction phase-by-phase of the current obtained in (3.14) by the current obtained in (3.15), as shown in Figure 3-5.
Similarly to the active current, the reactive current can be divided into two parts as given in (3.17), named as balanced and unbalanced reactive currents.

\[
\mathbf{\dot{i}}_r(A,B,C) = \mathbf{i}^b_r(A,B,C) + \mathbf{i}^u_r(A,B,C)
\]  

(3.17)

The first term of (3.17) is the balanced reactive current. This current is responsible to carry reactive energy considering a balanced load and it is given by (3.18).

\[
\mathbf{i}^b_r(A,B,C) = \frac{\langle \hat{v}_a i_a \rangle + \langle \hat{v}_b i_b \rangle + \langle \hat{v}_c i_c \rangle}{\| \hat{v}_a \|^2 + \| \hat{v}_b \|^2 + \| \hat{v}_c \|^2} \hat{v}(A,B,C)
\]

(3.18)

The implementation of (3.18) is similar to the diagram presented in Figure 3-4. The difference is that all phase voltage must be replaced by the unbiased phase voltage \( \hat{v}(t) \).

3.3.6 Three-Phase Balanced Reactive Current

The second term of (3.17) is the three-phase unbalanced reactive current. This current is responsible to carry the unbalanced reactive energy considering an unbalanced load and it is given by (3.19).

\[
\mathbf{i}^u_r(A,B,C) = \mathbf{i}_r(A,B,C) - \mathbf{i}^b_r(A,B,C)
\]

(3.19)

The implementation of (3.19) is similar to that presented in Figure 3.5, with the replacement of active current to reactive one.
3.3.8 Compensation of Unbalanced Load

In order to compensate the unbalance three-phase current for an unbalanced load, it is sufficient to sum (3.16) with (3.19) and use the result as current reference for a DER.

3.4 Three-Phase Four-Leg Grid-Tied Inverter Structure and Control

Figure 3-6 illustrates the schematic diagram of a grid-tied four-leg power electronic interface (PEI) unit, consisting of a four-leg voltage source converter (VSC) and its local loads connected to the distribution network [36], [37]. Three-phase, four-wire inverters have been realized using conventional three-leg converters with “split-capacitor” or four-leg converters [38], [39]. In a three-leg conventional converter, the ac neutral wire is directly connected to the electrical midpoint of the DC bus. In four-leg converter, the ac neutral wire connection is provided through the fourth switch leg. The “four-leg” converter topology has better controllability than the “split-capacitor” converter topology [40]–[42]. The local power source which can be any kind of renewable energy source such as wind, solar and fuel cell, is modelled as an ideal DC current source, $I_{dc}$ in parallel with the VSC DC-link capacitor, $C_{dc}$.

Figure 3-6 Considered grid-tied four-leg inverter with a current source modeled as DG.
The amplitude of current reference for active power injection, \( i_{\text{active},abc} \), is determined by the amount of power delivered by \( I_{dc} \) through the inverter, and its waveform follow the fundamental voltage waveform at the PCC, \( v_{pccabc}^f \), configuring a sinusoidal current synthesis. This results pure sinusoidal currents in phase with the fundamental component of the PCC voltages [43]. The control objective is to allow the local power source to inject the generated power, and to work as an active power filter (APF) for improving power quality based on the CPT theory when the system is not using the full inverter capability to inject active power to the grid. The parameters and values of the grid-tied system and the load are illustrated in Table 3-1. The circuit consists of single- and three-phase linear and nonlinear (balanced and unbalanced) loads.

Table 3-1 Three-phase Four-leg Inverter and load parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase peak voltage</td>
<td>( v_p = 127 ) (Vrms)</td>
</tr>
<tr>
<td>Grid frequency</td>
<td>( f = 60 ) Hz</td>
</tr>
<tr>
<td>Maximum output capacity</td>
<td>( S_{\text{max}} = 15 ) kVA</td>
</tr>
<tr>
<td>Output filter inductor</td>
<td>( L_f = 4 ) mH</td>
</tr>
<tr>
<td>Output filter resistor</td>
<td>( R_f = 0.15 ) Ω</td>
</tr>
<tr>
<td>Output filter capacitor</td>
<td>( C_f = 5 ) μF</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>( V_{dc} = 600 ) V</td>
</tr>
<tr>
<td>DC link capacitor</td>
<td>( C_{dc} = 2 ) mF</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>( f_s = 12 ) kHz</td>
</tr>
<tr>
<td>Sampling Period</td>
<td>( T_s = (1/12000) ) s</td>
</tr>
<tr>
<td>Grid inductor</td>
<td>( L_g = 0.3 ) mH</td>
</tr>
<tr>
<td>Grid resistor</td>
<td>( R_g = 1 ) Ω</td>
</tr>
<tr>
<td>Load inductor</td>
<td>( L_1 = 30 ) mH, ( L_2 = 4 ) mH</td>
</tr>
<tr>
<td>Load capacitor</td>
<td>( C_1 = 220 ) μF</td>
</tr>
<tr>
<td></td>
<td>( R_1 = 1 ) Ω, ( R_2 = 200 ) Ω, ( R_3 = 80 ) Ω, ( R_4 = 30 ) Ω, ( R_5 = 40 ) Ω, ( R_6 = 35 ) Ω, ( R_7 = 150 ) Ω, ( R_7 = 200 ) Ω</td>
</tr>
</tbody>
</table>
3.4.1 Four-Wire DG Inverter Control Strategy

In this section the current-controlled voltage source inverter is designed and modelled. The control scheme for the four-leg grid side inverter is shown in Figure 3-7. The inverter unit control system consists of two feedback control loops [37]. The first loop is a fast loop controlling the output current, showing that $i_{o,abcn}$ can rapidly track their respective reference commands $i^*_{o,abcn}$, while $i^*_{o,n}$ is determined as $i^*_{o,n} = -(i^*_{o,a} + i^*_{o,b} + i^*_{o,c})$. The outer loop is a slower loop regulating the DC-link voltage. The DC-link keeps the power balance between the power which is delivered to the system in the output of the inverter and the power in the DC-link. The desired inverter output current is the summation of the active current provided from the DG ($i_{active}$) and the compensation of unwanted load current disturbances ($i^*_{f}$) delivered by the CPT theory. The block diagram of the system shown in Figure 3-7 is designed in an $abc$ frame based on the classical frequency response analysis method.

![Figure 3-7 Four-wire four-leg grid-tied PEI.](image)

3.4.1.1 Current Controller Derivation

Consider the grid-tied four-leg inverter of Figure 3-6 and the current control loop block diagram of Figure 3-8; the dynamics of the AC-side currents $i_{o,abcn}(t)$ are described by (3.20) and (3.21).
Figure 3-8 Block diagram of the current control loop.

\[
L_f \frac{di_{o,abcn}(t)}{dt} + R_f i_{o,abcn}(t) = v_{o,abcn}(t) - v_{pcc,abcn}(t)
\]  

(3.20)

\[
v_{o,abcn}(t) = G_{inv} m_{o,abcn}(t) = \left(\frac{V_{dc}}{2}\right) m_{o,abcn}(t)
\]

(3.21)

Equation (3.20) represents a system in which \(i_{o,abcn}(t)\) are the state variables, \(v_{o,abcn}(t)\) are the control inputs, and \(v_{pcc,abcn}(t)\) are the disturbance inputs. Based on (3.21), the control input \(v_{o,abcn}(t)\) are proportional to, and can be controlled by, the modulating signal \(m_{o,abcn}(t)\) illustrated in Figure 3-8. Furthermore, the voltage feed-forward compensation is employed to mitigate the dynamic couplings between the four-leg inverter and the AC system, enhancing the disturbance rejection capability of the converter system [44]. The transfer function of the current control scheme, \(G_i(s)\), is determined as in (3.22).

\[
G_i(s) = \frac{i_{o,abcn}(s)}{v_{o,abcn}(s)} = \frac{1}{L_f s + R_f}
\]

(3.22)

For DSP implementation of the control system, in the next step, it’s suggested to convert the functions of continuous plane “s” to the discrete plane “z”. The Plant transfer function in z-domain is obtained by means of the z-transformation. The z-transformation of a transfer function in s-domain, combined to a Zero-Order Holder, is given by (3.23).

\[
G_i(z) = Z \left\{ \frac{(1 - e^{-sT_s})G_i(s)}{s} \right\}
\]  

(3.23)
Transformation is made using the relation \( z = e^{sT_s} \). So, \( G_i(z) \) can be defined as follows [44]:

\[
G_i(z) = (1 - z^{-1})Z \left\{ \frac{G_i(s)}{s} \right\}
\]

(3.24)

To allow the use of the frequency response method design, the conversion of \( G_i(z) \) transfer function from “\( z \)” plane to “\( w \)” plane is performed using the bilinear transform shown in (3.25):

\[
G_i(w) = G_i(z) \bigg|_{z = \frac{1 + \frac{T_s}{2}w}{1 - \frac{T_s}{2}w}} = \frac{-0.01042w + 250}{w + 37.5}
\]

(3.25)

Figure 3-9 presents a comparison between the frequency response of the system transfer function \( G_i(s) \), and digitized plant \( G_i(w) \). In Figure 3-9(a), the Magnitude Bode diagram and in Figure 3-9(b), the Phase Bode diagram of the current control plant in both “\( s \)” and “\( w \)” planes are illustrated, respectively. From Figure 3-9(a), it is noticeable that the frequency response magnitude presents conformity up to 2 kHz, while from Figure 3-9(b) the phase shows substantial error caused by the zero added because of the digitization process.

![Figure 3-9](image)

Figure 3-9 Bode diagram of the current control plant in both “\( s \)” and “\( w \)” planes: (a) Magnitude response, (b) Phase response.

The first step to perform the controller design is to obtain the open-loop current transfer function \( G_{oi}(w) \) as expressed in (3.26) with \( C_i(w) \) the controller of the current control loop, consisting of a lag compensator as (3.27), where the parameters of \( \omega_z \), \( \omega_p \) and \( k_c \) are the zero, pole and the gain of the compensator, respectively.
\[ G_{oi}(w) = \frac{C_i(w)}{R_f + sL_f} \] (3.26)

\[ C_i(w) = \frac{k_c (1 + \frac{w}{\omega_z})}{(1 + \frac{w}{\omega_p})} \] (3.27)

Table 3-2 presents the requirements chosen for current control scheme of the four-leg inverter. The crossover frequency is chosen to be one-tenth of the switching frequency to limit the current loop response to the switching noises. However, it is high enough to achieve a fast dynamic response. The desired phase margin is selected based on the approach introduced in [45] for determining the parameters of the lag compensator in a digitized system. Based on this technique, we choose \( f_z = 0.1f_{ci} \) to ensure that little phase lag is introduced at \( f_{ci} \). In (3.29), the lag controller reduce the system phase by 0.83°.

<table>
<thead>
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<th>Parameter</th>
<th>Value</th>
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</thead>
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<tr>
<td>Desired Phase Margin</td>
<td>( \varphi_{PMi} = 72^\circ )</td>
</tr>
<tr>
<td>Desired cut-off frequency</td>
<td>( f_{ci} = 1.2 ) kHz</td>
</tr>
</tbody>
</table>

The gain and the phase are used to calculate the lag controller design parameters as given by (3.28) and (3.29), respectively.

\[ G_{ci} = -|G_i(f_{ci})| \ dB = 29.17 \ dB = 28.77 \] (3.28)

\[ \varphi_{ci} = \varphi_{PMi} - \angle G_i(f_{ci}) - 180^\circ = -0.83^\circ \] (3.29)

Therefore, the zero, pole and the gain of the lag controller are given by (3.30), (3.31), and (3.32), respectively.

\[ f_z = \frac{f_{ci}}{10} = 120 \) Hz (3.30)

\[ f_p = \frac{(2\pi f_z + 2\pi f_{ci} \cdot \tan(\varphi_{ci}))}{2\pi \cdot \left[ 1 - (2\pi f_z) \cdot \frac{\tan(\varphi_{ci})}{2\pi f_{ci}} \right]} = 102.2 \) Hz (3.31)
\[ k_c = \frac{G_{ci}^2}{(2\pi f_p)^2 + [(2\pi f_c)^2 + (2\pi f_c)^2]^2} = 33.71 \quad (3.32) \]

The frequency response of the open-loop transfer function is illustrated in Figure 3-10. It can be seen that at cross over frequency, the open loop gain of 0 dB and the phase margin of 72° are obtained.

![Figure 3-10 Bode plot of the open loop current transfer function.](image)

The digital implementation of the lag controller (3.33) in the “\(z\)” domain is obtained by transformed back to “\(z\)” plane with a sampling time of \(T_s\) that is also the switching period.

\[ C_i(z) = C_i(w) \bigg|_{w=\frac{2z-1}{T_s z+1}} \quad (3.33) \]

Therefore, the controller transfer function \(C_i(z)\) can be expressed as:

\[ C_i(z) = \frac{n_1 z + n_0}{d_1 z + d_0} \quad (3.34) \]

The numerator parameters of (3.34) are calculated as follows:

\[ n_1 = \frac{k_c (2\omega_p + T_s \omega_z \omega_p)}{2\omega_z + T_s \omega_z \omega_p}, \quad n_0 = \frac{k_c (-2\omega_p + T_s \omega_z \omega_p)}{2\omega_z + T_s \omega_z \omega_p} \quad (3.35) \]
and the denominator parameters are calculated as:

\[ d_1 = 1, \quad d_0 = \frac{(-2\omega_z + T_s\omega_z\omega_p)}{2\omega_z + T_s\omega_z\omega_p} \]  \hspace{1cm} (3.36)

Having a sampling period, \( T_s = (1/12000) \) s, the controller transfer function \( C_i(z) \) can be expressed as:

\[ C_i(z) = \frac{28.8z - 27.1}{z - 0.94} \] \hspace{1cm} (3.37)

### 3.4.1.2 DC-Link Controller Derivation

The current reference, \( i_{active,abc} \), is used to inject the active power delivered from the DG through the inverter. The waveform of the active current reference is defined from the fundamental component of the measured load voltage, \( v_{pcc,abc}^f \), configuring sinusoidal current. Therefore, the active current is a pure sinusoidal current, in phase with the fundamental component of the instantaneous load voltage. Dimensioning of the DC-link voltage controller is determined by the transfer function between the defined current reference and the DC-link voltage.

From power balance of the inverter terminal, we have:

\[ P_{ac} + P_{DG} + P_{cap} = 0 \] \hspace{1cm} (3.38)

\[ \frac{3}{2} v_{pcc,abc}^f i_{active,abc} + V_{dc} I_{dc} + V_{dc} i_{capacitor} = 0 \] \hspace{1cm} (3.39)

where \( i_{capacitor} \) is the DC-link capacitor current and 3/2 factor comes from the average ac power flow using peak values and \( v_{pcc,abc}^f \) represents the fundamental component of the PCC voltage.

From (3.39) the current through the capacitor is:

\[ i_{capacitor} = - \left( \frac{3v_{pcc,abc}^f i_{active,abc}}{2V_{dc}} + I_{dc} \right) \] \hspace{1cm} (3.40)

The same current in terms of voltage across the capacitor is given by:

\[ C_{dc} \frac{dV_{dc}}{dt} = i_{capacitor} \] \hspace{1cm} (3.41)
From (3.40) and (3.41) the differential equation for the DC-link voltage becomes:

$$\frac{dV_{dc}}{dt} = -\frac{1}{C_{dc}} \left( \frac{3v_{pcc,abc}^f i_{active,abc}}{2V_{dc}} + I_{dc} \right)$$

(3.42)

Based on (3.42) the DC voltage is regulated by controlling the active current $i_{active,abc}$. The block diagram of the DC voltage control loop is shown in Figure 3-11.

The DC-link voltage controller $C_{vd}(s)$ is multiplied by $-1$ to compensate for the negative sign of DC bus voltage dynamics. We will select the bandwidth of DC voltage loop to be less than two orders of magnitude smaller than that of the current loop to avoid interaction with the current controller. Therefore, the closed current loop can be assumed ideal for design purposes and replaced by unity. The transfer functions of DC-link voltage control scheme, $G_{vd}(s)$, is presented in (3.43).

$$G_{vd}(s) = \frac{3v_{pcc,abc}^f}{2V_{dc}} \frac{1}{C_{dc}s}$$

(3.43)

For DSP implementation of the DC-link voltage control scheme, $G_{vd}(s)$, is converted from continuous plane “$s$” to the discrete plane “$z$” in (3.44). To allow the use of frequency response method design, the conversion of $G_{vd}(z)$ transfer function from “$z$” plane to “$w$” plane in (3.45) is performed, using the bilinear transform.

$$G_{vd}(z) = (1 - z^{-1})Z \left\{ \frac{G_{vd}(s)}{s} \right\}$$

(3.44)
\[ G_{vdc}(w) = G_{vdc}(z) \bigg|_{z = \frac{1}{1 + \frac{T_s}{2}w}} = \frac{-0.009375w + 225}{w} \]  

(3.45)

Table 3-3 presents the requirements chosen for control scheme of the DC voltage loop. The DC-side capacitor voltage is sensed and compared to the voltage reference. The target phase margin can be negotiated depending on the requirements for the transient settling time and the stability. When a system has a larger phase margin it will be more robust because the parameter variation will not affect the stability.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
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<tr>
<td>Desired Phase Margin</td>
<td>( \phi_{PMvdc} = 60^\circ )</td>
</tr>
<tr>
<td>Desired cut-off frequency</td>
<td>( f_{cvdc} = 10 \text{ Hz} )</td>
</tr>
</tbody>
</table>

Table 3-3 Requirements chosen for DC voltage control scheme.

On the other hand, a bigger phase margin makes the feedback response more sluggish and the system may take a longer time for settling down; therefore, a high frequency noise can propagate on the closed loop transfer function. Typically, a desired phase margin to meet the stability criterion is greater than \( 45^\circ \) [46].

The open loop transfer functions of the DC voltage control loop, \( G_{ovdc}(w) \), is presented in (3.46) with \( C_{vdc}(w) \) the controller of the DC voltage control loop, consisting of a Proportional Integral (PI) compensator as in (3.47), where the parameters of \( k_p \) and \( T \) are the proportional gain and time constant of the compensator, respectively.

\[ G_{ovdc}(w) = C_{vdc}(w)G_{vdc}(w) \]  

(3.46)

\[ C_{vdc}(w) = k_p \left( \frac{wT + 1}{wT} \right) \]  

(3.47)

The gain and the phase to be used for calculating the PI controller parameters are obtained according to (3.48) and (3.49), respectively.

\[ G_{cvdc} = -|G_{vdc}(f_{cvdc})| \text{ dB} = -11.08 \text{ dB} = 0.279 \]  

(3.48)
\[ \varphi_{cvdc} = \varphi_{PMvdce} - \angle G_{vdce}(f_{cvdc}) - 180^\circ = -29.85^\circ \quad (3.49) \]

Therefore, the time constant and proportional of the PI controller are given by (3.50) and (3.51), respectively.

\[ T = \frac{\tan(\varphi_{cvdc} + 90^\circ)}{2\pi f_{cvdc}} = 0.027 \text{ s} \quad (3.50) \]

\[ k_p = \sqrt{\frac{G_{cvdc}^2}{T^2 + (2\pi f_{cvdc})^2}} = 0.24 \quad (3.51) \]

Figure 3-12 shows the frequency response of the open loop DC-link voltage control scheme. It can be seen that at cross over frequency, the open loop gain of 0 dB and the phase margin of 60° are obtained.

Figure 3-12 Bode plot of the open loop DC-link voltage transfer function.

The digital implementation of the PI controller (3.52) in the “z” domain is obtained by transforming it back to “z” plane with a sampling time of \( T_s \) that is also the switching period.

\[ C_{vdce}(z) = C_{vdce}(w)|_{w=\frac{z-1}{T_s z+1}} \quad (3.52) \]
Therefore, the controller transfer function $C_{vdc}(z)$ can be expressed as:

$$C_{vdc}(z) = \frac{n_1 z + n_0}{d_1 z + d_0} \quad (3.53)$$

The numerator and denominator parameters of (3.53) are calculated as:

$$n_1 = \left(\frac{k_p}{2T_s}\right) T_s + k_p, \quad n_0 = \left(\frac{k_p}{2T_s}\right) T_s - k_p, \quad d_1 = 1, \quad d_0 = -1 \quad (3.54)$$

Having a sampling period, $T_s = (1/12000)$s, the controller transfer function $C_{vdc}(z)$ can be expressed as:

$$C_{vdc}(z) = \frac{0.24z - 0.24}{z - 1} \quad (3.55)$$

3.4.2 Analysis of Different Compensation Strategies by Means of Three-Phase Four-Leg Inverter

The control algorithm for the four-leg grid-tied inverter is implemented and validated in HIL system based on the Opal-RT and Texas Instrument DSP. The converter and power grid shown in Figure 3-1 were built inside Matlab/Simulink. Then, the system was compiled inside the real time simulator "Opal-RT". Opal-RT allows precise benchmarking of real-time controllers, with specific sampling for specific control blocks. The control of the converter was implemented in the co-processor DSP (TI TMS230F28335), outside the Opal-RT system. The CPT theory was coded inside the DSP along with the current controllers. A sampling frequency of 12 kHz is used to discretise the signals. The test is implemented for various cases.

3.4.2.1 Active Current Delivery

In this case study, the four-leg inverter is set to deliver active power produced by the DG to the load, ($i_{ref} = i_{active}$), and the remaining active power is delivered to the grid with unity power factor without doing any compensation strategy. Figure 3-13(a) shows the inverter voltages are in phase with the inverter currents meaning only active power is delivered to the load and grid. From Figure 3-13(b), the grid currents are unbalanced, distorted and out of phase with the voltages showing the requirement for power quality improvement. In Figure 3-13(c), it is clear that the utility is supplying the linear and nonlinear single loads through its neutral wire while the inverter neutral current is zero.
Figure 3-13 Active power delivery: (a) PCC voltage and inverter current, (b) PCC voltage and grid current, (c) grid neutral current and inverter neutral current.
3.4.2.2 Active Current Delivery and Reactive Current Compensation

In Figure 3-14, the controller is set to supply the balance reactive current/power component of the load besides the delivery of active power \( i_{ref} = i_{active} + i_r^b \). From the voltage and current waveforms shown in Figure 3-14(a), the inverter is supplying active and reactive power since the inverter currents are no longer in phase with the voltages. The result of this compensation strategy is shown in Figure 3-14(b) in which the void and unbalance current components of the load are supplied by the grid. It can be seen that the grid currents are in phase with the voltages as a result of the reactive current compensation. Figure 3-14(c) shows the grid is supplying the neutral current, related to single phase loads.

3.4.2.3 Active Current Delivery and Reactive and Unbalance Current Compensation

The load considered in the system imposes unbalance component to the grid’s current. Therefore, the CPT, is used to extract the unbalance current/power component of the load. In this study, the aim is to compensate the reactive and unbalance current components caused by the single- and intra-phase loads \( i_{ref} = i_{active} + i_r^b + i_u \). Therefore, the inverter currents are sinusoidal but unbalanced whereas the grid currents are balanced, in phase with PCC voltages but non-sinusoidal as shown in Figure 3-15(a) and Figure 3-15(b) respectively. In this case, the inverter current is responsible for supplying unbalance current component of the single phase loads through its fourth-leg as it is illustrated in Figure 3-15(c). Note that the harmonic current component of the single- and three-phase loads is still supplied by the grid.

3.4.2.4 Active Current Delivery and Non-active Current Compensation

In Figure 3-16 the inverter is set to compensate non-active or undesirable current components of the load currents including all disturbances, i.e. load reactive current, nonlinearities and unbalances \( i_{ref} = i_{active} + i_{na} \). Figure 3-16(a) shows that the inverter current contains non-active current component whereas Figure 3-16(b) shows the grid is absorbing the remaining active current which is not consumed by the load. Note that the active current, exported to the grid is proportional to the instantaneous PCC voltages. As shown in Figure 3-16(c), the grid supplies zero current through its neutral and the inverter is supplying the return current of single phase loads through its fourth-leg.
Figure 3-14 Active and reactive power delivery: (a) PCC voltage and inverter current, (b) PCC voltage and grid current, (c) grid neutral current and inverter neutral current.
Figure 3-15 Active power delivery and reactive and unbalance compensation: (a) PCC voltage and inverter currents, (b) PCC voltage and grid current, (c) grid neutral current and inverter neutral current.
Figure 3-16 Active power delivery and non-active compensation: (a) PCC voltage and inverter currents, (b) PCC voltage and grid current, (c) grid neutral current and inverter neutral current.
3.4.2.5 PCC Conformity Factors

Figure 3-17 shows the PCC conformity factors which is the dynamic response of the multifunctional inverter under selective compensation objectives. It includes the reactivity factor (LandaQ), unbalance factor (LandaN), distortion factor (LandaD), and power factor (Landa) at the PCC. Initially, the measured reactive factor is almost 0.6 due to reactive current supplied by the PCC, while the measured unbalance and distortion factors are 0.23 and 0.05, respectively, resulting in a power factor around 0.76. It can be seen after \( t = 0.5 \)s, the inverter the reactivity factor goes to zero showing the reactive current compensation by the inverter. This increase the power factor above 0.9. Similar behavior happens after the inverter compensates other undesirable current components at the PCC. It can be seen that after \( t = 0.9 \)s, the PCC reaches unity power factor showing presence of only active power component at the grid.

![Figure 3-17 PCC conformity factors under multifunctional mode of operation.](image)

3.4.2.6 Multi-Functional and Active Filter Modes

In this section, two different tests are performed to validate the overall performance of the converter controllers. In Figure 3-18, a test is done to validate the controller when it switches from active power delivery only to active and non-active compensation. From Figure 3-18, at \( t=0.5 \)s, the inverter started providing active power as well as non-active compensation. The DC-link voltage starts to oscillate but kept at its desired value. The grid current becomes sinusoidal and
balanced. The inverter current, on the other hand, becomes unbalanced and nonlinear. The neutral current is produced by the fourth leg of the inverter resulting in zero neutral current at the grid side.

Figure 3-18 Active power delivery and non-active compensation at t=0.5s.

3.5 Discussions

In this chapter, we developed control structures on the grid side converters of renewables such as wind turbine and photovoltaic power systems to carry out the power quality ancillary services in the distribution system instead of only balancing or selling active power to the grids. This is because of the need for power quality improvement in the presence of reactive, non-linear and/or unbalanced loads. We implemented the grid side converter unit based on four-leg voltage source
converters since it has better controllability than the “split-capacitor” converter topology for four-wire systems.

Two feedback control loops were designed for the grid side inverter. The outer loop regulates the DC-link voltage and the inner loop controls the grid-side inverter output current. The commanded current is the summation of the active current provided from the renewable power system and the compensation of undesirable load current disturbances delivered by the CPT theory. Finally, experimental results are provided in order to validate the proposed functionalities of the multifunctional DG control system.
Potion of this chapter is based on the journal paper titled “Cooperative Control of Multi-Master–Slave Islanded Microgrid With Power Quality Enhancement Based on Conservative Power Theory” published in IEEE Transactions on Smart Grid

A. Mortezaei\textsuperscript{2,3}, M. G. Simões\textsuperscript{4}, M. Savaghebi\textsuperscript{5}, J. M. Guerrero\textsuperscript{6}, and A. Al-Durra\textsuperscript{7}

Distributed Generation (DG) systems and microgrids are becoming more and more important as the penetration level of renewable energy increases in power grid [47]–[49]. Intelligent converters interfacing the generation sources and grid are an essential part of such DG and microgrid systems. These interfacing converters can be classified into current-controlled inverters to inject desired current into the grid and voltage-controlled inverters to establish and regulate voltage under autonomous or islanded operating conditions [50], [51].

Various schemes have been proposed in the literature for parallel connection of converters which can be roughly divided into two categories: communication-based [3], [52]–[58] and non-communication-based schemes [3], [52], [59]. Communication-based control of a microgrid system relies on sharing control information among different inverters. When inverters are located in close proximity of each other, methods such as central mode control, master-slave mode control and distributed control can be applied [3], [52], [53]. In the central mode, the control method requires common synchronization signals and current sharing modules [3]. The PLL circuit of each module can ensure the consistency between the frequency and phase of the output voltage and the synchronization signal. Also, the current sharing modules observe the total load and each module tracks the average current to achieve equal current distribution. This method directly adds current error to each inverter unit as a compensation component of the voltage reference in order to eliminate the differences among their output currents. However, this control scheme must include a centralized controller, which makes difficult to expand the system.
In the distributed control method, also represented as the instantaneous average current sharing method, no central controller is needed [3], [54]. All of the inverters take part in the voltage, frequency, as well as the current regulation, while the average current is the shared information for each module. Average current sharing requires a current sharing bus and reference synchronization for the voltage. An additional current control loop is used to enforce each converter to track the same average reference current, provided by the current sharing bus. Gain scheduler is introduced in instantaneous average current sharing scheme, to improve the current and power sharing for a condition, where the line impedance is different among the inverters [55].

In the master/slave control method, the master inverter operates as a voltage source to regulate the system voltage, while the slave inverter acts as a current source to track the output current of the master in order to achieve equal current distribution [3], [56]–[58]. Based on this scheme, inverters do not need any PLL for synchronization since these units are communicated with the master units. The close proximity makes it practical for control signals to be communicated between inverters with the potential to provide better controllability in terms of fast response to load changes, better voltage regulation, and proper power sharing [3], [4]. However, communication-based approaches have some drawbacks including: the need for high-bandwidth communication channels, especially in case of harmonics compensation which can be impractical and costly in microgrids with long connection distances between inverters; and the presence of a unit acting as a central control or a master which creates a single point of failure.

Non-communication-based control relies on the ability of individual DG units to regulate the output voltage and frequency while sharing the active and reactive power demands. A simple non-communication-based power sharing strategy can be realized in the sense of frequency and voltage droop method [59]. The advantage of the droop method is that it does not require communication signals amongst units in parallel; thereby enhancing the reliability of the system at the price of permitting a small error. Some low bandwidth communication can be added to the system so that voltage amplitude and frequency can be adjusted and generators scheduling is allowed. In [60] droop control has applied to control not only active and reactive power but also unbalance and harmonic power. A droop control method based on negative sequence reactive power has been presented in [61] for voltage unbalance compensation. In [62] a capacitive virtual impedance scheme has been presented for LCL-terminated voltage source inverters. The aim of this scheme is to compensate output voltage distortion. However, enhancement of filter output voltage quality...
is achieved at the price of voltage distortion increase at filter capacitance. Furthermore, for a proper load sharing, resistive virtual impedances are added which distorts again output voltage as a result of voltage drop on the virtual resistances. In [63], the secondary control level is applied to manage the selective compensation of sensitive load bus voltage unbalance and harmonics by sending proper control signals to the primary level. First, virtual resistances for fundamental negative sequence and harmonic components are added to improve the current sharing. The improvement is achieved at the expense of voltage distortion increase at DG units terminals and consequently at sensitive load. Furthermore, the addition of these virtual resistances leads to coupling between fundamental positive sequence and other components. After activating selective compensation, sensitive load bus voltage quality is improved. However, the compensation is achieved by the increase of output voltage distortion of DGs. Thus, considering the required power quality, possible practical limitations are still remained.

Therefore, in this chapter, a hybrid cooperative method which is a combination of both communication-based and non-communication-based schemes is proposed. In this proposal, communication links should be always an enhanced technical solution, therefore, DGs located in close proximity could have access to high-bandwidth communication links to provide rapid load sharing response for ancillary functions including voltage support, harmonic mitigation, and unbalance compensation; however, the impracticality of communication between DGs at remote nodes is recognized and the sharing between these groups is accomplished through the voltage and frequency droop methods with virtual impedance or resistive line impedance compensation. With this technique, the disadvantages of communication-based and non-communication-based schemes are overcome partially. Simulation results are presented to demonstrate the effectiveness of the proposed methods.

4.1 Cooperative Control of Four-Leg Interfacing Converters in Islanded Microgrid with Power Quality Enhancement Based on CPT Theory

In this section, a multi-master-slave-based control of four-leg interfacing converters in an islanded microgrid is proposed in which DGs connected to a common bus or located in close proximity operate as a group in master-salve mode, with slaves injecting their available energy and mitigate unwanted or non-active current components of their local nonlinear or unbalanced loads and masters sharing autonomously the remaining load power with distant groups using droop
control. This way, the non-active load current components in each group are compensated locally by the slaves with access to high-bandwidth communication links. As the secondary effect, the enhancement of voltage quality at master inverters terminal and load buses is achieved simultaneously. However, in contrast to conventional master-slave control strategy, where slave units track the current reference provided by the master in order to achieve equal current distribution [3], the slave reference currents in this strategy are synthesized from the load currents based on the CPT theory. The slave units in each group can track the load current at the voltage fundamental frequency which is controlled by the master unit without requiring PLL circuits for the synchronized operation. Since supplying the non-active load current components result in severe voltage distortion at the slave DG units (SDG) terminals or overloading the units interface converters, cooperation of slave units operating only as APF (SAPF) is also required [64]. Supervisory control checks the SDG output voltage THD and if they exceed their maximum allowable value, commands the SAPF to cooperate for reduction of the SDG compensation duty and consequently voltage distortion at their terminals. The major contributions of this section can be summarized as follows:

1) In contrast to conventional master-slave control strategy, the slave reference currents in this strategy are synthesized from the load currents based on the CPT.
2) The non-active load current components in each group are compensated locally by the slaves with access to high-bandwidth communication links.
3) Conventional droop control with resistive line impedance compensation is implemented to have decoupled active and reactive power controllers and proper active power sharing among DGs.
4) Enhancement of the voltage quality at master inverters terminals and also the load buses is achieved simultaneously as the secondary effect of the non-active load current compensation.
5) The slave units do not require PLL circuits for the synchronized operation providing a means for easy expansion of this type of parallel-connected inverters.
6) The cooperation between the SDG and the SAPF is discussed.

4.1.1 Microgrid Structure with Four-Leg Interfacing Converters

Figure 4-1 shows the single line diagram of the proposed multi-master-slave-based islanded microgrid, including groups, A, B, C, D, etc. Group A control structure is shown for illustration. It is composed of a master and a number of slave electronically interfaced DGs. The master
Voltage Source Inverter (VSI) is controlled as a voltage-controlled inverter to establish the load voltage and, simultaneously, to share load current components with the current-controlled or slave VSI-based DGs. Regarding load sharing, it should be noted that the conventional droop method for active and reactive power control is developed based on the predominantly inductive line impedance. However, in low voltage microgrid applications this assumption is challenged since low voltage distribution lines have complex values of the line impedance leading to coupling between P and Q [3], [65]. This, in turn, leads to poor performance of the system if conventional droop control method is applied. To deal with this problem, various methods such as voltage active power droop and frequency reactive power boost (VPD/FQB) droop, complex line impedance based droop, resistive-inductive virtual impedance, and virtual frame transformation have been introduced [3]. In this chapter, compensation of resistive line impedance is implemented to decouple P and Q by a feedback loop which adds the resistive voltage drop across the line impedance to the reference voltage.

Figure 4-1 Proposed multi-master-slave-based autonomous microgrid, including groups, A, B, C, D, etc.
The gain of this feedback loop is equal to the resistive impedance of the line causing to have decoupled active and reactive power controllers and proper active power sharing among DGs.

Figure 4-1 shows the implementation of this current feedback loop. For the sake of simplicity, all VSIs are assumed to have the same topology. Each unit consists of a four-leg VSI, three legs connected through a three-phase LC-filter and equal line impedances to the local network loads, and neutral wire is connected to the fourth leg. The inductance and capacitance of the output filter are $L_f$ and $C_f$, respectively, and $R_f$ models the ohmic loss of the inductor. The effect of DG unit is represented by a DC voltage source, connected in parallel with the VSI DC-link capacitor. The parameters of the microgrid inverters are illustrated in Table 4-1.

Table 4-1 Microgrid Inverters Parameters.

<table>
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<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<td>Phase peak voltage</td>
<td>$v_p = 127$ (Vrms)</td>
</tr>
<tr>
<td>System frequency</td>
<td>$f = 60$ Hz</td>
</tr>
<tr>
<td>Maximum output capacity of inverters</td>
<td>$S_{max} = 20$ kVA</td>
</tr>
<tr>
<td>Output filter inductor</td>
<td>$L_f = 3$ mH</td>
</tr>
<tr>
<td>Output filter resistor</td>
<td>$R_f = 0.1$ Ω</td>
</tr>
<tr>
<td>Output filter capacitor of Masters</td>
<td>$C_{fm} = 30$ µF</td>
</tr>
<tr>
<td>Damping filter capacitor resistor of Masters</td>
<td>$R_d = 0.01$ Ω</td>
</tr>
<tr>
<td>Output filter capacitor of Slaves</td>
<td>$C_{fs} = 2.5$ µF</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>$V_{dc} = 700$ V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s = 20$ kHz</td>
</tr>
<tr>
<td>Sampling Period</td>
<td>$T_s = (1/20000)$ s</td>
</tr>
</tbody>
</table>

An accurate and robust current control scheme is devised with a fast dynamic response, showing that $i_a$, $i_b$, $i_c$ and $i_n$ can rapidly track their respective reference commands $i_{ta}^*$, $i_{tb}^*$, $i_{tc}^*$ and $i_{tn}^*$. It should be pointed out that $i_{tn}^*$ is determined as $i_{tn}^* = -(i_{ta}^* + i_{tb}^* + i_{tc}^*)$. The block diagram of the current control strategy is illustrated in Figure 4-2.
Figure 4-2 Block diagram of the current control scheme.

Figure 4-2 shows the current control loop, where the dynamics of the AC-side currents $i_{o,abc}(t)$ are described by (4.1) and (4.2).

$$L_f \frac{di_{abc}(t)}{dt} + R_f i_{abc}(t) = v_{abc}(t) - v_{abc}(t)$$

(4.1)

$$v_{abc}(t) = G_{inv} m_{abc}(t) = \left(\frac{V_{dc}}{2}\right) m_{abc}(t)$$

(4.2)

The transfer function of the current control plant, $G_{plant,i}(s)$, is determined as in (4.3).

$$G_{plant,i}(s) = \frac{i_{abc}(s)}{v_{abc}(s)} = \frac{1}{L_f s + R_f}$$

(4.3)

To design a digital controller directly in “z” domain, the controlled plant should be digitized first. For microcontroller based control system, the controlled plant could generally be modeled as a sampling switch, zero-order-hold and plant transfer function as shown in Figure 4-1. The “z” domain transfer function of the current plant could be achieved by digitizing the multiplication of zero-order-hold and $G_{plant,i}(s)$ as follows:

$$G_{plant,i}(z) = \text{Z}\left\{1 - e^{-sT_s} s\right\} \cdot G_{plant,i}(s)$$

(4.4)

To allow the use of the frequency response design method, the conversion of $G_{plant,i}(z)$ transfer function from “z” plane to fictitious “w” plane is performed using the bilinear transform, where $T_s$ is sampling period.
\[
G_{\text{plant}_i}(w) = Z \left\{ \frac{1 - e^{-sT_s}}{s} \cdot G_{\text{plant}_i}(s) \right\} \bigg| \begin{array}{c}
Z = \frac{1 + T_s}{1 - T_s/2} \\
= -0.008333w + 333.3 \\
= 33.33
\end{array} = \frac{-0.008333w + 333.3}{w + 33.33} \quad (4.5)
\]

The next step to perform the controller design is to obtain the open loop current transfer function \(G_{oi}(w)\) as expressed in (4.6) with \(C_i(w)\) the each phase controller of the current control loop, consisting of a phase lag compensator as (4.7), where the parameters of \(\omega_z\), \(\omega_p\) and \(k_c\) are the zero, pole and the gain of the compensator, respectively. Furthermore, the voltage feed-forward compensation is employed to mitigate the dynamic couplings between the converter and the AC system, enhancing the disturbance rejection capability of the system.

\[
G_{oi}(w) = \frac{C_i(w)}{R_f + sL_f} \quad (4.6)
\]

\[
C_i(w) = \frac{k_c \left( 1 + \frac{w}{\omega_z} \right)}{\left( 1 + \frac{w}{\omega_p} \right)} \quad (4.7)
\]

Table 4-2 presents the requirements chosen for the current control scheme and the parameters of (4.7) in a digitized system [45].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Phase Margin</td>
<td>(\varphi_{PM_i} = 72^\circ)</td>
</tr>
<tr>
<td>Desired cut-off frequency</td>
<td>(f_{cl} = 2 \text{ kHz})</td>
</tr>
<tr>
<td>Zero frequency of the lag compensator</td>
<td>(f_z = f_{cl}/10 = 200 \text{ Hz})</td>
</tr>
<tr>
<td>Pole frequency of the lag compensator</td>
<td>(f_p = 174.98 \text{ Hz})</td>
</tr>
<tr>
<td>Gain of the lag compensator</td>
<td>(k_c = 41.06)</td>
</tr>
</tbody>
</table>

The frequency response in \(“w”\) domain of the open loop transfer function is illustrated in Figure 4-3. As shown, at the crossover frequency, the open loop gain of 0 dB and the phase margin of \(72^\circ\) are obtained.
For the digital control system implementation in the \( \mathbf{\omega} \) domain, the controller of (4.7) is transformed back to \( \mathbf{\omega} \) plane with a sampling time of \( T_s \). Therefore, the controller transfer function \( C_i(z) \) can be expressed as (4.8):

\[
C_i(z) = C_i(w)|_{w=\frac{2z-1}{T_s z+1}} = \frac{36.06z - 33.86}{z - 0.946} \tag{4.8}
\]

Master inverters in each group are controlled in voltage control mode to establish their local load bus voltage while, at the same time, share the load current components with the slave inverters. Figure 4-4 illustrates the control scheme for regulating \( v_{abc} \). A feed-forward based control strategy is developed in a multiloop voltage control scheme with the current-controlled scheme of Figure 4-2 as the inner loop to regulate load voltage/frequency in a wide range of load conditions [6]. Applying the filter inductor current as the inner loop feedback variable, the inductor current is then measured directly, allowing overcurrent protection to be easily added to the control.

Figure 4-3 Bode plot of the open loop current transfer function.

Figure 4-4 Block diagram of the voltage control scheme.
In Figure 4-4, \( v_{abc}(s) \) is controlled by \( i_{\text{cap} \, abc}^*(s) \) which is the output of the voltage controller. In order for easy understanding of controller design process in “z” domain, a simplified dual-loop control system with sampling switches is illustrated in Figure 4-5 [45].

Thus, the following equations are derived:

\[
E_2 = r - I \tag{4.9}
\]

\[
V = E_2^*D_2^*G_1G_2e^{-Ts}
\]

\[
I = E_2^*D_2^*G_1e^{-Ts}
\]

Figure 4-5 Simplified dual loop block diagram and flow graph.

Hence:

\[
r = E_2 + I = E_2 + E_2^*D_2^*G_1e^{-Ts} \tag{4.10}
\]

Thus:

\[
r^* = E_2^* + E_2^*D_2^*G_1^*e^{-Ts} \tag{4.11}
\]

\[
V^* = E_2^*D_2^*(G_1G_2)^*e^{-Ts}
\]

Transferring to “z” domain:

\[
r(z) = E_2(z) + E_2(z)D_2(z)G_1(z)z^{-1} \tag{4.12}
\]
$$V(z) = E_2(z)D_2(z)G_1G_2(z)z^{-1}$$

Then, the “z” domain transfer function for the voltage plant (ignoring $e^{-Ts} = z^{-1}$, where $T = T_s$, representing one digital signal controller sampling cycle delay) yields:

$$G_{plant,v}(z) = \frac{V(z)}{r(z)} = \frac{D_2(z)G_1G_2(z)}{1 + D_2(z)G_1(z)} \quad (4.13)$$

Observing (4.14), it is possible to find out that the “z” plane transfer function of voltage plant is not the direct multiplication of current closed loop “z” domain transfer function and capacitor “z” domain transfer function. It is their “s” domain transfer function multiplication transferred to “z” domain as a whole, shown as follows, where $T_s$ is sampling period.

$$G_1G_2(z) = Z \left[ \frac{1 - e^{-sT_s}}{s} \cdot \frac{1}{L_fs + r_{lf}} \cdot \frac{RdCs + 1}{Cs} \right] \quad (4.14)$$

And $G_{plant,v}(w)$ is controlled plant as expressed in (4.15).

$$G_{plant,v}(w) = G_{plant,v}(z) \bigg|_{z = \frac{1 + \frac{Ts}{2w}}{1 - \frac{Ts}{2w}}} \quad (4.15)$$

$$= -0.003371w^5 - 1.085 \times 10^4w^4 + 4.246 \times 10^8w^3 +$$

$$+ 5.88 \times 10^{11}w^2 + 2.056 \times 10^{14}w + 6.214 \times 10^{15}w^3 +$$

$$+ 6.19 \times 10^9w^2 + 1.869 \times 10^{11}w - 1.178 \times 10^6$$

In (4.16) the open loop voltage transfer function $G_{ov}(w)$ is expressed, while $C_v(w)$ is the controller of the each phase voltage control loop in “w” plane. The aim is to provide a satisfactory performance with fast dynamic response for system disturbances. This could be achieved using Proportional-Integral (PI) compensators as indicated in (4.17) where the parameters of $k_p$ and $T$ are the proportional and time constant of the converter, respectively.

$$G_{ov}(w) = G_{Plant,v}(w)C_v(w) \quad (4.16)$$

$$C_v(w) = k_p \left( \frac{wT + 1}{wT} \right) \quad (4.17)$$
Table 4-3 presents the requirements chosen for the voltage control scheme and the parameters of (4.17) in a digitized system.

Table 4-3 Requirements chosen for voltage control scheme.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Phase Margin</td>
<td>$\varphi_{PMV} = 50^\circ$</td>
</tr>
<tr>
<td>Desired cut-off frequency</td>
<td>$f_{cv} = 700$ Hz</td>
</tr>
<tr>
<td>Proportional gain of PI controller</td>
<td>$k_p = 0.131$</td>
</tr>
<tr>
<td>Time constant of PI controller</td>
<td>$T = 0.834$ ms</td>
</tr>
</tbody>
</table>

The frequency response in “$w$” domain of the open loop transfer function is illustrated in Figure 4-6. As shown, at the crossover frequency, the open loop gain of 0 dB and the phase margin of $50^\circ$ are obtained.

![Figure 4-6 Open loop voltage transfer function frequency response.](image)

The digital implementation of the voltage controller (4.17) in the “$z$” domain, $C_v(z)$, is also achieved using the bilinear transform with a sampling time of $T_s$ that is also the switching period. Therefore, the controller transfer function $C_v(z)$ can be expressed as:
\[ C_v(z) = C_v(w) \big|_{w=\frac{2 z - 1}{z+1}} = \frac{0.135z - 0.127}{z - 1} \quad (4.18) \]

4.1.2 Load Current Sharing Strategy among DG Inverter Units

Unbalanced or nonlinear loads result in the deterioration of voltage waveforms at load buses which is the direct consequence of voltage drop across the line impedances. The objective of the multi-master-slave-based cooperative control is the network at the load buses is seen resistive from the point of view of the master units that regulates the load buses voltages. This way, master units will be able to establish good quality voltages at load buses. To achieve this, master inverters need to provide only the balanced active current components of the loads to prevent the local load bus voltage in each group from distortion. This way, the non-active load current components in each group compensate locally by the slaves located in close proximity with access to high-bandwidth communication links. The slave units are current-controlled and the output current of slave units tracks the current reference distributed by the supervisory control. The supervisory control in each group has access to the load current, and act as operator/management unit. It decomposes the load current components into different orthogonal current terms, directly related to electrical characteristics, based on the CPT theory and assigns each slave to supply different current components and, therefore, the master inverter supplies the remaining load current simultaneously. Since the slave reference currents are synthesized from the load currents, the slave units in each group can track the load current at the voltage output frequency which is controlled by the master unit. Consequently, the slave units do not require PLL circuits for the synchronized operation providing a means for easy expansion of this type of parallel-connected inverters.

In this study, the design strategy is to assign the non-active load current compensation duty to the SDG to lessen capital investment. However, since the generation and consumption conditions in a microgrid can change considerably, it is probable that the compensation by the SDG leads to overloading of them or excessive voltage distortion at their terminals. In these conditions, SAPF can be considered to be installed at the load buses to address these requirements. A general structure of microgrid with DGs and units operating only as APF are presented in [64]. The cooperation is built on the following rules:
1) The SDG have priority in non-active load current compensation to utilize the available capacities of their interfacing converters while the voltage distortion rate of their terminals and the used capacity of their converters are within the rated limit.

2) While the SDG are compensating loads non-active currents, their output voltage distortions should not exceed from their maximum allowable values. To apply this constraint, voltages THDs of the SDG terminals are evaluated.

3) The SDG interfacing converters should not be overloaded while compensating loads non-active currents. To apply this constraint, output currents of DG units are evaluated.

4) Compensation task of the SAPF should be shared between them so that none of them are overloaded. Like DG units rating power constraints, their output current are evaluated for this purpose.

Voltage THD at the DG terminals and used capacity of the interface converters are computed for each unit and if cooperation is required, proper signal is calculated in the supervisory control and sent to the SAPF to start cooperating for reduction of the DGs compensation duty and consequently voltage distortion at their terminals. Note that the SAPF only cooperate with those DGs needing cooperation. If a group does not compensate entirely its non-active currents, then those currents will be shared by master units. Note that the slave units in each group are aimed to mitigate just their local load non-active currents. The slave units are not supposed to mitigate other unwanted currents that their information is not revealed for their group supervisory control. As mentioned before, conventional droop control with resistive line impedance compensation is applied to share the load active power components between master inverters. This is due to impracticality of communication between groups located at remote nodes. The applied droop control shows excellent performance for active power sharing between master units irrespective of the non-active currents mitigation by the slaves units.

4.1.3 Application Example by Means of Three-Phase Four-Wire Inverters

To evaluate the dynamic performance of the proposed cooperative control strategy, the schematic diagram of the multi-master-slave-based autonomous microgrid of Figure 4-7, was simulated in PSIM software.
The CPT current decomposition has been implemented by means of an algorithm programmed in a standard C compiler, while the controllers were implemented using z-domain transfer functions. Here, the system under study consists of two groups of inverters, groups A and B. Each group involves three sets of four-leg VSI-based DG units connected through line impedances to their local network loads. $L_l$ and $R_l$ represent the inductance and resistance of the inter-group line impedance that connects groups A and B inverters together, respectively. $L_{lA}$, $L_{lB}$, $R_{lA}$, and $R_{lB}$ represent the inductance and resistance of the group A and B line impedances, respectively.

4.1.3.1 Compensation of Non-Active Load Current

The load circuit used in group A and group B is shown in Figure 4-8; it contains balanced and unbalanced linear and non-linear loads. Originally, the system is under load configuration of Figure 4-8 for each group. At $t=0.9s$, another set of load circuit of Figure 4-8 is switched on in group A resulting in load current increment by twice in this group (see Figure 4-12 and Figure 4-13). Load and line impedance parameters are provided in Table 4-4.
Table 4-4 Load and Line Impedance parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Groups A and B Line inductor</td>
<td>( L_{lA} = L_{lB} = 1 \text{ mH} )</td>
</tr>
<tr>
<td>Groups A and B Line resistor</td>
<td>( R_{lA} = R_{lB} = 5 \text{ Ω} )</td>
</tr>
<tr>
<td>Inter groups line inductor</td>
<td>( L_l = 1 \text{ mH} )</td>
</tr>
<tr>
<td>Inter groups line resistor</td>
<td>( R_l = 0.1 \text{ Ω} )</td>
</tr>
<tr>
<td>Load inductor</td>
<td>( L_1 = 50 \text{ mH}, L_2 = 4 \text{ mH}, )</td>
</tr>
<tr>
<td>Load capacitor</td>
<td>( C_1 = 220 \text{ μF} )</td>
</tr>
<tr>
<td>Load resistor</td>
<td>( R_1 = 20 \text{ Ω}, R_2 = 80 \text{ Ω}, R_3 = 100 \text{ Ω}, )</td>
</tr>
<tr>
<td></td>
<td>( R_4 = 70\text{Ω}, R_5 = 40 \text{ Ω}, R_6 = 50 \text{ Ω} )</td>
</tr>
</tbody>
</table>

Figure 4-9 presents groups A and B master inverter voltage waveforms while Figure 4-10 and Figure 4-11 present the group A and B load buses voltages and currents and the current waveforms in each inverter before and after load bus voltage enhancement (t=0.3s), respectively. In groups A and B:
- $v_{\text{ref}A}$ and $v_{\text{ref}B}$: reference voltages,
- $v_{\text{abc}A}$ and $v_{\text{abc}B}$: capacitor voltages,
- $i_{\text{abc}A1}$ and $i_{\text{abc}B1}$: output currents of master inverters $A1$ and $B1$,
- $i_{\text{ref}A2}$ and $i_{\text{ref}B2}$: reference currents of slave inverters $A2$ and $B2$,
- $i_{\text{abc}A2}$ and $i_{\text{abc}B2}$: output currents of slave inverters $A2$ and $B2$,
- $i_{\text{ref}A3}$ and $i_{\text{ref}B3}$: reference currents of slave inverters $A3$ and $B3$,
- $i_{\text{abc}A3}$ and $i_{\text{abc}B3}$: output currents of slave inverters $A3$ and $B3$,
- $v_{\text{load}A\text{abc}}$ and $v_{\text{load}B\text{abc}}$: voltages of $\text{load}A$ and $\text{load}B$,
- $i_{\text{load}A\text{abc}}$ and $i_{\text{load}B\text{abc}}$: currents of $\text{load}A$ and $\text{load}B$.

From Figure 4-9 to Figure 4-11, until $t=0.3s$, the slave inverters gating signals are blocked, and controllers are inactive. Therefore, the local loads are supplied by the group $A$ and $B$ master inverters specified by $i_{\text{abc}A1}$ and $i_{\text{abc}B1}$ with the droop ratio of $(k_{pA1} = \frac{1}{2} k_{pB1})$ and $(k_{qA1} = k_{qB1})$ provided by the respective supervisory control (see Figure 4-12 to Figure 4-17). Since the loads are unbalanced and distorted, due to voltage drop across line impedances, the load buses voltages are also unbalanced and distorted which shows the necessity of voltage quality enhancement at load buses.

![Figure 4-9 Group A and B master inverters voltage waveforms before and after load bus voltage enhancement (t=0.3s).](image-url)
Note that the master inverters supplies the neutral currents associated with single-phase loads through their fourth-legs, that is \((i_{nA1} = i_{\text{load}A_n})\) and \((i_{nB1} = i_{\text{load}B_n})\). The neutral currents include both linear and nonlinear loads among phases and neutral.

At \(t=0.3\)s, the slave inverters start to inject available energy. Group \(A\) slave inverters take one-third of the balance active current/power component of their own local load \((\text{load}A)\), each slave one-sixth, and Group \(B\) slave inverters take two-third of the balance active current/power component of their own local load \((\text{load}B)\), each slave one-third. To improve the load voltage quality, the provision of non-active components are also carried out by the slave inverters meaning that the master inverters need to supply the remaining balanced active component with the droop ratio of \((k_{pA1} = \frac{1}{2} k_{pB1})\). Consequently, since the slave inverters supply non-active current components, the master units see the network at the load buses, as a resistive network ensuring a good quality load bus voltage with THD reduction from 12% to 2%.

![Figure 4-10 Group A load bus voltage and current and the current waveforms in each inverter before and after load bus voltage enhancement (t=0.3s).](image)
Figure 4-11 Group B load bus voltage and current and the current waveforms in each inverter before and after load bus voltage enhancement (t=0.3s).

For this study, the void and unbalanced currents in groups A and B are supplied by slave inverters 2 and 3, respectively. The reference current provided by the group A supervisory control for these inverters are \((i_{r_{ref}A2} = \frac{1}{6}i_a^b + \frac{1}{2}i_b^b + i_y)\) and \((i_{r_{ref}A3} = \frac{1}{6}i_a^b + \frac{1}{2}i_b^b + i_u)\) of loadA. The reference current provided by the group B supervisory control for respective slave inverters 2 and 3 are \((i_{r_{ref}B2} = \frac{1}{3}i_a^b + \frac{1}{2}i_b^b + i_y)\) and \((i_{r_{ref}B3} = \frac{1}{3}i_a^b + \frac{1}{2}i_b^b + i_u)\) of loadB. It is observed from Figure 4-10 and Figure 4-11 that the master inverters no longer supplies the neutral currents associated with single-phase loads and the slave inverters take this task through their fourth-legs, that is \((i_{nA1} = 0, i_{nA2} + i_{nA3} = i_{loadAn})\) and \((i_{nB1} = 0, i_{nB2} + i_{nB3} = i_{loadBn})\). It is noted that in each group the slave inverter 2 supplies the non-linear part of neutral current associated with single-phase loads and the slave inverter 3 supplies the linear part of neutral current associated with single-phase loads.
Note that in [62], the capacitive virtual impedance scheme enhances the LCL-filter output voltage quality at the expense of voltage distortion increase at filter capacitance, thus, in the cases that capacitor voltage quality is also important, a tradeoff should be made between capacitor and output voltage quality. In contrast to [62], [66], in this proposal, the enhancement of master inverters terminals voltage quality and load buses voltage quality is achieved simultaneously as it is shown in Figure 4-9 to Figure 4-11 and no tradeoff is needed to be made between master inverters terminals and load buses voltages quality. It means the line impedances of master inverters will not distort their terminal voltages. For the SDG taking part in compensating loads non-active currents, if the output voltage THD exceeds the maximum allowable value due to compensation, proper signals are calculated in the supervisory control and sent to the SAPF to start cooperating for reduction of the SDG compensation duty and consequently voltage distortion at their terminals.

4.1.3.2 Sharing of Load Components among DG Units

Figure 4-12 to Figure 4-17 illustrates the dynamic performance of the evaluated multi-inverter-based autonomous microgrid. Figure 4-12 and Figure 4-13 illustrate active, reactive, unbalance and distortion power components of the loads in groups A and B inverters. Originally, the system is under identical load configuration for each group. At t=0.9s, another set of load configuration is switched on in group A resulting in load current increment by twice in this group.

![Figure 4-12 Group A Load power components.](image-url)
Figure 4-13 Group B Load power components.

Figure 4-14 to Figure 4-17 show the generated power components by inverters in each group, respectively. Figure 4-14 shows the sharing of loads active power components ($P_{loadA}$) and ($P_{loadB}$) between groups A and B inverters. From Figure 4-14, as it was mentioned before, until $t=0.3s$, all the load currents are supplied by the master inverters in each group. As the ratio of active droop line setting for master inverters is ($k_{pA1} = \frac{1}{2} k_{pB1}$), group A master inverter supplies twice the balanced active power of group B master inverter, ($P_{A1} = 2P_{B1}$). Therefore, group A master inverter not only supplies $loadA$, but also partially supplies $loadB$ as it is shown by ($P_{lineAB}$).

Figure 4-14 Active power sharing.
At t= 0.3s, slave inverters start injecting energy. Group A slave inverters takes one-third of the balance active power component of loadA, each slave one-sixth, and group B slave inverters takes two-third of loadB, each slave one-third. This way, group A master inverter, (P_{A1}), supplies two-third of loadA compared to group B master inverter, (P_{B1}), which supplies one-third of loadB. As a result, (P_{lineAB}) is zero meaning there is no active power transfer between groups A and B.

At t=0.6s the supervisory control sets new ratio for master inverters active power droop slope as \( k_{pA1} = 2 k_{pB1} \) meaning that group B master inverter supplies twice the balanced active power component as group A master inverter (\( P_{B1} = 2P_{A1} \)). Therefore, it not only supplies loadB, but also provides part of loadA in group A. Consequently, (P_{lineAB}) has negative value meaning the direction of active power transfer is from Group B to A.

At t=0.9s, another set of load configuration is switched on in group A resulting in load increment by twice in this group. It can be seen that group B master inverter still supplies twice the balanced active power of group A master inverter (\( P_{B1} = 2P_{A1} \)) as \( k_{pA1} = 2 k_{pB1} \). Note that groups A and B slave inverters now supplies equal amount of active power, as group B slave inverters is set to supply two-third of loadB considering loadA is now twice loadB. Since group A load consumes twice group B load, (P_{lineAB}) has negative value meaning the direction of active power transfer is from Group B to A.

At t=1.2s the supervisory control sets new ratio for master inverters active power droop slope as \( k_{pA1} = k_{pB1} \) meaning that groups A and B master inverters share the same amount of active power components (\( P_{A1} = P_{B1} \)). (P_{lineAB}) is negative showing the power transfer is still from B to A, since group A load consumes twice group B load.

Figure 4-15 shows the sharing of load reactive power component (Q_{loadA}) and (Q_{loadB}) among group A and B inverters. Originally, the system is under identical load configuration for each group. As the ratio of reactive droop line setting for master inverters is \( k_{qA1} = k_{qB1} \), group A and B master inverters share the total balanced reactive power component of loadA and loadB equally, i.e., \( Q_{A1}=Q_{B1} \), with each master inverter supplying its respective local load. As loadA and loadB are identical, (Q_{lineAB}) is negligible meaning that, except for reactive power losses over the inter groups line impedance, there is no reactive power transfer between groups A and B.

After t= 0.3s, the master inverters are no longer supplying the balanced reactive current
component except for reactive power losses over their line impedances, while the groups A and B slave inverters start supplying the balanced reactive current component of their respective local loads, with each slave providing one half as set by their respective supervisory controls.

At $t=0.9s$, another set of load configuration in group A is switched. This means that groups A slave inverters now supplies twice reactive power compared to slave inverters in group B considering $loadA$ is now twice $loadB$. Again, there is no reactive power transfer between groups A and B, and $(Q_{lineAB})$ is negligible showing the inter groups line impedance reactive power losses. Due to the implementation of resistive line impedance compensation in droop control, $P$ and $Q$ are decoupled and changing the ratio of active power droop slope between master inverters in Figure 4-14, has no impact on $Q$, as can be seen in Figure 4-15.

Figure 4-15 Reactive power sharing.

Figure 4-16 and Figure 4-17 show the sharing of unbalance and distortion power components of the loads ($N_{loadA}$ and $N_{loadB}$) and ($D_{loadA}$ and $D_{loadB}$) among group A and B inverters, respectively. Until $t=0.3s$, the master inverters supply the load unbalance and distortion power components equally without unbalance and distortion power transfer between groups A and B as the load for both groups A and B is identical, and therefore, $(N_{lineAB})$ and $(D_{lineAB})$ are zero.
After $t=0.3s$, to improve power quality at the load buses, supervisory control in each group sets slave inverters 2 and 3 to inject the unbalance and distortion power components of the local load, respectively, as illustrated in Figure 4-16 and Figure 4-17. It means slave inverter 2 provides void current and slave inverter 3 supplies unbalanced current in their corresponding groups.

At $t=0.9s$, another set of load configuration is switched on in group A meaning that groups A slave inverters now supplies twice unbalanced and distortion power components compared to slave inverters in group B. It can be seen that there is no distortion and unbalance power transfer between groups A and B, as $(N_{lineAB})$ and $(D_{lineAB})$ are zero.
It is noted from Figure 4-14 to Figure 4-17 that the power components supplied by slave inverter 2 in group A exhibit overshoots at t=0.9s. This is because according to the CPT definitions, any disturbances in the microgrid are reflected in the void current. Since the load changes occurs in group A and the slave inverter 2 in this group is assigned to supply the void current, all the power components supplied by slave inverter 2 in group A are affected during load change at t=0.9s. It is also noted that in Figure 4-17 the inverters void power components exhibit overshoots due to the transitions during the change of the ratio of active droop line setting for master inverters or reference current for slave inverters since these transitions are also considered as disturbances for the CPT and are reflected in void current. However, no unpredictable behavior was found to occur.

4.2 Participation of Single-Phase Interfacing Converters in Three-Phase Islanded Microgrids with Power Quality Enhancement Based on CPT Theory

Since low-voltage (LV) microgrids are often populated by single-phase DG units, taking full advantage of the compensation capability of these units is particularly important. In this paper, participation of single-phase units for selective compensation of load current disturbances with the secondary effect of having enhanced voltage waveforms in an LV three-phase four-wire islanded microgrid is addressed. The control method is based on multi-master-slave operation of power electronic interfaces, and the goal is to have participation of single-phase slave units in each group for injecting their available energy and also compensating selectively the unwanted current components of their corresponding phases while three-phase master units share the remaining load power autonomously with distant groups using frequency droop. The single-phase inverters reference currents for compensation duty in each group are synthesized from the local load currents based on the CPT theory. Simulation results obtained by the PSIM software are presented to demonstrate the validation of the proposed functionalities of the single-phase units.

4.2.1 Microgrid Structure with Participation of Single-phase Interfacing Converters

Figure 4-18 shows the single line diagram of the considered autonomous microgrid of single-phase and three-phase power electronic interfaces. Here, the system under study consists of two groups of inverters, groups A and B. Group A structure is shown for illustration. It involves two set of three-phase master and three sets of single-phase slave VSI units connected to the local network load in group A via different line impedances. The three sets of single-phase slave units are connected to phases $a$, $b$, and $c$, respectively.
The three-phase master units are operated as voltage controlled VSI units to establish the load voltage and, autonomously, share load current components with the current-controlled single-phase VSI units. In general, a variety of structure could be considered for groups A and B. For example, the single-phase slave units can be connected to the terminal of three-phase master units instead of the load bus terminal. This makes the slave units to have the same line impedance as master units. The other consideration could be considering combination of three-phase and single-phase slave units in each group. We consider this in group B. Group B structure involves one set of three-phase master, one set of three-phase and two sets of single-phase slave VSI units connected to the local network load in group B. This way the three-phase slave units share the compensation effort with corresponding phases of the single-phase slave units. The two sets of single-phase slave units are connected to phases \( b \) and \( c \), respectively. In general, in any of these considerations, the slave units are able to share the compensation effort.

The active and reactive power droop controllers are developed based on the compensation of resistive line impedance to avoid the inaccuracy of the power sharing due to the distribution lines [42]. The parameters of the microgrid inverters is the same as Table 4-1. In this structure, the single-phase DC link inverters are half of the three-phase DC link inverters. The load circuits for both groups A and B are shown in Figure 4-19; it contains linear and non-linear loads. Load and
line impedance parameters are provided in Table 4-5.

Figure 4-19 Schematic diagram of the configurable load in groups A and B, (a) block diagram of load A in group A; (b) block diagram of load B in group B.

Table 4-5 Load and Line Impedance parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Groups A and B master line inductors</td>
<td>$L_{lmA} = L_{lmB} = 1$ mH</td>
</tr>
<tr>
<td>Groups A and B slave line inductors</td>
<td>$L_{lsa} = L_{lsb} = 0.5$ mH</td>
</tr>
<tr>
<td>Groups A and B master line resistor</td>
<td>$R_{lmA} = R_{lmB} = 4$ Ω</td>
</tr>
<tr>
<td>Groups A and B slave line resistor</td>
<td>$R_{lmA} = R_{lmB} = 1.5$ Ω</td>
</tr>
<tr>
<td>Inter groups line inductor</td>
<td>$L_l = 1$ mH</td>
</tr>
<tr>
<td>Inter groups line resistor</td>
<td>$R_l = 0.1$ Ω</td>
</tr>
<tr>
<td>Load inductor</td>
<td>$L_1 = 50$ mH</td>
</tr>
<tr>
<td>Load capacitor</td>
<td>$C_1 = 220$ μF</td>
</tr>
<tr>
<td>Load resistors</td>
<td>$R_1 = 30$ Ω, $R_2 = 10$ Ω, $R_3 = 25$ Ω, $R_4 = 15$ Ω, $R_5 = 25$ Ω</td>
</tr>
</tbody>
</table>
4.2.2 Load Current Components Sharing among Single-Phase and Three-Phase DG Inverters

In this section, the objective is to take efficient utilization of the compensation capability of single-phase units in LV microgrids for selective compensation of load current disturbances in order to enhance voltage quality at load buses. The control method is based on multi-master-slave operation of DGs for several network loads in several groups, and the goal is to have a combination of single-phase and three-phase slave units compensate selectively the unwanted current components of local loads connected to their corresponding phases besides injecting their available energy while master inverters share the remaining load power autonomously with distant groups using frequency droops. This way, the load current disturbances can be compensated locally by the participation of single-phase units with access to high bandwidth communication links. The single-phase units are current-controlled and their output current is the summation of the active current generation and the compensation of the non-active current components of their local nonlinear or unbalanced loads activated by the supervisory control. Non-compensation means that the slave units are only injecting active power. The supervisory control in each group has access to the load current, and act as operation/management unit. It decomposes the load current into different orthogonal current terms, based on the CPT theory and assigns slaves to inject their available energy by supplying part of the balanced active current components of the local loads and also to compensate selectively non-active load current component of their corresponding phases if the nominal power capability of the slave units is not fully used to process active power. This way, the master units supply autonomously the remaining load current with distant groups. Droop control method is employed due to impracticality of communication at remote nodes and resistive line impedance compensation is adopted to have decoupled active and reactive power controllers [42]. Since the generation and consumption conditions in a microgrid can change considerably, it is probable that the compensation by these slave units leads to excessive DG output distortion and interface inverters overloading. Therefore, while the slaves are compensating load current disturbances, voltages THDs of their terminals and their output currents should be evaluated [42]. If a group does not compensate entirely its local load current disturbances, then those currents will be shared by the three-phase master units.
4.2.3 Application Examples by Means of Single-Phase and Three-Phase Inverters

To provide a validation of the functionalities of the single-phase units for power quality enhancement in LV three-phase islanded microgrids, the system of Figure 4-18, was simulated in PSIM software. Group A involves two set of three-phase master and three sets of single-phase slave VSI units connected to phases \( a, b \) and \( c \), respectively. Group B involves one set of three-phase master, one set of three-phase and two sets of single-phase slave VSI units connected to phases \( b \) and \( c \), respectively. In groups A and B:

- \( v_{abcA1}, v_{abcA2}, v_{abcB} \): Capacitor voltages of master inverters A1, A2 and B1, respectively.
- \( i_{abcA1}, i_{abcA2}, i_{abcB} \): Output currents of master inverters A1, A2 and B1, respectively.
- \( i_{LA3}, i_{LA4}, i_{LA5} \): Output currents of single-phase slave inverters A3, A4, and A5, connected to phases \( a, b, \) and \( c \), respectively.
- \( P_{A1}, P_{A2}, P_{A3}, P_{A4}, P_{A5} \): Active power provision of VSI units A1, A2, A3, A4, and A5, respectively.
- \( i_{abcB2} \): Output current of three-phase slave inverter B2.
- \( i_{B3}, i_{B4} \): Output currents of single-phase slave inverters B3, and B4, connected to phases \( b \) and \( c \), respectively.
- \( P_{B1}, P_{B2}, P_{B3}, P_{B4} \): Active power provision of VSI units B1, B2, B3, and B4, respectively.
- \( v_{loadAabc}, v_{loadBabc}, i_{loadAabc}, i_{loadBabc} \): Voltages and currents of \( loadA \) and \( loadB \), respectively.

Figure 4-20 and Figure 4-21 present the current waveforms in groups A and B load bus terminals and current waveforms in each VSI unit, respectively, before and after participation of single-phase and three-phase slave units for compensation effort (\( t=0.6s \)). In Figure 4-20, before \( t=0.6s \), the single-phase slave units in group A are injecting their available energy by taking one-fourth of the balanced active current components of their local load (\( loadA \)), (see \( P_{A3}, P_{A4}, P_{A5} \) before \( t=0.6s \) in Figure 4-24). These units supply \( loadA \) balanced active current components equally in each phase to avoid unbalance currents related to active current provision in the three-phase master units as masters supply the remaining load current. In Figure 4-21, group B slave units initially supply zero current (see \( P_{B2}, P_{B3}, P_{B4} \) before \( t=0.6s \) in Figure 4-24), and therefore, the entire load current is supplied by the master units. The three-phase master units supply autonomously the remaining
load current with distant groups using droop control. The local loads supplied by the group A and B master inverters are specified by $i_{abcA1}$ and $i_{abcA2}$, and $i_{abcB1}$, respectively, with the droop ratio of ($k_{pA1} = k_{pA2} = k_{pB1}$) and ($k_{qA1} = k_{qA2} = k_{qB1}$) provided by the respective supervisory control (see $P_{A1}$, $P_{A2}$ and $P_{B1}$ before $t=0.6s$ in Figure 4-24).

After $t=0.6s$, the goal is to have a combination of single-phase and three-phase slave units to compensate selectively the unwanted current components of local loads connected to their corresponding phases besides injecting their available energy. In Figure 4-20, after $t=0.6s$, the additional task of provision non-active current component of $loadA$ in each phase is being performed by the single-phase units. In Figure 4-21, group B single-phase and three-phase slave units take two-third of the balance active current component of their local load ($loadB$).

Figure 4-20 Group A current waveforms before and after compensation of load non-active current components ($t=0.6s$).
Figure 4-21 Group B current waveforms before and after compensation of load non-active current components (t=0.6s).

Phase $a$ of three-phase slave unit of B2 takes two-third of the loadB balance active current component of its corresponding phase since no single phase slave unit is connected to this phase for sharing compensation effort while the balance active current component of other phase of loadB is shared between single-phase and three-phase slave units, each slave supply one-third of its corresponding phase (see $P_{B2}, P_{B3}, P_{B4}$ after t=0.6s in Figure 4-24). This is to avoid unbalance currents related to active current provision in the three-phase master units as masters supply the remaining load current. In addition to injecting their available energy, single-phase and three-phase slave units in group B also share loadB current disturbances. Non-active load current component of loadB in phase $a$ is supplied by phase $a$ of three-phase slave unit of B2 while loadB non-active load current component in other phases is shared equally between single-phase and
three-phase slave units, each slave supply one-half of its corresponding phase. This validates the selective compensation capability of the proposed strategy. For example, single-phase slave unit of B3 connected to phase b in group B supplies half of the loadB balanced reactive, unbalance and void currents of phase b. After t=0.64s, the compensation effort of B3 is changed due to the assumption that B3 is operating close to its power/current limit. The supervisory control assigns the three-phase slave unit of B2 to supply whole non-active current component of this phase. Therefore, single-phase slave unit of B3 only share the balance active current component of phase b of loadB with three-phase slave unit of B2, each slave supply one-third as discussed (see Figure 4-21 after t=0.64s). Note that in the three-phase slave unit of B2, only phase b current go through changes after t=0.64s as illustrated in Figure 4-21.

From Figure 4-20 and Figure 4-21, after t=0.6s the master units only need to supply the remaining portion of the balanced active current component of the loads, which are not supplied by the slave units. This current term is sinusoidal, balanced and in phase with the load voltages. Consequently, due to not supplying non-active load current component, the voltage drops of the three-phase master units across their distribution lines are not distorted, resulting in the decrease of voltage unbalance and harmonic levels and also compensation of fundamental positive sequence of voltages to the value near the rating at master inverters terminal and load buses. Note that compensation effort in Figure 4-20 and Figure 4-21 is performed with the assumption that all the disturbances including balanced reactive current, unbalance current and void current of the local loads can be supplied by the slave units. However, functionalities of active filtering are flexible because of the possibility of being performed selectively. This feature is powerful, especially when the DGS operates close to its power/current limits, where the prioritization of specific electrical disturbance compensation becomes relevant and useful. Also note that providing non-active load current component after t=0.6s, considerably changes the supplied currents of the single-phase units and, therefore, affect their active power generation (see $P_{A3}, P_{A4}, P_{A5}$ before and after t=0.6s in Figure 4-24).

Figure 4-22 presents the groups A and B three-phase master units output voltage waveforms. It is shown that the improvement of master units terminal voltage quality and load bus voltage quality is achieved simultaneously (after t=0.6s) as the secondary effect of selective non-active load current compensation of phases with participation of single-phase units.
Figure 4-23 presents the groups A and B load buses voltage waveforms. Due to sharing only load active current component by the three-phase master units, their line impedances will no longer distort load buses voltage waveforms.

Figure 4-22 Group A and B master inverters voltage waveforms before and after compensation of load non-active current components (t=0.6s).

Figure 4-23 Groups A and B load buses voltage waveforms before and after compensation of load non-active current components (t=0.6s).
This ensures good quality voltages on the load buses, with a reduction in their THD from 6% to less than 2% (after t=0.6s).

Figure 4-24 shows the sharing of the loads active power components between groups A and B inverters. From Figure 4-24, until t=0.3s, all the loads currents is supplied by the master units in each group. As the ratio of active droop line setting is \( k_{pA1} = k_{pA2} = k_{pB1} \), master units share the same amount of active power components \( P_{A1} = P_{A2} = P_{B1} \). Therefore, group A master units generate twice the balanced active power of group B master inverter, \( P_{A1} + P_{A2} = 2P_{B1} \). This means group A master inverters not only supply \textit{loadA}, but also partially supply \textit{loadB} as it is shown by \( P_{\text{lineAB}} \). Note that \( P_{\text{lineAB}} \) is positive meaning the direction of active power transfer is from group A to B.

At t= 0.3s, single-phase slave units in groups A start supplying one-fourth of the balanced active current components of \textit{loadA}. Yet, the remaining loads active power are shared between groups A and B three-phase master units with the predefined share factors. After t=0.6s, supervisory control in each group assigns slaves to compensate the non-active current components of their local nonlinear or unbalanced loads. Besides that, single-phase and three-phase slave units in groups B take two-third of the balance active current component of \textit{loadB}.

![Figure 4-24 Active power sharing among VSI units.](image)
Note that compensating load unbalance current component by the single-phase units changes their active power provision after $t=0.6s$. This is clear for group A single phase slave units since its slave active power provision changes before and after $t=0.6s$ as illustrated in Figure 4-24. Since $P_{\text{line}AB}$ has negative value, the direction of active power transfer is from group B to A.

At $t=0.9s$ the supervisory control sets new active power droop slope for three-phase master units as $(k_{pB1} = \frac{2}{3} k_{pA1} = \frac{1}{3} k_{pA2})$, meaning that group B master unit generates the same as the total summation of group A master units, $(P_{B1} = P_{A1} + P_{A2})$. Since $P_{\text{line}AB}$ become more negative, more active power is transferred from group B to A.

At $t=1.3s$ the supervisory control again changes ratio for the master units active power droop slope as $(k_{pA1} = \frac{1}{3} k_{pA2} = \frac{2}{3} k_{pB1})$, meaning that group A master units generate twice group B master unit, $(P_{A1} + P_{A2} = 2P_{B1})$.

At $t=1.7s$ the supervisory control sets new active power droop slope for three-phase master units. As the news ratio of active droop line setting is $(k_{pA1} = \frac{2}{3} k_{pA2} = \frac{1}{3} k_{pB1})$, group A master units generate fifth times more than that of group B master unit, $(P_{A1} + P_{A2} = 5P_{B1})$. Notice that inside group A, the three-phase master unit A1 generates one and a half times the three-phase master unit A2 as $(k_{pA1} = \frac{2}{3} k_{pA2})$.

4.3 Discussions

In this chapter, a platform that enables the coordinated operation of multifunctional distributed generators is investigated, aiming at making proper use of DG inverter units’ capability to improve power quality indices at microgrid load buses. In this platform, a multi-master-slave-based control of DGs is proposed in which slaves inject the available energy and compensate selectively unwanted current components of local loads with the secondary effect of having enhanced voltage waveforms while masters share the remaining load power autonomously with distant groups using frequency droop. The close proximity makes it practical for control signals to be communicated between inverters in one group with the potential to provide rapid load sharing response for mitigation of undesirable current components. Since each primary source has its own constraints, a supervisory control for each group is considered to determine convenient sharing factors as well as monitoring and gauging of electrical quantities of interest related to each of the inverters. The applied CPT theory makes possible to identify the load power terms related to non-active behavior.
and, based on some criteria, which could be the power rating of the converter or its current capability, choose the power components to be compensated. Due to complex values of the line impedance, which leads to coupling of active and reactive power droop controls, a compensation of resistive line impedance is implemented to make the line impedance appear to the converter as purely inductive impedance which enables decoupled control of those power terms.
CHAPTER 5 CASCADED MULTILEVEL CONVERTER FOR POWER QUALITY IMPROVEMENT IN SMARTGRID APPLICATIONS

Portion of this chapter is based on the journal paper titled “Grid-Connected Symmetrical Cascaded Multilevel Converter for Power Quality Improvement” published in IEEE Transactions on Industry Applications

A. Mortezaei²³, M. G. Simões⁴, T. D. C. Busarello⁵, F. P. Marafão⁶, and A. Al-Durra⁷

Multilevel inverters have experienced remarkable development in recent years and are considered the advanced technology for high-power and power-quality demanding energy conversion systems [67]. The aspect of the modular structure increases the reliability of the device, making it more attractive and competitive option for recent applications [67]. Therefore, multilevel converters have a great potential for future improvements on enhancing the energy efficiency and the system reliability. The most known and well established multilevel topologies include the neutral point clamped or diode clamped, flying capacitor or capacitor clamped, and the cascaded H-bridge [67]. Considering different topologies, the cascaded multilevel is attracting more and more attention because of its smaller number of components, straightforward physical layout, simpler modularity, and higher reliability, which makes this topology a potential candidate for renewable energy systems in low and medium power applications [68].

Given the current strength of multilevel converters and the claim for smart-grids realization, this chapter presents the study and development of the cascaded H-bridge multilevel inverter (CHMI) for applications in intelligent distribution systems. First, a control strategy for the application of shunt active power filter (SAPF) is developed in which the proposed control strategy regulates independent direct voltage links in each H-bridge cell and allows a selective and flexible compensation of disturbing currents under a variety of voltage conditions without requiring any reference frame transformation [69].

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Use of independent direct voltage links with reduced voltage values makes the CHMI topology an ideal candidate for medium and high power applications with increased reliability [70]. The experimental findings of this hardware setup validated the applicability and performance of the proposed control strategy, considering ideal and deteriorated voltage conditions.

5.1 Cascaded H-bridge Multilevel Converter Topology

The cascaded H-bridge multilevel converter is structured by a series of cascaded H-bridges, each fed by independent DC sources[68]. Each H-bridge as a power cell is capable of three different voltage levels at the output. The series connection of the H-bridges generates output voltage waveforms that are synthesized by the combination of each output of the H-bridges at certain switching states. The merit of this topology is that the modulation, control, and protection requirements of each bridge cell are modular. Figure 5-1 shows a single-phase topology of a CHMI with separate DC sources connected to the distribution network at the PCC.

Figure 5-1 CHMI Topology.
An output voltage waveform is obtained by adding the H-bridge cells output voltages as follows:

\[ v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,N}(t) = \sum_{k=1}^{N} v_{o,k}(t) \]  

(5.1)

where \( N \) is the number of H-bridge cells. If all DC-voltage sources in Figure 5-1 are equal to \( V_{dc} \), the inverter would be then known as symmetric CHMI. The number of output levels (\( N_L \)) in a symmetric CHMI multilevel inverter is related to the number of H-bridges (\( N \)) by the following equation:

\[ N_L = 1 + 2N \]  

(5.2)

The maximum output voltage \( V_{o,MAX} \) is then obtained as:

\[ V_{o,MAX} = NV_{dc} \]  

(5.3)

To increase the number of output levels generated by the inverter with the same number of H-bridge cells, asymmetric CHMI can be used. In [71], [72], the magnitudes of the DC voltage sources have been usually chosen according to a geometric progression with a factor of two or three, which are called binary and trinary multilevel inverters, respectively. The number of output voltage levels for binary and trinary asymmetric CHMI is as follows, respectively:

\[ N_L = 2^{N+1} - 1 \text{ if } V_{dc,k} = 2^{k-1}V_{dc}; \ k = 1,2, \ldots, N \]  

(5.4)

\[ N_L = 3^N \text{ if } V_{dc,k} = 3^{k-1}V_{dc}; \ k = 1,2, \ldots, N \]  

(5.5)

The maximum output voltage of an asymmetric CHMI including \( N \) H-bridge cells is as follows:

\[ V_{o,MAX} = \sum_{k=1}^{N} V_{dc,k} \]  

(5.6)

Equation (5.6) can be rewritten as (5.7) and (5.8) for binary and trinary DC sources asymmetric CHMI, respectively.

\[ V_{o,MAX} = (2^N - 1)V_{dc} \text{ if } V_{dc,k} = 2^{k-1}V_{dc}; k = 1,2, \ldots, N \]  

(5.7)
\[ V_{o,MAX} = \left( \frac{3^N - 1}{2} \right) V_{dc} \text{ if } V_{dc,k} = 3^{k-1}V_{dc}; k = 1,2,\ldots,N \] (5.8)

Therefore, using asymmetric CHMI, some switching-state redundancies are avoided, reducing the switching losses, and more output voltage levels and a higher maximum output voltage with the same number of H-bridge cells are generated.

Modulation strategies for CHMI are an extension of the traditional two-level switching schemes [73]. Various modulation strategies have been presented for CHMI to switch the transistors in each cell. By their switching frequency, they can be mainly classified either as fundamental or high switching frequencies. The first approach suggests lower switching losses, but the harmonics in the output voltage waveform appear at lower frequencies. Low-frequency strategies, such as Selective Harmonic Elimination (SHE) [74] and Space Vector Control (SVC) [75] are applied to high power and low dynamic systems. For the second approach, the harmonics are multiples of the switching frequency and their sidebands. Space Vector Modulation (SVM) [76] and Carrier-based PWM [77]–[79] are examples of high-frequency strategies. The Carrier-based modulation schemes can be divided into two categories: Phase-Shifted (PS-PWM) and Level-Shifted (LS-PWM) methods. In this chapter, Phase-Shifted PWM (PS-PWM) is used to switch the cascaded H-bridge cells.

5.2 SAPF CHMI Modulation and Control

The cascaded multilevel shunt converter is indicated in Figure 5-2, where it is also possible to see the network loads connected at the PCC. The PCC loads are constituted by both balanced and unbalanced linear and nonlinear devices. For SAPF and STATCOM applications, capacitors might be used at the CHMI DC-links, instead of DC sources, and a variety of strategies for controlling the CHMI DC-link voltage is reported in the literature [80]–[85]. This section proposes the control of a 7-level SAPF CHMI with individual H-bridge DC-link voltage regulation, applied for selective compensation or minimization of particular load disturbances, under a variety of voltage conditions. The presented control method is modular, and it can be adapted to any number of modules in series. The selective control strategies are based on the decompositions proposed in the CPT theory, which result in several current-related terms associated with specific load characteristics. These current components are independent of each other and may be used to define
different compensation strategies, which can be selective in minimizing particular effects of disturbing loads.

Figure 5-2 Block diagram of the power circuit, control scheme, and loads to the power grid.

Since each H-bridge cell is a three-level converter, the traditional unipolar PWM switching schemes are adopted. The series-connected H-bridge cells of the converter are modulated with individual carrier waveforms while sharing the same reference signals. A phase shift among the carrier waveforms is applied to adjacent H-bridge cells. The angle of the phase shift depends on the level of the converter and is tailored to the specific switching scheme, which is implemented in each H-bridge cell. Optimum harmonic cancellation can be achieved when the phase shift between the carriers is $180^\circ / N$, where $N$ is the number of series-connected H-bridge cells [86]. In this section, the CHMI is composed of three modules, synthesizing a 7-level output voltage waveform. The triangular carriers with a phase shift of $60^\circ$ are compared with two sinusoidal references for the presented 7-level CHMI is illustrated in Figure 5-3.

The implementation of a $60^\circ$ Phase shift among the three PWM triangular carriers inside the TMSF28335 DSP microcontroller for the 7-level CHMI is shown in Figure 5-4.
Figure 5-3 Reference and carrier signals for one phase of the 7-level CHMI.

Figure 5-4 DSP implementation of the PS-PWM for the 7-level CHMI.

Their implementations are listed as below:

1) Counter register on PWM 1, PWM 2, and PWM 3 modules (which are carriers) count from 0 to 6249. Note that period at each counter step for TMS320F28335 DSP board is 1/150Mhz, and the value 6249 is calculated as $6249 = \frac{150MHz}{24KHz} - 1$, where 24KHz is twice of the switching frequency (see Table 5-1).
2) Each PWM waveform has a 60° degree phase shift, which is achieved inside DSP by synchronization of PWM 1, PWM 2, and PWM 3 waveforms.

3) Each time PWM 1 counter counts to 0, event trigger introduced the synchronization process, which makes PWM 2 and PWM 3 counters load the saved numbers into their counters, at which time PWM 2 and PWM 3 counters will count from those saved numbers. Note that at the end of each cycle, PWM 1 block sends out a command to begin interrupt function. This action is independent of the synchronization process.

4) The saved numbers are calculated in (5.9) as:

\[
2083 = \frac{1}{3} \times 6249, \quad \text{and} \quad 4166 = \frac{2}{3} \times 6249
\]

(5.9)

5) At the beginning of each cycle (where the red arrow points showing the counter reaches zero, and interrupt function begins), the PWM 1 module will send out a signal to ADC block to let it read the feedback sampled results, then CPU compares the results with references and errors will be processed through control algorithm; the output of the control algorithm will be then sent out to the shadow mode of compare register of PWM 1, PWM 2 and PWM 3 modules (where the black arrow points showing all the calculation finished). At the beginning of next cycle (when PWM 1 module’s counter counts to zero again), the PWM 1 compare register will load the shadow mode value. The PWM 2 and PWM 3 modules will load from their shadow registers when their counters count to zero. (where blue and yellow line points, respectively).

5.2.1 Control Strategy

The proposed 7-level CHMI is controlled to regulate the DC-link voltages of each H-bridge cell, and to compensate current load terms related to disturbing effects. The voltage controller output, from H-bridge cells, is multiplied by the PCC voltage \((v_{pccabc})\), so as to define an additional current reference \((i_{pabc}^*)\) to be added to the reference of the disturbance currents \((i_{fabc}^*)\). The resulting current reference \((i_{abc}^*)\) is directed to the current controller output of the active filter. Thus, the active filter must act as a high power factor controlled rectifier during transient load conditions and as a current compensator under steady state conditions. Notice that there is no need for any type of coordinate transformation or synchronization algorithm to provide the reference signals. Assuming one phase \((a)\) of the CHMI, the control strategy for DC voltage controllers of each H-bridge cell is illustrated in the diagram of Figure 5-5, which is comprised of inner and outer
control loops. The inner loop regulates the inverter output current at the desired reference \( i_{a}^{*} \), and the outer loop regulates the DC-link voltages in each H-bridge cell. The desired inverter current is the sum of the DC link voltage regulation currents \( i_{pa}^{*} \) and the compensation references from the CPT decomposition \( i_{fa}^{*} \).

![Figure 5-5 Block diagram of the proposed control scheme with DC voltage controllers of H-bridge cells in phase a.](image)

The currently proposed controller is designed in the \( abc \) frame based on frequency response requirements. Consider the CHMI of Figure 5-2, the parameters of the converter are provided in Table 5-1. The PCC voltages \( v_{pccabc} \) are dictated by the grid.

<table>
<thead>
<tr>
<th>Table 5-1 CHMI parameters.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Phase peak voltage</td>
</tr>
<tr>
<td>Grid frequency</td>
</tr>
<tr>
<td>Maximum output capacity</td>
</tr>
<tr>
<td>Output filter inductor</td>
</tr>
<tr>
<td>Output filter resistor</td>
</tr>
<tr>
<td>DC link voltages</td>
</tr>
<tr>
<td>DC link capacitor</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
<tr>
<td>Sampling Period</td>
</tr>
</tbody>
</table>
5.2.1.1 Current Controller Derivation

The dynamics of the AC-side current $i_a$ is described by (5.10). It represents a system in which $i_a$ is the state variable, $v_{o,ak}$ are the control inputs, and $v_{pcca}$ is the disturbance input.

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = \sum_{k=1}^{N} v_{o,ak}(t) - v_{pcca}(t) \tag{5.10}$$

The H-bridge converter terminal voltages can be written as:

$$\begin{bmatrix} v_{o,a1}(t) \\ v_{o,a2}(t) \\ \vdots \\ v_{o,aN}(t) \end{bmatrix} = \begin{bmatrix} m_{o,a1}(t)V_{dc} \\ m_{o,a2}(t)V_{dc} \\ \vdots \\ m_{o,aN}(t)V_{dc} \end{bmatrix} \tag{5.11}$$

where $m_{o,a1}(t), m_{o,a2}(t), ..., m_{o,aN}(t)$ denote the modulation signals for each H-bridge converter. Their signals are continuous and their values are in the range [-1 1]. In order to facilitate the controller design and to reduce the model expressions, it is convenient to transform (5.11) by the definition given in (5.12) [81].

$$m_{o,a}(t) = m_{o,a1}(t) = m_{o,a2}(t) = \cdots = m_{o,aN}(t) \tag{5.12}$$

Therefore, (5.10) can be rewritten as (5.13).

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = NV_{dc} m_{o,a}(t) - v_{pcca}(t) \tag{5.13}$$

Assuming the CHMI of Figure 5.2:

$$v_{o,a}(t) = G_{inv} m_{o,a}(t) = NV_{dc} m_{o,a}(t) \tag{5.14}$$

Therefore, the dynamics of the AC-side current $i_a$ is determined as (5-15). Based on (5.14), the control input $v_{o,a}$, can be controlled by the modulating signal $m_{o,a}$.

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = v_{o,a}(t) - v_{pcca}(t) \tag{5.15}$$

The last term in (5.15), $v_{pcca}(t)$, will be compensated by the feedforward action to mitigate the dynamic couplings between the CHMI and the AC system. By applying the perturbation and linearization technique and taking the Laplace transformation, the CHMI output filter transfer function is determined by (5.16).
\[ G_t(s) = \frac{i_a(s)}{v_{o,a}(s)} = \frac{1}{L_f s + R_f} \] (5.16)

For the implementation of the control system inside DSP, the system transfer function of (5.16) is first digitized. To allow the use of the frequency response design method, the conversion of \( G_i(z) \) transfer function from “z” plane to fictitious “w” plane is performed using the bilinear transform:

\[
G_i(w) = Z \left\{ 1 - \frac{e^{-sT_s}}{s} \cdot G_i(s) \right\}_{z \rightarrow \frac{1 + \frac{T_s}{w}}{1 - \frac{T_s}{w}}} = \frac{-0.02083w + 500}{w + 50} \] (5.17)

To perform the controller design, the open-loop current control transfer function \( G_{oi}(w) \) is obtained as expressed in (5.18). \( C_i(w) \), the controller of the current control loop, consists of a lag compensator as (5.19), where the parameters of \( \omega_z \), \( \omega_p \) and \( k_c \) are the zero, pole and the gain of the compensator, respectively.

\[
G_{oi}(w) = C_i(w)G_i(w) \] (5.18)

\[
C_i(w) = \frac{k_c \left( 1 + \frac{s}{\omega_z} \right)}{\left( 1 + \frac{s}{\omega_p} \right)} \] (5.19)

Table 5-2 presents the requirements chosen for control scheme of the CHMI output current and the parameters of (5.19) in a digitized system [45].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Phase Margin</td>
<td>( \varphi_{PMi} = 72^\circ )</td>
</tr>
<tr>
<td>Desired cut-off frequency</td>
<td>( f_{ci} = 1.2 ) kHz</td>
</tr>
<tr>
<td>Zero frequency of the lag compensator</td>
<td>( f_z = f_{ci}/10 = 120 ) Hz</td>
</tr>
<tr>
<td>Pole frequency of the lag compensator</td>
<td>( f_p = 100.1 ) Hz</td>
</tr>
<tr>
<td>Gain of the lag compensator</td>
<td>( k_c = 17.22 )</td>
</tr>
</tbody>
</table>
The frequency response in “w” domain of the open loop transfer function is illustrated in Figure 5-6. As shown, at the crossover frequency, the open loop gain of 0 dB and the phase margin of 72° are obtained.

The digital implementation of the lag controller (5.19) in the “z” domain is obtained by transformed back to “z” using the bilinear transform plane with a sampling time of $T_s$ that is also the switching period.

$$C_i(z) = C_i(w)\big|_{w=\frac{2}{T_s}} = \frac{14.43 - 13.55z^{-1}}{1 - 0.948z^{-1}}$$  \hfill (5.20)

![Bode plot of the open-loop current transfer function.](image)

Figure 5-6 Bode plot of the open-loop current transfer function.

5.2.1.2 DC-Link Controller Derivation

The dimensioning of the DC-link voltage controller is based on the transfer function between the defined current reference value and the DC-link voltage in each H-bridge cell [87]. Thus, considering phase $a$, from the power balance of the inverter in this phase one may have:

$$P_{cap} + P_{ac} = 0$$  \hfill (5.21)

$$3V_{dc}I_{cap} + \frac{V_aI_a}{2} = 0$$  \hfill (5.22)
where factor 3 represents the number of H-bridge cells in phase $a$, $V_{dc}$ is the regulated DC-link voltage for each H-bridge cell, $I_{cap}$ is the respective capacitor current, $V_a$ and $I_a$ represent the peak value of the AC-side voltage and current of phase $a$ respectively, and factor $1/2$ comes from the average ac power flow using peak values.

From (5.22) the current through each H-bridge cell capacitor is:

$$I_{cap} = -\frac{V_a I_a}{6V_{dc}} \quad (5.23)$$

And the same current regarding voltage across the capacitor is given by:

$$C_{dc} \frac{dV_{dc}}{dt} = I_{cap} \quad (5.24)$$

From (5.23) and (5.24) the differential equation for the DC voltage becomes:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} \left( -\frac{V_a I_a}{6V_{dc}} \right) \quad (5.25)$$

Based on (5.25), the DC-link voltage for one H-bridge cell is regulated by controlling the inverter current reference ($i_a^*$). The selected bandwidth of the DC voltage loop is reduced to avoid interaction with the current controller. This means the individual capacitor voltage controllers are decoupled from the current controller as their dynamics are slowed down. Therefore, the closed current loop can be assumed ideal for designing purposes and replaced by unity. The transfer functions of the DC voltage control scheme, $G_{vdc}(s)$, is presented in (5.26). The DC-link voltage controller $C_{vdc}(s)$ is multiplied by $-1$ to compensate for the negative sign of DC bus voltage dynamics.

$$G_{vdc}(s) = \frac{V_a^2}{6V_{dc} C_{dc} s} \quad (5.26)$$

For the implementation of the control system inside DSP, the system transfer function of (5.26) is first digitized. To allow the use of frequency response method design, the conversion of $G_{vdc}(z)$ transfer function from "$z$" plane to "$w$" plane is performed using the bilinear transform:

$$G_{vdc}(w) = Z \left\{ \left( \frac{1 - e^{-s T_S}}{s} \right) \cdot G_{vdc}(z) \right\}_{z = \frac{1 + \frac{T_S}{w}}{1 - \frac{T_S}{w}}} = -0.6429w + 15430 \quad (5.27)$$
The open-loop transfer functions of the DC voltage control loop, \( G_{ovdc}(w) \), is presented in (5.28). A Proportional Integral (PI) compensator is intended for \( C_{vdc}(w) \) as in (5.29) for DC-link voltage regulation, where the parameters of \( k_p \) and \( T \) are the proportional gain and time constant of the compensator, respectively.

\[
G_{ovdc}(w) = C_{vdc}(w)G_{vdc}(w) \quad (5.28)
\]

\[
C_{vdc}(w) = k_p \left( \frac{wT + 1}{wT} \right) \quad (5.29)
\]

Table 5-3 presents the requirements chosen for control scheme of the DC voltage loop and the parameters of (5.29) in a digitized system. The DC-side capacitor voltages are sensed and compared to a set of voltage references.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Phase Margin</td>
<td>( \varphi_{PMvdc} = 60^\circ )</td>
</tr>
<tr>
<td>Desired cut-off frequency</td>
<td>( f_{cvdc} = 10 \text{ Hz} )</td>
</tr>
<tr>
<td>Proportional gain of PI controller</td>
<td>( k_p = 0.0035 )</td>
</tr>
<tr>
<td>Time constant of PI controller</td>
<td>( T = 0.027 \text{ s} )</td>
</tr>
</tbody>
</table>

The frequency response in “\( w \)” domain of the open loop transfer function is illustrated in Figure 5-7. As shown, at the crossover frequency, the open loop gain of 0 dB and the phase margin of 60° are obtained.

The digital implementation of the PI controller (5.29) in the “\( z \)” domain is obtained by transformed back to “\( z \)” using the bilinear transform plane.

\[
C_{vdc}(z) = G_{vdc}(z) \bigg|_{z = \frac{1 + \frac{T}{2w}}{1 - \frac{T}{2w}}} = \frac{0.0035 - 0.0035z^{-1}}{1 - z^{-1}} \quad (5.30)
\]
5.2.2 Analysis of Different Compensation Strategies by Means of Experimental Results

To evaluate the performance of selective compensation strategies by using the cascaded multilevel shunt converter, the three-phase system of Figure 5-2 is experimentally verified under different voltage conditions using a real-time HIL system. The power plant was built inside Matlab\Simulink. Then, the system was compiled inside the real-time simulator “Opal-RT.” The control algorithm was implemented in a TMSF28335 DSP microcontroller with the switching and sampling frequencies set at 12 kHz. The load parameters are listed in Table 5-4.

Table 5-4 Load parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid inductor</td>
<td>$L_g = 1\text{mH}$</td>
</tr>
<tr>
<td>Grid resistor</td>
<td>$R_g = 0.1\ \Omega$</td>
</tr>
<tr>
<td>Load inductor</td>
<td>$L_1 = 58\ \text{mH},\ L_2 = 4\ \text{mH}$</td>
</tr>
<tr>
<td>Load capacitor</td>
<td>$C_1 = 220\ \mu\text{F}$</td>
</tr>
<tr>
<td>Load filter resistor</td>
<td>$R_{DC} = 120\ \Omega$</td>
</tr>
<tr>
<td></td>
<td>$R_1 = 5\ \Omega,\ R_2 = 110\ \Omega,\ R_3 = 30\ \Omega,$</td>
</tr>
<tr>
<td></td>
<td>$R_4 = 35\ \Omega,\ R_5 = 40\ \Omega,\ R_6 = 50\ \Omega,$</td>
</tr>
<tr>
<td></td>
<td>$R_7 = 25\ \Omega$</td>
</tr>
</tbody>
</table>
The nonlinear loads were composed of three- and single-phase full bridge rectifiers feeding capacitive and resistive loads. The results were captured using a HAMEG HMO724 four channel oscilloscope.

Figure 5-8 presents the PCC voltage and grid current waveforms measured at the PCC, before implementing any compensation strategy, and the grid supplies the entire load current. Notice that the currents are unbalanced and significantly distorted. Next sections present and discuss three possible scenarios (1, 2, and 3).

![Figure 5-8 Before implementing any compensation strategy: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b.](image)

5.2.2.1 Symmetrical and Sinusoidal Voltage Source with $v_a = 127\angle 0^\circ$, $v_b = 127\angle -120^\circ$ and $v_c = 127\angle 120^\circ$

Figure 5-9 to Figure 5-11 present the waveforms of voltages and currents measured at the PCC of Figure 5-2, under symmetrical and sinusoidal voltage conditions. In the next sub-sections, the CHMI starts operating as active filter showing the waveforms and their quantitative values for some of the more elucidative compensation strategies. Note that the current circulating in the CHMI differs in each strategy.
5.2.2.1.1 Reactive Current Compensation

In this case, the aim is to attenuate the reactive power. Thus, the current references for the shunt active power filter should be \(i_r^b\), added the charging current of the H-bridge DC-side capacitors \(i_{pabc}^r\). From the CHMI terminal voltages and currents shown in Figure 5-9(a), the inverter is supplying reactive power or the reactive current component of the load since the CHMI currents are orthogonal to the terminal voltages. In other words, when the terminal voltages reach zero, the corresponding phase inverter currents reach their peak value. The resulting compensated PCC voltage and grid current waveforms are shown in Figure 5-9(b). Notice that the compensated grid currents are unbalanced, distorted, and slightly out of phase with the voltages. The unbalance and nonlinearity can be explained due to the fact that the current reference sent to the active filter \(i_r^b\) is not related to these disturbances. There could be a minor remaining lag in the compensation because of the components of unbalanced reactive currents, which were not compensated, since reactive power is determined only by balanced reactive currents. If the total reactive currents \(i_r = i_r^b + i_r^u\) were applied as current references for the active filter, both the lag and the unbalance phenomena would be compensated.

(a) (b)

Figure 5-9 Compensation of balanced reactive current component: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b, (b) Compensation of balanced reactive current component: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b.
5.2.2.1.2 Unbalanced Current Compensation

The load considered in the system imposes unbalance component to the grid’s current. Therefore, the CPT theory is used to extract the unbalance current/power component of the load. In this case, the goal is to compensate only the components of unbalanced current, \( (i^u) \). The CHMI terminal voltages and currents are shown in Figure 5-10(a). Notice that the resulting compensated currents shown in Figure 5-10(b) remain non-sinusoidal and out of phase with the voltages, i.e., distorted and lagging behind the PCC voltages, but are practically balanced (same amplitude in all the phases).

![Figure 5-10](image)

Figure 5-10 (a) Compensation of unbalance current component: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b, (b) Compensation of unbalance current component: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b

5.2.2.1.3 Harmonic Current Compensation

At this case study, the CHMI in Figure 5-11 starts compensating only the void currents \( (i_v) \). From Figure 5-11(a), the inverter currents are nonlinear whereas the compensated currents in Figure 5-11(b) are quasi-sinusoidal, unbalanced, and not in phase with their corresponding voltages indicating the balanced active, balanced reactive, and unbalance current components of the load is supplied by the grid.
Figure 5-11 (a) Compensation of void current component: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b, (f) Compensation of void current component: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b.

To simplify the quantitative analysis of the compensation strategies, Table 5-5 illustrates the values of the grid power portions from the CPT decomposition, the collective RMS values of the grid currents and shunt active power filter and the power factor of the three-phase system.

Table 5-5 PCC Power Components, Inverter and Grid Currents, and Power Factor under possible selective compensation strategies.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Without Com.</th>
<th>Com. $i_v$</th>
<th>Com. $i^b$</th>
<th>Com. $i^u$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$(VA)</td>
<td>7302</td>
<td>7263</td>
<td>7144</td>
<td>7247</td>
</tr>
<tr>
<td>$P$(W)</td>
<td>6676</td>
<td>6700</td>
<td>7011</td>
<td>6683</td>
</tr>
<tr>
<td>$Q$(VA)</td>
<td>2654</td>
<td>2623</td>
<td>14</td>
<td>2649</td>
</tr>
<tr>
<td>$N$(VA)</td>
<td>931</td>
<td>937</td>
<td>977</td>
<td>5</td>
</tr>
<tr>
<td>$D$(VA)</td>
<td>916</td>
<td>185</td>
<td>962</td>
<td>914</td>
</tr>
<tr>
<td>$I_{grid}$(A)</td>
<td>36.6</td>
<td>36.4</td>
<td>34.9</td>
<td>36.3</td>
</tr>
<tr>
<td>$I_{inv}$(A)</td>
<td>0.0</td>
<td>5</td>
<td>13.7</td>
<td>4.7</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.914</td>
<td>0.922</td>
<td>0.981</td>
<td>0.922</td>
</tr>
</tbody>
</table>

Notice that the currents circulating through the CHMI are different in each strategy, with the highest current for ($i^b$) compensation and the lowest for ($i^u$) compensation. As a result, if only
current nonlinearities or current unbalances must be compensated, the installed filter (converter) can have almost threefold lower power (in this particular case) than if it was designed to compensate balanced reactive current, which would directly affect the financial cost of an active filter. It is important to indicate that for each case of compensation, only the portion of power selected for compensation underwent significant changes in value, which establishes the selectivity and decoupling of the current components due to the orthogonality of the CPT decompositions.

From Table 5-5, it seems that the compensation of \((i_v)\) still leaves some deviation in the value of the \(D\) component. The explanation for this behavior is because the load used for verification of our system is highly distorted. The harmonic current has sharp peaks of 8A shown in Figure 5-11(a) leaves some distortion on the PCC voltages after compensation in Figure 5-11(b). Therefore, this deviation is mainly due to the limits imposed by the current controllers, not the CPT decomposition.

5.2.2.1.4 Non-active Current Compensation

In Figure 5-12, the CHMI is set to compensate non-active current components of the load current. This current component is associated with all the disturbances created by the load (reactive currents, asymmetries, imbalances, and nonlinearities), and is formed by \((i^b_r + i^u + i_v)\). Figure 5-12(a) depicts the PCC voltages and the resulting compensated grid current waveforms under symmetrical and sinusoidal voltage condition. The source currents in this compensation strategy are the load balanced active current components \((i^b_a)\) which are practically sinusoidal, balanced, and in phase with the voltages, describing the proper condition for an electric system. In Figure 5-12(b), the CHMI terminal voltages \((v_{o,abc})\) are presented. The scaling for terminal voltages is 110V per division. The CHMI terminal synthesizes a 7-level output voltage with symmetrical modules. Figure 5-12(c) presents the H-bridge DC-link voltages of phase \(a\) (channels 1, 2 and 3) and the DC-link current of H-bridge \(a1\) (channel 4). The three module DC-link voltages are controlled at the reference value while the CHMI contains non-active current component under symmetrical and sinusoidal voltage condition. The DC-link voltages have higher ripples as the CHMI supplies unbalance power component of load. The DC-link current of H-bridge \(a1\) in Figure 5-12(c) has pulsating shape showing its DC-link capacitor, \(C_{dc}\), is charging and discharging in order to regulate its corresponding DC bus voltage at 70 V.
Figure 5-12 Compensation of non-active current component under symmetrical and sinusoidal voltage source: (a) PCC voltage (90 V/div) and grid current (40 A/div). (b) CHMI terminal voltages (110 V/div). (c) H-bridge DC-link regulated voltages (25 V/div) of phase a and DC-link current (12 A/div) of H-bridge a1.
Table 5-6 illustrates the values obtained through the compensation of non-active current, in which all the electrical disturbances are compensated (nonlinearities, unbalances, and reactive power). As it is shown, the current of the compensated system shows a lower value than that of the system without compensation, as the undesirable components of currents have been attenuated. Notice that the current that flows through the active filter may be up to three times higher than that of the compensation strategy for void or nonlinear current. This information is important from a financial perspective.

Table 5-6 PCC Power Components, Inverter and Grid Currents and Power Factor through the non-active compensation - Case 1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without Compensation</th>
<th>With Compensation of $i_{na}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$ (VA)</td>
<td>7302</td>
<td>7052</td>
</tr>
<tr>
<td>$P$ (W)</td>
<td>6676</td>
<td>7044</td>
</tr>
<tr>
<td>$Q$ (VA)</td>
<td>2654</td>
<td>12</td>
</tr>
<tr>
<td>$N$ (VA)</td>
<td>931</td>
<td>11</td>
</tr>
<tr>
<td>$D$ (VA)</td>
<td>916</td>
<td>188</td>
</tr>
<tr>
<td>$I_{grid}$ (A)</td>
<td>36.6</td>
<td>34.5</td>
</tr>
<tr>
<td>$I_{inv}$ (A)</td>
<td>0.0</td>
<td>15.2</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.914</td>
<td>0.999</td>
</tr>
</tbody>
</table>

5.2.2.2 Asymmetrical and Sinusoidal Voltage Source with $v_a = 106\angle 0^\circ$, $v_b = 127\angle -120^\circ$ and $v_c = 116\angle 120^\circ$

To evaluate the proposed compensation strategies for a case in which the source voltages have not been idealized, an asymmetrical and sinusoidal voltage source is considered. The CHMI operates as an active filter using the CPT theory, supplying all the undesirable components of the load (balanced reactive, unbalanced and harmonics), that is $(i_r^b + i_u + i_v)$. Figure 5-13(a) illustrates the voltages and currents at the PCC, after the compensation of non-active currents, while the grid supplies the balanced active current components of the load $(i_a^b)$. The compensated currents are sinusoidal, unbalanced due to the asymmetrical voltage source, and in phase with their corresponding voltages, as in the case of a balanced resistive load.
Figure 5-13 Compensation of non-active current component under asymmetrical and sinusoidal voltage source: (a) PCC voltage (90 V/div) and grid current (40 A/div), (b) CHMI terminal voltages (110 V/div), (c) H-bridge DC-link regulated voltages (25 V/div) of phase a and DC-link current (12 A/div) of H-bridge a1.
It is because the CPT theory decouples the load and supply responsibility and quantifies the number of resistive characteristics of the load under various supply voltage conditions [5]. Figure 5-13(b) depicts the CHMI terminal voltages. It is shown the modulation of upper levels in phase $c$ (channel 3) is lower than phase $b$ (channel 2) and is higher than phase $a$ (channel 1) proportional to the amplitudes of their corresponding phase voltages. In Figure 5-13(c), the H-bridge DC-link voltages of phase $a$ and the DC-link current of H-bridge $a1$ is depicted under asymmetrical and sinusoidal voltage condition.

From Table 5-7, one can see that all the load disturbances were compensated. Notice that the slight deviations in the values of the powers are due to the limits imposed by the controllers used here.

Table 5-7 PCC Power Components, Inverter and Grid Currents and Power Factor through the non-active compensation - Case 2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without Compensation</th>
<th>With Compensation of $i_{na}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A(VA)</td>
<td>6005</td>
<td>5811</td>
</tr>
<tr>
<td>P(W)</td>
<td>5490</td>
<td>5808</td>
</tr>
<tr>
<td>Q(VA)</td>
<td>2169</td>
<td>11</td>
</tr>
<tr>
<td>N(VA)</td>
<td>782</td>
<td>12</td>
</tr>
<tr>
<td>D(VA)</td>
<td>763</td>
<td>157</td>
</tr>
<tr>
<td>$i_{grid}$ (A)</td>
<td>32.9</td>
<td>31.1</td>
</tr>
<tr>
<td>$i_{inv}$ (A)</td>
<td>0.0</td>
<td>13.7</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.914</td>
<td>1</td>
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</tbody>
</table>

5.2.2.1 Symmetrical and Non-sinusoidal Voltage Source with 5% of 5th and 7th Harmonics

The evaluation of the proposed compensation strategies for symmetrical and non-sinusoidal voltages is considered in Figure 5-14, where the CHMI is set to compensate non-active or undesirable components of the load (balanced reactive, unbalanced and harmonics) that is ($i^b_r + i^u + i_v$). Having the CPT supply the non-active currents of the load, the deterioration of the supplied current by the grid is only due to the imposed voltage distortion, because the generated current emulates a balanced resistive load.
Figure 5-14 Compensation of non-active current component under symmetrical and non-sinusoidal voltage source: (a) PCC voltage (90 V/div) and grid current (40 A/div), (b) CHMI terminal voltages (110 V/div), (c) H-bridge DC-link regulated voltages (25 V/div) of phase a and DC-link current (12 A/div) of H-bridge a1.
Figure 5-14(a) illustrates the voltages and currents at the PCC after the compensation of non-active currents. The source current contains the balanced active current component of the load. Figure 5-14(b) depicts the CHMI terminal voltages ($v_{o,abc}$). The scaling for terminal voltages is 110V per division. Figure 5-14(c) depicts the H-bridge DC-link voltages of phase $a$ and the DC-link current of H-bridge $a1$ under symmetrical and non-sinusoidal voltage condition.

The results illustrated in Table 5-8 establish the effectiveness of the compensation of non-active current under extreme voltage condition. It is demonstrated that the portion of the entire disturbance undergoes a significant change in its value when compared with the values of uncompensated loads.

<table>
<thead>
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<th>Parameters</th>
<th>Without Compensation</th>
<th>With Compensation of $i_{na}$</th>
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<td>A (VA)</td>
<td>7313</td>
<td>7015</td>
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<td>P (W)</td>
<td>6631</td>
<td>7008</td>
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<tr>
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<td>2764</td>
<td>12</td>
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<tr>
<td>N (VA)</td>
<td>922</td>
<td>7</td>
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<td>D (VA)</td>
<td>1004</td>
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<td>34.2</td>
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<td>$I_{inv}$ (A)</td>
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<td>15.8</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.907</td>
<td>0.999</td>
</tr>
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</table>

5.3 Discussions

Multilevel inverters have several merits over conventional inverters include low THD, low switching losses, good power quality, reduced Electromagnetic Interference (EMI), modularity and low switch voltage stress of electronic components. Among different topologies of multilevel converters, a CHMI is one of the most popular. It is composed of multiple H-bridge power cells. In practice, the number of power cells in a CHMI is mainly determined by its operating voltage and manufacturing cost. The series connection of the H-bridge cells generates output voltage waveforms that are synthesized by the combination of each output of the H-bridges at certain
switching states. In this chapter a symmetrical CHMI is developed for SAPF for flexible power conditioning in smart-grid applications. The main feature of the proposed scheme is the use of independent DC-links, with reduced voltages, which makes such a topology an ideal candidate for medium and high power applications with increased reliability. The developed control strategy regulates independent DC-link voltages in each H-bridge cell and allows selective and flexible compensation of disturbing currents under a variety of voltage conditions without requiring any reference frame transformation. Experimental results are provided to validate the possibilities and performance of the proposed control strategies, considering ideal and deteriorated voltage conditions.
6.1 Conclusions

This dissertation proposes DG interfacing systems with multifunctional capabilities to improve power quality by injection of different current components during integration of DG resources. In this dissertation, we worked on several research projects, some of them are concluded as follow:

Our studies on power theories in chapter two is important for the power measurement techniques, revenue metering, instrumentation technology and also flexible power conditioning strategies. We investigated important time domain power theories for current decompositions and related definitions from the performance perspective in flexible power conditioner in three-phase three-wire and three-phase four-wire systems. This could be particularly important for defining technical responsibilities in smart microgrids or modern power grids. For instance, we noticed that CPT theory separates linear and non-linear portions of single-phase loads as its decomposition is based on load characteristics, while PQ couldn’t decompose linear and non-linear components of single-phase loads. As a second example, we noticed that CPT theory separates disturbances imposed by the load from irregularities caused by the supply. This is important in terms of the appropriation of responsibilities in case of smart microgrids or power grids. PQ theory does not allow the separation of load and supply responsibilities. As a third example, we noticed that under asymmetrical and sinusoidal voltages, PQ theory with constant power strategy may not be a good solution as it may generate other harmonics in the system, while CPT theory leads to exchange of sinusoidal active current waveforms with the grid. As a fourth example, we noticed that under non-sinusoidal voltages, CPT theory is able to provide unity power factor in the presence of distorted voltages. Therefore, a comprehensive study of advanced power theories is an important issue and may be very attractive for designing power conditioners or any other grid-tied switching power interface for modern grids. This helps the designer choose the appropriate control technique or the disturbances needed to be compensated, especially when the inverter has limited capacity. The effectiveness of control strategies are experimentally verified with the control algorithm implemented in the TMSF28335 DSP microcontroller.

Our research on the renewables to carry out the power quality ancillary services in the distribution system in chapter three plays a very important role in the modernization of electric
power systems. It makes the renewable energy sources connected through switching power interfaces to the utility grid experience an evolution in terms of the number of functionalities. The interfacing converters now can be used as multi-functional compensators with the capability of enhancing power quality, rather than being limited to active power generation. It also provides technical solutions for the distribution system operator to efficiently manage the grid resources in the case of highly integrated distributed energy resources (DERs).

Our research in chapter four proposes a platform that enables the coordinated operation of multifunctional distributed generators, aiming at making proper use of DG inverter units’ capability to improve power quality indices at microgrid load buses. In this platform, we investigated the coordinated control of parallel interfacing DG systems to enhance the operation of microgrid systems. Two important issues that we addressed are the power quality and undesirable current sharing, particularly in the low-voltage distribution network, where electronic devices are drawing distorted and unbalanced currents. The interactions of such current disturbances with high feeder/line impedances, in a low voltage system cause considerable voltage deterioration and possibly affect sensitive loads. We proposed a hybrid cooperative method which is a combination of both communication-based and non-communication-based schemes. In our proposal, communication links should be always an enhanced technical solution, therefore, DGs located in close proximity could have access to high-bandwidth communication links to provide rapid load sharing response for ancillary functions including voltage support, harmonic mitigation, and unbalance compensation; however, the impracticality of communication between DGs at remote nodes is recognized and the sharing between these groups is accomplished through the voltage and frequency droop methods. Therefore, with our technique, the disadvantages of communication-based and non-communication-based schemes are overcome partially.

Our research in chapter five is useful for companies that work in the area of integrating renewable energy and storage resources to power grids in medium and low voltage systems. This research investigates the study and implementation of the cascaded multilevel converters, detailing the main concepts about the structure, the modulation, and the control schemes. This project proposes the CHMI topology to integrate energy sources and battery storages. Moreover, new functions can be embedded without the necessity of changing the physical structure. This increases the options of management of the system operator. For example, in one proposal, we use a symmetrical CHMI for SAPF for flexible power conditioning in smart-grid applications. The main
feature of the proposed scheme is the use of independent DC links, with reduced voltages, which makes such a topology an ideal candidate for medium and high power applications with increased reliability. In another proposal, we present a three-phase BSS for distribution grid applications. The proposed BSS is an attractive solution for applications in medium-voltage grids, contributing to the reliability and to the uninterrupted supply of the distribution system. Experimental results for hardware setup implementation were provided to validate the possibilities and performance of the proposed control strategies.

6.2 Future Work

The aim of my research is to facilitate utilization of clean, renewable energy resources (wind, and solar) that would significantly benefit the nations regarding reducing greenhouse gas emissions and mitigating global warming. In my future work, I intend to extend my prior experiments on intelligent distributed energy systems aiming to the autonomous and intelligent operation of distributed generation systems, as well as other grid-tied power electronic converters, such as electronic power compensators. The main focus is directed to the micro grids, configuring the so-called smart micro grids scenario.

6.2.1 Development of Cooperative Control Strategies for Maintenance of Power Quality Indexes in Microgrids with Multiple Bus Considerations

In the literature, several approaches based on hierarchical or decentralized methodologies have been proposed to cooperatively coordinate multifunctional inverters dispersed over microgrids, focusing mainly on the power flow control at a PCC or in a specific bus. As a consequence, there remains a gap regarding alternatives that are able to coordinate inverters under a multiobjective context in microgrids, providing sharing of active, reactive and harmonic electrical quantities, not only striving for a specific goal at the PCC or in a sensitive load bus, but also complying with power quality indexes in non-sensitive buses. Therefore, we intend to study a methodology able to cooperatively control inverters looking at multiple bus operation goals within a microgrid, under islanded or grid-connected conditions, with single- or three-phase topology, and considering distorted and asymmetrical voltage scenarios.
6.2.2 Development of Bidirectional Electric Vehicle (EV) Charging System for Smart Grid Applications

The aim of this work is to provide a bidirectional power exchange and isolation with compact transformer design between the battery and the AC system using Dual active bridge and CLLC resonant tank DC–DC converters for off-board and on-board EV charging systems, respectively. Bidirectional charging enables the vehicle-to-grid (V2G) capability, allowing EVs to inject energy into the grid. It can also contribute in stabilizing unbalanced situations during peak hours or even provide electric energy for emergency backup during a power outage. Hence, the bidirectional power flow capability of EVs connected to electric power grid considers as one key opportunity that electro mobility is offering toward more efficient distribution network. In addition to normal and rapid charging, and grid support including V2G mode, we intent to develop ancillary functionalities such as active filtering for EV charging system to minimize particular load disturbances at the PCC. Such flexibility is particularly important in the presence of reactive, unbalanced, and nonlinear loads and in conditions where the grid might be weak.

6.2.3 Study of Energy Management System for Smart Microgrids

This research project proposes the discussion and study of an energy management system (EMS) for microgrids, aiming to optimize generation and consumption of energy in local and/or distributed level. The microgrid may be composed of several generation units, e. g., Photovoltaic and/or wind turbines, and those technologies have power converter interfaces, which is responsible for the control of power flow between the microgrid and the main grid. The main goal is to evaluate the applicability of primary and secondary control techniques based on objective functions such as power loss minimization, generation cost minimization, reliability, etc. Thus, expressions for various objective functions should be developed for a coordination framework. Thus, we intend to study the EMS as an intelligent platform that will integrate various control algorithms running in each component of the microgrid, allowing the smart operation of the energy suppliers in the microgrid.
REFERENCES CITED


[67] S. Kouro et al., “Recent advances and industrial applications of multilevel converters,”


[81] A. A. Valdez-Fernández, P. R. Martínez-Rodríguez, G. Escobar, C. A. Limones-Pozos,


