DETERMINATION OF PRISTINE MARGIN IN F-RAM USING THE

SECTIONAL SHMOO

by

JUSTIN LYNN BEAVERS

B.S., University of Colorado, Colorado Springs, 2015

A thesis submitted to the Graduate Faculty of the

University of Colorado Colorado Springs

In partial fulfillment of the

requirements for the degree of

Master of Science

Department of Electrical and Computer Engineering

2018
This thesis for the Master of Science degree by

Justin Lynn Beavers

Has been approved for the

Department of Electrical and Computer Engineering

by

T.S. Kalkur, Chair

John Lindsey

Darshika Perera

DATE: 11/15/2018
ABSTRACT

As demand for consumer electronics continues to grow, device manufacturers are pushing semiconductor companies to develop and innovate memories to have higher reliability, faster read/write performance, lower power and smaller die/package footprints than the current top performing memory technologies. The present leading memories in the industry (Flash, EEPROM, battery backed SRAMs, DRAMs) check many of the boxes, but no single options cover all of these requirements. F-RAM meets or exceeds many of the growing demands from device manufacturers. Where F-RAM fails to meet industry, requirements are storage density per unit area, and performance across extreme temperature ranges. Most F-RAM devices on the market today are configured in the 2T2C cell structure. The 2T2C cell structure has great performance across temperature ranges of -55C to 125C, however it requires twice the die area as the 1T1C cell structure. Switching to the 1T1C cell structure doubles the storage density for a given die area, however it shows a lower tolerance to temperature related effects with current market products operating from -45C to 85C. Due to the destructive read behavior of F-RAM memories these temperature limitations were not measurable and purely based on whether the device was functional at a given temperature. The Sectional Shmoo was developed to measure these temperature limitations across the die without touching a given memory cell more than once, thereby preserving any temperature related change. This new measurement value is called the Pristine Margin. Using the pristine margin, the temperature related effects on the F-RAM were analyzed and a discussion about the impact on 1T1C operation is presented.
ACKNOWLEDGMENTS

I would like to thank all the people who contributed in some way to the work described in this thesis. First and foremost, I thank my thesis advisor, Dr. T.S. Kalkur, for your guidance and support throughout my entire academic career and for allowing me to pursue a topic that I am truly passionate about. I would like to thank Dr. John Lindsey and Dr. Darshika Perera, for serving on my thesis committee, always being available to answer questions and for challenging me throughout my coursework. It is the dedication and enthusiasm of these three professors that made my time in the UCCS graduate program enjoyable and rewarding!

I would also like thank Madhu Joseph, Shan Sun, and Fan Chu. It has been a privilege working with you at Cypress Semiconductor for the last three years. Your level of knowledge and insight into the field of ferroelectric memory is truly humbling and continues to motivate me to learn all I can. A special thanks to Madhu, I can’t even begin to express how much I appreciate the time and effort that you have put into mentoring me. I would not have achieved the level of success that I have experienced at Cypress without your leadership.

I would like to thank my family to whom I owe a great deal. To my late father Brian, taken from this world far too early, thank you for always loving and believing in me, even in the face of my greatest failures. To my mother Diane, the strongest woman I have ever met, who has always only ever wanted the best for her children, has done everything she can to make it happen, and never asked for anything in return. To my in-laws Mike and Madonna, thank you for your continuous encouragement and interest in whatever I’m working on. Finally, to my wife, Lindsay for her endless patience throughout our marriage even that 3-year period where we had to move in with my parents while I earned my undergraduate.
# TABLE OF CONTENTS

**CHAPTER**

**INTRODUCTION** ......................................................................................................... 1

1.1 Background ..................................................................................................... 1

1.2 Aims/Objectives .............................................................................................. 3

1.3 Thesis Structure ............................................................................................... 3

1.4 Expected Contribution..................................................................................... 3

**FERROELECTRICS BACKGROUND** ................................................................. 4

2.1 Basic Physics of F-RAM.................................................................................. 4

2.2 Ferroelectric Free Energy Diagram ............................................................... 10

2.3 Under-saturation ............................................................................................ 12

2.4 Polarization Back-switching ......................................................................... 14

2.5 Thermal Depolarization ............................................................................... 15

2.6 F-RAM Cell Structure and Operation ........................................................... 16

**TESTING METHODOLOGY** .............................................................................. 20

3.1 Sample Selection ........................................................................................... 20

3.2 Test Equipment ............................................................................................. 20

3.3 Conventional Shmoo versus Sectional Shmoo.............................................. 21

3.4 Sectional Shmoo ............................................................................................ 22

3.5 F-RAM Margin ............................................................................................. 24

**EXPERIMENTAL METHODOLOGY AND RESULTS** ................................. 26
4.1 DOE1: New Margin versus Temperature...................................................... 26
  4.1.1 DOE1: Experimental Methodology ....................................................... 26
  4.1.2 DOE1: Experimental Results............................................................... 27

4.2 DOE2: Thermal Depolarization by Pristine Margin ............................... 33
  4.2.1 DOE2: Experimental Methodology ....................................................... 33
  4.2.2 DOE2: Experimental Results............................................................... 34

4.3 DOE3: Writing Temperature Effects by Pristine Margin ....................... 36
  4.3.1 DOE3: Experimental Methodology ....................................................... 36
  4.3.2 DOE3: Experimental Results............................................................... 36

4.4 DOE4: Reading Temperature Effects by Pristine Margin ....................... 40
  4.4.1 DOE4: Experimental Methodology ....................................................... 40
  4.4.2 DOE4: Experimental Results............................................................... 40

DISCUSSION.............................................................................................................. 44

5.1 Conclusions ................................................................................................... 44

5.2 Future Work .................................................................................................. 45

REFERENCES ............................................................................................................ 45
LIST OF FIGURES

Figure 2-1 John Valasek’s Ferroelectric Hysteresis Loop [1] .............................................. 5
Figure 2-2 Ideal Perovskite crystalline structure [5] .......................................................... 6
Figure 2-3 Oxygen Octahedral in the Perovskite crystal structure [5] ............................ 7
Figure 2-4 Ferroelectric domains before, during and after polarization [6] ................. 8
Figure 2-5 P.U.N.D. Pulse Train (left) and Ferroelectric Hysteresis Loop (right) ....... 9
Figure 2-6 Hysteresis Loop Current Measurement ....................................................... 10
Figure 2-7 Basic Free Energy Diagram ................................................................. 10
Figure 2-8 Free Energy Diagram Vs. Temperature ......................................................... 11
Figure 2-9 P-E Hysteresis Loop at various temperatures [10] ........................................ 12
Figure 2-10 P-E Hysteresis Loop with difference applied electric fields ....................... 13
Figure 2-11 Back switching polarization at different electric fields [16] ......................... 15
Figure 2-12 Basic F-RAM Cell [8] ........................................................................ 16
Figure 2-13 2T2C (left) and 1T1C (right) F-RAM cells .............................................. 17
Figure 2-14 F-RAM Cell Write Operation and Hysteresis Diagrams [10] ....................... 18
Figure 2-15 F-RAM Cell Read Operation and Hysteresis Diagrams [10] ..................... 18
Figure 3-1 Handtest Board Socket and Temperature Sensor Layout ............................. 21
Figure 3-2 Conventional Shmoo versus Sectional Shmoo ............................................ 23
Figure 3-3 F-RAM Margin ......................................................................................... 25
Figure 4-1 DOE1: New Margin vs. Temperature Flow ................................................. 27
Figure 4-2 DOE1: P Expected vs. P Actual Values ..................................................... 28
Figure 4-3 DOE1: U Expected vs. U Actual Values ................................................... 29
Figure 4-4 Schematic of domain structure inside of polycrystalline material [14] ...... 30
Figure 4-5 Undersaturation and back-switching effect ............................................... 31
Figure 4-6 DOE1: Pristine Margin vs. Temperature Results ....................................... 33
Figure 4-7 DOE2: Thermal Depolarization Effects Flow……………………………………34
Figure 4-8 DOE2: Thermal Depolarization Results of a single unit .........................34
Figure 4-9 DOE2: Thermal Depolarization Results of 16 units ...............................35
Figure 4-10 DOE3: Writing Temperature Effects Flow .............................................36
Figure 4-11 DOE3: Pristine Margin vs. Temperature Results.................................37
Figure 4-12 DOE1 vs. DOE3: P-U Pristine Margin vs. Temperature Results .........38
Figure 4-13 DOE3: Read Temperature Effects Flow ...............................................40
Figure 4-14 DOE4: Pristine Margin vs. Temperature Results.................................41
Figure 4-15 DOE4: P+U Pristine Margin vs. Temperature Results .........................42
1.1 Background

We live in an era of technology, where nearly every facet of our daily lives is linked to some form of electronic device. These electronic devices take on many forms, from personal electronic devices such as cell phones and tablets to automotive electronics such as infotainment systems and event data recorders (collision black boxes), and even portable medical devices such as blood glucose sensors and hearing aids. While these electronic devices differ in many ways, one thing that they share is that they all take advantage of memory to store data. When it comes to memory, the phrases too much, too fast, and too low-power do not apply.

As demand for consumer electronics continues to grow, device manufacturers are pushing semiconductor companies to develop and innovate memories to have higher reliability, faster read/write performance, lower power and smaller die/package footprints than the current top performing memory technologies. The present leading memories are static RAM (SRAM), high speed but volatile memory; dynamic RAM (DRAM), a high density but volatile memory; EEPROM and Flash both have non-volatility but are slower and require high voltages during data write. Additionally, Flash has extremely high density but limited rewrite endurance. Although not a new technology, ferroelectric RAM (F-RAM) has recently emerged as a strong candidate to replace other memory technologies. It is already marketed as a replacement memory for EEPROM, and battery-backed SRAM. It also has the potential to replace DRAM and Flash memories in the future. F-RAM combines the best features of other memories with fewer drawbacks. F-RAM is non-volatile like Flash and EEPROM, with the high-speed performance of SRAM and D-RAM. F-RAM also has added advantages of being
low-power with high endurance reliability, is immune to magnetic fields and naturally resistant to radiation (RADHARD). With all the benefits that F-RAM has over other memory technologies, why is F-RAM not already the primary choice for device manufacturers? The primary challenge facing F-RAM is storage density.

For F-RAM to achieve the market success enjoyed by other memory technologies memory density needs to be increased. The primary limitation to F-RAM density is die size. There are two primary cell structures used in F-RAMs today; the more popular 2T2C (two transistors two capacitors) structure and the 1T1C structure. The 2T2C cell structure is made up of two 1T1C cells. Because the 2T2C structure is two 1T1C cells, it also takes twice the chip area to duplicate the same density. Therefore, just by changing from 2T2C to 1T1C, the memory density is doubled within the same area. So why aren’t all manufacturers using just 1T1C cell structures?

2T2C is more widely used because it performs better across temperature. There are current 2T2C products on the market with temperature ranges from -55C to 125C. Whereas, in 1T1C the operational range is -45C to 85C. To understand the temperature limitations, it is necessary to understand the behavior of the F-RAM cell across temperature. Due to the F-RAM having a destructive read process, data collection of the pristine margin across temperature was not previously possible. This thesis introduces a new testing technique called the Sectional Shmoo to measure the pristine margin of the device across temperature. This new look at device performance will help to improve our understanding of F-RAM performance and highlight possible improvements to overcome the temperature related limitations.
1.2 Aims/Objectives

This thesis aims to further the understanding of F-RAM cell performance concerning temperature by using a new testing method called the sectional shmoo. The sectional shmoo will understand the following issues in F-RAMS:

- Thermal Depolarization Effects
- Temperature effects on writing
- Temperature effects on reading

1.3 Thesis Structure

The next chapters describe the theoretical background, experiment design, results, and conclusions. Specifically, chapter 2 of this thesis introduces the phenomenon of ferroelectricity and how it is used to store data in current memory cell configurations. Chapter 3 outlines the sample selection and systems used for testing. Chapter 3 also introduces the new sectional shmoo program that was used to collect the data presented in Chapter 4. Chapter 4 describes the design and results of the experimental data collected during the experiments. Finally, chapter 5 summarizes the results and impact as they relate to the objectives of the thesis.

1.4 Expected Contribution

This thesis will address F-RAM manufacturers and researchers about the across temperature performance and limitations of current ferroelectric memory cells. It will contribute by providing data not previously seen, thanks to the new Sectional Shmoo testing method, showing the performance of F-RAM across temperature.
CHAPTER II
FERROELECTRICS BACKGROUND

2.1 Basic Physics of F-RAM

Ferroelectric Random-Access Memory, or F-RAM for short, relies on ferroelectric materials that take advantage of a spontaneous electric polarization phenomenon to store data. To understand the principals of F-RAM operation, one must first understand how the phenomenon works. Ferroelectricity derives its name from ferromagnetism which occurs in materials like iron. When an external magnetic field is applied to a ferromagnetic material, the atoms within that material will orient themselves in the direction of the magnetic field, and the material becomes magnetized. When the magnetic field is removed, part of the atomic alignment will remain. Thus, the material remains magnetized. The ferromagnetic will remain magnetized in the same direction until, either a magnetic field is applied in the opposite direction, switching the direction of the magnetism, or with the use of high heat, which will demagnetize the material. The ability to magnetize a ferromagnetic in the direction of a magnetic field and its subsequent retention results in a hysteresis within the material.

A similar effect was discovered in 1920 by Joseph Valasek while working with Rochelle salt and electricity. In his paper titled “Piezoelectric and allied Phenomena in Rochelle salt,” Valasek describes how in the presence of an electric field, the atoms of the Rochelle salt would align in themselves in the direction of the field and after the removal of the field, the alignment would remain. Comparing these results to the then known phenomenon of ferromagnetics he states that “the dielectric displacement $D$, electric intensity $E$, and polarization $P$” that he observed in Rochelle Salt are “analogous to $B$, $H$ and $I$ in the case of magnetism.” It was in this paper that the ferroelectric hysteresis loop, Figure 2-1, was first introduced. [1]
Although Valasek never used the term ferroelectricity in his research, it was his explanation of the phenomena that ultimately lead to the adoption of the term. The term ferroelectricity was first coined by Erwin Schrödinger in 1912 when he postulated that all solids should become “ferroelectrish” at sufficiently low temperatures [2]. After Valasek’s discovery of the ferroelectric behavior in Rochelle Salt, academics around the world began to research whether other materials showed similar characteristics. Gert Steulmann, a scientist from the “Institut fur allgemeine Electrotechnik” (Institute of General Electrical Engineering) in Dresden, Germany, theorized that there was some form of dipole within the crystal structure of the ferroelectric materials that gave them their unique properties. Stuelmann’s theory was later proven correct in 1935 by Paul Scherrer and his student Georg Busch using monopotassium phosphate, KH$_2$PO$_4$. This discovery became the new groundwork for the field of ferroelectricity.

During World War 2, while looking for a replacement for the dielectric material known as “mica,” scientists in the United States, Russia, and Japan independently created a new human-made material known as Barium Titanate (BaTiO$_3$). BaTiO$_3$ was discovered to have a dielectric constant ten times larger than any other materials known.
at the time. While trying to understand the characteristics that made BaTiO$_3$ have such a large dielectric constant, scientists discovered that BaTiO$_3$ demonstrated the same ferroelectric properties described by Valasek’s experiments with Rochelle Salt. In 1945, Helen Megaw published a paper describing the crystal structure of BaTiO$_3$; observed through x-ray diffraction, she found that BaTiO$_3$ had a distorted perovskite crystal structure. Lead zirconate titanate (PZT (Pb(Zr$_{1-x}$Ti$_x$)O$_3$)), the most common ferroelectric material used in F-RAM, including the devices evaluated for this document, also exhibits this distorted perovskite structure. The ideal perovskite crystal structure, known as ABO$_3$, illustrated in Figure 2-2, is cubic, centrosymmetric, and para-electric.

![Figure 2-2 Ideal Perovskite crystalline structure](image)

Para-electric means that in the presence of an electric field the material will temporarily polarize, once the field is removed the material will return to its non-polarized state. While ideal for the perovskite structure this is non-ideal for ferroelectrics, which is why the distorted perovskite crystal structure is so important. The Goldschmidt tolerance factor, created by Victor Goldschmidt in 1926 [3], is used to describe the stability or distortion of the perovskite crystal structure. The tolerance factor formula shown below is a ratio of the ionic radii of the crystal structure, where $r_A$ is the radius of the A ion, $r_B$ is the radius of the B ion, and $r_X$ is the radius of the X ion [3].
\[
t = \frac{r_A + r_X}{\sqrt{2(r_B + r_X)}}
\]

A tolerance factor of 1 indicates an ideal perovskite crystal structure. If the tolerance factor is larger or smaller than 1 and the material is below the Curie temperature, the structure becomes distorted to a rhombohedral, orthorhombic or tetragonal shape. As the material approaches and then exceeds the Curie temperature, the perovskite structure takes on the cubic, centrosymmetric, and para-electric characteristics of the ideal structure, meaning that polarization in the material is lost.

The distorted perovskite crystal structure forces the oxygen ions on the cubic face into an octahedral. The stretching of the unit cell allows the B ion to shift into one of two low energy stables states along the polar axis of the oxygen octahedral, creating an electrical dipole. It is this dipole, as Stuelmann theorized, that aligns in the direction of the applied electric field. Figure 2-3 shows the two possible positions of the B ion within the oxygen octahedral.

![Figure 2-3 Oxygen Octahedral in the Perovskite crystal structure [5]](image)

In a ferroelectric crystal, the dipoles of all unit cells within a given region will align in the same direction. These regions are called ferroelectric domains. When a ferroelectric crystal is first formed, there will be multiple domains, with individual and random polarizations such that there is no net polarization. In the presence of an
electrical field, the domains will align themselves in the direction of that field, polarizing the crystal. Figure 2-4, is a representation of how the domains look before, during and after the application of an electric field, where $\Delta S$ is the change in crystal length during polarization, and $\Delta S_r$ is the residual change in length after polarization [6].

![Ferroelectric domains before, during and after polarization](image)

Figure 2-4 Ferroelectric domains before, during and after polarization [6]

After the electric field is removed, there is a remnant polarization ($P_r$) within the crystal. The remnant polarization will remain until an electric field higher than the coercive field, the minimum electric field required to reverse the polarization, is applied in the opposite direction, or until the material is brought above the Curie temperature. Above the Curie temperature the material is para-electric, and polarization is lost. Remnant polarization and resistance to domain switching are what give the ferroelectric material the hysteresis described by Valasek, making it non-volatile.

In F-RAM cells, PZT is used as a dielectric between two electrodes creating a ferroelectric capacitor. The capacitor exhibits the same hysteresis characteristics observed in a single ferroelectric crystal. One method to measure the hysteresis geometry of a ferroelectric capacitor is the Positive Up Negative Down (P.U.N.D.) method [7]. This method uses five sequential pulses to measure the polarization in the
positive and negative directions. The P.U.N.D. pulse train and the resulting hysteresis loop are shown in Figure 2-5 below.

![Figure 2-5 P.U.N.D. Pulse Train (left) and Ferroelectric Hysteresis Loop (right)](image)

After each pulse, the energy (voltage) is brought back to zero, and either negative remnant polarization (-$P_r$) or positive remnant polarization ($P_r$) remains. The first pulse, a negative pulse, is used to place the ferroelectric crystal into a known state, the ferroelectric is polarized in the -$P$ direction. A positive pulse ($P$) is applied, and the polarization is changed to the opposite state, during the polarization change a “switching” current is created. A second positive pulse ($U$) is applied, but because the capacitor is already in the positive direction no switching occurs, during this phase “non-switching” current is created. The subsequent negative pulses $N$ and $D$ perform the same function as $P$ and $U$, only in the negative polarization direction. Figure 2-6 shows the difference between the switching and non-switching currents.
By measuring the difference between the switching and non-switching current, it’s possible to tell if the ferroelectric capacitor is charged in the positive or negative direction.

### 2.2 Ferroelectric Free Energy Diagram

As discussed in the last section, when ferroelectric materials are brought below their respective Curie temperature, the crystal structure distorts, and two low energy states form. The center B cation can travel between these two stable states if enough energy is applied. This can be explained in terms of potential energy between the two adjacent low energy states. A simplified energy diagram is shown in Figure 2-7.
In the energy diagram, the low energy states are represented by two minima. These minima are the same as the remnant polarization locations in the hysteresis loop, \(-P_r\) and \(P_r\). Between the two energy wells, there is an energy barrier, \(\Delta E\), that prevents the ferroelectric from switching polarizations without an ample electric field being applied. As the ferroelectric material is heated and approaches the Curie temperature, the energy wells become shallower, decreasing the energy barrier. This means that the amount of energy required to switch states decreases as the temperature increases. This change in characteristics indicates that the polarization states become less stable with higher temperatures. Once the material exceeds the Curie temperature, the material becomes para-electric, and only one minimum remains. This effect on the energy diagram across temperature is shown below in Figure 2-8, where \(U\) is the energy potential and \(P\) is the polarization at temperatures of \(T << T_c\), \(T < T_c\) and \(T > T_c\).

![Figure 2-8 Free Energy Diagram Vs. Temperature](image)

As the free energy diagram shows, as the temperature decreases, the distance (d) between the two stable B cations sites, \(-P_r\) and \(P_r\), increases along the axis of polarization. This means that as the temperature decreases, polarization is expected to increase. Additionally, as the temperature decreases the energy barrier between the two
energy wells becomes more substantial, this means that a higher electric field needs to be applied to switch the material.

Figure 2-9 shows experimental data collected on a PZT capacitor and published in the journal article “Temperature-Dependent Ferroelectric Hysteresis Properties of Modified Lead Zirconate Titanate Ceramics” [16]. The figure shows the ferroelectric polarization versus energy (P-E) hysteresis loop across the temperature range of 300K to 433K (27°C to 160°C). As previously mentioned, when the electric field equals zero, only the remnant polarization remains. Comparing the Y-axis of Figure 2-9 to the X-axis of Figure 2-8, we can again see that as the temperatures decrease, the distance between $-P_r$ and $P_r$ and the polarization increases. It is also important to note that this data collection was performed using the same electric field across all temperatures; therefore, the only variable affecting polarization in this data is temperature.

![Figure 2-9 P-E Hysteresis Loop at various temperatures](image)

2.3 Under-saturation

In addition to temperature effects, under-saturation is another issue that affects the performance of ferroelectric materials. Under-saturation is caused when an insufficient electric field is applied to the ferroelectric material. There are two possible
reasons that the electric field would not be large enough to overcome the energy barrier between the two energy wells. The first reason is temperature related, as discussed in the previous sections as the temperature of the ferroelectric material is decreased, the perovskite crystalline structure continues to stretch. Therefore, the energy barrier between the two energy wells increases and a higher electric field is required to switch energy wells.

The second reason is the strength of the applied electric field. If the applied electric field is not large enough then some domains won’t switch, this reduces the net polarization of the ferroelectric material. The hysteresis loops in Figure 2-10 were experimentally collected using a Keithley 4200-SCS Parameter Analyzer using the P.U.N.D. pulse train method described at the end of Section 2.1. All data collection was performed at room temperature to prevent any temperature related effect interference. As the figure shows, when the electric field is decreased, the polarization decreases as well.

![Figure 2-10 P-E Hysteresis Loop with difference applied electric fields](image)

Figure 2-10 P-E Hysteresis Loop with difference applied electric fields
Under-saturation is a primary concern for F-RAM developers because the strength of the electric field is controlled by the design of the chip. For example, if the chip has a maximum voltage source of 1.6V, then the maximum available voltage to polarize the ferroelectric capacitors is 1.6V. As shown in Figure 2-10, the 1.6V hysteresis loop has less polarization than the 2.0V. Therefore, by design, the ferroelectric material is already underperforming then if the chip had a larger supply voltage.

2.4 Polarization Back-switching

Polarization back-switching (also referred to as polarization reversal) is a critical issue that affects F-RAM because it reduces the polarization stored in the ferroelectric capacitor. With the decrease in polarization, it becomes more difficult to determine between a data “0” and “1”. When enough electric field is applied to a ferroelectric capacitor, the polarization reaches saturation, $P_s$. After the field is removed, polarization settles back to the stable remnant polarization, $P_r$. This settling is called relaxation. During the relaxation period, some of the switched domains switch back to the opposite state, back switching. This polarization of the back switched domains is the difference between the remnant and the saturated polarizations. Therefore, the back-switching polarization, $P_{bc}$ can be expressed as [16]

$$R_{bc} = P_s - P_r$$

Research has shown that the back-switching polarization obeys the Arrhenius law. Therefore, back switching polarization can be further defined as:

$$R_{bc} = P_0 \exp \left( \frac{-E_A}{k_B T} \right)$$

Where $E_A$ is the activation energy needed to overcome the energy barrier and switch the ferroelectric, and $P_0$ is a constant. As discussed in Section 2.2, as the temperature increases the energy barrier decreases, with the decreased energy barrier, the equation
shows that back switching becomes easier. Figure 2-11 below shows the back-switching polarization from 300K to 440K [16], the overall trend is expected to continue in both directions. Therefore, as the temperatures decrease there is less back switching and higher remnant polarization is expected.

![Figure 2-11 Back switching polarization at different electric fields [16]](image)

2.5 Thermal Depolarization

Thermal depolarization is defined as the reduction of polarization due to temperature. Thermal depolarization is like back-switching but unlike back-switching, thermal depolarization does not occur as the result of a read or write cycle. Thermal depolarization is purely a result of exposure to higher temperatures to the device. As previously discussed, when the temperature of the ferroelectric is increased the activation energy needed to switch between the two remnant polarizations locations decreases. As the back-switching equations show, the lower the activation energy (E_A) and the higher the temperature (T) means that the probability of the switching is much higher.

\[ P_{bc} = P_0 \exp \left(-\frac{E_A}{k_BT}\right) \]
Therefore, if the temperature of the material is increased the activation energy required to switch is decreased, and some of the remnant polarization is switched to the opposite low energy well.

### 2.6 F-RAM Cell Structure and Operation

F-RAM cells are produced in a wide range of configurations; however, two primary configurations dominate the market for F-RAM devices. They are the 2T2C (two transistors two capacitors) and the 1T1C (one transistor one capacitor) configurations. Both 1T1C and 2T2C use the same basic cell structure, as shown in Figure 2-12. The basic structure consists of one ferroelectric capacitor (C\text{FE}) connected to a plate line (PL) at one end and a bit line (BL) on the other, via an access transistor. The gate of the transistor is connected to a word line (WL).

![Figure 2-12 Basic F-RAM Cell [8]](image)

When the word line is active, the transistor turns on creating a capacitive-voltage divider between the ferroelectric capacitator (C\text{FE}) and the total parasitic capacitance of the bit line (C\text{BL}). The plate line voltage is then divided between the two capacitors. The effective capacitance of the ferroelectric capacitor can take one of two states depending on the data stored. Therefore, C\text{FE} can be defined as C\text{FE}_x, where “x” is the defined state, “0” or “1”, respectively. The resulting bit line voltage can then be defined as V_{BL0} and V_{BL1}, where [8]
In the 2T2C configuration, two of the cells from Figure 2-12 are paired together, one ferroelectric capacitor stores the true data state while the other stores the complementary data state. The word lines of the two access transistors are shorted so that when one cell is accessed the complement is also accessed. One cell is connected to the bit line, and the other is connected to bit line bar. Both bit lines feed a sense amplifier, where the bit line bar voltage is used as a reference to determine the state of the bit line voltage. The 1T1C cell is just the basic F-RAM cell from Figure 2-12, but instead of using complementary data as a reference, it uses a fixed internal reference voltage set during manufacturing. Due to the similarity of the circuit most F-RAM device are capable of both 1T1C and 2T2C operations. The configuration is typically set during device assembly, once configured it cannot be changed by the end user. Figure 2-13 below, shows the 2T2C cell compared to the 1T1C cell.

\[
V_{BL0} = V_{PL} \left( \frac{C_{FE0}}{C_{FE0} + C_{BL}} \right)
\]

\[
V_{BL1} = V_{PL} \left( \frac{C_{FE1}}{C_{FE1} + C_{BL}} \right)
\]
To perform a write operation, as shown in Figure 2-14, the bit line is set high for a data ‘1’ or low for a data ‘0’. The word line is set high, connecting the ferroelectric capacitor to the bit line. Finally, a voltage pulse is applied to the plate line. To write data ‘0’ the plate line pulsed high. To write data ‘1’, the plate line is pulled low. This operation allows the full voltage supply to be applied across the capacitor ensuring enough voltage to switch polarization.

![Figure 2-14 F-RAM Cell Write Operation and Hysteresis Diagrams](image)

To perform a read operation, as shown in Figure 2-15, the bit line is pre-charged to 0V and then floated. The word line is set high, connecting the ferroelectric capacitor to the bit line. Next, the plate line is pulsed to high, allowing the ferroelectric capacitor charge to flow onto the bit line, resulting in a bit line voltage increase. As was explained in Section 2.1, the increase in bit line voltage from reading ‘1’ (switching) is larger than when reading a ‘0’ (non-switching).

![Figure 2-15 F-RAM Cell Read Operation and Hysteresis Diagrams](image)

Since polarization switching is needed to read the data state of the ferroelectric capacitor, the data on the ferroelectric capacitor is destroyed after reading the cell, this is known as a destructive read. Due to the destructive read, the data state must be
restored at the end of the read cycle. To restore the data state, the plate line is set low, and the bit line voltage is restored from sense amp, returning the ferroelectric capacitor charge to its original state. After restoring the data, the word line is turned off. All signals are now back to the initial state.
CHAPTER III
TESTING METHODOLOGY

3.1 Sample Selection

For this experiment, 16 units of CY15B104Q were selected. The CY15B104Q is a 4-Mbit Serial (SPI) F-RAM using the 1T1C memory cell structure discussed in Section 1.3. This device is manufactured by Cypress Semiconductor and is commercially available from multiple vendors. The CY15B104Q comes in two package types, the 8-pin EIAJ, and 8-pin TDFN. For this experiment, the package type does not affect the outcome of the testing. Therefore, the EIAJ package was selected due to hardware availability.

The CY15B104Q has a datasheet specified operating temperature from -40°C to 85°C. The experiments contained in this paper push the operation of the device outside of the specified temperature. The official datasheet states that datasheet parameters are only guaranteed between the specified operating temperatures. The results presented in this paper were independently collected and in no way change the operating conditions specified by the datasheet.

All units were provided by Cypress Semiconductor for this experiment. The units underwent the standard production flow. The units were received in the exact condition that any customer would expect to receive them. They did not undergo any unique configuration or additional stresses that would affect the performance of the devices in either a positive or negative way.

3.2 Test Equipment

All data collection for this experiment was performed using the Teradyne Nextest Magnum I system connected to a custom x8 parallelism hand test board. This allowed for data collection on eight units at a time significantly reducing the total test time.
required to collect all data. Due to the amount of data collection needed, an automated handler would have been more efficient, however, due to the number of temperature changes required it would have been difficult to implement.

The temperature was a crucial component of this testing; therefore, it had to be applied and monitored across all devices to ensure an even temperature distribution. Temperatures were maintained using a Temptronic temperature forcing system and monitored using three external thermal couple sensors. The hand test board has four sockets, each able to test 2 units at a time. One sensor was positioned at each outside socket, and the third sensor was placed between the two center sockets, as indicated by the arrows in Figure 3-1. Temperature across all three sockets was kept within +/- .5 degrees of the other two sensors.

![Handtest Board Socket and Temperature Sensor Layout](image)

**Figure 3-1 Handtest Board Socket and Temperature Sensor Layout**

### 3.3 Conventional Shmoo versus Sectional Shmoo

Testing F-RAM performance has traditionally used a test method called the conventional shmoo. To evaluate the performance of the F-RAM, the conventional shmoo sets an internal reference voltage to a specific voltage. The device is written to either data “1” or data “0” and then read back. The reference voltage is fed to the sense amplifier of each memory cell and compared to the bit line voltage output of each ferroelectric capacitor. The test program then compares the data read from the device to the data that was written to the device and reports the number of failed bits for that reference level, increments the internal reference voltage, and the process is repeated, for all internal reference levels.
There is one major disadvantage of using the conventional shmoo on F-RAM devices. This disadvantage is that every read cycle destroys the data stored in the ferroelectric capacitor, and then writes the data back at the end of the cycle. As discussed in Chapter 2, there are multiple temperature effects that influence the polarization stored on the ferroelectric capacitor. Therefore, for example, the memory cells polarization changes from a -65°C write to a 110°C read cannot be measured using the conventional shmoo. This is because the F-RAM is written at -65°C, then read back and restored at 110°C. On the subsequent read for the next reference level, the previous data was written at 110°C. Therefore, the polarization stored on the capacitor is for a 110°C write not a -65°C write. This has significantly limited the ability to characterize the performance of the F-RAM cells across temperature.

3.4 Sectional Shmoo

To measure the effect of writing at one temperature and reading at another a new testing method needed to be developed. This new method is called the Sectional Shmoo. The sectional shmoo divides the F-RAM array into 64 sections and assigns an internal reference setting to each partition. Using the previous example of writing at -65°C and reading at 110°C, when one section of data is read at 110°C for one reference level and restored, all other sections are left untouched. Therefore, all reference levels can be measured for any write and read temperature combination. The previously untitled margin measurement from the sectional shmoo program has been aptly named the pristine margin.

Another example where the sectional shmoo is a powerful tool is when testing for the effects of thermal depolarization due to high temperature bakes. To test for thermal depolarization, a unit is written at a given temperature and then baked at a high temperature for a short period of time. The unit is then read back at the same
temperature as the write to evaluate what effect the bake has on the F-RAM cell. Because of thermal depolarization, it is expected that margin will be lost during the bake. However, when using the conventional shmoo, the data is again destroyed and written back, destroying any measurable change caused by thermal depolarization. The sectional shmoo was used to collect the data presented in Chapter 4 of this thesis. This new data has given us an unprecedented look at how the F-RAM cell works across temperature.

Figure 3-2 below shows the measurement difference between the Conventional Shmoo and Sectional Shmoo. The data shown was collected on the same unit at room temperature with no additional stresses between measurements. The data shows a slightly lower bit fail count when measuring with the sectional shmoo. This is because the sample size of the sectional shmoo is 1/64 the size (65536 bits) of the conventional shmoo (4194304 bits). Therefore, the probability that the lowest performing bit is measured at a given reference is less. Measurements across multiple units showed only an average of 1 reference unit difference between the two shmoos; this is negligible.

Figure 3-2 Conventional Shmoo versus Sectional Shmoo
3.5 F-RAM Margin

The term margin in F-RAM memories is used to refer to the difference between the measured bit line voltage and a reference voltage. As mentioned in Section 2.6, in the 2T2C configuration a ‘0’ or ‘1’ is determined by feeding the two paired capacitors to the same sense amplifier. Bit line bar is then used as the reference to determine if the bit line is above or below the reference, the sense amplifier will then output data “1” (also referred to as P term) or data “0” (also referred to as U term), respectively. Therefore, the margin of a 2T2C cell is the difference between the voltage on the bit line and the bit line bar voltage. Using the alternate terms margin is often described as P – U.

In 1T1C operation, the data state is determined by finding the difference between the bit line voltage and a reference voltage. The reference voltage is an internal setting that is set by the manufacturer. If the bit line voltage is greater than the reference voltage the sense amplifier outputs data “1” (P Term), and if the bit line voltage is below the reference voltage the sense amplifier outputs data “0” (U Term). In 1T1C, the margin is defined as P – Ref or Ref – U. From these two equations, if the P becomes too small or U becomes too large, then the margin becomes a negative margin measurement externally is seen as the opposite data state internally to the part. Therefore, a P becomes a U and vice versa. Since the 1T1C reference is placed between P and U, the margin for 2T2C will also be larger than 1T1C margin. It’s for this reason that 2T2C (although taking up more chip area) is considered more robust than 1T1C. Figure 3-3 shows the internal reference versus the bit fail count. U0 and P0 are the last measured reference voltage that shows a bit fail count of zero bits. The U0 and P0 are the worst-case for all the measured capacitors.
Figure 3-3 F-RAM Margin
CHAPTER IV

EXPERIMENTAL METHODOLOGY AND RESULTS

There are two parts to any experiment: the design of the experiment and the statistical analysis of the data. Each section in this chapter focuses on the methodology and results of one experiment. All plotted values shown are the mean value of the 16 units for the given measurement. The mean value was selected for data presentation because this thesis intends to evaluate the overall trend in ferroelectric performance across temperature. As previously stated in Section 3.5, the P and U values refer to the last reference value to show zero failing bits.

4.1 DOE1: New Margin versus Temperature

The purpose of this experiment is to determine the read and write performance of the ferroelectric capacitor at a given temperature. The experimental methodology and results are presented in the following sections.

4.1.1 DOE1: Experimental Methodology

In this experiment, the write and read of a data state are both performed at the same temperature. This is believed to be the ideal condition to test the ferroelectric capacitor because there are no factors such as a change in temperature placing any stress that alter the physical performance of the ferroelectric capacitor. As mentioned in Chapter 3, the devices used for this thesis have an operating range of -40C to 85C, it is understood that this is an active product that is currently in production and available to customer’s so to understand the capabilities of the ferroelectric material the devices were tested from -65C to 110C. Figure 4-1 below shows the initial flow that was created to perform the data collection.
4.1.2 DOE1: Experimental Results

The P-term performed as expected, as the temperatures decrease from 110°C to -20°C, the margin to the reference increases linearly. This was expected due to the increase in polarization caused by the increase in cation displacement as discussed in Section 2.2. To recap, as the temperatures decrease the perovskite crystal lattice stretches, increasing the distance between the two stable cation sites, thus increasing the polarization of cell. After -20°C however, the P-term margin begins to decrease, this due to under-saturation, as discussed in Section 2.3. As the temperature decreases, a higher voltage is required to switch the ferroelectric capacitor. If we assumed that voltage available to polarize the ferroelectric capacitor is unlimited, we would expect the linear trend of the P-term at lower temperatures to continue, until the crystal lattice is no longer physically capable of stretching. This expected linear trend versus the actual data collected is shown in Figure 4-2. The expected trend line is purely based on the expected trend and not calculated values.
However, since the F-RAM chip can only provide so much voltage by design, there is a point where the voltage is no longer high enough to saturate (under-saturation) the ferroelectric capacitor, thereby reducing the polarization, which reduces the bit line voltage of the F-RAM cell. In the case of DOE1, it is impossible to determine if the under-saturation is occurring during the write or read cycle.

Unlike the P-term, the U-term did not behave as expected. Stepping back and looking at the ideal physical behavior of a single ferroelectric crystal it was expected that the U-term would mirror the P-term about a central axis. As with the P-term, if the temperature decreases then the cation displacement increases increasing polarization. Therefore, the U-term margin was expected to improve as the temperature decreases. Additionally, if voltage available to the ferroelectric capacitor is unlimited we would expect the linear trend of the U-term to continue at lower temperatures, as shown by U-expected in Figure 4-3. The expected trend line is purely based on expected trend and not calculated values.
The actual versus expected data challenged the understanding of how the ferroelectric capacitor was expected to behave. There are two possibilities for the discrepancy. First, the data collected is incorrect, or the behavior is the result of unanticipated factors. If one accepts that the reported value from the experiment is accurate then what effects would lead to the discrepancy between expected and actual measurements? Although not confirmed during this thesis, based on the physics of ferroelectrics it is believed that this behavior is the result of back-switching due to process defects in the alignment of domains within the ferroelectric capacitor.

In an ideal ferroelectric capacitor, the polar axes of all PZT domains would be oriented in the same direction, and parallel to the electrical field. With all polar axes aligned in the same direction, when an electrical field is applied all polarization would orient in the direction of the field. This would result in the highest possible polarization for the given area of material. Real-world ferroelectric ceramics are polycrystalline materials. This means that instead of a single crystal the materials are made of multiple
crystallites referred to as grains. In a polycrystalline material, the crystallographic orientation of the grains is mostly random. Therefore, the orientation of the polar axes is random as well [12] as shown in Figure 4-4.

As Figure 4-4 shows, due to the random orientation of the domains, the magnitude and direction of the polarization vectors are also random. Using vector mathematics, we can define the magnitude of the vector as \( P \), and the direction as \( \theta \). Only the polarization in the direction of the applied field (Y-axis) affects the net polarization of the material, which can be defined as \( P_y \). Converting from Polar coordinates to Cartesian, the polarization in the direction of the field can be found by the equation:

\[
P_y = P \cdot \sin(\theta)
\]

The net polarization of the capacitor is the summation of all \( P_y \) terms. As the equation shows if the polarization vector is perpendicular to the applied field then \( P_y = 0 \). Therefore, the polarization for that domain is zero.

Figure 2-10 showed the hysteresis loops for three different applied voltages at one temperature. The hysteresis loops showed that at the different voltages the switched polarization at \(-P_r\) (P term) remained relatively consistent, whereas the polarization at \( P_r \) (U term) decreased as the applied voltage decreased. This means that the back
switching, $P_{bc}$, of the U term is higher than that of the P term. Figure 4-5 combines the undersaturation P-E hysteresis loop, Figure 2-10, presented in Section 2.3, collected on a PZT capacitor test structure similar to those used within the memory cells, and the back switching theory presented in Section 2.4.

![Figure 4-5 Undersaturation and back-switching effect](image)

Section 2.4 defines back-switching as:

$$P_{bc} = P_s - P_r$$

Figure 4-5 also shows that the saturated polarization ($P_s$) reaches roughly 33µC/cm$^2$ for both a P and U-terms. Using the back-switching equation and the value for $P_s$, it is shown that $P_r$ for the U-term is approximately 17.5µC/cm$^2$ and for the P-term, it is approximately 21µC/cm$^2$. As stated in Section 2.4, the back-switching polarization can also be calculated as:

$$P_{bc} = P_0 \exp\left(-\frac{E_A}{k_B T}\right)$$

In this equation, $P_0$ and $k_B$ are both fixed values, and all measurements were taken at room temperature. This means that for this equation to hold true when the applied
voltage is removed the activation energy must be lower for U-term than for the P-term. The lower activation energy means that when a U-term is written, there is a higher probability of back switching. This back switching reduces the polarization charge of the U-term, causing a higher bit line voltage, and thus reducing the U margin as shown in Figure 4-3 DOE1: U Expected vs. U Actual Values. As previously stated it is believed that this effect is the result of the random orientation of the PZT domains within the ferroelectric capacitor.

Figure 4-6 below, shows P and U-terms from DOE1 combined on a single plot. As discussed in Section 2.6, the 2T2C operation is a comparison of P to U. If the bit line is P and bit line bar is U, then data is ‘0’ and vice versa for data ‘1’. The section also states that 1T1C margin is determined by an internal reference signal minus P or U. This means that if you can fit a reference between P and U and there is enough margin for the sense amplifier circuit to discern a difference, then 1T1C operation is possible from -65C to 110C. We know that as the temperature increases polarization decreases. Therefore, the trend of Figure 4-6 will continue as the temperatures increase. Eventually, the P and U terms would be equal at the Curie temperature where the ferroelectric capacitor becomes para-electric, and a reference could no longer be placed between the two terms meaning that the device would not be able to differentiate between a 1 and a 0.
4.2 DOE2: Thermal Depolarization by Pristine Margin

The purpose of this experiment is to determine the effects of thermal depolarization after bake at increasing temperatures.

4.2.1 DOE2: Experimental Methodology

In this experiment, the data is written at room temperature, the units are then baked at increasing temperatures and then read back at room temperature using the Sectional Shmoo to measure the pristine margin. Testing with this methodology guarantees that any change in the F-RAM cell behavior can be attributed to the effects of thermal depolarization. To understand the effect of thermal depolarization on the ferroelectric material the devices were baked from 85°C to 260°C. Figure 4-6 Figure 4-10 below shows the initial flow that was created to perform the data collection.
4.2.2 DOE2: Experimental Results

The net polarization of a ferroelectric capacitor does not change for a given temperature. Therefore, any polarization lost from one energy well is transferred to the other energy well. Therefore, if a device is written at 25C, heated up to 260C, then read at 25C, all effects seen are due to the thermal depolarization effect. The results were plotted using two methods. The first plot, Figure 4-8 shows the thermal depolarization of a single unit across temperature.

Figure 4-8 DOE2: Thermal Depolarization Results of a single unit
In Figure 4-8 the effect of thermal depolarization can be clearly seen. As the bake temperature increases the P and U margin continue to decrease as excepted. In Figure 4-9 below, each pair of U and P term points represents the average U0 and P0 values from all 16 units. Two data sets are shown, the first using circles as markers shows the temporary effect due to thermal depolarization, that is that the read is performed immediately after the bake without any reconditioning. The second data set using squares as markers shows the permanent effect on the memory cell. The measurement was taken after reconditioning the device with a write after the bake. This showed ~3 reference unit of permanent margin loss due to the thermal depolarization effect.

Figure 4-9 DOE2: Thermal Depolarization Results of 16 units

As the bake temperature increased to 260C, the P – U margin becomes so small (~2 reference units) that this confirmed that data in 1T1C will not survive a 260C 10-minute bake and that there is a risk to the data even in 2T2C. The F-RAM datasheet for the CY15B102Q-SXE states that the devices max reflow is 260C for 3 seconds, this is to reduce the risk of data loss to the device’s configuration settings. As discussed in
Section 3.4, this data was not previously possible to collect, due to the difference between new margin versus pristine margin.

4.3 DOE3: Writing Temperature Effects by Pristine Margin

The purpose of this experiment is to understand the effects of temperature when writing to the F-RAM. The experimental methodology and results are presented in the following sections.

4.3.1 DOE3: Experimental Methodology

In this experiment, the data is written across temperature and then read back at 110C using the Sectional Shmoo to measure the pristine margin. Testing with this methodology guarantees that all reads are saturated. Therefore, any change in the F-RAM cell behavior can be attributed to the effects of temperature during the write cycle. To understand the performance of the ferroelectric material the devices were tested from -65C to 110C. Figure 4-10 below shows the initial flow that was created to perform the data collection.

![Figure 4-10 DOE3: Writing Temperature Effects Flow](image)

4.3.2 DOE3: Experimental Results

If the write at each temperature is always saturated, it is expected that U and P would remain constant as the temperature decreased, shown as dotted lines in Figure
4-11. This is because if the ferroelectric capacitor is saturated, the measurement is being taken during the read cycle. Therefore, polarization remains the same regardless of the temperature during the write cycle. Another way to think about this is in terms of cation displacement as a function of temperature. As discussed in Section 2.2, the distance between the energy wells increases as the temperatures decrease. As the device is heated back up to 110°C for the read, the cation displacement decreases to the same distance, meaning that the polarization is the same if the ferroelectric capacitor is saturated during the write. Figure 4-11 below shows the actual measured results.

![Figure 4-11 DOE3: Pristine Margin vs. Temperature Results](image)

Both the U and P-term performed close to expectation, as the temperatures decrease from 110°C to 25°C, the margin to the reference remains relatively flat. Below 25°C the effects of under-saturation can be seen, and the effect is stronger at lower write temperatures. This effect is expected to continue as the temperature decreases until eventually U and P are at the same polarization level, where the voltage needed to
switch is much higher than the voltage applied on the ferroelectric capacitor and the device can no longer distinguish between a “1” and “0”.

If we look at the results of DOE3 in terms of P-U, as shown in Figure 4-12, we can easily compare the results with DOE1. As discussed in the DOE1 results section, the plot shows that total polarization increases as the temperature decreases. It was expected that DOE3 would remain constant until it reached the under-saturation temperature seen in DOE1. However, based on the DOE1 results it was expected that the under-saturation effect would begin at -20C, and as Figure 4-12 appears to show that under-saturation begins at 0C. The total difference between the DOE3 110C write and -20C write however is only four ref units, this is a small variation when compared to the 15 ref units change between DOE1s 110C to -20C.

![Figure 4-12 DOE1 vs. DOE3: P-U Pristine Margin vs. Temperature Results](image)

As stated above, since the read temperature is fixed at 110C, unlike DOE1 all temperature effects seen here are related to the write. Data collection was performed in order from -65C to 110C, so it is believed that this small variation in total polarization
is related to an effect known as “wake up.” Effectively, wake-up is a reorientation of the domains in the direction of the electric field. Experiments have shown that increased temperatures led to a reduction of cycles needed for wake-up [15]. So as the write-read cycles occur, more domains align with the electric field increasing the total polarization. This means that the electric voltage available during the write cycle is not large enough to fully overcome the energy barrier. Therefore, the ferroelectric capacitor is not entirely switching.

There are two design concepts to consider with regards to the data presented from this experiment. The first concept is that to overcome under-saturation due to write temperatures both the bit line and plate line voltages would need to be increased. This increase in voltage would lead to an increase in current, which as discussed in the introduction is not desired by customers. This means that by design, the device will have a minimum temperature range. The total margin at -65C is ~15 ref units. This is more than enough margin to fit a reference signal between the U and P terms for 1T1C operation, however as the temperatures continue to decrease the under-saturation effect will eventually prevent proper operation.

The second design concept is that if device supply power is brought lower in future products, the voltage available to the plate line and bit lines for writes is also reduced. The under-saturation effect would begin at higher temperatures, and this would also move the convergence point of U and P to higher temperatures preventing the device from being able to distinguish between a “1” and a “0”. Both design concepts have the potential to adversely affect future product designs, especially as manufacturers push for smaller products with lower power usage.
4.4 DOE4: Reading Temperature Effects by Pristine Margin

The purpose of this experiment is to understand the effects of temperature when reading from the F-RAM. The experimental methodology and results are presented in the following sections.

4.4.1 DOE4: Experimental Methodology

In this experiment, the data is written at 110C and then read back across temperature using the Sectional Shmoo to measure the pristine margin. Testing with this methodology guarantees that all writes are saturated. Thus, any change in the F-RAM cell’s behavior can be attributed to the effect of temperature on the read, or from the difference in temperature between the write and read. To understand the performance of the ferroelectric material the devices were tested from -65C to 110C. Figure 4-13 below shows the initial flow that was created to perform the data collection.

Figure 4-13 DOE3: Read Temperature Effects Flow

4.4.2 DOE4: Experimental Results

With the write temperature fixed at 110C, this guarantees that the write is always saturated. Because the write is fully saturated, and it is the read that is being
affected by the temperature it is expected that U and P would follow the trends of DOE1. Figure 4-14 below shows the actual measured results.

![Graph showing U, P Pristine Margin vs. Temperature Results](Figure 4-14 DOE4: Pristine Margin vs. Temperature Results)

Both the U and P-term performed as expected, as the temperatures decrease from 110°C to 25°C, the margin follows the trend of DOE1. Below -20°C the effects of under-saturation can be seen which was expected from DOE1. This effect is expected to continue as the temperature decreases until eventually U and P are at the same polarization level and the device can no longer distinguish between a “1” and “0”. Despite the loss of margin, the total polarization does not change, which means that for all the loss in P-term margin, the U-term gains the same margin. This is easily confirmed by plotting the P-term plus U-term for both DOE1 and DOE4, as shown in Figure 4-15 below.
Figure 4-15 DOE4: P+U Pristine Margin vs. Temperature Results

Since the only difference between DOE1 and DOE4 is the read temperature, the expectation is that all effects are related to the read temperature. In this case, the change in margin is due to the write temperature of 110°C. This is because when written at 110°C the cation displacement is smaller than if the device was written at -65°C. When written at 110°C the polarization is set, as the temperature is decreased the cation displacement increases, increasing polarization. However, without the addition of an electric field as with DOE1, the number of domains that have switched was fixed at 110°C; therefore, no additional polarization is created. This effect is the only issue affecting the margin until the temperature reaches ~-20°C at which point the under-saturation effect takes over.

The DOE4 results show that there is still plenty of margin between the P and U-term to place a reference signal for 1T1C operation. Between the DOE1 and DOE4 results there are approximately 34 ref units of difference related to this effect. It is expected that as the write temperature increases and the cation displacement decreases,
the polarization difference between the U and P-terms will continue to decrease. This means that the higher the write temperature, the more the margin loss at lower temperatures. There are several ways to reduce these effects on the ferroelectric capacitor. As with DOE3, one method would be to increase voltage within the device to provide a higher polarization. Another would be to grow perfectly oriented PZT. As stated in DOE3, the plate and bit line voltages are set by design to reduce the current and voltage requirement for the end customer. Perfectly oriented PZT is currently not possible with current processing techniques.
CHAPTER V
DISCUSSION

5.1 Conclusions

A new testing method, called the Section Shmoo, was created and allowed for the first successful collection of pristine margins after varying temperature during read and write operations. The program was also used to measure change in margin due thermal depolarization of the F-RAM devices at temperatures up to 260°C. The known temperature effects on ferroelectrics were presented, the sectional shmoo was used to measure the pristine margin for the first time, and finally the pristine margin was used to validate the known temperature effects on real-world F-RAM devices. Prior to the creation of the sectional shmoo, the temperature performance of the F-RAM was based purely on the understanding of how a single ferroelectric capacitor operated across temperature. This new program allows for analysis of the entire memory array.

Analysis of the data collected and presented in Chapter 4, shows that the F-RAM devices performed as expected regarding reading across temperature and thermal depolarization. It was previously known that writing across temperature did not perform as expected. Thanks to the collection of the pristine margin using the Sectional Shmoo, for the first time the effect was measured, and evaluation shows that this unexpected performance is likely related to undersaturation due to process defects. The data presented in this paper validates 2T2C operation across temperature from -65°C to beyond 110°C, but that thermal depolarization beyond 260°C will have a negative impact on data retention. As stated in the introduction, the largest limitation facing F-RAM today is chip area and density, by converting from 2T2C to 1T1C chip area remains the same and density doubles. The analysis of the pristine margin shows that with an appropriate referencing scheme 1T1C operation from -45°C to 110°C is plausible. This
higher temperature range gives consumers greater flexibility. Unlike 2T2C operation, thermal depolarization of the 1T1C device is likely limited to 200°C, to maintain enough margin to the reference. In addition to device performance, possible areas of improvement such as PZT orientation, or increasing the applied voltage for switching were also presented. With the data presented in Chapter it will be possible for engineers to evaluate the potential design/process changes that could improve device performance across temperature.

In addition to the temperature related data collection, the sectional shmoo can also be used to evaluate the performance F-RAM in situations where devices show low margin issues during testing and qualification by the manufacturer. This new testing methodology opens many opportunities to better understanding the device performance using pristine margin.

5.2 Future Work

This thesis has introduced a novel method for testing the pristine margin of the F-RAM. Analysis of the data showed weaknesses and limitations of F-RAM across temperature and exposed the following areas as recommendations for further work.

- Improved sensing scheme for 1T1C operation.
  - Development of a new scheme for setting the 1T1C internal reference would provide greater device performance across temperature.

- Further investigation into root cause of lower U-term polarization than expected in DOE1.
  - This is believed to be due to undersaturation as a results of process defects within the material, this effect should be further investigated to confirm or reject the hypothesis.
- Process improvement in PZE deposition could be explored to reduce defects.

- Expanded experimental testing using the Sectional Shmoo program.
  - The experiments performed for this thesis are limited in scope to Thermal depolarization and read and writing temperature effects.
  - Further exploration for uses of the program, such as for failure analysis or yield improvement, would be invaluable to F-RAM manufacturers.
REFERENCES


