THESIS

LOW-NOISE, LOW-POWER TRANSIMPEDANCE AMPLIFIER FOR INTEGRATED ELECTROCHEMICAL BIOSENSOR APPLICATIONS

Submitted by

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ABSTRACT

LOW-NOISE, LOW-POWER TRANSIMPEDANCE AMPLIFIER FOR INTEGRATED ELECTROCHEMICAL BIOSENSOR APPLICATIONS

Biosensor devices have found an increasingly broad range of applications including clinical, biological, and even pharmaceutical research and testing. These devices are useful for detecting chemical compounds in solutions and tissues. Current visual or optical methods include fluorescence and bio/chemiluminescence based detection. These methods involve adding luminescent dyes or fluorescent tags to cells or tissue samples to track movement in response to a stimulus. These methods often harm living tissue and interfere with natural cell movement and function.

Electrochemical biosensing methods may be used without adding potentially harmful dyes or chemicals to living tissues. Electrochemical sensing may be used, on the condition that the desired analyte is electrochemically active, and with the assumption that other compounds present are not electrochemically active at the reduction or oxidation potential of the desired analyte. A wide range of analytes can be selectively detected by specifically setting the potential of the solution using a potentiostat. The resulting small-magnitude current must then be converted to a measurable voltage and read using a low-noise transimpedance amplifier.

To provide spatial resolution on the intra-cellular level, a large number of electrodes must be used. To measure electrochemical signals in parallel, each electrode requires a minimum of a transimpedance amplifier, as well as other supporting circuitry. Low power consumption is a requirement for the circuitry to avoid generating large amounts of heat, and small size is necessary to limit silicon area.

This thesis proposes the design of a low-noise, low-power transimpedance amplifier for application in integrated electrochemical biosensor devices. The final proposed design achieves a 5MΩ transimpedance gain with 981aA/$\sqrt{Hz}$ input inferred noise, 8.06μW at 0.9V power supply, and occupies a silicon area of 0.0074mm^2 in a commercial 0.18μm CMOS process. This thesis also explores the development of a multi-channel electrochemical measurement system.

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Chapter 1 Introduction

Biosensor devices have found an increasingly broad range of applications, including but not limited to clinical, biological, environmental, and pharmaceutical testing and research. With ever increasing applications for biosensors, detection hardware in biosensors are required to cover an increasingly broad range of bio-signals. These signals often require very specifically designed detection hardware, to account for conditions such as very weak input signal coupled with high input noise.

With the goal of designing a biosensor system to meet specific biosensor requirements, one specific area of interest is in the ability to detect the spatiotemporal process of cellular communication. The ability to visualize the molecules of cellular communication allows scientists to further understand the biology that drives normal and pathophysiological processes. Electrochemical sensor arrays provide new opportunities for chemical vision without the addition of labels, such as chromophores or fluorophores. The growing interest in high density electrochemical sensor arrays [1] [2] dictates a size requirement for the sensor's electronics which often conflicts with achieving low noise and low power consumption per read channel.

1.1 Biosensing Techniques

Sensing techniques currently in use include fluorescence spectroscopy, bioluminescence and chemiluminescence detection, and electrochemical detection. Fluorescence spectroscopy is a process of adding and tracking fluorescent light-responsive dyes or "label" molecules in a sample. Bio and chemiluminescence detection rely on the detection of a naturally luminescent

substance in an analyte. Electrochemical detection uses a reduction or oxidation reaction (i.e. a redox process) to detect an electrochemically active analyte.

1.1.1 Fluorescence Detection

Fluorescence imaging detection involves adding a fluorescent label to the sample material. As shown in Figure 1, a filtered light source is used to create a single frequency excitation light. Application of the excitation light on a sample containing a fluorescent label causes photon emission from the fluorescent tag to occur at a different frequency, allowing for the optical detection of the fluorescent tag, its target, and their location.

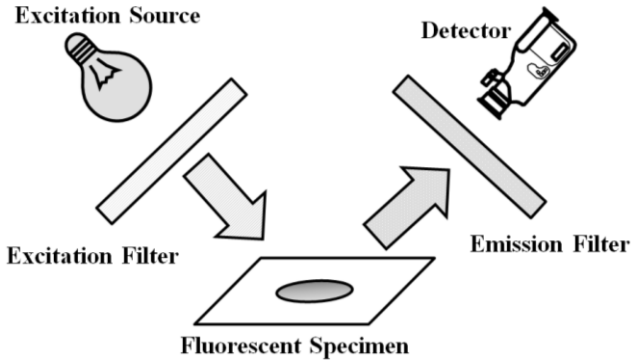

Figure 1-1: Fluorescence Detection Example

Typical fluorescence detection systems use either a high-performance single pixel detector with a scanning excitation source or a two-dimensional array of detectors, such as a CCD sensor, with a homogeneous excitation light source. In a fluorescence detection system, possible array size is determined by CCD implementation and the number of photosensitive pixels [3]. In optical based systems; however, lenses and strategic illumination patterns can be utilized to achieve single-molecule measurement resolutions without the need to greatly reduce the scale of the detection devices [4].

1.1.2 Bio/Chemiluminescence

Bioluminescence and chemiluminescence techniques rely on the emission of light from the analyte. Although generally (but not necessarily) in the visible light spectrum, the small amount of light emitted is usually not visible to the human eye [5]. Detection has been typically achieved with an extremely sensitive CCD sensor and photomultiplier tubes. CMOS image sensors have not been utilized in bioluminescence until more recently due to poor but improving performance and lower SNR [3].

1.1.3 Electrochemical Detection

Using a redox (reduction-oxidation) process, electrochemical detection can be used in a wide range of measurements under the condition that the analyte being measured is electrochemically active [6] [7]. Typical measurement instrumentation includes a two or three electrode system, where a potentiostat is used to hold a specific potential across a sample. Setting a specific potential between the reference (RE) and the working electrode (WE) can be used to selectively detect a specific analyte. The potentiostat also sources or sinks the required current through the counter electrode (CE). A typical three electrode potentiostat system is shown in Figure 1-2 [8].

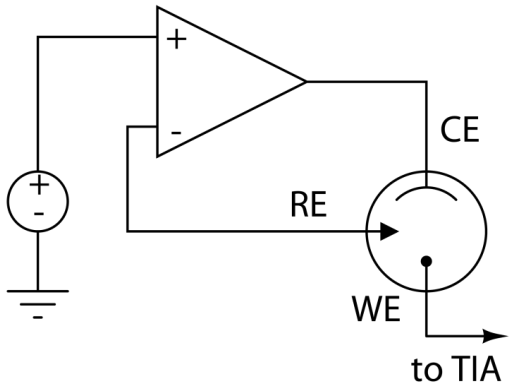

Figure 1-2: Potentiostat and 3-Electrode System

The popularity of electrochemical sensing stems from its ability to detect a wide range of molecules. These molecules include glucose [9], Dopamine [10], Nitric Oxide [11], and γ-Aminobutyric Acid [12]. The electrical nature of this detection method also makes electrochemical detection a more suitable option for integrated sensors and sensor arrays. The sensor circuits presented in this thesis are intended for use in high density electrochemical biosensor arrays, which could be used to provide cellular scale resolution.

1.2 Motivations for Integrated Biosensors

Currently, typical biosensor implementations include custom made sensing devices, ranging from single pixel light detection sensors or single (working) electrode electrochemical systems, all the way to two dimensional light sensors such as CCD or CMOS light detection sensors and multi-dimensional electrode arrays. Many biosensor systems must be further supported with a system of electronics and/or software to supply the end user with meaningful data and a useable interface. In many implementations, designing or even setting up the supporting electronic hardware can become more involved or time consuming than the detection device itself.

With discrete devices external detection hardware is often used due to the readily available forms of computer video recording devices for CCD/CMOS video-based sensors, and the wide range of computer interfaced potentiostat systems. These readily available interfaces have some limitations, including their size, lack of portability, lack of spatial resolution, and need of trained personnel with appropriate laboratory facilities.

1.2.1 Ease of Use

Many integrated solutions include supporting hardware, such as a transimpedance amplifier for both photodiode based light detectors and electrochemical detectors. Including the sensor and detection hardware on a single chip or package with either a wired or wireless interface simplifies the use of the biosensor in research, and allows for greater complexity in hardware. With an integrated system, a user could easily connect an array of thousands of electrodes to a computer for data acquisition using a single connector or wireless interface, eliminating the need for highly trained personnel and bulky hardware. Complete sensor backend integration also provides an abstraction of the sensor's functionality. This can eliminate time consuming setup and the possibility of incorrectly connected devices.

1.2.2 Increased Spatiotemporal Resolution

The use of small molecules to send signals between cells is a hallmark of biological communication. Understanding cellular communication allows for greater insight regarding the biology that drives normal and pathophysiological processes. One of the major difficulties in understanding the actions of small molecules is our inability to directly visualize their release and diffusion through biological tissues. Therefore, understanding cellular communication through cellular level visualization is an important goal in biomedical research. Cellular sizes of interest typically lie within the range of a 20-50μm radius. It is highly desirable to place electrodes with spacing below 50μm [13] [14]. This puts physical limits on the sizing and power consumption of underlying electronics in integrated sensor design. Furthermore, molecules of interest such as nitric oxide, can have a half-life of approximately 500ms. This short half-life

requires biosensors with arrays of electrodes to have high electrode density to provide temporal resolution sufficient for fast evolving molecules during cellular communication.

1.3 Project Goal

The primary goal of this project is the creation of a multi-electrode, electrochemistry-based integrated biosensor system. The proposed device will combine a µ-electrode array, as well as supporting circuitry to both set the potential of a solution and amplify and read out any current induced on the working electrode during a reaction.

A system with a single working electrode can provide temporal resolution, i.e. the concentration of a chemical at a single point in space can be monitored over time. An electrode array can be used to provide both temporal and spatial resolution, allowing the chemical concentration to be monitored over both space and time. If the electrode array is combined with a microscope objective, and a method of visually detecting cells (such as fluorescence marking and detection), the overall system can be used to monitor cells' reaction to the introduction or presence of a particular electrochemically active compound. A diagram of this overall system is shown in Figure 1-3.

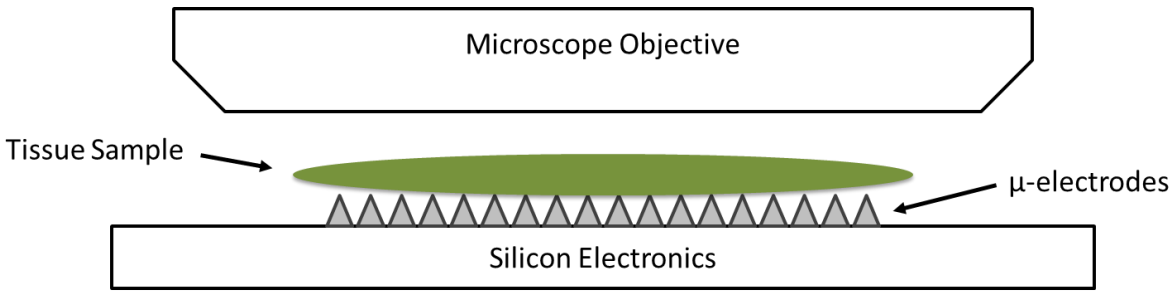

Figure 1-3: Proposed Biosensor and Microscope System

With this proposed system, the user would be provided with both a chemical gradient mapping from the electrode array, as well as a view of cell location and movement from the microscope.

1.4 Objectives

For this project, the primary focus is to create an integrated signal chain to be used for the detection of electrochemically active analytes. A proposed signal chain, consisting of a variety of sub-circuits is shown in Figure 1-4.

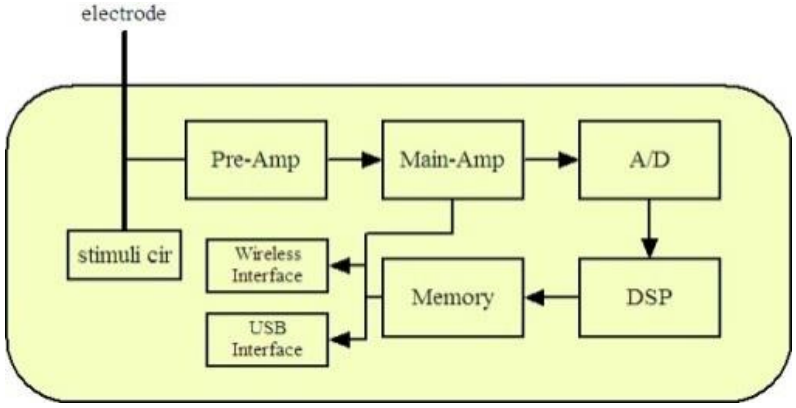

Figure 1-4: Biosensor Signal Chain

The proposed sub-circuits include several critical circuits: a stimuli circuit (potentiostat), a transimpedance-based pre-amplifier, a main voltage amplifier, and an analog-to-digital converter. For the purpose of an integrated sensor array, every working electrode will require its own signal chain for amplifying and converting the current induced on the working electrode to a digital signal.

Due to the small magnitude of the currents being measured, the gain and noise performance of the front-end circuits are key design parameters. Since there will be multiple copies of all of the electronics in the signal chain, the overall circuit area and power consumption

must be kept to a minimum, to maximize spatial resolution and minimize energy dissipation to avoid changing the temperature of the solution or tissue sample on the electrode array. Minimizing power dissipation in the backend circuitry will also allow the potential use of alternative power sources, such as wireless power or energy harvesting, and in the simplest case, increase battery life if the device is battery powered. Reducing the silicon footprint can help reduce the overall device size. Ideally, the supporting electronics would fit directly below the electrode array, allowing the device footprint to be only slightly larger than the area of the electrode array itself.

Chapter 2 Existing TIA Design Work and Theoretical Background

2.1 Introduction

Transimpedance amplifiers are used in a variety of applications, and cover an extremely broad range of specifications. Common applications include detecting signal from photodiodes in high-speed optical communication, and detecting current from accelerometers in micro electromechanical systems applications.

A transimpedance amplifier can be thought of simply as a current to voltage converter, which linearly converts a current input to a corresponding voltage output. The input/output relationship can be described using Ohm's law, and the overall transimpedance gain is measured in Volts/Amperes, or simply in Ohms.

2.2 Transimpedance Amplifier Requirements

2.2.1 Circuit Interface Requirements within the Signal Read Channel

Because the integrated biosensor project is utilizing circuits from several different designers, care must be taken to make sure the sub-circuits are compatible with one-another. As shown in Figure 1-4, the input side of the pre-amplifier circuit is attached to an electrode and a stimuli circuit, which are the Working Electrode and Potentiostat shown in Figure 1-2. Due to

the nature of electrochemical systems, the current input is a single-ended signal. The main amplifier circuit is attached to the output side of the pre-amplifier circuit. The main amplifier uses a differential voltage as its input to improve common-mode noise rejection of the read-channel signal chain, requiring the Transimpedance amplifier to have a differential voltage output.

These requirements designate that a single-ended to differential conversion must take place, and several approaches were taken toward implementing circuits that perform this conversion. These approaches are specifically discussed in section 4.3.2, and throughout Chapter 4.

2.2.2 Noise Requirements

Depending on the application and specifics of the sensor design, the analyte detection process will have an inherent noise level. If the input inferred noise level of the supporting circuitry can be pushed below the noise level of the sensor itself, the circuitry won't impose a limitation on the resolution of the measurements.

In electrochemical detection systems, noise standard deviation has been shown to vary based on electrode area. The noise standard deviation (σ_I) on indium tin oxide electrodes has been shown to increase with the square-root of electrode area for small electrodes, and linearly with area for larger electrodes [15]. Figure 2-1 shows noise generated at the electrode-solution interface as a function of electrode area for electrochemical sensors. For electrodes used in highly integrated sensors, their sizes typically range from a few μm^2 to tens of μm^2 [16]. The standard deviation of the inherent noise from an electrode-solution interface can be lower than 100fA. This puts a limit on the amount of noise that analog biosensor frontend circuitry can generate without compromising sensitivity. The TIA design in this paper focuses on achieving

low input inferred noise and low power consumption while meeting other design requirements for electrochemical sensor arrays.

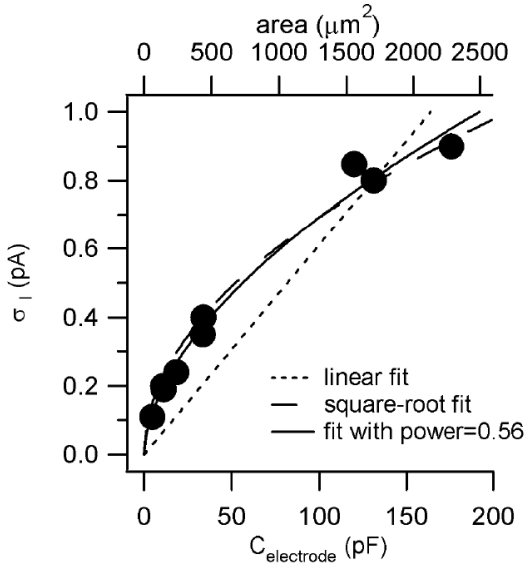

Figure 2-1: Noise Standard Deviation vs. Electrode Area

2.3 Existing Work on Integrated Transimpedance Amplifiers (TIA)

2.3.1 Basic Resistive Transimpedance Amplifier

A basic transimpedance amplifier can be constructed using an operational amplifier, a resistor, and a capacitor. A schematic of the basic topology is shown in Figure 2-2.

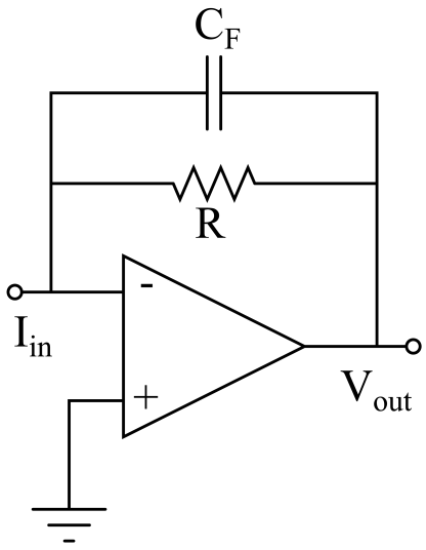

Figure 2-2: Basic Resistive Transimpedance Amplifier

Although simple, this design has several disadvantages. The primary disadvantage in this design is the need of a large resistor, which increases with the required transimpedance gain. Further issues and disadvantages associated with this topology are discussed in sections 2.4 and 2.5.

2.3.2 Novel Continuous Time TIA Designs

One method of avoiding the large resistor needed for high gain and high sensitive TIA design is the use of a resistor T-network to generate a large effective feedback resistance with smaller physical resistors. This topology can be used to achieve both a high transimpedance gain and low noise, while maintaining a large signal to noise dynamic range [17]. An example of this topology is shown in Figure 2-3.

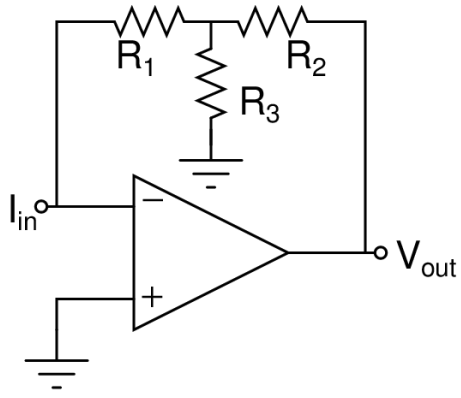

Figure 2-3: Example T-Network TIA Schematic [17]

Although this topology requires significantly less total resistance on chip than its equivalent single-resistor counterpart, the overall size reduction is often still not at the level required by designs of highly integrated biosensor arrays.

An alternative TIA implementation employs the use of an active current reducing circuit in place of the resistor [18]. The overall TIA design with the active feedback network is shown in Figure 2-4.

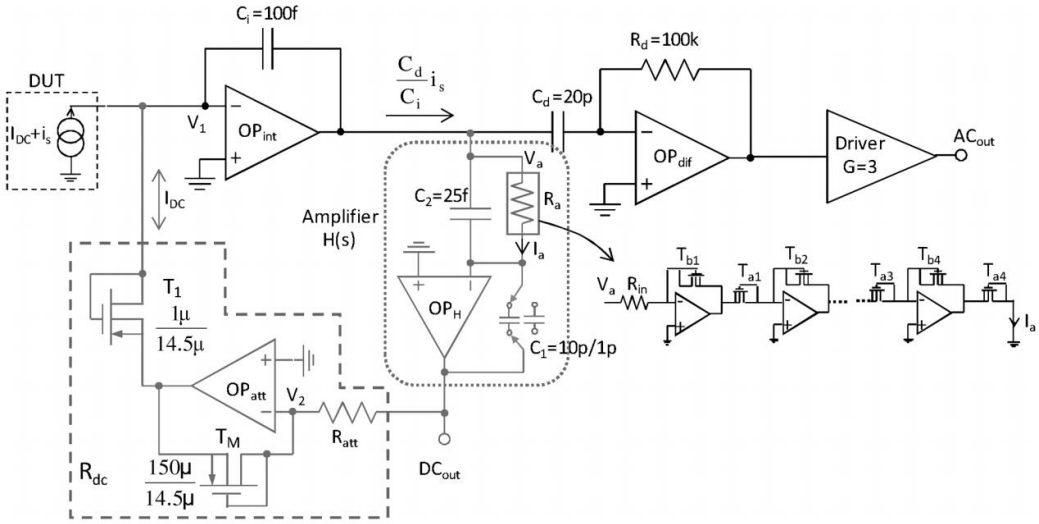

Figure 2-4: TIA with Active Feedback Network [18]

This type of design can be used to emulate very high equivalent resistances of hundreds of GΩ with relatively high linearity. This design implements the current reducing circuit using a series of operational amplifiers which can increase power consumption while still maintaining a reasonable die area. This increased level of power consumption may not be suitable due to the stringent operating temperature requirements of live tissue on our biosensor applications. This design does manage to achieve an extremely low input noise level.

Two other continuous time implementations involve using an active load and ratio of capacitors to generate high effective transimpedance gains [19] [20]. These designs tend to rely on extremely high impedance input biasing circuits, which can consume large amounts of die area. Despite this fact, this topology does tend to produce respectable input noise specifications. A schematic of the overall implementation is shown in Figure 2-5.

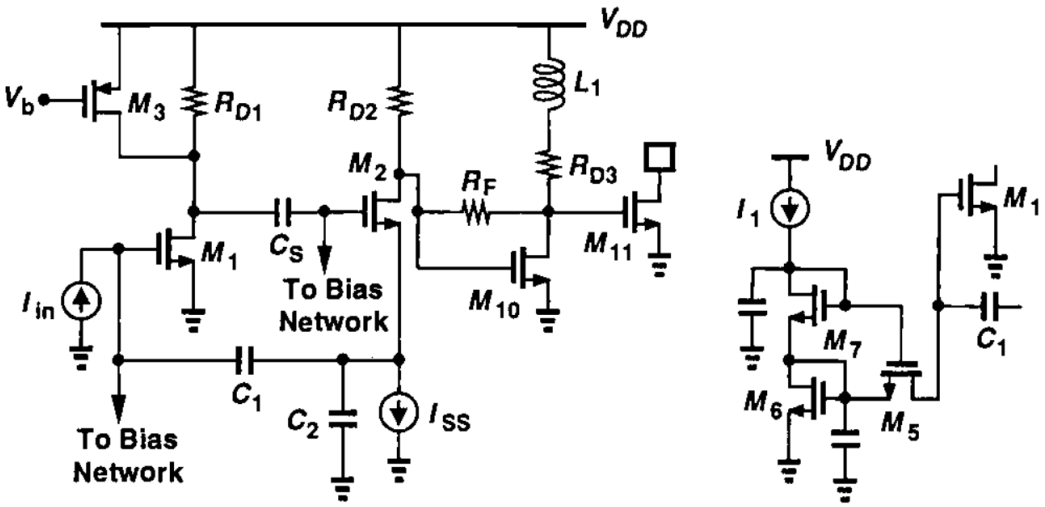

Figure 2-5: Capacitive TIA and Input Bias Network Schematics [19]

An additional continuous TIA design intended for high-speed communication uses a simple resistive TIA topology with an added DC cancellation feedback network [21]. This overall topology is shown in Figure 2-6.

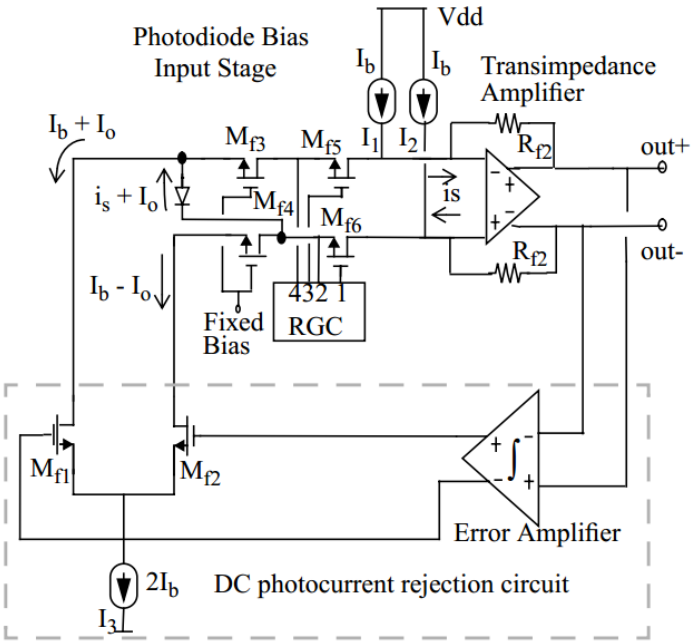

Figure 2-6: DC Cancelling TIA Schematic [21]

The design achieves a bandwidth over 200MHz, and has a power consumption of 12mW at 3V. This significantly increased power consumption is needed for high bandwidth in optical communications. The DC cancellation feedback network is advantageous in communication, eliminating issues due to amplifier offset and 1/f noise. However, in a bio-signal application this DC cancellation can be problematic, causing a loss of slow-changing signals.

A final continuous time implementation utilizes a unique configuration, consisting of a common-gate amplifier in parallel with a common-source amplification stage [22]. The overall schematic diagram is shown in Figure 2-7.

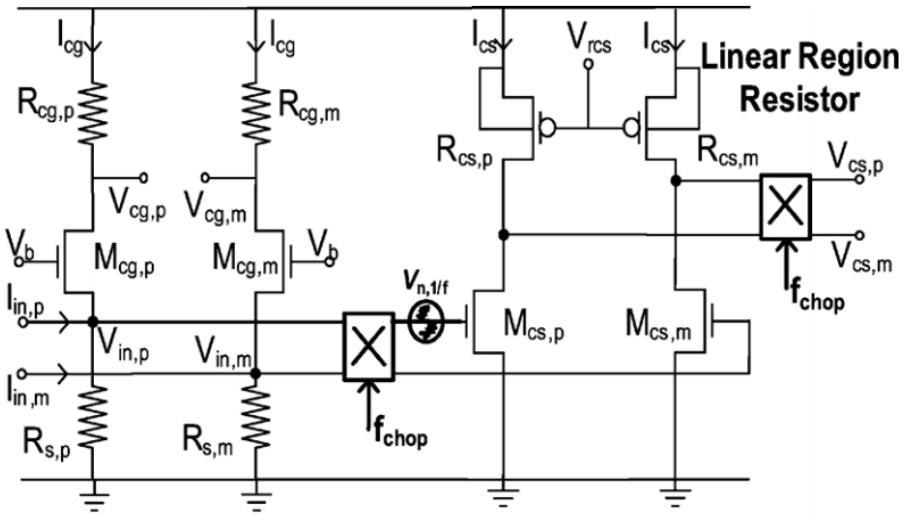

Figure 2-7: TIA CS-CG Design Proposed in [22]

This combination of amplifier types and a chopper-stabilization technique are carefully used to reject 1/f noise. The overall circuit architecture shows promising results, achieving a low input-referred noise, as well as high overall linearity. Although this circuit performs well, the overall bandwidth and power consumption are significantly higher than our goal, and the overall circuit is likely to be larger than our application would allow.

2.3.3 Switched-Capacitor TIA Designs

Since large resistors (several to tens of MΩ's) can consume large amounts of die area and can be inaccurate once fabricated, an alternative is to replace the resistor with a "switched capacitor." This can be useful in larger scale voltage amplifiers, as well as transimpedance amplifiers. Switched capacitor implementations are also referred to as charge integrating transimpedance amplifiers. Special considerations such as charge injection and switch noise minimization or cancellation must be taken into account when using switching circuits with high sensitivity current measurements.

Although switching can have undesirable effects in high sensitivity transimpedance amplifiers, it can be used to the designer's advantage, providing a means to effectively cancel undesired 1/f noise and amplifier offset through correlated double sampling. One such design uses a slow integrator, integrating the input current onto a capacitor and sampling the output voltage periodically [23]. Integrator designs eliminate the need for a large capacitor, and allow for low noise performance. This type of design has achieved spot noise specifications as low as 25fA/√Hz.

A reduced noise floor is one of the main advantages of low-speed switched integrator designs. Allowing the signal to integrate over an extended period of time produces a reduction in switching noise and charge injection, leading to the potential for a lower overall input inferred noise current.

2.4 Basic Transimpedance Amplifier Operation

A basic transimpedance amplifier constructed with an operational amplifier, a resistor, and a feedback capacitor, is shown in Figure 2-2. If a transimpedance amplifier has gain R, the ideal output voltage can be calculated as written in Equation 2.1.

$$V_{out} = I_{in} * R \tag{2.1}$$

While this design itself is simple, several practical issues arise in implementation. The resistor size, R, is a direct function of transimpedance gain. With high transimpedance gain, the size of the resistor quickly approaches the limits of on-die components. Furthermore, the absolute accuracy of on-die resistor values is not well controlled in modern CMOS process. In the resistor-based topology, the zero created by the input capacitance and feedback resistor may need to be cancelled with a feedback capacitor for overall stability.

In a biosensor system, the parasitic capacitance level can vary from one electrode to the next, and change depending on the medium in which the electrodes are placed, making this a difficult design problem in large electrode arrays.

2.5 Noise Sources in Transimpedance Amplifiers

In a traditional resistive transimpedance amplifier, the resistor has an inherent level of thermal noise. Depending on the desired transimpedance gain and input signal magnitude, it is possible that the input referred noise due to thermal noise can limit the smallest detectable input signal.

In the transimpedance amplifier topology shown in Figure 2-2, if we assume a 10MΩ linear feedback resistor is used, and the circuit is at room temperature, the noise current can be calculated as shown in Equation 2.2.

$$i_n = \sqrt{\frac{4kT}{R}} = 40.69fA/\sqrt{Hz} \quad (2.2)$$

This noise floor doesn't consider the additional noise generated in the OTA, but rather the just the noise in the feedback network itself. Care must be taken to ensure that the noise floor is kept below the inherent noise level of the electrode, to minimize the smallest detectable current level.

In switched capacitor integrator circuits, kT/C noise and charge injection become the primary noise sources. Methods of reducing charge injection including bottom-plate sampling and dummy switches were tested and implemented, and results are discussed throughout Chapter 4.

Chapter 3 Inverter-Based Operational Amplifier Design

3.1 Introduction

Operational amplifiers are basic building blocks used in many signal processing circuit designs. Nearly all types of analog circuits including continuous and discrete time amplifiers, analog to digital converters, sense amplifiers, as well as many other types of circuits use operational amplifiers as their basic building blocks. These and various other circuit designs are used in many tasks, including the amplification of small signals, as well as various types of mixed-domain processing for complex audio and video signals [24].

For a complex system such as an integrated biosensor, each signal processing channel can contain anywhere from several to tens of operational amplifiers. In a multiple-channel system, the overall number of operational amplifiers is further multiplied by the number of channels, resulting in rapidly growing silicon area and power consumption. This large number of instances of operational amplifiers increases the need for a low-power design with a small silicon footprint that can still maintain a high gain and meet bandwidth requirements for discrete time applications.

3.1.1 Challenges in Reducing Amplifier Size and Power

Traditional operational amplifier designs most commonly use transistors in the saturation region, which generally requires at least one DC bias current. As technology size has decreased, low power, high gain amplifier design has become more challenging for designers. Since

transistor threshold voltage generally doesn't decrease as fast as feature size and power supply voltage, many cascaded or folded designs are not possible with reduced voltage supply. Given that the reduction in headroom reduces the ability to cascode devices, low voltage high-gain amplifiers are commonly built by expanding outward, using two or even three cascaded amplification stages. These multi-stage cascaded designs require the designer to take extra measures to ensure amplifier stability, and, depending on the topology, can be very challenging or complex to stabilize. Most stabilization schemes require additional compensation capacitors and/or nulling resistors, which use additional silicon area, and can decrease circuit bandwidth; however, these compensation schemes have been improving with the usage of active compensation networks [25] [26] [27].

Reduced power supply voltage and the increasing demand for low power consumption make sub-threshold operation and design a more viable alternative when a reduction in bandwidth is acceptable. Operation in the sub-threshold region causes the drain current to increase exponentially with V_{GS} as opposed to quadratically in the saturation region [28]. The disadvantage with sub-threshold operation is the reduction in amplifier driving current, and the loss of ability to quickly drive large capacitive loads.

3.2 Operational Amplifier Topology

Previous works on achieving high gain with minimal DC biasing [29] [30] [31] [32] replace traditional input transistors with CMOS inverters in a differential topology, as shown in Figure 3-1.

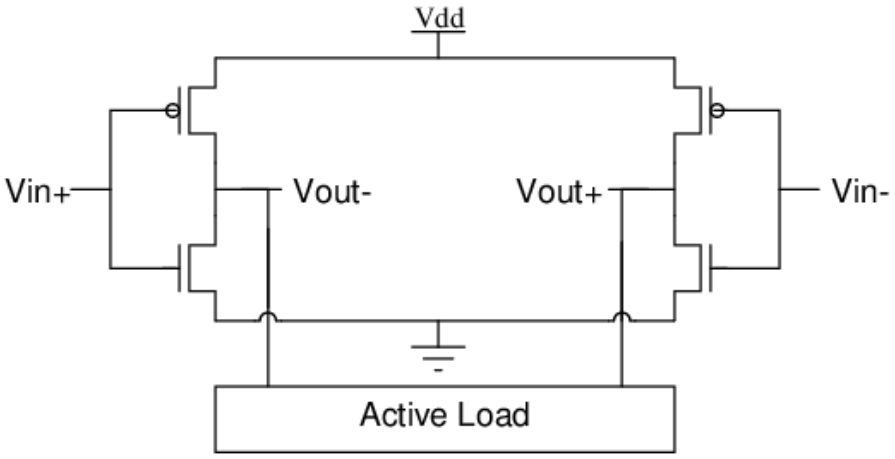

Figure 3-1: Inverter based op-amp proposed in [30] and [31]

This amplifier topology has several advantages over a traditional differential pair. One advantage is the increased transconductance of the input stage. In the inverter configuration, the input stage now has a final transconductance equivalent to the sum of the n-type and p-type transistors, as written in Equation 3.1.

$$G_m = G_{m_n} + G_{m_p} \tag{3.1}$$

Assuming the transconductance of the two input transistors is balanced, the combination of the two transconductances should provide a 6dB increase in gain when compared to a traditional common source amplification stage. It should also use approximately the same DC bias current.

When implemented using a standard supply voltage ($>2v_t$), the overall transconductance can be increased significantly depending on inverter sizing and resulting drain current through the inverters. With a high current, a significantly high output bandwidth can be achieved. This topology also has an increase in output swing and linearity when compared with a traditional common source amplifier, assuming the p-type and n-type transconductances are appropriately balanced.

Inverter-based operational amplifiers can provide a lower equivalent noise resistance compared to an equivalent common source topology. Assuming a balance between the n and p type transistors, and equivalent noise resistances of R_n and R_p respectively, the equivalent noise resistance is defined in Equation 3.2.

$$R_N = \frac{G_{mn}^2 R_{Nn} + G_{mp}^2 R_{Np}}{\left(G_{mn} + G_{mp}\right)^2} \tag{3.2}$$

One drawback to the inverter-based topology is its limited common mode rejection ratio when used in a differential configuration as shown in Figure 3-1. This issue is addressed in the proposed amplifier design section.

3.3 Proposed Differential Amplifier Design

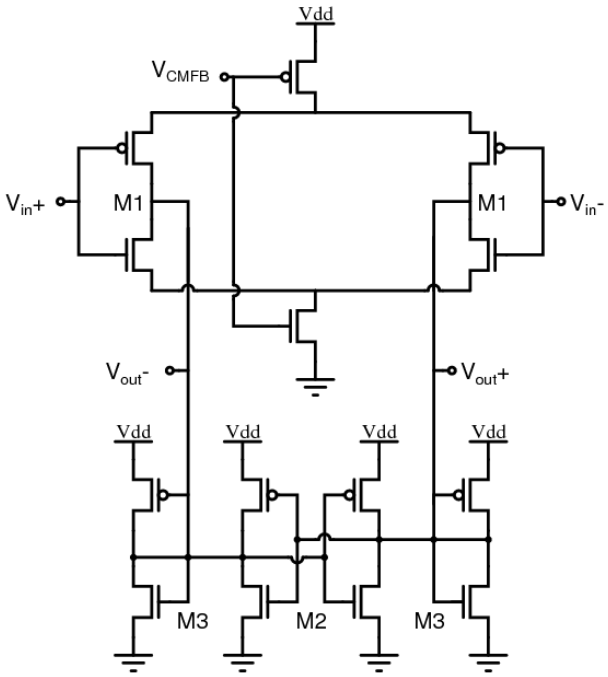

Figure 3-2: Proposed Inverter-Based Op-Amp Topology

3.3.1 Sub-Threshold Operation and Current Starving Tails

The schematic for the proposed design is shown in Figure 3-2. When implemented with a low supply voltage ($V_{supply} < 2v_t$), the inverter transistors operate in the sub-threshold region. This mode of operation greatly reduces bias current and therefore overall power consumption, but reduces amplifier bandwidth and output drive strength.

The addition of the tail current source transistors allows for further reduction of the overall bias current. This reduction in bias current further reduces power consumption, and also provides the benefits of an increased CMRR as well as an additional input terminal which can be used to add common mode feedback to the circuit. In addition, the use of tail current sources help separate the competing requirements for both low power and low offset; low offset can be achieved with an increase in inverter size, and overall power consumption can still be reduced with a change in tail transistor sizing [33].

3.3.2 Active Load Utilizing Positive Feedback

The proposed topology shown in Figure 3-2 employs an active load that consists of four additional load inverters (M2, M3). The innermost pair of inverters is connected in a cross-coupled configuration, and the outer pair of inverters is diode-connected. The schematic for these inverters is shown in Figure 3-3.

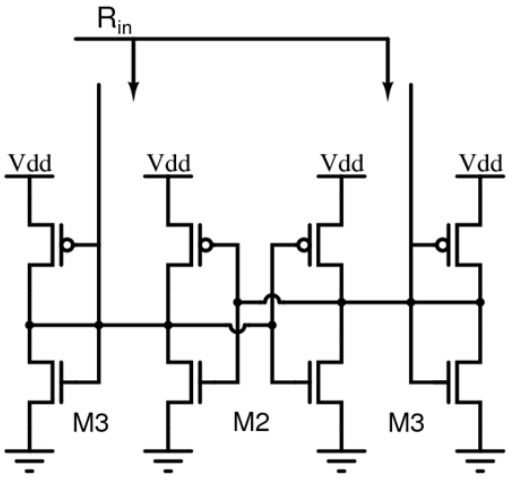

Figure 3-3: Active Load Inverter Configuration

With a common source amplifier, large load impedance can be advantageous when trying to increase the gain. Using the schematic shown in Figure 3-4, the impedance of the overall load can be calculated as shown in Equation 3.3.

$$R_o = (R_{cross} // R_{diode}) \tag{3.3}$$

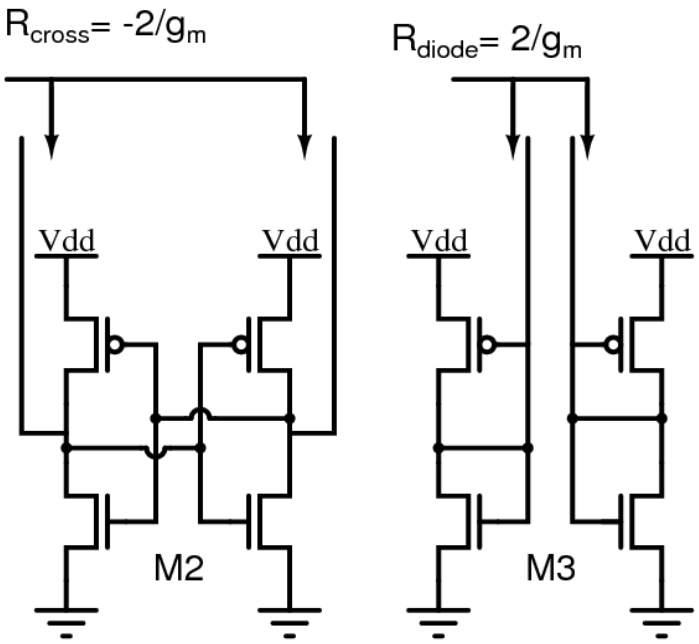

Figure 3-4: Cross Coupled and Diode Connected Load Circuit Halves

Assuming inverters M2 and M3 have transconductances g_{m_2} and g_{m_3}, the overall load resistance can be calculated as

$$R_o = \frac{1}{g_{m_2} - g_{m_3}} \tag{3.4}$$

Assuming the load transistors are balanced, as the inverter pairs become more closely matched, the denominator of Equation 3.4 approaches zero, making the theoretical overall resistance infinitely high. While perfect matching and infinite impedance are not physically possible, well-matched devices and positive feedback can be used to help further increase the overall gain of the amplifier without increasing overall power consumption.

3.3.3 Overall Amplifier Operation and Sizing Methodology

The positive portion of the resistance provided by the diode connected inverters helps stabilize the inherently unstable negative impedance of the cross-coupling, as well as provide additional DC bias stability for both the input and cross-coupled inverter pairs.

The overall voltage gain of the amplifier's half-circuit can then be defined as

$$A_{v_o} = \frac{g_{m_1}}{g_{m_2} - g_{m_3}} \tag{3.5}$$

When sizing the transistors in this design, it is desirable for the input and tail transistors to have reasonably large lengths (typically >1μm) and large W/L ratios (typically >16) to improve output impedance, and to have an increased transconductance. Large lengths, especially in the cross-coupled inverters help alleviate the effects of PVT. Large lengths and W/L ratios also help decrease the amplifier's voltage offset.

During the design of this amplifier, OCEAN scripting was used to find balanced inverter sizes, or inverters sized such that the transconductances ($g_{m_p}$and g_{m_n}) were balanced, and the output of the inverter was half the supply voltage when the input was set to half the supply voltage. Valid inverter sizes were then used by an additional script, to build and simulate combinations of inverters, maximizing the overall figure of merit at different supply voltages. These scripts can be found in Appendix B: Matlab Code for Data Acquisition.

3.4 Proposed Amplifier Figure of Merit

A figure of merit commonly used to compare amplifier performance is shown in Equation 3.6

$$FOM_1 = \frac{GBW(MHz) \times C_L(pF)}{I(mA)} \quad (3.6)$$

The figure of merit shown in Equation 3.6 focuses primarily on return-on-driving current. This figure of merit doesn't directly measure the impact of supply voltage scaling. This means that this figure of merit is accurate and useful for comparing circuits operating on the same supply voltage. Otherwise, this figure of merit tends to penalize circuit designs that operate on lower supply voltages.

To consider the impact of supply voltage scaling in comparisons, a power-based figure of merit is proposed in Equation 3.7**Error! Reference source not found.**.

$$FOM_2 = \frac{GBW(MHz) \times C_L(pF)}{P(mW)} \quad (3.7)$$

The second figure of merit uses overall power consumption in the place of current consumption. This allows the figure of merit to consider the reduction in power achieved by supply scaling, as well as the return-on-driving current and overall driving strength of the circuit.

3.5 Amplifier Simulation Results

Circuit designs were optimized for three different supply voltages of 0.7V, 0.9V, and 1.1V. Varying the supply voltage allows the circuit to operate at varying levels of sub-threshold regions with different driving strengths and power consumptions. With a focus on low-power bioelectronics applications, the design goal is to achieve maximum power efficiency possible, while still maintaining the performance necessary to drive lower-capacitance internal circuit nodes at the required bandwidth. Table 3-1 shows simulation results of the three different amplifier versions at their optimal supply voltages.

Table 3-1: Inverter Amplifier Simulation Results

Designed Supply Voltage	700mV	900mV	1.1V
DC Gain	46.22dB	48.36dB	47.9dB
Load	1.8pF	6pF	15pF
GBW	463.9kHz	2.408MHz	3.94MHz
Overall DC Current	207.6nA	4.157µA	20.56µA
Power Consumption	145.32nW	3.741µW	22.616µW
Offset Voltage	2.273mV	2.167mV	2.443mV
Input Referred Noise	25.524µV	6.428µV	3.5µV
CMRR	124.397dB	153.055dB	177.897dB
FOM_1	4022	3475	2874
FOM_2	5746	3861	2612

It can be seen that the overall figure of merit seems to be inversely proportional to the circuit's supply voltage. The results in Table 3-1 show the broad range of specifications that can be covered by low-power inverter based amplifiers. This flexible topology allows the designer to precisely control the power consumption without sacrificing output impedance and gain.

If an application requires a higher amplifier bandwidth, the width of the tails can be increased, increasing the overall transconductance and bandwidth, at the sacrifice of overall power consumption and a decreased figure of merit. An increased power supply voltage can cause the circuit to operate less deep in the sub-threshold region, or even in the saturation region, which will greatly increase the overall bandwidth of the circuit.

3.5.1 Amplifier Design Comparisons

We would like to compare the proposed design in the context of a wide range of existing designs from simple common source amplifiers, to telescopic amplifiers, to traditional Miller compensated amplifiers, and to the more advanced three-stage amplifiers. Simple or folded cascode operational amplifier designs typically can achieve a FOM of 200-300 [24] [34]; telescopic amplifiers typically have a higher FOM around 500-700; traditional Miller compensated two-stage amplifiers achieve a FOM of around 1000. State-of-the-art three-stage Miller compensated amplifiers can achieve a FOM in the 3000-5000 range, and even over 10,000 [35] [36]. As stated previously, these larger three stage Miller amplifiers require complex stabilization and compensation schemes, and can be significantly large on silicon.

Table 3-2 shows the comparison of the amplifiers in this work to various types of operational amplifiers. The table includes all parameters necessary for figure of merit calculation, as well as both the power and current based figures of merit.

Many of the existing amplifier topologies listed in Table 3-2 consist of multiple stages, and employ complex stabilization schemes. These amplifiers are generally designed to have a high bandwidth and drive very large capacitive loads. Due to the nature of current-starved circuitry, the inverter-based amplifiers are more suitable for smaller loads and less stringent settling time requirements. Therefore, low power bio-applications will be able to take the full advantage of the power saving properties of this design. Despite the lower drive strength and the lower FOM associated with the inverter based design at 1.1V supply voltage, its FOM still surpasses some of the more complex designs.

Table 3-2: Amplifier Design Comparison

Existing Designs	Amplifier Type	Process	C_L (pF)	GBW (MHz)	Power ($\mu W@V_{DD}$)	FOM_1	FOM_2
TSEFC [37]	3-Stage Miller Comp.	0.35µm	500	1.4	225@1.5	4666.5	3111
SMCFC [35]	3-Stage Miller Comp.	0.35µm	150	1.6	21@1.5	17143	11430
MNMC [27]	Multipath Nested Miller Comp.	bipolar	100	100	76000@8	1056	132
NGCC [38]	Multistage Nested G_m-C Comp.	2µm	20	0.61	680@2	36	18
NMCFNR [39]	Nested Miller Comp.	0.8µm	100	1.8	406@2	886	443
DFCFC [40]	3-Stage w/Active Feedback Freq. Comp.	0.8µm	100	2.6	420@2	1238	619
AFFC [41]	3-Stage w/Active Feedback Freq. Comp.	0.6µm	100	5.5	250@1.5	330	220
DLPC [42]	Dual Path, Dual-Loop Parallel Comp.	0.6µm	120	7	330@1.5	3817.5	2545
$ACBC_F$ [43]	3-Stage AC Boosting Comp.	0.35µm	500	1.9	324@2	5864	2932
700mV supply Inverter-based	**Inverter-Based**	**0.18µm**	**1.8**	**0.4639**	**0.14532@0.7**	**4022**	**5746**
900mV supply Inverter-based	**Inverter-Based**	**0.18µm**	**6**	**2.408**	**3.741@0.9**	**3475**	**3861**
1.1V supply Inverter-based	**Inverter-Based**	**0.18µm**	**15**	**3.94**	**22.616@1.1**	**2874**	**2612**

Chapter 4 TIA Design for Biosensor Applications

4.1 Introduction

In an integrated biosensor application, it is desirable for all circuitry to have low power consumption, high gain, and sufficient bandwidth for amplifying biological signals. When dealing with electrochemical signals, the amplitude of currents induced on the working electrode can range from tens of nano-amperes to as small as several pico-amperes. This small input range designates requirements for both high gain and low noise.

4.2 Objectives

In our biosensor application, the Transimpedance amplifier serves as the pre-amplifier for the biosensor signal chain, as shown in Figure 1-4.

Table 4-1: Transimpedance Amplifier Design Goals

Specification	**Target**
Gain (Standalone)	As high as possible
Gain (Signal Chain)	6MΩ
Signal Bandwidth	1kHz
Available Clock Frequency	1MHz
Supply Voltage	900mV (Split rail +/- 450mV)
Input Referred Noise	Minimal
Power Consumption	Minimal
Silicon Area	Minimal

4.3 Supporting Circuitry

4.3.1 Clock Booster

With the use of an inverter-based operational amplifier, it is optimal for the input and output to have a DC bias point exactly halfway between the supply rails. In the case of an inverter based amplifier in a switched capacitor configuration using a 900mV power supply, the switches surrounding the amplifier have an inherent source/drain voltage of 450mV.

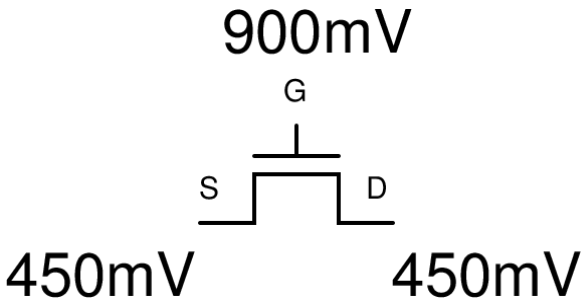

Figure 4-1: Example Switch Voltages

With the use of a standard 900mV peak-to-peak clock signal, V_{GS} on the switching transistor is only 450mV during the "on" phase. In a typical 0.18µm CMOS process, transistors have a threshold voltage (v_t) of approximately 500mV, meaning that the switch transistor doesn't have a large enough gate to source voltage (v_{gs}) to operate deep in the saturation region, or "fully" turn on. This means the switch has a large internal resistance, which can be detrimental to the performance of switched capacitor integrator circuits.

To allow the switches to operate deeper in the saturation region v_{gs} must be increased. To increase the gate voltage of the switch during the on phase, a bootstrapping circuit known as a clock booster [44] was used.

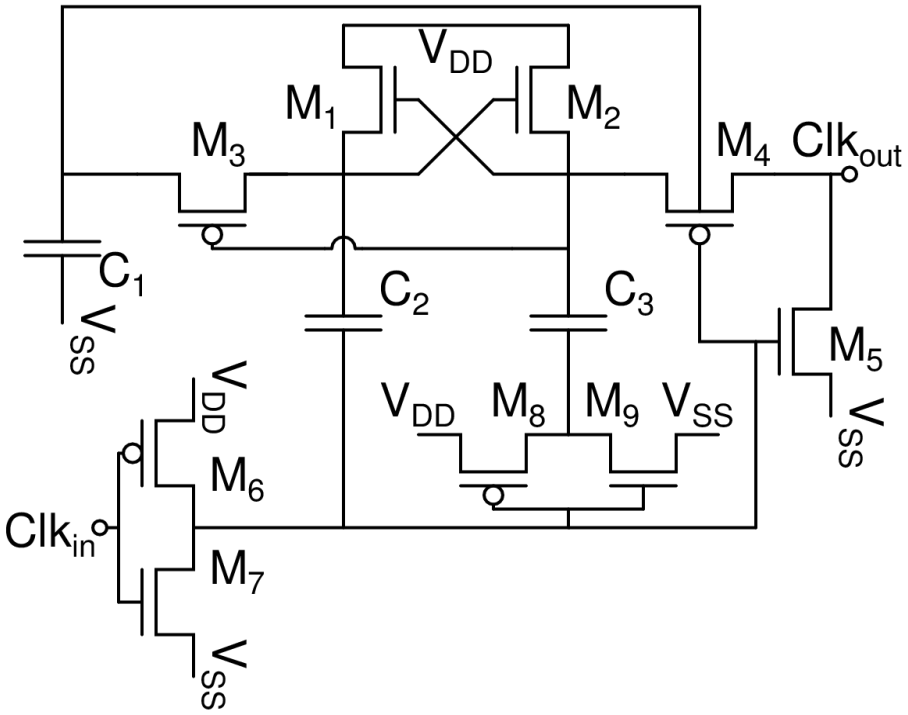

Figure 4-2: Clock Doubler Circuit

During normal operation, when Clk_{in} is low, Clk_{out} is also low (V_{ss}). When Clk_{in} is high, the charges accumulated on C_1, C_2, and C_3 during the previous phase are used to temporarily push Clk_{out} higher than V_{DD}, creating a much larger v_{gs} for the circuit's switches during the "on" phase. Simulation results for the clock booster with a 900mV supply are shown in Figure 4-3.

Extra care must be taken when sizing the capacitors in this design. If the load driven by the clock booster is to large relative to the capacitors in the circuit, the boosted clock voltage won't reach the intended potential, since the charge accumulated on the capacitors is finite. The capacitors were sized very liberally, to ensure that the clock booster would function with parasitic routing capacitances and a large number of gates attached.

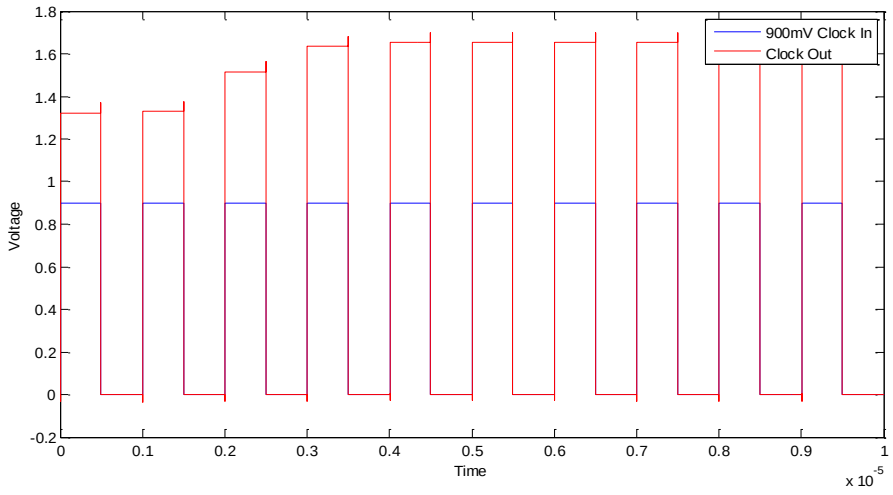

Figure 4-3: Clock Booster Operation

This increase in gate voltage greatly improves the performance of switched transimpedance amplifier circuits, due to the significantly decreased switch resistance. This circuit was used in all switched transimpedance amplifier designs that utilized inverter-based amplifier designs. The layout for the clock booster circuit measures approximately $29\mu m \times 42\mu m$. The layout is shown in Figure 4-4, with device sizes listed in Table 4-2.

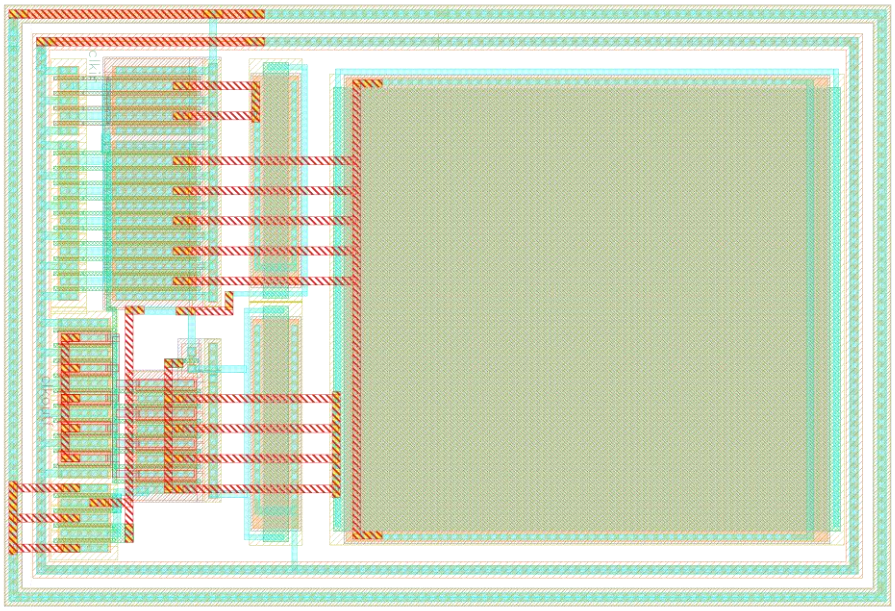

Figure 4-4: Clock Booster Layout

Table 4-2: Clock Booster Transistor Sizing

Device	Type	Width	Length
M1/M2	NMOS	5µm	0.18µm
M2	NMOS	5µm	0.18µm
M3	PMOS	0.22µm	0.18µm
M4	PMOS	19.985µm	0.18µm
M5	NMOS	25µm	0.18µm
M6	PMOS	16µm	0.18µm
M7	NMOS	4µm	0.18µm
M8	PMOS	40µm	0.18µm
M9	NMOS	10µm	0.18µm
C1	100fF	10µm	1.22µm
C2	100fF	10µm	1.22µm
C3	4pF	23µm	21.21µm

4.3.2 Single-to-Differential Current Mirror

In the biosensor signal chain shown in Figure 1-4, the transimpedance amplifier resides between the electrode and main amplifier. The main amplifier requires a differential input voltage signal, and the electrode provides a single-ended current to the TIA. This means that a single-to-differential conversion must be implemented either before or after the transimpedance amplifier.

Since noise is a primary concern, and differential circuitry can be used to reduce the effects of common mode noise sources, the TIA was designed in a differential configuration, requiring a conversion of the input current from single-ended to differential. This conversion was done using a combination of high-impedance current mirrors, in the topology shown in Figure 4-5. A variation of this circuit was used in each of the differential TIA designs, with minor adjustments from one revision to the next.

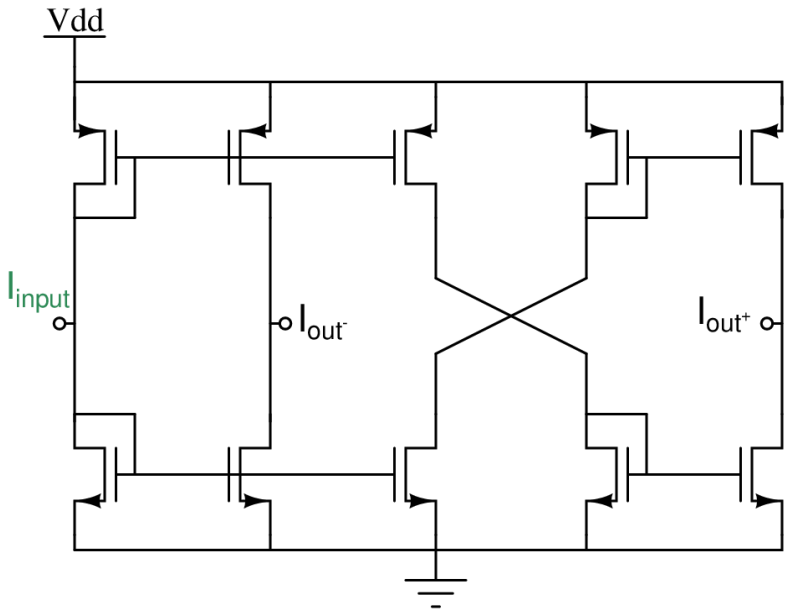

Figure 4-5: Single-Ended to Differential Current Mirror

Ideally, the current mirror would have two outputs, one with a current gain of 1, and the second with a current gain of -1. Simulation results showing ideal current mirror behavior is shown in Figure 4-6.

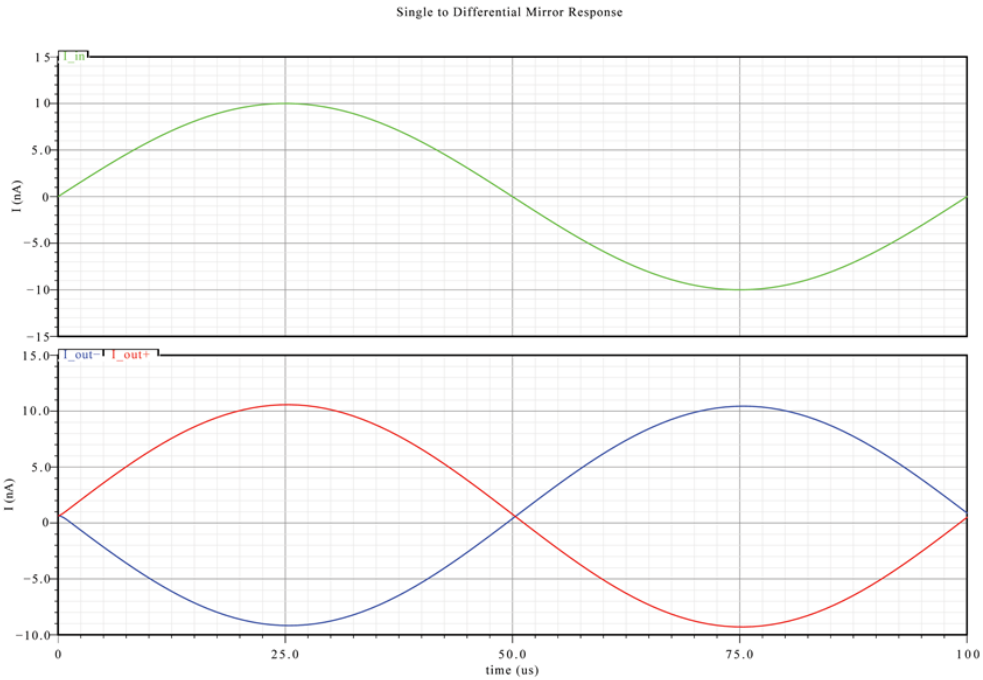

Figure 4-6: Simulated Current Mirror Response

Due to the highly-variable nature of high-impedance nodes, this circuit was highly susceptible to problems caused by process variation. While the magnitude of the response to a small-signal input would remain appropriate, it was likely that the mirror would introduce DC shifts in the differential output currents, which would impose an artificial and problematic DC shift on the output of the differential transimpedance amplifier. A slight shift is apparent on the response in Figure 4-6.

These issues were addressed in later iterations of the current mirror and TIA, with an increase in device sizing, and the introduction of self-cascoding to help reduce output drift due to process variation. Ultimately it was decided that the main amplifier could be used to complete the single-ended to differential conversion, by simply attaching a constant DC bias to one of the amplifier's two input voltage terminals. This also removed the variation in the current mirror as an additional source of error.

4.4 Transimpedance Amplifier Designs

4.4.1 Differential Resistor-Based TIA

As a reference for measurements and as a proof-of-concept, a continuous time, purely resistive transimpedance amplifier was included in the revision G tape-out. This design utilized the differential inverter amplifier from the correlated double sampling design presented in section 4.4.5.

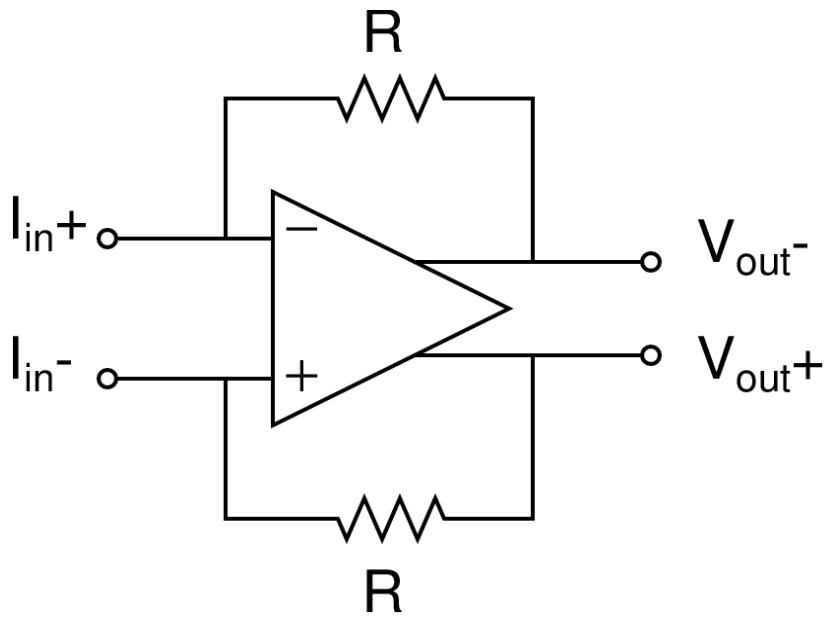

Figure 4-7: Differential Resistive TIA Schematic

The design used two thin film resistors, each with a final value of 2.785MΩ. Each resistor had an overall area of about 40µm x 36µm. Since the circuit was fully differential, an existing common-mode feedback circuit was added to help stabilize the circuit's DC operating voltages. The complete circuit with amplifier and a common-mode feedback circuit occupied an overall area of 110µm x 90µm. The overall layout is shown in Figure 4-8.

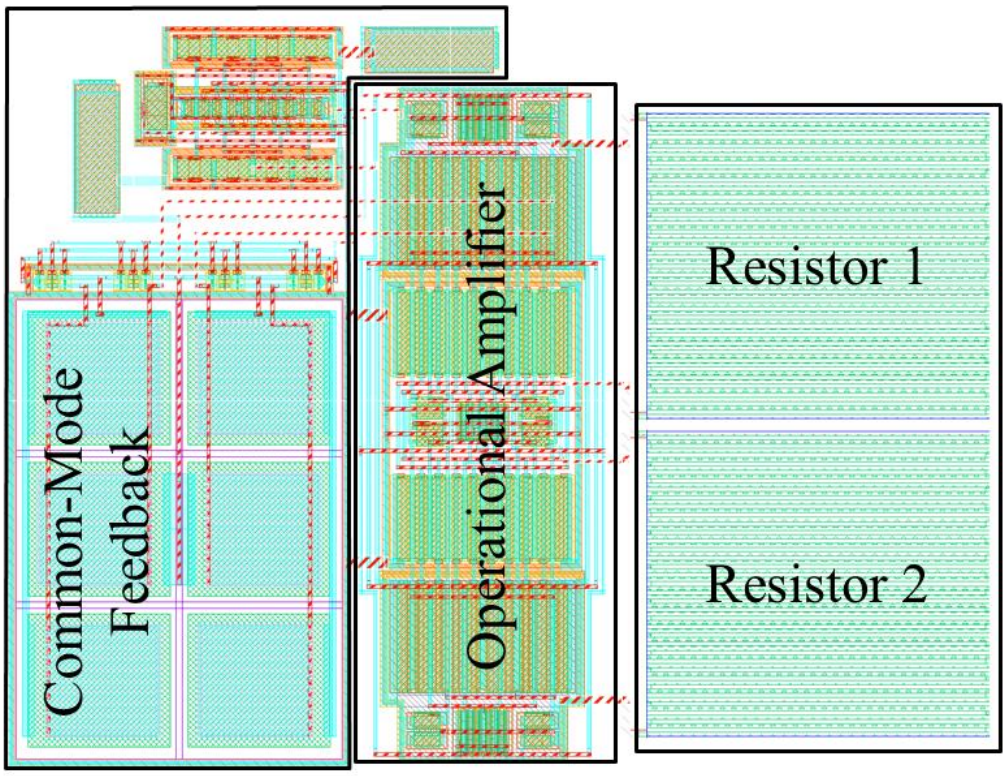

Figure 4-8: Differential Resistive TIA Layout

There are many issues commonly associated with on-chip resistors, the most significant issues being absolute inaccuracy and large size. A statistical analysis showed a 3-sigma variation in overall gain of the circuit of about ± 33%. National Semiconductor's 0.18µm process allows the use of thin film resistors, which are significantly smaller and more linear than other types of on-silicon resistors. Additionally, as discussed in Section 2.5, the thermal noise from on-chip resistors may also pose a challenge when designing low-noise circuitry.

4.4.2 Single-Ended Switched Capacitor TIA

The original design of the transimpedance amplifier was a basic switched capacitor integrator. The schematic of the initial design is shown in Figure 4-9. The design uses a differential non-overlapping clock, and was designed to run at a clock frequency of 1MHz.

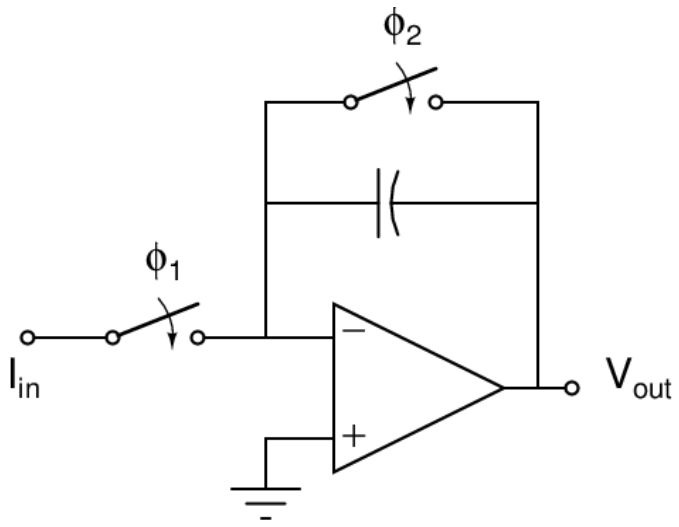

Figure 4-9: Single-Ended Switched Capacitor TIA Schematic

All switches were implemented using complementary CMOS transmission gates. The transistor level schematic and device sizing are shown in Figure 4-10 and Table 4-3 respectively.

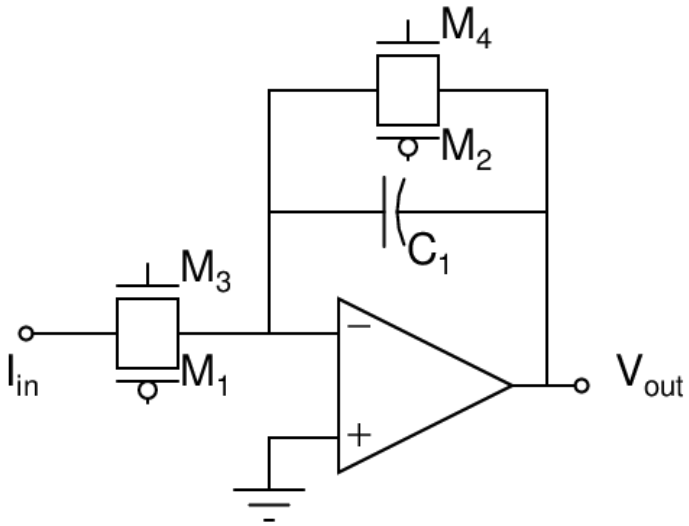

Figure 4-10: Transistor Configuration

Table 4-3: Switched Capacitor Integrator Device Sizing

Device	Type	Width	Length
M1/M2	PMOS	270nm	180nm
M3/M4	NMOS	270nm	180nm
C1	3.5pF Poly-Poly	62.5µm	65.9µm

The ideal circuit was simulated, and circuit was laid out and simulated both with and without parasitic effects. The simulated response to a 100 kHz, 10nA sinusoidal input is shown in Figure 4-11.

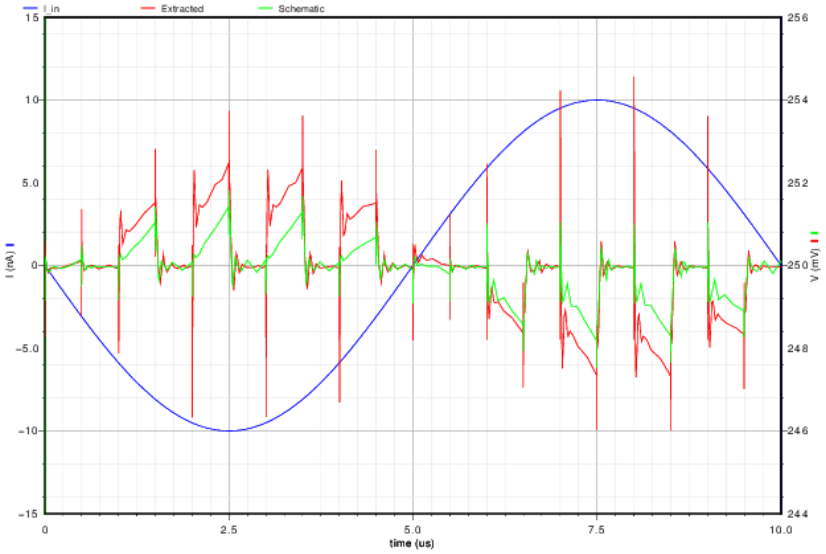

Figure 4-11: Single-Ended TIA Sine Wave Response

A noise simulation was also run on the extracted layout. The input referred noise current is shown in Figure 4-12.

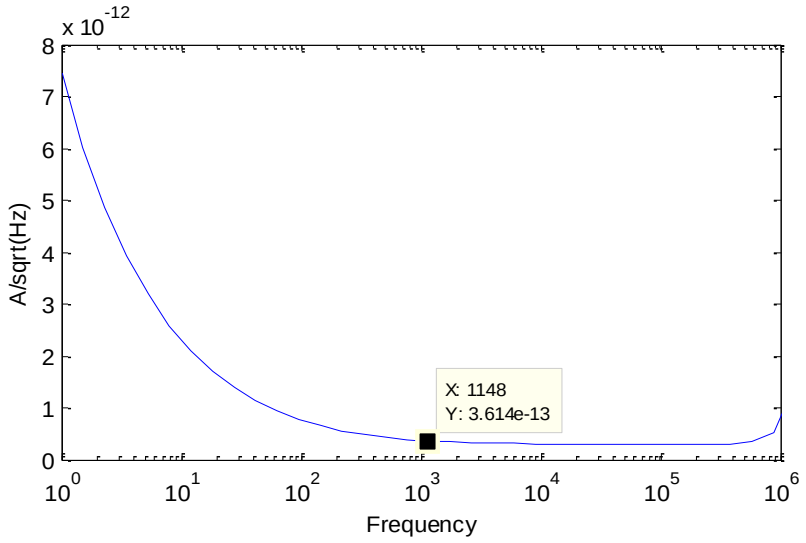

Figure 4-12: Input Referred Noise Current

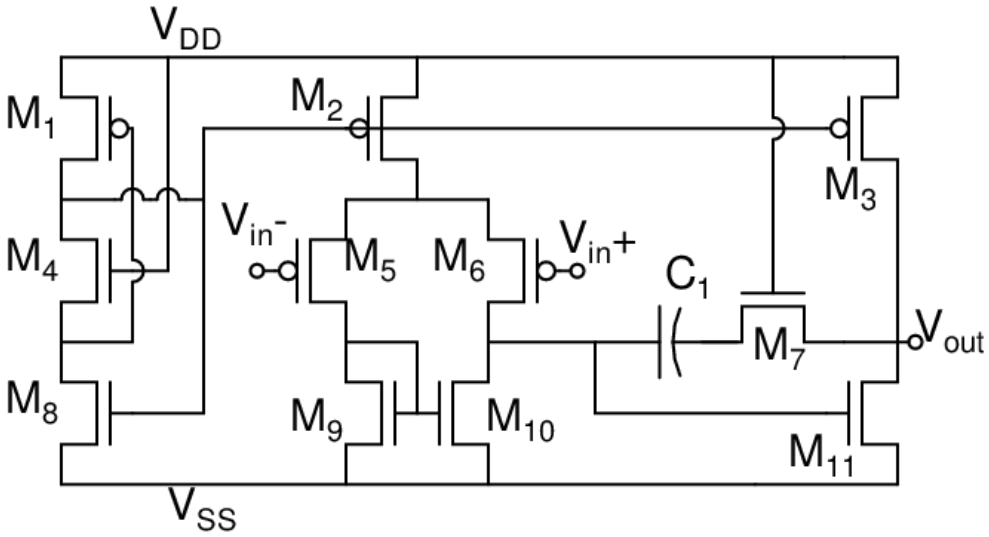

Figure 4-13: Switched Capacitor TIA Operational Amplifier Design

The operational amplifier used in the single ended switched-capacitor design was a differential pair staged followed by a single-ended common source output stage, as shown in Figure 4-13. Both the input and output were biased at 250mV above V_{ss}, or at an absolute voltage of -200mV. Performance specifications for the overall TIA design are shown in Table 4-4. Sizing for all transistors in Figure 4-13 are shown in

Table 4-5.

Table 4-4: Single Ended Switched-Capacitor TIA Performance Specifications

Overall Transimpedance Gain	300kΩ
Overall Signal Bandwidth	~2.2kHz
Opamp DC Gain	70.2dB
Opamp -3dB Bandwidth	10.4kHz
Opamp Unity Gain Freq.	27.43MHz
Opamp Phase Margin	52.2°
Average Power Consumption	32µW@0.9V

Table 4-5: Single-Ended Switched-Capacitor Op-amp Sizing

Device	**Type**	**Width**	**Length**
M1	PMOS	980nm	500nm
M2	PMOS	15.84µm	500nm
M3	PMOS	6µm	500nm
M4	NMOS	3.39µm	500nm
M5/M6	PMOS	62.44µm	2µm
M7	NMOS	1.01µm	500nm
M8	NMOS	700nm	500nm
M9/M10	NMOS	11.91µm	4µm
M11	NMOS	2.78µm	500nm
C1	1.5pF n-well	14.77µm	12.385µm

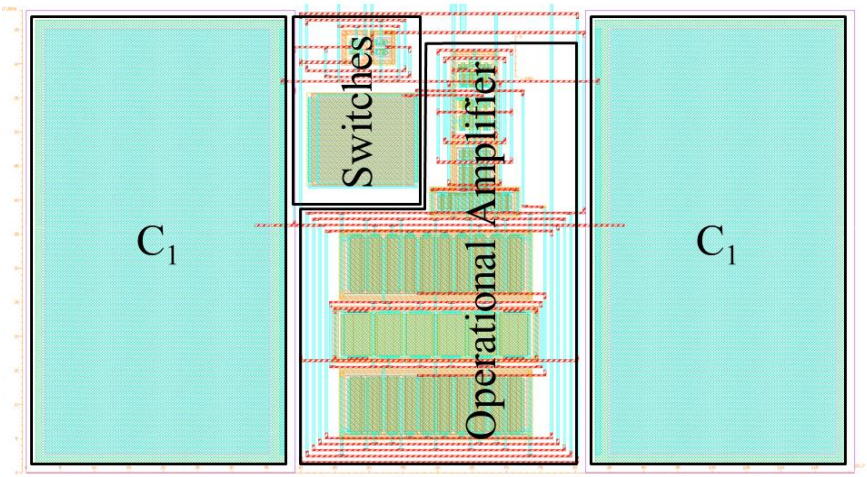

Figure 4-14: Single-Ended Switched-Capacitor TIA Layout

4.4.3 Pseudo-Differential TIA

The next revision of the TIA utilized two single-ended switched capacitor transimpedance amplifiers in a pseudo-differential configuration. The operational amplifier design, switch configuration, and switch sizing were identical to the previous TIA design. A schematic of the pseudo-differential TIA is shown in Figure 4-15.

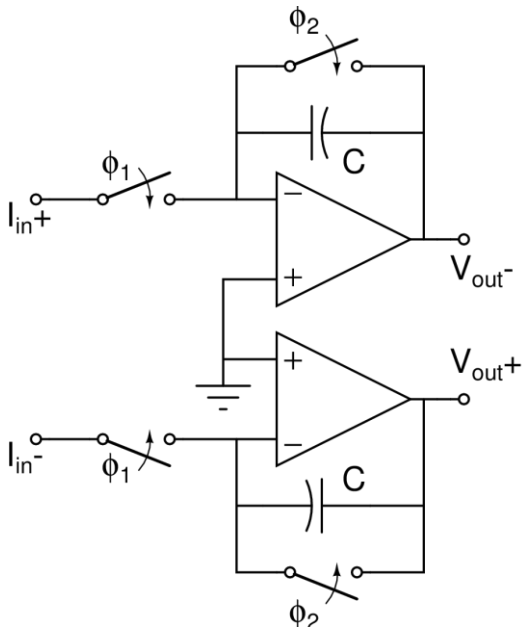

Figure 4-15: Pseudo-Differential TIA Schematic

This differential design was also the first design to utilize the current mirror discussed in section 4.3.2 to convert the single-ended input current to a differential current to ultimately produce a differential voltage output.

Table 4-6: Pseudo-Differential TIA Performance Specifications

Overall Transimpedance Gain	~500kΩ
Overall Signal Bandwidth	~2.2kHz
Opamp DC Gain	70.2dB
Opamp -3dB Bandwidth	10.4kHz
Opamp Unity Gain Freq.	27.43MHz
Opamp Phase Margin	52.2°
Average Power Consumption	64µW@0.9V

The differential transimpedance amplifier was extracted and simulated with a 10nA current input. The simulation result is shown in Figure 4-16.

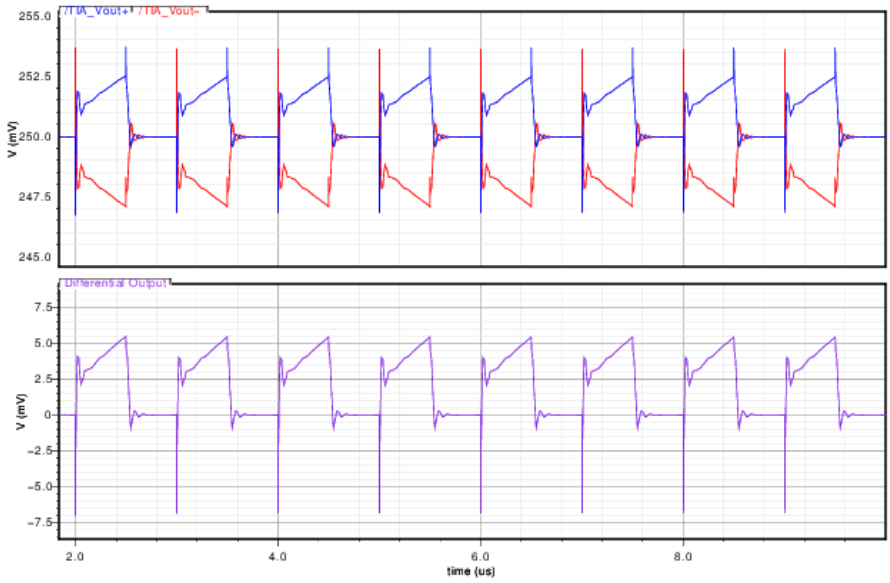

Figure 4-16: Pseudo-Differential TIA Response to a 10nA DC Input Current

It can be noted that the output signals from both the single ended and differential TIA have a large voltage jump at the beginning of the integration phase. It was hypothesized that this large voltage step was due to a combination of charge injection, and charge buildup on the input node during the non-sampling phase (while ϕ_1 is low). Both of these issues were addressed and are discussed in the next design.

The overall layout consisted of the input current mirror, the single-to-differential mirror, two single-ended switched capacitor TIA's, and two output voltage buffers. The layout of the overall circuit is shown in Figure 4-17.

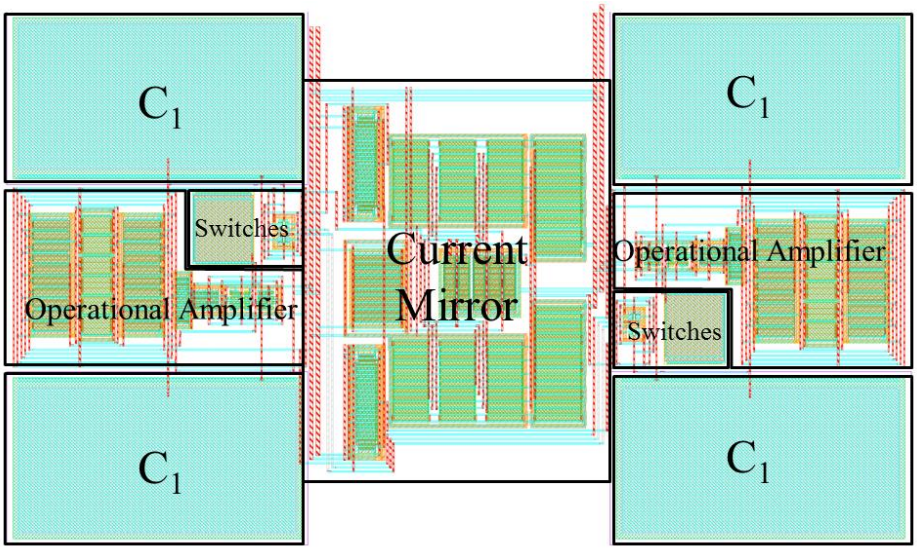

Figure 4-17: Pseudo-Differential TIA Layout with Current Mirror

4.4.4 Fully Differential TIA with Bottom Plate Sampling

When a CMOS transistor is turned on, a channel of minority carriers is formed below the gate. If the device is then turned off, the charge currently in the channel is pushed out through the source and drain terminals of the device. This movement of charges is known as charge injection. Charge injection can have detrimental effects on the performance of sensitive switched capacitor circuits.

Bottom plate sampling is a technique used to reduce the effects of charge injection in switched capacitor circuits. The concept behind bottom plate sampling is to integrate a current onto the sampling capacitor (C_1), and then disconnect the bottom plate of the capacitor from the common mode voltage before the integrating switch is opened. This prevents the charge on the capacitor from changing, since there is no longer a resistive path from the capacitor's bottom plate to ground which would allow charge to flow.

Using a two-phase non-overlapping clock with an added set of delayed phases allows us to manipulate the switch timing in order to accomplish this. An example of this clock configuration is shown in Figure 4-18.

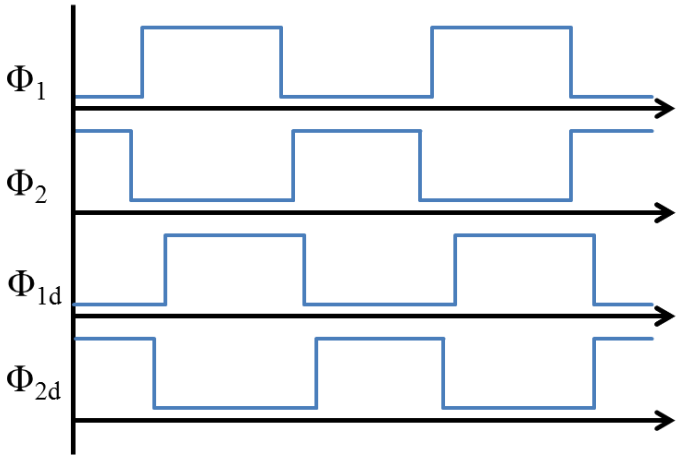

Figure 4-18: Two-Phase Non-Overlapping Clock with Delayed Phases

This circuit uses the ϕ_2 clock phase to disconnect the sampling capacitor's bottom plate from the common mode reference voltage just before the sampling input is disconnected by ϕ_{2d}. This ensures that the charge from the input switch cannot be injected onto C_1, since the opposite plate of the capacitor is floating and cannot balance the charge on the opposing (bottom) plate. The switch configuration for bottom plate sampling is shown in Figure 4-19.

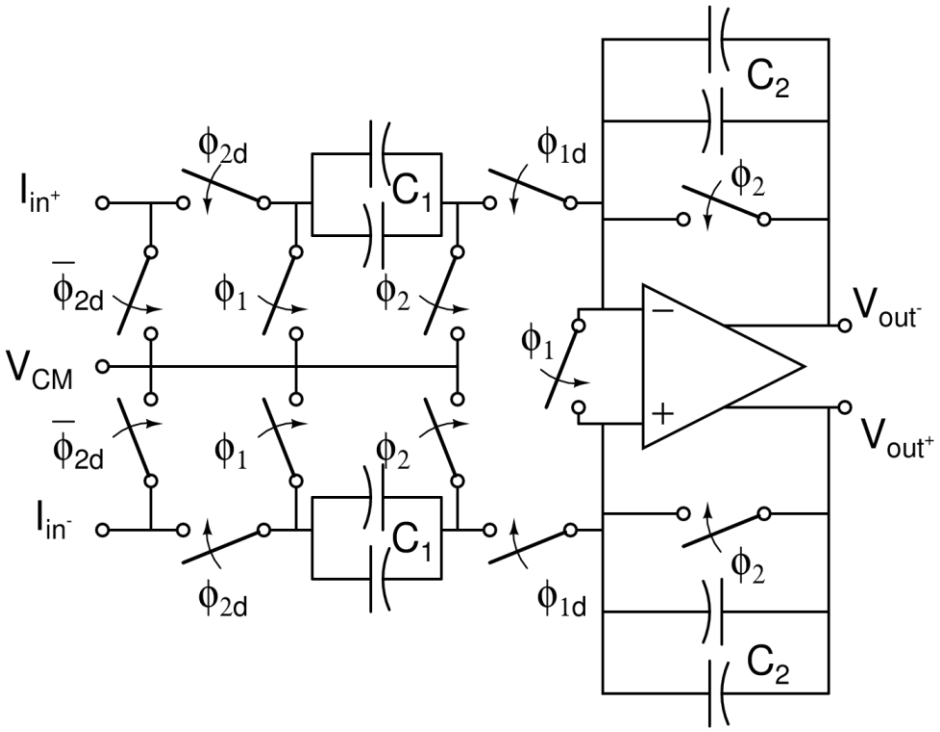

Figure 4-19: Fully Differential TIA Schematic with Bottom Plate Sampling

The extracted layout of the fully differential TIA was simulated with a 1nA sinusoidal input with a frequency of 10 kHz. The results of this simulation are shown in Figure 4-20. A periodic-steady-state noise simulation was also run on the circuit, and the resulting input noise current is shown in Figure 4-21.

The use of bottom plate sampling seemed to reduce the effects of charge injection, but a small amount of voltage jump was still apparent. The issue with a DC difference between the

outputs during reset was addressed with the addition of a reset switch between the two input nodes, forcing the nodes to the same voltage during reset.

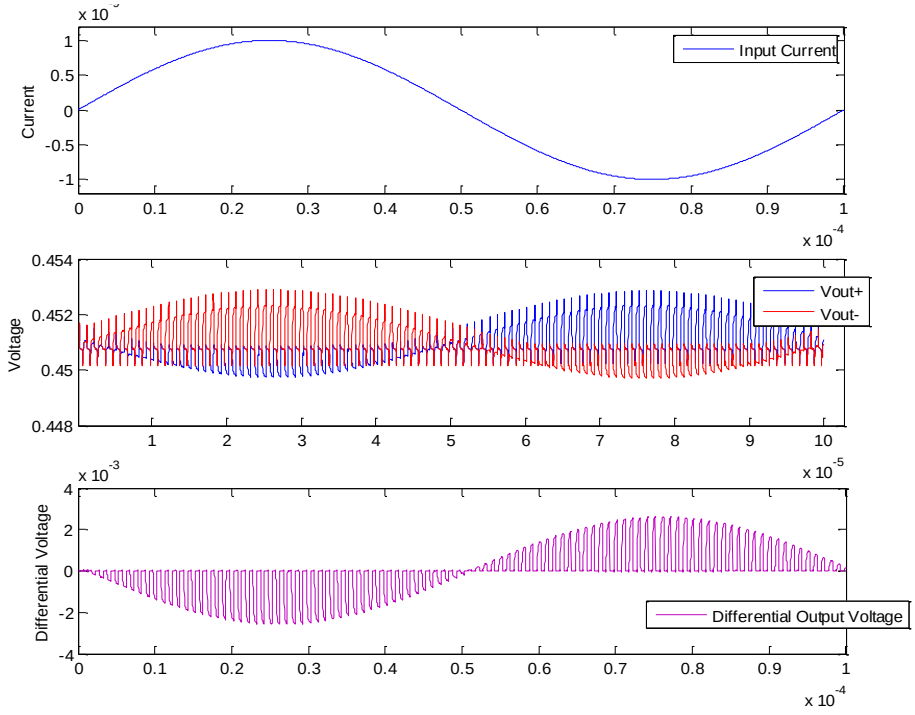

Figure 4-20: TIA Response to 1nA 10 kHz Input Current

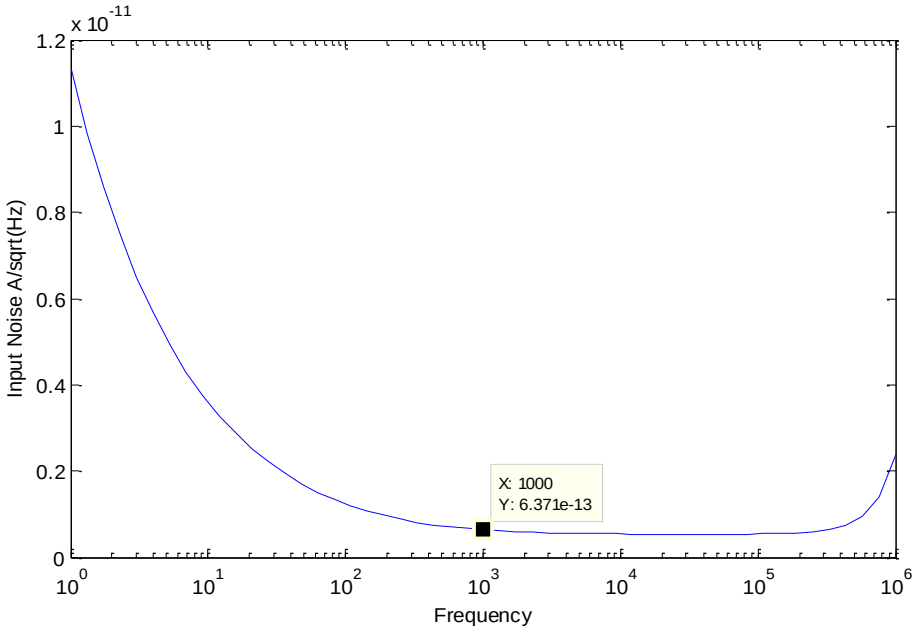

Figure 4-21: Differential TIA Input Referred Noise Current vs. Frequency

4.4.5 Correlated Double Sampling

Correlated double sampling is a technique commonly used to effectively reduce offset of an op-amp, increase the effective op-amp gain, and reduce flicker (1/f) noise in switched capacitor circuits. Because of these effects CDS can be used to achieve high performance specifications in applications where low noise and high precision are necessary.

The proposed topology, shown in Figure 4-22, is a slightly modified differential version of the schematic proposed in [45]. The proposed schematic includes an additional pair of switches on the input, which allow current to flow from the input to the common mode voltage node, to prevent the buildup of residual charge on the input node. This residual charge can cause a large current spike at the beginning of the integration phase, having effects similar to those of charge injection.

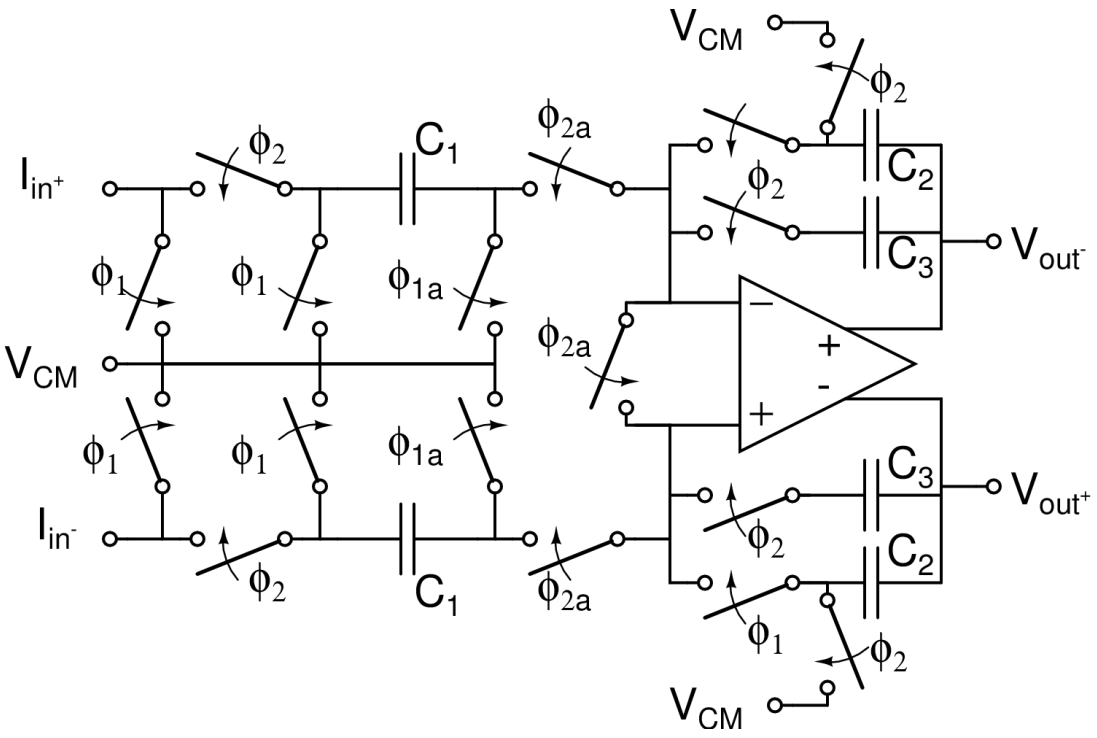

Figure 4-22: Differential TIA with Correlated Double Sampling

This design uses a set of two-phase non-overlapping clocks, as shown in Figure 4-23. The operation can be divided into 4 phases: 1. reset, 2. pre-charge, 3. integration, and 4. output-hold.

During phase 1, the charge on C_1 is set to 0 while C_2 holds the previous output and C_3 is disconnected. During phase 2, the offset voltage and 1/f noise of the OTA is stored on C_1. During phase 3, the input current is integrated onto C_1 along with the OTA offset and 1/f noise, cancelling the effects of offset and 1/f noise at the output. Finally, during phase 4, the voltage on C_2 is connected to the output.

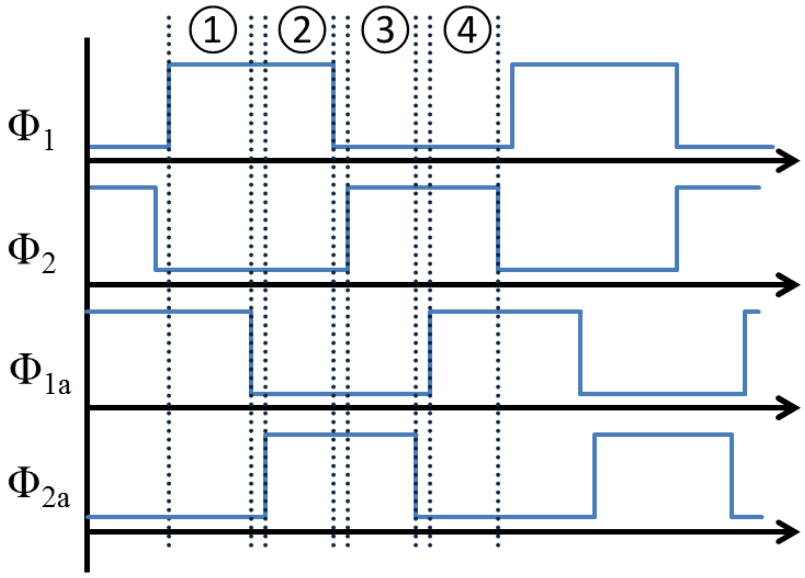

Figure 4-23: Correlated Double Sampling Clock Phases

This design utilized a fully differential OTA topology shown in Figure 4-24. The sizing for the OTA transistors is shown in Table 4-7.

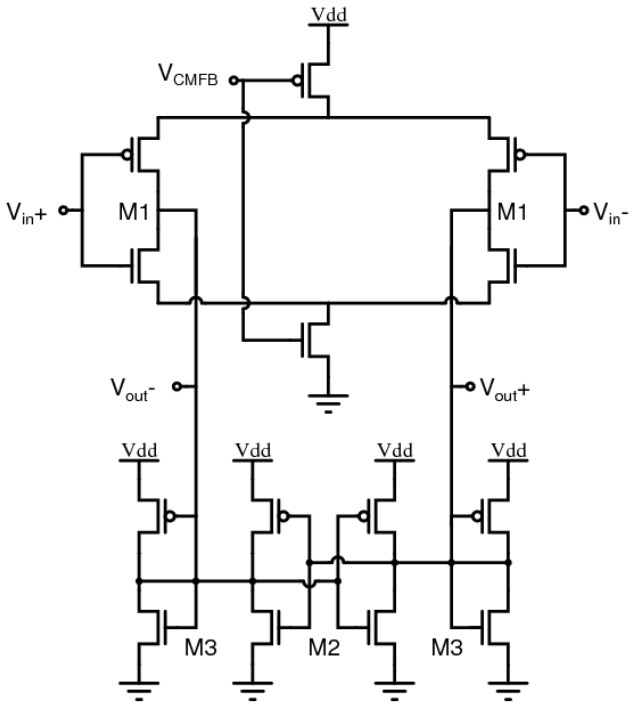

Figure 4-24: Correlated Double Sampling TIA OTA Topology

Table 4-7: Fully Differential Inverter OTA Device Sizing

Device	**Width**	**Length**
PMOS Tail	55.98µm	180nm
PMOS Input Pair	98.24µm	1.5µm
NMOS Input Pair	75.16µm	1.5µm
NMOS Tail	23.76µm	180nm
PMOS Load	2.3µm	3µm
NMOS Load	870nm	3µm

The correlated double sampling TIA was simulated with a 5nA 1 kHz sinusoidal input current. The individual output voltages and differential response are shown in Figure 4-25. A periodic-steady-state noise simulation was also run on the extracted circuit. The input referred noise current is shown in Figure 4-26.

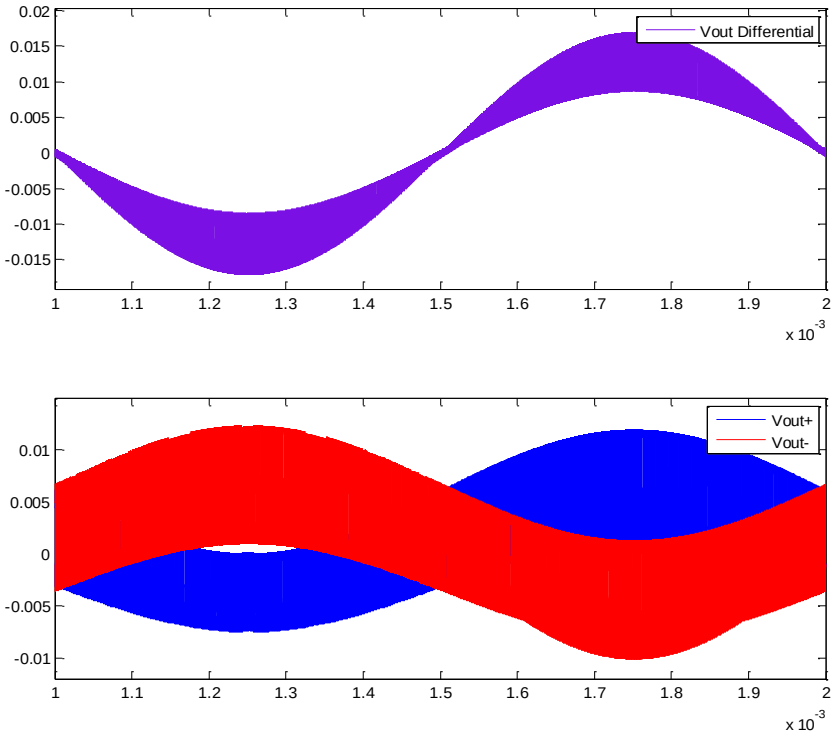

Figure 4-25: CDS TIA Simulated Response to a 1 kHz 5nA Sinusoidal Current Input

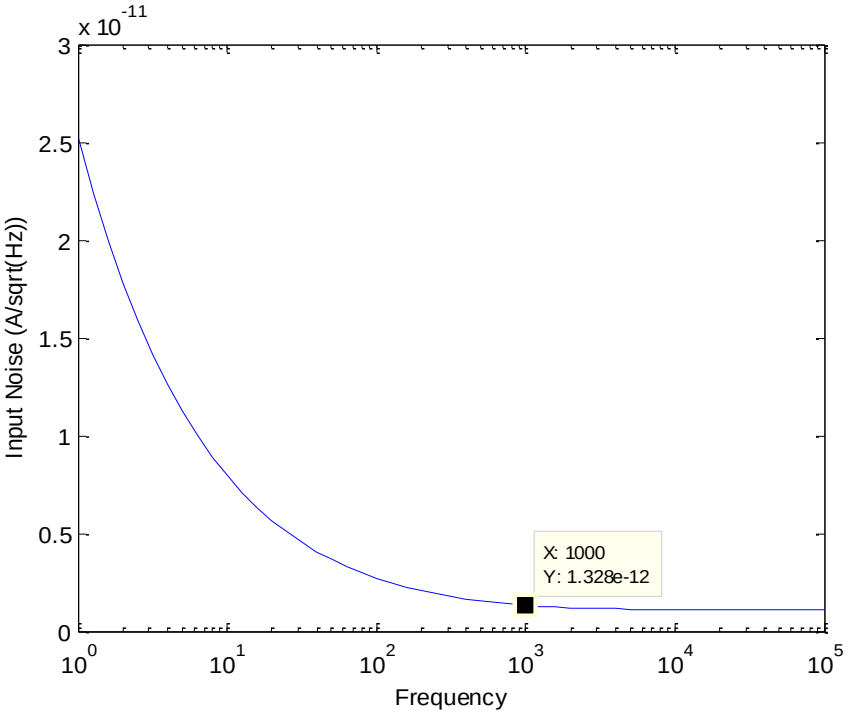

Figure 4-26: CDS TIA Input Noise vs. Frequency

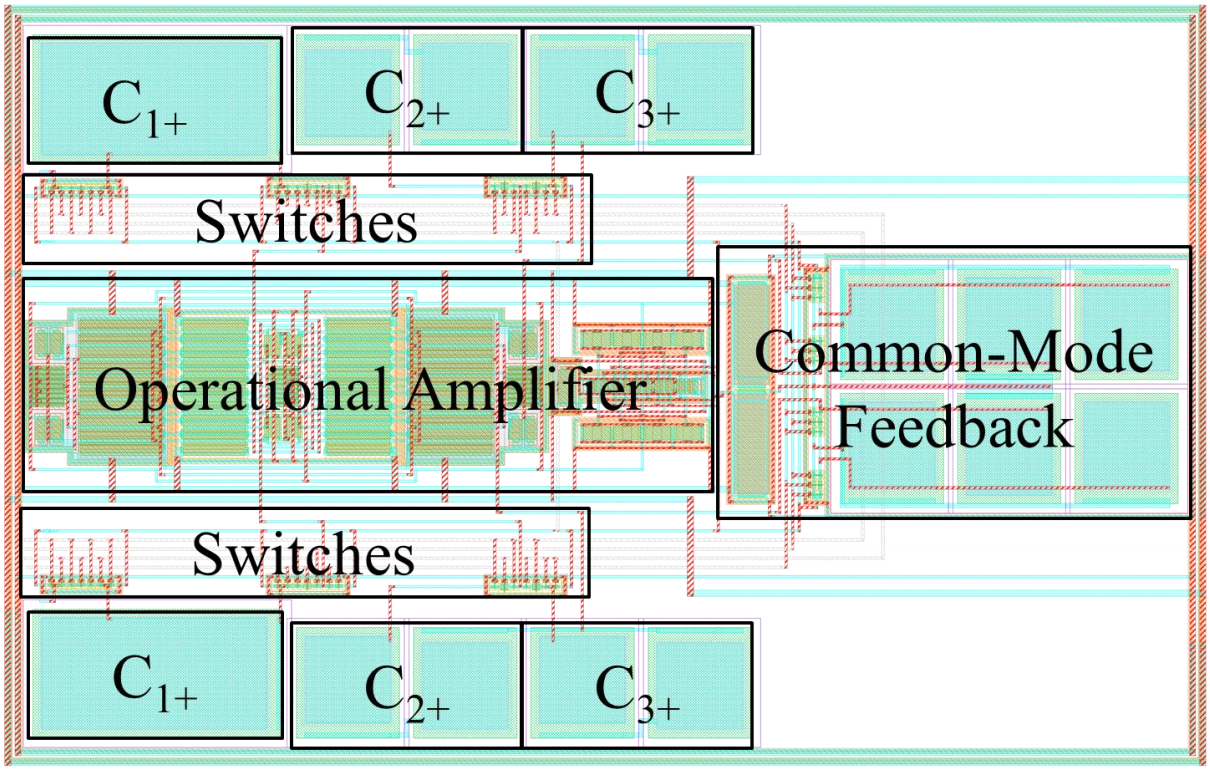

Figure 4-27: Correlated Double Sampling TIA Layout

After finding that small spacing between signal routing traces could create large parasitic capacitances that were detrimental to performance, the routing was spaced liberally in a later version of the layout. The layout also proved to be highly sensitive to asymmetry in the routing, so the circuit was laid out as symmetrically as possible. The overall CDS TIA layout is shown in Figure 4-27.

4.4.6 Slow Integrator Using Correlated Double Sampling

The slow integrator TIA design is a switched capacitor transimpedance amplifier (SCTIA) design with a dedicated three-phase clock scheme to perform correlated double sampling. A modified inverter-based operational amplifier was used in a slow integrating switched capacitor topology. The TIA topology is shown in Figure 4-28. Although this circuit topology has been previously proposed [23], this design takes advantage of the inverter-based amplifier to further reduce the input inferred noise.

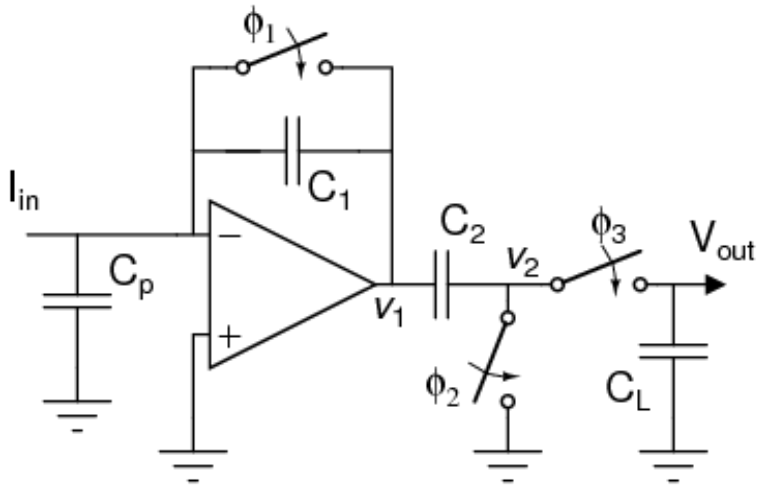

Figure 4-28: Slow Integrator TIA Schematic

Clock phase timing is shown in Figure 4-29, and example input response is shown in Figure 4-30. Basic circuit operation is as follows: during Φ_1, the charges on C_1 and C_2 are set to 0. During the time that Φ_1 is low, C_1 is charged with the input current. The voltage V_1 changes with a slope proportional to the magnitude of the input current. V_2 follows the change in V_1 after Φ_2 goes low.

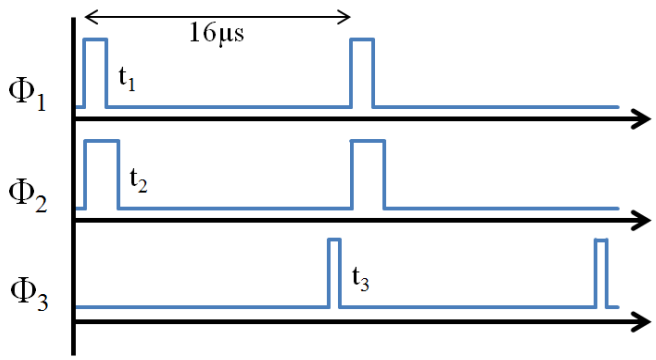

Figure 4-29: Clock Phase Timing

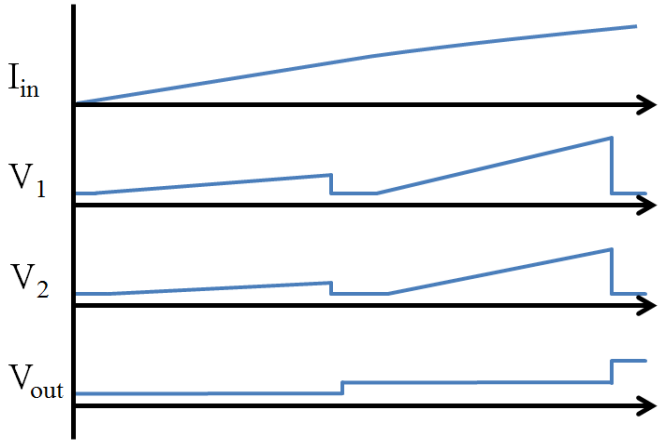

Figure 4-30: Example Input Response

During Φ_2, the OTA offset and 1/f noise are stored as a voltage V_{err} on C_2. At the end of Φ_2, the op-amp output is subtracted by V_{err}, effectively removing the low frequency noise and offset. At this point, the voltage V_2 consists of only the desired signal. The switch controlled by Φ_3 along with the circuit load (next amplification stage, or output capacitance) serves as a sample and hold, which holds the output voltage until the end of the next period. With t_2 and t_3 indicated in Figure 4-29, the TIA output voltage at the end of each clock period can be expressed as shown in Equation 4.1.

$$V_{out}(nT) = \frac{1}{C_1} \int_{t_2+(n-1)T}^{t_3+(n-1)T} i_{in}(t)dt \qquad (4.1)$$

The Class-C inverter-based OTA topology used in this design is shown in Figure 4-31. This design had a slightly modified topology, which allowed for a single-ended output. A summary of OTA performance parameters is shown in Table 4-8.

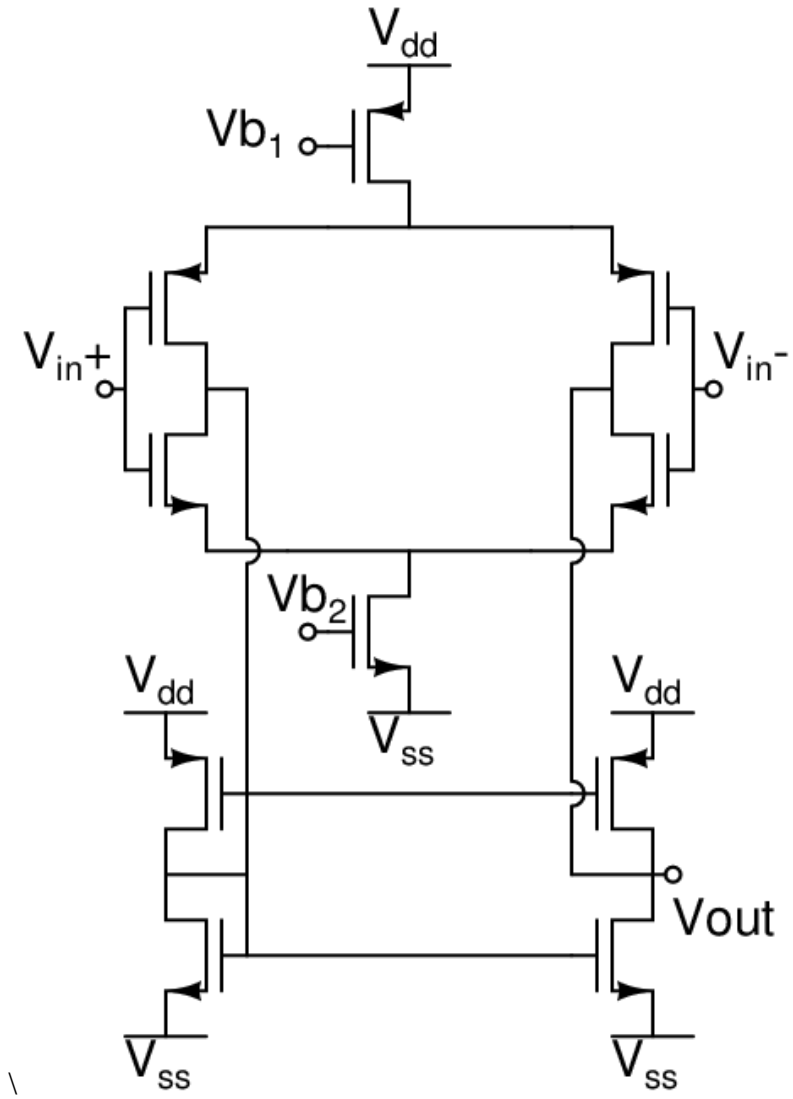

Figure 4-31: Single Ended Inverter-Based OTA Schematic

Table 4-8: Single-Ended OTA Performance Parameters

DC Gain	58.6dB
-3dB Bandwidth	22kHz
Unity Gain Freq.	10.2MHz
Power	8.06µW@0.9V
Phase Margin	53.06°
PSRR	50.4dB
Layout Area	75µm x 51.5µm

Table 4-9: Single-Ended OTA Device Sizing

Device	**Width**	**Length**
PMOS Tail	20µm	500nm
PMOS Input Pair	80µm	4µm
NMOS Input Pair	50µm	4µm
NMOS Tail	2µm	500nm
PMOS Load	38.4µm	5µm
NMOS Load	16µm	5µm

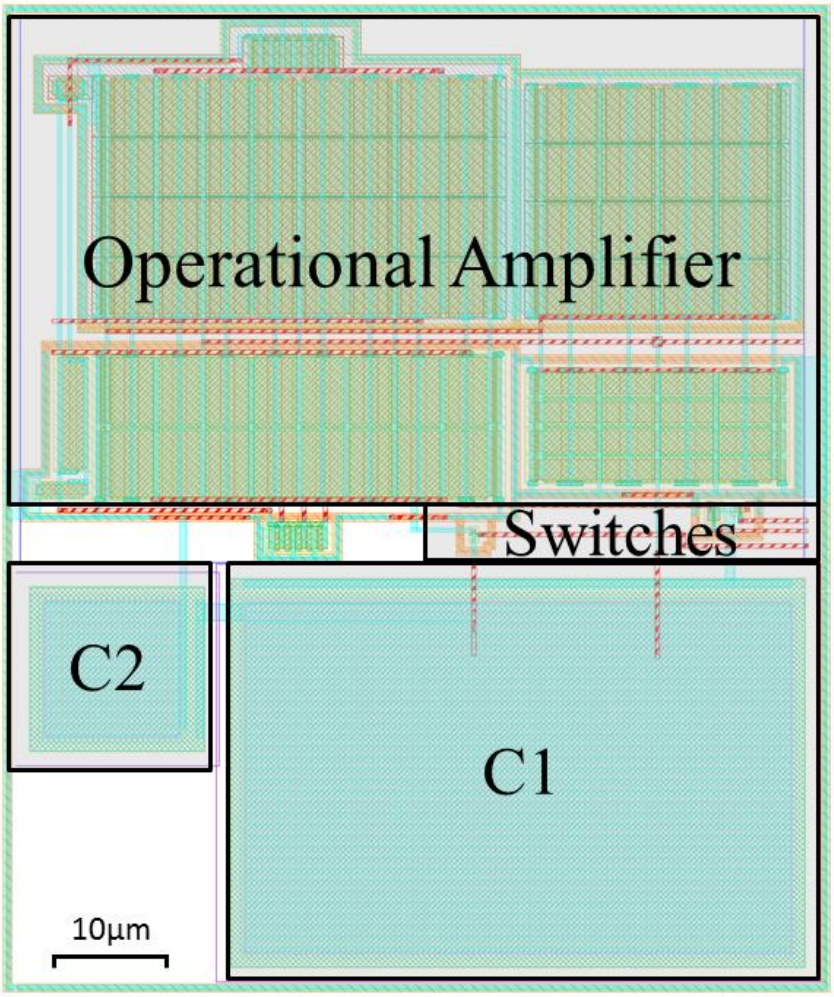

Figure 4-32: Slow Integrating TIA Layout

In simulation, this design achieved a transimpedance gain of approximately 50MΩ. The extracted amplifier layout was simulated with a 1 kHz, 1nA peak sinusoidal current. The output voltage and two internal node voltages, V_1 and V_2 are shown in Figure 4-33.

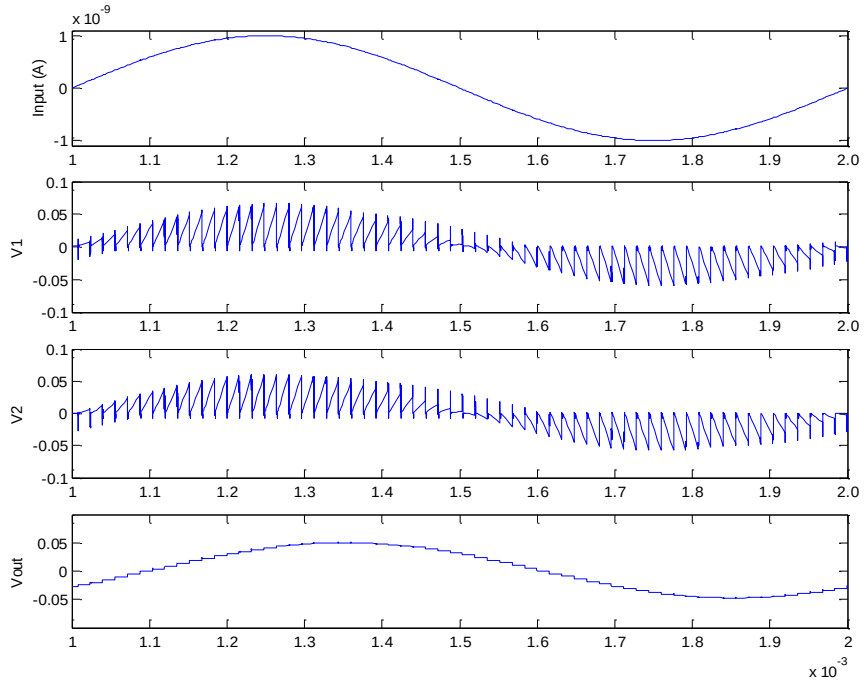

Figure 4-33: Slow Integrator TIA Transient Simulation Results

A periodic steady state noise analysis was also run on the extracted layout. The total overall input referred noise over frequency is shown in Figure 4-34. The design achieved a noteworthy input spot noise of $981fA/\sqrt{Hz}$ at 1 kHz.

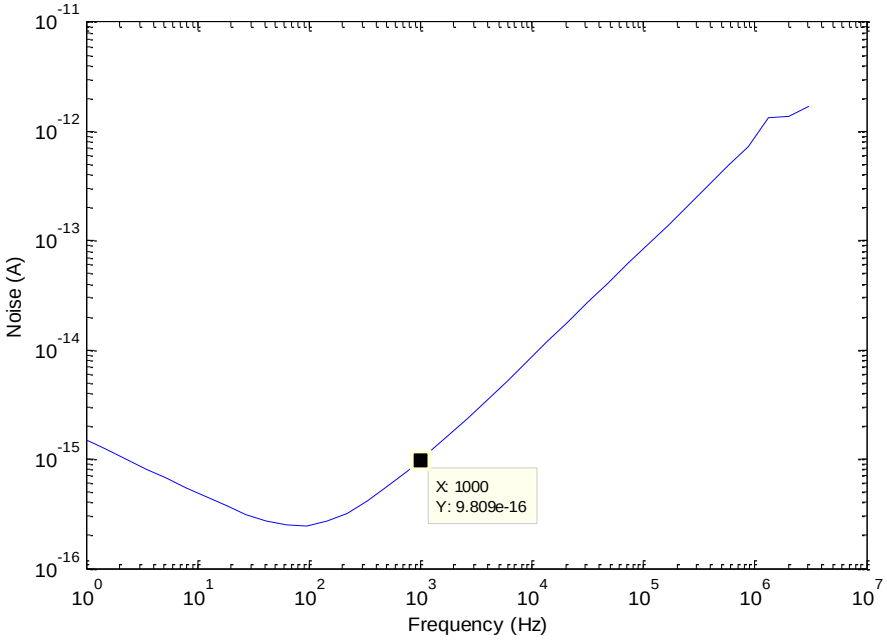

Figure 4-34: Slow Integrating TIA input Noise vs. Frequency

This design's noise characteristics are better than the current low noise integrator designs, and a comparison of performance parameters is shown in Section 7.2.

Chapter 5 Silicon Measurement Results

5.1 Introduction

All of the circuits described in Chapter 4 were fabricated using Texas Instruments' (formerly National Semiconductor's) 180nm CMOS (cmos9t5v) process.

5.2 Testing Setup and Microchip Size Comparisons

The silicon dies were packaged by Texas Instruments, and used either a 40-pin or 64-pin QFN package. A size comparison of the Texas Instruments silicon packages is shown in Figure 5-1.

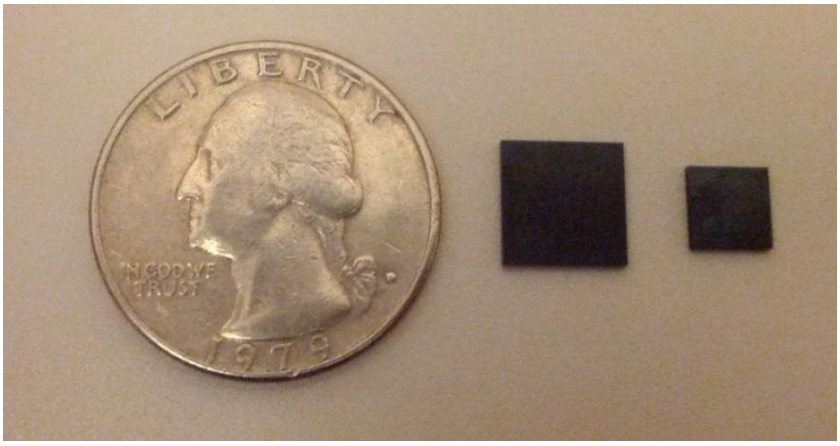

Figure 5-1: National Semiconductor/Texas Instruments QFN Package Size Comparison

To test the circuitry on these silicon chips, a QFN test socket attached to a custom designed printed circuit board (PCB) is used as a breakout board to make the pins on the package more easily accessible. The 64 pin PCB and socket are shown in Figure 5-2, while the 40 pin PCB and socket are shown in Figure 5-3.

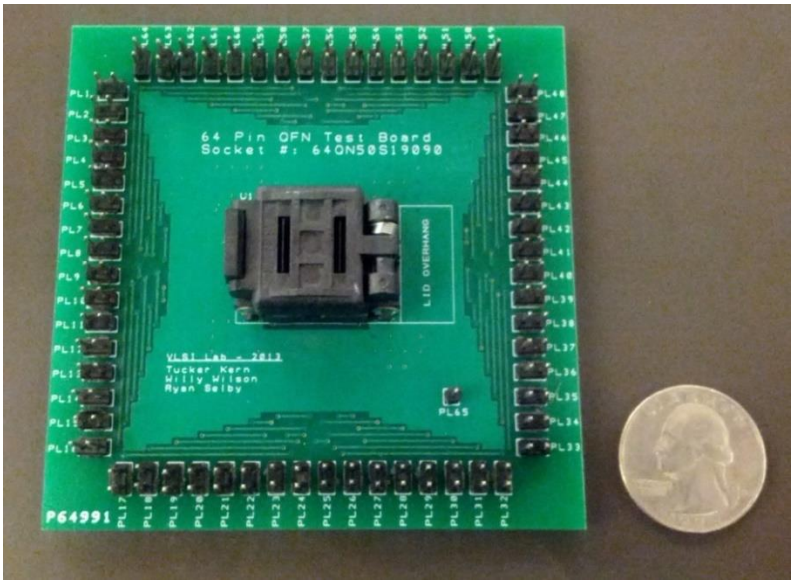

Figure 5-2: 64 Pin Test Socket Size Comparison

It can be noted that the headers (pins surrounding the test socket) are spaced further apart, and that there are two header pins per signal on the 64 pin board. After using the 40 pin board for testing and experiencing difficulty with connecting large numbers of leads, the design was improved when the 64 pin version was drawn.

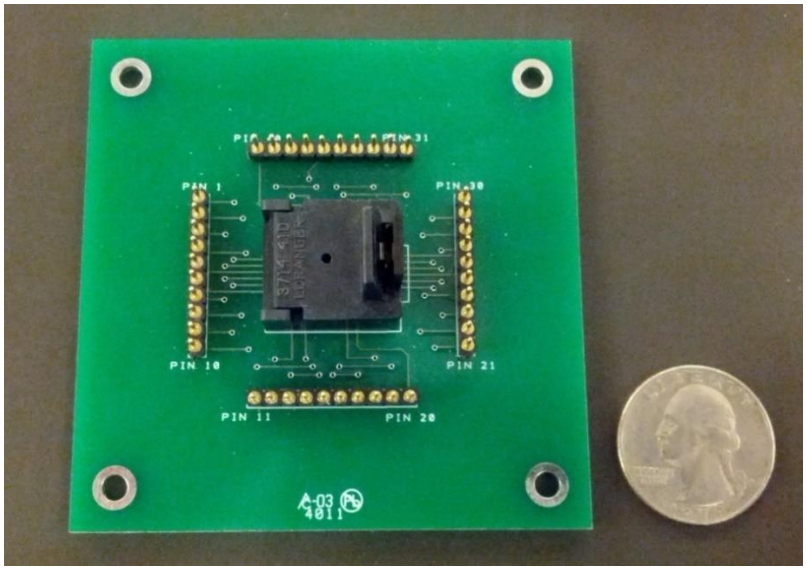

Figure 5-3: 40 Pin Test Socket Size Comparison

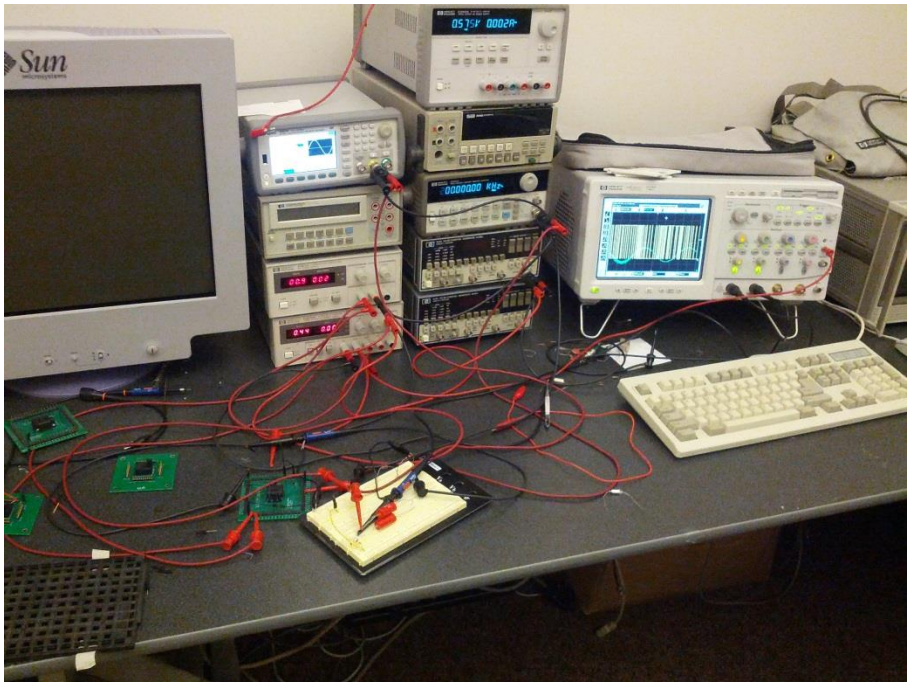

Figure 5-4: Testing bench

A photo of one of the testing bench configurations is shown in Figure 5-4. The overall test bench equipment tends to generate noise itself; this often makes it difficult to determine which noise is coming from the output or outside sources.

5.3 Clock Booster and Current Mirror Silicon

Due to the nature of the clock booster, attaching a largely capacitive trace, pad and oscilloscope probe would deteriorate the performance of the circuit, both in terms of slew and overall peak voltage. When a signal is being sent off-chip, an analog buffer with large drive strength is a common approach; however, in the case of the clock booster, the output needs to be able to swing above the supply voltage. An analog voltage buffer's output would be limited to the supply voltage, and would not solve the problem. Because of these issues, the clock booster's output could not be viewed, but circuitry dependent on the clock booster made its functionality apparent.

5.4 Transimpedance Amplifier Iteration Results

5.4.1 Resistor-Based TIA

The resistive TIA was fabricated in two different versions, one standalone, and one with the main amplifier attached to the output. The main amplifier was attached with input select switches, so that the TIA could be bypassed and the main amplifier could be tested independently. A photo of the resistive TIA in silicon is shown in Figure 5-5.

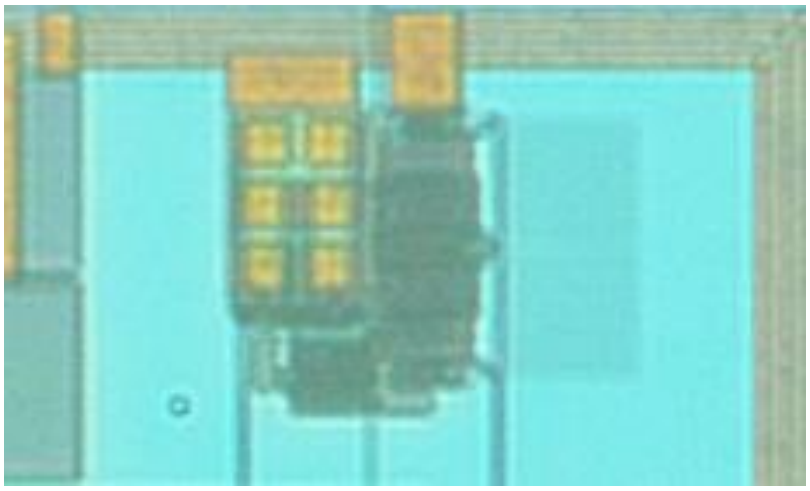

Figure 5-5: Resistive TIA Silicon Image

Due to a lack of necessary input and output pins, the independent resistive TIA was attached to the pad using a set of analog switches. These switches were put in place so that the pins could be shared between multiple circuits. Since the circuit was run at a 900mV supply voltage with a 450mV common mode voltage, a voltage-boosting circuit similar to the clock booster circuit to turn the switches on.

No visible response to a current input could be seen from the standalone resistive TIA. The output consisted of clock noise, possibly indicating that the switched capacitor common-mode feedback circuit was operating. This could be explained by the circuit's input not being

physically connected to the input pad, or the outputs not being properly connected to the output pad through the pin-sharing circuitry.

An additional copy of the resistive TIA which was attached to the main amplifier and sigma-delta ADC was also fabricated. A sinusoidal input current was generated using a function generator and a resistor, and applied to the input of the TIA. The main amplifier and modulator response to the sinusoidal current input are shown in Figure 5-6.

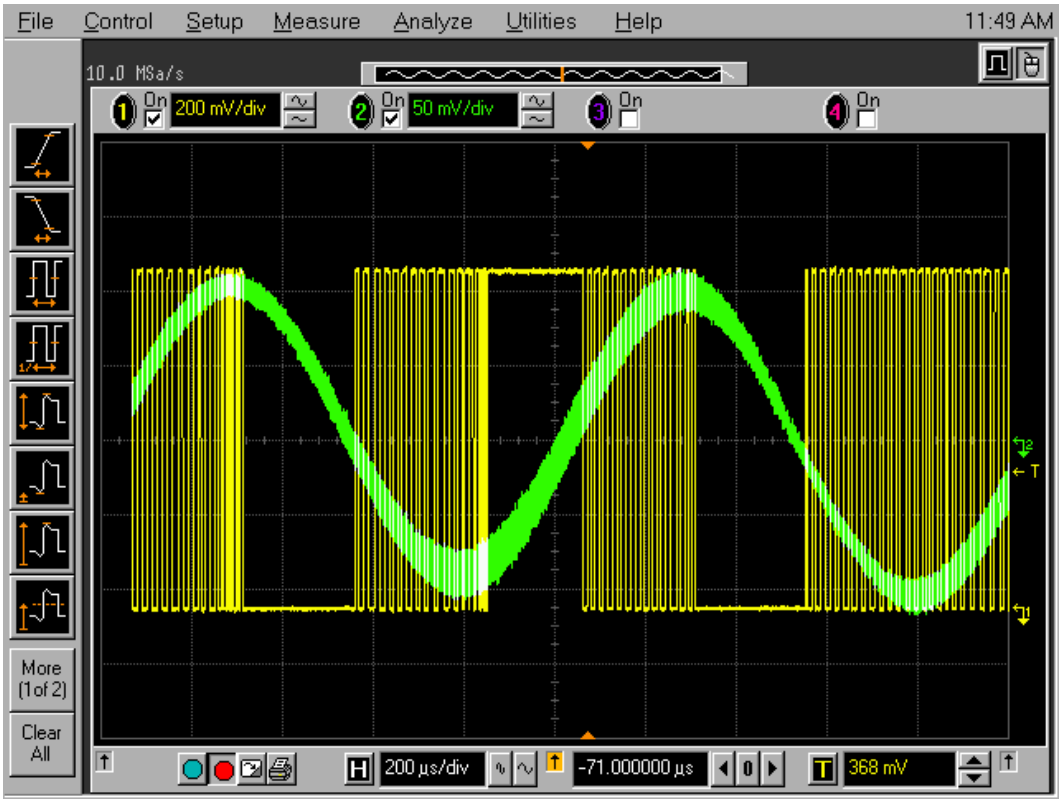

Figure 5-6: Main Amplifier and Modulator Response to Sinusoidal TIA Input

5.4.2 Single-Ended Switched Capacitor

With the single-ended switched capacitor TIA, an input current mirror was also fabricated in the silicon, to allow the creation of a current in the 10's of nA range. Since the input current mirror was a traditional p-type transistor mirror, the circuit could only inject current into the circuit. This meant testing with a negative input current was not possible at the time. The

fabricated silicon showing the TIA as well as the input current mirror and output voltage buffer is shown in Figure 5-7.

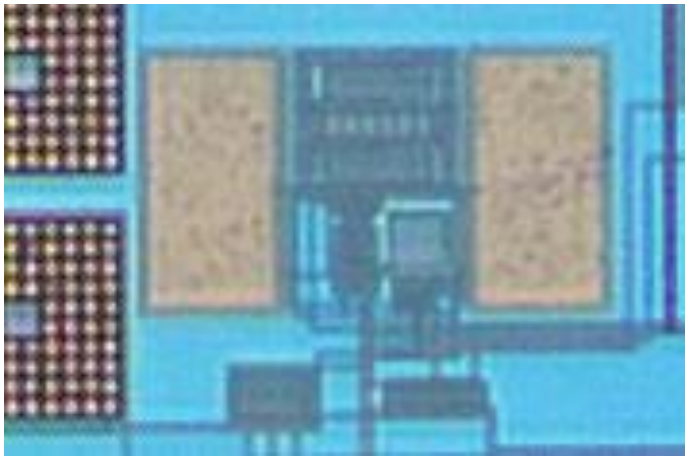

Figure 5-7: Single Ended Switched Capacitor TIA Silicon Photo

The input current mirror, shown in Figure 5-8, is a high impedance p-type mirror, which allows us to create sub-µA magnitude currents without a high-precision bench-top current source. The current mirror output was also attached to an external pad, to allow the input mirror to be bypassed if a small-magnitude current mirror became available.

Due to the resolution of the equipment used to measure the output signals from the TIA, as well as noise from the test bench, the small voltage output generated with a 10nA signal could not be seen. In order to more easily measure the output voltage, the input current was increased.

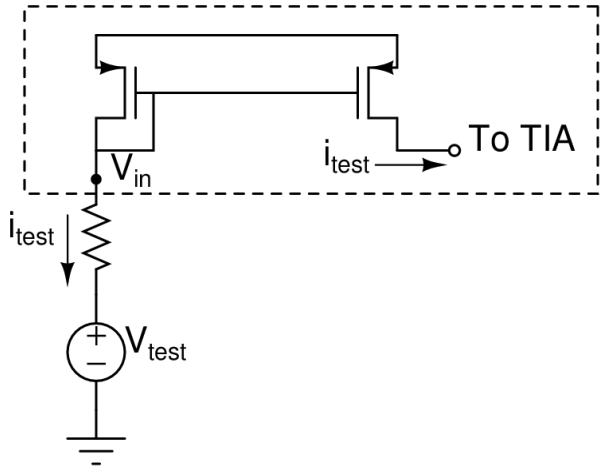

Figure 5-8: Input Current Mirror Schematic

The circuit was tested with a 100nA input current and initially run at the designed clock speed of 1MHz. The measured output is shown in Figure 5-9. During testing, the output showed large amount of switching noise, as well as a voltage step that is hypothesized to be effects of charge injection. This noise could also be attributed to instability in the overall feedback network.

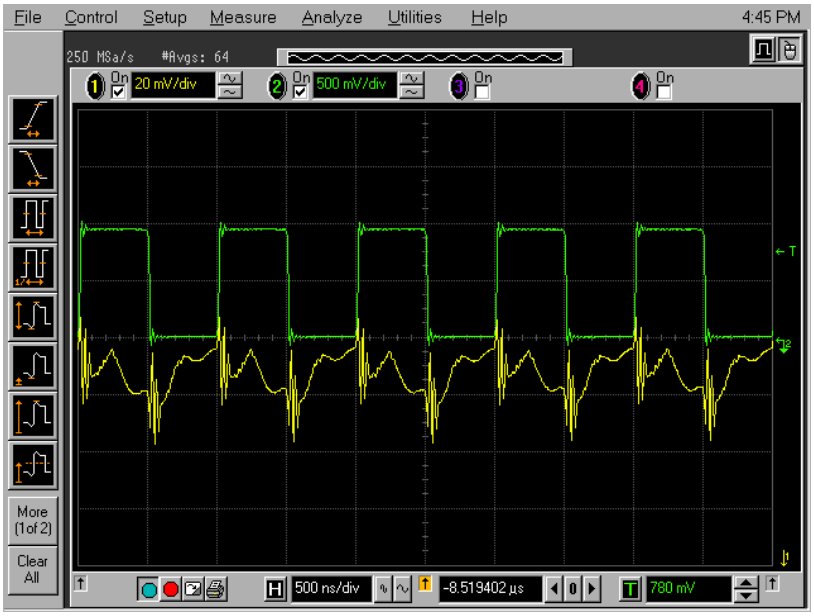

Figure 5-9: Response to a 100nA DC current at 1MHz clock

The signal peaks at about 20mV at the end of the integration phase, indicating that the circuit achieves an overall transimpedance gain of about 200kΩ.

With a traditional switched integrator design, the clock speed can be slowed down, increasing the gain proportionally. When the clock rate was reduced to 500 kHz, the circuit's output indicated an increase in the overall transimpedance gain of about 2x.The Circuit's response to the same 100nA input current while running at 500 kHz is shown in Figure 5-10

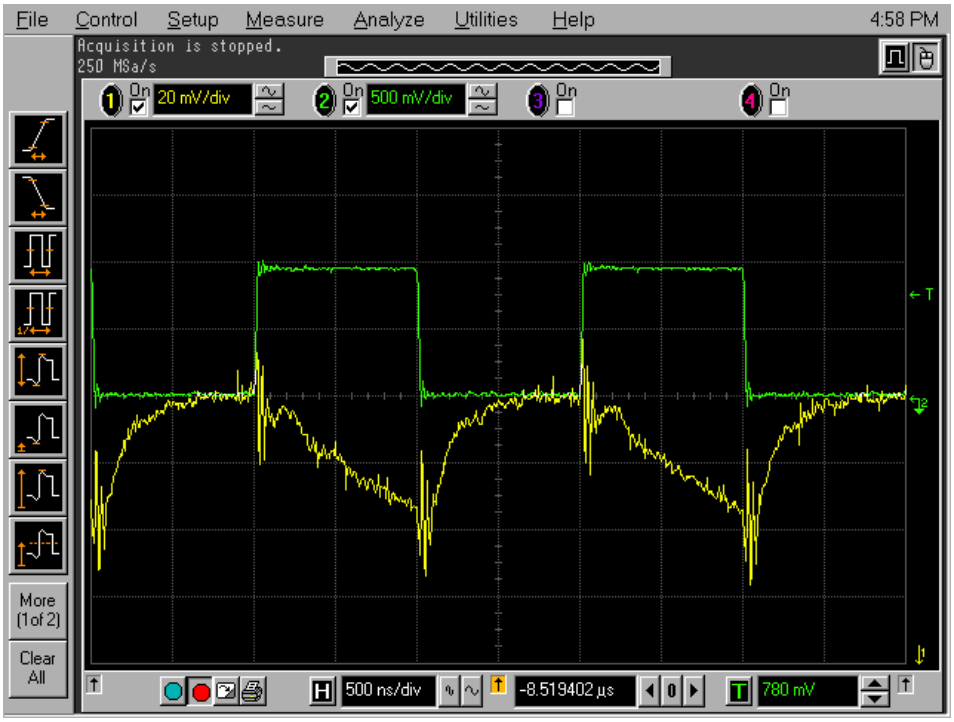

Figure 5-10: Response to a 100nA DC current at 500 kHz clock

At 500 kHz, the magnitude of the switching and charge injection noise appears to be the same, but the circuit now has more time to integrate a larger amount of charge before resetting. With the slowed clock, the circuit achieves a gain of approximately 350kΩ.

To further test the circuit's functionality, the input current was increased to 300nA. With the increased input current, the peak response increased to approximately 100mV. This

corresponds to a gain of approximately 330kΩ, which is appropriate for the amount of voltage swing occurring at the circuit's output.

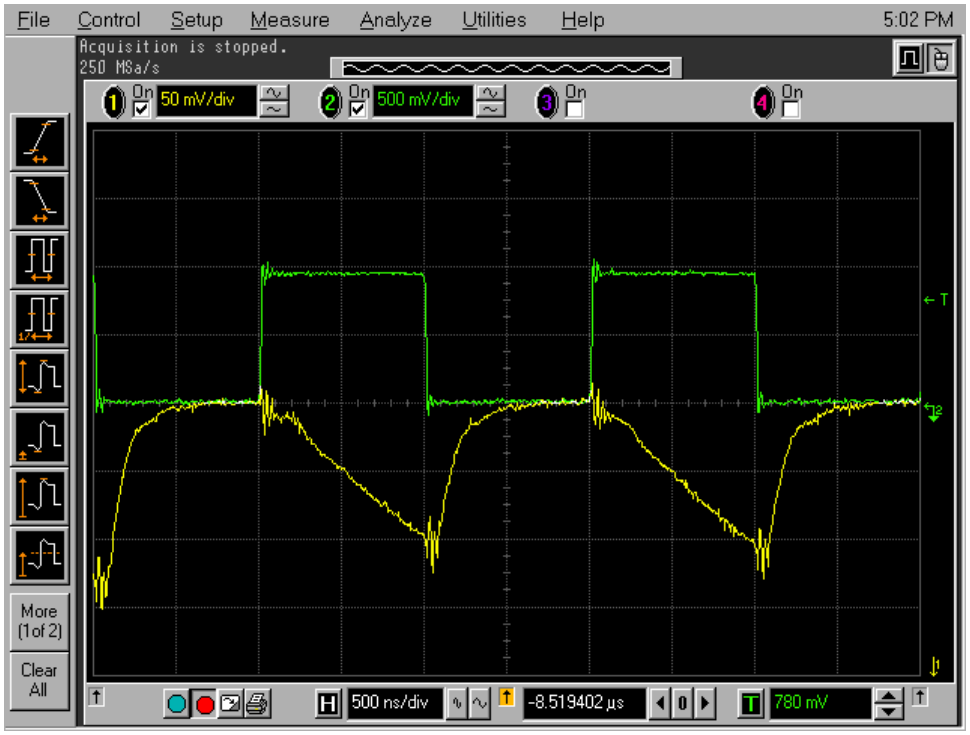

Figure 5-11: Response to a 300nA DC current at 500 kHz clock

5.4.3 Pseudo-Differential TIA

The pseudo-differential TIA included a single-to-differential current mirror, which was driven by the input current mirror shown in Figure 5-8. The overall circuit in silicon is shown in Figure 5-12.

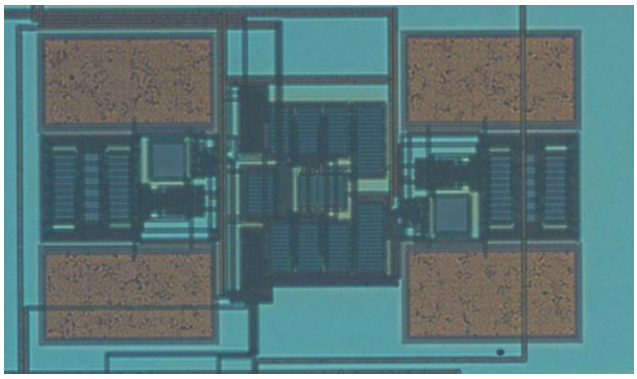

Figure 5-12: Pseudo-Differential TIA Silicon Photo

To start, the circuit was tested with a 10nA input current at a 1MHz clock rate. Both outputs appeared to consist primarily of clock noise. This output is shown in Figure 5-13.

Figure 5-13: TIA Response to 10nA Input Current at 1MHz Clock Rate

When the circuit's clock rate was reduced to 500 kHz, a difference started to appear between the integration and reset phases. The output from the circuit running at 500 kHz is shown in Figure 5-14.

Figure 5-14: TIA Response to 10nA Input Current at 500 kHz Clock Rate

The output magnitude was still too small to accurately measure the gain, so the clock was further slowed to 200 kHz. At this frequency, the circuit's response to a 10nA signal was clearly visible. The integration of a 10nA DC current resulted in a 20mV differential peak at the end of the integration phase, as shown in Figure 5-15. A 20mV peak with a 10nA input current corresponds to a transimpedance gain of 2MΩ at 200k Hz. Assuming the transimpedance gain scales inversely proportional to operating frequency, 2MΩ at 200 kHz corresponds to a differential transimpedance gain of 400kΩ at a 1MHz clock rate.

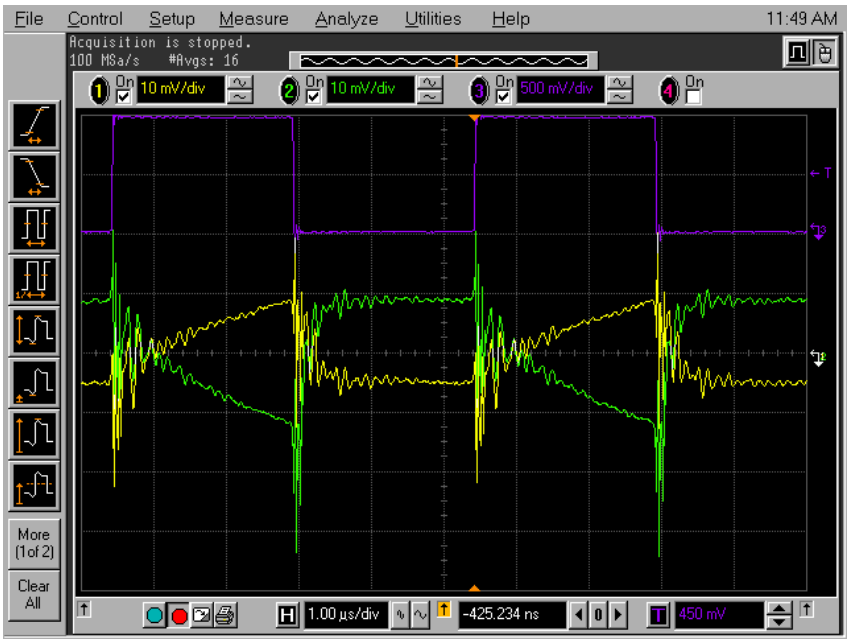

Figure 5-15: TIA Response to 10nA Input Current at 200 kHz Clock Rate

The overall circuit appears to function similar to the single-ended circuit. In the oscilloscope outputs shown throughout this sub-section, common mode switching noise is apparent. Additionally, there appears to be issues with the two outputs not resetting to the same value during the reset phase, as well as a DC error during the integration phase. These issues can be attributed to op-amp offset, and effects of process variation on the current mirror output.

5.4.4 Fully Differential TIA with Bottom Plate Sampling

The fully differential TIA design included a redesigned single-to-differential current mirror, which used larger split-length transistors and common centroid layout techniques to help reduce output current variation due to process variation and device mismatch. This TIA revision also was the first to omit the input mirror, and have the current input pin directly feed the single to differential mirror. The overall layout of the differential TIA is shown in Figure 5-16.

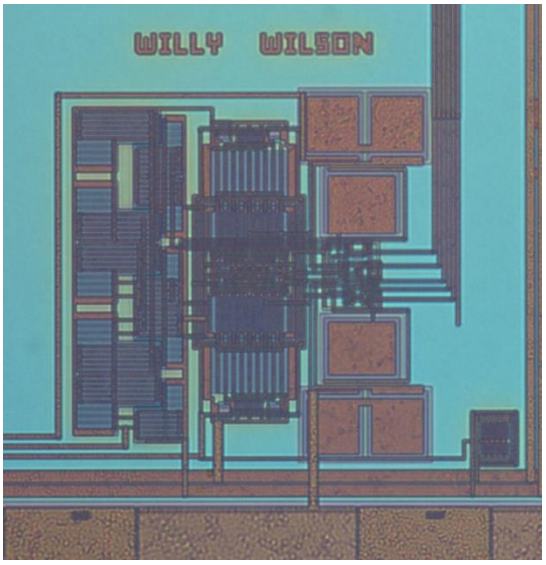

Figure 5-16: Bottom-Plate Sampling TIA Silicon Photo

Testing of the differential TIA showed that the circuit was functioning, but the gain and output parameters were far from ideal. Throughout the layout and testing process, the device was shown to be very sensitive to parasitic capacitances and asymmetric routing.

To begin testing, zero input current was attached to the input of the current mirror. The results of zero current input gave a differential voltage of approximately 10.68mV at the end of the integration phase. The response to zero current input is shown in Figure 5-17.

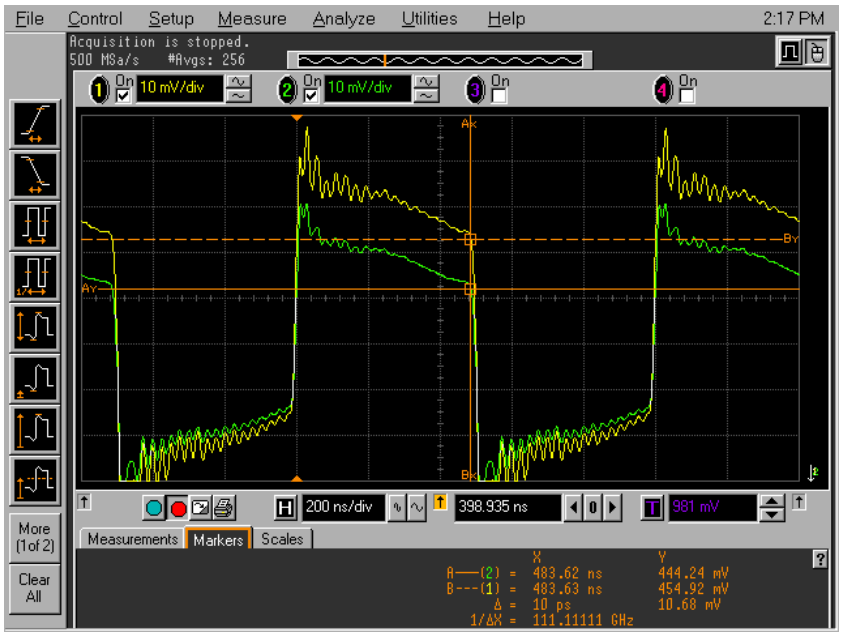

Figure 5-17: Zero Input Current Response at 1MHz Clock Rate

To test the response of the circuit to a positive input, a 300nA DC current was applied to the input of the current mirror. The measured output is shown in Figure 5-18.

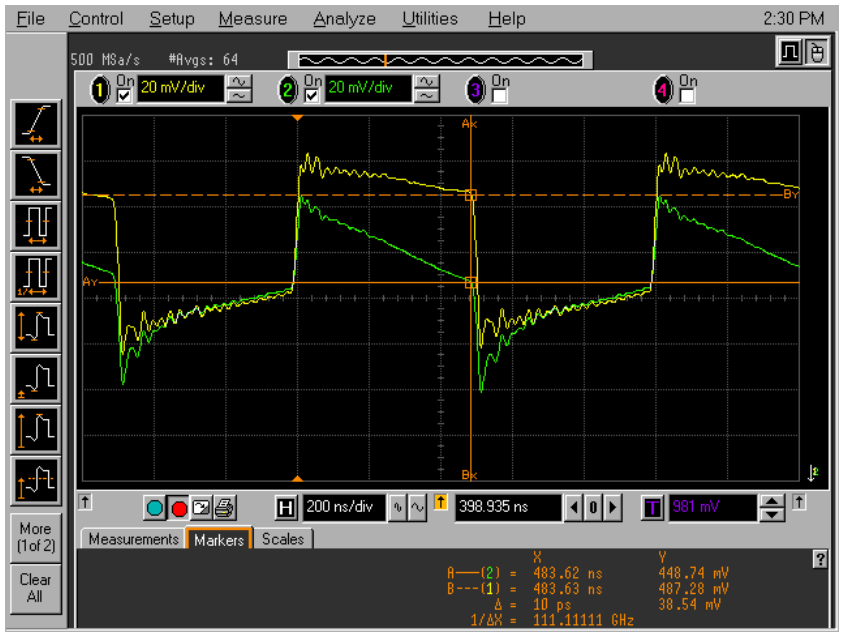

Figure 5-18: 300nA Input Current Response at 1MHz Clock Rate

A 300nA DC input caused a differential output change of approximately 27.9mV. This change corresponds to a transimpedance gain of only 93kΩ, as opposed to the designed 3MΩ.

The next step was to test the circuit's response to a negative current input. A -300nA DC current was applied to the input of the current mirror, and gave the result shown in Figure 5-19.

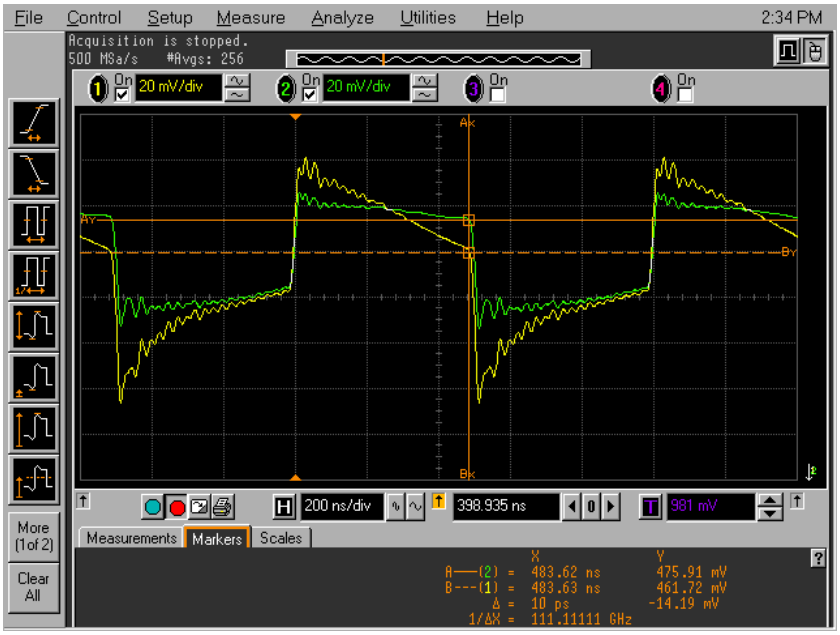

Figure 5-19: -300nA Input Current Response at 1MHz Clock Rate

The application of a -300nA test current to the current mirror input caused a differential voltage output change of only 24.9mV, which corresponds to a transimpedance gain of under 90kΩ.

The overall discrepancies in gain can be attributed to multiple sources, including high sensitivity to parasitic capacitances, variation in the higher-impedance single-to-differential current mirror, and an overly ambitious reduction in overall circuit power consumption and drive strength.

5.4.5 Correlated Double Sampling

The correlated double sampling TIA was a complex design that required a 2MHz clock input that was divided down to two out-of-phase 1MHz clocks by a set of on-die flip flops. The 1MHz clocks were then fed into two separate non-overlapping clock generators with clock

booster circuits attached to the outputs. The overall clocking scheme was complex and left significant room for errors. It also had the disadvantage of having an integration phase that lasted less than 250ns when a 1MHz clock was used.

During layout, the CDS TIA was prone to issues caused by asymmetry in trace routing, as well as parasitic capacitances on devices and traces that weren't spaced at sufficient distances. The overall layout is shown in Figure 5-20.

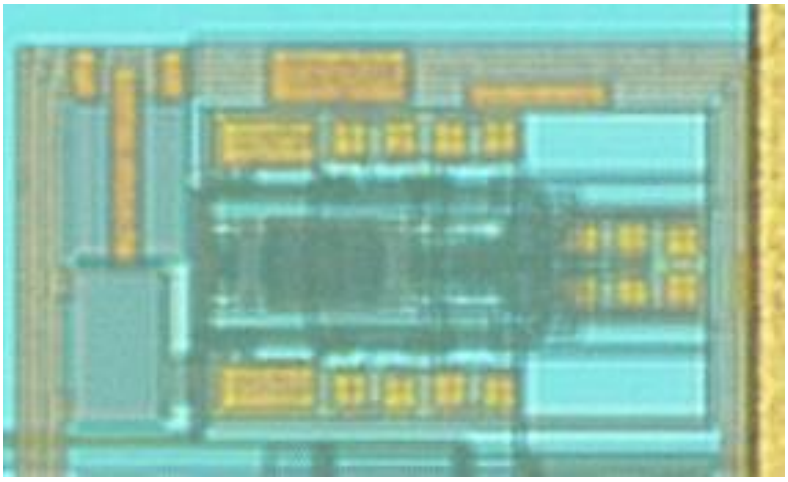

Figure 5-20: Correlated Double Sampling TIA Silicon Photo

As with the resistive TIA design, the correlated double sampling design was attached to the output pins using a set of analog multiplexing switches. Both a standalone version and two copies of the circuit with main amplifiers and modulators were fabricated. No visible response to any input current input could be seen from any of the correlated double sampling designs.

5.4.6 Slow Integrator Using Correlated Double Sampling

The slow integrator design utilized a special three-phase, 125 kHz clock. The use of this slow clock gave the circuit the advantage of an integrating phase that lasted approximately 15µs. This allowed ample time for small currents to be integrated onto the sampling capacitor before the circuit reset, creating a much cleaner output signal in simulation.

The slow integrator TIA, as well as the dedicated 3-phase clock generator and voltage output buffers are shown in Figure 5-21.

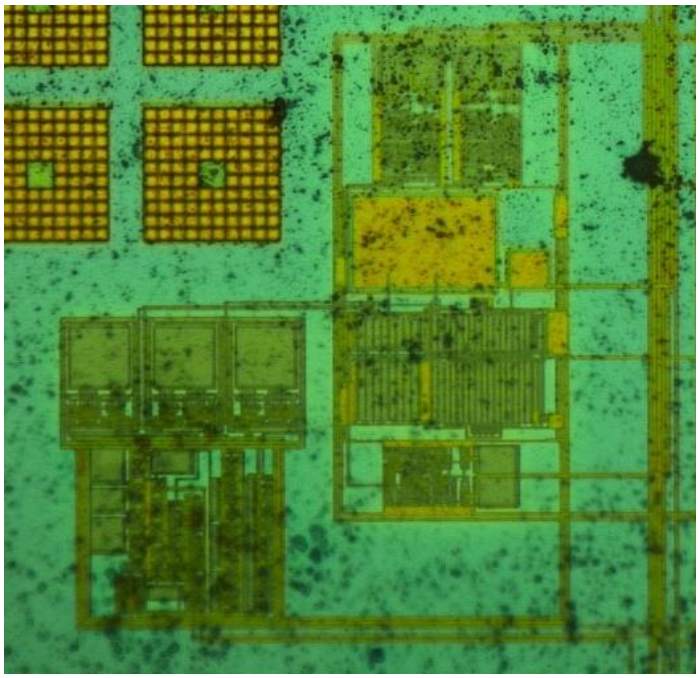

Figure 5-21: Slow Integrator Silicon with TIA, Output Buffers and Clock Generator

The circuit was tested by sweeping the input current from -90nA to +90nA in 10nA increments. A test script was written to change the current input, wait two seconds and measure the DC output level, increase the input current, and repeat. The script was used to test a sample set of 20 chips. The resulting input current vs. output voltage is shown in Figure 5-22

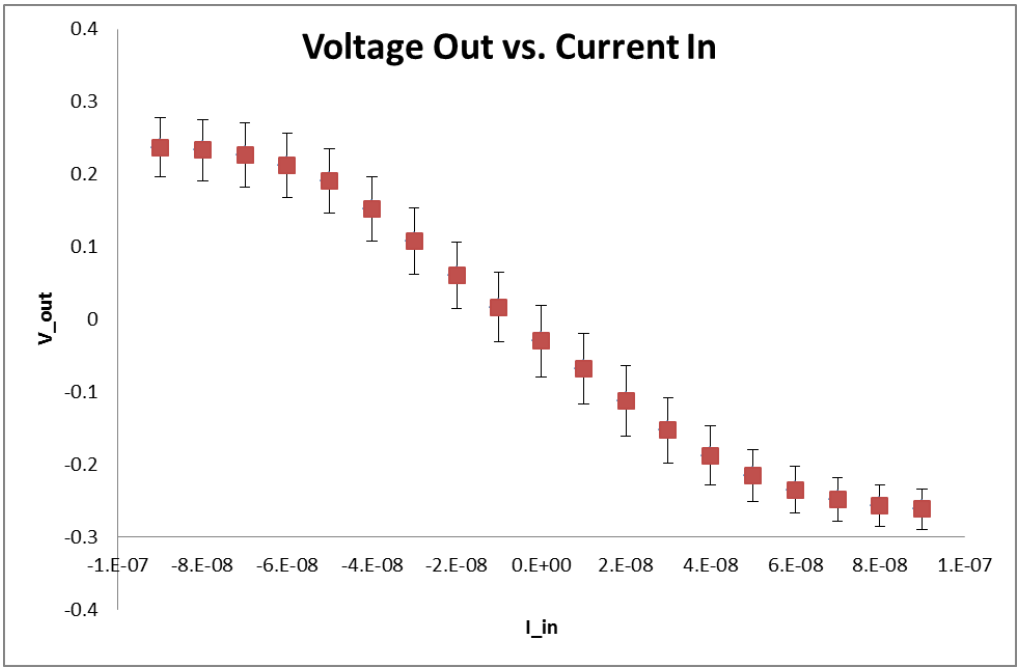

Figure 5-22: Slow Integrator Output Voltage vs. Input Current (20 Samples)

The circuit appears to have a transimpedance gain of approximately 5MΩ while still operating linearly. As the input current magnitude increases to above 50nA, the circuit's output begins to saturate. This transimpedance gain was a factor of 10 lower than the designed gain.

The circuit was also tested using a 10nA sinusoidal current input, giving the result shown in Figure 5-23.

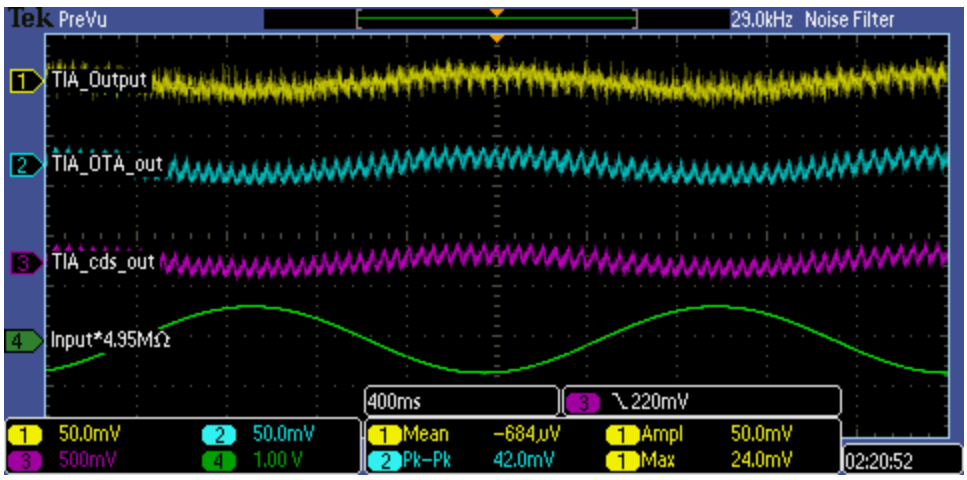

Figure 5-23: Slow Integrator Response to a 10nA Sinusoidal Input Current

The circuit operated at a consistent 125 kHz clock rate, and the three internal node voltages appeared to integrate as expected. The output, although somewhat noisy, had the expected track-and-hold operation pattern. With the oscilloscope's noise filter bandwidth decreased, the circuit output and internal node voltages appeared as clean sinusoidal voltages, as seen in Figure 5-24.

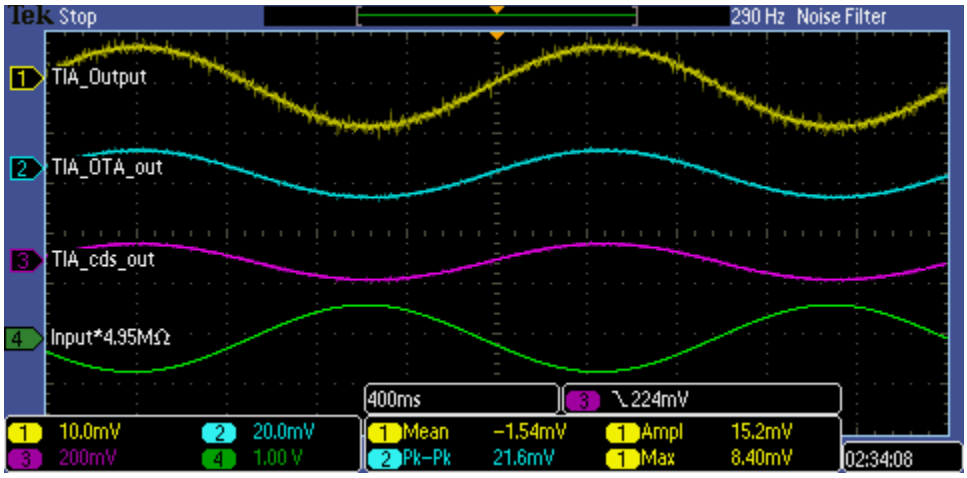

Figure 5-24: Filtered Circuit Response to a 10nA Sinusoidal Input Current

An additional measurement with no noise filter was taken to show the detail of the integrating operation of the internal node voltages. This measurement is shown in Figure 5-25.

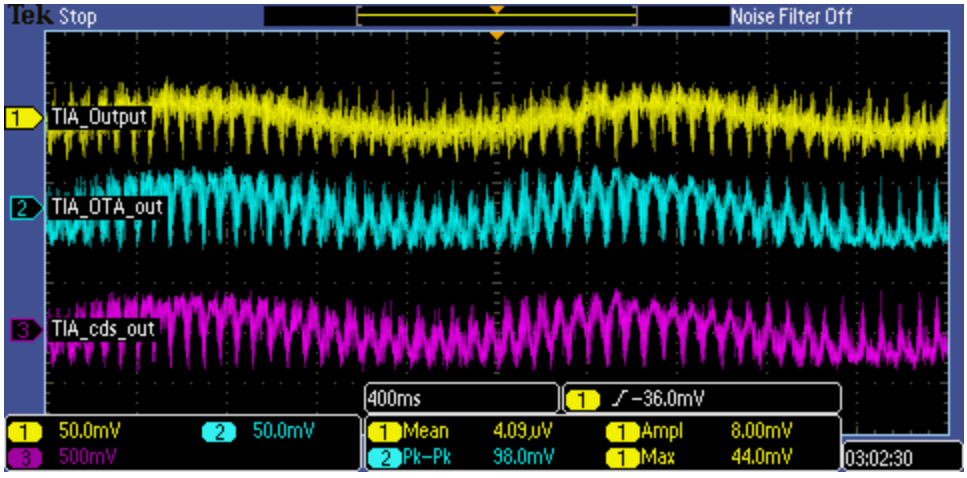

Figure 5-25: Circuit Response showing Detailed Integration Phases

The slow integrator operated as expected, with the exception of the reduced transimpedance gain. After further investigation and simulation, it was discovered that parasitic capacitances on the internal nodes could have an effect on the gain of the circuit, by offsetting the expected ratio of the two capacitors. The circuit was designed with the intention of having minimal capacitance on the internal node routing. At the time of the final layout before fabrication, it was decided that probing the internal node voltages using on chip voltage buffers would be beneficial to the overall debugging of the circuit design.

One potential method to solve this issue would be to simply build the circuit without the internal node voltage being probed. This could solve the issue, but runs the risk of having no response at the output with no debugging tools available. Another solution would be to increase the size of the internal capacitances as well as the overall current consumed by the amplifier, but this would be compromising the small size and power consumption of the overall circuit.

Chapter 6 Experiments with Biosensor Systems (Generation 2 Avago Chip)

6.1 Introduction

In May of 2013 the VLSI lab submitted a design for an integrated biosensor chip which included a large electrode array. This chip consisted of 8192 working electrodes, which were divided into 64 sub-arrays, each containing 128 electrodes. With the division of the chip into 64 sub-arrays, the electrodes could now be time-multiplexed into 128 read channels, each consisting of a current mirror, transimpedance amplifier and voltage amplifier.

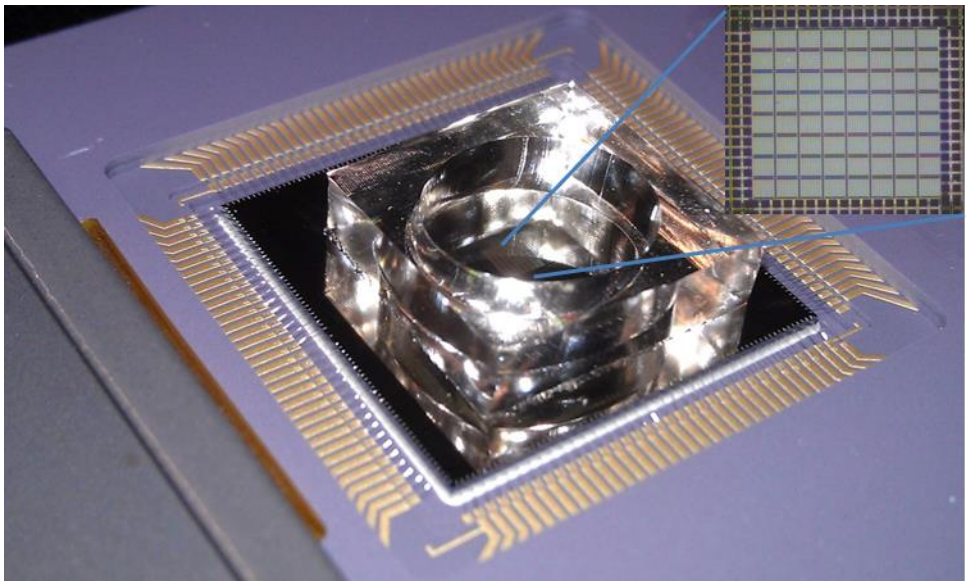

Figure 6-1: Packaged Avago Chip with PDMS Well, Showing 64 Sub-Arrays

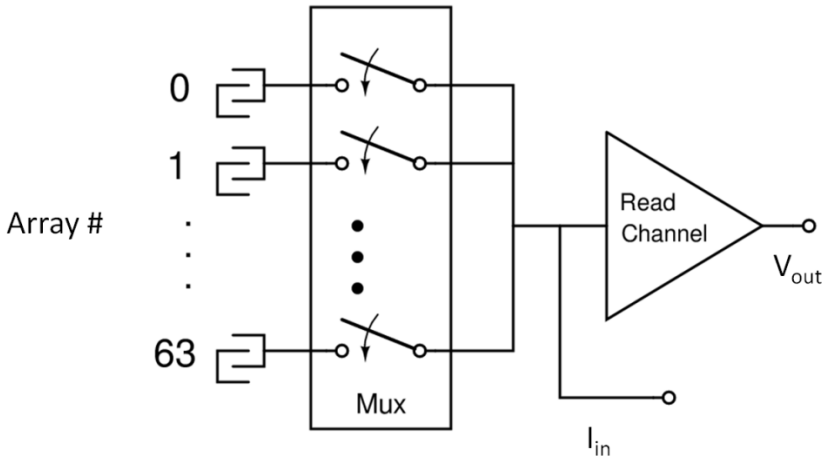

Figure 6-2: Avago Electrode Multiplexing (1 of 128 channels)

Silicon testing showed that the on-chip read channels were inoperable, and after further testing, a DC leakage current of about 90nA was measured at the output of the electrode multiplexing circuitry (I_{in} terminal in Figure 6-2). Since the read channel circuitry was initially designed to detect currents of about 1nA, it was concluded that the on-chip electronics were pushed beyond their usable range by the leakage current introduced either from the electrode multiplexing circuits or the read channel electronics. Although the leakage current rendered the on-chip read channels unusable, the multiplexing circuitry was operational, meaning the on-chip electrode array could still be used with external electronics, as long as the leakage current is within the external circuit's input current range.

6.2 External TIA Design for Connection to ADLINK DAQ-2208 Boards

In order to utilize the integrated electrode array, an external transimpedance amplifier was needed. To keep the manufacturing of 128 channels simple, a basic resistive design utilizing

10MΩ (±5%) resistors and a Texas Instruments OPA381 amplifier was used. To reduce noise and help stability, a 1nF feedback capacitor was also added.

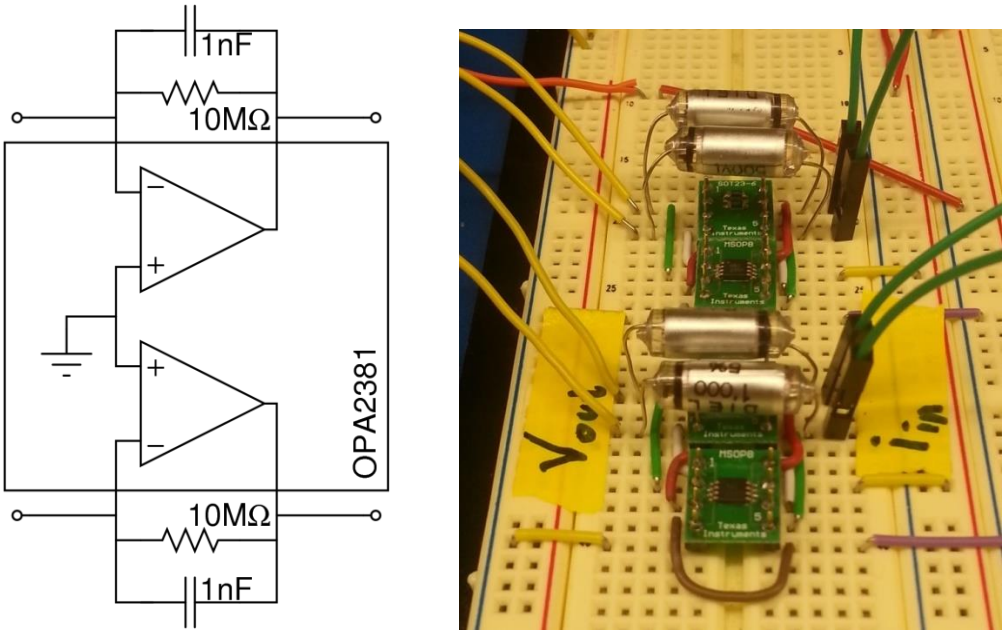

Figure 6-3: Two-Channel Discrete TIA Schematic and Breadboard Testing Setup

For the implementation of the schematic shown in Figure 6-3, an MSOP8 surface mount dual op-amp package and surface mount 0805 resistors and capacitors were used. A photo of the pcb-mounted dual op-amp package, resistors and capacitors is shown in Figure 6-4.

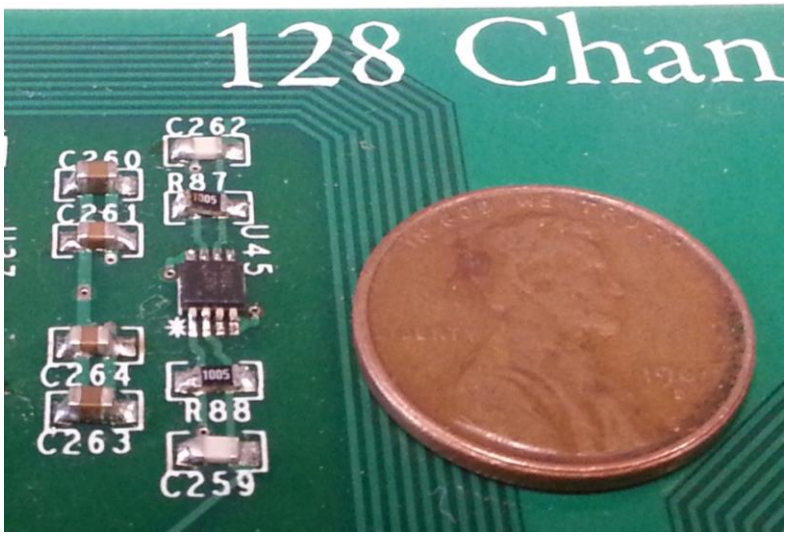

Figure 6-4: Discrete TIA on PCB Size Comparison

These discrete transimpedance amplifiers were connected to the electrode multiplexing circuitry through a PCB-mounted test socket, and their outputs were connected to two ADLINK 2208 96 channel analog to digital converter pci express cards inside a PC, using 68-pin VHDCI connectors.

6.3 MATLAB Script for Data Acquisition

Once the hardware for connecting the chip to the PC was built, a method for acquiring data was necessary. The ADLINK cards included drivers and acquisition software, but the abilities of the acquisition software were inadequate for our purposes. Since MATLAB drivers were also available, it was decided that data acquisition should be done using MATLAB.

The MATLAB script had two primary tasks: acquire data with consistent timing, and plot live, real-time results in a graph window. Since MATLAB doesn't support true multi-threading, plotting and recording simultaneously proved to be a challenge. After several revisions, a version of the software that can coherently keep track of time while plotting and switching electrode arrays was completed.

6.4 Gradient Recording as a Proof of Concept

Since the ultimate goal of the project is to create a method of visualizing the movement of electrochemically active compounds across the electrode array over time, one of the first steps taken was to create and record a diffusion gradient on the array.

To create a diffusion gradient, a PDMS well was placed on the surface of the chip. The well was filled with 200µL adult neurobasal (ANB) media, data recording was started on a single sub-array, and a baseline (zero value) was collected for the electrodes. After a baseline was

collected, a 10µL drop of 100mM Norepinephrine solution was gently dropped into the upper-leftmost corner of the well. The result was the signal shown in Figure 6-5.

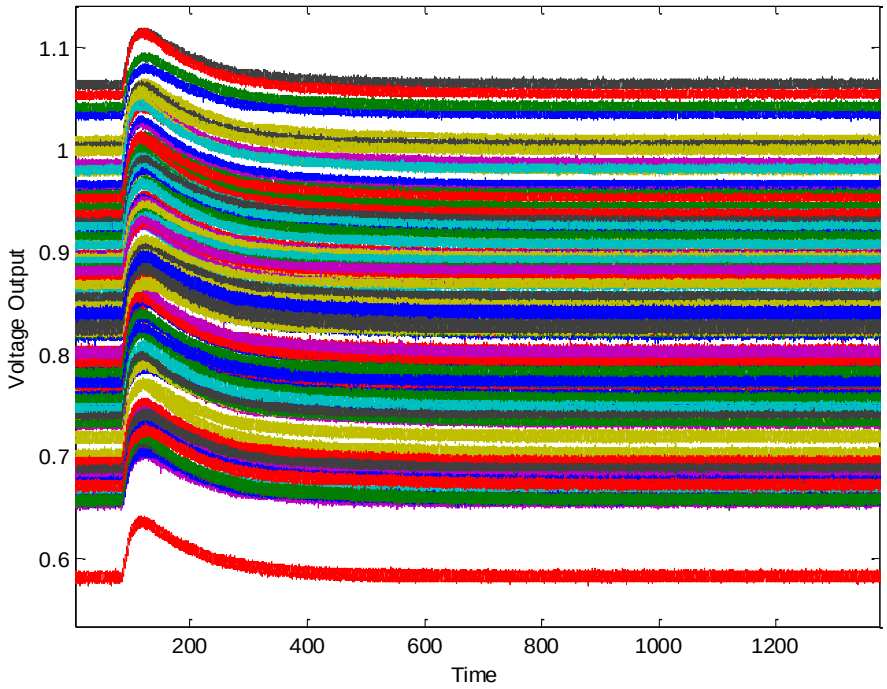

Figure 6-5: Raw Signal from 10µL 100mM Norepinephrine Diffusion Gradient

An additional MATLAB script was written to turn the recorded data into a corresponding electrode heat-map video. Snapshots showing the diffusion from the upper-left to bottom-right corner of a single sub-array are shown in Figure 6-6.

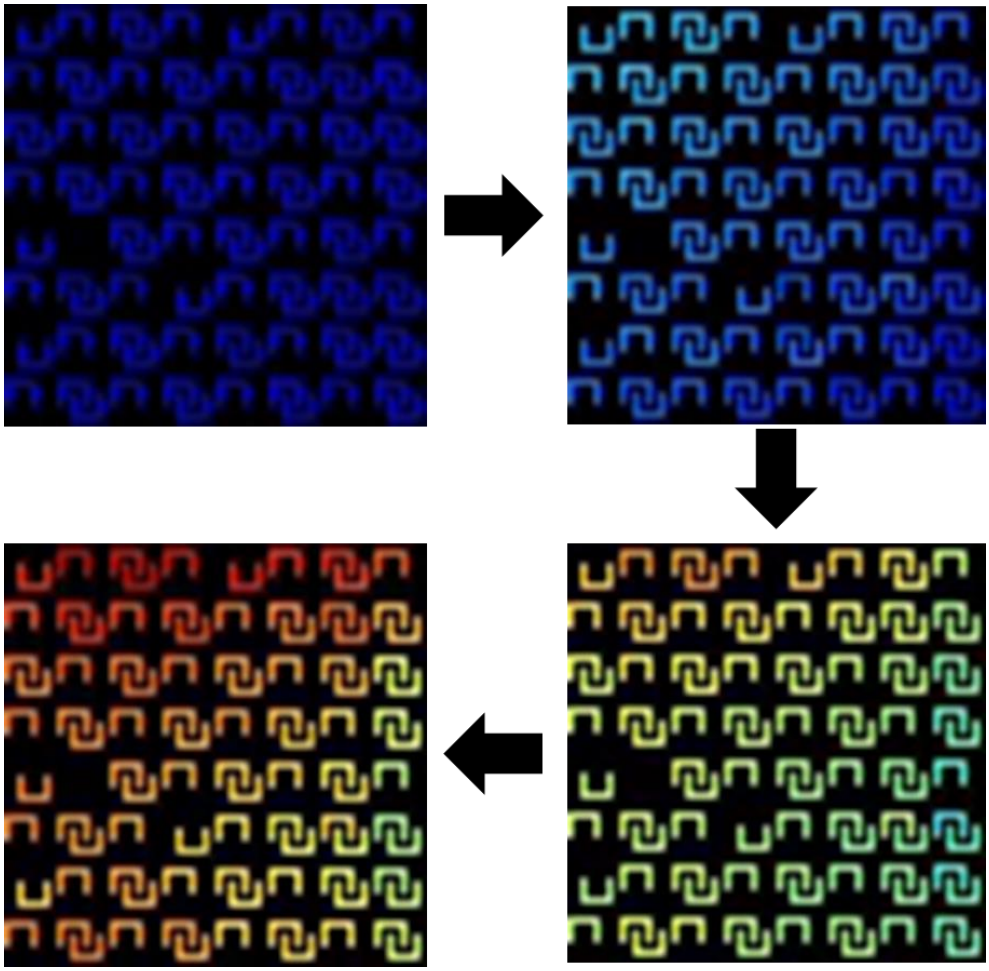

Figure 6-6: Example Heat-Map Video Generated from Gradient Data

Due to implementation issues with the ADLINK boards, two boards could not be synchronized to collect all 128 channels of data, so the system is currently limited to either the 96 channels attached to card 1 or the 32 channels attached to card 2. This limitation explains the missing electrode shapes in Figure 6-6.

6.5 Improvements to Chip Packaging

A standard method of packaging silicon chips after fabrication is to adhere the silicon die to a package, and use extremely small and thin bonding wires to connect the input and output

pads to the package. This package can then be sealed so the silicon and delicate bonding wires are protected, and then either soldered to a printed circuit board or used in a socket.

With the Avago-manufactured biosensor chip, the top of the silicon contained the electrode array, and could not be covered with any type of protective coating. This also means that the delicate wire bonding must also be exposed, where it is susceptible to leaked fluids and difficult to clean if a leak happens.

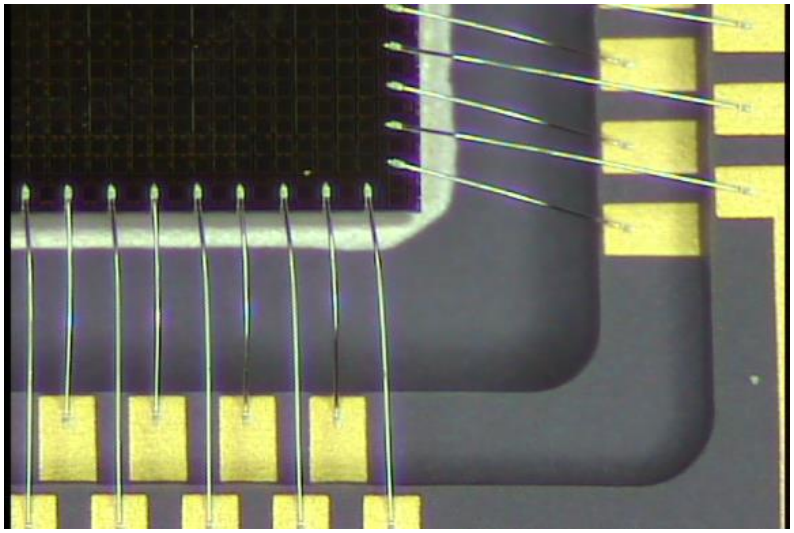

Figure 6-7: Avago Wire Bonding Close-Up

After several chips were ruined during the cleaning of leaked fluid, a polyester resin was proposed as a method of protecting the wire bonding. The resin used for initial testing was a clear polyester casting resin, intended for encasing objects in clear plastic. The results of the initial resin pouring are shown in Figure 6-8.

Figure 6-8: Results of Preliminary Resin Test

An 18mm PDMS square was used as a mask to cover the silicon surface as well as the electrode array. Since the device was eventually going to be used with a 17.25mm square microfluidic device, the opening was made slightly larger than the PDMS to allow for proper alignment. The slightly larger opening also allowed the PDMS to lay flat on the surface of the chip, reducing the likelihood of leaks. The Avago chip with poured resin and a PDMS microfluidic device is shown in Figure 6-9. An example of a microfluidic gradient is shown in Figure 6-10.

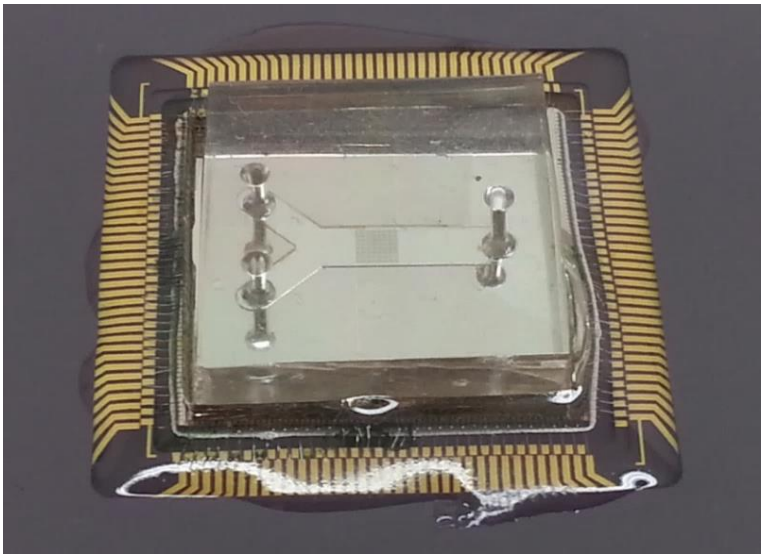

Figure 6-9: Poured Resin and Microfluidic Device on Avago Chip

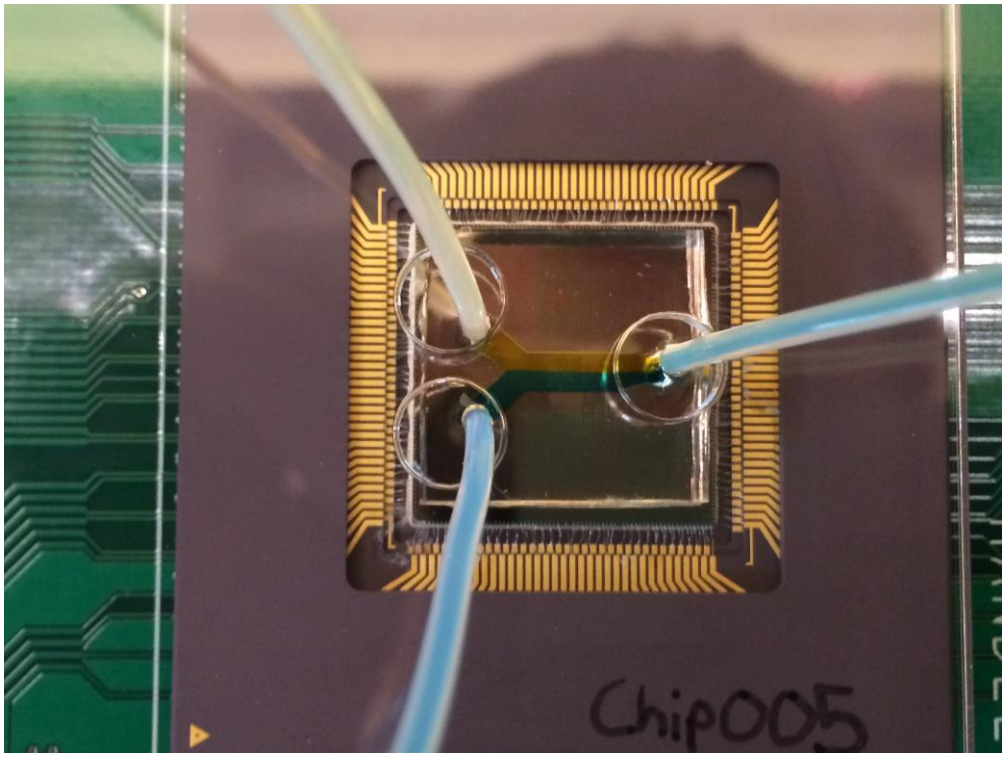

Figure 6-10: Image of Microfluidic Device Generating a Gradient on Avago Chip

Chapter 7 Discussions and Comparisons

7.1 TIA Design Conclusions

Throughout the evolution of the transimpedance amplifier designs, several trends have become apparent. Charge injection must be carefully monitored throughout the design of a transimpedance amplifier. Since the overall purpose of a TIA is to measure current, and one of the most noise-effective methods of doing this is to integrate the current on a capacitor, charge injection can significantly decrease the precision of a transimpedance amplifier.

A second trend that has become apparent is that circuits amplify small currents significantly better at lower clock rates. It is likely that this observation is due to the simple fact that operating at a slower clock rate allows more charge to accumulate, creating a voltage that is larger and an overall lower amount of noise due to switching.

An additional important parameter that has been observed throughout the course of these designs is the linearity of capacitors. If a circuit is being used to amplify a bi-directional current input (both positive and negative magnitude), it is extremely important that the integration capacitors are linear in both possible voltage directions. In the case of national's poly-poly capacitors, it was discovered that the charging characteristics weren't symmetrical. Placing two capacitors in opposite orientations in parallel in place of the original capacitor significantly helped improve the charging characteristics of the overall circuit.

Finally, low power consumption and high impedance nodes must be carefully balanced. Increasing overall impedance from the positive to negative supply rails can significantly decrease power consumption, but it can also significantly increase the effects of process variation on the

overall node voltages. Feedback and voltage stabilization techniques should always be considered when designing low-power circuits.

7.2 TIA Performance Comparison

The performance parameters of the final TIA design from section 4.4.5 were compared with a few state of the art designs, as shown in Table 7-1.

Table 7-1: Transimpedance Amplifier Performance Comparison

Work	Sharma [17]	Ferrari [18]	Razavi [19]	Salvia [20]	Zand [21]	Balasubramanian [22]	Tang [23]	**SCTIA (Simulation)**
Power	400µW	45mW @3V	30mW @3V	436µW @1.8V	30mW@ 3V	90µW@ 1.8V	3.2mW	**8.06µW@ 0.9V**
Gain	up to 25MΩ	60MΩ	8.7kΩ	56MΩ	33kΩ	150KΩ - 550KΩ	88MΩ	**50MΩ**
Spot Noise	88fA/ √Hz @ 1.6MΩ	4fA/ √Hz	n/a	65fA/ √Hz	n/a	n/a	25fA/ √Hz	**981aA/ √Hz @ 1kHz**
Avg. Noise	n/a	n/a	4.5pA/ √Hz	n/a	6.8pA/ √Hz	1.6pA/√Hz	n/a	**1.08pA/√Hz**
Area	n/a	n/a	n/a	n/a	300µm x 155µm	n/a	n/a	**93.5µm x 78.5µm**
Process	0.6µm	0.35µm	0.6µm	0.18µm	0.35µm	0.18µm	0.35µm	**0.18µm**

The overall power consumption and input referred noise currents were significantly lower than other published integrator designs. When comparing power consumption parameters, it must be considered that the design presented in this thesis didn't include features such as

variable gain or automatic gain control, and the overall bandwidth of some of the compared circuits may have been significantly higher than the bandwidth of the presented design.

Chapter 8 Conclusions and Future Work

Throughout this thesis, the design evolution of an integrated low-power transimpedance amplifier was presented. The work presented also included some of the first steps toward creating a functional and effective integrated electrode array for simultaneous spatial and temporal electrochemical detection.

The final circuit design proposed in this thesis was able to meet the design goals required the overall biosensor system. A comparison of the design goals and the achieved specifications is shown in Table 8-1. The final transimpedance amplifier design achieved a low input current noise floor with sufficient gain, with an overall power consumption of less than 10µW.

Specification	Target	Achieved
Gain (Standalone)	As high as possible	5MΩ
Signal Bandwidth	1kHz	>2kHz
Supply Voltage	900mV (Split rail +/- 450mV)	900mV (Split rail +/- 450mV)
Input Referred Noise	Minimal	981aA/$\sqrt{Hz}$
Power Consumption	Minimal	9.08µW
Silicon Area	Minimal	93.5µm x 78.5µm

Table 8-1: Design Goals vs. Achieved Values

All of the components necessary for a working overall biosensor array system have been created in this project. The primary focus of future work should be put toward refining the performance of the individual circuits as well as improving the overall integration of the electronics system. With these improvements, a novel, high-performance biosensor system can be achieved.

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Appendix A: Ocean Scripts for Inverter-Based Op-Amp FOM Optimization

Ocean Script for Inverter Sizing

```
simulator( 'spectre )
design(
"/home/rselby/simulation/inv_test_ocean/spectre/schematic/netlist/netlist")
resultsDir( "/home/rselby/simulation/inv_test_ocean/spectre/schematic" )
modelFile(

'("/space/analog_design_DB/national_semi_cadence/NSCmodels/spectre_current/ty
p_cmos9t5v/cmos9t5v_definition.scs" "")

'("/space/analog_design_DB/national_semi_cadence/NSCmodels/spectre_current/ty
p_cmos9t5v/cmos9t5v_corner.scs" "")
)
analysis('dc ?saveOppoint t  ?param "pWidth"  ?start "220n"
            ?stop "50u"  )
desVar(       "pLength" 250n  )
desVar(       "pWidth" 1u     )
envOption(
      'analysisOrder  list("dc" "ac")
)
temp( 27 )
run()
selectResult( 'dc )
plot(getData("/diode_connected_out") )
\4\5\0mV_crossing = cross(v("/diode_connected_out" ?result "dc-dc") 0.45 1
"either" nil nil)
plot( \4\5\0mV_crossing ?expr '( "450mV_crossing" ) )
```

Ocean Script for OTA Optimization

```
simulator( 'spectre )
design( "inv_opamp_testlib_willy" "inv_opamp_fully_differential_ocean"
"schematic")
cellview = dbOpenCellViewByType("inv_opamp_testlib_willy"
"inv_opamp_fully_differential_ocean" "schematic" "" "r")
modelFile(

'("/space/analog_design_DB/national_semi_cadence/NSCmodels/spectre_current/ty
p_cmos9t5v/cmos9t5v_definition.scs" "")

'("/space/analog_design_DB/national_semi_cadence/NSCmodels/spectre_current/ty
p_cmos9t5v/cmos9t5v_corner.scs" "")
)
```

```
;;Functions needed to change W/L in devices
load("/home/willyw/OceanScripts/CCSinvokedCdfCallbacks.il")
load("/home/willyw/OceanScripts/changeCDF.il")

;load("/home/willyw/OceanSizingData/InverterSizingData/Final/700mV_vdd/0.5vdd
/0.5vdd_1.5um_length.csv")
load("/home/willyw/OceanTest/0.5vdd_1.5um_length.csv.pp.pp")
load("/home/willyw/OceanTest/1.5uTail700mV.csv.pp.pp")

xcorner_full_l = list("typ,27")

supply = 0.7;

analysis('ac ?start "1"  ?stop "10G"  )
analysis('dc ?saveOppoint t  )
analysis('tran ?stop "2m"  ?errpreset "conservative"  )
desVar(  "amp" 1u     )
;desVar(         "compCap" 0  )
desVar(  "f" 1k       )
desVar(  "load" 1p    )
desVar(  "supply" 0.7)
desVar(  "vinDC" 350m )
envOption(
       'analysisOrder  list("dc" "tran" "ac")
)
save( 'i "/vSupply/MINUS" )
temp( 27 )

foreach(isize xsize_l
       parsedi        = parseString(isize ",")
       printf("%s" isize)
       in_nWidth      = evalstring(nthelem(1 parsedi))
       in_nLength     = evalstring(nthelem(2 parsedi))
       in_pWidth      = evalstring(nthelem(3 parsedi))
       in_pLength     = evalstring(nthelem(4 parsedi))

       foreach(xsize xsize_l
              ;nWidth,nLength,pWidth,pLength,Power,Current
              parsed  = parseString(xsize ",")
              nWidth  = evalstring(nthelem(1 parsed))
              nLength = evalstring(nthelem(2 parsed))
              pWidth  = evalstring(nthelem(3 parsed))
              pLength = evalstring(nthelem(4 parsed))

              foreach(tsize tsize_l
                     parsed2        = parseString(tsize ",")
                     nTailWidth     = evalstring(nthelem(1 parsed2))
                     nTailLength = evalstring(nthelem(2 parsed2))
                     pTailWidth     = evalstring(nthelem(3 parsed2))
                     pTailLength = evalstring(nthelem(4 parsed2))

                     if(nWidth > 0 then

                            ;Create variables to hold length and width data for FETs
                            sprintf(neg_input_p_w "%g" in_pWidth)
                            sprintf(neg_input_p_l "%g" in_pLength)
                            sprintf(neg_input_n_w "%g" in_nWidth)
                            sprintf(neg_input_n_l "%g" in_nLength)
                            sprintf(pos_input_p_w "%g" in_pWidth)
                            sprintf(pos_input_p_l "%g" in_pLength)
                            sprintf(pos_input_n_w "%g" in_nWidth)
                            sprintf(pos_input_n_l "%g" in_nLength)

                            sprintf(neg_load_p_w "%g" pWidth)
                            sprintf(neg_load_p_l "%g" pLength)
                            sprintf(neg_load_n_w "%g" nWidth)
                            sprintf(neg_load_n_l "%g" nLength)
```

```
                                sprintf(pos_load_n_w "%g" nWidth)
                                sprintf(pos_load_n_l "%g" nLength)
                                sprintf(pos_load_p_w "%g" pWidth)
                                sprintf(pos_load_p_l "%g" pLength)

                                sprintf(tail_p_w "%g" pTailWidth)
                                sprintf(tail_p_l "%g" pTailLength)
                                sprintf(tail_n_w "%g" nTailWidth)
                                sprintf(tail_n_l "%g" nTailLength)

                                ;Change lengths and widths.
                                changeCDF(cellview "neg_input_p" "w" neg_input_p_w)
                                changeCDF(cellview "neg_input_p" "l" neg_input_p_l)
                                changeCDF(cellview "neg_input_n" "w" neg_input_n_w)
                                changeCDF(cellview "neg_input_n" "l" neg_input_n_l)
                                changeCDF(cellview "pos_input_p" "w" pos_input_p_w)
                                changeCDF(cellview "pos_input_p" "l" pos_input_p_l)
                                changeCDF(cellview "pos_input_n" "w" pos_input_n_w)
                                changeCDF(cellview "pos_input_n" "l" neg_input_n_l)

                                changeCDF(cellview "neg_load_p" "w" neg_load_p_w)
                                changeCDF(cellview "neg_load_p" "l" neg_load_p_l)
                                changeCDF(cellview "neg_load_n" "w" neg_load_n_w)
                                changeCDF(cellview "neg_load_n" "l" neg_load_n_l)
                                changeCDF(cellview "pos_load_p" "w" pos_load_p_w)
                                changeCDF(cellview "pos_load_p" "l" pos_load_p_l)
                                changeCDF(cellview "pos_load_n" "w" pos_load_n_w)
                                changeCDF(cellview "pos_load_n" "l" neg_load_n_l)

                                changeCDF(cellview "neg_load_cross_p" "w" neg_load_p_w)
                                changeCDF(cellview "neg_load_cross_p" "l" neg_load_p_l)
                                changeCDF(cellview "neg_load_cross_n" "w" neg_load_n_w)
                                changeCDF(cellview "neg_load_cross_n" "l" neg_load_n_l)
                                changeCDF(cellview "pos_load_cross_p" "w" pos_load_p_w)
                                changeCDF(cellview "pos_load_cross_p" "l" pos_load_p_l)
                                changeCDF(cellview "pos_load_cross_n" "w" pos_load_n_w)
                                changeCDF(cellview "pos_load_cross_n" "l" neg_load_n_l)

                                changeCDF(cellview "p_tail" "w" tail_p_w)
                                changeCDF(cellview "p_tail" "l" tail_p_l)
                                changeCDF(cellview "n_tail" "w" tail_n_w)
                                changeCDF(cellview "n_tail" "l" tail_n_l)

                                ;Invoke callbacks
                                ;CCSinvokeCdfCallbacks( cellview )

                                ;Check and save
                                schCheck(cellview)
                                dbSave(cellview)

                                ;Generate netlist
                                createNetlist(?recreateAll t ?display 'nil)

                                foreach(xcorner_full xcorner_full_l

                                        parsed = parseString(xcorner_full ",")
                                        xcorner = nthelem(1 parsed)
                                        xtemp = nthelem(2 parsed)

                                        sprintf(path
"/home/willyw/OceanSimdata/Inv_Opamp_char/%g_%g_%g_%g_%g_%g_%g_%g_%g_%g_%g_%g_%g_%s_%s" in_nWidth
in_nLength in_pWidth in_pLength nWidth nLength pWidth pLength nTailWidth nTailLength pTailWidth
pTailLength supply xcorner xtemp)
                                        resultsDir(path)

                                        run()

                                        printf("PATH=%s\n" path)
                                )
                        ) ;foreach xcorner
                ) ;if
```

```
      ) ;foreach size
)
;load("mir_cas_verify_nch_dataOrig.ocn");
;load("mir_cas_verify_nch_data_short.ocn");
```

Script for Extracting Data from Inverter Opamp Simulations

```
p1 = outfile("/home/willyw/OceanSimdata/1.5u_700mV_vdd.txt" "w")

output_name_string = "in_nWidth in_nLength in_pWidth in_pLength load_nWidth
load_nLength load_pWidth load_pLength tail_nWidth tail_nLength tail_pWidth
tail_pLength current Vout VDD Power GBW Load FOM"

;fprintf(p1 "Extracted on: %s\n" getCurrentTime())
fprintf(p1 "%s\n" output_name_string)

load("/home/willyw/OceanSimdata/Inv_Opamp_char.txt")

foreach(sim sim_l

      parsed = parseString(sim "_")
      in_nWidth   = nthelem(1 parsed)
      in_nLength  = nthelem(2 parsed)
      in_pWidth   = nthelem(3 parsed)
      in_pLength  = nthelem(4 parsed)
      load_nWidth = nthelem(5 parsed)
      load_nLength= nthelem(6 parsed)
      load_pWidth = nthelem(7 parsed)
      load_pLength= nthelem(8 parsed)
      tail_nWidth = nthelem(9 parsed)
      tail_nLength= nthelem(10 parsed)
      tail_pWidth = nthelem(11 parsed)
      tail_pLength= nthelem(12 parsed)
      VDD               = nthelem(13 parsed)
      ;still need  - (current Power GBW Load FOM)"
      sprintf(path "/home/willyw/OceanSimdata/Inv_Opamp_char_8Multiple/%s"
sim)
      printf("sim - %s\n" path)
      openResults(path)

      selectResult("dcOp-dc")
      Vout  = v("voutn" ?result "dcOp-dc")
      selectResult("dcOpInfo-info")
      current = (pv("vSupply" "i" ?result "dcOpInfo-info")*-1)
      Power = (pv("vSupply" "pwr" ?result "dcOpInfo-info")*-1)
      Load  = pv("C0" "cap" ?result "dcOpInfo-info")

      selectResult("ac-ac")
      GBW         = unityGainFreq(v("voutn" ?result "ac-ac")/v("vinn" ?result
"ac-ac"))
      FOM         = (pv("C0" "cap" ?result "dcOpInfo-
info")*unityGainFreq(v("voutn" ?result "ac-ac")/v("vinn" ?result "ac-
ac"))*10E2)/(i("vSupply:p" ?result "dcOp-dc")*(-1))
      ;                             1  2  3  4  5  6  7  8  9 10 11 12 13 14
15 16 17 18 19
```

```
      sprintf(outstring "%s %s %s %s %s %s %s %s %s %s %s %s %g %g %s %g %g
%g %g" in_nWidth in_nLength in_pWidth in_pLength load_nWidth load_nLength
load_pWidth load_pLength tail_nWidth tail_nLength tail_pWidth tail_pLength
current Vout VDD Power GBW Load FOM)
      ;printf("%s\n" outstring)
      fprintf(p1 "%s\n" outstring)

)

close(p1)
```

Appendix B: Matlab Code for Data

Acquisition

```
function varargout = PlotVoltage(varargin)
% PLOTVOLTAGE M-file for PlotVoltage.fig
%      PLOTVOLTAGE, by itself, creates a new PLOTVOLTAGE or raises the
existing
%      singleton*.
%
%      H = PLOTVOLTAGE returns the handle to a new PLOTVOLTAGE or the handle
to
%      the existing singleton*.
%
%      PLOTVOLTAGE('CALLBACK',hObject,eventData,handles,...) calls the local
%      function named CALLBACK in PLOTVOLTAGE.M with the given input
arguments.
%
%      PLOTVOLTAGE('Property','Value',...) creates a new PLOTVOLTAGE or
raises the
%      existing singleton*.  Starting from the left, property value pairs are
%      applied to the GUI before PlotVoltage_OpeningFcn gets called.  An
%      unrecognized property name or invalid value makes property application
%      stop.  All inputs are passed to PlotVoltage_OpeningFcn via varargin.
%
%      *See GUI Options on GUIDE's Tools menu.  Choose "GUI allows only one
%      instance to run (singleton)".
%
% See also: GUIDE, GUIDATA, GUIHANDLES

% Edit the above text to modify the response to help PlotVoltage

% Last Modified by GUIDE v2.5 15-Nov-2013 12:03:44

% Begin initialization code - DO NOT EDIT
gui_Singleton = 1;
gui_State = struct('gui_Name',       mfilename, ...
                   'gui_Singleton',  gui_Singleton, ...
                   'gui_OpeningFcn', @PlotVoltage_OpeningFcn, ...
                   'gui_OutputFcn',  @PlotVoltage_OutputFcn, ...
                   'gui_LayoutFcn',  [] , ...
                   'gui_Callback',   []);
if nargin && ischar(varargin{1})
    gui_State.gui_Callback = str2func(varargin{1});
end

if nargout
    [varargout{1:nargout}] = gui_mainfcn(gui_State, varargin{:});
else
    gui_mainfcn(gui_State, varargin{:});
```

```
end
% End initialization code - DO NOT EDIT


% --- Executes just before PlotVoltage is made visible.
function PlotVoltage_OpeningFcn(hObject, eventdata, handles, varargin)
% This function has no output args, see OutputFcn.
% hObject    handle to figure
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)
% varargin   command line arguments to PlotVoltage (see VARARGIN)

% Choose default command line output for PlotVoltage
handles.output = hObject;

% Initialize the "loopflag" field of the handles structure
handles.loopflag = false;

% Initialize the "haschannels" field of the handles structure
handles.haschannels = false;

% Initialize the "smooth100flag" field of the handles structure
handles.smoothpts = 0;

handles.ai_device0 = analoginput('mwadlink', 0);% Opens the analog input
functionality
handles.ai_device1 = analoginput('mwadlink', 1);% Opens the analog input
functionality

set(handles.ai_device0,'SampleRate', 10000);
set(handles.ai_device0,'SamplesPerTrigger', 100);
set(handles.ai_device0,'TriggerType', 'Immediate');
set(handles.ai_device0,'TriggerCondition', 'None');

set(handles.ai_device1,'SampleRate', 10000);
set(handles.ai_device1,'SamplesPerTrigger', 100);
set(handles.ai_device1,'TriggerType', 'Immediate');
set(handles.ai_device1,'TriggerCondition', 'None');
% Update handles structure
guidata(hObject, handles);

% UIWAIT makes PlotVoltage wait for user response (see UIRESUME)
% uiwait(handles.figure1);



% --- Outputs from this function are returned to the command line.
function varargout = PlotVoltage_OutputFcn(hObject, eventdata, handles)
% varargout  cell array for returning output args (see VARARGOUT);
% hObject    handle to figure
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% Get default command line output from handles structure
```

```
varargout{1} = handles.output;


% --- Executes on button press in start_pushbutton.
function start_pushbutton_Callback(hObject, eventdata, handles)
% hObject    handle to start_pushbutton (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% If we are already looping, exit early so that only one
% copy of the loop is executing
if handles.loopflag
    return;
end

%if ~handles.haschannels
%    return
%end


%plot(handles.axes1, xaxis, data);

count = 1;
% Set the flag, refresh the figure's GUIDATA to match "handles"
handles.loopflag = true;
guidata(hObject, handles);
data = [];

%cla(handles.axes1);

% On each loop check whether the flag has been reset
set(findall(handles.ChannelSelPanel, '-property', 'enable'), 'enable', 'off')
while handles.loopflag

    start(handles.ai_device0);
    wait(handles.ai_device0,30);
    data = [data; getdata(handles.ai_device0)];
    %data = [data; getsample(handles.ai_device0)];
    %xaxis(count) = count;

    %plot(xaxis,smooth(data,1000));
    %plot(handles.axes1, x, y);

    if handles.smoothpts == 0
        plot(handles.axes1, data);
    else
        plot(handles.axes1,
reshape(smooth(data,handles.smoothpts),size(data)));
    end

    %plot(handles.axes1, xaxis, data);
    %set(handles.axes1, ...
    %'YLim', [-2.5 2.5]);
    count = count + 1;
```

```
    %hist(smooth(data,1000),100);
    drawnow;

    % DRAWNOW both allows plotting events to execute, and gives a chance
    % for other callbacks to interrupt

    % This is in case the figure is killed ("X") while the loop is running
    if ~ishandle(hObject)
        return;
    end

    % Refresh "handles" to match the figure's GUIDATA
    handles = guidata(hObject);
end
%scrollplot();
set(findall(handles.ChannelSelPanel, '-property', 'enable'), 'enable', 'on')

% --- Executes on button press in stop_pushbutton.
function stop_pushbutton_Callback(hObject, eventdata, handles)
% hObject    handle to stop_pushbutton (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% Set the flag, refresh the figure's GUIDATA to match "handles"
set(findall(handles.ChannelSelPanel, '-property', 'enable'), 'enable', 'on')
handles.loopflag = false;
guidata(hObject, handles);



% --- Executes on button press in radio10PtSmooth.
function radio10PtSmooth_Callback(hObject, eventdata, handles)
% hObject    handle to radio10PtSmooth (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% Hint: get(hObject,'Value') returns toggle state of radio10PtSmooth
handles.smoothpts = 10;
guidata(hObject, handles);

% --- Executes on button press in radio100PtSmooth.
function radio100PtSmooth_Callback(hObject, eventdata, handles)
% hObject    handle to radio100PtSmooth (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% Hint: get(hObject,'Value') returns toggle state of radio100PtSmooth
handles.smoothpts = 100;
guidata(hObject, handles);

% --- Executes on button press in radio1000PtSmooth.
function radio1000PtSmooth_Callback(hObject, eventdata, handles)
% hObject    handle to radio1000PtSmooth (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)
```

```
% Hint: get(hObject,'Value') returns toggle state of radio1000PtSmooth
handles.smoothpts = 1000;
guidata(hObject, handles);


% --- Executes on button press in radioSmooth0Pt.
function radioSmooth0Pt_Callback(hObject, eventdata, handles)
% hObject    handle to radioSmooth0Pt (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% Hint: get(hObject,'Value') returns toggle state of radioSmooth0Pt
handles.smoothpts = 0;
guidata(hObject, handles);


% --- Executes on button press in TestAqButton.
function TestAqButton_Callback(hObject, eventdata, handles)
% hObject    handle to TestAqButton (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)
%%getsample(handles.ai_device)
handles.ai_device0
handles.ai_device1

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%   Channel Box Callbacks
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% --- Executes on button press in Ch1chkbox.
function Ch1_0chkbox_Callback(hObject, eventdata, handles)
% hObject    handle to Ch1chkbox (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)

% Hint: get(hObject,'Value') returns toggle state of Ch1chkbox

%if ~handles.haschannels
%    handles.haschannels = true;
%end
if get(hObject,'Value') %if box is NOT checked
    handles.ai0_1 = addchannel(handles.ai_device0, 1);%Add channel #0 to
ai_device
    set(handles.ai0_1, 'InputRange', [-2.5 2.5]);
else                    %box is checked

end

% --- Executes on button press in Ch2_0chkbox.
function Ch2_0chkbox_Callback(hObject, eventdata, handles)
% hObject    handle to Ch2_0chkbox (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)
```

```
% Hint: get(hObject,'Value') returns toggle state of Ch2_0chkbox

if get(hObject,'Value') %if box is NOT checked
    handles.ai0_2 = addchannel(handles.ai_device0, 2);%Add channel #0 to
ai_device
    set(handles.ai0_2, 'InputRange', [-2.5 2.5]);
else

end
```