

THESIS

ADVANCED RESEARCH DEPOSITION SYSTEM (ARDS) FOR PROCESSING CdTe SOLAR CELLS

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## ABSTRACT

### ADVANCED RESEARCH DEPOSITION SYSTEM (ARDS) FOR PROCESSING CdTe SOLAR CELLS

CdTe solar cells have been commercialized at the Gigawatt/year level. The development of volume manufacturing processes for next generation CdTe photovoltaics (PV) with higher efficiencies requires research systems with flexibility, scalability, repeatability and automation. The Advanced Research Deposition Systems (ARDS) developed by the Materials Engineering Laboratory (MEL) provides such a platform for the investigation of materials and manufacturing processes necessary to produce the next generation of CdTe PV.

Limited by previous research systems, the ARDS was developed to provide process and hardware flexibility, accommodating advanced processing techniques, and capable of producing device quality films. The ARDS is a unique, in-line process tool with nine processing stations. The system was designed, built and assembled at the Materials Engineering Laboratory. Final assembly, startup, characterization and process development are the focus of this research. Many technical challenges encountered during the startup of the ARDS were addressed in this research. In this study, several hardware modifications needed for the reliable operation of the ARDS were designed, constructed and successfully incorporated into the ARDS. The effect of process condition on film properties for each process step was quantified. Process development to achieve 12% efficient baseline solar cell required investigation of discrete processing steps, troubleshooting process variation, and developing performance correlations. Subsequent to this research, many advances have been demonstrated with the ARDS. The ARDS consistently produces devices of 12%  $\pm$  0.5% by the process of record (POR). The champion cell produced to date utilizing the ARDS has an efficiency of 16.2% on low cost commercial sodalime glass and utilizes advanced films.

The ARDS has enabled investigation of advanced concepts for processing CdTe devices including, Plasma Cleaning, Plasma Enhanced Closed Space Sublimation (PECSS), Electron Reflector (ER) using Cd<sub>1-x</sub>Mg<sub>x</sub>Te (CMT) structure and alternative device structures. The ARDS has been instrumental in the collaborative research with many institutions.

## ACKNOWLEDGEMENTS

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I want to thank Jim Sites for your contribution my knowledge of PV physics and device characterization. The resources that you have established through the PV Characterization Lab, both personnel and equipment, have been instrumental to advancing the research in this study. The body of literature reflecting your contribution to the field is respectable and highly valuable.

For his personal commitment to my success, for always having great advice, and for supporting the opportunity to pursue this degree, I cannot thank Anders Olsson enough. You have demonstrated excellence in leadership that I hope to eventually achieve.

For the opportunity to make a contribution to the PV field, I give many thanks to Dr. Sampath, Kurt Barth and Al Enzenroth. The Materials Engineering Lab and Abound Solar have been most profound in defining who I am as a professional. The members of the MEL and Abound Solar demonstrated great confidence in my abilities and reciprocated great knowledge and guidance, without their support this research would not have been possible.

The success of the ARDS has been achieved only by the hard work of many. The members of the MEL, Paul Kobayakov, Jason Kephart, Drew Swanson, and Kevin Walters supported diverse activities to successfully bring the ARDS into the current state of operation. The R&D team at Abound Solar including Nathan Schuh, Alan Davies, Nicole Landou, Richard Hafer, Nirav Vora, Kishore Kamath and Anders Olsson .provided critical support, experience, interpretation and guidance necessary to the success of this research. Neil Scofield and Steven Barnes were vital to the rapid production of small area devices (SAD) and Lei Chen for supporting measurement equipment and characterization requests. I thank Bill Yates for support and training on the operation of microscopy techniques used for this research. The members of the PV characterization lab, specifically Russel Geisthardt, Valerie Jacobson, Tyler McGoffin, John Raguse, and Katherine Zaunbrecher have provided pertinent device characterization and analytical interpretation. Pat McCurdy and Den Heyes of the CSU Central Instrumentation Facility provided training of advanced material characterization techniques.

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## CHAPTER 1: INTRODUCTION AND MOTIVATION

### 1.1 Why Renewable Energy?

Directly converting sunlight to electricity by means of the photovoltaic effect is the most elegant form of energy conversion. As the global community recognizes the limited resources and detrimental effects of conventional fossil energy, additional efforts will be made to utilize renewables. Trends indicate global energy demands will increase 56%, with fossil fuels accounting for 80% of energy production, and increased CO<sub>2</sub> emissions of 46% by 2040 [1]. According to the US Energy Information Administration (EIA), future US electricity generation by non-hydropower renewables will nearly double by 2040 as indicated in Figure 1-1 [2].

Solar energy presents a viable alternative source of energy to meet the global energy and environmental demands. An increase in non-hydro power renewables is expected as new technologies demonstrate increased efficiency, and reduced manufacturing costs. The depletion of easily accessible fossil fuel resources will drive energy costs upward, and stimulate popular interest in sustainable energy technologies. As we move towards a globally modernized and expanding population, supplying the global energy demands will continue to be a significant challenge. Figure 1-2 demonstrates the exponential energy consumption, even as population growth starts to stabilize. The need to balance current energy practices with renewable resources is critical for achieving a sustainable energy future.

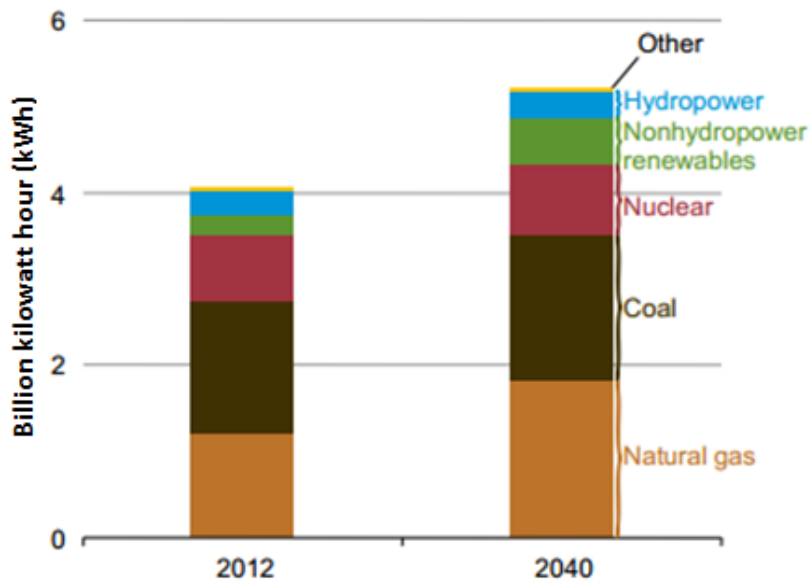


Figure 1-1: Total U.S. electricity generation by energy source, 2012 and 2040. [2]

## World Population & Energy Demand Growth

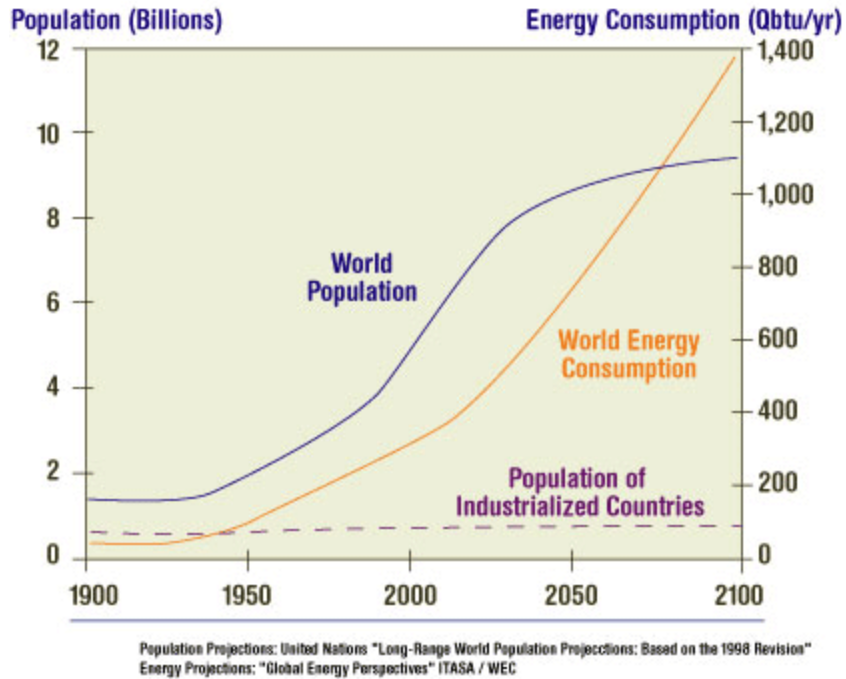


Figure 1-2: World population and energy demand growth. [3]

A sustainable energy portfolio would include a blend of renewable technologies such as wind, hydro, bio and solar in addition to limited fossil fuel and nuclear sources. Annual global installations of new PV expanded between significantly from 2000-2011, as presented in Figure 1-3. The EIA predicts electricity generation from renewables to nearly double by 2040, with an increasing renewable generating capacity resulting from solar as seen in Figure 1-4 respectively. While it is accepted that most renewable technologies have energy production limitations due to variation in environmental conditions, the ability to offset peak demands is significant.

Solar photovoltaic technologies are well suited to be installed at point of use in residential and commercial space, and are becoming common among dual purpose shade structures and commercial rooftop installations. Photovoltaics are ideal for these applications due to the simplicity, versatility, reliability, and low environmental impact of installations. Large utility installations are becoming more popular in the arid southwest where the land is not suitable for agriculture, but has excellent solar resources [4]. With the development of the smart grid and advancements in the electrical distribution infrastructure, renewable energy integration will become increasingly manageable [5] In addition to the improvements in grid transmission; integration of renewable technologies into construction has opened new venues previously too valuable for low density energy production [6]. Capitalizing on the available solar resources would enable practical diversification of the global energy portfolio.

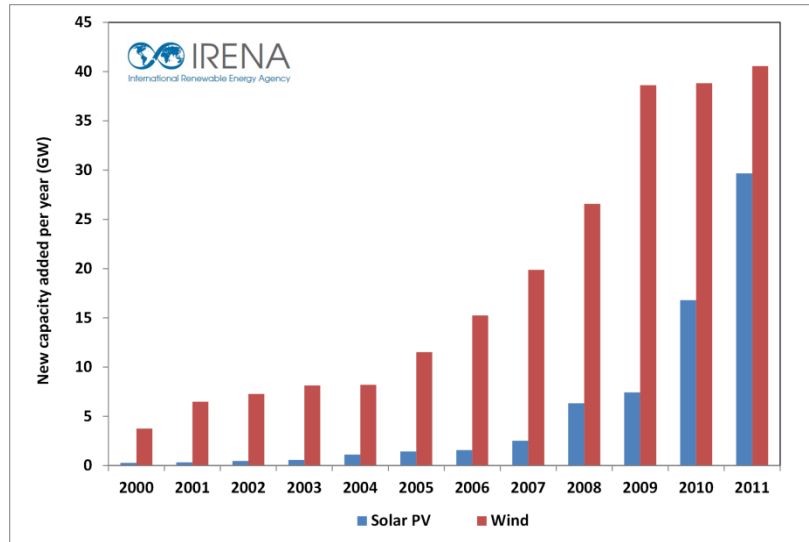


Figure 1-3: Global annual new installed capacity of solar PV and wind, 2000-2011 [7]

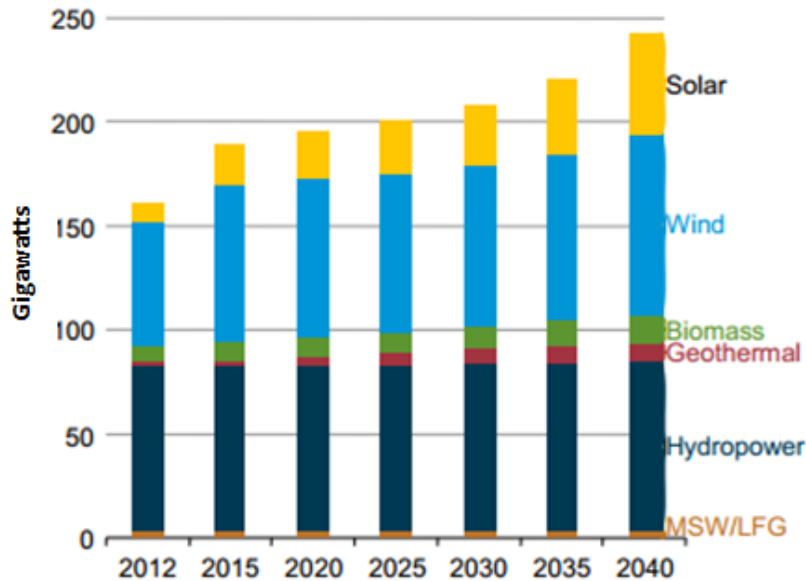


Figure 1-4: Predicted renewable electricity generating capacity by energy source. [2]

With reductions in manufacturing costs, improvements to conversion efficiency, and public acceptance, photovoltaics will become an important source of economical premium-quality power. Trends tell us that module and balance of systems (BOS) costs will continue to diminish with increased capacity and improved technologies. The Department of Energy (DOE) launched the SunShot Initiative to stimulate the revitalization of photovoltaics research by the private sector after continued decreases in the market share of solar manufacturing. The SunShot program has a target cost of electricity from PV systems of \$.06 per kilowatt-hour (kWh) by 2020; effectively achieving grid parity, and making solar a sustainable industry without subsidies. While the program is just a few

years old, it has already accomplished a 60% reduction in the cost of utility-scale systems [8]. Market trends demonstrate the significant reduction in the cost per watt (\$/watt) of module pricing as seen in Figure 1-5, which directly affects the residential and utility system costs.



Figure 1-5: Price forecasts of solar system; forecast with post 2008 curve. Figure reproduced from [7]

## 1.2 Fundamentals of a Solar Cell

When one or more semiconductor materials are joined to form a p-n diode, a solar cell is created. A solar cell converts light photons to electrical current through the photovoltaic effect. Using solar photovoltaics to transforming just a fraction of the solar energy reaching the earth would have a significant impact on the energy picture.

Sunlight is a portion of the electromagnetic radiation emitting from the sun. We define sunlight as a spectrum of discrete units of energy called photons, whose energy is based on wavelength. Light reaching the earth has a spectral distribution that affects the potential efficiency of a solar cell. The spectrum as measured at the edge of the earth's atmosphere is considered the solar constant of air mass zero (AM0). As the radiation passes through earth's atmosphere, it interacts with gases and aerosols that cause significant losses due to absorption, reflection and scattering. The spectrum incident on a surface at sea level with a zenith angle of 37deg, is denoted air mass 1.5 global (AM1.5g), and has a normalized intensity of 1,000 W/m<sup>2</sup> [9]. This distribution accounts for both diffuse and direct irradiance, as solar cells are effective at converting both. The AM1.5 spectral distribution is recognized as the standard for terrestrial characterization.

# Solar Radiation Spectrum

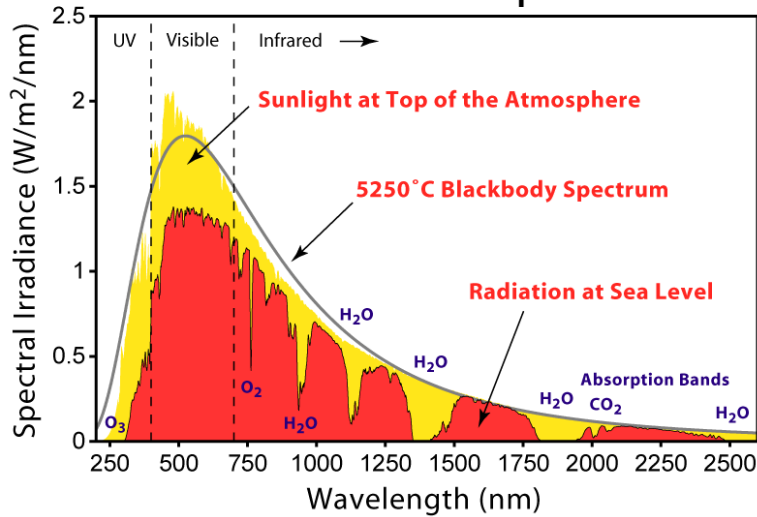


Figure 1-6: The AM1.5 global solar radiation spectrum. [9] [10]

Only photons with energy higher than the band gap of the semiconductor are absorbed and contribute to the generation of electrical energy. The band gap of a direct-gap semiconductor is the difference in energy between the top of the valence band and the bottom of the conduction band, defining the energy necessary to generate an electron-hole pair. Figure 1-7 represents the band diagram of a basic single junction solar cell under illumination. The Shockley-Queisser model, predicts the efficiency limits for p-n junction solar cells using the  $E_g$  of the absorber layer. Graphically represented in Figure 1-8, one can see the ideal theoretical conversion efficiency of CdTe solar devices.

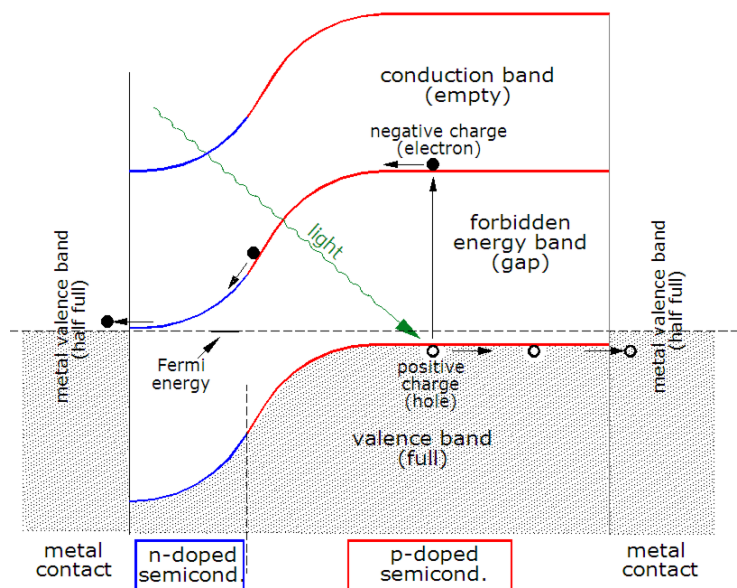


Figure 1-7: Illuminated band diagram of single junction solar cell. [11]

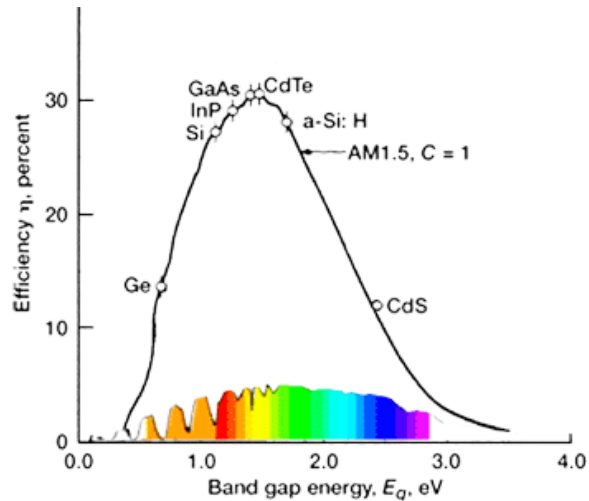


Figure 1-8: Shockley-Queisser efficiency limit of single junction solar cells. [12] [13]

A p-n heterojunction is established when different p-type and n-type semiconductors are joined. As demonstrated in Figure 1-9, carriers immediately diffuse across the junction resulting ionized atoms and establishing neutral regions of fixed charge. This space charge region becomes depleted of both electrons and holes, producing a built in field that acts as a barrier to the further drift of majority carriers and presents a low resistance path to minority carriers. With illumination, the built in field causes charge separation, driving electrons to the n-side and holes to the p-side inducing photo-generated current and performing work when attached to an external load.

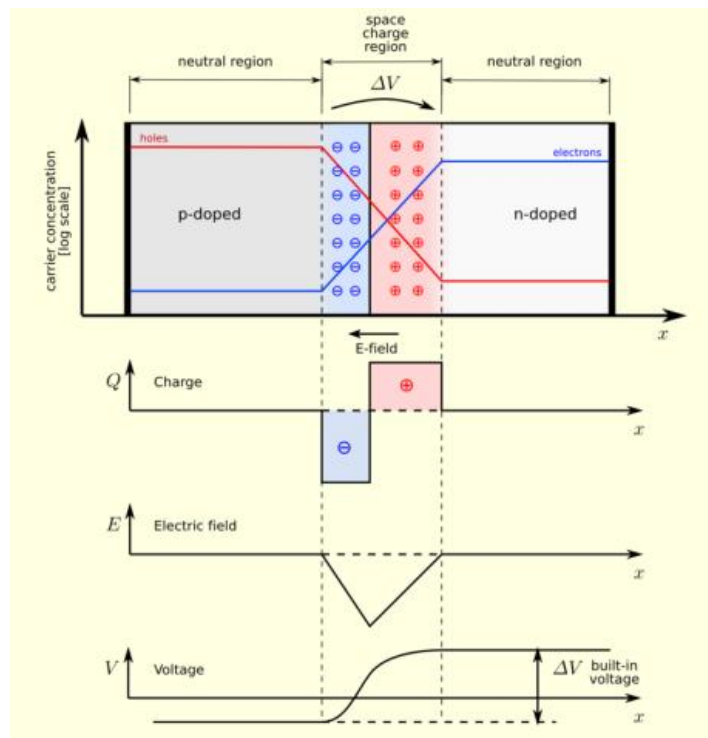


Figure 1-9: Development of the space charge region for heterojunction solar cell. [14]

Hetero-junctions are limited by the formation of interface states which work to trap charges at the junction, reducing the built in voltage. A quantifiable performance gap exists between lab and ideal efficiencies, related to open circuit voltage ( $V_{oc}$ ), Fill-Factor (FF), and short circuit current ( $J_{sc}$ ). Performance losses due to these parameters are well explained by Sites and others [15] [16]. Developing better correlations between process, performance and structure should allow improvements to all parameters. The performance gap between lab and commercial efficiencies are expected to reduce as advanced manufacturing techniques are achieved to improve window layers, uniformity and cell interconnections.

### 1.3 CdS/CdTe Solar cell

Solar cells are formed through the assembly of n-type and p-type semiconductor layers. Thin film structures are formed directly on substrates consisting of polymers, glass, metal or ceramics. Solar devices may be produced in either a superstrate or substrate configuration depending on process and application. A superstrate configuration is most common for fabrication ease and encapsulation quality. In this configuration the incident light first passes through the substrate before being absorbed in the photojunction. This structure requires the use of a highly transparent substrate, and transparent conductive oxide layer (TCO).

Terrestrial solar applications have an optimal bandgap of  $\sim 1.5\text{eV}$  [17] [13]. Selection of a material system for large scale applications is based on potential device efficiency and manufacturing costs resulting the metric of  $\$/\text{kWh}$ . The use of CdTe is attractive as it is a direct gap semiconductor with a bandgap of  $\sim 1.45\text{eV}$ , and high absorption coefficient. These qualities result high conversion efficiencies of wavelengths up to  $\sim 810\text{nm}$  with absorber layers of  $\sim 2\mu\text{m}$  thickness. The typical heterojunction CdTe device utilizes an n-type CdS window layer with a band gap of  $\sim 2.42\text{eV}$ . This wide bandgap allows transmission of wavelengths greater than  $\sim 510\text{nm}$  when thin layers are used.

Various techniques for manufacture of CdS/CdTe thin film solar cells are possible, including chemical bath deposition (CBD), closed space sublimation (CSS), physical vapor deposition (PVD) and vapor transport deposition (VTD). Both CdS and CdTe are well suited to closed space sublimation (CSS). Films grown by CSS have many advantages over low temperature processes; producing excellent microstructure, and device performance when treated with a high temperature  $\text{CdCl}_2$  process. High volume manufacturing benefits of CSS include high deposition rates, large area uniformity, and excellent material utilization. Record device efficiencies have been

produced by CSS and VTD techniques. The CdTe solar cell described herein is produced using a novel heated pocket deposition (HPD), a variation of closed space sublimation (CSS).

#### 1.4 State of the Technology/Structure

Significant advancements in performance and cost reduction have been accomplished in thin film solar spurring increased installations, especially at the utility scale. First Solar is currently the leading global provider of solar systems utilizing CdTe thin film with more than 8GW installed worldwide. Reported by NREL, the historical research-cell efficiency records are presented in Figure 1-10. Significant progress has been made in field of thin film CdTe technologies since 2011. In February 2014, First Solar announced a record setting research cell of 20.4%, besting its previous of 19.6%. This accomplishment matches the multicrystalline Si research cell efficiency, which are nearing ultimate entitlements. In 2009, First Solar became the first solar panel manufacturing company to lower its manufacturing cost to \$1 per watt. This Arizona based Auga Caliente solar project demonstrates electricity production at \$0.06/kWh, near grid parity. It is one of the largest operational PV power plants in the world (Figure 1-11), with a generating capacity of 290MWp of alternating current [18].

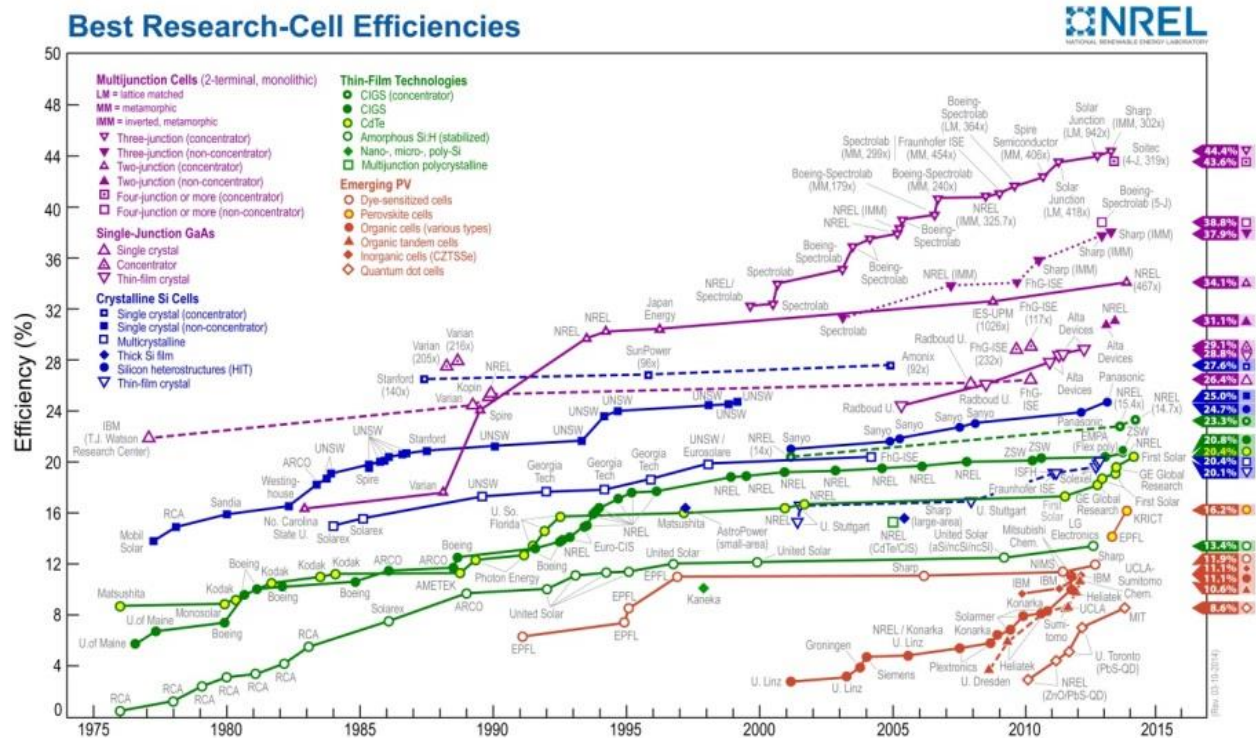


Figure 1-10: Best Research-Cell Efficiencies, NREL [19]





Figure 1-11: Agua Caliente solar farm, First Solar [20]

## 1.5 Roadmap of Research

There are many approaches currently under investigation for improving the efficiency of CdTe solar devices. The focus at the Colorado State University Materials Engineering Laboratory (MEL) is that of volume manufacturing techniques. Target objectives are improvements to the window layer transmission, reducing bulk recombination, improving back contact quality and the development of the electron reflector.

Working closely with the Colorado State University Electric Propulsion and Plasma Engineering Lab (CEPPE), incorporation of plasma enhancing techniques for the preparation and deposition of films are being investigated. Exposure of the TCO to low energy plasma just prior to deposition has shown to reduce shunting defects and improve material density [21] [22]. Plasma Enhanced Close Space Sublimation (PECSS) has been demonstrated for improving species incorporation during deposition and benefits film uniformity. The novel hollow cathode concept can be readily incorporated in existing systems and has been tested in large format and volume production environments. Both of these techniques enable thinning of the CdS window layer, increasing blue spectrum response and current densities [23]. Broadening of the CdS bandgap can reduce absorption losses in the window layer. In addition to PECSS, sputtering CdS in the presence of Oxygen to form CdS:O has been demonstrated [24].

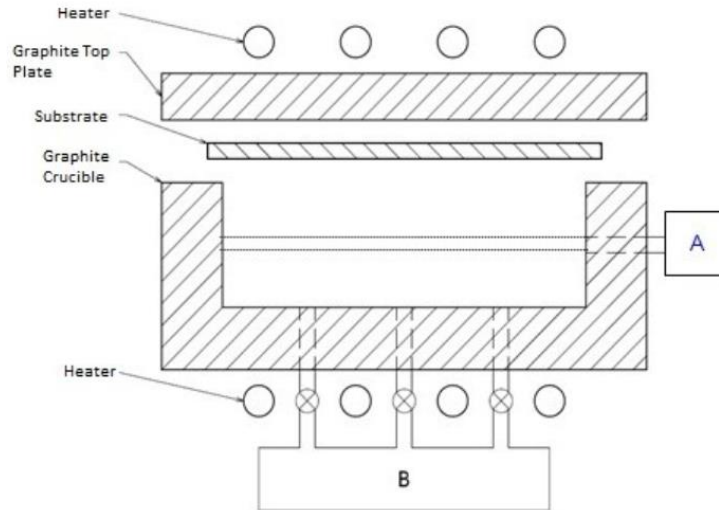


Figure 1-12: HPD Co-sublimation source used for CMT (B) with PECSS (A).

Another area of research is in creating a layer of  $Cd_{1-x}Mg_xTe$  (CMT) at the back of the absorber, that would lead to the formation of an electron reflector at the back of the current structure [25] [26]. Multiple techniques for depositing the absorber layer, including the HPD co-sublimation source (Figure 1-12) developed at the MEL. Preliminary results demonstrate feasibility of creating a higher band gap material by means of co-sublimation, and are accordingly a focused effort. The roadmap of the Materials Engineering Laboratory and National Science Foundation Next Generation Photovoltaics Industry/University Center for Research Collaboration (I/UCRC) to pursue higher efficiency through incorporation of sputtered CdS:O and multiple-junction cells is presented in Figure 1-13. The devices in this study have the structure marked as current.

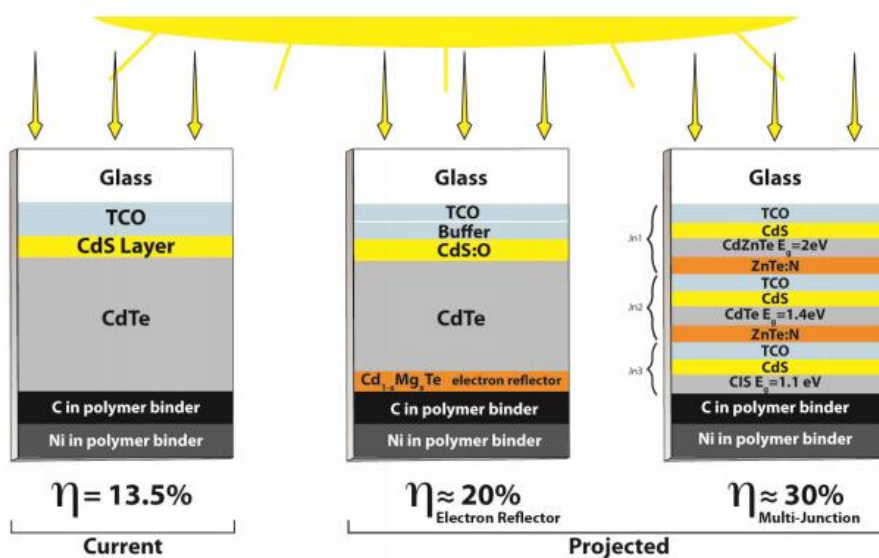


Figure 1-13: MEL and NSF I/UCRC research roadmap to high efficiency photovoltaics.

## 1.6 The Advanced Research Deposition System

The original R&D system developed at the MEL was a continuous, in-line process, transporting samples from Air to Vacuum to Air (AVA) on a continuous belt conveyor represented in Figure 1-14 [27]. The AVA system was conceived to demonstrate volume manufacturing of the thin film solar process, and eventually achieved success with the startup of Abound Solar (Formerly known as AVA Solar). The HPD process combined with a conveyor transport is suitable for production, but is limiting in all aspects of research. The AVA system utilized a multistage molecular seal instead of common load lock configurations. This necessitated specific substrate tolerances to maintain process pressure, limiting the ability to test alternative substrate geometries. There was no ability to generate partial or intermediate films while simultaneously producing full devices. As the samples were continuously exposed to the high temperature sources, motion had to be maintained. This meant that a large number of transient samples were produced between target set-points, and the potential for process drift to occur was common.

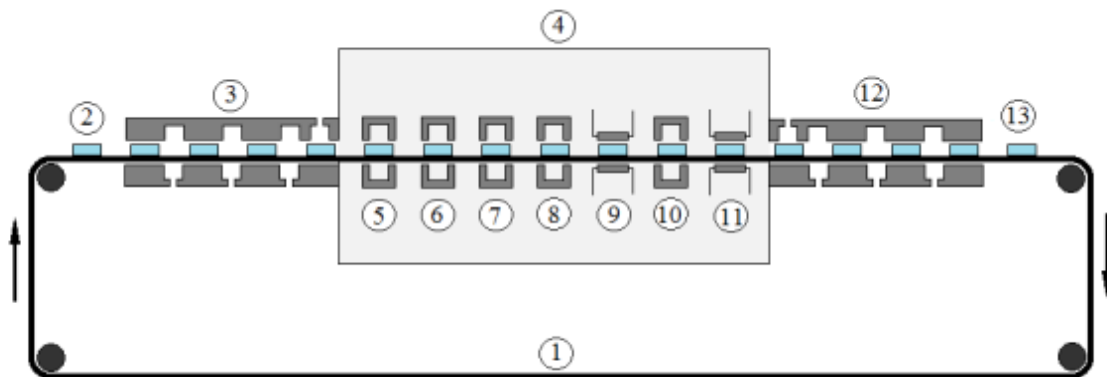


Figure 1-14: Diagram of AVA system developed at the MEL. (1) continuous conveyor belt (2) base glass substrate (3) AVA seal (4) vacuum chamber (5) substrate heating (6)CdS deposition (7)CdTe deposition (8) CdCl<sub>2</sub> deposition (9) CdCl<sub>2</sub> annealing and stripping (10) back contact formation (11) back contact annealing (12)AVA molecular seal (13) completed device

To achieve experimental flexibility, and maintaining a concept capable of volume manufacturing, an in-line research tool was necessary. Considering current and future process limitations, a linear tool configuration utilizing the well-established HPD technique was developed. The ARDS design enabled hardware and process flexibility, with the potential for future additions. The linear layout was selected for ease of sample transport and necessitated by an existing boundary limitation. The hardware was designed to be modular, providing a spatial envelope for which prototype hardware could be tested, including alternative deposition techniques. The single sample transport mechanism allows variation of substrate type, process sequence, dwell times, and the ability to generate intermediate

films for characterization. The ARDS provides a highly versatile platform for development of next generation solar cells, and key features will be presented in Chapter 3, process characterization and results discussed in Chapter 4.

### 1.7 The need for Automation of Experiments

Experimental efficiency minimizes time, resources and waste. Carefully controlling the manufacturing process is necessary to produce meaningful and repeatable results. Automation of the ARDS is accomplished by the integration of process controls through a custom Labview interface. Operators' are able to define process recipes, load a substrate, and let the machine do the rest, eliminating user variation. All valve actuation for transfer, pumping and purging is automated, minimizing disruptions to the process environment and potential damage to the equipment. Compared to the previous AVA system, the ARDS executes experimentation with significantly fewer transient samples.

### 1.8 Statement of work

The purpose of this research is the integration, startup and process development on the ARDS. In addition to the startup and process development, secondary requirements included the development of techniques for glass preparation, chemical processing and establishing chemical containment and safe practices to limit and monitor Cadmium migration and exposure. Considerable effort was put into the development of procedures and documentation necessary for the maintenance and operation of the ARDS, including training of students.

### 1.9 Supporting members

The Materials Engineering Laboratory is supported by students and faculty with diverse skills, and a passion for PV technology. Undergraduate, graduate and Ph.D. level students' research advanced concepts for improving manufacturing technologies and characterization. My peers, Paul Kobayakov, Jason Kephart, Drew Swanson, and Kevin Walters brought valuable skills to the MEL team. Paul's characterization and interpretive capacity was highly beneficial to process optimization. The focus on improved window layers by Jason and Drew, supported incremental optimization of the device structure. Jason's expertise with Labview supported automation development. Thermal modeling by Kevin provided insight to hardware improvements, and mechanical optimization. Detailed characterization of devices by Russel Geisthardt, John Raguse, Tyler McGoffin, Katherine Zaunbrecher and Jim Sites of the PV Characterization lab enhanced process to performance correlations. Their assistance was highly valuable and necessary to the success of the ARDS.

## CHAPTER 2: EXPERIMENTAL DETAILS

### 2.1 Cell Fabrication

Baseline cells are fabricated on low cost commercially available soda lime float glass with a pyrolytically deposited transparent conductive oxide (TCO) layer. The TCO is typically a fluorine-doped  $\text{SnO}_2$  layer, which serves as the front electrical contact. The ARDS is designed to utilize 3.6" x 3.1" substrates, or a high temperature carrier to facilitate smaller samples. A high temperature CSS process is used for the subsequent deposition of n-type CdS, p-type CdTe, CdCl<sub>2</sub> activation and back contact doping, resulting the device structure presented in Figure 2-1.

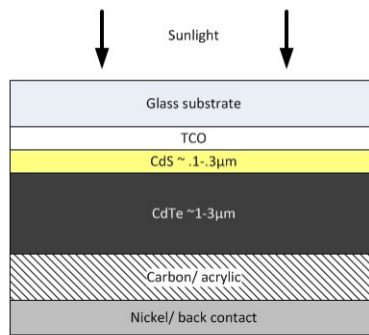


Figure 2-1: Superstrate structure of CdTe solar cells produced with ARDS.

Finished photodiodes are removed from vacuum and rinsed in deionized (DI) water to remove excess CdCl<sub>2</sub> residual. Samples are inspected and divided according to research needs, raw films are immediately desiccated or stored in an inert environment glovebox, and films to be used for solar cells are prepared with back electrode. The back contact is formed by spray application of a thin layer (~2μm) of colloidal carbon, followed by thicker layer (~100μm) of nickel particle in acrylic binder onto the exposed CdTe surface [28]. Small area devices (SAD) are formed by careful masking and abrasive blasting to define active cell regions of approximately 0.7cm<sup>2</sup> as represented in Figure 2-2.

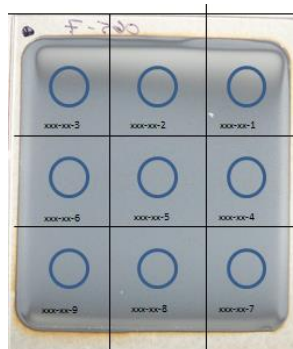


Figure 2-2: Sample division resulting 9 small area devices.

## 2.2 Film and Device Characterization

All solar cells and partial films studied in this research were generated with the ARDS. Many techniques are used to fully assess the material and the electrical characteristics of solar cells. These techniques are common to thin film characterization and are well defined in literature. The techniques used for the electrical characterization of devices are Current density-Voltage (J-V), Capacitance-Voltage (C-V), and Quantum Efficiency (QE). Techniques used to investigate discrete film properties are UltraViolet- Visible spectroscopy (UV-Vis), Profilometry, Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM), X-ray Photoelectron Spectroscopy (XPS), X-ray Diffraction (XRD), X-ray Fluorescence (XRF). Advanced device and film characterization by Photo-Luminescence (PL), Electro-Luminescence (EL) and Time Resolved Photo-Luminescence (TRPL) are used to evaluate defect state and minority carrier lifetime. This suite of techniques is used to correlate process conditions to film and device performance. The results presented are not exhaustive, and specific to the discoveries associated with the ARDS.

### 2.2.1 Current-Voltage (J-V)

Measuring current density as a function of applied voltage (J-V), under controlled illumination and temperature provides whole cell performance, and key parameters relating to device quality and conversion efficiency. It is useful to visualize the solar cell with an equivalent electrical circuit as Figure 2-3. An IV measurement is performed by monitoring the device response to an applied voltage, from 0 volts (short circuit) to the open circuit voltage, with constant AM1.5g illumination. The current measured at zero voltage is the short circuit current  $I_{sc}$  (mA) and is often discussed in terms of short circuit current density ( $J_{sc}$ ) expressed as (mA/cm<sup>2</sup>). The open circuit voltage ( $V_{oc}$ ) is measured at zero current. Figure 2-4 represents a common IV curve, and identifies these parameters. From the IV curve a power curve can be generated, identifying the maximum power voltage ( $V_{mp}$ ), maximum power current density ( $J_{mp}$ ), and maximum power point (MPP). The power lost due to series and shunt resistance is represented with fill factor (FF). Fill factor is a ratio of MPP to the product of  $V_{oc}$  and  $J_{sc}$ . Parasitic losses from shunt ( $R_{sh}$ ) and series ( $R_s$ ) resistances reduce the FF. Device efficiency ( $\eta$ ) is calculated as a ratio of produced power to the power input. Test methods and apparatus are well defined by Davies [29].

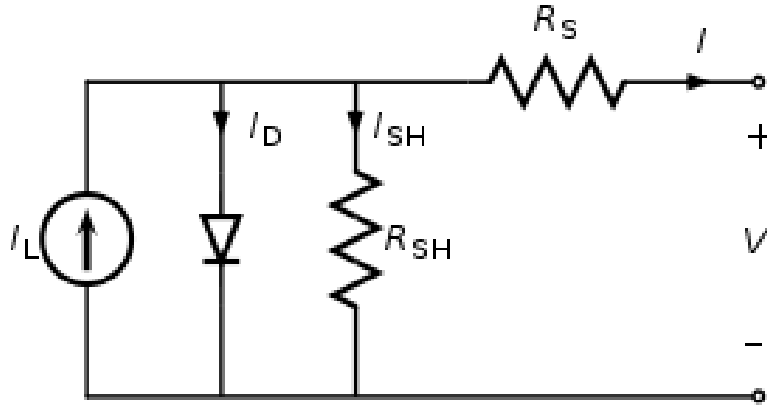


Figure 2-3: Equivalent circuit of a solar cell [11]

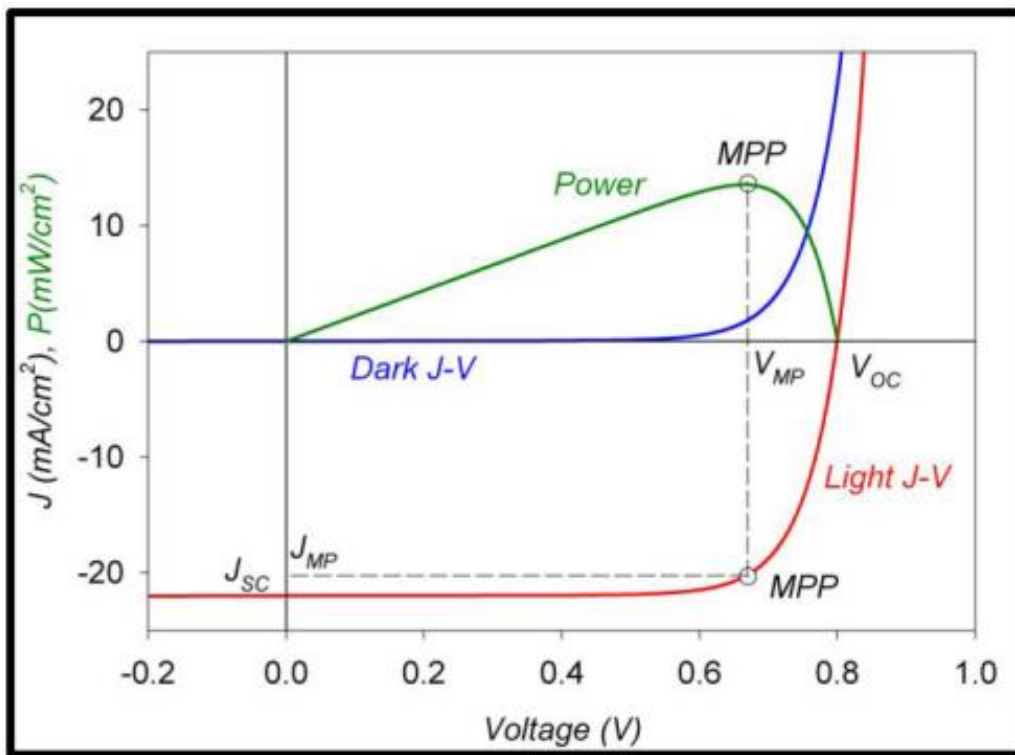


Figure 2-4: Current density-Voltage plot representing key device parameters. [30]

## CHAPTER 3: ADVANCED RESEARCH DEPOSITION SYSTEM

3.1 Basic Schematic and Vacuum Parameters The ARDS is an inline, single vacuum research tool (Figure 3-1) with an isolating load lock for sample exchange. There are a total of 9 modular stations to accommodate cell fabrication as depicted in Figure 3-2. A simple racking system allows integration of alternative source technologies, including PECSS and Co-Sublimation.. Vacuum is accomplished by a combination rotary vane and diffusion pumps, to achieve a process of record (POR) deposition pressure of 40mT. Background gas can be premixed or custom blended to satisfy research interests. Typically a high purity gas blend of 2%O<sub>2</sub> in N<sub>2</sub> is used for all baseline studies, but can be tailored to specific composition using a gas manifold and MFCs (Figure 3-3). A Residual Gas Analyzer (RGA) is utilized for monitoring the residual composition prior to and during deposition.

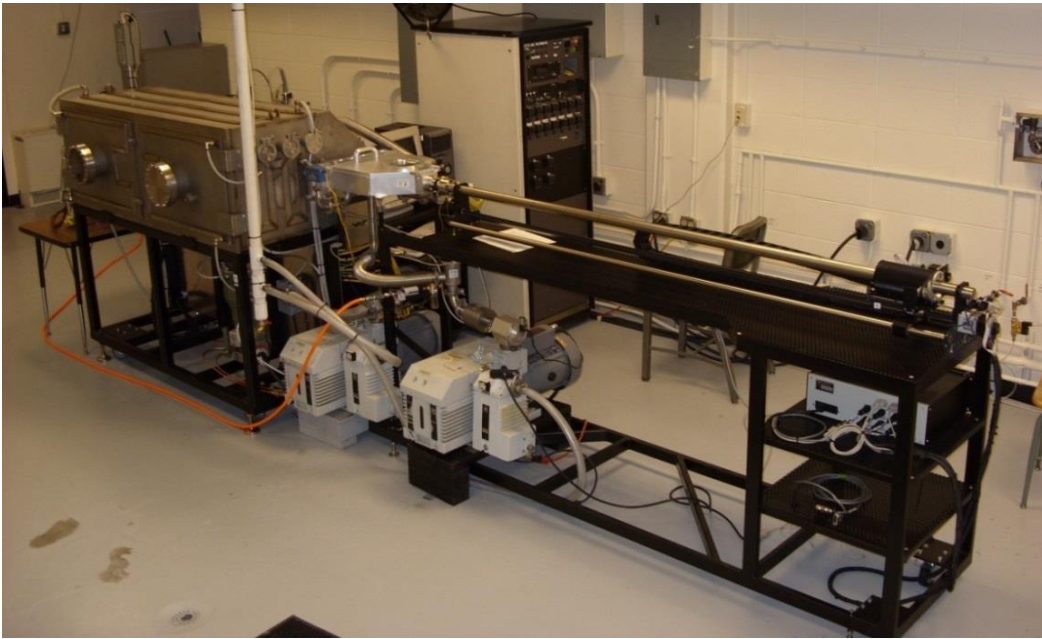


Figure 3-1: ARDS System prior to implementation of control environments.

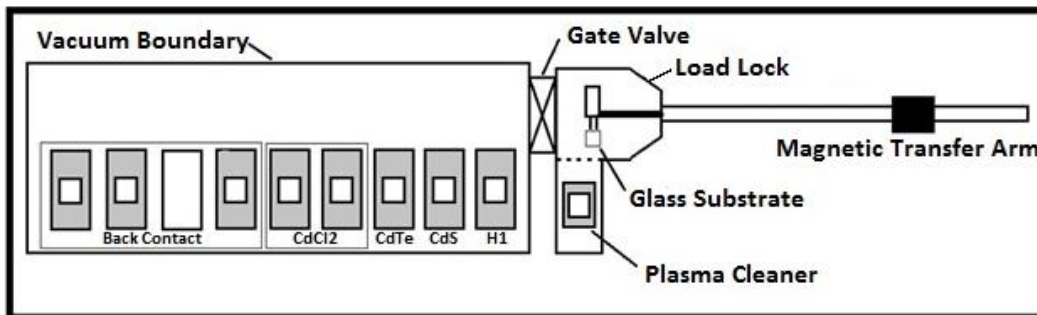


Figure 3-2: ARDS schematic of key features.



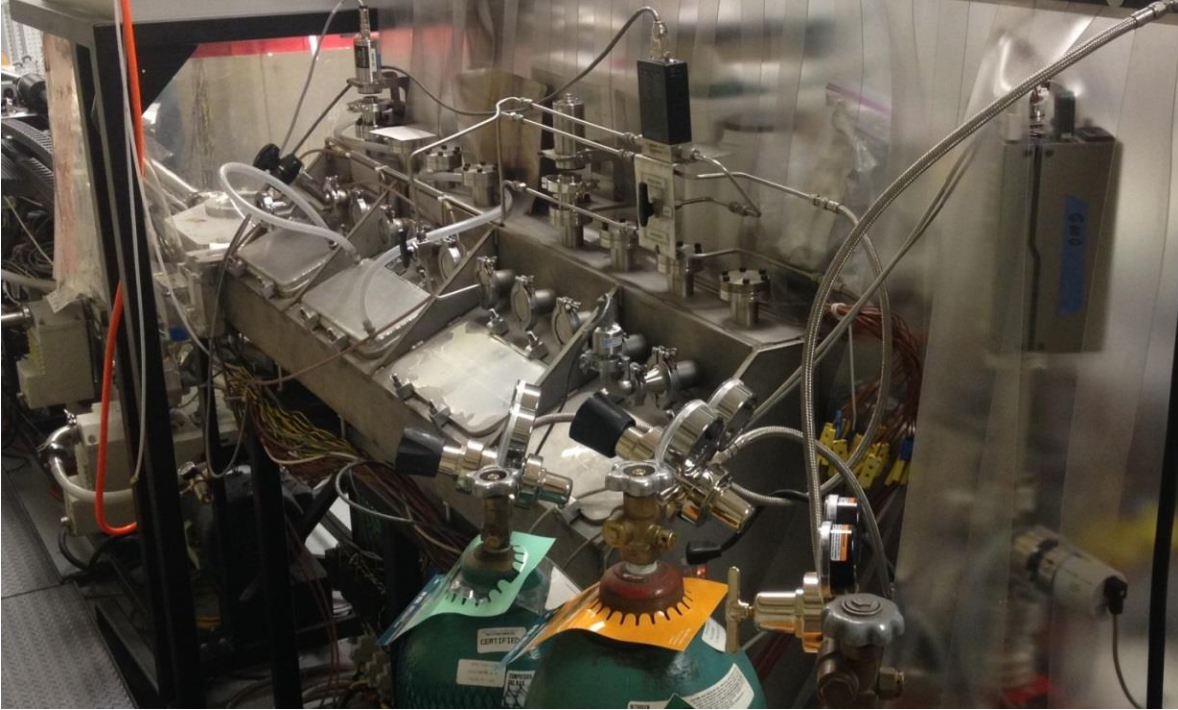


Figure 3-3: ARDS expansion ports, pyrometers and gas delivery.

### 3.2 Process Outline

The ARDS is based on the process developed in the AVA system. The source hardware is arranged sequentially and coincidentally by the thermal profile of the process. After performing the plasma treatment of the TCO, the substrate is rapidly heated to  $\sim 500^{\circ}\text{C}$ . Subsequent CSS depositions of CdS and CdTe occur, followed by a  $\text{CdCl}_2$  activation sequence. After cooling of the film, a low temperature CuCl back contact is applied and annealed. All steps are performed in a common environment, without breaking vacuum. The ARDS is easily modified to accomplish unique research tasks while allowing large combinations of process conditions.

### 3.3 Substrate Preparation

Substrates received from the manufacturer are packed with a paper interleaving. Samples are inspected for edge damage or defects in the field of deposition. They are then sorted by TCO orientation and inserted into a stainless wash rack with perimeter supports only. Immediately prior use, the substrates are suspended in an ultrasonic bath with a heated solution of de-ionized (DI) water and surfactant for one hour. A thorough DI water rinse is performed to remove detergent from the substrates, ensuring no residue is allowed to dry. The samples are then transferred to a second ultrasonic tank for a final DI water agitation for an additional 30 minutes. The samples are quickly moved to a static isopropyl alcohol bath for 20 minutes. Upon expiration of this time, samples are removed, allowing the IPA to sheet dry the substrates. The washed substrates are stored in a mini-environment

(Figure 3-4) area adjacent to the load lock until use. Once under vacuum, samples receive a final plasma treatment in the load lock, immediately prior to deposition. Further information regarding this technique is presented by Swanson [22].

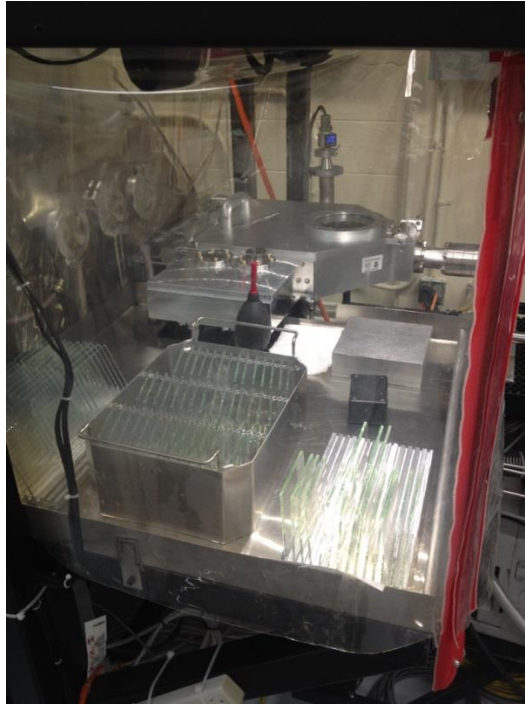


Figure 3-4: Down draft mini-environment for substrate staging.

### 3.4 Plasma Cleaning

As a means to improve substrate preparation, or modify the front contact, a novel hollow cathode plasma cleaning source was developed and implemented in the load lock of the ARDS. As part of the deposition routine, samples are exposed to a short (~30sec) low energy plasma cleaning process in the presence of process gas. This process has demonstrated significant improvements in window layer density and quality, reducing shunting defects and improving uniformity [21].

### 3.5 Substrate Transfer and Manipulation

In the ARDS, a single substrate is transported by a magnetically coupled end effector. Linear transfer motion is achieved by a ball bearing lead screw driving the carriage assembly in Figure 3-5. The carriage is magnetically coupled to the transfer arm within the stainless tube. A rack and pinion gear mounted at the end effector converts rotational motion of the carriage, to linear motion of the end effector in Figure 3-6. The end effector is mounted on a precision guided transfer arm which moves linearly behind the deposition stations. At the desired station, the end effector is extended into the process station. The end effector is made of Inconel to inhibit

thermal and chemical degradation. The ARDS represents the longest automated magnetic transfer arm currently in operation according to the manufacturer, Transfer Engineering.

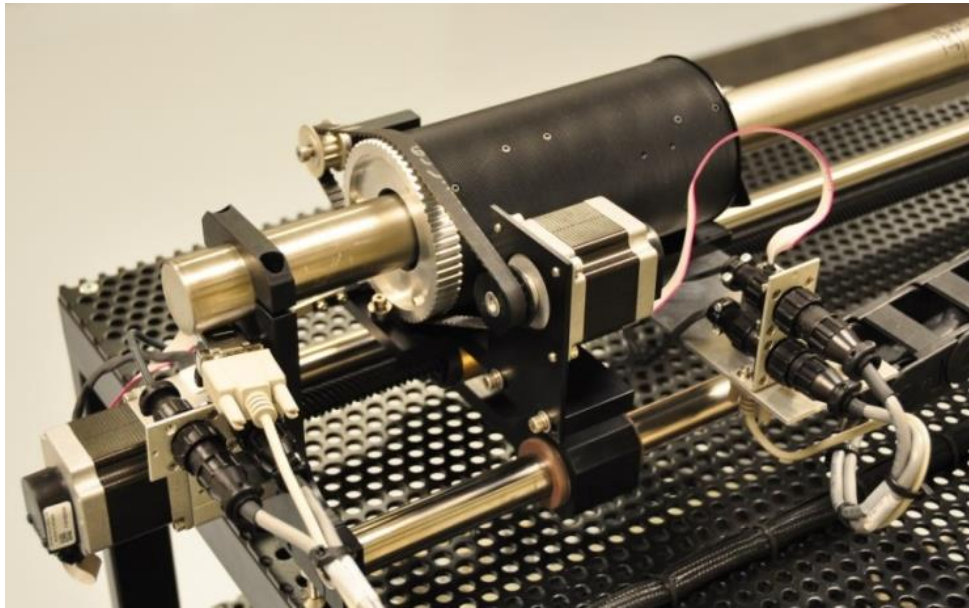


Figure 3-5: Magnetic coupling carriage assembly of the ARDS vacuum transfer arm; developed by Transfer Engineering.

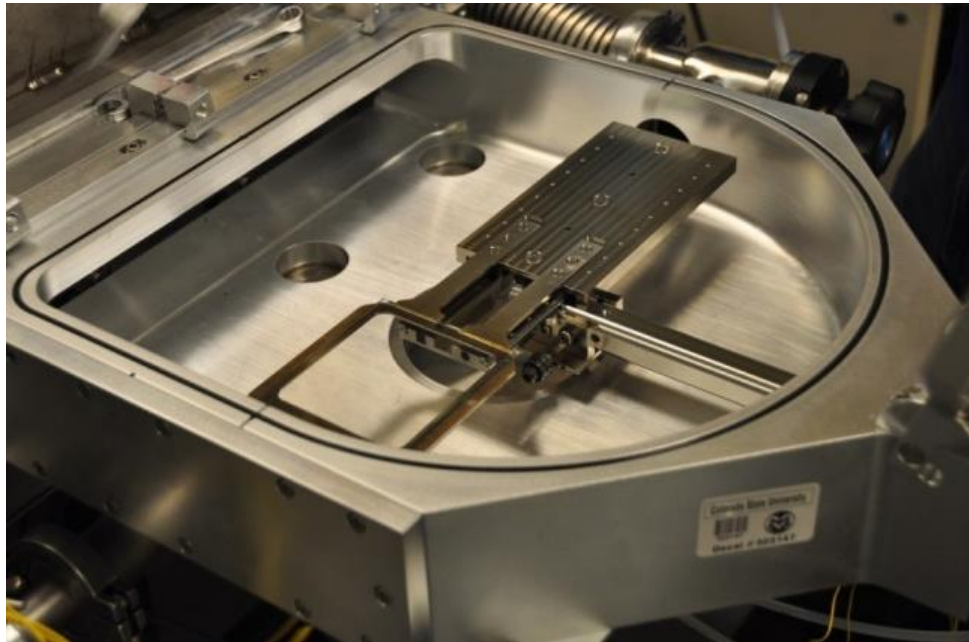


Figure 3-6: ARDS load lock and end effector for substrate transport and manipulation.

### 3.6 Heated Pocket Deposition Source Design

Achieving predictable results requires maintaining a steady state condition within the process space. The primary factor affecting run length is material consumption via loss mechanisms. Material sublimation is sustained

at elevated temperatures over the duration of an experiment, but material usage is managed by a novel shutter system. A passive shutter was conceived to close the sublimation sources between samples. The graphite shutters are actuated open by the translating end effector into the source, where the substrate becomes the target and receives the material vapor. As the substrate is withdrawn, a counter weight system closes the shutter and caps the source, preserving charge. The CAD model of the HPD source assembly in Figure 3-7 identifies the Top/Bottom sources and shutter. The physical hardware as installed in the ARDS is presented in

Figure 3-8, and with the top source removed to view pocket and shutter hardware in Figure 3-9.

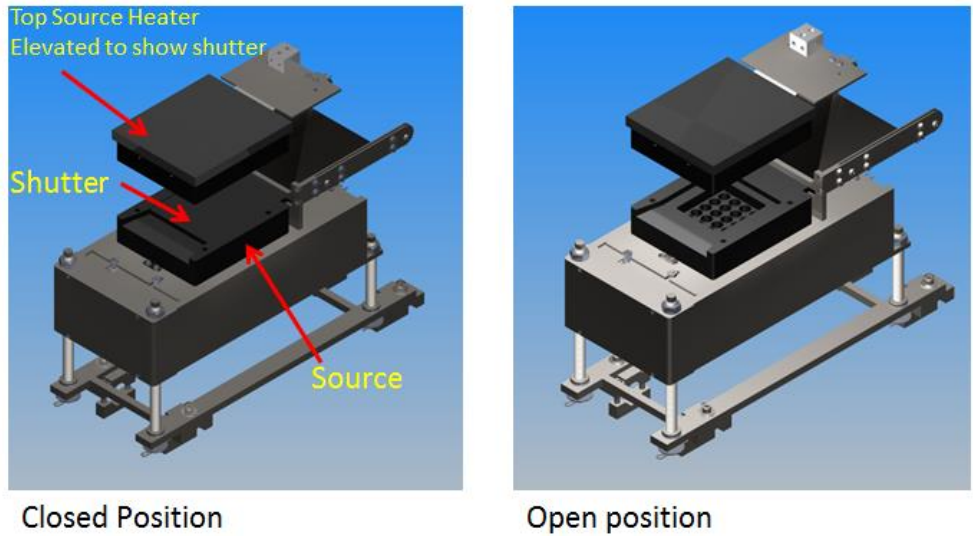


Figure 3-7: Assembly view of ARDS HPD hardware with shutter in closed and open position.



Figure 3-8: ARDS source hardware inside vacuum system



Figure 3-9: Heated pocket deposition source revealing pocket and shutter hardware

Heating of the source material, and substrate, are by means of radiation heat transfer, requiring tight thermal uniformity. Careful design and analysis was performed to provide uniform and rapid heating of the sublimation crucible [31]. Graphite was selected for the source material based on having excellent thermal conductance and chemical inertness. Heating is accomplished by coiled Nichrome elements. The elements have been electrically isolated and cemented into the crucible with a ceramic compound as visible in Figure 3-10. This technique produces rapid uniform heating and minimizes the thermal influence on surrounding components. This heating technique also enables the precise placement of heating elements for tuning of thermal gradients. The embedded elements have enabled the stacked source geometry utilized in the co-sublimation source. The heating system is controlled by Watlow temperature controllers, communicating with high voltage solid state switching devices, and responding to k-type thermocouples located in the body of the crucible.

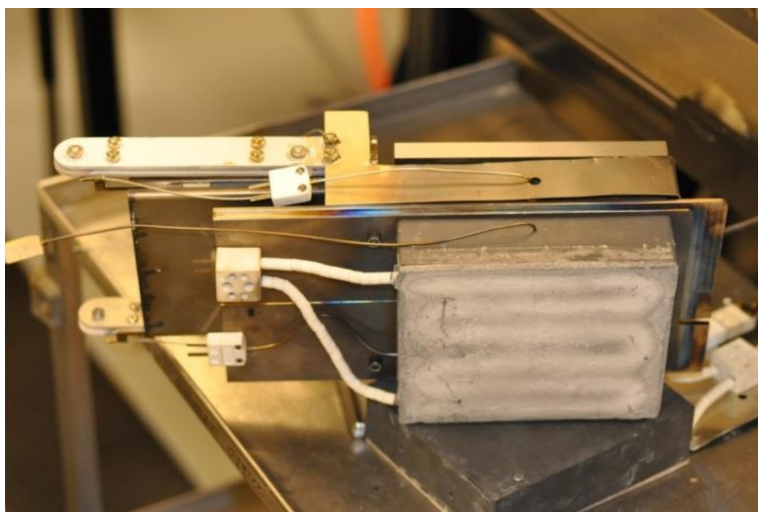


Figure 3-10: Bottom HPD source presenting embedded heater.

A section view of the bottom HPD source is presented in Figure 3-11. Photovoltaic material, of varying form, is placed in thermal wells within the source as demonstrated with CdS in Figure 3-12. The thermal wells provide additional radiating surface area to improve the uniformity of sublimation. Material forms include powder, granular, chunks, and slugs. The powder and granular material are pressed into the wells, increasing charge density and improving control of the sublimating surface area.

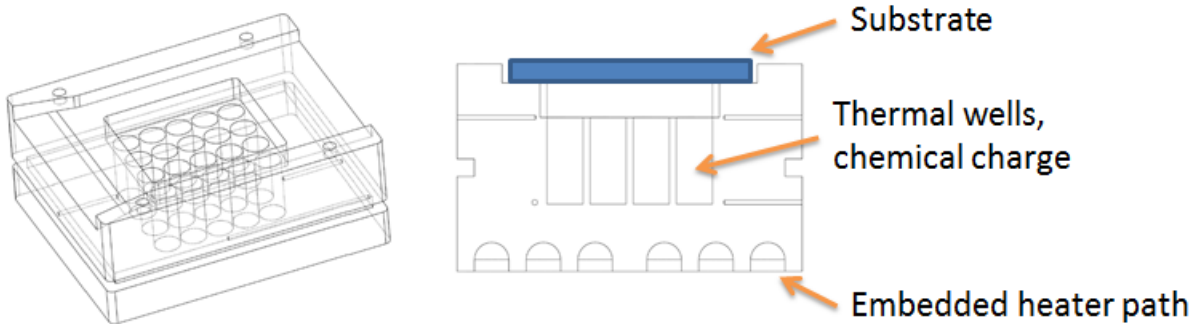


Figure 3-11: Sectional view of ARDS HPD bottom source, and substrate placement.

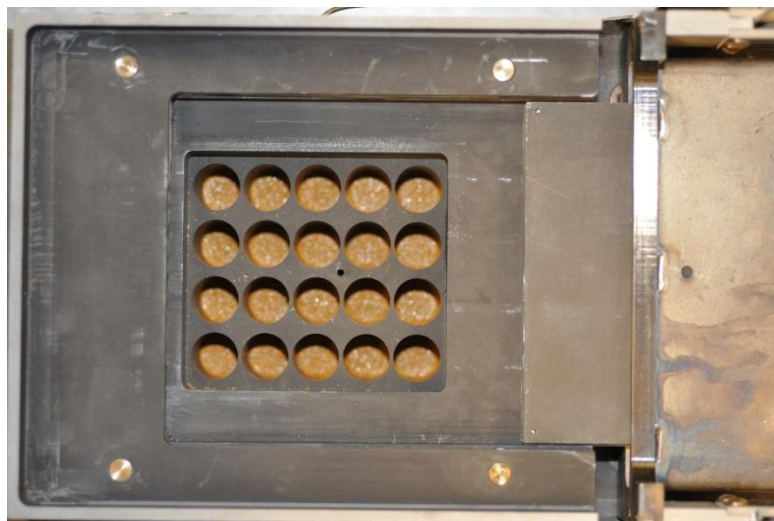


Figure 3-12: Bottom HPD source presenting CdS charge.

With the help of simple radiation heat transfer algorithms, the substrate and source temperatures can be approximated and tuned. Thermal control of the substrate is dominated by radiation heat transfer through the front side of the glass, opposite to the deposition surface, where the emissivity is largest through most of the process. During deposition, heat is transferred to the substrate by radiation and material transport. A heated top source is used to maintain the temperature of the substrate.

### 3.7 Heated shutter

As the shutter is displaced by the incoming substrate, it undergoes a drop in temperature. This reduced temperature allows condensation of source material, limiting run length and inhibiting motion. To control this deposition of material, an actively heated shutter was developed, Figure 3-13. Utilizing the previously defined method, an embedded heating element was integrated into the shutter, maintaining a deposition free temperature. A reduction in the material consumption and reliable actuation of the shutter resulted, increasing run lengths.

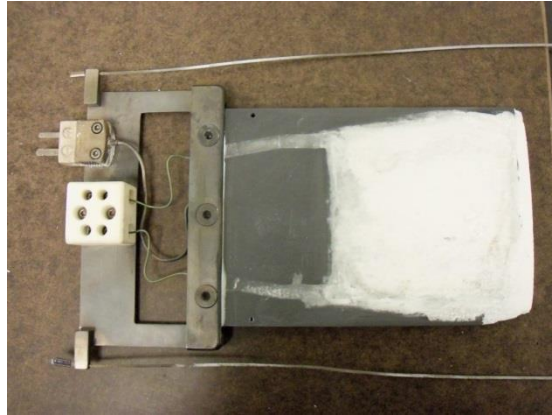


Figure 3-13: ARDS heated shutter hardware

### 3.8 Temperature measurement

As a means to monitor substrate temperature, provisions for pyrometers were installed behind each station, above the transfer galley, Figure 3-14. The pyrometer has a measurement range of 100-1300C, and emissivity adjustment of 0.2-1 at a spectral range of 5 micron. Calcium fluoride pyrometer viewports are utilized for their high IR transmission. The sample is rapidly scanned beneath the pyrometer providing a thermal profile of the process, while minimally impacting substrate temperature.



Figure 3-14: Mikron pyrometer installed on ARDS

Source temperature is monitored with shielded k-type thermocouples installed within the body of the sublimation source. The location of measurements was determined from thermal modeling to be representative of the pocket temperature. Redundant TCs are installed for process security, and uniformity monitoring.

### 3.9 Process Control

In-situ characterization techniques are limited in the ARDS due to the high operational temperatures and high operating pressures. Precise control of key parameters including process pressure and composition, source and substrate temperature, and dwell time enable repeatable process results. Careful mapping of process parameters to device performance are highly valuable for process tuning. The ARDS is highly repeatable when maintained according the standard operating procedures (SOP). Rapid testing of film thickness and Voc during sample generation is useful to confirm process performance.

### 3.10 Integration and Startup

The shell of the system and many of the primary components were fabricated before this research was started. Final integration of pumping systems, source hardware, transfer mechanisms and process control were necessary prior to initial startup of the system. This research included the definition and execution of machine maintenance and modifications throughout the period of study. This included manufacturing new hardware and coordination of resources as necessary.

System startup began with atmospheric testing to address mechanical issues associated with substrate transfer and shutter actuation. Fine tuning of shutter components to correct clearances and alignment was necessary. Stainless galling was corrected by careful application of Boron Nitride to metal-metal interfaces, and utilization of high temperature ceramics where possible. Initially, the length of the transfer arm presented difficulties in maintaining repeatable positioning. Guiding mechanisms were inadequate to resist bending and rotational moments, occasionally interfering with source hardware. Modification to bearing assemblies and precision alignment of supporting structures has resulted in reliable motion.

Achieving quality vacuum required locating leaks by means of helium leak detection and correcting. The large number of feedthroughs, o-ring seals and chamber deflection frequently presented challenges in sealing. Baseline quantification of virtual leaks and outgassing of components assists in monitoring vacuum quality over the life of the system. Further mechanical testing under vacuum was performed to ensure component alignments were



maintained as deflection of the vacuum chamber occurred. Adjustments to pumping and venting systems were made to optimize operation and minimize process pressure variation.

With mechanical and vacuum testing complete, thermal testing was initiated. CSS operating temperatures in excess of 600C present a serious mechanical and thermal challenge. Further modification to hardware to account for and/or control thermal deflection was necessary. Managing chamber skin temperature was major challenge, as the radiation shielding was inadequate, and top sources relied upon radiation cooling to the skin. Extensive heat load at the front end of the process cause heating induced vacuum seal failure, and chamber distortion impacting substrate transfer. Internal radiation shields were developed and external heat management techniques were implemented to mitigate thermal issues. Additional alignment of the transfer arm at process temperatures was performed, correcting for thermal expansion of components. High voltage arcing due to insufficient electrical isolation frequently blew fuses and tripped breakers until corrective shielding was implemented. The original method of potting heater elements into sources caused separation of source and element under thermal cycling. A design change to incorporate a locking element was derived and corrected this failure.

Testing of feedback and control loops was performed, ensuring systems were communicating correctly. Tuning of the PID heater control parameters was performed to achieve rapid heating, minimal overshoot and stable response. It was revealed that the potential for thermocouple failure, randomly or through maintenance activities, necessitated the installation of redundant thermocouples. A second source location was identified for the redundant measurement and further improved the understanding of source uniformity. Several studies were performed to measure heating rates, uniformity, and cross talk between sources. The results were used to improve and validate modeling efforts. Thermal characterization of the substrate uniformity was performed with an IR camera, and compared to the in-situ pyrometer. The thermal impact of the end effector is realized in Figure 3-15.

Satisfied with mechanical and thermal qualifications, the introduction of chemical was approved. Prior to the loading of chemical into the system, safety measures were to be addressed due to the handling of Cadmium compounds. The installation of a containment bubble seen in Figure 3-16, with HEPA filtration, and tacky mats served to contain chemical migration. Generating dedicated tool sets, including a HEPA vacuum, for performing maintenance was required to limit exposure of lab personnel. Configuring a portable fume hood for access from the containment bubble allowed chemical processing and loading of sources.

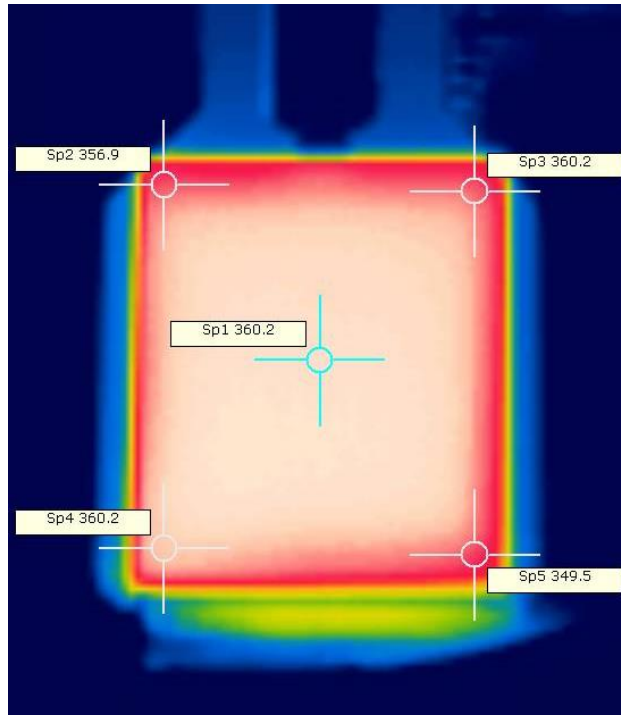


Figure 3-15: IR image of a substrate in the end effector after heating.

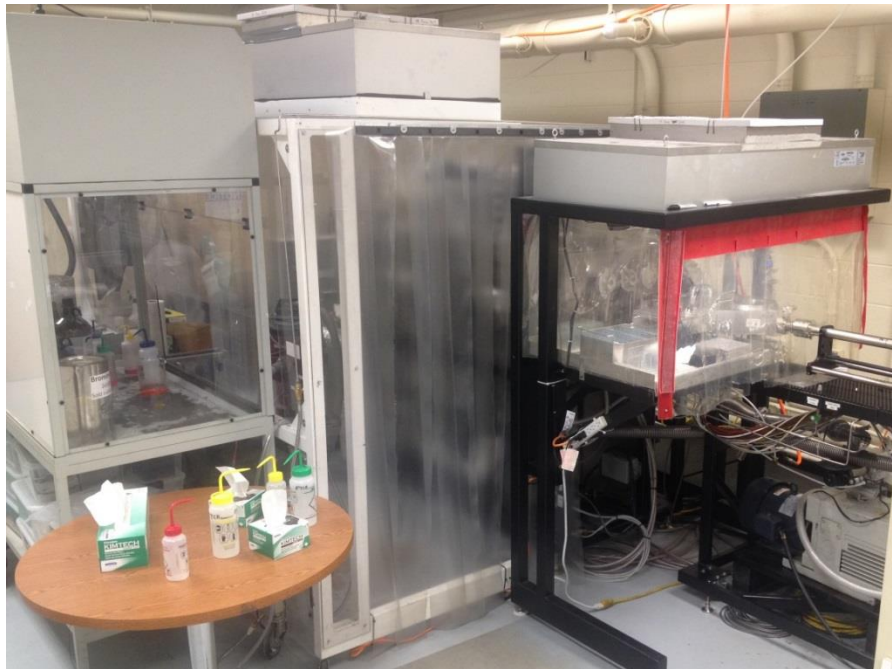


Figure 3-16: ARDS with containment and mini-environment.

The introduction of chemicals was done individually to monitor for migration and contamination. Films would be carefully characterized for material composition to ensure isolation of species. Routine testing of performance and process repeatability of devices with no copper was used to establish confidence in process control. Baseline films were produced for each species and catalogued as a means to identify contamination.

## CHAPTER 4: PROCESS DEVELOPMENT AND DEVICE RESULTS

### 4.1 Methodology

Achieving device performance requires a strong correlation to processing conditions, but decoupling process and performance can be very challenging with CdTe cells. The development of the ARDS process required careful mapping of process parameters and performance metrics. Fortunately, the ARDS provides a highly tunable process, allowing individual parameters to be modified while maintaining the balance of process conditions. The process space for CdTe solar cells is very non-linear and requires concurrent tuning of all parameters. Strong interdependencies exist between the as deposited CdS/CdTe layers and the CdCl<sub>2</sub> and Cu back contacting processes. Optimized individual parameters do not directly translate to an optimized complete device, as complex interactions result during junction formation and treatment. Establishing the baseline process to demonstrate 12% device efficiency required an extensive test methodology to understand device structure, process and performance. At the onset of chemical tuning, the strategy described in Table 4-1 was used as a guideline.

Table 4-1: ARDS experimental strategy for process development

<b>ARDS Experimental Strategy for Process Development Resulting &gt;12% Device Efficiency</b>					
<b>Environment: 40mT w/ 2%O<sub>2</sub>/BalN<sub>2</sub></b>					
<b>Dwell time: 110s</b>					
<b>Transfer time: 9sec</b>					
<b>Chemical: 5Nplus</b>					
<b>Substrate: 3.2mm TEC10, 550ppm FE</b>					
<b>Mimic AVA process space</b>					
<u>Species</u>	<u>Material Form</u>	<u>Objective</u>	<u>Target</u>	<u>Runs</u>	<u>Characterization</u>
CdS	Pressed Powder	t vs. T , repeatability	50-200nm	5	Profilometry, UV-vis, XPS, XRD, AFM, SEM
CdTe	Chunks	t vs. T , repeatability	1-2.5um	5	Profilometry, XPS, XRD, AFM, SEM
CdCl <sub>2</sub>	Pressed Powder	Voc>750mV, Rsh>2500	Same	15	Profilometry, JV, SEM, AFM, XRD, TRPL
CuCl	Pellets	Voc>800m, Rs<1, PM~90%	Same	10	Profilometry, JV, JVT, JV2, CV, QE, TRPL, SIMS, XPS, PM
<b><u>Limitations</u></b>					
Minimum top temperatures					
No in-situ substrate temperature measurement					

The introduction of Cu would only be considered after a strong no-Cu performance resulting Voc>750mV was achieved. This restriction is due to the concern for high mobility of Cu within the system. Unintentionally introduced Cu at elevated temperatures or prior to effective CdCl<sub>2</sub> treatment produces artificially improved device performance and poor stability.

## 4.2 Closed Space Sublimation Basics

Closed space sublimation (CSS) is a novel technique that has been used to produce many record cell efficiencies. The ARDS utilizes heated pocket deposition (HPD), a variation of CSS. HPD can be utilized for the sequential deposition of films to form the complete photodiode, providing an inline, single vacuum process. The primary benefits are the achievement of high deposition rates and material utilization, modest vacuum requirements, and simplicity of hardware. CSS is a high temperature technique by which a solid to vapor transformation occurs in an inert environment, transporting source material to a target as demonstrated in Figure 4-1, where it is re-condensed as a polycrystalline thin film [32]. Cruz-Campa presents a deposition rate model for CdTe deposition by close-space sublimation. As presented in Figure 4-2 and Figure 4-3, Cruz-Campa demonstrates the dependence of pressure and substrate temperature on the resulting deposition rates [33].

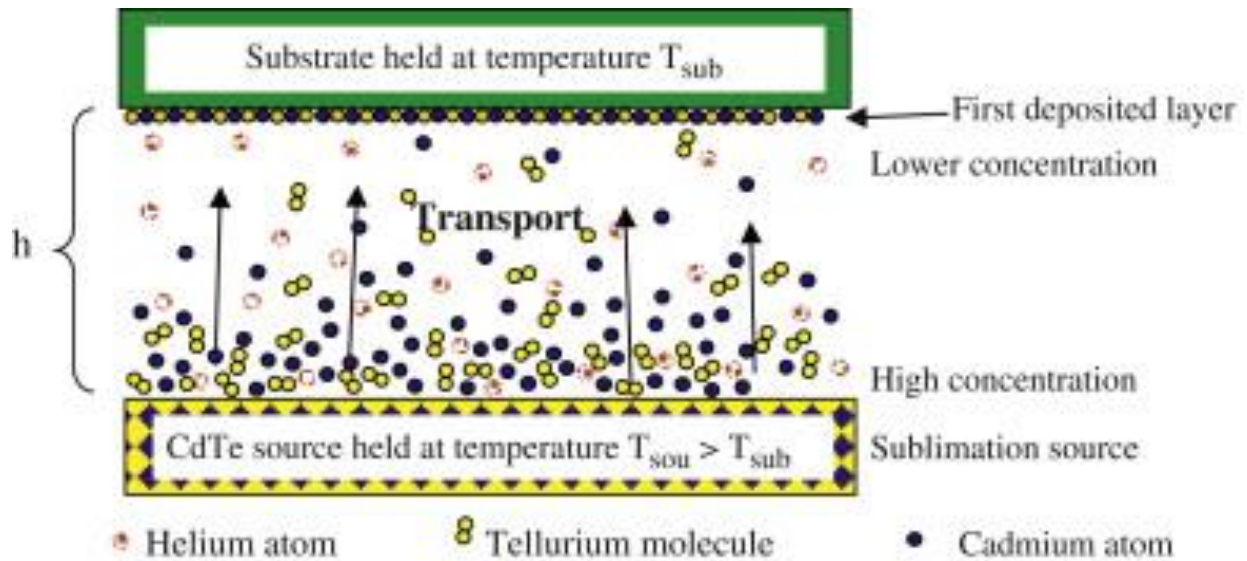


Figure 4-1: Close-space sublimation of CdTe [33]

The source material is produced in various forms, from powder to slugs, and is deposited in a heated source. At given pressure and gas composition, the source material will have a sublimation profile. The material is heated to a temperature for which a desired rate of sublimation occurs, and the material travels in the direction of diminishing partial pressure until it reaches a surface where deposition can occur or achieves a saturation pressure. This approach results in a high rate of non-equilibrium deposition that has the potential to induce significant intrinsic defects in the bulk of the film, limiting device performance [34]. Modification of the deposition dynamics can be achieved through source geometry, sublimation rate, and the deposition energy relating to substrate temperature. Deposition rates are dominated by the substrate temperature, and produce microstructural features based on the

growth rate. Condensation of particles on the substrate and resulting film formation are a function of sticking, diffusion, nucleation and growth. Management of intrinsic defects through process control results higher efficiency devices [35]

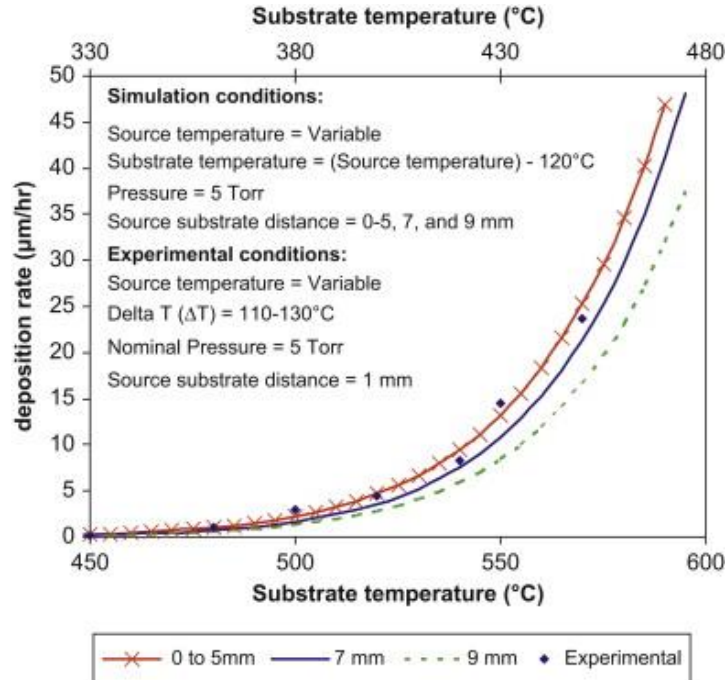


Figure 4-2: Exponential behavior of the estimated deposition rate vs. source temperature for different source-substrate separations. [33]

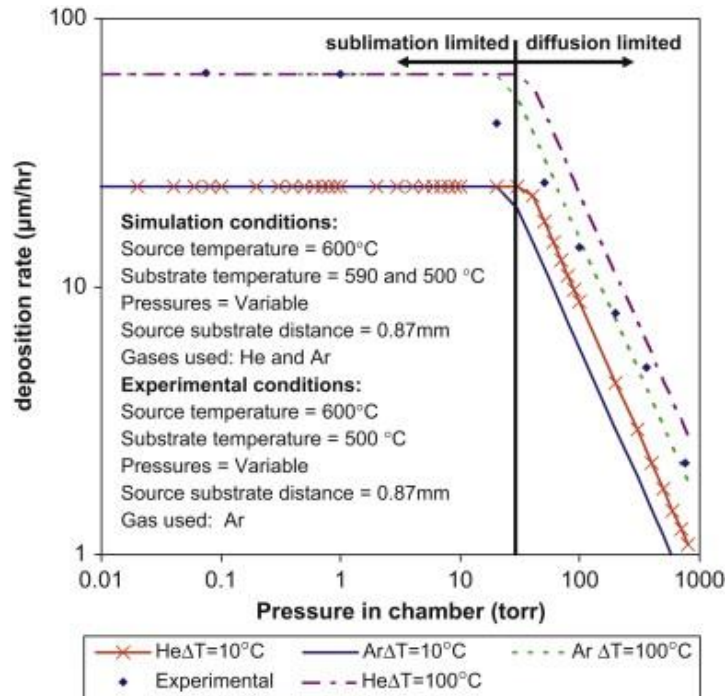


Figure 4-3: Estimated deposition rates vs. chamber pressure. The growth rate increases as pressure decreases in the diffusion-limited regime; in the sublimation-limited regime, the growth rate remains constant. [33]

### 4.3 Process Space

Utilizing knowledge gained on the AVA system, and criteria from the Abound Solar process, a background gas composition of 2%O<sub>2</sub> in N<sub>2</sub> at 40mT was selected. For this environment, a starting source and substrate temperature profile was specified. Studies to produce a baseline process would systematically explore a large process space to achieve the target device parameters. Investigation of sequence, dwell times, process pressure and gas composition would be performed to increase understanding of process response, and device performance.

A Labview program was created to estimate the thermal profile of the substrate through the process. Input parameters for each process step included top and bottom source temperatures and emissivity, dwell time, and substrate emissivity for both the coated and uncoated side of the sample. With the substrate thickness, an algorithm determined the resulting heat transfer between source and substrate to produce the temperature profile of the substrate through the process, as presented in Figure 4-4

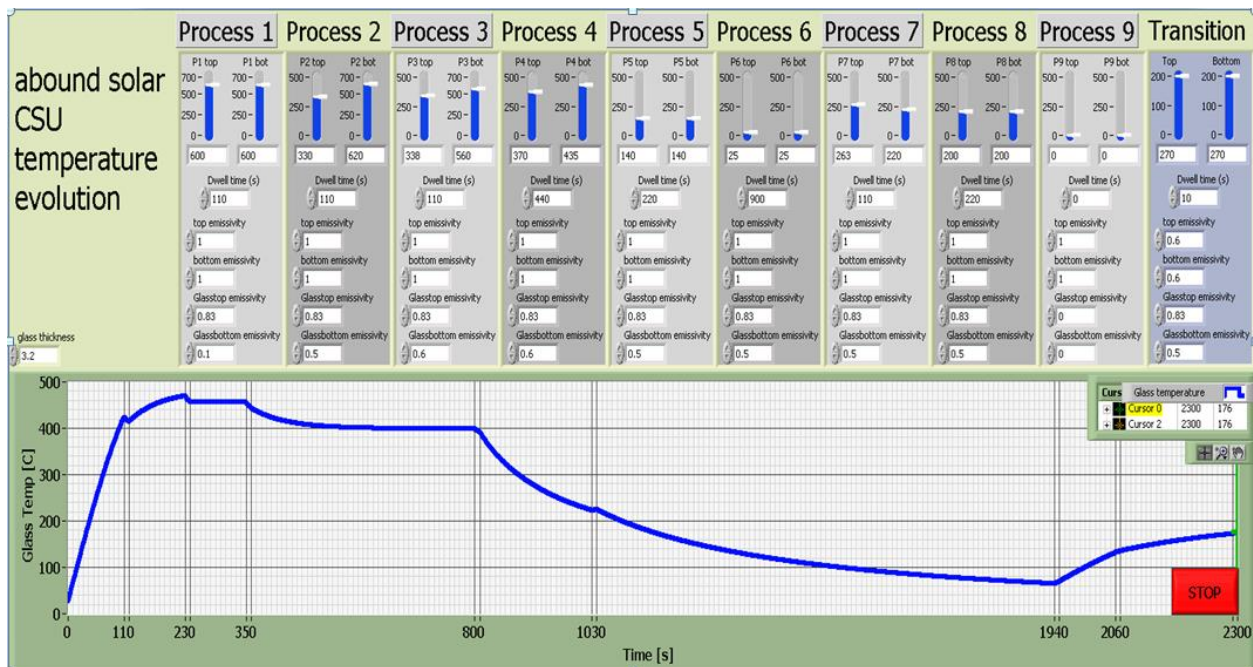


Figure 4-4: Predicted thermal profile of substrate.

### 4.4 Substrate Heating

At the onset of this research, a target substrate temperature of ~370C was demonstrated to produce suitable CdS film crystallography in the AVA system. The exit temperature of the substrate is critical to the nucleation of CdS and subsequent film morphology. The substrate exit temperature directly affects the CdS deposition dynamics. The strong interaction of process parameters is initially demonstrated by the substrate exit temperature. Further

tuning of the substrate heater is performed after the development of CdCl<sub>2</sub> films to test thinner CdS, while maintaining exit temperature.

The open source geometry and high temperature of the heating station are well suited for thermal cleaning of the end effector between samples. Various dwell conditions were investigated to identify a condition resulting complete re-sublimation of chemical deposits from the end effector. A 440sec dwell was necessary to achieve a carrier temperature adequate to resublime CdS deposits, and is performed after every CdCl<sub>2</sub> treatment.

The heating station is also used to perform reheating of previously deposited films, such as sputtered CdS:O prior to further deposition. Its proximity to the pyrometer allows precise tuning of substrate exit temperature.

#### 4.5 CdS Optimization

Producing a sufficiently thin, high density CdS window layer is critical to achieving maximum potential Voc. Non-conformal coverage in the form of pinhole defects and gross discontinuities act as weak diode regions between the CdTe and TCO effectively reducing Voc [36] [29]. The method preferred for high growth rate CdS processing is CSS, typically resulting larger grain size and band gap than films grown by chemical bath deposition (CBD), an alternative method [37]. The large CdS grain structure produced with CSS can make achieving conformal coverage difficult, but careful substrate preparation and optimized deposition conditions improve nucleation and coverage.

To control the influence of pinhole defects, CdS films of 100-200nm thickness are necessary with standard substrates. To maximize J<sub>sc</sub>, the CdS layer should be thinned just until a reduction in the voltage is observed. High temperature CdCl<sub>2</sub> treatments drive the interdiffusion of CdS-CdTe, which serves to effectively reduce the thickness of the CdS layer. With aggressive treatments, the entire CdS layer can be consumed, creating a junction between the resulting CdTe<sub>1-x</sub>S<sub>x</sub> alloy and TCO [38].

Tuning of the process to achieve thin and dense films was performed as a first priority. To test the stability of the sublimation source, samples were generated at a constant temperature over a period of time after source replenishment. The data set presented in Figure 4-5 represents repetitive samples from a single run, and continued over successive runs. Sampling is not performed until source temperature has maintained steady state for 20minutes. The film thickness vs. time exhibits an initial elevated sublimation rate, which stabilizes over an extended period of time. This observation demonstrated the need for a routine “burn-in” procedure after loading new CdS material. The “burn-in” procedure is performed by locking the shutter assembly open and placing a substrate directly on the

source to capture sublimated material. A temperature of ~640C is maintained for ~6hrs to burn off loose material, leaving a compact plug of material in the source.

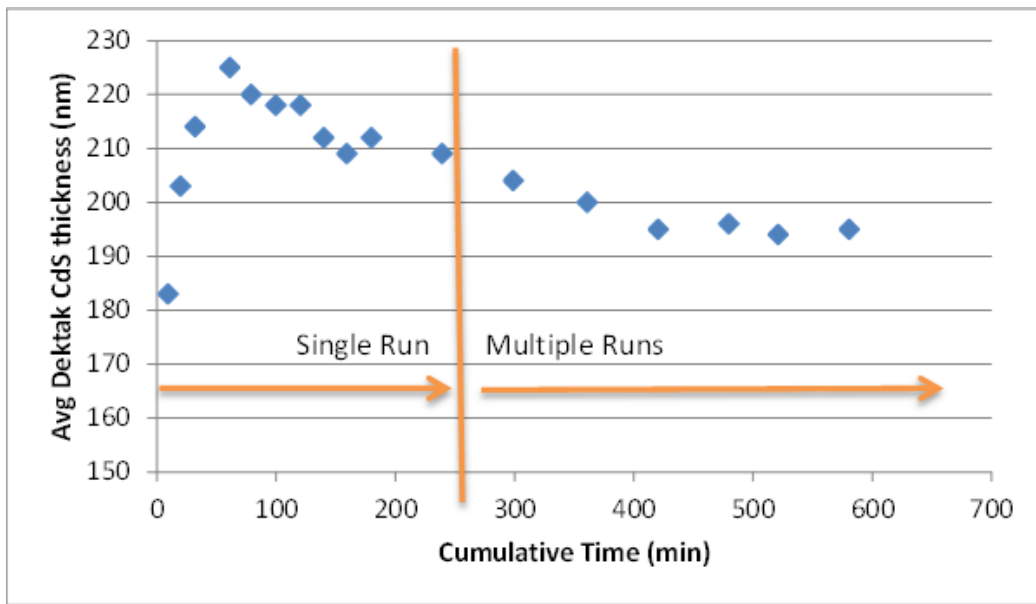


Figure 4-5: Deposition rate resulting over cumulative run time

The next objective was to generate thickness vs. Temperature curves. Film deposition rates were determined empirically, targeting 60nm/min, using Design of Experiment (DOE) methodologies. Combinations of thermal profiles for source and substrate were performed, investigating deposition rates and resulting film quality. Maintaining all other process parameters, CdS bottom source temperature was swept over a temperature range. The resulting optical images in Figure 4-6, and thickness curves in Figure 4-7, represent a process space resulting films of ~50-300nm thickness. Films were measured using profilometry and compared to UV-vis results. The spectral dependence of transmission and absorption of CdS films with varying thickness are presented in Figure 4-8 and Figure 4-9. Samples were studied using blue light measurements to characterize pinhole density and results presented by Tashkandi [39].

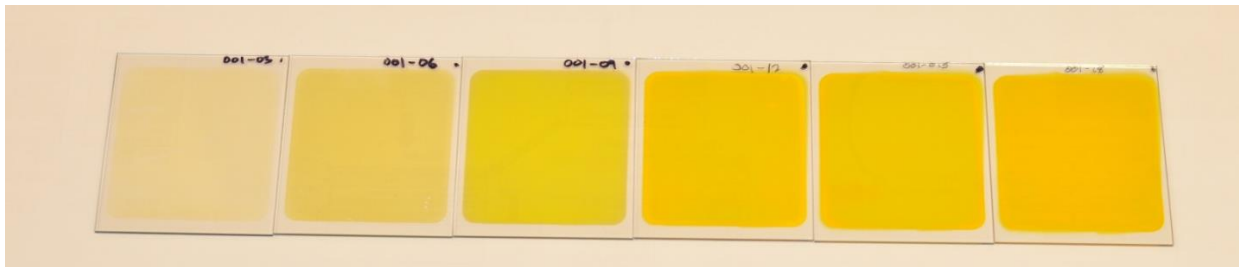


Figure 4-6: Optical images of CdS thickness sweep



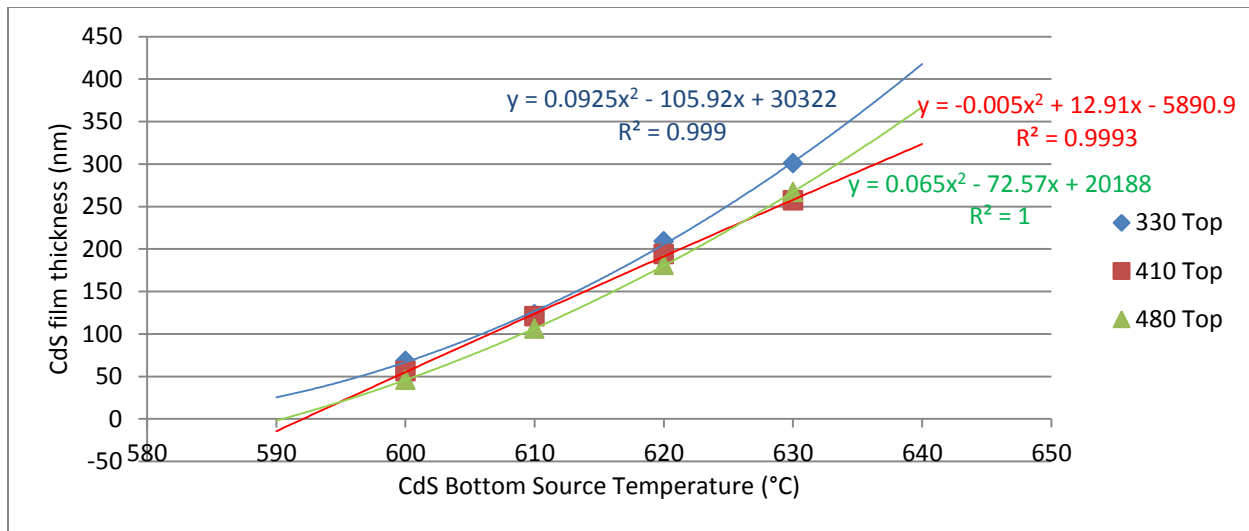


Figure 4-7: CdS Thickness vs. Bottom source temperature; 3 Top temperatures presented

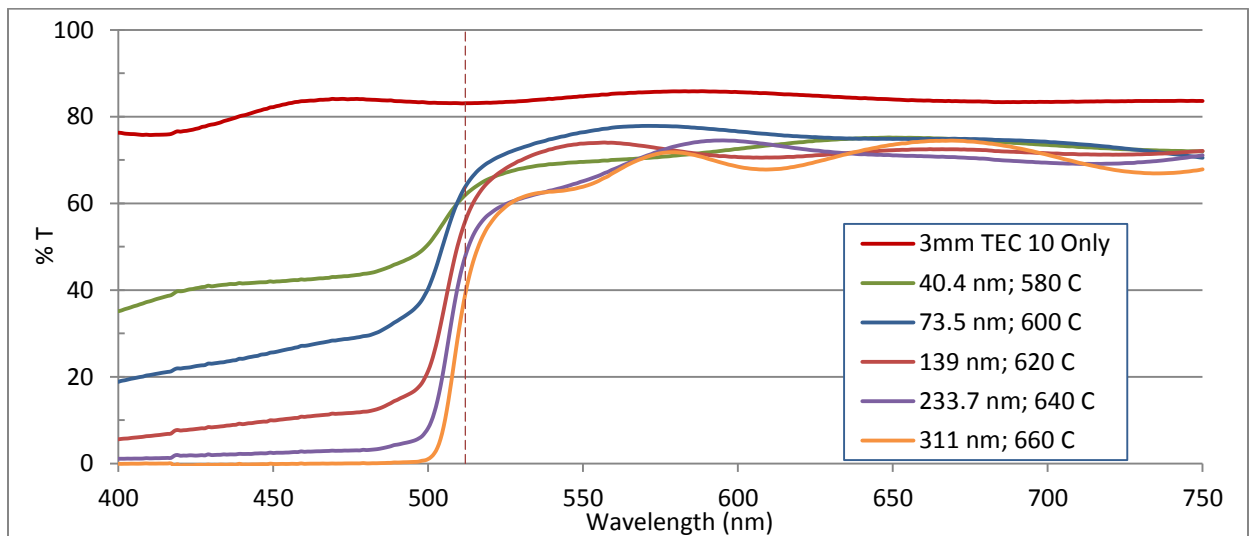


Figure 4-8: Transmission vs. Wavelength of varying thickness CdS films on 3mm TEC10 substrate.

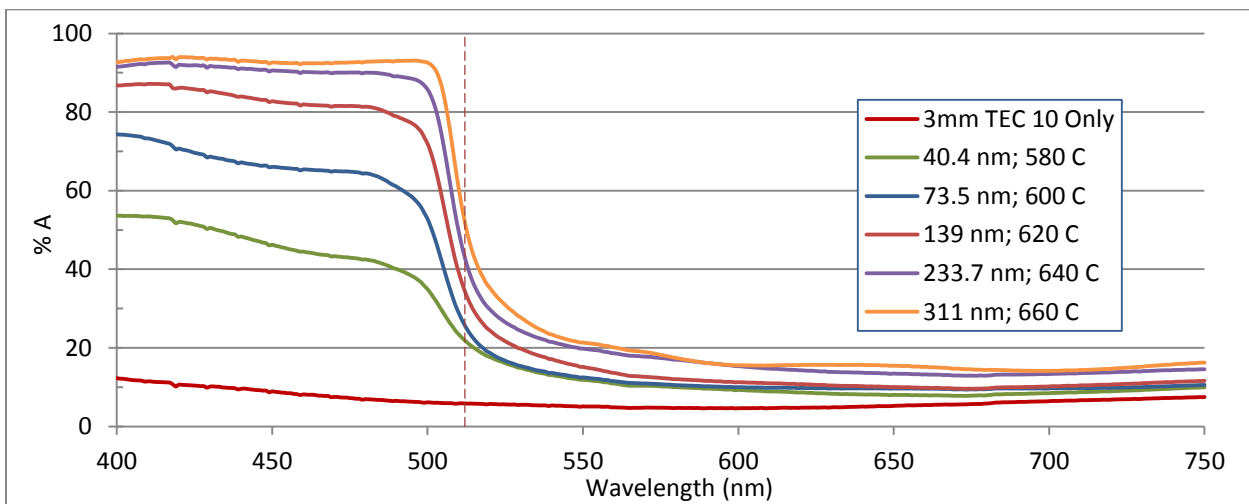


Figure 4-9: Absorption vs. Wavelength for varying thickness CdS films on 3mm TEC10 substrate.

Nucleation samples were generated at 10 second intervals using the target deposition rate. The correlation presented in Figure 4-10, provides an understanding of the linear relationship, and ability to produce varying film thickness without modifying source temperatures. Individual films were studied to investigate nucleation and growth characteristics in an attempt to improve resulting crystallographic properties. To ensure repeatable film thickness was achievable, samples were compared over 3 runs. The thickness curves are presented in Figure 4-11, and indicate a  $\pm 2.5\text{C}$  temperature variation for each setpoint tested. This confirmation allows rapid tuning of thickness for target device structures.

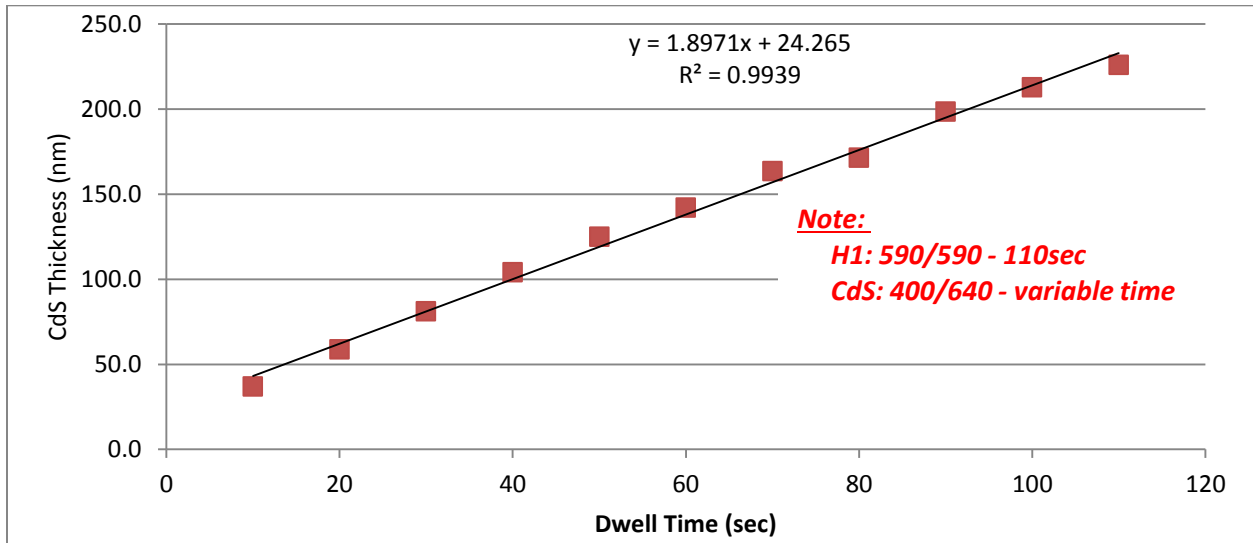


Figure 4-10: CdS Thickness vs. Deposition dwell time

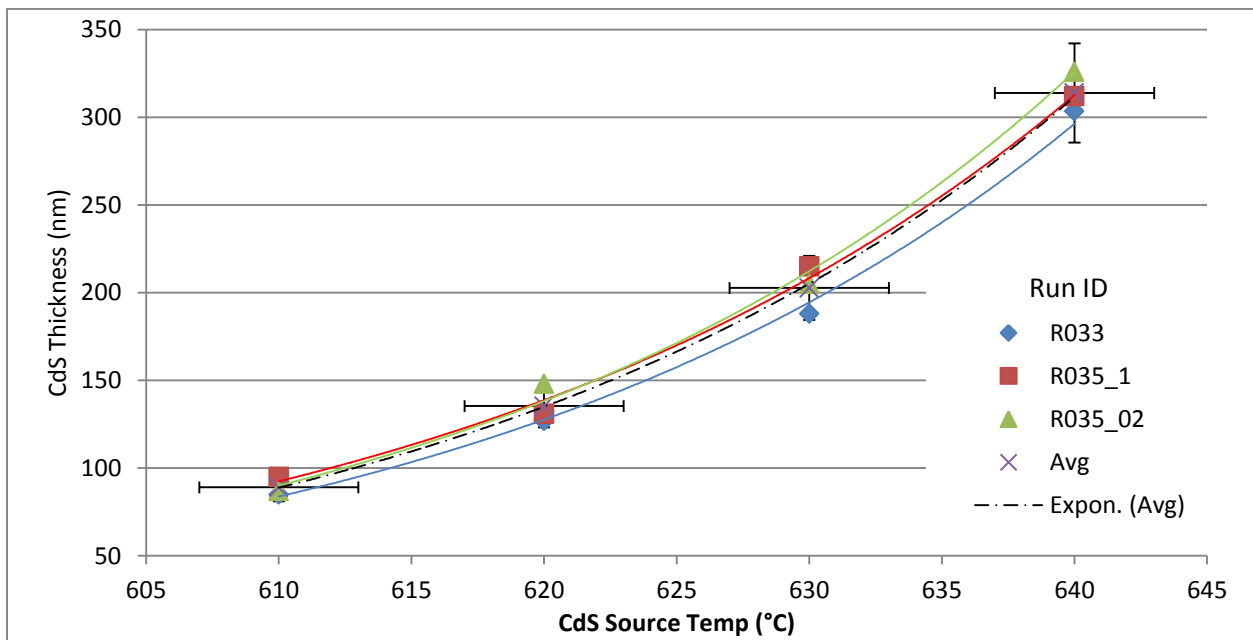


Figure 4-11: CdS repeatability over three runs

Early runs revealed the passive cooling of the top source was insufficient to test lower substrate temperature. New hardware to reduce thermal coupling of the top and bottom sources was implemented after the introduction of CdTe. Second generation top source hardware, having a larger radiation cooling surface, was subsequently installed achieving a reduction of the driven top source temperature from 370C to 325C. Investigation of films grown at the cooler temperatures produced very columnar grain structure and was deemed poor process space.

Through design of experiments (DOE) investigations of CdS-CdTe process interactions, several additional runs were generated to optimize POR CdS film. Higher substrate temperatures were required to achieve uniform film thickness and dense films. The baseline process, without plasma cleaning of the substrate, demonstrated a Voc cliff at ~110nm CdS as demonstrated in Figure 4-12. A typical CdS film on TCO is presented in Figure 4-13. Further optimization was achieved with the integration of a hollow cathode plasma source in the load lock for treatment of the substrate prior to deposition. A reduction in pinhole density of 95% [39] was observed with plasma cleaning, enabling thinner CdS films, resulting in Jsc improvement while maintaining Voc.

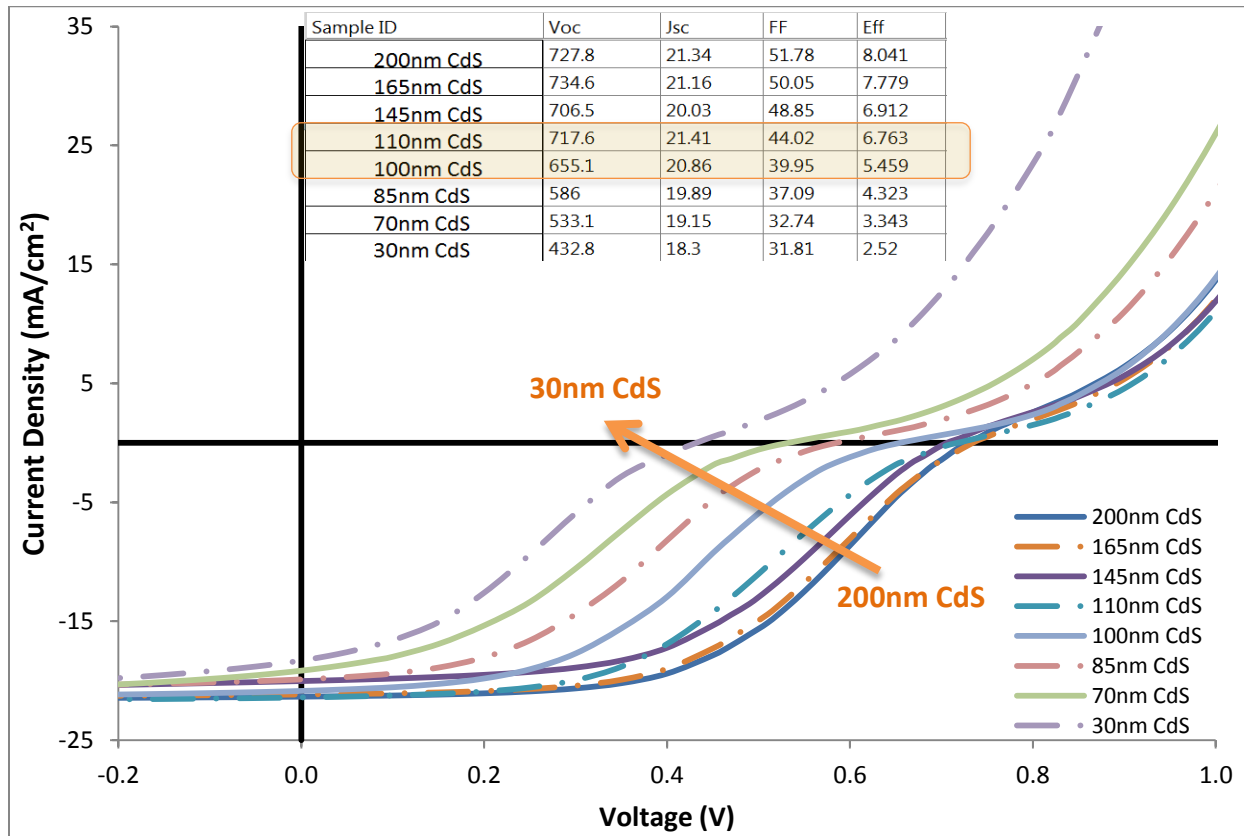


Figure 4-12: J-V curves representing thinning of CdS on no-Cu devices.

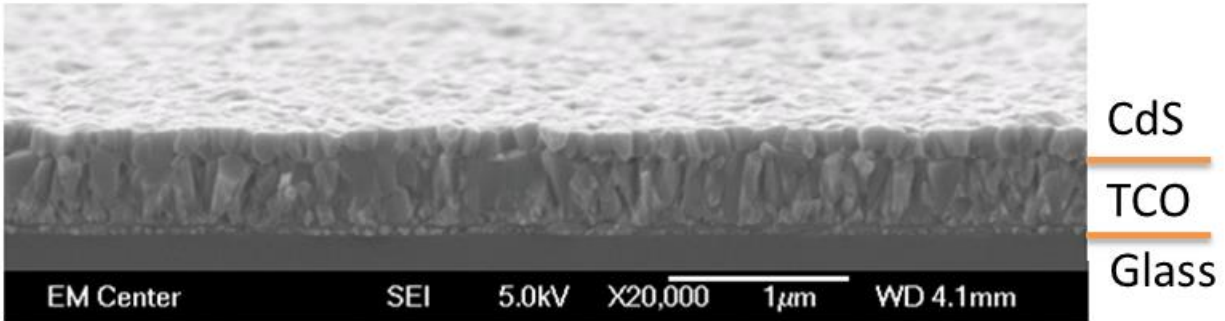


Figure 4-13: SEM Micrograph (edge view) of typical ARDS CdS on TCO.

Additional runs were committed to produce specific CdS films supporting other research interests.

- (1) Development of Ellipsometry models for the optical measurement of CdS/CdTe solar cells [40].
- (2) Intentional film defects and sample preparation methods for characterization by EL, PL, and blue light microscopy [23] [41].
- (3) Investigation of reheating previously deposited CdS layers, either by CSS, sputtering or CBD for complete device fabrication.
- (4) Investigation of film and device properties resulting from the intermediate CdCl<sub>2</sub> treatment of CSS CdS prior to CdTe deposition.

#### 4.6 CdTe Optimization

Thickness control of the discrete layers is critical to maximum device efficiency. Optical techniques are commonly implemented for rapid non-destructive characterization, specifically material thickness. Optical properties of thin films can be dominated by the surface roughness, diminishing the precision and accuracy of measurement techniques [42]. Developing thickness profiles and correlating to key process parameters was performed. CdTe thickness correlations were generated by several techniques including XRF, SEM and primarily Profilometry.

Performing film analysis by XRF is a fast, non-destructive method. Kobayakov [43] demonstrated this technique for evaluating Cu treatments, which produces data for Cd and Te concurrently. Initially it was considered that this technique could serve dual purposes, monitoring Cu treatment and film measurement. The large area averaging technique does not account for grain density and surface texture, and therefore was determined to not have the accuracy necessary for process control. The early correlation is presented (Figure 4-14), but not used for further process development.

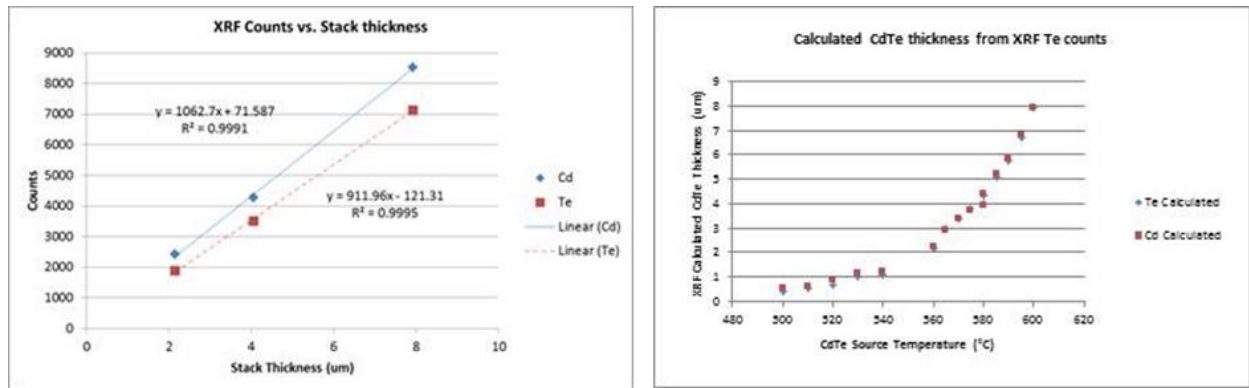


Figure 4-14: XRF correlation of Cd and Te counts to measured thickness (left), predicted growth rates using XRF trends (right)

It has been shown that the optimal properties of CdTe require only 2 $\mu\text{m}$  film thickness for better than 95% absorption of incident irradiation at 800nm. Developing a useful process space for producing  $\sim 2\mu\text{m}$  CdTe films and achieving quality CdTe microstructure, is essential to optimization of the  $\text{CdCl}_2$  treatment [44]. Maintaining other process parameters, CdTe thickness was correlated to the sublimation source temperature (Figure 4-15). While it has been shown that the substrate structure does not directly influence the structure of epitaxially grown CdTe films [45], CdTe films grown by CSS demonstrate a dependency to the deposition conditions [46].

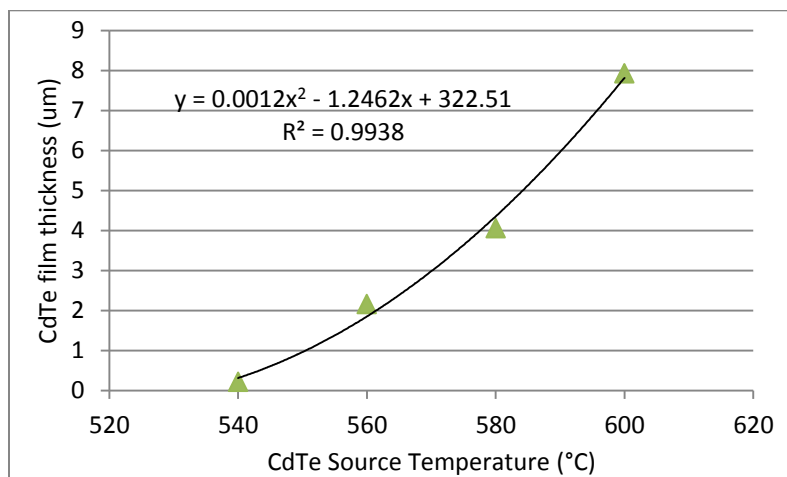


Figure 4-15: CdTe thickness vs source temperature

The CdTe structure produced in the ARDS is dependent on substrate temperature during growth (Figure 4-16), likely affecting the nucleation and coalescence of grains [47]. While the exact mechanism is not well understood, there is a distinct relationship to between morphology and substrate temperature. Thornton [48] indicates three major zones (Figure 4-18) exist for micro-structural growth based on the processing conditions. Our findings are consistent with Thornton, and others relating substrate temperature to structure [49]. The three growth zones commonly referenced when discussing the morphology of thin films are defined as: (1) Zone 1 resulting

tapered crystals with domed tops which are separated by void boundaries. Internal structure of the crystals is poorly defined, with a high dislocation density; (2) Zone 2 identified by columnar grains separated by distinct dense, intercrystalline boundaries. The surface has a smooth, mat appearance; (3) Zone 3 producing equiaxed grains with a bright surface.

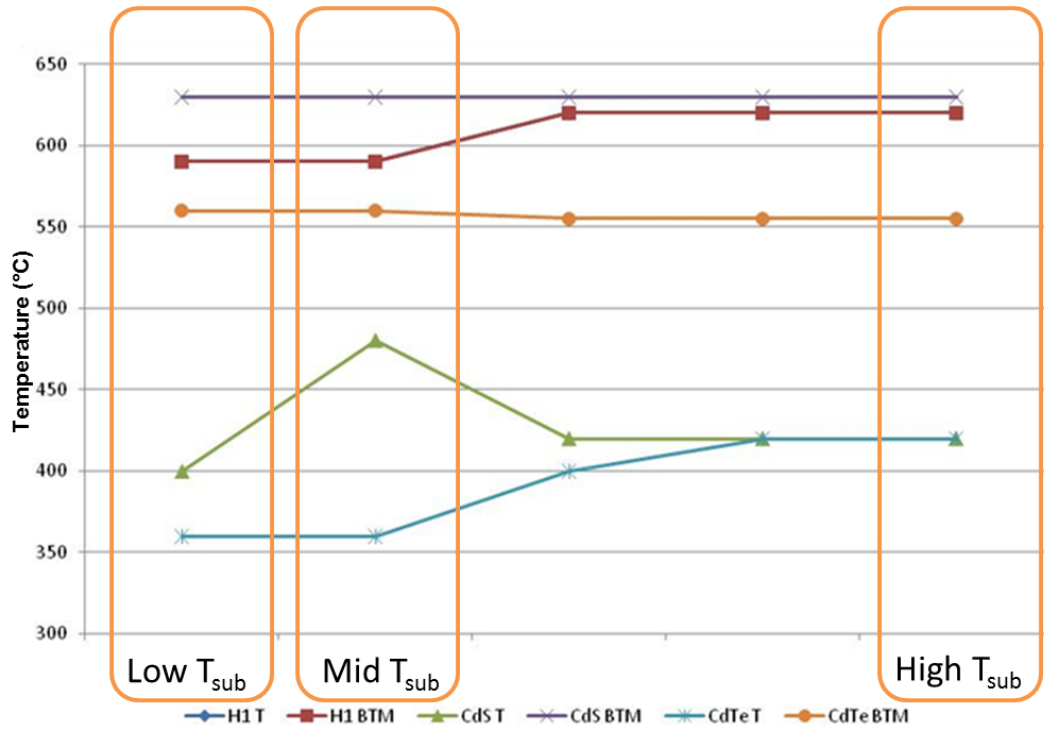


Figure 4-16: Process conditions resulting Low, Mid, and High substrate temperatures

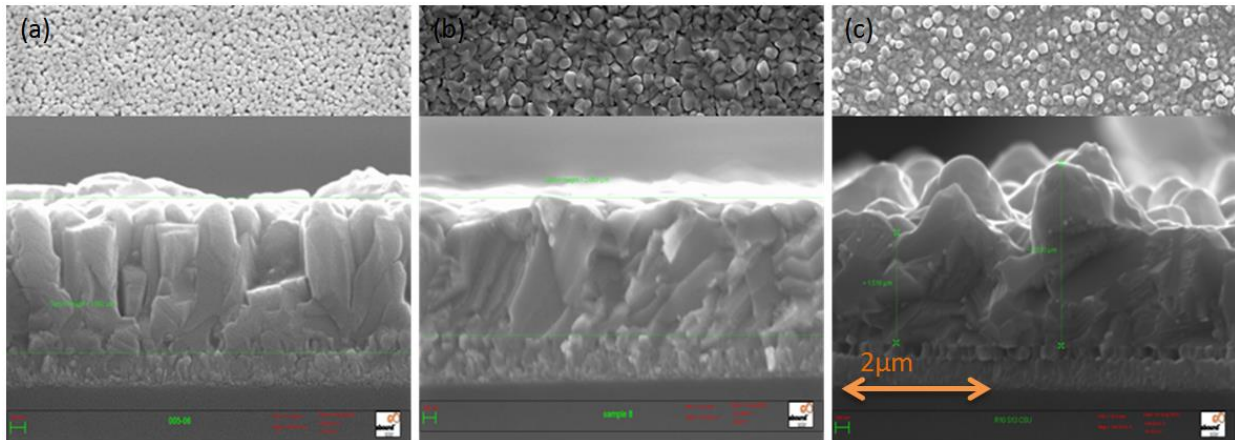


Figure 4-17: SEM images of ARDS CdTe morphology at corresponding (a)Low, (b)Mid and (c)High substrate temperature.

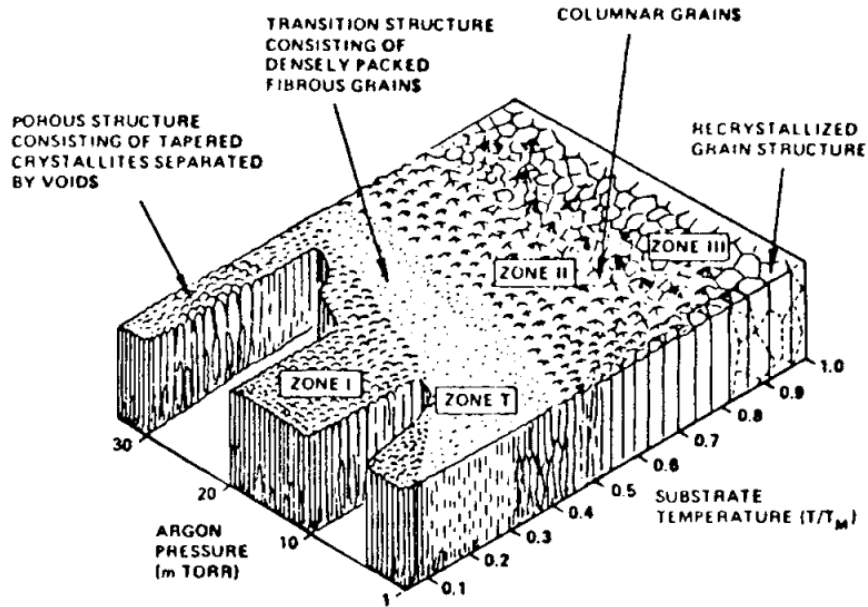


Figure 4-18: Generalized micro-structural zones in PVD films as related to pressure and  $T/T_M$ . [48] [50]

As a means to produce varying CdTe thickness, without adjusting the sublimation rate, the film thickness was compared to dwell time using a single source temperature (Figure 4-19). This was beneficial for investigation of CdTe thickness impact on the  $CdCl_2$  treatments, and ultimately the  $CdCl_2$  optimization for  $2\mu m$  CdTe.

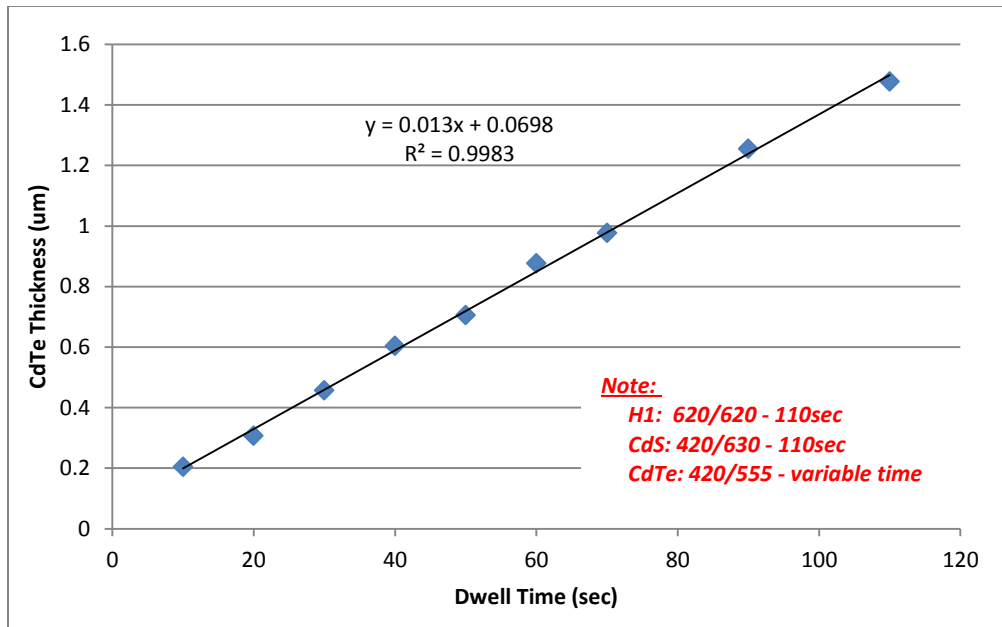


Figure 4-19: CdTe film thickness vs. deposition dwell time

As the process space for CdTe thickness was established, high surface roughness frequently resulted. The poorly coalesced grain structure and deep grain boundaries diminished the uniformity of  $CdCl_2$  treatment and

increased defects deep into the absorber layer. As identified by Sites [51], the primary causes of Voc loss in CdTe cells are a result of poor crystallinity. Others have also indicated the detrimental performance effects related to structural inhomogeneities emphasizing the need to improve the grain structure. [35]

As a first test, films were produced with various sublimation rates. The CdTe bottom source temperature was adjusted to achieve approximately .25, .5 and 1 $\mu$ m/min deposition rates, and the time interval adjusted to achieve the target film thickness. SEM was used to investigate the variation in microstructure. Cross sectional images are presented in Figure 4-20. These results confirm the 1 $\mu$ m/min growth rate was ideal for further development.

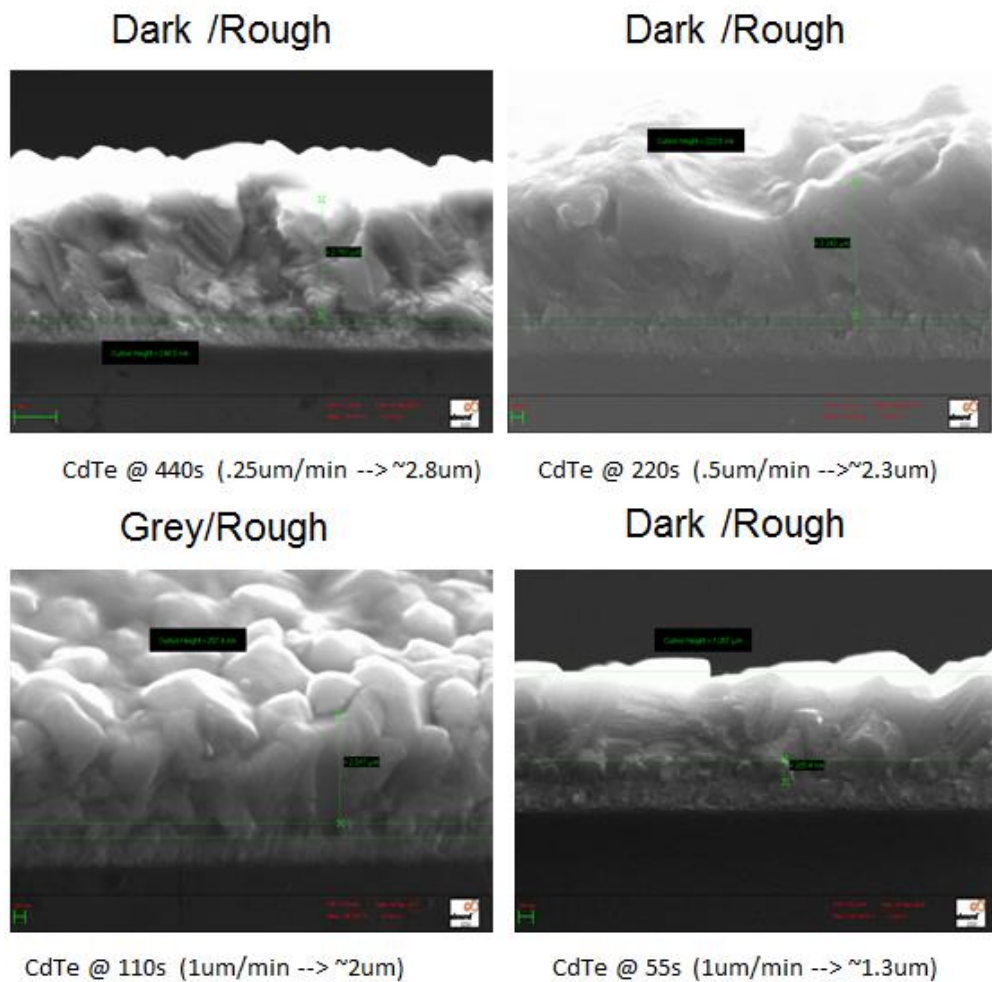


Figure 4-20: Cross sectional SEM images of CdTe microstructure resulting from different growth rates; visual appearance of the films are denoted above the image.

As the source shutter effectively maintains a closed condition of the source pocket, no gas exchange occurs except during sample ingress/egress. To increase the available O<sub>2</sub> content during deposition, the source to sample



clearance was increased to produce an “open” condition during deposition. The modification provided no improvement to the CdTe morphology, but a slight boost in performance. Multiple runs were performed to test the effect of substrate temperature and growth rate on the resulting CdTe morphology. Several combinations of process and substrate temperatures improved CdTe morphology, but all were detrimental to the overall device performance. Lower substrate entrance temperatures achieved by dropping CdS top, caused non-uniform CdS films to result. Hotter substrate entrance temperatures required significant increase in the CdCl<sub>2</sub> process temps to maintain performance. The final process profile selected maintained a compromise between uniformity, morphology and Voc performance.

As an alternative approach to improving the CdTe morphology, a CdCl<sub>2</sub> treatment of CdS prior to CdTe was investigated. This has been suggested by several groups as a means to improve the as deposited crystallographic quality of the CdS layer, recrystallizing and increasing grain size of lower energy deposition techniques [52]. Testing of this concept in the ARDS was accomplished by simple modification to the process sequence, allowing the CdCl<sub>2</sub> treatment to be performed between the established POR CdS and CdTe processing steps. A reduction in the CdTe roughness and improvement in the spatial uniformity of physical film qualities resulted. While the exact mechanism is not well understood in the ARDS, improvements to device performance were accomplished and are discussed in section 4.10.1 .

Additional runs were utilized to improve understanding of ARDS process parameters affecting CdTe growth. Unique samples were generated for Elipsometry, EL, PL, TRPL and CdTe morphology characterization. Concurrent optimization of the CdTe structure is necessary as CdCl<sub>2</sub> optimization is achieved.

#### 4.7 CdCl<sub>2</sub> Optimization

The benefit of annealing CdTe thin films in the presence of CdCl<sub>2</sub> is well recognized by the scientific community. Various techniques have been utilized and investigated since its discovery in 1976 [53], yet little is known about the precise mechanisms resulting performance enhancement [54]. As grown CdTe films have a high density of intrinsic defects, limiting the cell performance. A high temperature CdCl<sub>2</sub> treatment of CdTe films deposited by CSS results a significant improvement in device performance [55]. An effective CdCl<sub>2</sub> process is a function of time and temperature in the presence of reactive Cl<sub>2</sub> and O<sub>2</sub> species. High temperature CdCl<sub>2</sub>:O<sub>2</sub> treatments have been shown by many groups to be an effective technique for activating the photojunction and producing stable devices. Solid phase CdCl<sub>2</sub> treatments are more effective, but increase material consumption and

are potentially not as uniform.  $\text{CdCl}_2$  treatments are known to relax CdTe film strain and improve crystallography, increase the CdS-CdTe inter-diffusion and increase effective carrier lifetime. [56] [57] Both solid phase and isothermal  $\text{CdCl}_2$  techniques were evaluated in the ARDS; ultimately a solid phase process was utilized for this research.

The introduction of  $\text{CdCl}_2$  to the process revealed a control deficiency affecting the CdS deposition. Residual  $\text{CdCl}_2$  deposits on the end effector suppressed the deposition of CdS on subsequent samples. Incremental improvement was observed for subsequent CdS films when no  $\text{CdCl}_2$  processing was performed. This observation necessitated a means to control end effector contamination. Chemical, mechanical and thermal cleaning methods were tested, and evaluated with XPS for incorporation of species into the CdS films. The thermal method was selected for repeatability and ease. Baking of the end effector after  $\text{CdCl}_2$  processing for ~440sec in the open heater station at ~620C, was determined to be sufficient for process control. The XPS data in Figure 4-21 represents the baseline film prior to CdTe processing, indicating < 0.1at% Te in the CdS film. The presence of Cl was later determined to be a post deposition handling issue, and was resolved. The data in Figure 4-22 was generated from a CdS film created immediately following a CdTe deposition and thermal end effector cleaning. It confirms the effectiveness of the thermal cleaning technique, and lack of Cl or Te contamination in the bulk CdS film.

Early testing revealed the need for additional chemical isolation between sources. The direct line of sight between components allowed the migration and re-deposition of materials throughout the machine. Partition shields were produced to provide a removable “getter”, capturing material exiting the sublimation source. As  $\text{CdCl}_2$  is a low vapor pressure material, migration and re-sublimation of material within the transfer galley was an issue. To control depositing  $\text{CdCl}_2$  at the entrance of upstream sources, the POR reduced the substrate temperature sufficiently in the strip source.

The treatment is highly process dependent and must be tuned to the particular film structure [58]. Precise control of the CdTe thickness is necessary for repeatable  $\text{CdCl}_2$  treatment, as subtle variations in thickness have significant impact on the  $\text{CdCl}_2$  effectiveness. A quality  $\text{CdCl}_2$  treatment must be achieved if Cu is to be used for creating a p-CdTe layer. Barth [59] demonstrated a strong correlation between initial performance and device stability for  $\text{CdCl}_2$  treated devices with no intentional Cu.

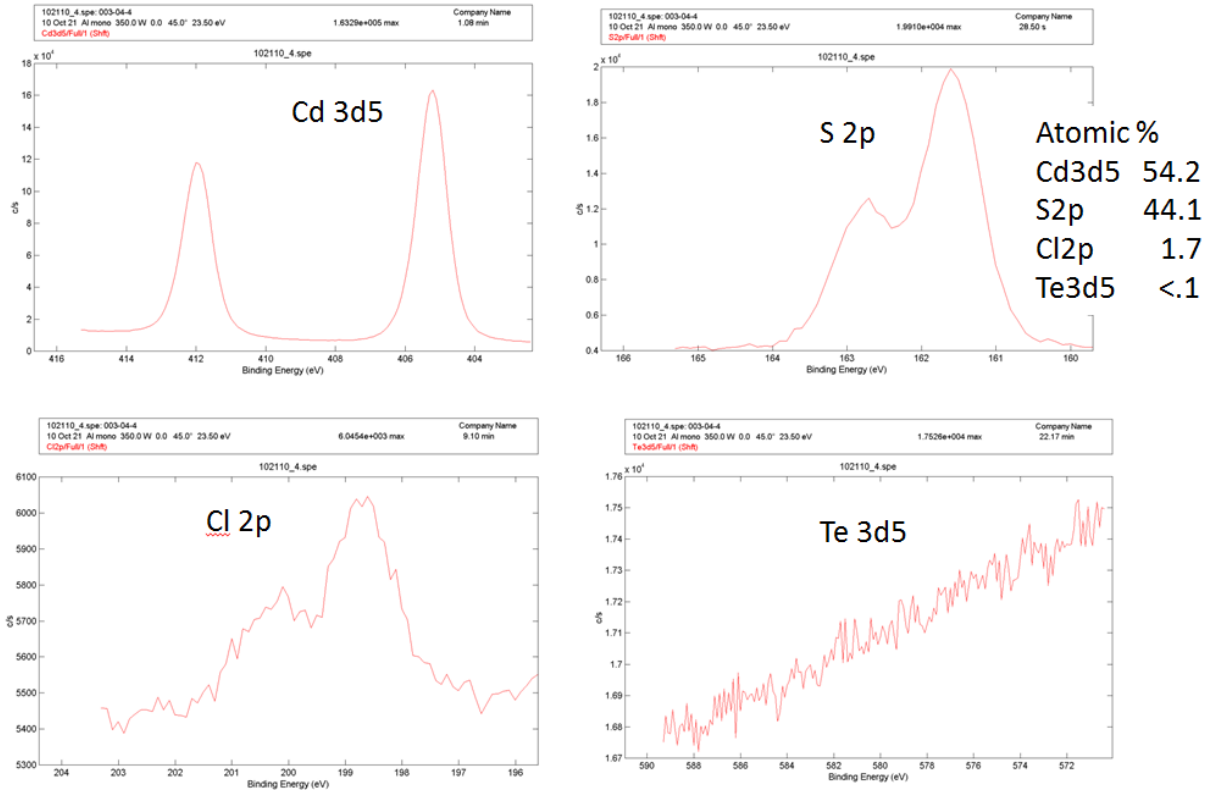


Figure 4-21: XPS of CdS film; Baseline prior to introduction of CdTe

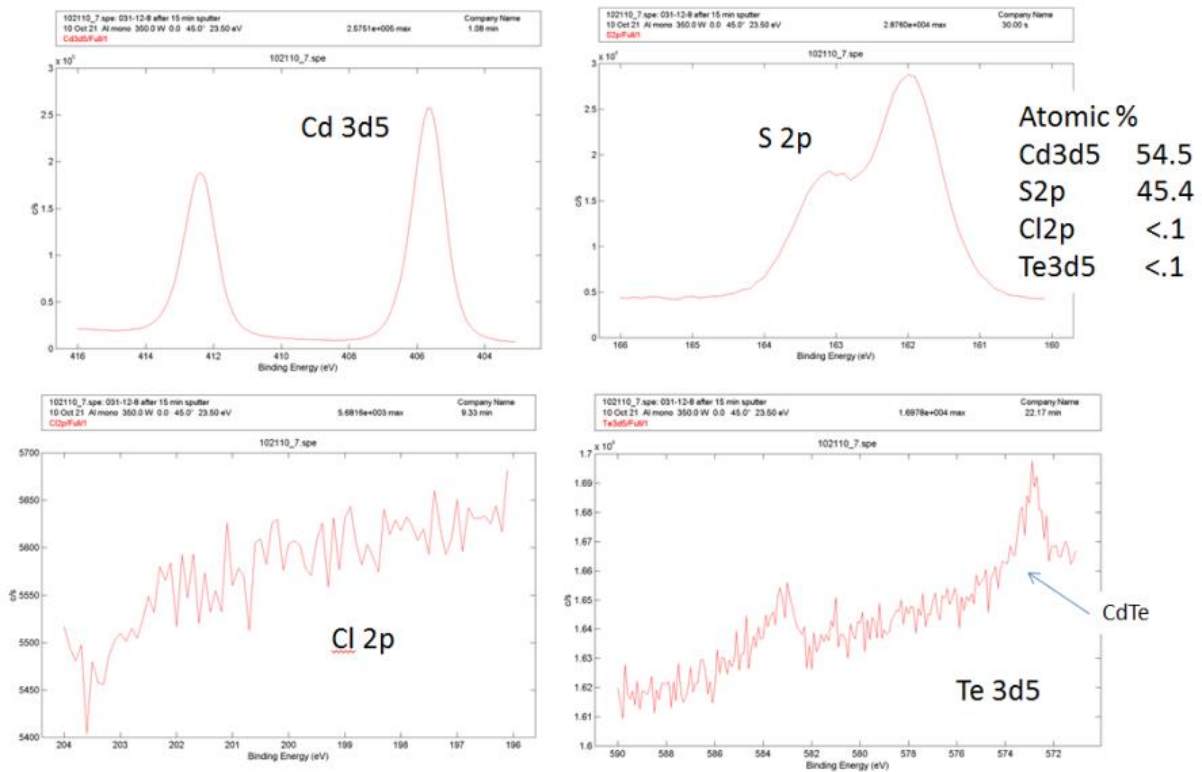


Figure 4-22: XPS of CdS Film post CdTe deposition and thermal bake of end effector; Analysis performed after sputtering ~24nm of material from surface to measure bulk composition

The historical CdCl<sub>2</sub> treatment was performed in multiple stages. First, a solid film of CdCl<sub>2</sub> material was deposited onto CdTe at the CdTe deposition temperature. Followed by, a vapor phase treatment at ~400C with elevated O<sub>2</sub> concentration. This treatment sequence was determined to be necessary to achieve best device voltage.. In the ARDS, CdCl<sub>2</sub> deposition occurs in a single source and can be defined as a single dwell, or multiple dwells. Identifying the process condition producing a uniformly thin CdCl<sub>2</sub> film is a first requirement, and is evaluated visually (Figure 4-23).

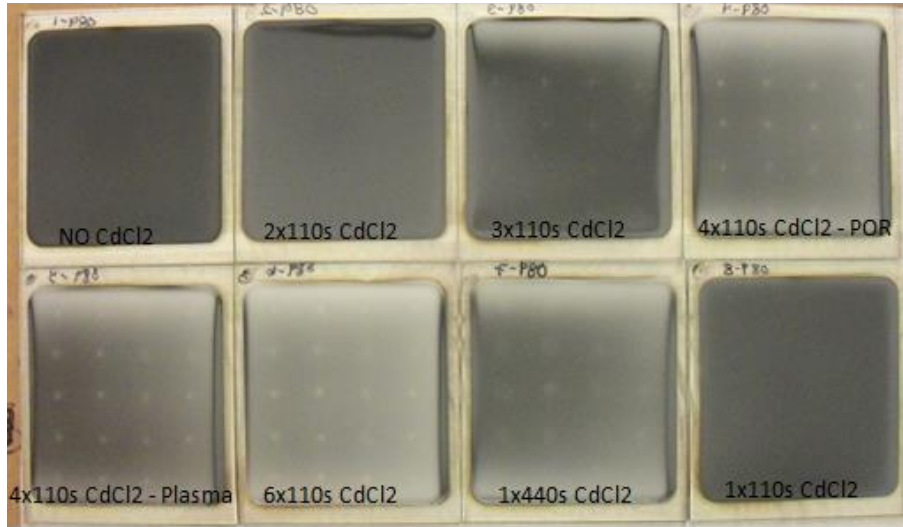


Figure 4-23: Visual haze patterns produced by varying CdCl<sub>2</sub> treatments

The presence of a CdCl<sub>2</sub> film is not sufficient to achieve an effective treatment. Device “activation” is accomplished by a high temperature anneal in the presence of CdCl<sub>2</sub>. The effectiveness of the treatment is time, temperature, and thickness dependent. Following the CdCl<sub>2</sub> anneal, the excess solid phase CdCl<sub>2</sub> is removed from the film in a reverse sublimation process. A heavy residual CdCl<sub>2</sub> film can impact the uniformity and effectiveness of the subsequent CuCl process. Optimization of the CdCl<sub>2</sub> treatment is highly interdependent on the previous process steps and difficult to decouple.

The Voc of a CdCl<sub>2</sub> treated film is a strong indicator of the CdCl<sub>2</sub> activation effectiveness. A target Voc>750mV was defined as a treatment baseline for process development. As a means to quickly evaluate the performance of the CdCl<sub>2</sub> process during experimentation, the device voltage is measured by a carbon dot. By applying only a carbon dot to the CdTe film, the film is protected from probe damage and the device voltage is acquired. Creation of the complete back contact requires approximately 12 hours for complete curing of electrode material, and does not allow process tuning during sample generation. While this test does not provide a precise measurement of the Voc, it does present an acceptable indicator of process status.

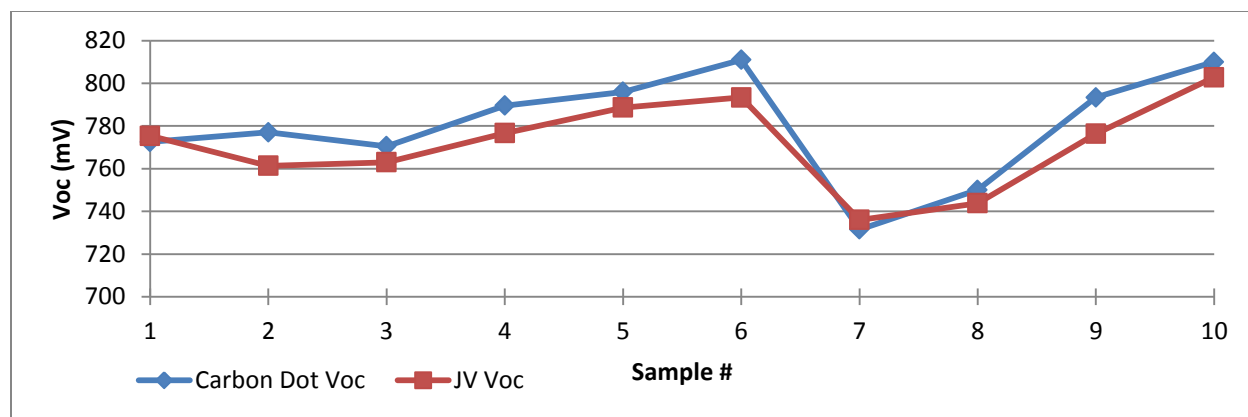


Figure 4-24: Comparison of carbon dot and J-V measured Voc for rapid feedback

The strong interdependence of CdTe thickness and CdCl<sub>2</sub> effectiveness necessitated continuous optimization as previous processing steps were modified. The ARDS accomplishes multivariate experimental research with ease, tuning CdTe thickness and testing CdCl<sub>2</sub> treatments simultaneously. This capability significantly reduced the required sample quantity, and resulting characterization.

Targeting a Voc > 750mV, incremental adjustments were made to walk the process in. As a starting point, single dwell treatments were explored. Single dwell results were consistently low, regardless of the anneal time (Figure 4-25). As with many breakthroughs, an accidental changed the direction of investigation. The closed pocket condition was suspected when a device was processed after the CdCl<sub>2</sub> shutter failed to close resulted improved Voc. It was thought that the combination of O<sub>2</sub> starvation and accumulation of TeCl<sub>2</sub> within the pocket may be limiting the effectiveness of treatment.

Two methods to remedy this issue were explored. The first was cycling of the substrate during deposition, allowing O<sub>2</sub> regeneration and venting of reactive byproducts from within the pocket. The cycling also provided a method to modify the substrate temperature, and alter the CdCl<sub>2</sub> anneal. The other method was to modify the source geometry such that a clearance existed between the sample and source pocket, resulting an “open” condition. Both methods proved beneficial and were included in the POR.

Incremental improvement is observed with increasing CdCl<sub>2</sub> exposure and temperature (Figure 4-26). The possible combinations of deposition temperature, duration, and cycles produced a wide process space and a narrow optimal zone. The result of various combinations of CdCl<sub>2</sub> dwell cycles and dwell time are presented in Figure 4-27 and Figure 4-28. Ultimately, a ~2μm CdTe layer and 4x110s CdCl<sub>2</sub> treatment resulted the best performance and repeatability for this hardware configuration.

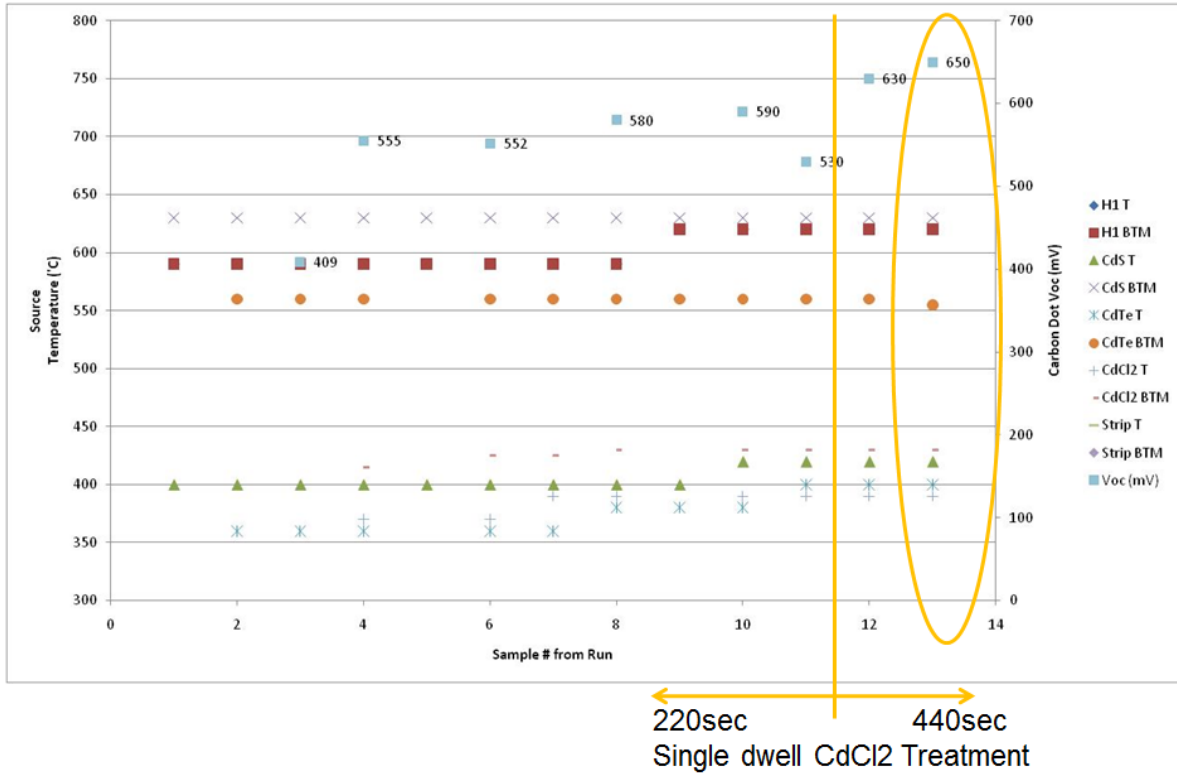


Figure 4-25: Single dwell deposition conditions and resulting Voc

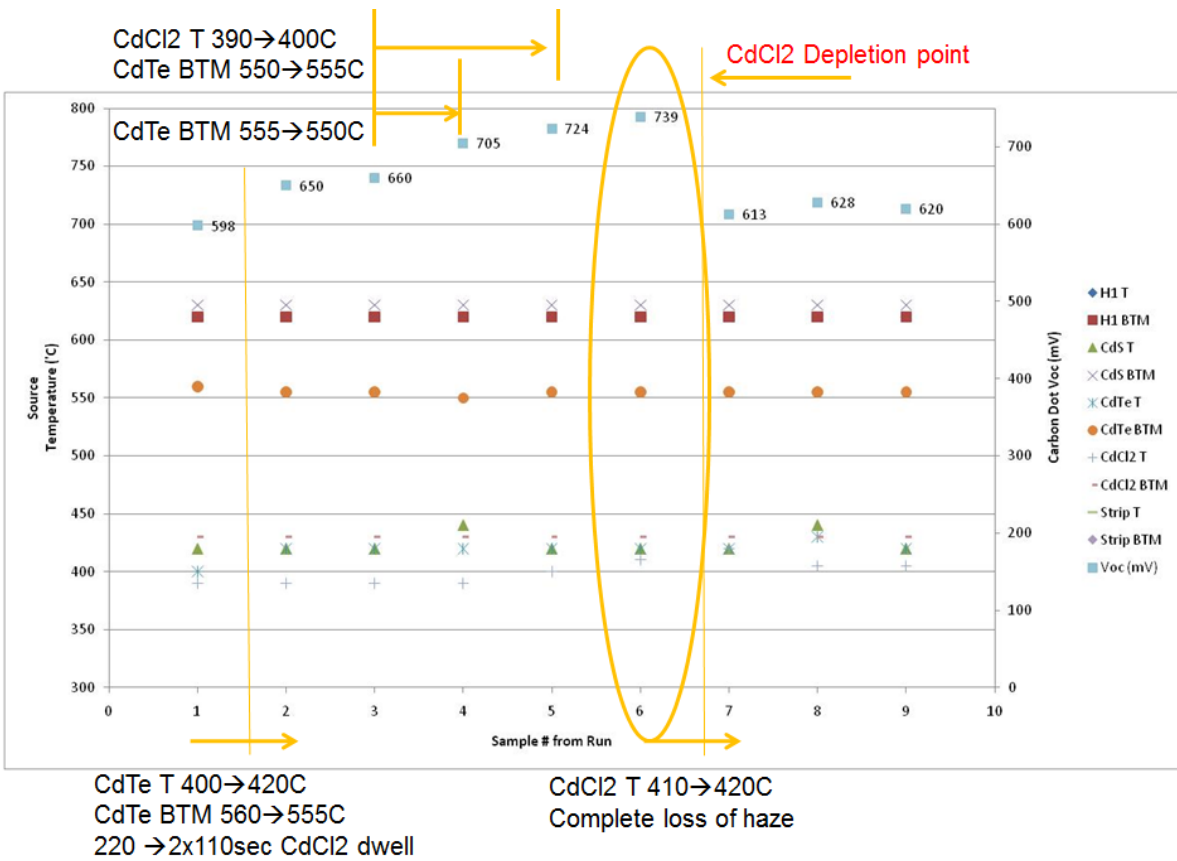


Figure 4-26: Multi-dwell deposition conditions and resulting Voc

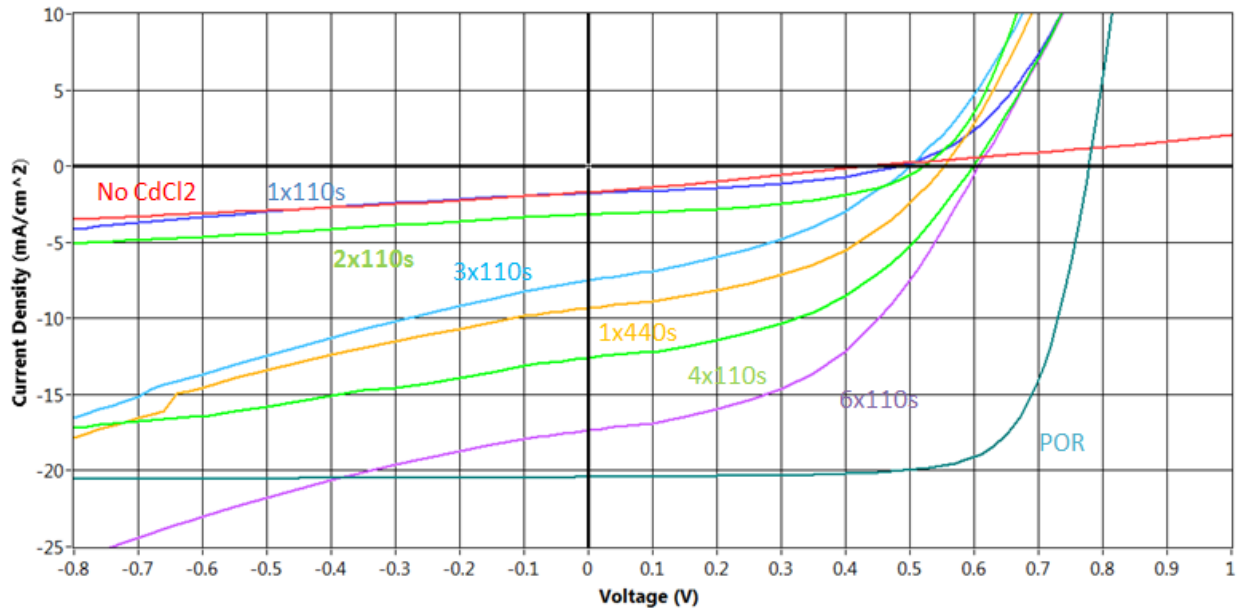


Figure 4-27: J-V of CdCl<sub>2</sub> process variations

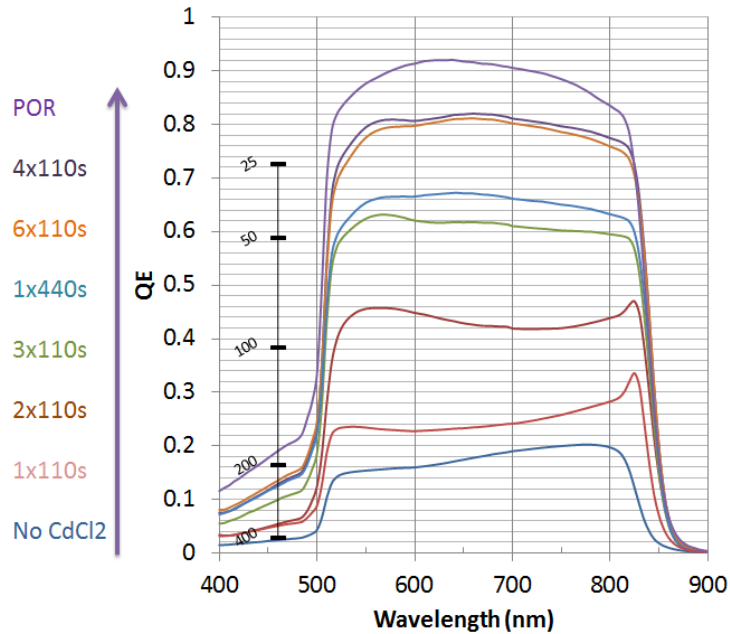


Figure 4-28: QE of devices with CdCl<sub>2</sub> process variations

To understand the elemental composition through the body of a film, Secondary Ion Mass Spectroscopy (SIMS) is employed. Samples are sputtered from the CdTe surface towards the substrate, with an increase in the sputter rate occurring at the CdS layer. The CdCl<sub>2</sub> annealing process causes the incorporation of Cl into the CdTe film. Evaluation of the diffusion profile of the Cl by SIMS indicates a high concentration near the back of the film, with reducing profile towards the CdS/CdTe interface (Figure 4-29). The intermixing of CdS and CdTe is also

detectable, as indicated by the Sulfur diffusion into the CdTe layer. Both mechanisms are well supported in literature and are believed to benefit the device performance [54] [57] [60].

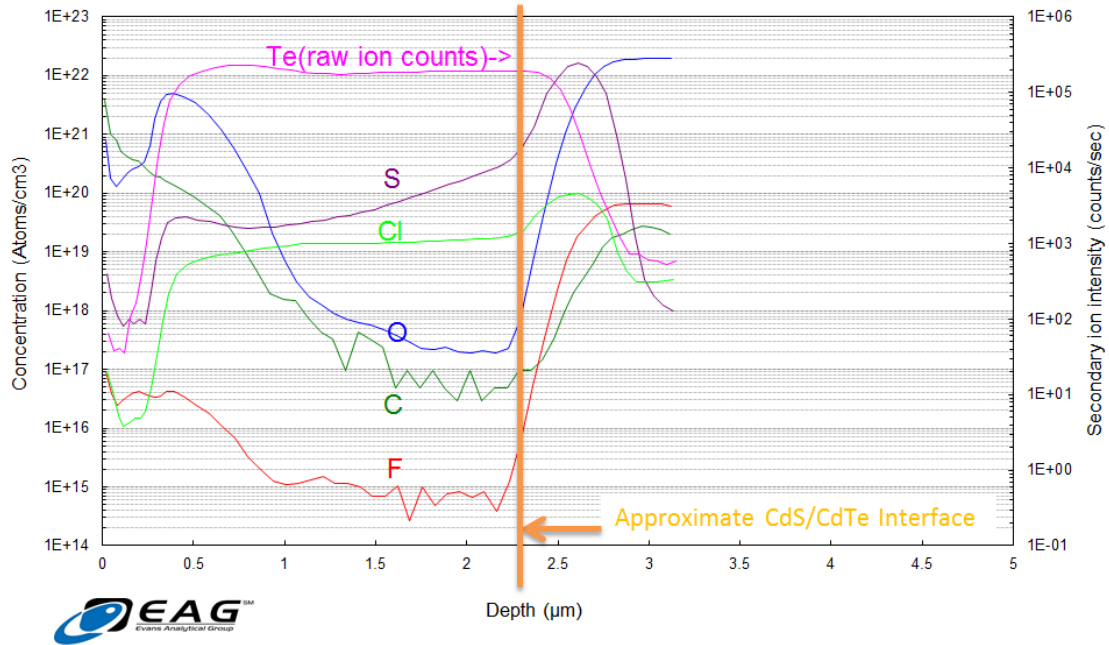


Figure 4-29: SIMS profile of no-Cu CdTe film; Analysis performed by EAG

Samples for characterization to investigate the effect of annealing treatments on as deposited CdTe films were supplied to Loughborough Materials characterization center. High resolution SEM images of the CdTe surface morphology before and after receiving the CdCl<sub>2</sub> treatment (Figure 4-30), indicate no effect on the grain size as a result of the treatment. This result is common with CdTe films grown at high temperature. Transmission Electron Microscopy (TEM) images in Figure 4-31, indicate a change in the stacking faults and densities as a result of annealing conditions [61] [62]. Further research to understand the mechanisms related to the recrystallization of CdTe was performed, developing relationships between electrical performance and micro-structure. [63]



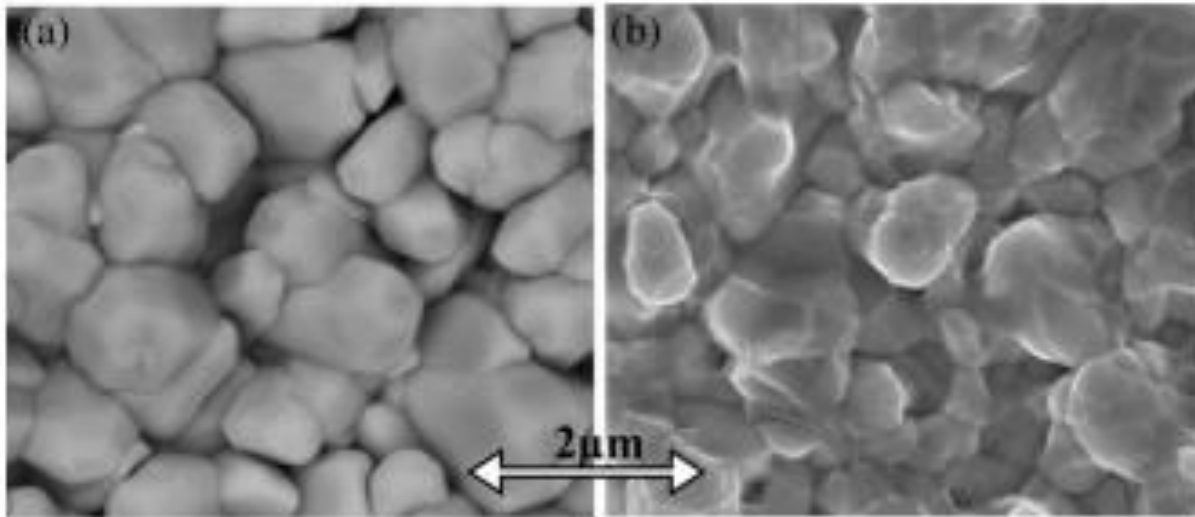


Figure 4-30: SEM micrograph of the surface (a) untreated and (b) cadmium chloride treated CdTe cell [62]

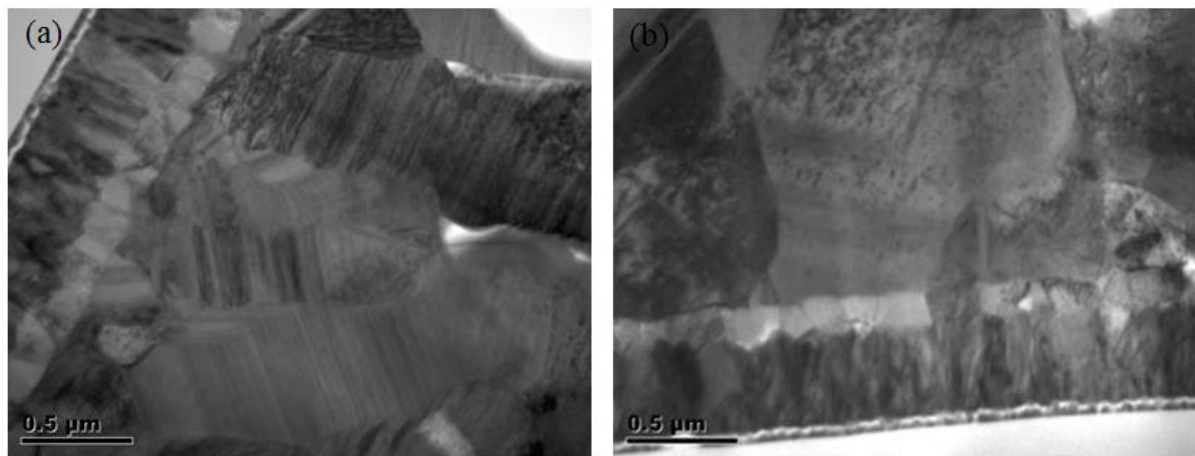


Figure 4-31: TEM image of CdTe cell before (a) and after (b) CdCl<sub>2</sub> treatment [62]

#### 4.8 CuCl process optimization

The formation of an ohmic contact by introduction of a low concentration of Cu has been demonstrated by several groups. Achieving stable device performance requires controlling the incorporation of Cu, as excess Cu<sup>+</sup> is found to diffuse and accumulate in the depletion region forming recombination centers and limiting device lifetime and degrading FF and Voc. Device degradation can occur on various time scales and by various mechanisms. [64] [59] Device stability is critical for the success of solar energy, and is highly scrutinized in industry.

The ARDS deposits CuCl via CSS at low substrate and sublimation temperatures forming a doped CdTe region at the back. Doping profiles are measured by C-V, indicating approximate surface and bulk concentrations. The target process space provides a modest boost in the Voc and FF due to the improvement of series resistance but does not demonstrate performance loss under light soak and heat.

Initially, the Cu treatment occurred in two steps. The first treatment was done at an elevated substrate temperature of ~400°C with a low CuCl sublimation. The film temperature induced diffusion of a low concentration of Cu into the bulk of the CdTe. After cooling the substrate to ~100°C, a second treatment with an elevated CuCl sublimation was performed. The low film temperature produced a surface deposition reducing the contact resistance to the back electrode. Finally, a low temperature anneal is performed to stabilize the Cu profile in the CdTe.

The introduction of Cu occurred with the 19<sup>th</sup> run on the ARDS. Interpretation of J-V, C-V and QE results indicated CdCl<sub>2</sub> and Cu optimization was necessary. An additional DOE was executed to increase the CdCl<sub>2</sub> treatment and reduce Cu incorporation, leading to the first 12% solar cell after just 20 runs. Additional optimization to reduce the bulk and surface Cu concentrations were critical to stabilizing device performance. High bulk Cu produces excellent instantaneous performance, but has a rapid and unrecoverable deterioration. High surface concentrations diffuse towards the junction over time, especially at elevated temperatures and results a gradual degradation.

A concise progression of varying Cu treatments investigated from this research is presented below. Device parameters derived from J-V measurement are found in Table 4-2, the corresponding graphs in Figure 4-32. A significant improvement in Voc and Rsh boost FF and device η. The C-V measurement does not give absolute carrier densities as there are many confounding interactions, but is useful for comparative analysis. Comparison of carrier density profiles as measured with C-V and presented in Figure 4-33, demonstrate the effect of Cu content and placement within the CdTe film. Concentrations of 10<sup>13</sup> atoms/cc in bulk and 10<sup>16</sup> at the back has been found to be adequate. Only subtle variation are observed with QE but are presented in Figure 4-34 for completeness.

Table 4-2: J-V parameters resulting from varying Cu conditions and corresponding to Figure 4-32

<b>Sample Description</b>	<b>VOC (mV)</b>	<b>JSC (mA/cm<sup>2</sup>)</b>	<b>Fill Factor (%)</b>	<b>Efficiency (%)</b>	<b>RS (Ω)</b>	<b>RSh (Ω)</b>
As Deposited CdTe	397.7	1.7	26.2	0.2	134.8	542.3
CdCl <sub>2</sub> , No-Cu	730.3	21.7	50.6	8.0	33.4	1136.2
Low-Cu	781.0	19.6	51.0	7.8	49.2	1622.3
2 Step Cu	796.7	19.6	73.0	11.4	1.0	1248.2
High-Cu	797.3	19.4	51.0	7.9	43.1	587.5
POR	778.7	20.8	76.0	12.3	0.5	4679.8

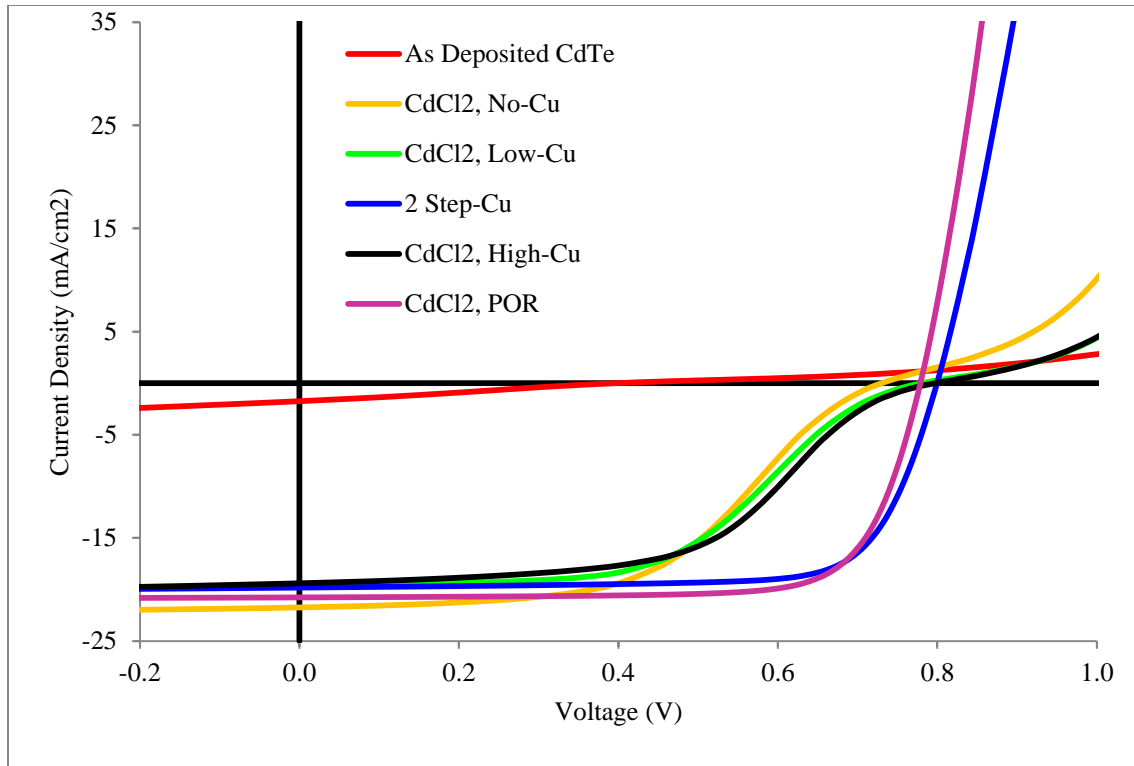


Figure 4-32: J-V results of varying Cu conditions

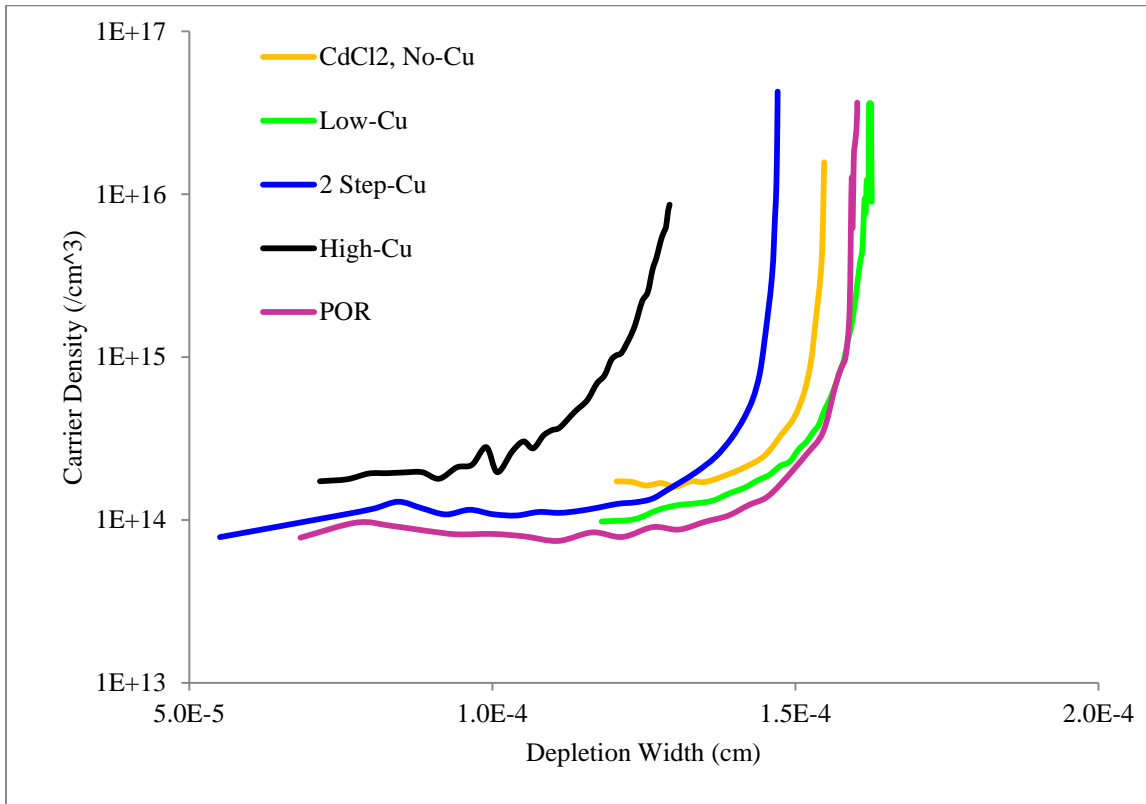


Figure 4-33: C-V results of varying Cu conditions

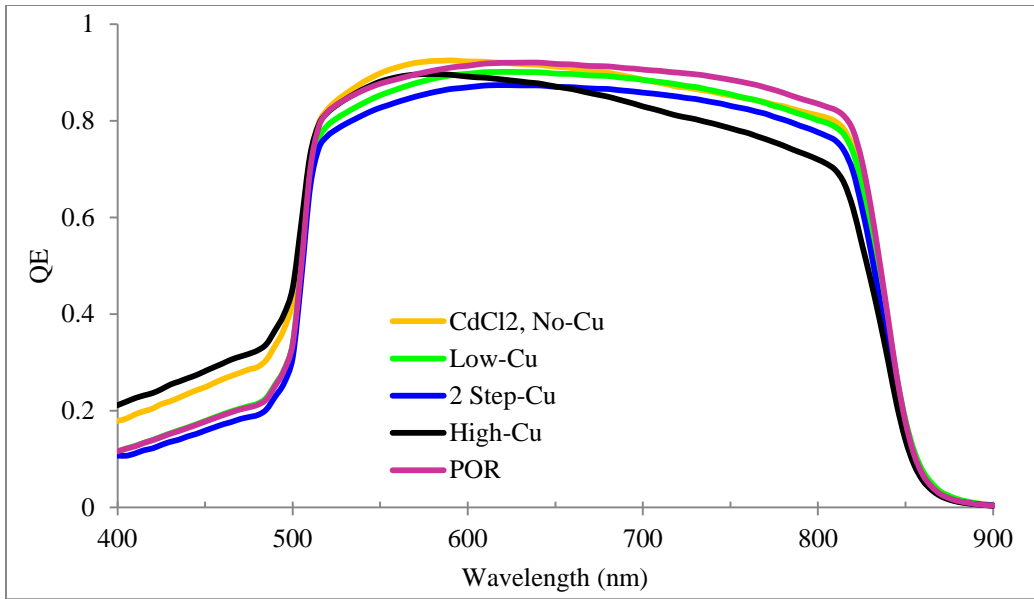


Figure 4-34: QE results of varying Cu conditions

Several variations of the Cu sequencing were investigated and compared for diagnostic purpose. Samples were generated utilizing the flexibility of the ARDS, and the CSU PV Characterization Lab performed in depth analysis. Comparison of dark and light J-V measurements is beneficial in determining diode quality and is presented in Figure 4-35. All devices demonstrate weak diode behavior and back barrier effects. The poor CdCl<sub>2</sub> treatment is easily masked with high Cu content, which is not desirable for device stability, but is detectable in C-V as seen in Figure 4-36.

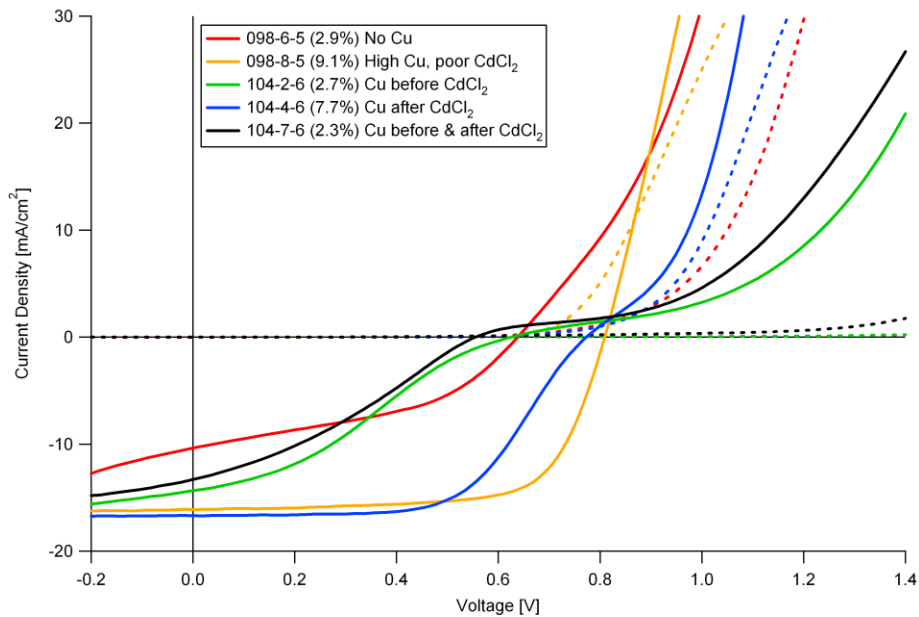


Figure 4-35: Dark/Light J-V for various CdCl<sub>2</sub>/Cu sequencing, measurements by R. Geisthardt [65]

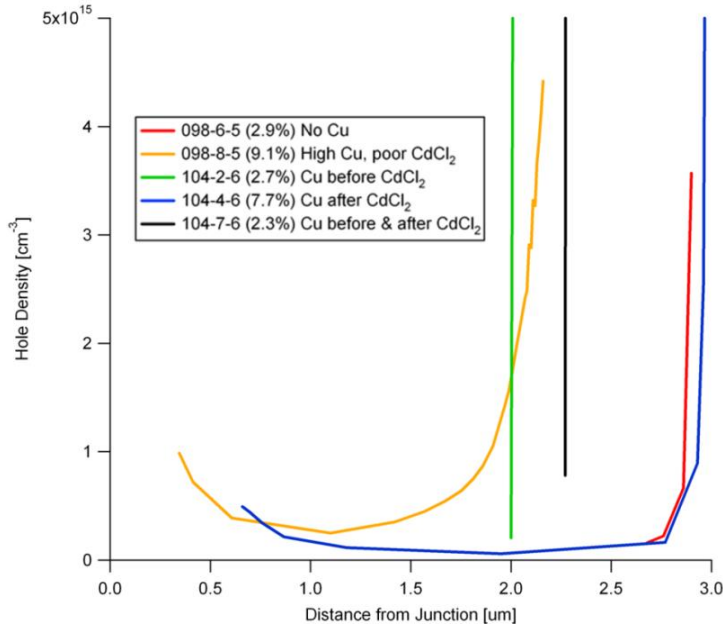


Figure 4-36: C-V for various CdCl<sub>2</sub>/Cu sequencing, measurements by R. Geisthardt [65]

#### 4.9 Device optimization and Process of Record

Over one hundred separate runs were performed to achieve confidence that the ARDS hardware and process were characterized sufficiently to proceed with the next phase of research. Continuous hardware and process optimization was performed resulting a reliable research tool capable of producing nearly one hundred unique, full process samples, between routine preventative maintenance. Over the duration of this research, the continuous optimization of hardware and processes to improve the ARDS operation was necessary. Not all runs were required to produce the POR, but all samples supported process to performance understanding.

Sample frequency depends on the desired structure. Typical completed films, with CdCl<sub>2</sub> and Cu treatment, are produced in ~48min intervals, from substrate introduction to sample exchange. Partial structure samples are produced according to the process times in Table 4-3. The recipe used to produce the POR devices in this study is presented in Table 4-4, and represents source temperatures and deposition dwell time. Subsequently, a single step Cu process was developed that has resulted improved device stability.

Table 4-3: ARDS processing times required to produce indicated sample structure

<b>Approximate Process Times:</b>	
CdS:	13 min
CdS/CdTe:	15 min
CdS/CdTe/CdCl <sub>2</sub> :	24 min
CdS/CdTe/CdCl <sub>2</sub> /Cu:	36 min

Table 4-4: ARDS POR recipe for 12% device efficiency

POR Recipe				
Position	Process	Top Temperature (°C)	Bottom Temperature (°C)	Dwell (sec)
P1	Heating	620	620	110
P2	CdS	480	630	110
P3	CdTe	360	565	110
P4	CdCl2	410	435	4x110
P5	Strip	140	140	110
P6	Cu1	115	115	110
P7	Cool	50	50	500
P8	Cu2	150	220	110
P9	Anneal	200	200	220
Environment	40mT	>67sccm	2% O2/BalN2	

Achieving process uniformity within a large sample is desirable, but not always necessary for research systems like the ARDS. The spatial distribution of performance can be used to understand a subtle variation in processing conditions when careful analysis is performed. Spatial uniformity of device performance from the ARDS showed improvement over the course of an experiment. This is attributed to the large thermal mass of the hardware, and represents a time constant that should be considered for precise process control. The J-V results in Figure 4-37 represent the spatial performance achieved within a single sample after 7hrs of operation. Subsequently, spatial uniformity has been improved with modified hardware and process tuning.

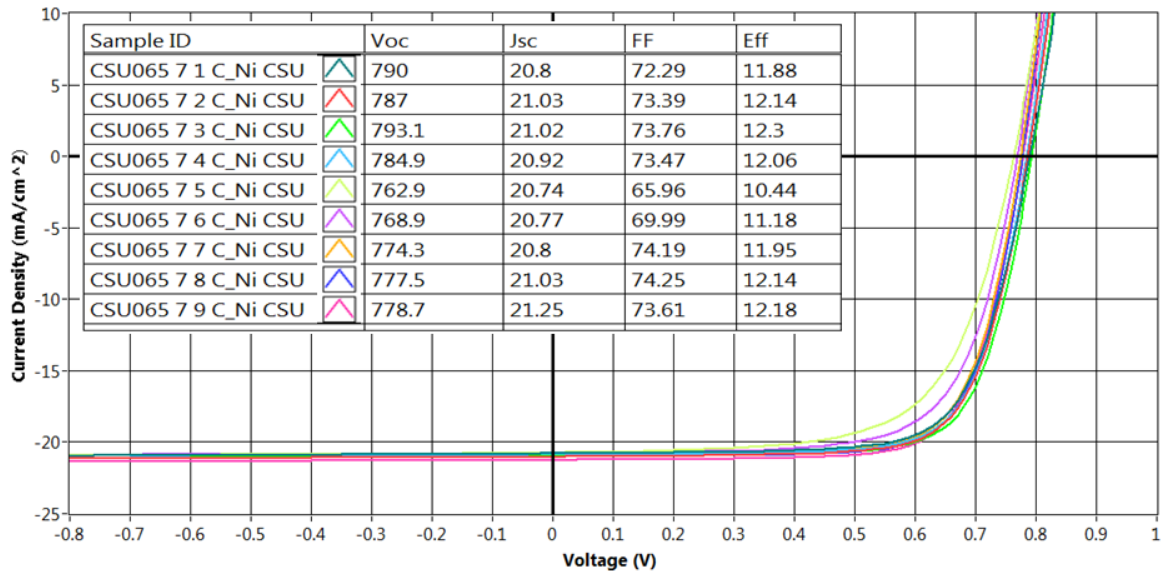


Figure 4-37: Spatial uniformity of single sample measured at 9 device locations.

Process repeatability within run, and from run-to-run, is most critical to achieving meaningful results and building strong process correlations. Comparing a single device location, over 7 samples, generated within a single

run, are presented in Figure 4-38. These results are consistent with the process control demonstrated over a larger period of time.

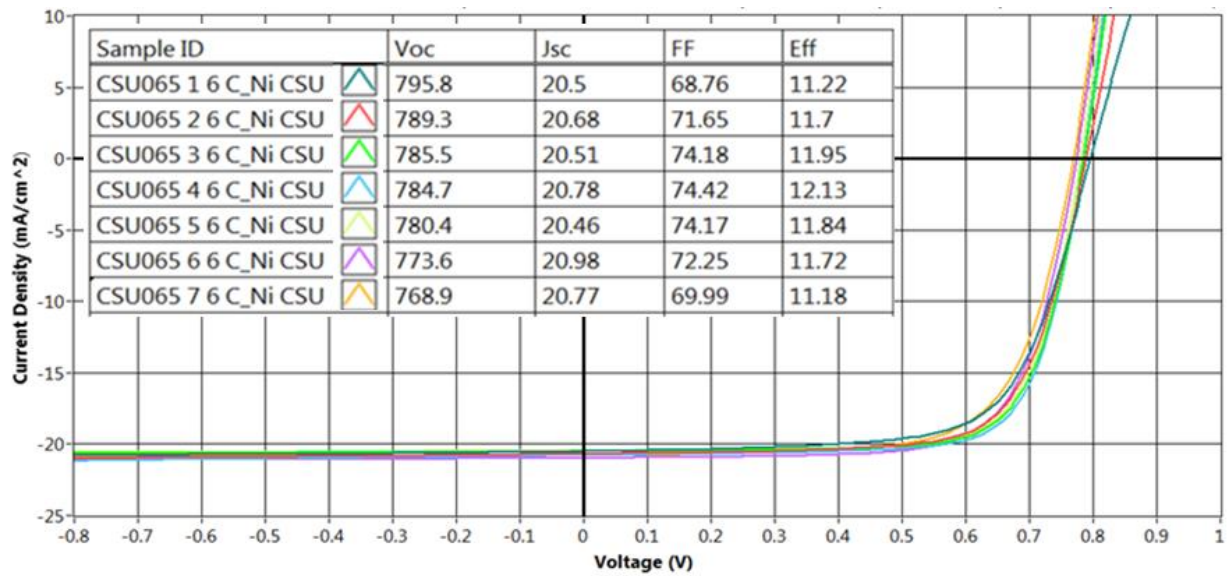


Figure 4-38: J-V measurements of 7 samples produced in a single repeatability experiment

Process repeatability is a critical metric used to describe tool capability. The ARDS has a high degree of repeatability as confirmed over 40 runs. Processing conditions were maintained, with minor tuning to reduce Cu treatment for improved device stability. A comparison of J-V, C-V, and QE results for the devices fabricated are presented Figure 4-39, Figure 4-40 and Figure 4-41 respectively. The individual POR champion parameters achieved with the ARDS during this study, on commercially available TEC10 follow in Table 4-5, and would result a 13.2% device if achieved in a single sample.

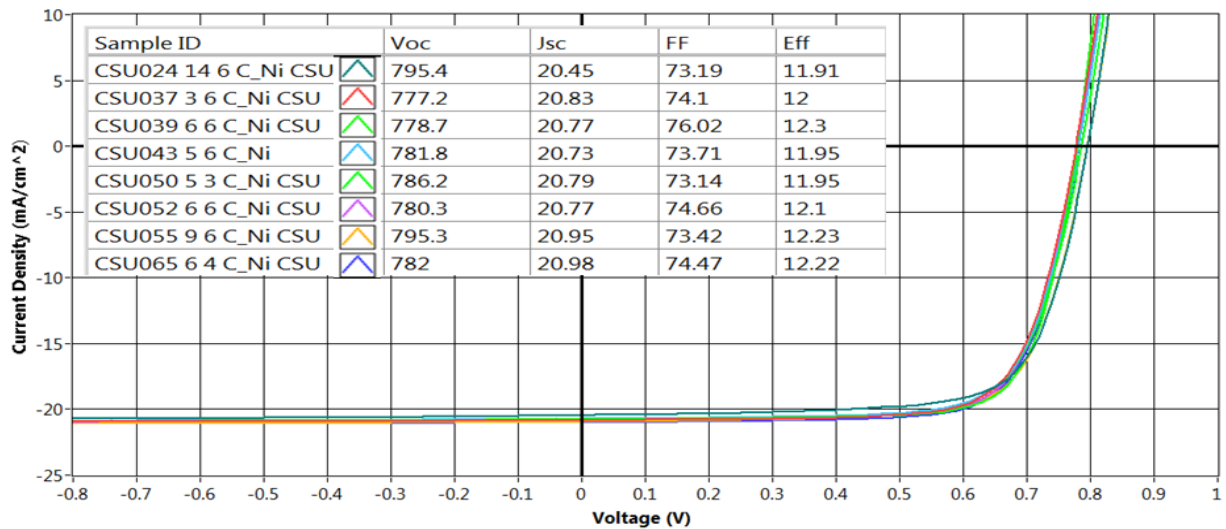


Figure 4-39: J-V comparison of POR samples over 40 runs

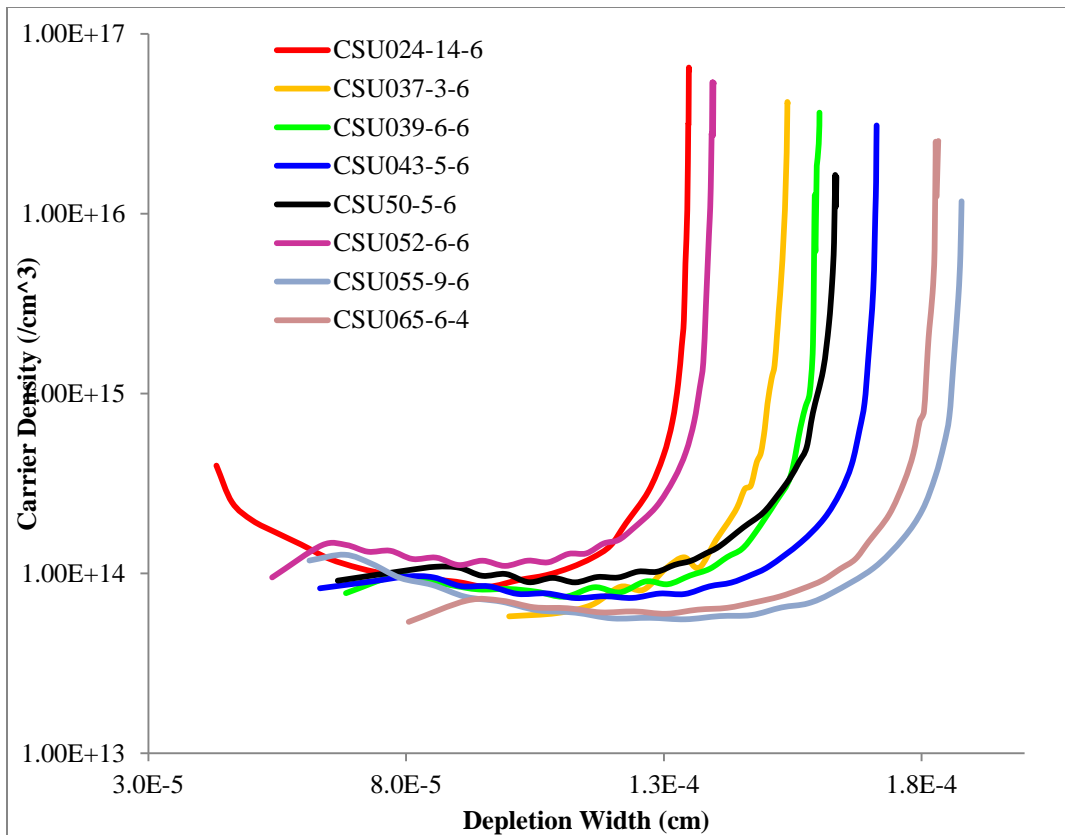


Figure 4-40: C-V comparison of POR samples over 40 runs

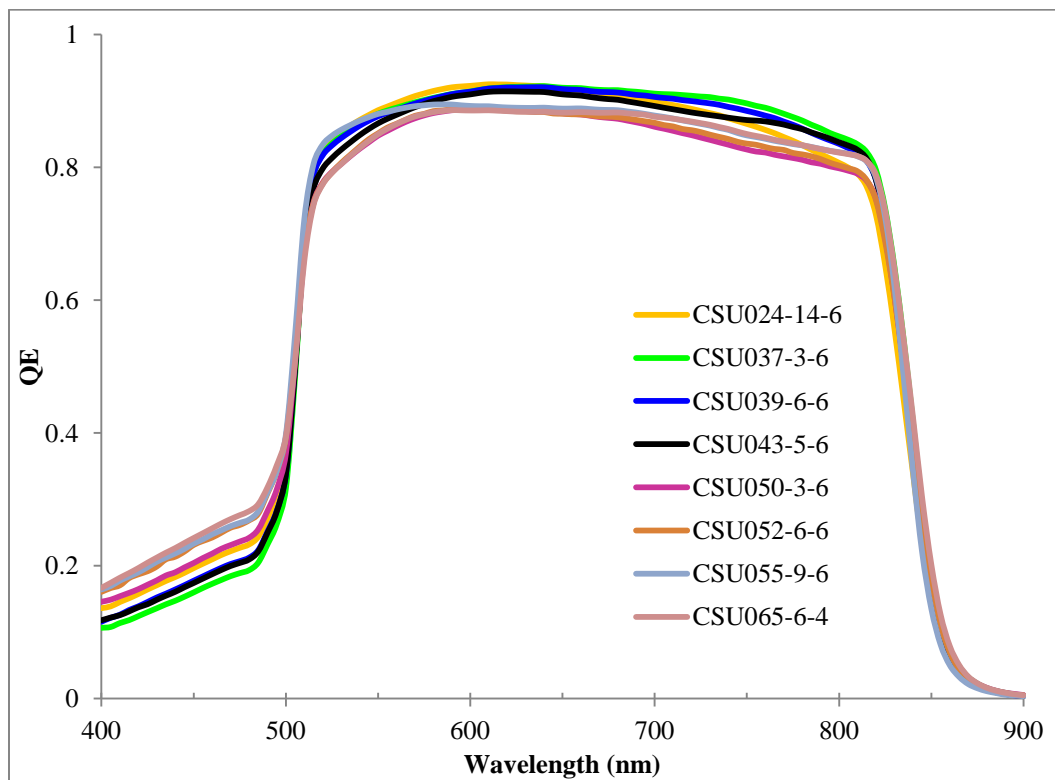


Figure 4-41: QE comparison of POR samples over 40 runs



Table 4-5: ARDS TEC10 champion parameters of individual samples produced during this study

ARDS TEC10 Individual Parameter Champions	
Voc:	809mV
Jsc:	21.5mA/cm <sup>2</sup>
FF:	76%
η:	12.30%
<b>η<sub>calculated</sub></b>	<b>13.22%</b>

#### 4.10 Additional Studies

##### 4.10.1 Intermediate CdCl<sub>2</sub> treatment of CdS prior to CdTe (CdS/CdCl<sub>2</sub>/CdTe)

The intermediate treatment of the CdS layer by high temperature CdCl<sub>2</sub> prior to the deposition of CdTe has been shown to induce CdS recrystallization, reduce inter-diffusion and modify the subsequent CdTe microstructure [66]. The chemical affinity of CdS and CdTe result the formation of zinc blend CdTe<sub>1-x</sub>S<sub>x</sub> and wurtzite CdS<sub>1-y</sub>Te<sub>y</sub> alloys near the junction, effectively lowering the bandgap of the CdS window layer. High temperature CdCl<sub>2</sub> treatment of the CdS layer prior to the deposition of CdTe, have demonstrated the ability to minimize the formation of the CdS<sub>1-y</sub>Te<sub>y</sub> alloy by limiting the diffusion of Te into the CdS layer [66]. This should result gains in Jsc and maintain the CdS bandgap as observed with QE.

The technique was investigated with the ARDS and resulted improvements to CdTe morphology, film uniformity and device performance. Several variations of the intermediate CdCl<sub>2</sub> process step were performed to develop an understanding as to whether the CdCl<sub>2</sub> treatment or temperature was responsible for the observed changes. Variable intermediate CdCl<sub>2</sub> dwell times were also tested and discovered very short (~25sec) intermediate treatments still had an impact on the CdTe morphology. The intermediate CdCl<sub>2</sub> process will be denoted CdS/CdCl<sub>2</sub>/POR when completed devices are discussed.

To achieve the best comparison of results, a POR sample and CdS/CdCl<sub>2</sub>/POR sample were generated sequentially such that CdS and CdTe thickness are maintained, and all other processing conditions are identical. The J-V results of this single test are presented in Table 4-6 and Figure 4-42. An increase in the Voc and FF are observed. The QE curve in Figure 4-43 suggest a tighter CdS band possibly due to less intermixing. A larger depletion width is observed in the C-V measurement in Figure 4-44.

Table 4-6: J-V results of POR and CdS/CdCl<sub>2</sub>/POR devices generated sequentially

Sample ID	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	Fill Factor (%)	Efficiency (%)	RS (Ω)	RSh (Ω)
POR	774.5	20.9	70.2	11.4	0.8	2540.9
CdS/CdCl <sub>2</sub> /POR	795.3	20.9	73.4	12.2	0.5	4083.7

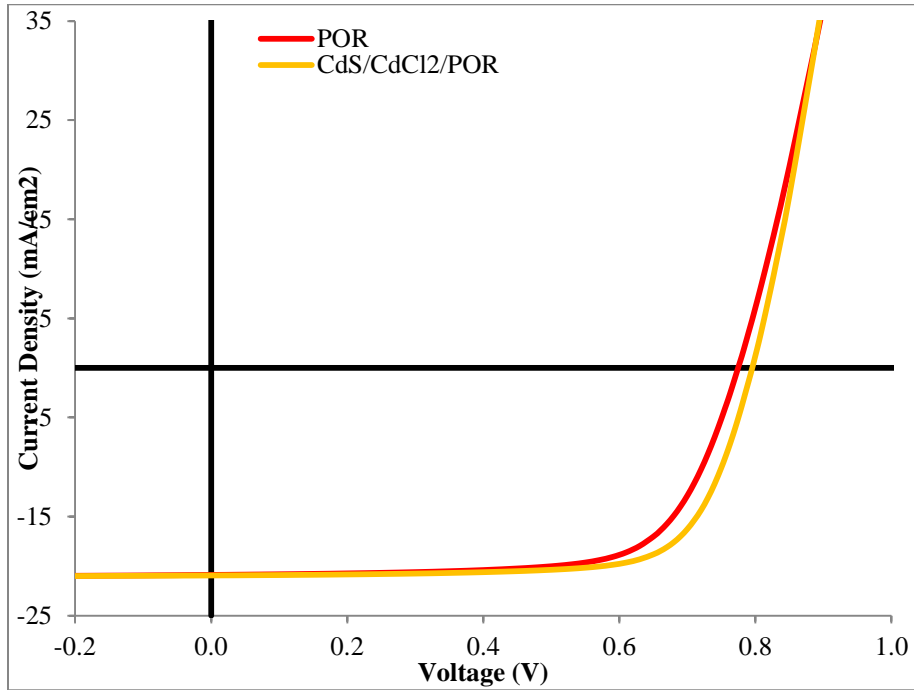


Figure 4-42: J-V of POR and CdS/CdCl<sub>2</sub>/POR devices generated sequentially

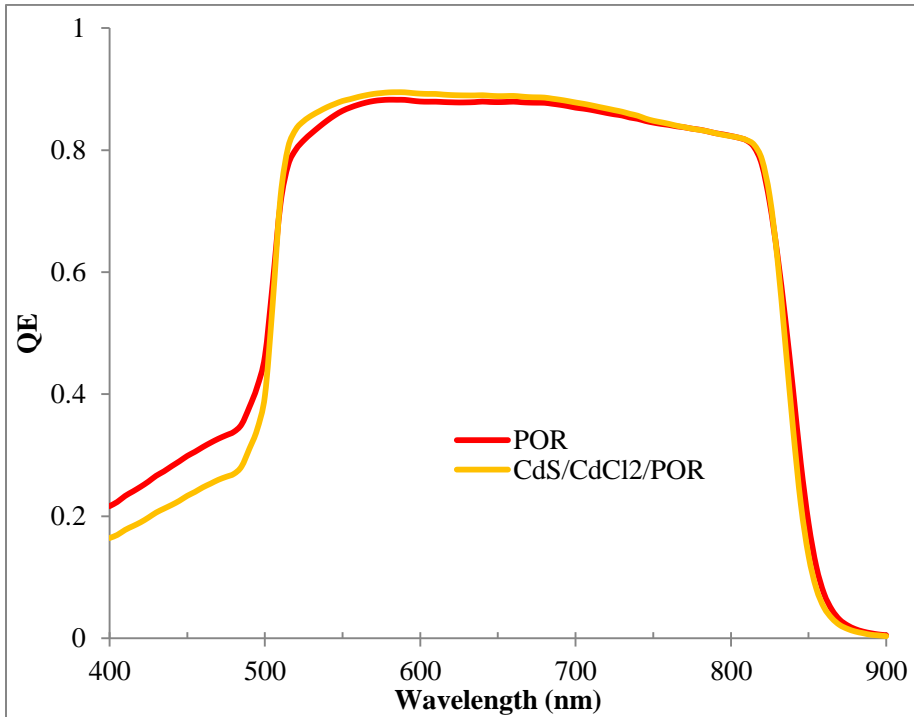


Figure 4-43: QE comparing POR and CdS/CdCl<sub>2</sub>/POR generated sequentially

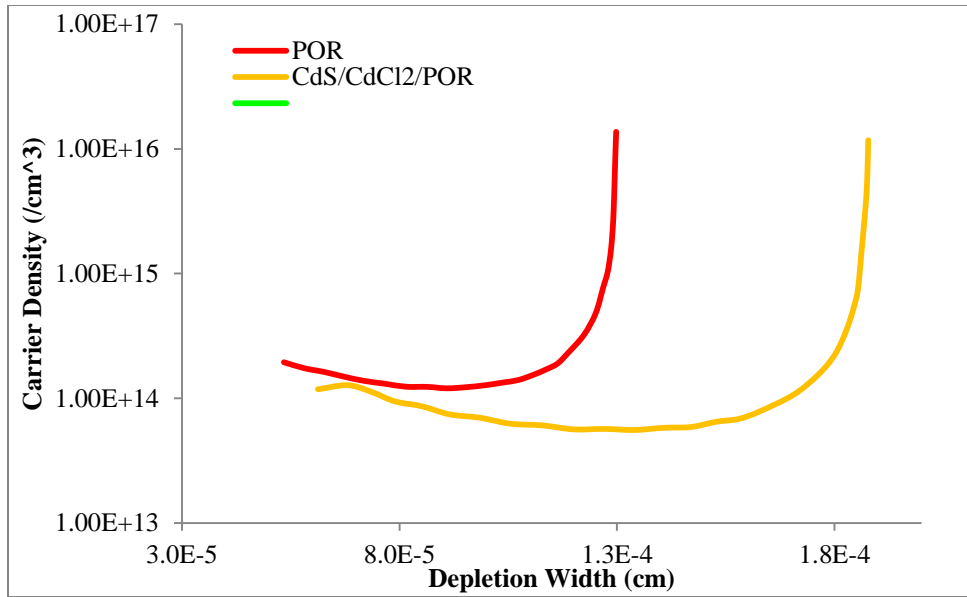


Figure 4-44: C-V comparing POR and CdS/CdCl<sub>2</sub>/POR generated sequentially; nominally same thickness

The modified treatment produced a significant improvement in the CdTe morphology. An optical image of the CdS/CdCl<sub>2</sub>/POR and POR films is presented in Figure 4-45. The intermediate treatment produces a bright gray, reflective film while the POR is dark and dusty in appearance. The SEM comparison in Figure 4-46 and Figure 4-47 demonstrates the reduction of surface topography and denser CdTe layer as a result of the treatment. Both samples received an identical CdCl<sub>2</sub> treatment post CdTe. An increase in the CdTe lateral grain size is observed with the 3D AFM rendering in Figure 4-48

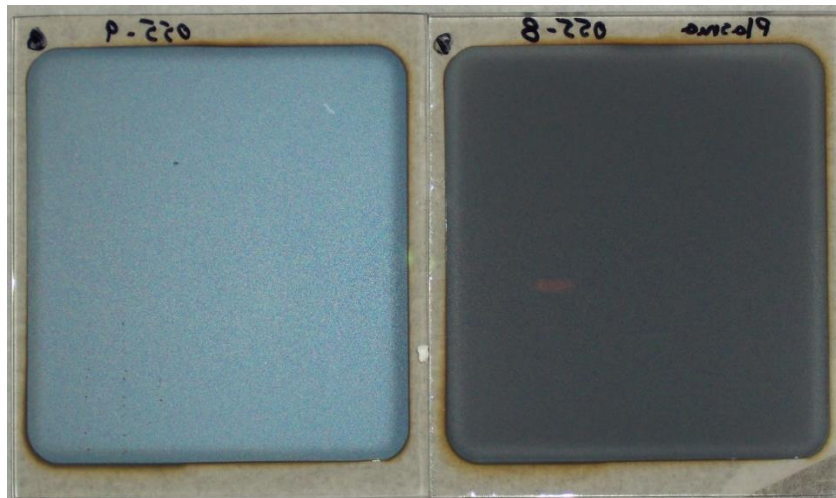


Figure 4-45: Optical comparison of CdS/CdCl<sub>2</sub>/POR (Left) and POR films (Right)

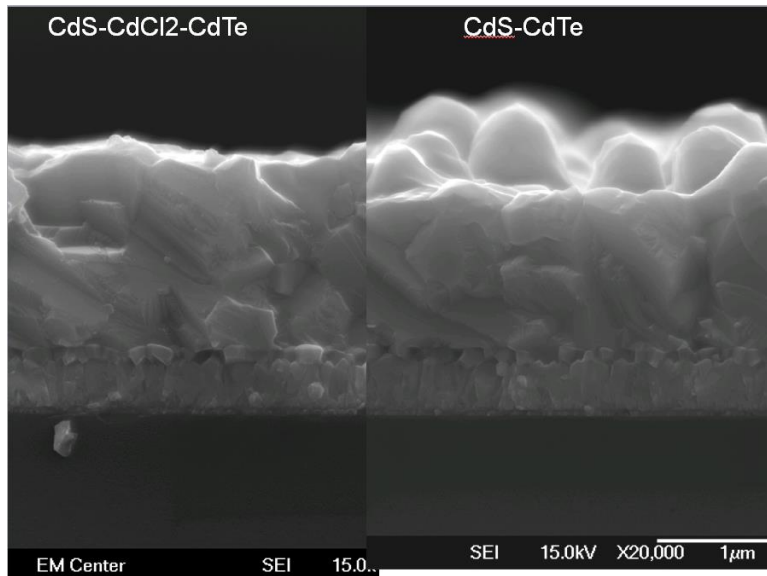


Figure 4-46: SEM cross-sections of CdS/CdCl<sub>2</sub>/CdTe (Left) and CdS/CdTe (Right)

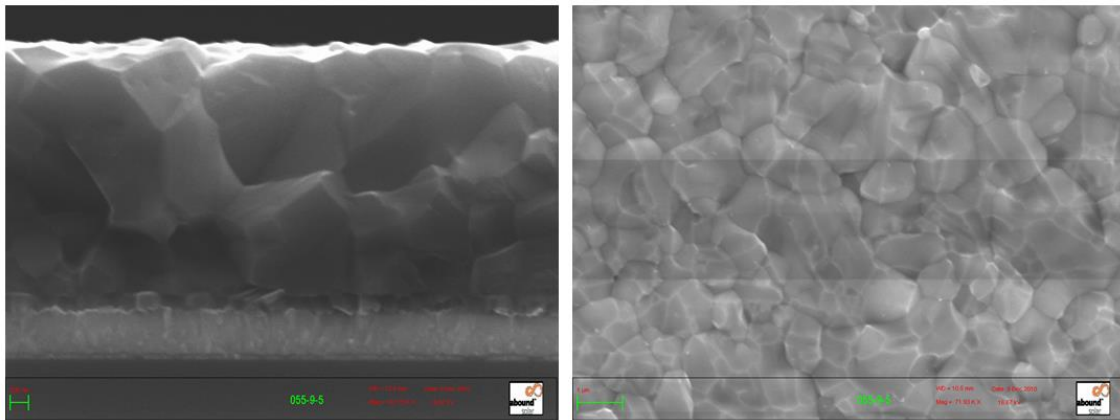


Figure 4-47: SEM cross-section (Left) and planar (Right) of CdS/CdCl<sub>2</sub>/POR film

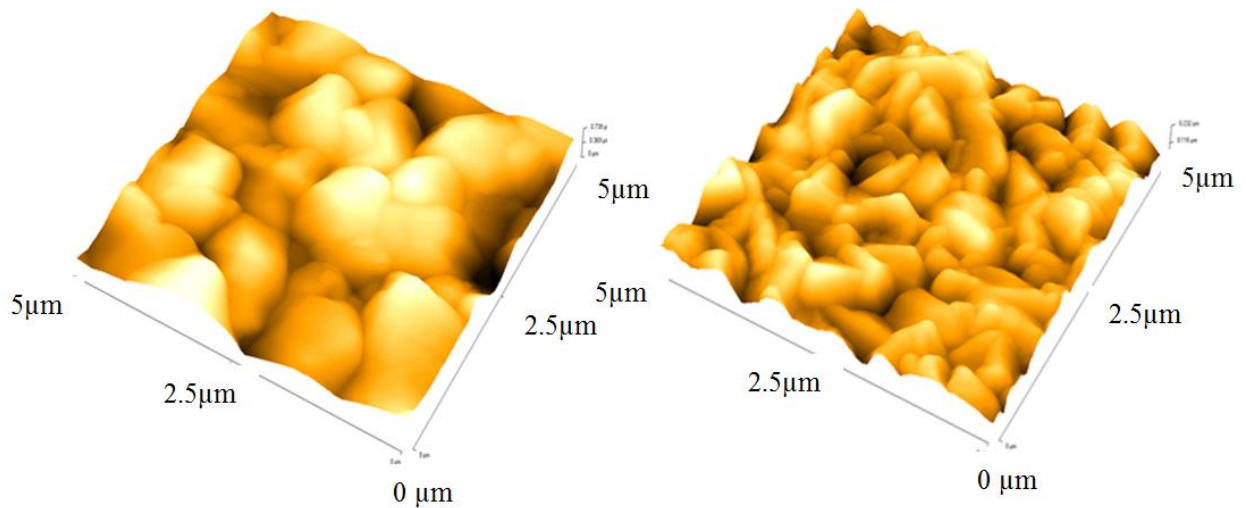


Figure 4-48: 3D AFM rendering of CdS/CdCl<sub>2</sub>/POR (Left) and CdS/CdTe (Right) films

To understand the crystallographic impact of the treatment, XRD of CdS/CdTe and CdS/CdCl<sub>2</sub>/CdTe films, with no additional CdCl<sub>2</sub> treatment was performed and presented in Figure 4-49. The CdTe peaks are labeled with their orientation; other peaks are CdS and TCO diffractions. Normal CdTe films show a (111) preference and distribution typical to CdTe powder. The CdTe films deposited on CdCl<sub>2</sub> treated CdS show a preference towards the (220) orientation.

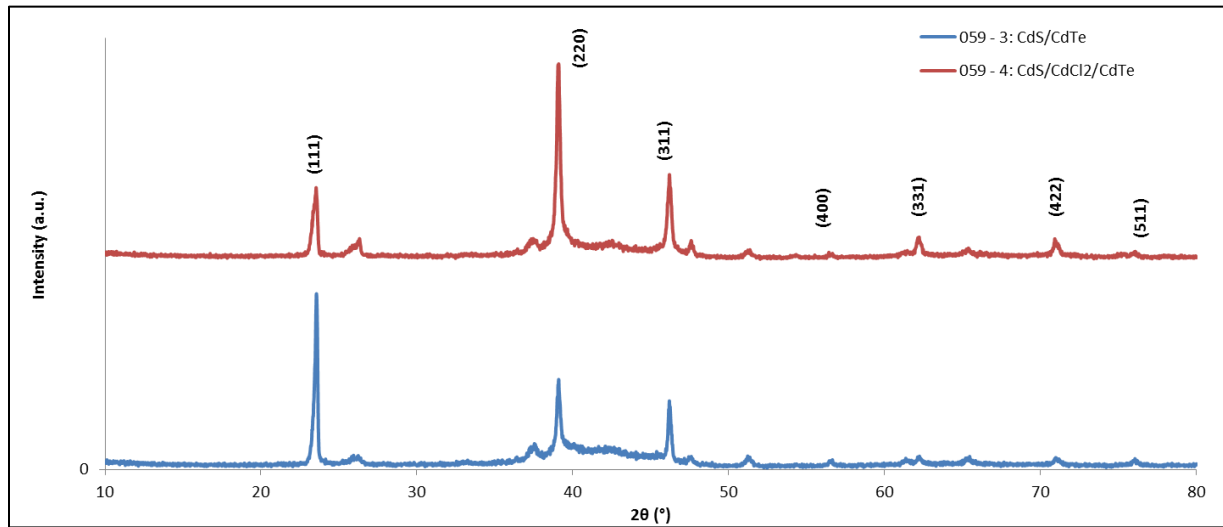


Figure 4-49: XRD of CdS/CdTe (Bottom) and CdS/CdCl<sub>2</sub>/CdTe (Top) films

#### 4.10.2 Precision Glass and Optics substrate with Indium Tin Oxide (ITO) TCO

Glass substrates with a more transparent TCO were obtained from Precision Glass and Optics of Germany. Sample geometries of 1x3" with a thickness of ~1mm were provided. The unique sample format required the use of a quartz carrier for sample transport as demonstrated in Figure 4-50. The low thermal mass of the sample required a significantly different deposition profile. The objective was to produce devices demonstrating increased J<sub>sc</sub>, as a result of increased substrate transmission (Figure 4-51) and thinning of the CdS window layer due to smoother TCO. Several sample sets were tested to develop the process, J-V and QE results of the best PGO ITO device produced during this study are presented in Figure 4-52 and Figure 4-53. Achieving results on the PGO ITO was a significant challenge. The ITO is exceptionally smooth, reducing mechanical adhesion of films and narrowing CdCl<sub>2</sub> process space. Initial results suffered from film delamination, as a result of excessive CdCl<sub>2</sub>. A limited sample set was available, narrowing the search of potential process space. Once adhesion issues were resolved, 23.7mA/cm<sup>2</sup> was achieved, representing ~3mA/cm<sup>2</sup> improvement over TEC10 devices. Device parameter extracted from J-V are presented in Table 4-7.



Figure 4-50: PGO ITO sample in quartz carrier post deposition

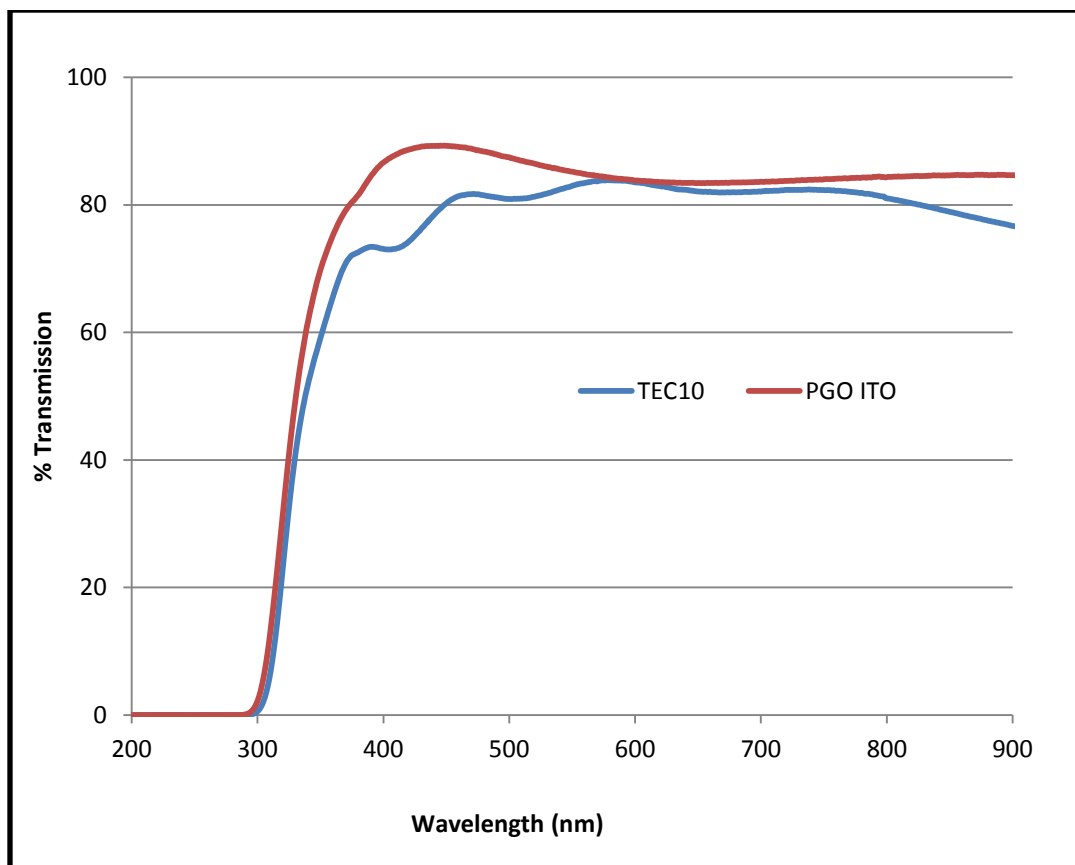


Figure 4-51: Transmission curves comparing TEC10 and PGO ITO

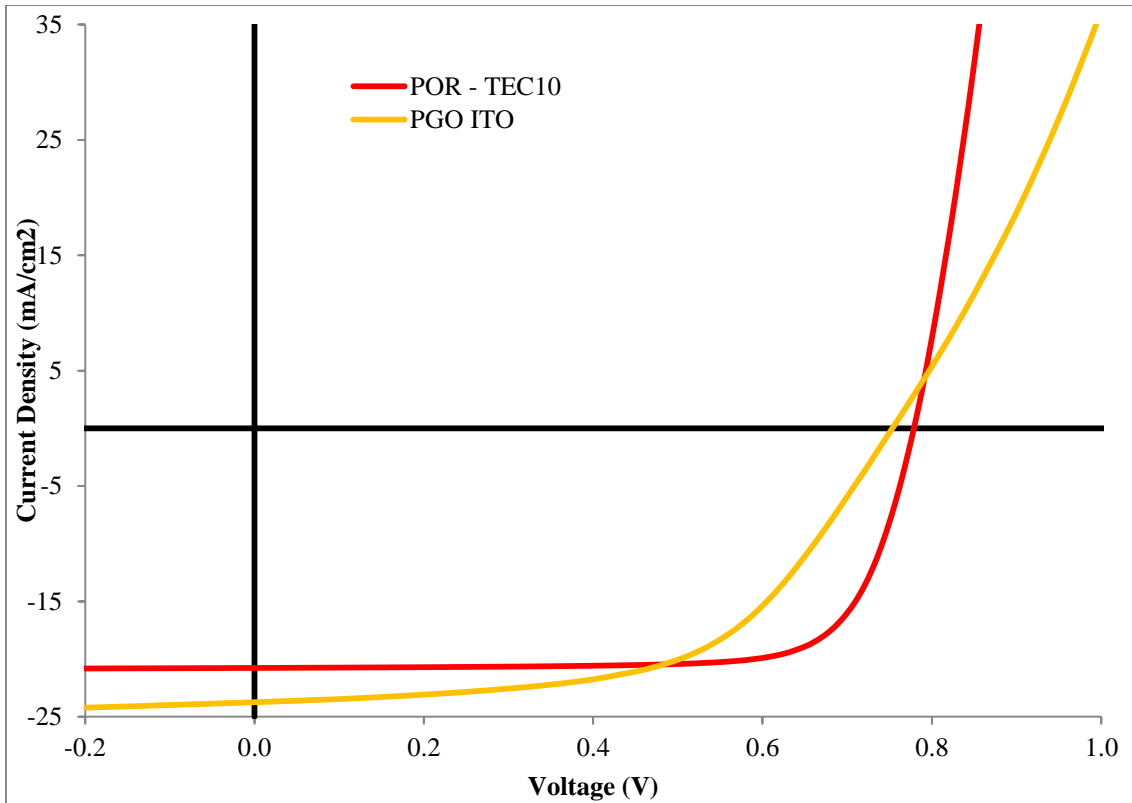


Figure 4-52: J-V of baseline TEC10 compared to PGO ITO

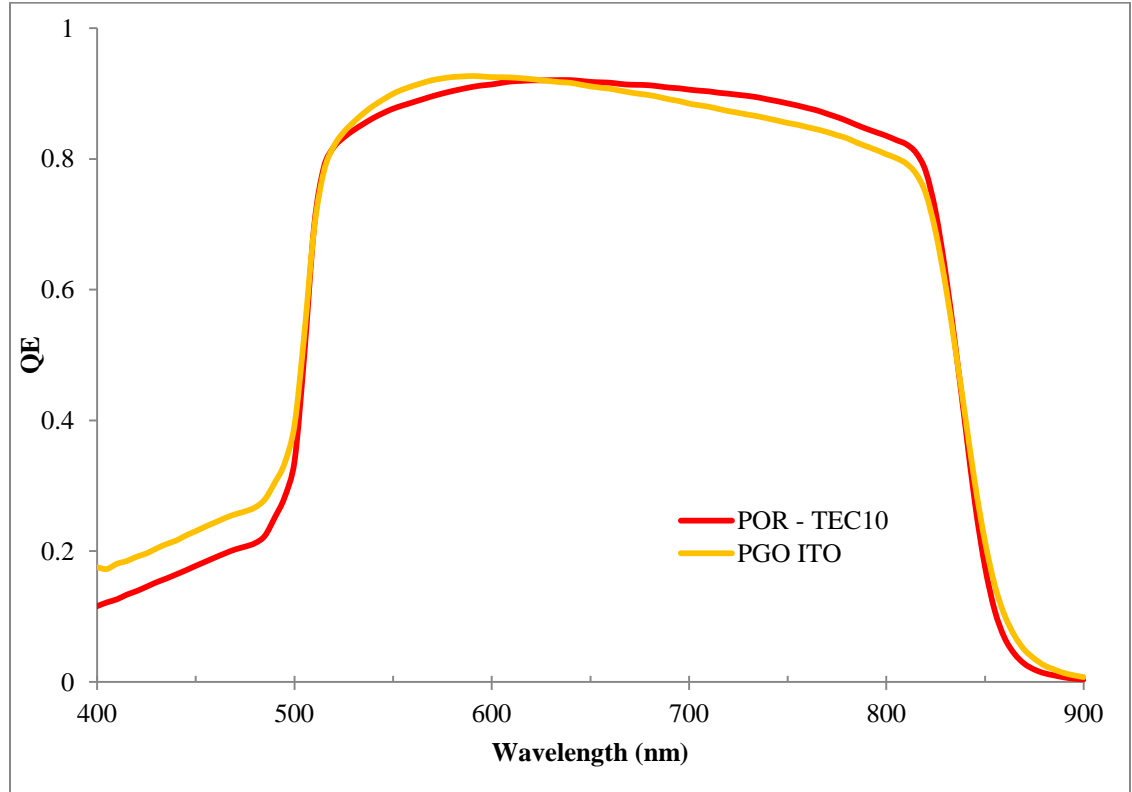


Figure 4-53: QE of baseline TEC10 compared to PGO ITO

Table 4-7: JV results demonstrating Jsc improvement with PGO ITO

Sample ID	VOC (mV)	JSC (mA/cm <sup>2</sup> )	Fill Factor (%)	Efficiency (%)	RS (Ω)	RSh (Ω)
POR - TEC10	778.7	20.8	76.0	12.3	0.5	4679.8
PGO ITO	753.3	23.7	56.7	10.1	4.6	444.0

The resulting microstructure of CdS and CdS/CdTe films deposited by the ARDS on PGO ITO is presented in Figure 4-54. The morphology was better than TEC10, potentially as a combined result of hotter substrate temperature and smoother TCO increasing surface mobility. A sample to test the effect of the intermediate CdCl<sub>2</sub> treatment was generated. A marked improvement in the morphology resulted as observed in Figure 4-47.

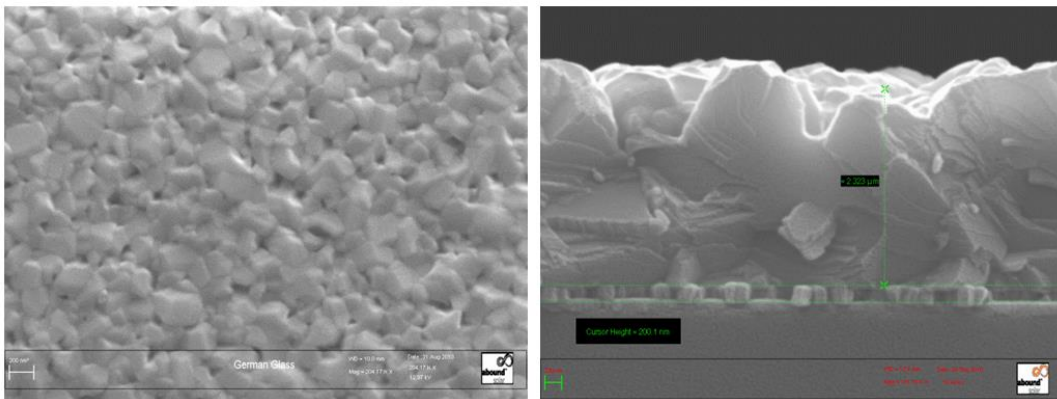


Figure 4-54: SEM micrograph of planar CdS and cross section CdS/CdTe on PGO ITO substrate

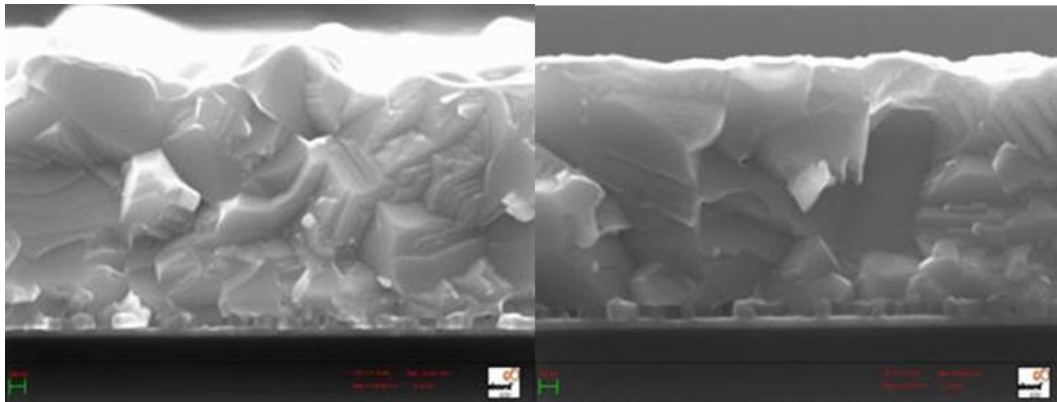


Figure 4-55: SEM cross-section of CdS/CdTe (left) and CdS/CdCl<sub>2</sub>/CdTe (right) on PGO ITO

#### 4.10.3 EL, PL, DLIT Studies

Multiple runs were committed to generating partial and full devices for characterizing various intentional macro defects with EL, PL, and Dark Lock in Thermography (DLIT), which were published by Zaunbrecher [67]. EL and PL images (Figure 4-56) revealed wash process deficiencies, and film defects due to TCO/CdS damage. The interface quality and uniformity, as well as defect states due to impurities and doping are exposed with this



technique. Shunt defects at the perimeter of finished devices are illuminated with DLIT in Figure 4-57, as well as uniformity issues with the activation process. Samples were generated to explore signatures of intentionally created defects at all stages of the process, representing defects occasionally incurred during device fabrication

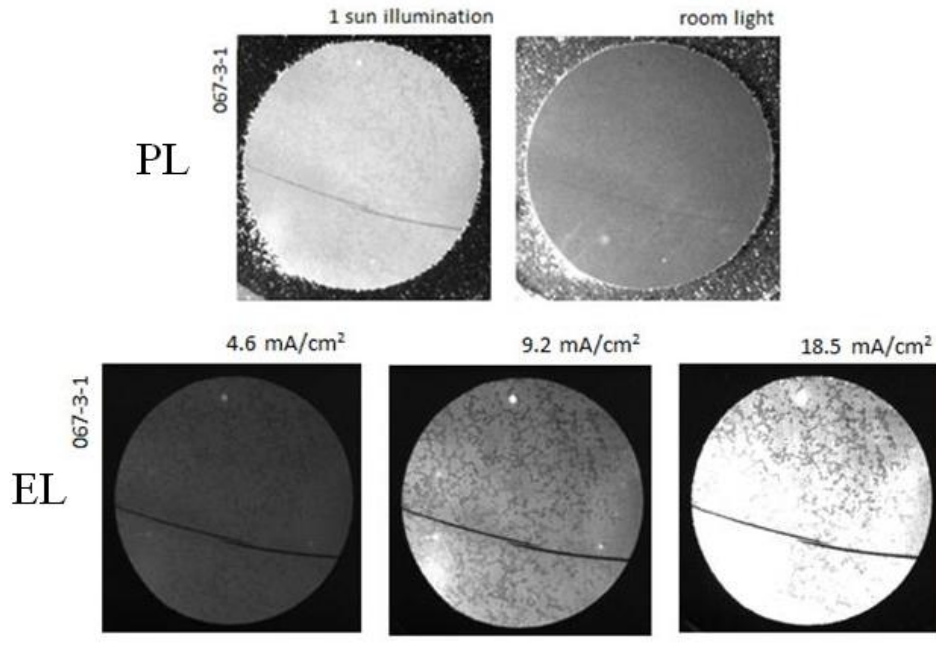


Figure 4-56: PL (top) and EL (bottom) images of fully treated un-filmished film, images courtesy of Katherine Zaunbrecher [65].

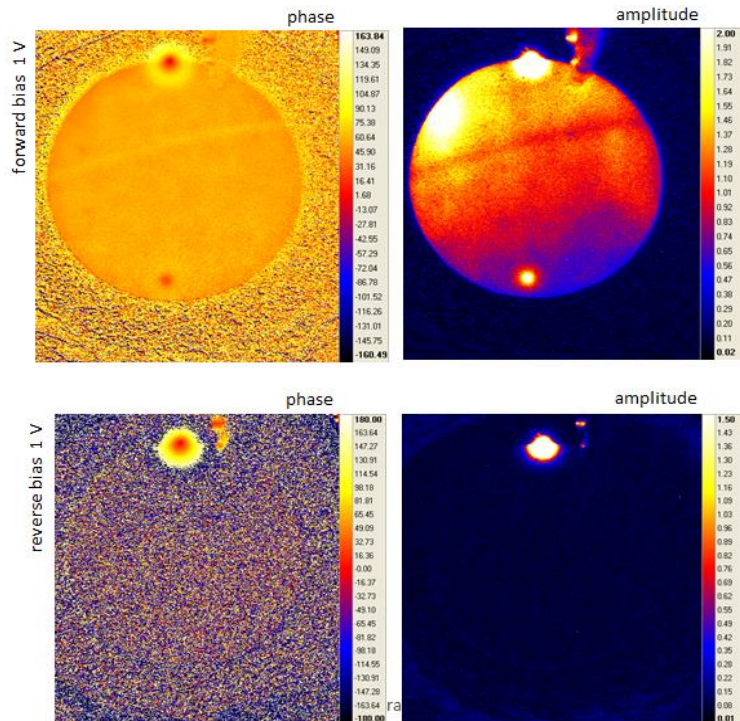


Figure 4-57: DLIT of finished device from Figure 4-56, images courtesy of Katherine Zaunbrecher [65].

## CHAPTER 5: CONCLUSIONS

### 5.1 Progress

The final assembly, startup, characterization and process development of the ARDS has been completed. Several modifications to the hardware needed to obtain reliable performance of the ARDS were completed in this study. These include (I)thermal shielding of sources (II)vapor shielding between the sources for chemical isolation (III)modification to the substrate top heaters for improved process control (IV)installation of pyrometer for monitoring substrate temperatures. The novel method of embedded Nichrome heaters have proven to be robust, and enabled the development of a co-sublimation source, the co-sublimation process has enabled the deposition of ternary alloys like  $Cd_{1-x}Mg_xTe$  at high throughput. Incorporation of this heating method into the source shutter has increased potential run length to more than 75 full samples between replenishing the source charge.

The effect of the process conditions on the properties of the films for each process has been quantified. A standard operating procedure (SOP) has been developed to produce ~12% efficient devices. As a result of this research, devices efficiencies of  $12\% \pm .5\%$  are repeatedly produced. Incorporation of 2.5% oxygen in to the CdS:O window layer resulted a device with  $J_{sc}$  of  $25\text{mA}/\text{cm}^2$  and 16.2% efficiency. A total of 110 runs were completed during this research, producing ~1050 samples. To date more than 565 runs have been completed, due to the efforts of this research and successful operation of the ARDS. The ARDS has been found to be highly effective to study the effect of process conditions on device performance. The capabilities of the ARDS are significant for new process development in CdTe PV and present many future opportunities.

Since the completion of this research effort, more than 565 runs have been completed, producing 10,000+ unique samples supporting diverse research objectives. The ARDS continue to operate with a high level of research efficiency, and repeatability. A recent demonstration of ARDS capability on TEC12D glass produced 9 devices from a single sample with a 12.9% mean efficiency and a standard deviation of 0.2. The complete J-V parameters and curves are presented in Table 5-1 and Figure 5-1 respectively.

Table 5-1: J-V parameters for 9 devices of a sample

Device Number	Voc	Fill Factor	Jsc	Efficiency	Cell Area
	[mV]	[%]	[mA/cm <sup>2</sup> ]	[%]	[cm <sup>2</sup> ]
1	812	74.3	21.3	12.86	0.696
2	811	74.7	21.8	13.18	0.697
3	807	73	21.2	12.49	0.71
4	810	74.3	21.4	12.9	0.683
5	803	74.5	21.6	12.9	0.688
6	806	74.9	21.1	12.71	0.708
7	811	73.6	21.5	12.83	0.687
8	808	75.1	21.5	13.07	0.687
9	807	74.2	21.3	12.76	0.699
<b>Mean</b>	<b>808.3</b>	<b>74.3</b>	<b>21.4</b>	<b>12.9</b>	<b>0.695</b>
<b>Std. Dev</b>	<b>2.9</b>	<b>0.7</b>	<b>0.2</b>	<b>0.2</b>	<b>0.009592</b>
<b>SD (%)</b>	<b>0.4</b>	<b>0.9</b>	<b>1.0</b>	<b>1.6</b>	<b>1.4</b>

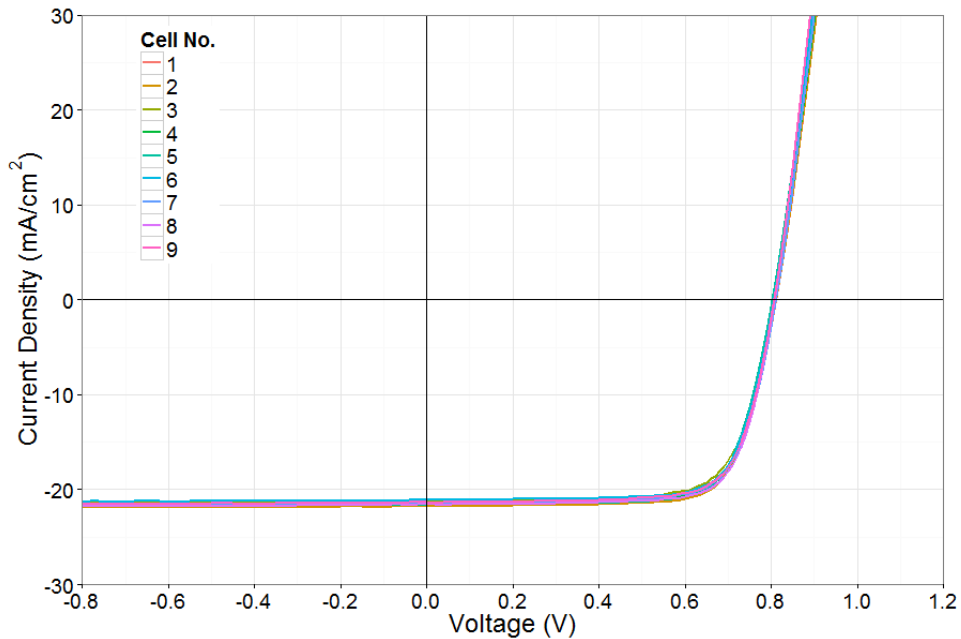


Figure 5-1: J-V curves for 9 devices of a sample, sample and results generated by Jason Kephart

The ARDS has been instrumental in the demonstration of CMT ER, resulting Voc and TRPL improvements. Efforts to improve window layers employ the flexibility of the ARDS to produce completed devices utilizing CdS:O, indium tin oxide (ITO) and high resistivity transparent (HRT) TCO buffer layers. A collaborative effort with Loughborough University, UK relies heavily on the ARDS to support 3 major projects advancing CdTe PV. (1)The investigation of atomic level features associated with the ARDS manufacturing process utilizing high resolution Transmission Electron Microscopy (HR-TEM). (2)The development of advanced antireflection wide band gap coatings to increase the current from cells (3)The development of a unique interconnection method for fabricating modules. Samples are generated in the ARDS by both MEL and Loughborough members, and characterized at the Loughborough Materials Characterization Centre.

## 5.2 Challenges addressed

Many challenges were addressed during the development of the ARDS POR. Developing methods and methodologies to address operational and process control were a significant portion of the research performed. Achieving proper sample preparation and end effector cleaning eliminated front end variation. Developing solutions to mechanical deficiencies and optimizing those which could not be altered, resulted in a robust research system. Process development is a perpetual process, and will evolve as new discoveries and research interests' advance. The progress made during this research provided a strong platform for further improvements, and much is still to be learned from the samples generated as a result.

## 5.3 Perspective

The opportunity to bring the ARDS online was a unique challenge, testing mechanical, thermal, and vacuum deposition competencies. The process development required extensive material and device characterization, expanding my knowledge of key techniques and the interpretation thereof. Successful device characterization is accomplished only after developing a strong understanding of advanced physics principles, and acceptance of the unique characteristics of CdTe PV.

## 5.4 Future Work

Currently the ARDS is configured only with HPD sources for thin film deposition. Future research of more advanced devices shown in Figure 1-13 will require alternative hardware such as sputtering, MOCVD, and PVD, as well as longer cluster tools. The ARDS is well suited for the continued development of alternative substrate/TCO combinations, window layer optimization, PECSS, and CMT.

The ARDS currently does not support in-situ characterization. The incorporation of basic optical methods such as ellipsometry would benefit the investigation of film properties while under continuous vacuum.

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## APPENDIX

### A1 Additional Characterization Techniques

#### A1.1 Capacitance-Voltage

Capacitance measurements provide information about the depletion region, in response to an applied direct current (DC) voltage bias. Parameters such as semiconductor depletion width, doping concentration and doping profile are extracted. Test methods and apparatus are well defined by Davies [29] and Nagle [68].

#### A1.2 Quantum Efficiency (QE)

Quantum efficiency provides a spectral response of the device to monochromatic illumination. This measurement allows identification of specific photocurrent losses. Test methods and apparatus are well defined by Davies [29] and Nagle [68].

#### A1.3 Ultra Violet-visible spectroscopy (UV-Vis)

UV-Vis is a method used to characterize material absorption, reflection and transmission as a function of wavelength. A broad spectrum light source is collimated and passed through a monochromator, separating the light into different wavelengths. An aperture is used to select the incident wavelength, and is passed through the sample and measured by a photodetector. For CdTe solar cells, Transmission versus wavelength for the 300-1000nm spectrum is recorded and provides useful information about the band gap of a film.

#### A1.4 Atomic Force Microscopy (AFM)

The AFM uses a high precision probe to map the surface of a material. AFM can be performed in several operating modes including static (contact) and dynamic (non-contact and tapping). Depending on the material and properties of interest, each of these techniques has advantages. The probe tip is typically silicon with a radius of a few nanometers, and can be coated to improve specific characteristics. The deflection of the probe is measured by a laser optic system, reflecting from the top of the cantilever beam. In static modes, the tip is “dragged” across the surface of the sample generating contours. In the Dynamic modes, the probe is held a fixed distance or oscillated to maintain a minimum distance. The van der Waals forces work to influence the position of the tip, producing a measured deflection. This deflection is mapped to produce topography of the surface. Both static and dynamic modes were used to characterize films at all phases of fabrication for CdTe solar devices.

#### A1.5 Profilometry

A profilometer operates on similar principles of the AFM. A precision probe is used to follow the surface of interest, typically only in a linear path, while the deflection of the probe is recorded through a laser optic system. The profilometer is used to determine feature depth, often formed through subtractive methods such as etching to generate a step.

#### A1.6 Scanning Electron Microscope

The Scanning Electron Microscope (SEM) achieves high magnification imaging of materials with the use of electrons. A highly focused column of electrons is directed at the point of interest, causing secondary electrons and x-rays to be emitted. The secondary electrons are detected, producing a high resolution image. Critical operating parameters are sensitive to material and sample preparation, and are often device specific. SEM enables investigation of planar and cross-sectional features of thin films.

#### A1.7 X-ray Photoelectron Spectroscopy (XPS)

XPS is a surface sensitive quantitative spectroscopic technique used for the elemental analysis of materials. High energy x-ray irradiation produces photo-emitted electrons having characteristic kinetic energy related to the binding energy of the atoms. Electron count vs. binding energy (eV) of the study sample is compared to characteristic sets of XPS spectrum for elements from an extensive library.

#### A1.8 X-ray Diffraction (XRD)

XRD is performed by irradiating a target with high energy x-rays, while precisely rotating the sample. A diffraction pattern is produced from the collection of reflected x-rays, producing information about the atomic and molecular structure of the material.

#### A1.9 X-ray Fluorescence (XRF)

XRF provides elemental and chemical analysis of materials. A high energy x-ray source bombards the material of interest, causing the emission of characteristic “secondary” x-rays.

#### A1.10 Photoluminescence (PL)

PL is the emission of photons resulting from the relaxation of excited carriers that had been previously promoted to the higher energy state by illumination. Various excitation wavelengths can be utilized to activate specific defects. Samples in this study were characterized by Katherine Zaunbrecher at NREL using a 1mW 532nm

laser having a spot size of ~1mm, and a sample temperature of 9K. The intensity and spectral content of the PL signature provides information about the bandgap, impurity level and defects, and carrier lifetime

#### A1.11 Electroluminescence (EL)

EL is utilized to spatially resolve the uniformity of solar junctions over a large area by the inverse of the photovoltaic effect. The film or device is operated in a forward bias condition, producing a photoemission as a result of radiative recombination of electrically excited carriers. The photons are collected by a high sensitivity CCD camera. The EL signal can be correlated to specific device parameters, and allows identification of spatial defects [69].

#### A1.12 Time-Resolved Photoluminescence (TRPL)

TRPL is used to characterize minority carrier lifetime and recombination rates in CdTe layer of solar cells, and is dependent on defect states and film quality.. Analysis of samples in this study was performed at NREL by Katherine Zaunbrecher. Optical injection of excess carries is performed with a 630nm, short pulse (~200fs) laser. A data acquisition system records the distribution of photon emission as a function of time. From the decay curves, the lifetime of carriers as an average, in the bulk or in the junction region can be extracted.