THESIS

LOW-POWER SWITCHED-CAPCITOR AMPLIFIER AND SIGMA-DELTA MODULATOR DESIGN FOR INTEGRATED BIOSENSOR APPLICATIONS

Submitted by

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ABSTRACT

LOW-POWER SWITCHED-CAPCITOR AMPLIFIER AND SIGMA-DELTA MODULATOR DESIGN FOR INTEGRATED BIOSENSOR APPLICATIONS

Neurotransmitters are chemicals present in living tissue which regulate biological functions. Some neurotransmitters which are present in the brain, such as nitric oxide (NO), are believed to play a role in the process of cellular migration during development. Today there is no practical way to measure gradients of neurotransmitters across pieces of tissue in both the spatial and temporal domains. Single electrode systems can be used to determine neurotransmitter concentrations at specific locations, but do not provide spatial resolution. Dyes and marking compounds can be used to locate concentrations of neurotransmitters across a piece of tissue, but kill the tissue in the process, thus limiting temporal resolution.

Integrated silicon biosensor arrays have been proposed as a method for detecting neurotransmitters in both the spatial and temporal domains. Using large arrays of microelectrodes placed at pitches comparable to the size of individual cells, a high resolution chemical image of neurotransmitters could be captured in real time. For such an array, a large number of electronic components are necessary. Two such components are high precision amplifiers and analog-to-digital converters which are necessary to amplify the extremely small chemical signals and then convert them to digital values such that they can be stored and analyzed. These components must be low power to avoid generating heat, and small in size in order to limit total silicon area.

This thesis proposes the design of a low power switched-capacitor amplifier and Sigma-Delta modulator for use as an analog-to-digital converter. The switched-capacitor amplifier

achieves a gain of 40dB with -63.7dB total harmonic distortion while using 6.82µW and occupying 0.076mm^2 silicon area. The Sigma-Delta modulator achieves a signal-to-noise ratio of 86.8dB over 2kHz signal bandwidth and uses 9.1µW while occupying 0.043mm^2 silicon area. Both of these designs were implemented in a 0.18µm CMOS process with a supply voltage of 900mV and their functionality verified was in silicon.

ACKNOWLEDGMENTS

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Chapter 1: Introduction

1.1 Advancements in Medical Science

Progress in the fields of biology and medical research are advancing at an incredible pace. Every day our understanding of biology increases and new drugs and treatments for diseases are introduced. However, as we learn more about how living organisms work and what causes diseases, it becomes more and more time consuming and costly to develop treatments. Treatments can no longer be developed by simple trial and error. Rather, the specific reactions to treatments need to be observed and quantified.

The study of neurotransmitters within tissue is an area of particular interest in biological research today. While neurotransmitters are important for many reasons, their role in cell movement and migration is especially interesting. This is true in the case of the migration of cells within the brain as it develops. As the brain grows, cells are formed in the center of the brain and must migrate to their final locations where they are needed. If the cells do not migrate to the correct position then the brain will not function as it should. This biological process evokes a number of important questions: What causes cells to move in a particular direction? How do the cells know what distance to travel? If the cells migrated to the wrong position, what caused it? The answers to these questions are important to understanding the development and function of the brain, but the answers are not definitely known. If the answers to these questions can be found then it may be possible to create treatments which facilitate proper brain growth and will reduce the possibility of neurological disorders.

Prevailing theories suggest that gradients of neurotransmitters within the tissue determine which way cells will move. However, while cellular movement itself can be easily observed through microscope, neurotransmitters are not so easy to see. Luckily many neurotransmitters, such as nitric oxide (NO) and dopamine, are electrochemically active. Chemicals which are electrochemically active oxidize or reduce when electrodes are used to apply a voltage across a solution which contains them. When the chemical oxidizes or reduces an electric current is created between the two electrodes proportional to the concentration of the chemical. If this current can be accurately measured then the amount of the neurotransmitter that is present at the electrode site can be determined.

1.2 Motivation

The overall goal of this project is to obtain the ability to visualize the molecules of cellular communication. This will allow us to understand both simple and complex biology that drives normal and pathophysiological processes as the communication signals often provide stimuli for cell functions such as birth, movement, and death. This is the top level goal. In order to make further progress in the study of cellular migration, a definitive correlation needs to be established between neurotransmitter concentrations and cell movement. Determining this correlation requires measurement of neurotransmitters in both the spatial and temporal domains. With current technology such a measurement is not possible. Using dyes and marking compounds, spatial concentrations of neurotransmitters in tissue can be determined, but these chemicals kill living tissue and prevent any temporal measurement. Similarly, dedicated electrochemical sensors can measure neurotransmitter levels over time, but their size prevents measuring a large number of points simultaneously. The research proposed here attempts to solve this problem by enabling the development of a biosensor array. Such an array will include

thousands of electrochemical sensors which can detect neurotransmitters in both the spatial and temporal domains when live tissue is placed directly in contact with the biosensor. VLSI technology is the best and perhaps only solution to this problem, as it allows for a large number of sensors and devices to be implemented on a scale comparable to that of individual cells (20-30µm spacing). A diagram of the proposed biosensor system is shown in Figure 1-1 below. Tissue sits on top of the biosensor while a microscope monitors the cell movement from above.

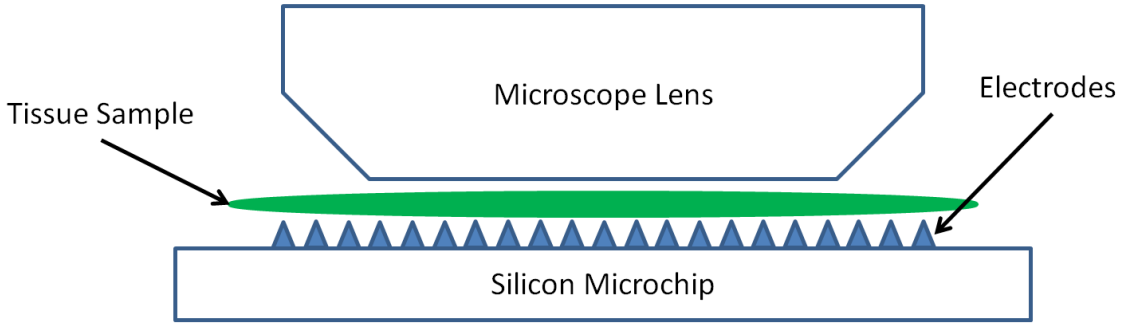

Figure 1-1: Proposed biosensor system

1.3 Objectives

Designing an integrated biosensor array is an enormous challenge that requires many different types of circuits. A block diagram of the biosensor signal chain is shown in Figure 1-2.

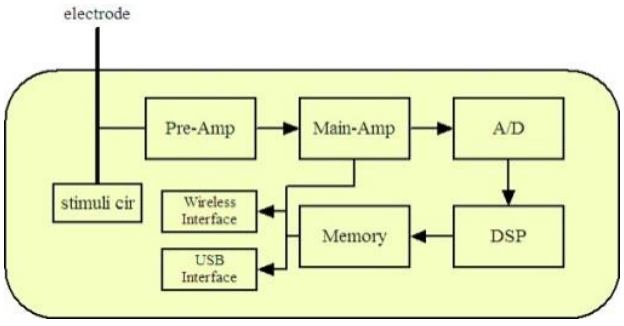

Figure 1-2: Biosensor signal chain

Electrodes, such as those proposed in [1], are placed directly on the surface of the silicon microchip, and a circuit called a potentiostat is used to induce a current through the electrodes. A suitable potentiostat is proposed in [2]. A pre-amplifier, known also as a transimpedance amplifier, is used to convert the input current into a voltage which is then amplified by the main-amplifier. Next, the output voltage of the main-amplifier is converted to a digital value with an analog-to-digital converter (ADC). After the signal is converted to a digital value, the data passes through a digital signal processor (DSP), is stored in memory, and then transferred to a computer for analysis and storage. While it is certainly possible and desirable to multiplex several electrodes to a single signal chain, in a biosensor with thousands of electrodes there will still need to be many copies of the signal chain in order to achieve a reasonable sample time of the array. The objectives of this research are to implement an effective main-amplifier and analog-to-digital converter for use in such a system.

In the biosensor system power consumption is the number one concern which much be addressed. Power consumption generates heat which must be dissipated by the system, and since the biosensor directly interfaces with tissue this becomes a more serious problem. If the microchip becomes too warm it can kill the tissue or change its behavior such that the collected data is no longer valid. For these reasons the power consumption of the main-amplifier and the analog-to-digital converter should be minimized as much as possible, preferably to only a few μW each.

Circuit area is also a large concern in the biosensor system. Since the microchips will be interfacing directly with tissue they must be inexpensive and disposable. The price for a microchip is directly related to its size, and thus a small chip will be less expensive and more

useful for research. As such, circuit area for the main-amplifier and analog-to-digital converter need to be minimized.

Previous biosensors have attempted to measure biological signals with integrated electrodes, however none have attempted the same electrochemical current measurement proposed here, and none have tried to implement so much circuitry on a single microchip. This research attempts to expand on previous biosensor work and solve problems left unattended by previous work.

This thesis is organized as follows. In Chapter 2 background information about electrochemistry and previous work on integrated biosensors will be reviewed. Chapter 3 and 4 will provide detailed information about the design and simulation results of the proposed main-amplifier and Sigma-Delta modulator respectively. Chapter 5 presents silicon test results for the circuits proposed in Chapters 3 and 4, and finally Chapter 6 will provide conclusions and recommendations for future work.

The work proposed here includes a 3-stage, switched-capacitor main amplifier, and a 2^{nd} order, switched-capacitor, Sigma-Delta modulator for use as the analog-to-digital converter. The main amplifier uses 6.82µW and occupies $0.076mm^2$ silicon area, while the Sigma-Delta modulator uses 9.1µW and occupies $0.043mm^2$ silicon area. These figures represent a substantial improvement over previous implementations and both simulations and silicon testing show that these circuits are well suited for use in an integrated biosensor system.

Chapter 2: Background and Previous Research

2.1 Introduction

This chapter introduces the concept of an integrated biosensor system and how electrochemistry can be used to detect chemicals in solution. Section 2.2 explains the details of electrochemical reactions and the electrode system that can be used for measurement. Section 2.3 highlights existing work on integrated biosensors and their applications. Finally, sections 2.4 and 2.5 will discuss previous research in switched-capacitor amplifiers and Sigma-Delta modulators. Section 2.6 will provide a summary of the chapter.

2.2 Electrochemical Reactions and Electrode Systems

Figure 2-1 depicts a potentiostat and basic 3-electrode system for detecting electrochemically active substances. This structure is the basis for detecting neurotransmitters in the silicon biosensor. When the electrodes are placed in solution, a connection is formed between the counter electrode (CE) and reference electrode (RE) which places the op-amp in a unity gain configuration. In this configuration, whatever voltage is applied as V_{ref} will also appear at the counter and reference electrodes. Since the working electrode (WE) is held at a constant potential by a current sensing circuit, changing V_{ref} will change the voltage potential applied across the solution. Electrochemically active substances within the solution will begin to oxide or reduce if the proper potential is applied across the solution. This reaction will cause a current to

flow out of the working electrode which can be detected and measured. The magnitude of the measured current is proportional to the concentration of the current. The design of the electrodes plays a large role in the performance of the overall circuit, and optimized electrode geometry is proposed in [1]. The design of the potentiostat also plays a large role in the accuracy of the system, and a high performance version is proposed in [2].

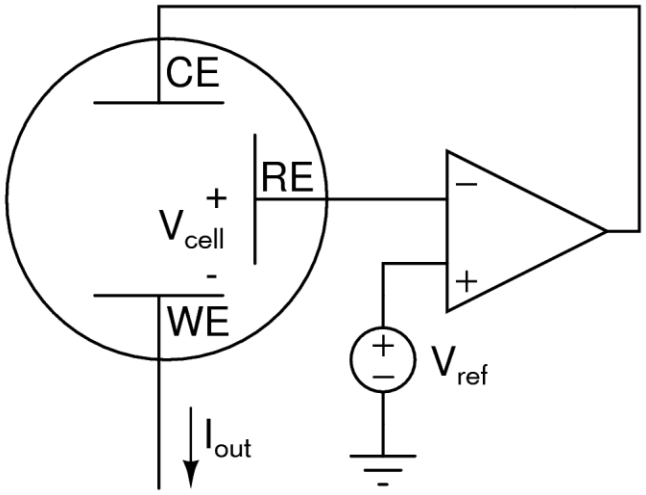

Figure 2-1: Potentiostat and 3-electrode system

2.3 Previous Research in Integrated Biosensors

A variety of previous research on the topic of integrated biosensors has been performed. While none of these projects have attempted to measure neurotransmitters in the same manner that is being proposed here, it is important to examine the prior work and determine how their results can help improve this research.

2.3.1 Electrical imaging of neuronal activity by multi-transistor-array (MTA) recording at 7.8μm resolution [3]

An interesting biosensor design can be found in [3]. This design features a 128x128 array of transistor based sensors. Much like the proposed design, this research places live tissue, in this

case cultured neurons, directly onto the chip. A schematic of the signal chain used in this design is found below in Figure 2-2. Small voltages from the neurons modify the gate voltage of the sensor transistor, which in turn modifies the drain current and voltage of the transistor. This voltage change is buffered through an op-amp and then sent out to 16 multiplexed analog-to-digital converters on chip.

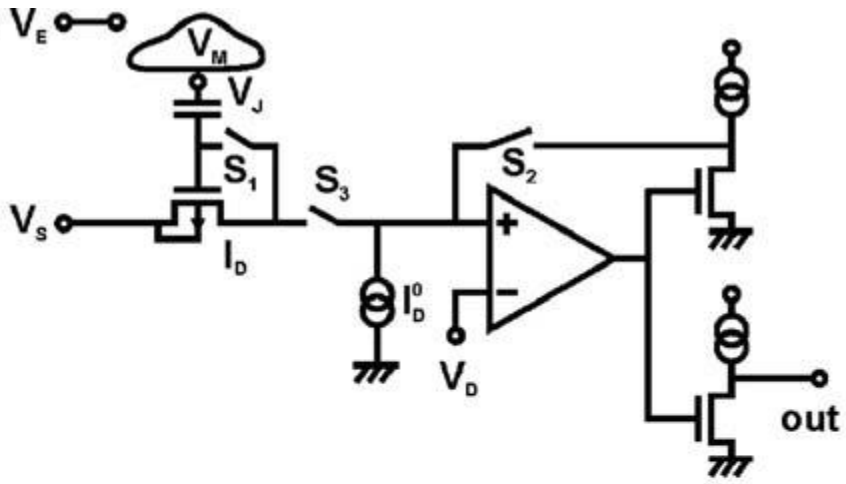

Figure 2-2: Transistor-based sensor chain proposed in [3]

This design utilizes multiplexing so that each individual sensor does not require all of the signal chain circuitry. In the figure above, everything to the left of switch S_3 is represents the individual sensor, while everything to the right of switch S_3 is a row amplifier, meaning there are only 128 total amplifiers. The supply voltage and power consumption of this design are not reported.

The design of this microchip is very similar to the proposed design in that the array of sensors is placed on chip and the pitch of the sensors is comparable to the size of individual cells. However, it is fundamentally simpler in that voltages are being detected rather than small

currents. This means that a transimpedance amplifier is unnecessary and the overall signal chain is easier to implement. A picture of the completed microchip from [3] is shown in the figure below in Figure 2-3. This picture shows the well placed on top of the finished microchip in which the neurons can be cultured.

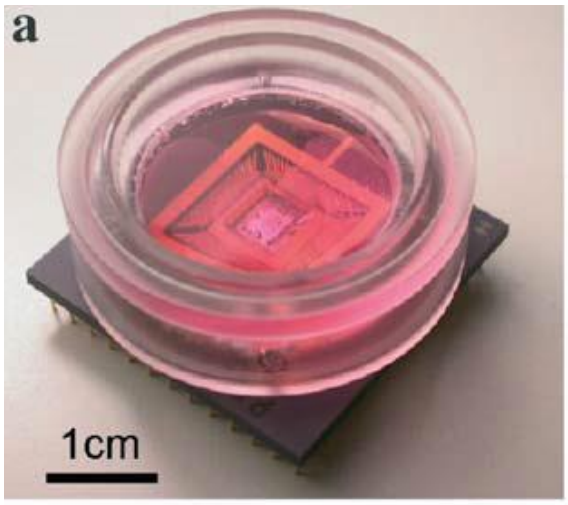

Figure 2-3: Completed microchip with well from [3]

2.3.2 A Fully Electronic DNA Sensor with 128 Positions and In-Pixel A/D Conversion [4]

DNA sensors are another area in which the idea of an integrated biosensor can be applied. Two projects which have implemented an on-chip DNA sensor are [4] and [5]. While these microchips are not attempting to make measurements on live tissue, they do have a fully integrated array of electrodes and complete sensing and analog-to-digital conversion systems.

In [4] an array of 128 sensors in a 16x8 array is implemented. The schematic for this design is shown in Figure 2-4. DNA molecules are bonded to the electrodes and then a

potentiostat is used to set the voltage across the electrodes to induce a current through the DNA molecules.

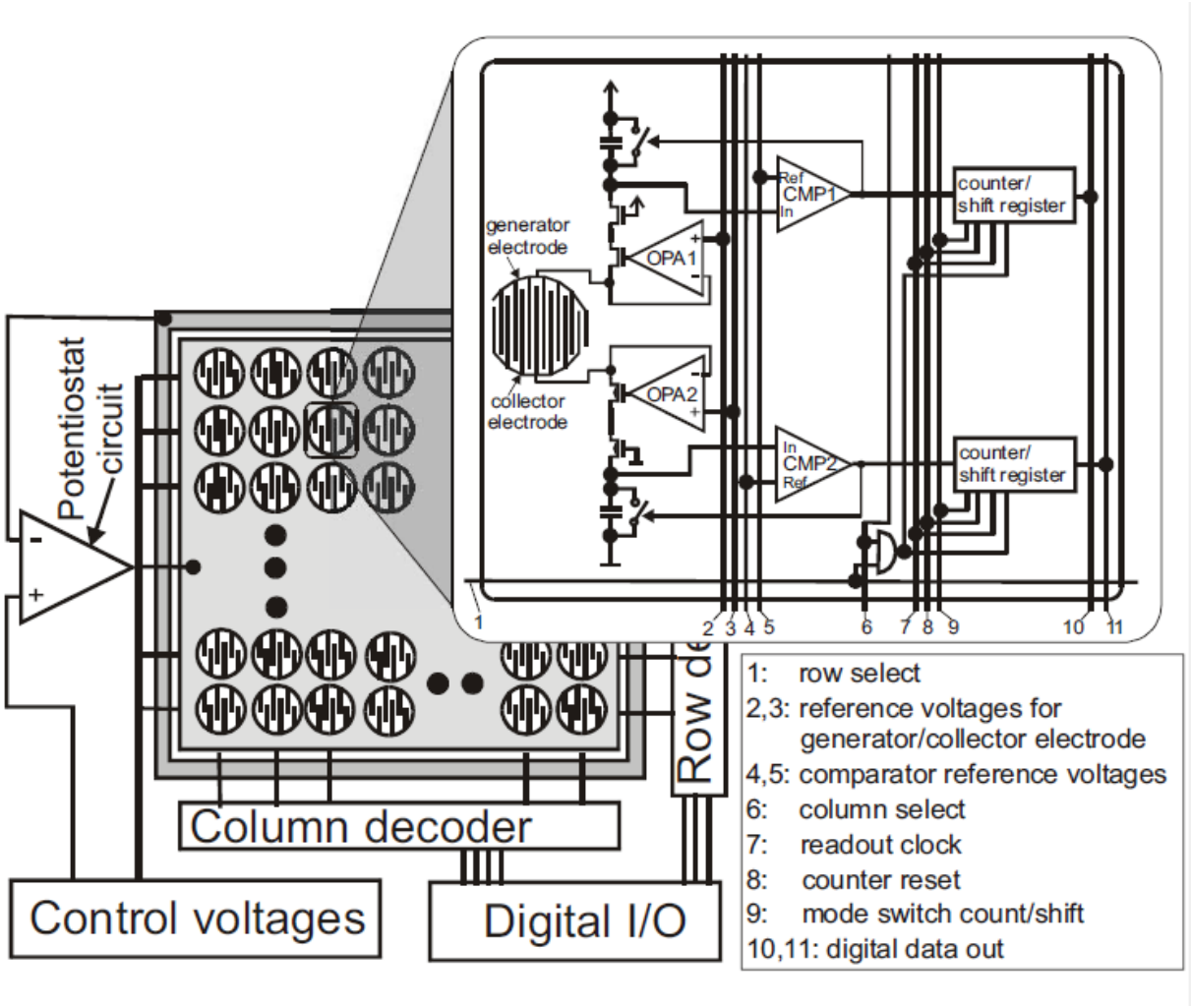

Figure 2-4: Schematic of DNA sensor proposed in [4]

The analog-to-digital converter on this chip uses a simple counter based conversion method. Current from the electrode charges a capacitor, and when the capacitor reaches a certain threshold voltage the counter is incremented and the capacitor is discharged. This cycle is allowed to continue for a predetermined amount of time set by the user and then the final counter value is read out. The number of counts within a specified time period allows you to determine

the magnitude of the current. While this is a very simple to use and implement system, it is not suitable in the case of the proposed biosensor. This is because for very small currents on the order of picoamps, the time that the sensor must be sampled is very long, and thus the time resolution of the chemical image would be very long as well. For the proposed biosensor a time resolution of a few milliseconds is required, and thus a different ADC topology is needed. This microchip is implemented in 0.5µm CMOS with a 5V supply voltage, power consumption is not reported.

2.3.3 CMOS DNA Sensor Array with Integrated A/D Conversion Based on Label-Free Capacitance Measurement [5]

The second DNA sensor proposed in [5] also features a 128 element sensor array in a 16x8 configuration. However, rather than measuring current this design measures the capacitance of the electrodes. Fundamentally the scheme is very similar to that used in [4]. As DNA bonds to the electrodes, it changes the capacitance of the electrode. A constant current source is then used to charge and discharge the electrode capacitor. Every time the capacitor is charged a counter increments and then the capacitor is discharged. Depending on the capacitance change caused by the DNA the charge and discharge rate of the electrode capacitor will change, and thus the number of counts over a specified time period will also change. The principle is illustrated in the Figure 2-5 below. This system is also implemented in 0.5µm CMOS with a 5V power supply.

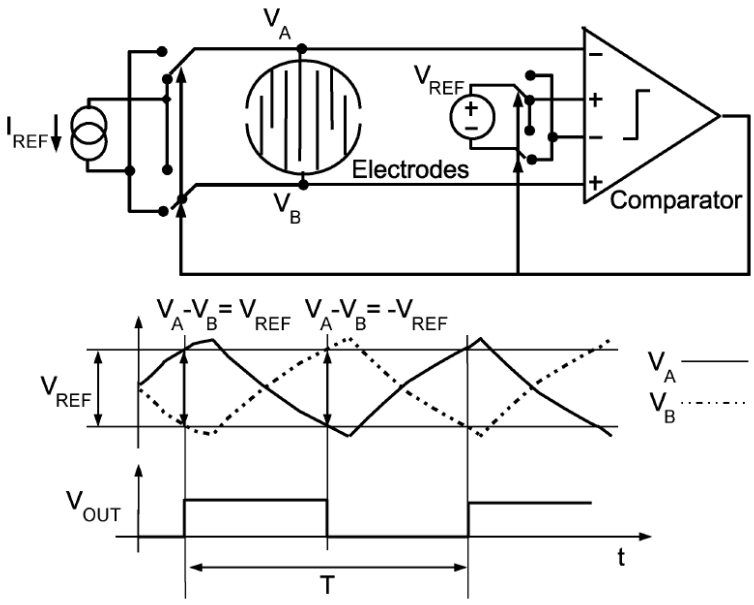

Figure 2-5: Schematic of the DNA sensor proposed in [5]

While total power consumption for the microchip is not reported, since this system of measurement is dependent on rather large capacitors and currents from a 5V supply voltage the power consumption per sensor will be significant. This system also suffers the same drawback as [4] in that a very long sensing time is required. For both of these reasons this architecture is unsuitable for our applications.

2.3.4 Low-Power High-Resolution 32-channel Neural Recording System [6]

[6] proposes a biosensor signal chain which is very similar to what is needed for the proposed design, however electrodes are not integrated into the microchip. Rather this work is simply a 32-channel amplification and analog-to-digital conversion system for recording data from neural sensors. The architecture proposed in [6] is shown in Figure 2-6 below:

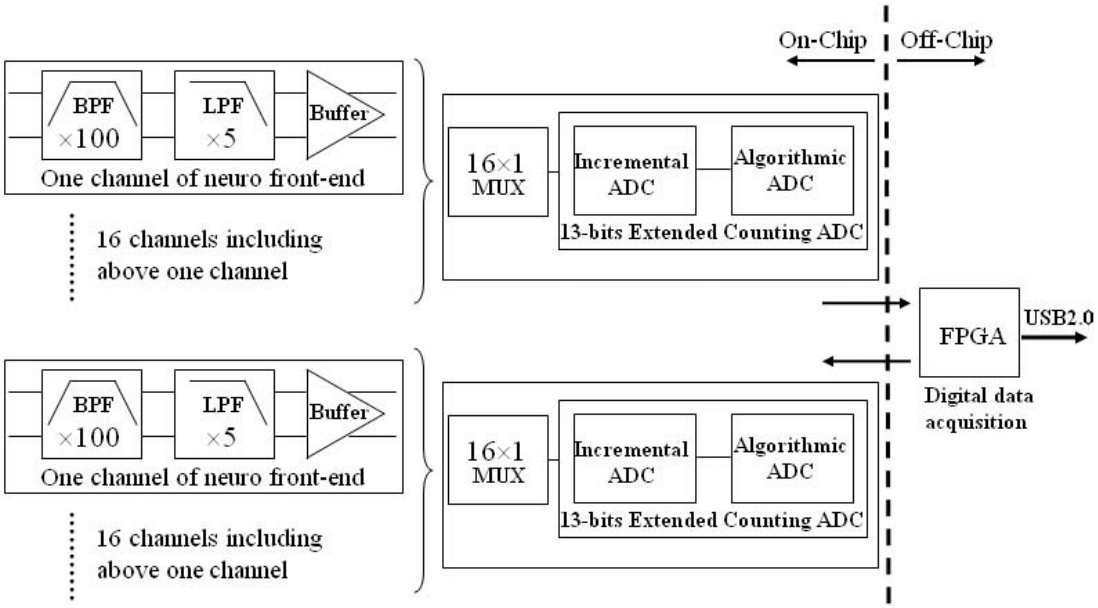

Figure 2-6: Biosensor signal chain proposed in [6]

In this work, the voltage signal from a neural sensor is amplified and buffered by the neuro front-end and then converted to a digital value by a 13-bit extended counting analog-to-digital converter. Signal processing is then handled off chip by a FPGA.

The signal architecture proposed in [6] has several advantages and disadvantages that should be noted. First of all, 32 neuro front-ends are multiplexed into just two analog-to-digital converter stages in order to reduce the power consumption of the device and reduce the silicon area required. However, since only two of the input channels can be sampled at any given time by the ADC blocks the other 30 input channels are wasted. A more efficient implementation of this idea would place the multiplexer in front of the neuro front-end and simply switch between the sensors attached to the input channels.

In the design proposed in [6] the chip uses a 3.3V supply voltage. Each neuro front-end uses 56µW and is able to sense neural input signals with a bandwidth of 100Hz to 7 kHz. However the analog-to-digital converters use 10mW each from a 3.3V supply. While the power

consumption of the neuro front-end is very good, the analog-to-digital converters use far too much power for a large number of them to be implemented on a single microchip. The analog-to-digital converters also occupy 0.56mm^2, which is quite a large amount of silicon area.

2.3.5 Comparison of Previous Integrated Biosensor Devices

Table 2-1 below summarizes the results of the currently reported integrated biosensors. Unfortunately most of these designs do not report power consumption which is a key metric in determining their real usefulness.

Table 2-1: Previous integrated biosensor comparison

Design	Technology	Die Area	Supply Voltage	Power Consumption	Power Consumption per Channel
[3]	Unknown	35.1mm^2	Unknown	Unknown	Unknown
[4]	0.5µm CMOS	28.8mm^2	5V	Unknown	Unknown
[5]	0.5µm CMOS	28.8mm^2	5V	Unknown	Unknown
[6]	0.6µm CMOS	9mm^2	3.3V	22mW	11mV

2.4 Previous Research in Low-Power Switched-Capacitor Amplifiers

In recent years a large amount of research has occurred in the area of switched-capacitor circuits. Switched-capacitor circuits have become extremely popular because of the shift to smaller and smaller integrated circuit process nodes. The performance of amplifiers is usually highly dependent on the ability to match components in the circuit. In a continuous time circuit, resistors must be precisely matched which is very difficult to do in integrated circuits. In a switched-capacitor circuit, capacitors must be well matched which is much easier to accomplish on an IC. Switched-capacitor circuits are also usually consume less power than similar

continuous time circuits making them ideal for this application. Even with the benefits of better matching and power consumption, switched-capacitor amplifiers can become extremely complicated and difficult to design. Switching adds a large amount of non-linearity to the circuit a large amount of the available research focuses on reducing switch non-linearity, especially at low supply voltages. Other approaches focus on running at high speed with high resolution, which presents other unique challenges. This section will present prior research in switched-capacitor amplifiers and how it can be further improved for use in the biosensor system.

2.4.1 A Low-Voltage Sample-and-Hold Circuit in Standard CMOS Technology Operating at 40 Ms/s [7]

The design proposes a switched op-amp technique for operating at low supply voltages where a clock booster would normally be necessary. In low-voltage switched-capacitor circuits, often times the clock voltage is too low to allow signals to pass through MOS transistor switches. In the switched op-amp architecture, a low power op-amp is switched on and off every clock cycle. While the op-amp in turned on it simulated a closes switch, reproducing its input signal at its output. When the op-amp is turned off the input is not reproduced at the output, simulating an open switch. Switched op-amp designs are excellent in low voltage situations, however they typically cannot run at the same speed as normal designs because of the time needed for the op-amps to settle every clock period.

2.4.2 A Precision Low-Power Mismatch-Compensated Sample-and-Hold Circuit for Biomedical Applications [8]

The research presented in [8] is a low-power switched capacitor buffer specifically designed for biomedical applications. What makes this design interesting is that it features a mismatch compensation technique which makes it insensitive to capacitor mismatch, offset, and finite op-amp gain. The main disadvantage of such a system is the increased number of clock phases, which add complexity and slow the circuit down. The schematic for the design is shown in [8].

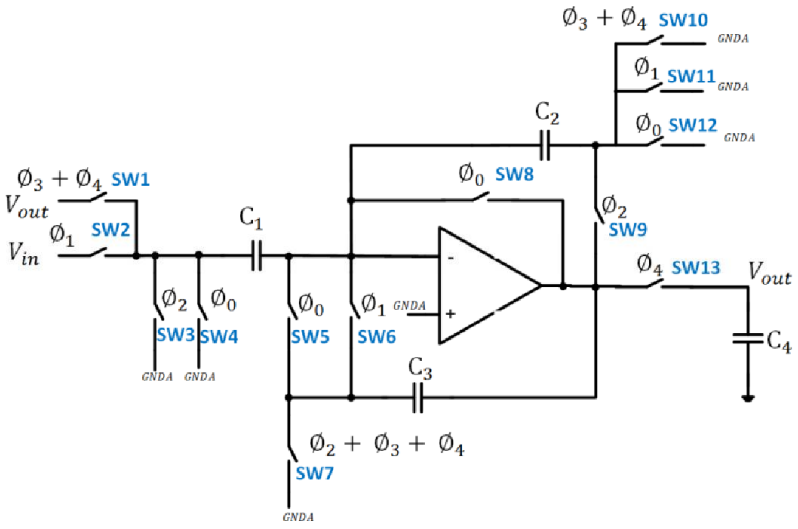

Figure 2-7: Mismatch compensation proposed in [8]

2.4.3 An Ultra Low-Power CMOS EMG Amplifier with High Efficiency in Operation Frequency per Power [9]

The design proposed in [9] is especially applicable to the integrated biosensor project because the design is specifically tailored towards low-power and low-bandwidth applications. Using a single stage with a gain of 100V/V, the amplifier uses just 15.14µW and has a bandwidth of 3.2kHz with a 32kHz clock. The most interesting aspect of this research is that

power in the op-amp was reduced by lowering the effective output capacitance that the op-amp has to drive through series capacitors. The concept is shown in Figure 2-8 below.

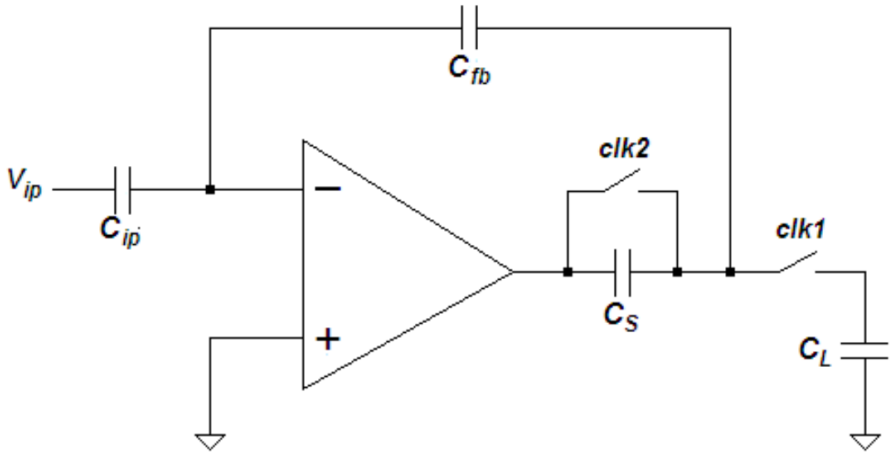

Figure 2-8: Effecting load capacitance reduction in [9]

While this technique has the obvious benefit of lower op-amp power consumption it also has several disadvantages. First of all the effective output swing of the reduced because a change in the output voltage of the op-amp does not result in the same magnitude of voltage change appearing at the amplifier output. The loss in output swing makes this design impractical in low-voltage situations. Secondly, this design compensates for large capacitors by adding more capacitors to the circuit, meaning that in a silicon layout it would not be layout efficient. While the design is extremely interesting it was not implemented in silicon, and thus its real world performance cannot be evaluated.

2.5 Previous Research in Low-Power Switched-Capacitor Sigma-Delta Modulators

There are many different types of analog-to-digital converters which can be implemented. Some examples common examples include Sigma-Delta, successive approximation register (SAR), pipelined, and flash ADCs. Counter based ADCs are also feasible and are implemented in the integrated biosensors reviewed in Section 2.3. All of these architectures offer certain strengths and weaknesses which are summarized in Figure 2-9. Sigma-Delta ADCs offer high resolution at low sampling rates, while pipelined and flash ADCs work at very high sampling rates but low resolution. Sigma-Delta ADCs are the perfect solution for an integrated biosensor because high accuracy is required, and since biological reactions are very slow and low sampling rate is acceptable. Sigma-Delta ADCs are also perfect for small, low-power applications because relatively low-performance components can be used to create a high-precision converter.

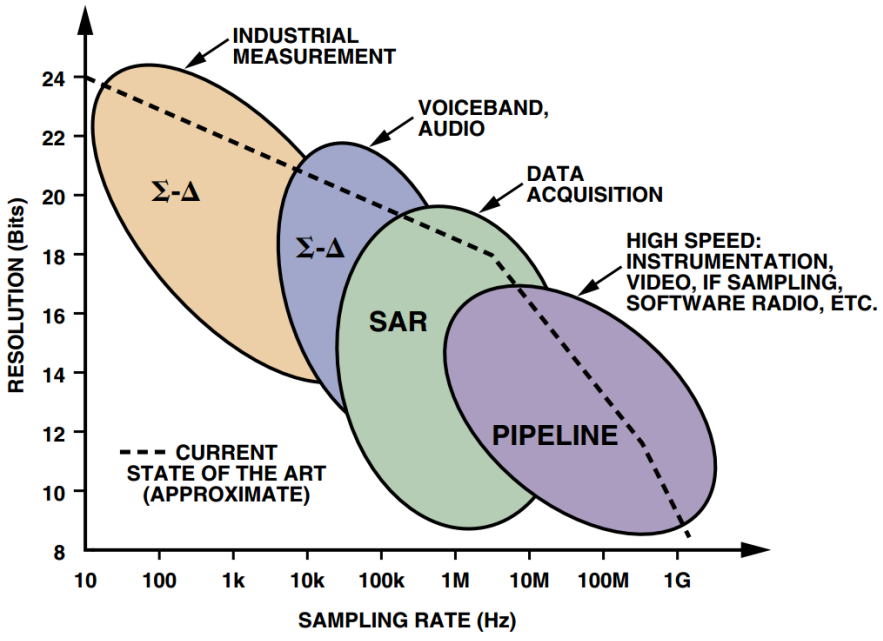

Figure 2-9: ADC topology comparison courtesy of [10]

2.5.1 A Low-Voltage Low-Power Sigma-Delta Modulator for Bio-potential Signals [11]

While the work proposed in [11] is not implemented in a biosensor device, it's intended purpose is the measurement of biological signals and has many parallels to this research. The design implements a 2nd order Sigma-Delta modulator in 0.18µm CMOS using a 900mV supply voltage. At these low supply voltages boosted clock voltages are normally needed to pass signals through switches, but instead [11] uses a switched op-amp technique shown in Figure 2-10. This design achieves a 70.2dB signal-to-noise ratio with 10kHz bandwidth and 60µW power consumption.

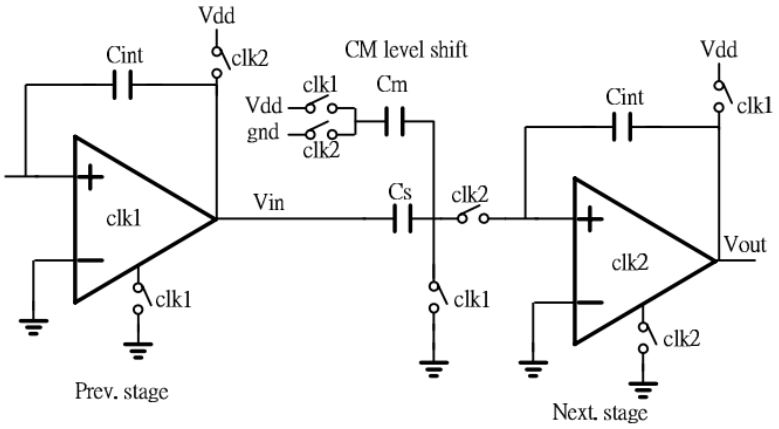

Figure 2-10: Switched op-amp technique in [11]

2.5.2 A 0.7V 36µW 85dB-DR Audio Sigma-Delta Modulator Using Class-C Inverter [12]

The research proposed in [12] is intended for audio processing applications but it uses an extremely interesting low-power inverter based architecture. Rather than use traditional op-amps, simple inverters are used in a pseudo-differential configuration.

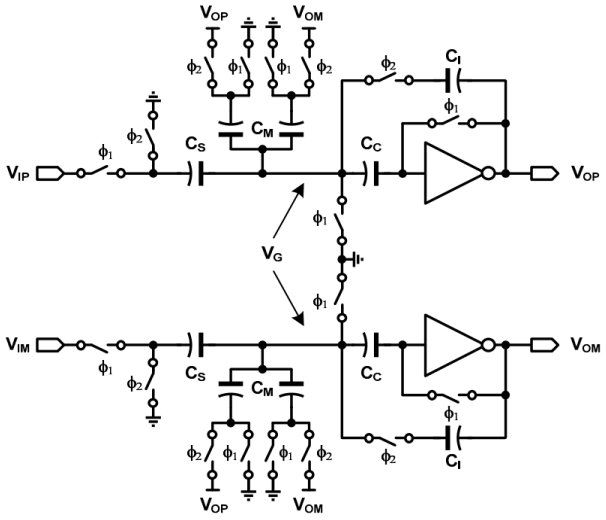

Figure 2-11: Inverter-based integrator proposed in [12]

Using inverters allows the modulator to operate at extremely low supply voltages. Overall it uses a 3rd order architecture and achieves a 81dB signal-to-noise ratio with 20kHz bandwidth and 700mV supply voltage. The design is implemented in 0.18µm CMOS with a total power consumption of 36µW.

2.5.3 A 84dB SNDR 100kHz Bandwidth Low-Power Single Op-Amp Third Order SigmaDelta Modulator Consuming 140µW [13]

[13] proposes an alternate scheme for saving power by using a single op-amp for multiple integration stages within the modulator. A multi-bit digital-to-analog converter (DAC) is used to provide feedback within the modulator which also increases efficiency versus other designs which implement single-bit feedback. The block diagram is shown in

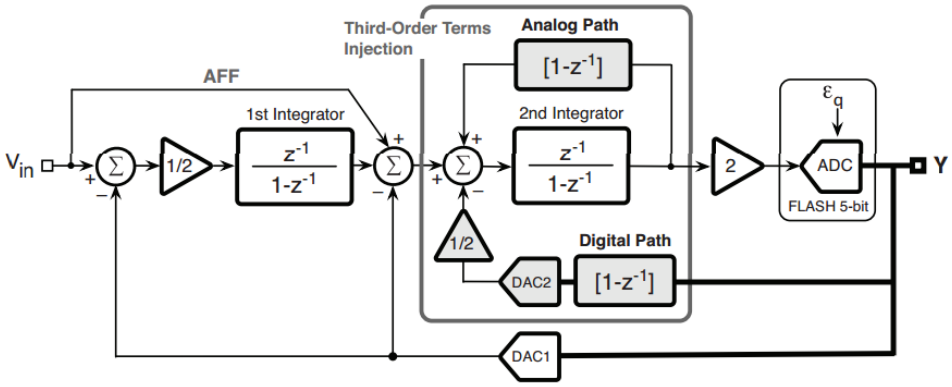

Figure 2-12: Block diagram of modulator proposed in [13]

Using these architecture enhancements very promising results were achieved. The modulator offers 84DB SNDR over 100kHz bandwidth while using just 140µW. The design is implemented in 0.18µm CMOS with 1.5V supply voltage.

2.5.4 A 250mV 7.5µW 61dB SNDR CMOS SC ΣΔ Modulator Using a Near-Threshold-Voltage-Biased CMOS Inverter Technique [14]

The work proposed in [14] takes the idea of low-voltage design to the extreme by using a supply voltage of only 250mV. As in [12], inverters are used in place of traditional op-amps as they are the only structure that can function at such low voltages. The design achieves 61dB SNDR over a 10kHz bandwidth while using just 7.5µW.

2.6 Summary

In summary, there have been many previous attempts to build integrated biosensors and/or components that are needed for an integrated biosensor. However, previous attempts fail to realize the specific characteristics needed to measure neurotransmitters on a cellular level.

1. The electrode density of previous worked designed to sense current is much too low to detect neurotransmitters at high resolutions. High density biosensors have been developed, but they are only capable of detecting electrical potential, not chemical concentrations.
2. The temporal resolution and sensitivity of existing designs is poor due to the use of counter based analog-to-digital converters.
3. Low-power and high-resolution amplifiers and analog-to-digital converters have been proposed, however circuit area is often sacrificed to achieve high performance. An integrated amplifier and analog-to-digital converter signal chain with minimal silicon area has yet to be presented.

By addressing these issues, the goal of an integrated biosensor system with excellent spatial and temporal resolution can be accomplished.

Chapter 3: Proposed Main-Amplifier Design

3.1 Introduction

In the biosensor signal chain introduced in Figure 1-2, a main amplifier is needed to amplify the small biological signals to match the input needed by the analog-to-digital converter. This chapter will outline the proposed main-amplifier for use in the integrated biosensor system. Section 3.2 will introduce design objectives, while Section 3.3 will discuss the top-level design of the main-amplifier. Sections 3.4 and 3.5 cover the design of the op-amp used within the amplifier and the common-mode feedback scheme respectively. Section 3.6 will outline implementation of the main-amplifier and Section 3.7 the will detail the computer simulation results of the proposed design. Two versions of the main-amplifier will be presented, henceforth referred to as Revision A and Revision B. Revision A has been implemented in silicon and its test results are discussed in Chapter 5. Revision B is an improved version of Revision A and has not yet been fabricated, so only simulation results for this circuit will be discussed.

3.2 Objectives

In order to support a working system a variety of design goals needed to be met with the main-amplifier. As discussed previously, power consumption and die area are the main constraints, and they must both be minimized. However, gain, bandwidth, noise and resolution

are all important parameters. The complete list of design specifications are shown in Table 3-1 below.

Table 3-1: Main-Amplifier Design Goals

Specification	Target
Gain	100V/V (40dB)
Signal Bandwidth	1kHz
Clock Frequency	1MHz
Supply Voltage	900mV (Split rail +/- 450mV)
Technology	0.18µm CMOS
Resolution	10-bit or greater
Input Referred Noise	Minimal
Power Consumption	Minimal
Silicon Area	Minimal

Clock frequency, supply voltage, and signal bandwidth for the main-amplifier were determined based on system-wide design goals. The 0.18µm CMOS process usually uses a 1.8V supply, however to reduce the overall power consumption of the microchip the supply voltage was cut in half to 900mV. A 1MHz clock was also chosen in order to reduce power, but also because it satisfies the oversampling requirements of the Sigma-Delta modulator proposed in Chapter 4. Similarly, 1kHz signal bandwidth is more than sufficient to accurately amplify slow biological signals.

The gain required by the main-amplifier was determined based on the output characteristics of the transimpedance amplifier as well as the input characteristics of the Sigma-Delta modulator. The maximum expected differential output of the transimpedance amplifier is approximately 6mV peak-to-peak, and the maximum differential input voltage of the modulator

is 600mV peak-to-peak. Based on these output and input requirements, it was easy to determine that the main-amplifier would require a gain of 100V/V, or 40dB.

Resolution and input referred noise specifications are simply goals which will impact the overall performance of the system. Since the currents being detected at the electrode sites are extremely small, noise in the amplification stage of the signal chain increases the uncertainty of this measurement. Also, the resolution of the Sigma-Delta modulator proposed in Chapter 4 is approximately 14 bits, and thus if the resolution of the main-amplifier is very low then the power burned by the modulator is wasted.

3.3 Top-Level Design

The design for the proposed main-amplifier is an extension of the work proposed in [15]. While the design presented in [15] is very similar to the proposed design, it was a simple low-gain amplifier which would not work in the overall biosensor system. Building off of [15], the first step in designing the main-amplifier for the biosensor was to decide on the optimal number of stages based on the known constraints of the system. In the simple switched-capacitor amplifier shown below in Figure 3-1, the gain of the circuit is determined by the ratio of the input and feedback capacitors as described by Equation 3-1.

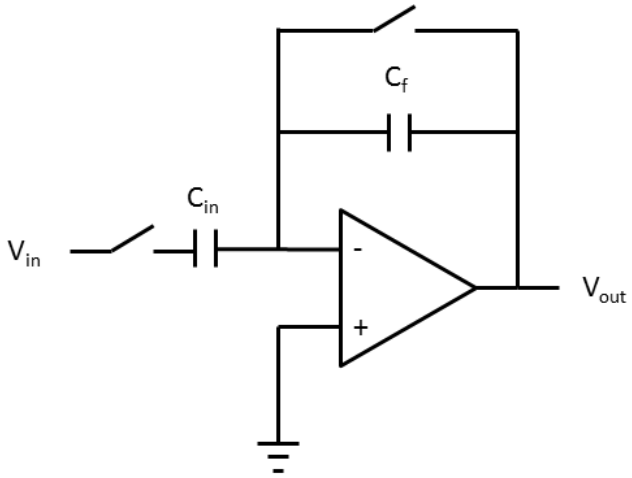

Figure 3-1: Basic switched-capacitor amplifier

$$\frac{V_{out}}{V_{in}} = -\frac{C_{in}}{C_f}$$

Equation 3-1: Ideal switched-capacitor amplifier gain

In order to achieve a high gain, a large capacitor ratio can be used or multiple amplifiers, each with a smaller gain, can be cascaded. Both of these approaches have advantages and disadvantages, especially when working at extremely low power levels. To find the optimal number of stages for this particular design several factors had to be taken into account:

1) Op-amp gain is limited to 200V/V (46dB) because low-power, single stage op-amps will be used in the final design.
2) Capacitor area, which should be minimized, will dominate the total area of the circuit.
3) Minimum capacitor size is 148.5fF based on the silicon process.
4) Capacitors occupy roughly 1,717μm^2/pF

Based on the first assumption the gain error associated with using a non-ideal op-amp becomes very significant in this application. When considering the finite open loop gain of the op-amp the overall gain of the switched capacitor amplifier can be defined as:

$$\frac{V_{out}}{V_{in}} = -\frac{A_{OL}C_{in}}{C_{in} + C_f + A_{OL}C_f}$$

Equation 3-2: Switched-capacitor amplifier gain with finite op-amp gain

This equation shows that as the capacitor ratio C_{in}/C_f increases the actual gain of the amplifier will become less and less ideal. If the capacitance ratio becomes large enough then the gain error of the overall amplifier will be very large. Table 3-2 compares the performance and size of using different numbers of stages to achieve a gain of 100V/V.

Table 3-2: Characteristics of multi-stage amplifiers

Number of Stages	Amplification per Stage	Input Capacitance (per stage)	Feedback Capacitance (per stage)	Total Capacitance	Capacitor Area	Gain Error
1	100	14.85pF	148.5fF	29.997pF	51,505μm^2	33.5%
2	10	1.485pF	148.5fF	6.534pF	11,719μm^2	10.1%
3	4.64	689.3fF	148.5fF	5.027pF	8,631μm^2	7.96%
4	3.13	469.6fF	148.5fF	4.945pF	8,491μm^2	7.91%
5	2.51	373fF	148.5fF	5.215pF	8,954μm^2	8.34%

The table shows that using a single stage amplifier would be a very poor choice. Because the capacitance ratio and gain of the op-amp are comparable in this case, the gain error is very large. Also, since the feedback capacitor can be no smaller than 148.5fF the input capacitors must be very large and thus the area occupied by the circuit would be very large. Choosing three to four stages results in the smallest capacitor area and gain error, and since the improvements when moving from three to four stages are so small it is not worth the extra complexity of implementing 4 stages. Based on these calculations a three stage design was chosen. Also, by

lowering the input capacitance through a three stage design the power consumption of the transimpedance amplifier can be reduced because it drives a smaller capacitive load. While non-integer gains were used to simplify calculations for the table, in order to improve capacitor matching in the layout an integer gain was chosen for each stage. A top level schematic of the main-amplifier with correct gain for each stage is shown in Figure 3-2.

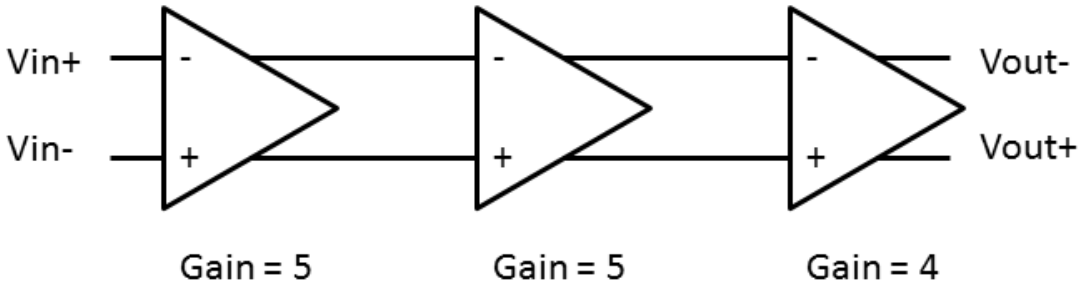

Figure 3-2: Three stage main-amplifier design

3.4 Op-Amp Design

3.4.1 Op-Amp Topology

Designing op-amps which are suitable to low-voltage situations is not a trivial task. Traditional op-amp architectures using MOSFETs are based around keeping large stacks of transistors operating in the saturation region. The best example of this is the classical folded-cascode architecture, which can provide exceptional performance in a relatively simple package. At low supply voltages however, designs such as the folded-cascode become impractical because the transistors cannot be kept in the saturation region, and thus performance degrades. Popular

low-voltage solutions today are op-amps based on the CMOS inverter rather than traditional architectures.

The op-amp used in the proposed main-amplifier is based on the work first proposed in [16] and [17]. This architecture, shown in Figure 3-3, utilizes a pair of CMOS inverters coupled together with a cross-couples CMOS inverter load to create a fully differential amplifier.

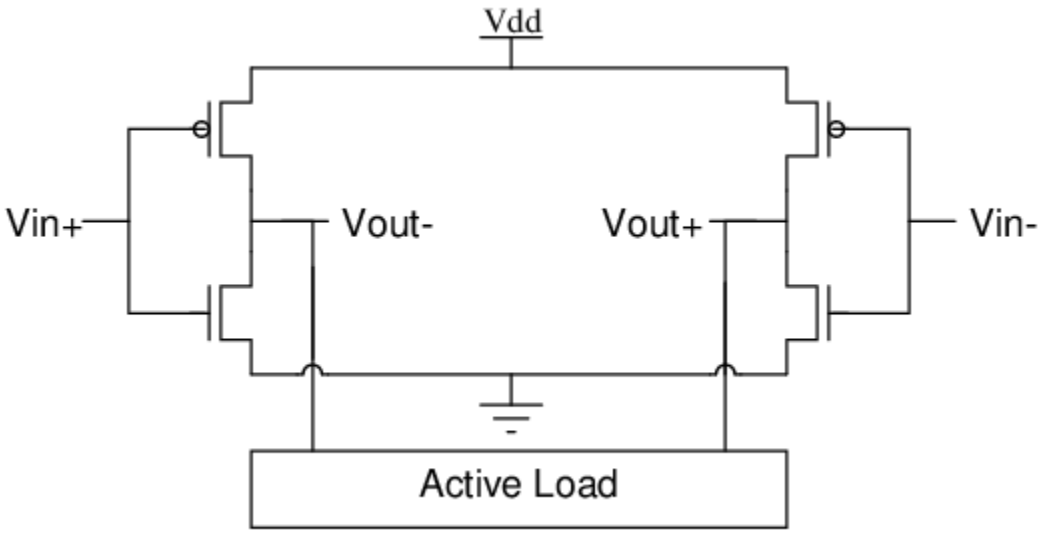

Figure 3-3: Inverter based op-amp proposed in [16] and [17]

This op-amp architecture was originally designed to work with normal supply voltages. In this case, large amounts of current can flow through the inverters, and since it is a simple single-stage architecture incredible bandwidths can be achieved. This architecture also benefits from enhanced gain versus other single stage designs. Since the op-amp input terminals are connected to both the NMOS and PMOS devices of the inverter, the transconductance of the input stage is the sum of the two transistors as shown in Equation 3-3.

$$g_m = g_{m\_n} + g_{m\_p}$$

Equation 3-3: Total transcoductance of inverter op-amp input stage

This architecture becomes even more interesting when low supply voltages are used. As the supply voltage drops, the transistors drop into the sub-threshold region and the bias current through the op-amp decreases dramatically. However, compared to traditional op-amp architectures operating in the sub-threshold region the bandwidth and gain remain high.

For all of its benefits this op-amp does have a few drawbacks. First of all, the cross coupled nature of the active load connecting the positive and negative sides of the op-amp means that the output voltage cannot swing rail to rail without becoming unstable. Secondly, since there is no tail to regulate the total current flowing through the input inverters, the op-amp has very poor common-mode and power supply noise rejection. Finally, while the diode connected inverters in the cross coupled load tend to hold the output common-mode voltage close to half-VDD, in this architecture there are no terminals where a common-mode feedback loop can be connected.

The first step towards solving these problems was to add a pair of tails to the top and bottom of the input inverters. This architecture was first presented in [18] and can is shown in Figure 3-4 below. The addition of the tails allowed for the current through the input inverters to be regulated and increased the op-amps common-mode and power supply rejection ratio. The gate voltage of the tails also provides a terminal to apply common-mode feedback which allows the op-amp to work better in multi-stage systems such as the proposed main-amplifier.

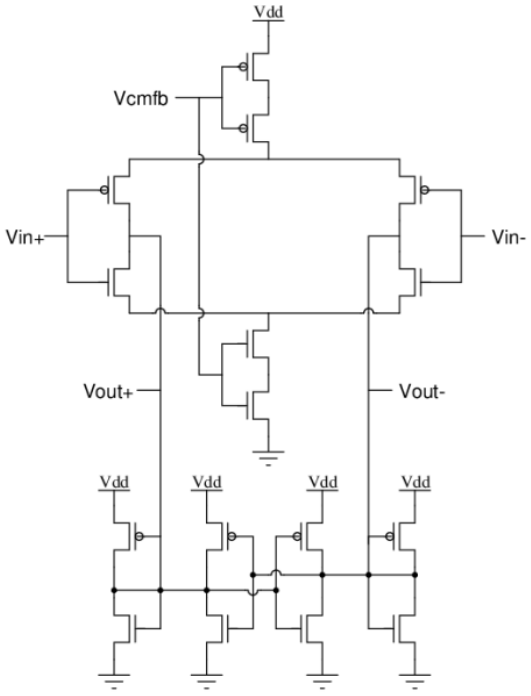

Figure 3-4: Inverter based op-amp proposed in [18]

While these changes allowed improved greatly on the original op-amp from [16] and [17], further testing of the op-amp proposed in [18] showed that with the addition of the tail transistors, the cross-coupled load was no longer necessary. This testing led to the final op-amp architecture shown in Figure 3-5.

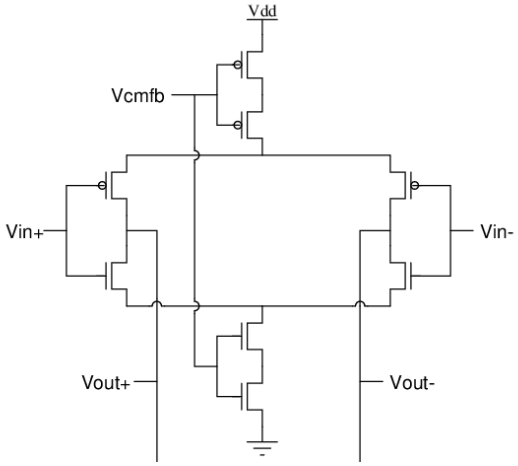

Figure 3-5: Proposed inverter based op-amp architecture

The proposed design improves the deficiency of the designs proposed in [17] and [18] maintains excellent gain and bandwidth with low power consumption. With only eight transistors, the op-amp is also easy to design and implement in layout. As an added bonus, since the op-amp is a single stage design it does not need internal compensation and is inherently stable.

3.4.2 Transistor Sizing

Sizing the transistors for an op-amp with this architecture is relatively simple. The transistors making up the input inverters have large W/L ratios and long lengths to promote high gain and reduce the op-amp's offset voltage. The tails use self cascodes to increase their output impedance and increase the common mode rejection ratio of the op-amp. Since there is very little voltage drop across the tails (approximately 50mV) they also have very large W/L ratios in order to supply the needed current for the input inverters. Under normal operation the input and output common mode voltages, along with the common mode feedback voltage, are centered at half VDD. The sizes for the transistors used in the proposed op-amp are shown in Table 3-3 below.

Table 3-3: Op-Amp Transistor Sizing

Transistor Name	Type	Function	Width/Length	Fingers	Effective Width
M1	PMOS	Input	12.28µm/1.5µm	8	96.24µm
M2	PMOS	Input	12.28µm/1.5µm	8	96.24µm
M3	NMOS	Input	4.685µm/1.5µm	8	37.48µm
M4	NMOS	Input	4.685µm/1.5µm	8	37.48µm
M5	PMOS	Dummy	12.28µm/1.5µm	4	49.12µm
M6	NMOS	Dummy	4.685µm/1.5µm	4	18.74µm
M7	PMOS	P-Tail	7.535µm/1.5µm	8	60.28µm
M8	PMOS	P-Tail	8.135µm/1.5µm	8	65.08µm
M9	PMOS	Dummy	7.535µm/1.5µm	2	15.07µm
M10	PMOS	Dummy	8.135µm/1.5µm	2	16.27µm
M11	NMOS	N-Tail	3.88µm/1.5µm	8	31.04µm
M12	NMOS	N-Tail	3.925µm/1.5µm	8	31.4µm
M13	NMOS	Dummy	3.88µm/1.5µm	2	7.76µm
M14	NMOS	Dummy	3.925µm/1.5µm	2	7.85µm

3.4.3 Op-Amp Layout

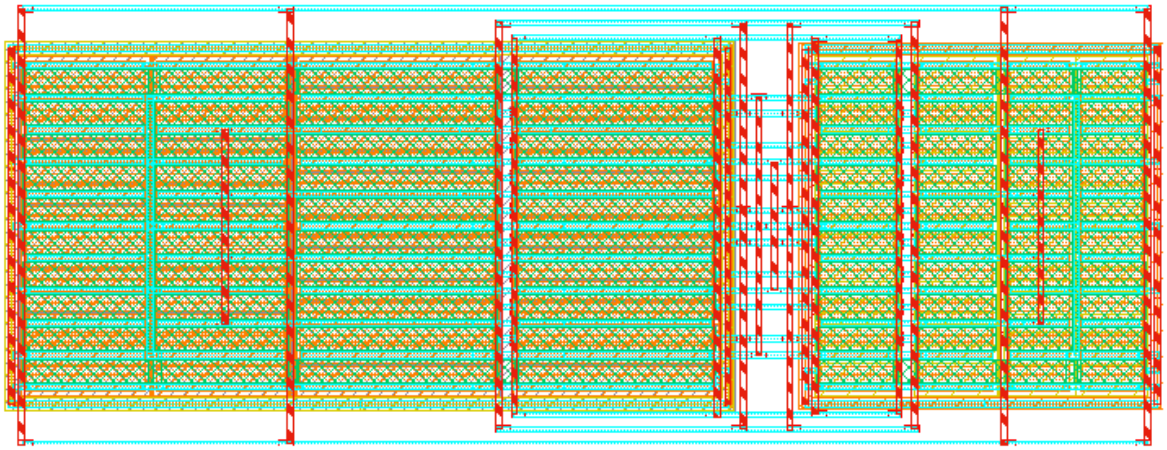

Figure 3-6: Proposed op-amp layout

The layout of the op-amp is shown in Figure 3-6 above. All of the transistors in the op-amp are placed in common-centroid arrangements to improve matching. Also, dummy transistors are placed at the end of every row to reduce edge effects. PMOS devices are all located within an

n-well on the left side of the layout while NMOS devices are located on the right half of the layout. Input and output connections are made in the small gap between the NMOS and PMOS devices. The layout measures 73.57µm by 27.94µm and occupies a total area of 0.0021mm^2.

3.4.4 Op-Amp Simulation Results

Simulation results of the fully extracted op-amp layout are presented below. Figure 3-7 shows the gain and phase plots of the op-amp output while Table 3-4 summarizes the performance of the op-amp. Overall the op-amp has a gain of 48.53 dB and a gain-bandwidth product of 7.9MHz while consuming just 2.31µW from a 900mV supply.

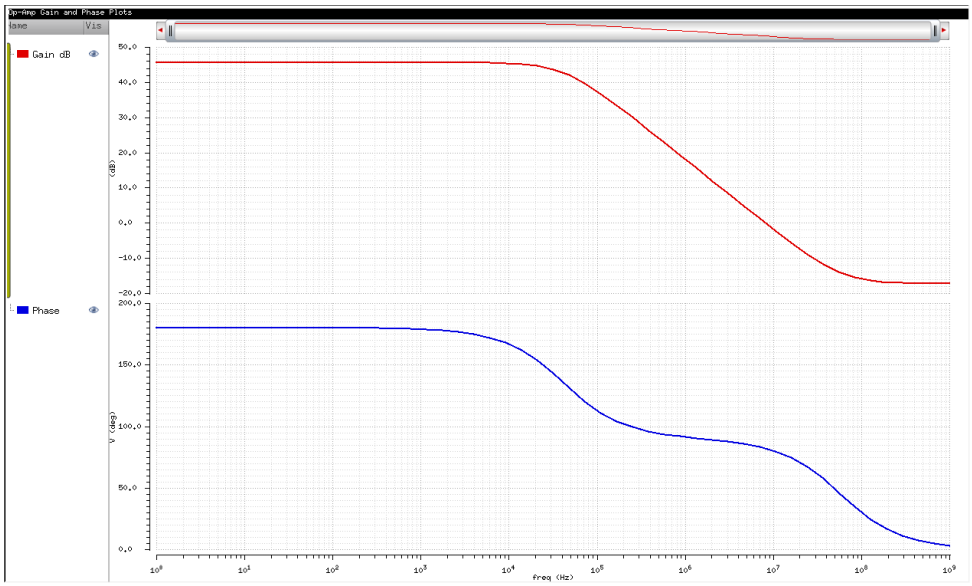

Figure 3-7: Op-Amp Gain and Phase vs. Frequency

Table 3-4: Op-amp performance characteristics

Parameter	Results
DC Gain	48.53dB
Phase Margin	82.2 degrees
Gain-Bandwidth Product (with 1 pf load)	7.9MHz
Power Consumption	2.31µW
Integrated Input Referred Noise	3.37µV
Offset Voltage	1.955mV

Since the transistors in the op-amp operate in the sub-threshold region, large devices are needed get the desired current level. These large devices have the benefit of reducing the overall noise and offset voltage of the op-amp. As the table shows, the input referred noise is just 3.37µV and offset voltage is only 1.955mV. Overall these results prove that the proposed op-amp is incredibly efficient. In order to compare this topology against other designs a common figure of merit was used to compute the efficiency of the op-amp. The figure of merit is calculated as:

$$FOM = \frac{GBW(MHz) \times C_L(pF)}{I(mA)}$$

Equation 3-4: Op-amp figure of merit calculation

Based on this equation the proposed op-amp achieves a figure of merit of 3081. Table 3-5 compares the proposed design to existing architectures. This is much greater than the figures of merit reported for traditional architectures such as cascode, telescopic, or miller compensated designs. One architecture that is able to achieve a higher figure of merit is the 2-stage cross coupled design proposed in [19]. This design uses a cross coupled active load which produces negative output impedance, allowing for greatly increased bandwidth. While this design provides excellent efficiency, architectures such as this are hard to implement because of the inherent

instability of cross coupled designs. In general, the proposed op-amp excels because of its efficiency. Because it only uses eight transistors, it is easy to design and implement.

Table 3-5: Comparison of op-amp figures of merit

Design	Figure of Merit
Proposed Op-Amp	3081
High Swing Telescopic [20]	225
Cascode [21]	80
Nested Miller Compensated [22]	1053
2-Stage Cross Coupled [19]	4889

3.5 Common Mode Feedback

3.5.1 Common-Mode Feedback Schematic Design

In any fully differential amplifier a common mode feedback system is needed to ensure that the output common mode voltage of the amplifier does not drift. In the proposed three stage main-amplifier, each stage needs its own common mode feedback circuit to make sure its output will comply with the input common mode requirements of the next stage. The common mode feedback circuit used in the proposed design is shown in Figure 3-8:

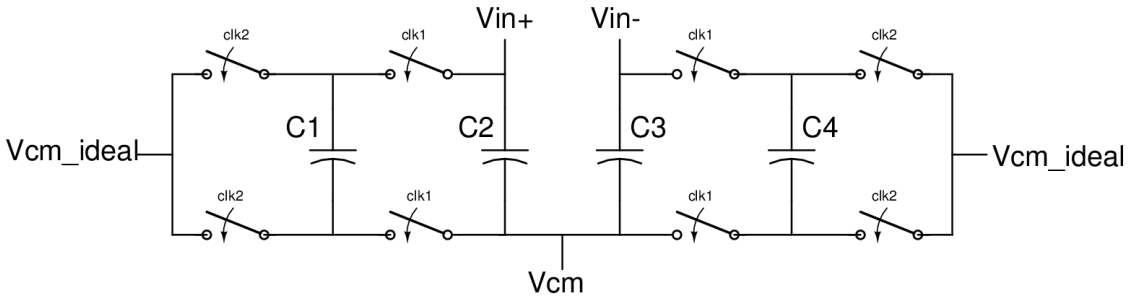

Figure 3-8: Common mode feedback circuit schematic

This circuit works using a two-phase clocking scheme. When clk2 is high, the ideal common mode voltage, in this case ground, is sampled on to capacitors C1 and C4. At the same

time the output of the amplifier is stored on capacitors C2 and C3. During the next clock phase, clk2 goes high and the amplifier output voltage is summed with the ideal common mode output voltage. This causes the current output common mode voltage to appear at the Vcm pin. This voltage is fed back to the common mode feedback terminal on the op-amp. During startup, this circuit requires several clock cycles to properly set the output common mode, however once set the output common mode voltage remains very stable. The simulation shown below in Figure 3-9 illustrates the common-mode feedback circuit stabilizing as the circuit starts up.

Figure 3-9: Common-mode feedback simulation

The switches within the common-mode feedback circuit are implemented as NMOS transistors driven by a bootstrapped non-overlapping clock generator. All of the transistors have a width of 540nm and a length of 180nm. Capacitor sizes within the circuit are kept small to lessen the capacitive loading of the op-amp. The ratio of capacitor sizes within the circuit is also important. The inner capacitors are kept the minimum size of 148.5fF while the outer capacitors

are double the size, 297fF. This ratio allows for a more stable common-mode feedback voltage than if all the capacitors were the same size.

3.5.2 Common Mode Feedback Layout

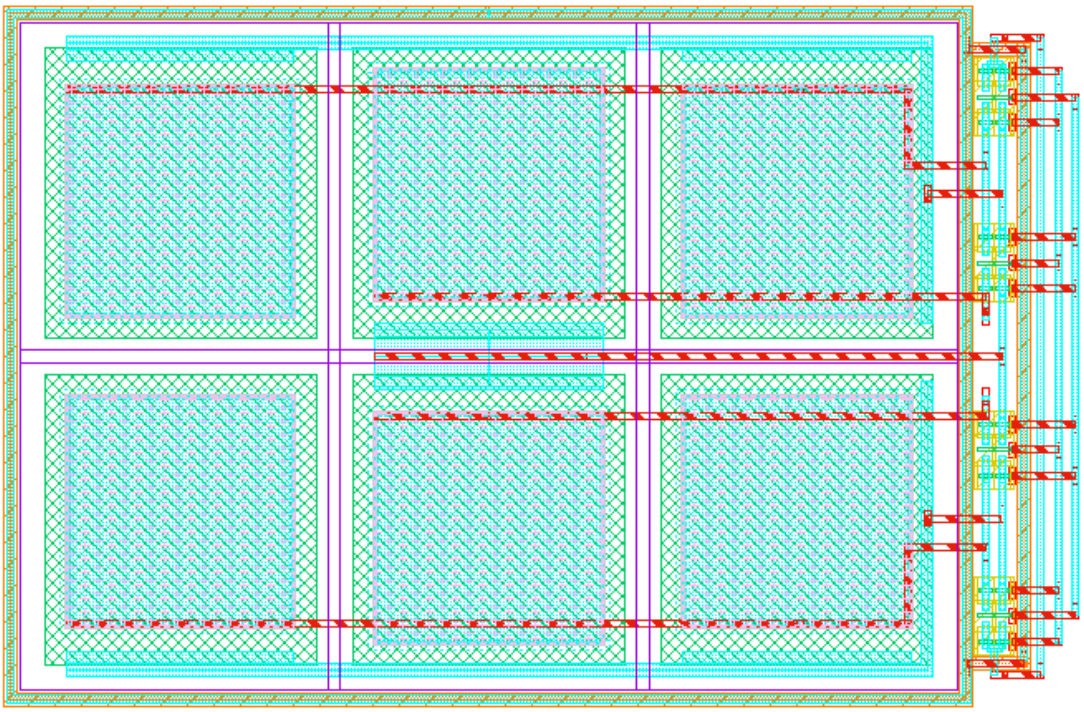

Figure 3-10: Common-mode feedback circuit layout

The layout for the common mode feedback circuit is shown above in Figure 3-10. The capacitors are the large blue rectangles which occupy most of the layout. The inputs, output, clock bus, and switches are all located along the right edge of the layout. Again, a common centroid layout is used to increase matching of the capacitors in the circuit, and guard rings are placed around the capacitors and switches to ensure that substrate noise does not impact the common mode feedback circuit. The layout measures 61.34µm by 39.9µm and occupies a total area of 0.0024mm^2.

3.6 Main-Amplifier Design Specifics

3.6.1 Main-Amplifier Schematic Design

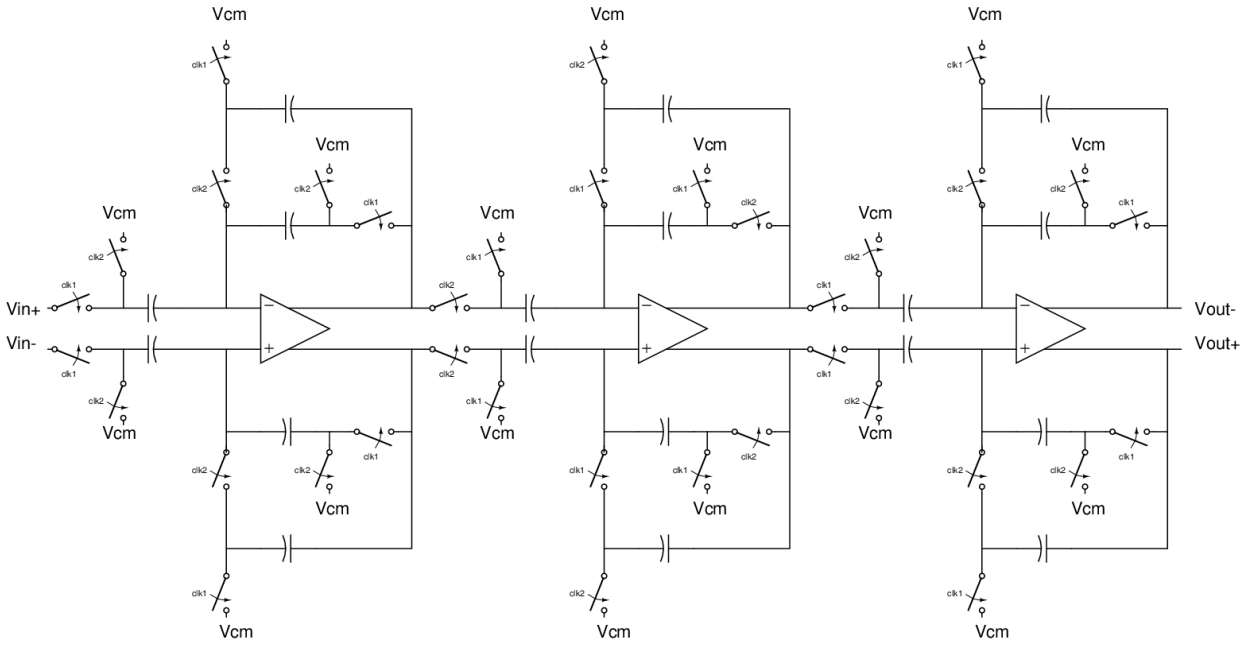

Figure 3-11: Proposed main-amplifier schematic

The schematic for the proposed main-amplifier is shown above in Figure 3-11. As originally discussed in Section 3-3, the amplifier uses a three stage design which is clearly visible in the figure. Unlike the simple switched-capacitor amplifier shown in Figure 3-1, the proposed design uses two feedback capacitors instead of one. During operation, on the first clock phase the input signal is sampled and amplified, while during the second clock phase the amplifier's output is stored onto the second feedback capacitor. This allows the amplifier to maintain it's out output during both phases of the clock instead of resetting the output to the common-mode voltage. This architecture allows for a lower power op-amp because the slew requirements are greatly reduced.

3.6.2 Revision A and B Differences

Both main-amplifier revisions, A and B, implement the same architecture and use the same op-amp described in Figure 3-5. Revision B is simply an improved version of the original design optimized for low noise. As such, the differences between the revisions are the absolute size of the capacitors used and the clock speed that each is run with. Revision B uses a 500kHz clock rather than 1MHz in order to allow for bigger, lower noise capacitors without increasing the power consumption of the op-amp. All switches in the main-amplifier were implemented using NMOS transistor with a width of 540nm and a length of 180nm, driven with a bootstrapped non-overlapping clock generator. The capacitor sizes used in both versions of the main amplifier are shown below in Table 3-6. The input referred noise of Revision A is 119µV while the noise drops to 59.2µV for Revision B.

Table 3-6: Main-amplifier capacitor sizes

Capacitor	**Revision A**	**Revision B**
First Stage Input	742.4fF	2.9696pf
First Stage Feedback	148.5fF	594fF
Second Stage Input	742.4fF	742.4fF
Second Stage Feedback	148.5fF	148.5fF
Third Stage Input	594fF	594fF
Third Stage Feedback	148.5fF	148.5fF

3.6.2 Main-Amplifier Layout

The layouts for revision A and B of the main-amplifier are shown in Figure 3-12 and Figure 3-13 respectively. In order to function well, fully differential circuits such as the main amplifier need to have well matched capacitors and be symmetrical with respect to the positive and negative sides of the amplifier. To accomplish this, the op-amps are placed in the center of

the layout with the matched capacitors and switches flanking the op-amps on either side. Parasitic extractions on the layouts have shown that nodes on the positive and negative sides of the amplifier are matched within 1fF of parasitic capacitance. Revision A of the main-amplifier measures 239.045µm by 226.32µm and occupies 0.0541mm^2 silicon area. Revision B measures 335.785µm by 226.32µm and occupies 0.076mm^2 silicon area.

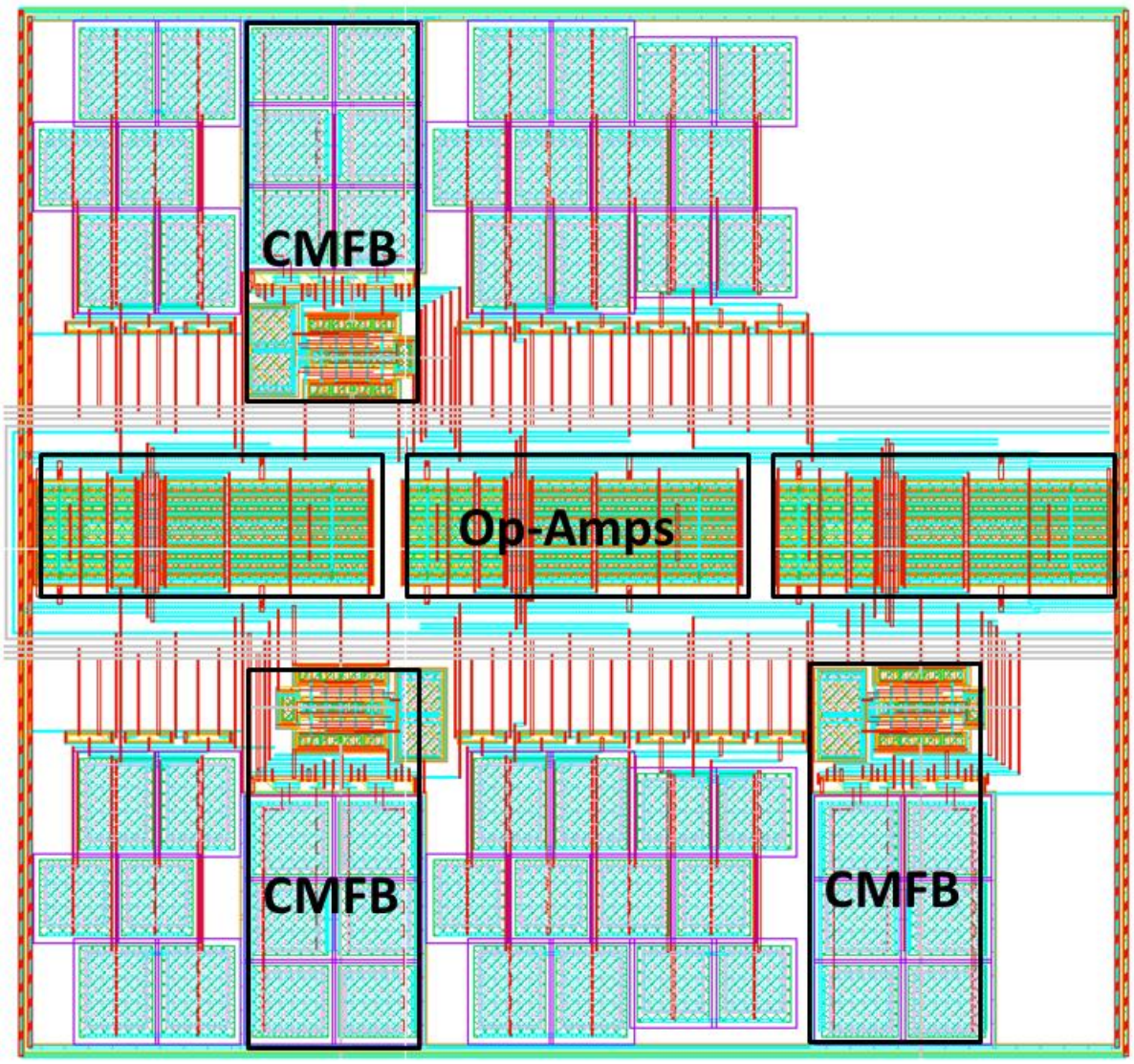

Figure 3-12: Main-amplifier Revision A layout

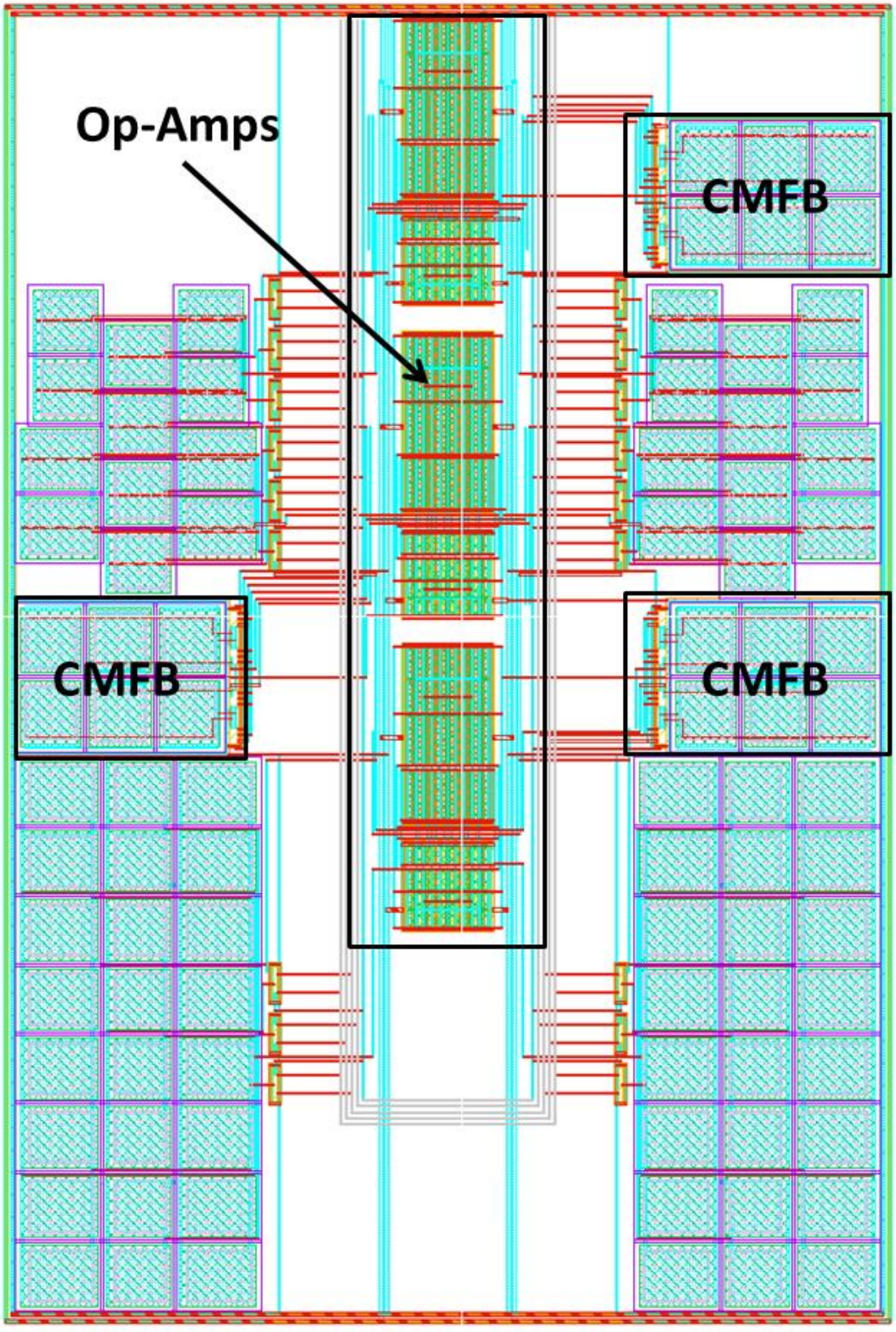

Figure 3-13: Main-amplifier Revision B layout

3.7 Main-Amplifier Simulation Results

The fully extracted layouts of the main-amplifier were used to run simulations and test the performance of the circuits. Figure 3-14 and Figure 3-15 show transient simulations of main-amplifier Revision A, while Figure 3-16 shows the frequency spectrum of the transient simulation. The transient simulations show that the amplifier performs as expected with the desired gain of 100V/V. However, looking at the spectral output reveals more about the quality of the amplifier. Based on the output spectrum the total harmonic distortion of the amplifier was calculated to be -54.31dB which is equivalent to 8.73 bits. Thus, Revision A failed to meet the resolution specification discussed in Section 3.2.

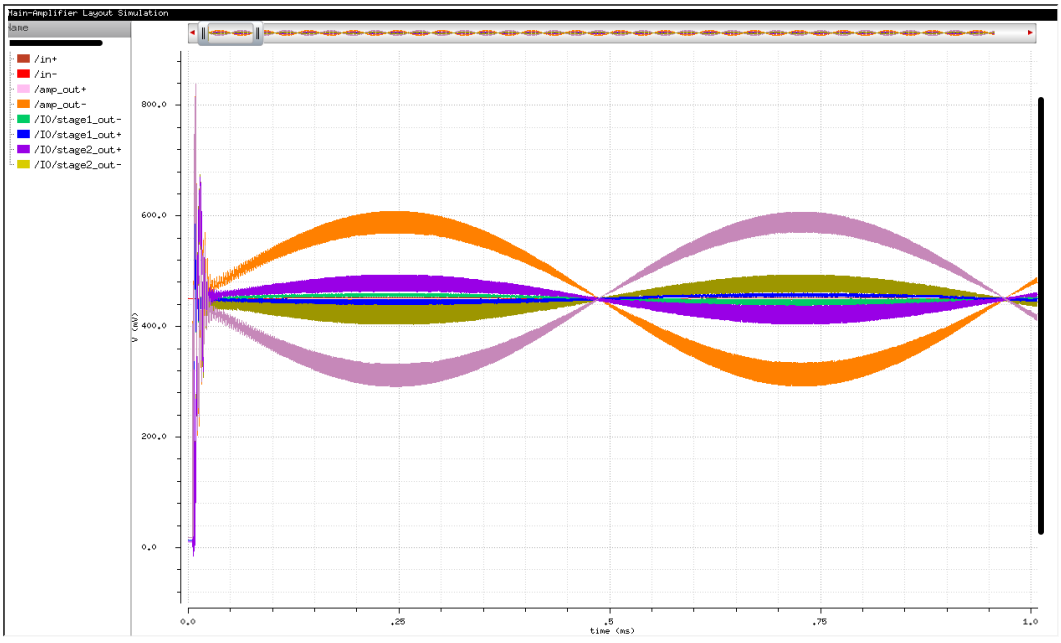

Figure 3-14: Main-amplifier Revision A transient simulation

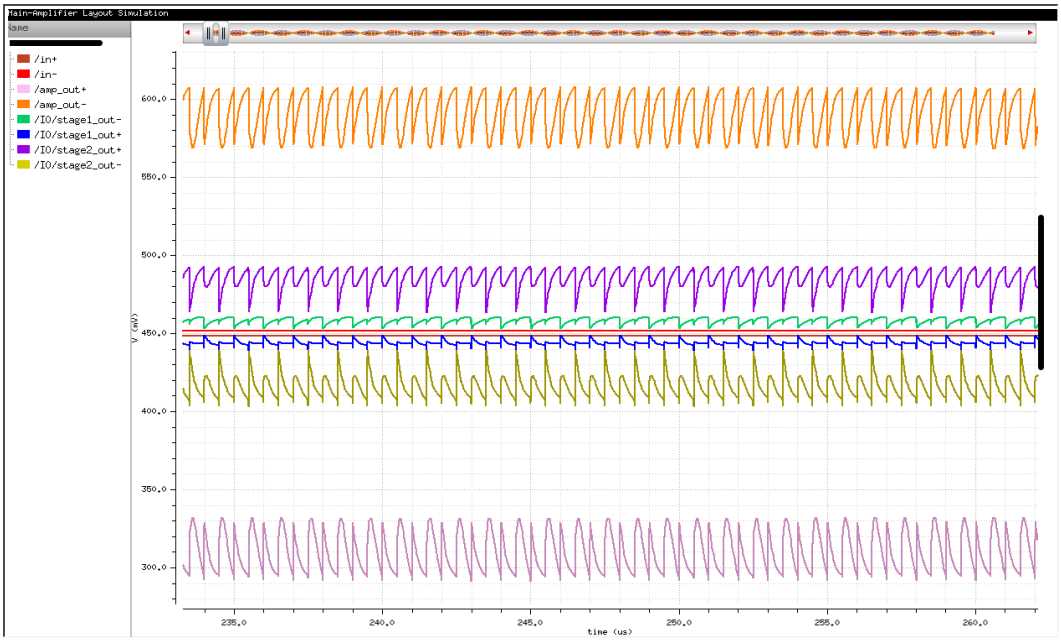

Figure 3-15: Main-amplifier Revision A transient simulation zoomed

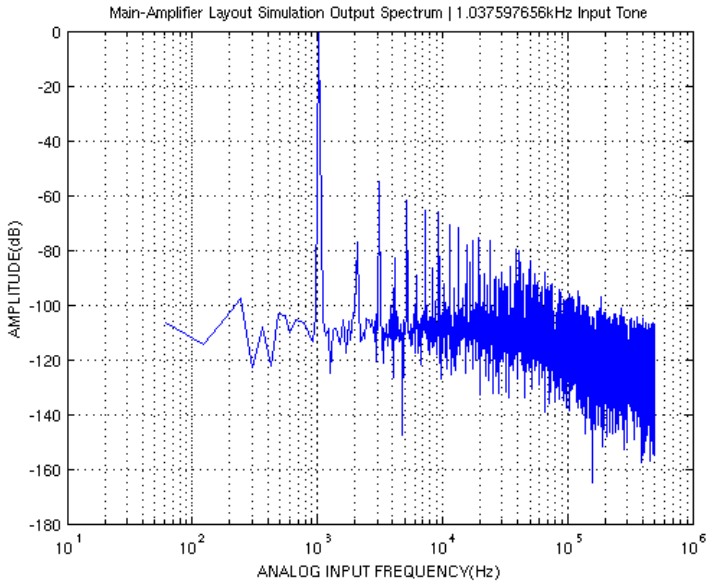

Figure 3-16: Main-amplifier Revision A output spectrum

Figure 3-17 and Figure 3-18 display the transient simulation results of Revision B of the main-amplifier. Once again the transient simulations performed as expected, however in this case

the total harmonic distortion of the output was much better. The total harmonic distortion was calculated as -63.65dB, for an effective resolution of 10.28 bits.

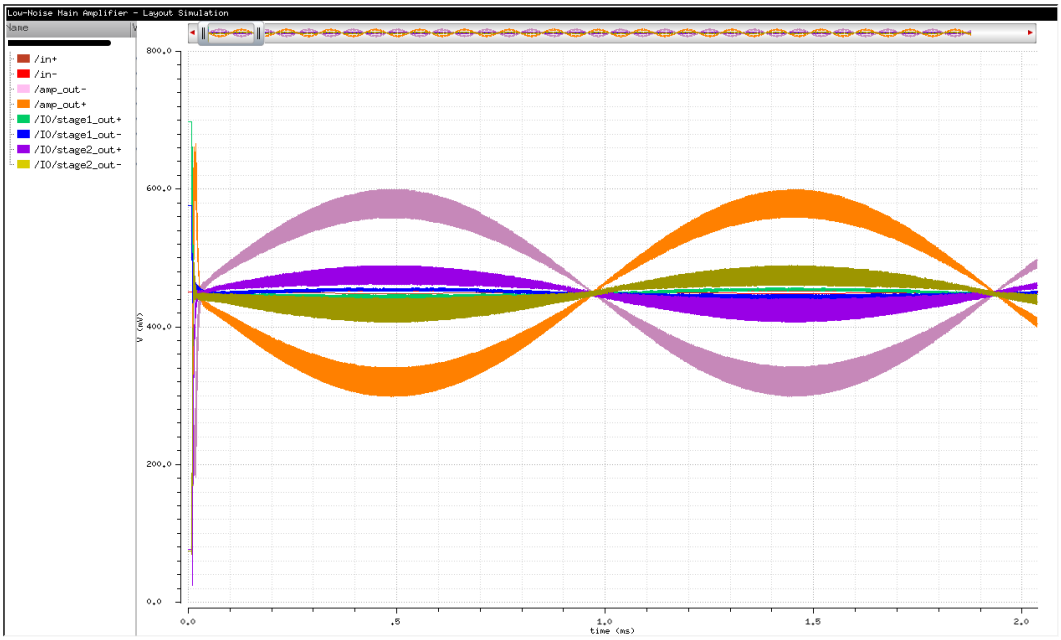

Figure 3-17: Main-amplifier Revision B transient simulation

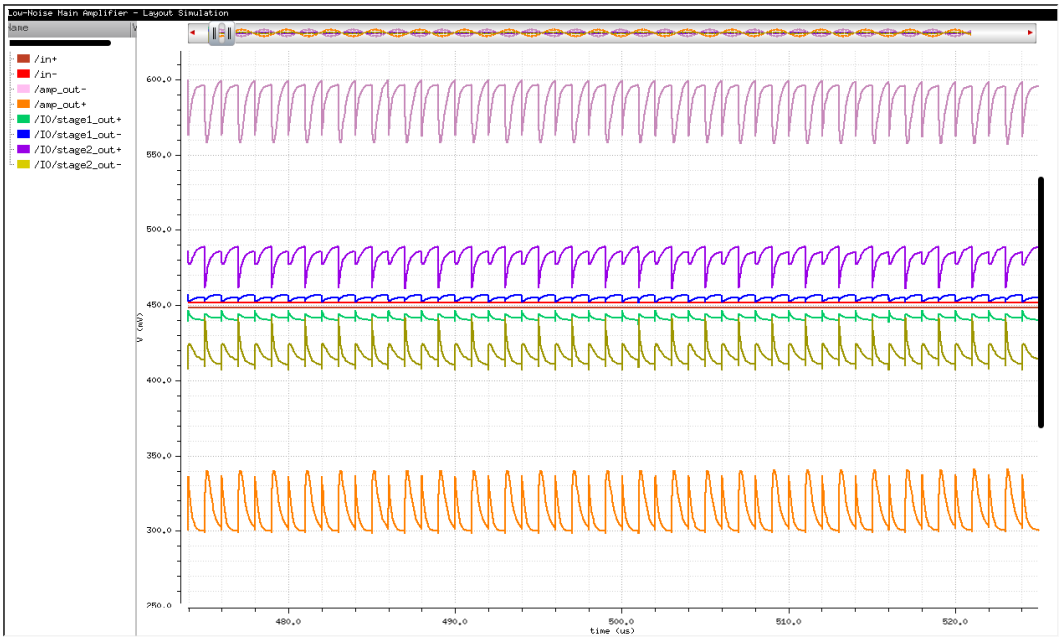

Figure 3-18: Main-amplifier Revision B transient simulation zoomed

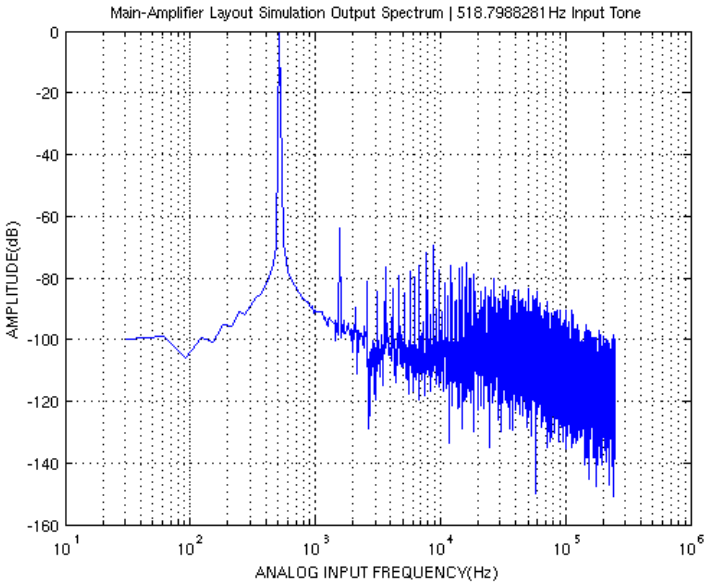

Figure 3-19: Main-amplifier Revision B output spectrum

The performance of the proposed main-amplifier is compared with other reported designs in Table 3-7. In order to compare with other designs a common figure of merit is used to quantify the efficiency of each amplifier. The figure of merit is calculated using Equation 3-5. In this case the lower the figure of merit the greater the efficiency of the amplifier.

$$FOM = \frac{I(\mu A)}{2^{ENOB_{THD}} \times f_s(MHz)}$$

Equation 3-5: Main-amplifier figure of merit

Table 3-7: Main-amplifier performance comparisons

Design	**$ENOB_{THD}$**	**Voltage**	**Power**	**fs**	**Process**	**FOM**
Revision A	8.72 bits	900mV	7.145µW	1MHz	0.18µm	0.019
Revision B	10.28 bits	900mV	6.818µW	500kHz	0.18µm	0.012
[23]	10.46 bits	3.3V	70mW	185MHz	0.35µm	0.081
[7]	8.3 bits	1.2V	1.2mW	40MHz	0.5µm	0.079
[24]	11.46 bits	3V	20mW	250MHz	0.35µm	0.0095
[25]	11.18 bits	800mV	3.5mW	250MHz	0.13µm	0.0075
[8]	12.62 bits	1.8V	12.04µW	128kHz	0.18µm	0.00830
[9]	N/A	1.8V	15.14µW	32kHz	0.18µm	N/A

Compared to [24] and [25], the proposed design is not as efficient, however these designs are intended for high speed, high power applications, so the results are not directly comparable. [8] is a low-power, low-frequency design which compares well to the proposed design. It achieves a better figure of merit than the proposed design, however it uses a full 1.8V supply which benefits its figure of merit. Overall, the proposed design's efficiency is comparable with other recent publications.

Chapter 4: Proposed Sigma-Delta Modulator

4.1 Introduction

This chapter will introduce the design and implementation of the proposed Sigma-Delta modulator for use as the analog-to-digital converter in the biosensor system. During the course of this research, several different modulators were developed iteratively, and thus the design of three separate Sigma-Delta modulators will be presented. Section 4.2 will outline the design goals and objectives for the modulator, and Section 4.3 will discuss top-level architecture choices. Section 4.4 will detail the implementation of each of the three modulators and Section 4.5 will cover layout. Finally, computer simulation results will be presented in Section 4.6.

4.2 Objectives

Many of the objectives in the design of the Sigma-Delta modulator mirror the objectives of the main-amplifier discussed in Chapter 3. For instance, the clock frequency, supply voltage, and resolution are all the same as the main-amplifier. This is because the modulator is designed to interface with the decimation filter proposed in [26], which is a 10-bit design. Also as in the case of the main-amplifier, power and silicon area are the main constraints and should be minimized as much as possible. The complete modulator specifications are shown in Table 4-1.

Table 4-1: Modulator specifications

Specification	Target
Clock Frequency	1MHz
Supply Voltage	900mV (Split rail +/- 450mV)
Technology	0.18µm CMOS
Signal Bandwidth	1KHz
Resolution	10-bit or greater
Power Consumption	Minimal
Silicon Area	Minimal

4.3 Modulator Architecture

When designing a Sigma-Delta modulator, the two most important characteristics are the order of the loop filter and the oversampling ratio. By using a higher order modulator, it is possible to achieve higher resolutions using lower oversampling ratios. However, the price of using high order filters is the added design complexity, silicon area, and the inherent instability of 3rd order and higher filters. 1st and 2nd order filters are inherently stable and relatively easy to design. Theoretical signal-to-noise ratios for Sigma-Delta modulators are well established and illustrated by Figure 4-1 below. In this case, the oversampling ratio of the modulator was based on global parameters of the biosensor system. The oversampling ratio is determined by Equation 4-1.

$$OSR = \frac{f_s}{2 \times f_{in}}$$

Equation 4-1: Oversampling ratio calculation

With a clock frequency of 1MHz and input frequency limited to 1kHz, the oversampling ratio of the modulator is 500. In order to determine the effective number of bits (ENOB) based on the signal-to-noise ratio of the modulator, Equation 4-2 is used.

$$ENOB = \frac{SNR - 1.76}{6.02}$$

Equation 4-2: ENOB Calculation

Based on the specification of 10-bit resolution, a signal-to-noise ratio of 61.96dB is needed. According to Figure 4-1, even a 1st order modulator with an oversampling ratio of 500 should be able to achieve this, however the figure is based on the ideal limits of the Sigma-Delta architecture and not real world designs. Non-idealities within the components of the modulator will always mean that the real signal-to-noise ratio for a given order and oversampling ratio will be lower than what is shown in the figure. For these reasons it is realistic to assume that a 2nd order or higher filter will be required to achieve 10-bit resolution at an oversampling ratio of 500.

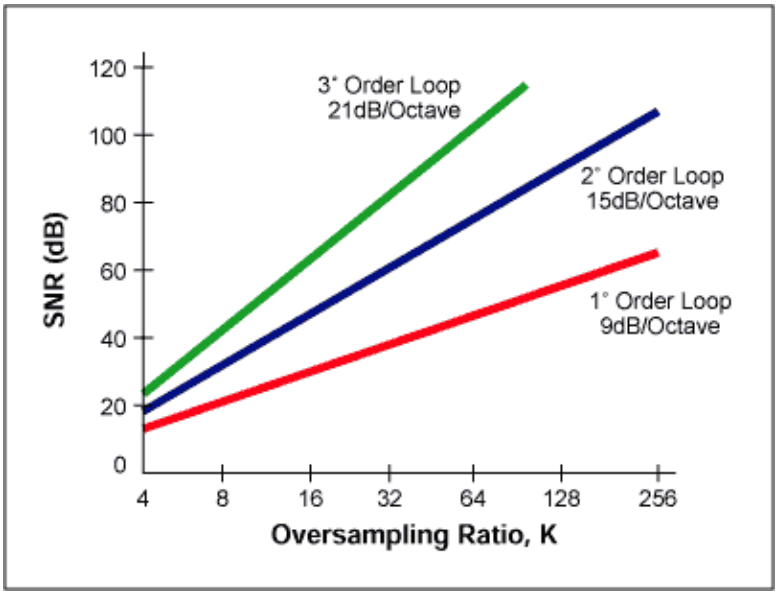

Figure 4-1: Comparison of modulator architectures [27]

4.4 Schematic Design

The three Sigma-Delta modulators proposed in this section will be referenced with the names A, B, and C. Modulators A and B are both 2nd order designs with Modulator A being the initial design and Modulator B being a second, revised version. Modulator C is based on the same design as A and B, but uses 3rd order architecture.

The overall schematic level diagram of the proposed 2nd order Sigma-Delta modulator is shown in Figure 4-2. The loop filter is implemented using two switched capacitor integrators, with digital feedback controlled by the modulator output. The proposed 3rd order modulator is uses the same architecture but simply has three integration stages instead of two. V_{ref_high} and V_{ref_low} are bias voltages which determine the maximum input voltage range of the modulator. These voltages are set to 625mV and 275mV respectively. This allows for a total input range of 300mV (300mV to 600mV) as well as providing and extra 25mV on each side to ensure stability.

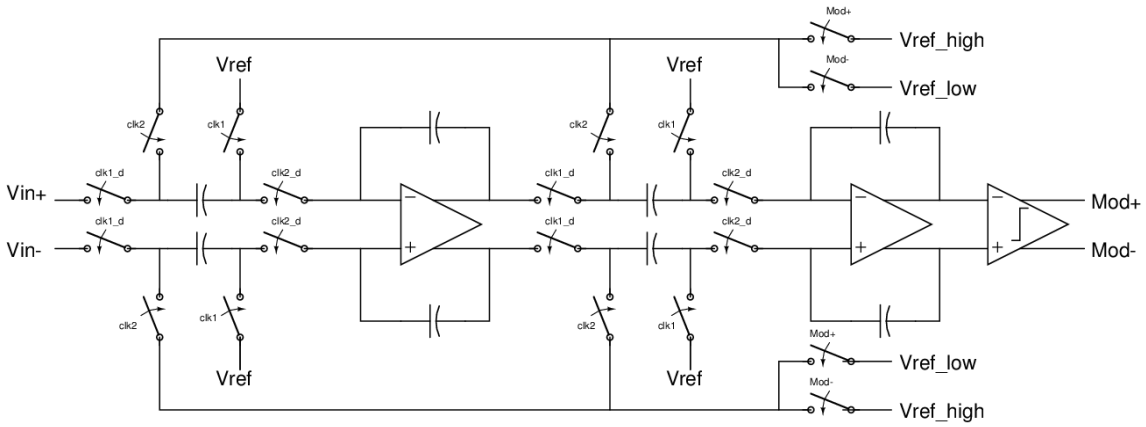

Figure 4-2: 2nd Order Sigma-Delta Modulator Schematic

Common mode feedback circuits are needed to account for common mode shifts between stages in the biosensor chip. Each op-amp in the modulator uses a hybrid switched

capacitor/continuous time common mode feedback system to accomplish this. The switched capacitor circuit described in Section 3.5 is also in the modulator to detect the output common mode of the op-amp, and this common mode signal is fed to the single stage op-amp shown in Figure 4-3. The op-amp used in the common mode feedback circuit is biased completely in the sub-threshold region and consumes just 72nW. Since the common mode feedback op-amp uses so little current it has very limited driving strength, resulting in a very smooth common mode feedback signal even though the switched capacitor detection circuit can produce a jittery output.

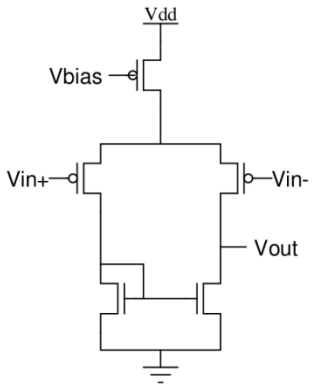

Figure 4-3: Common-mode feedback op-amp

Table 4-2 describes the capacitor sizes used throughout the proposed modulators. All capacitors sizes are multiples of 148.5fF, as this is the minimum size available in the silicon process. The ratio of feedback to input capacitor in each stage was chosen to maximize the stability of the modulator.

Table 4-2: Sigma-Delta modulator capacitor sizes

Capacitor	**Modulator A (2^{nd} Order)**	**Modulator B (2^{nd} Order)**	**Modulator C (3^{rd} Order)**
First Stage Input	148.5fF	594fF	594fF
First Stage Feedback	2.079pF	2.376fF	4.753pF
Second Stage Input	148.5fF	148.5fF	297fF
Second Stage Feedback	297fF	1.188pF	2.376pF
Third Stage Input	N/A	N/A	297fF
Third Stage Feedback	N/A	N/A	594fF
Total Capacitance	5.346pF	8.613pF	17.822pF

4.5 Layout

The layouts for modulators A, B, and C are shown below in Figure 4-4, Figure 4-5, and Figure 4-6 respectively. While modulator A performed well, it features an asymmetrical layout which is not idea for switched-capacitor systems. In moving to modulator B, the layout was switched to mirror that of the main-amplifier in Chapter 3. The op-amps and comparator are placed in the center of the layout allowing for symmetrical arrays of capacitors to be placed around the edges. Modulator C also follows this design technique. Modulators A, B, and C have dimensions of 288.62µm by 152.415µm, 191.25µm by 228.28µm, and 266.06µm by 296.66µm respectively.

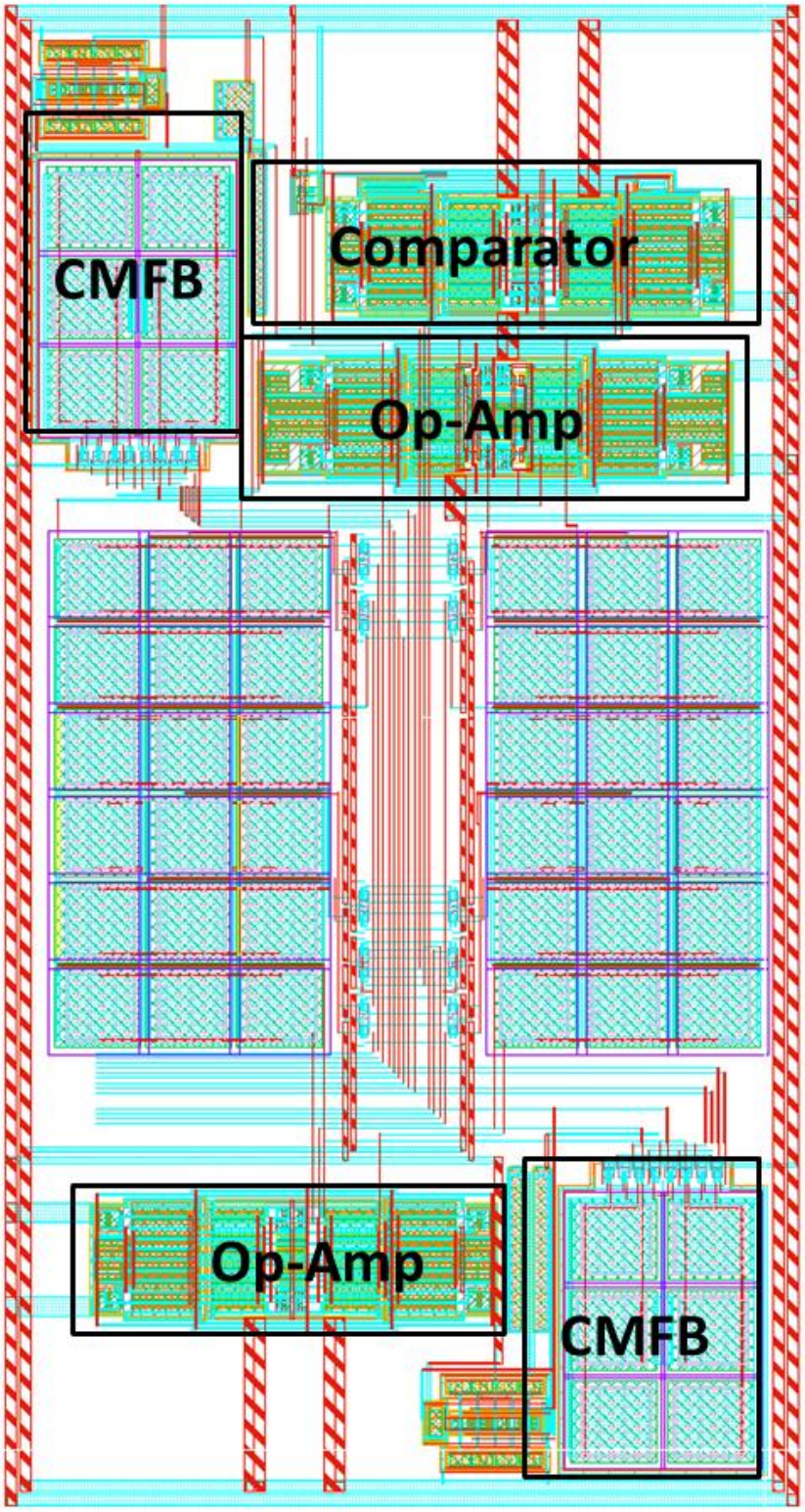

Figure 4-4: 2nd Order Modulator Revision A Layout

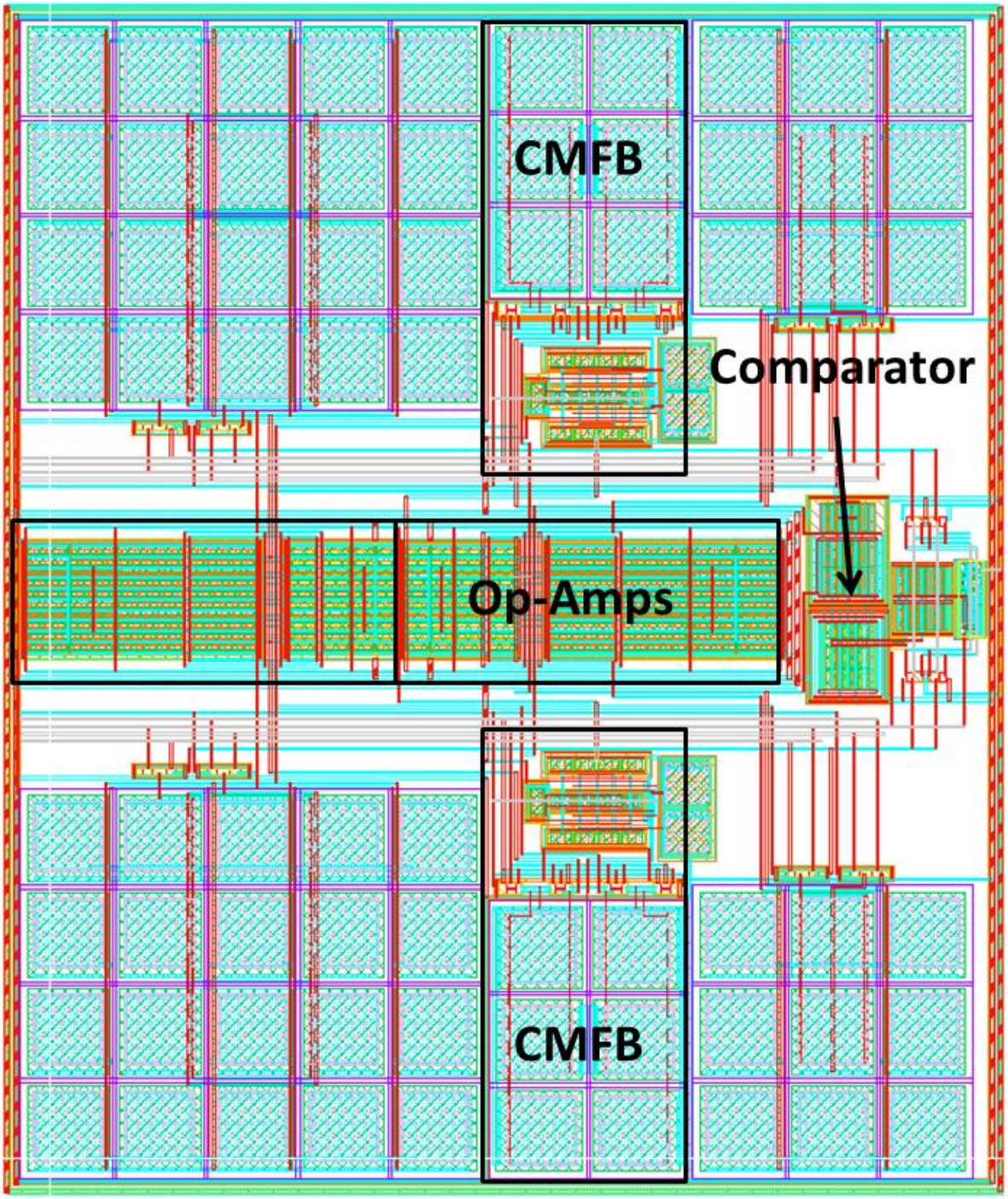

Figure 4-5: 2nd Order Modulator Revision B Layout

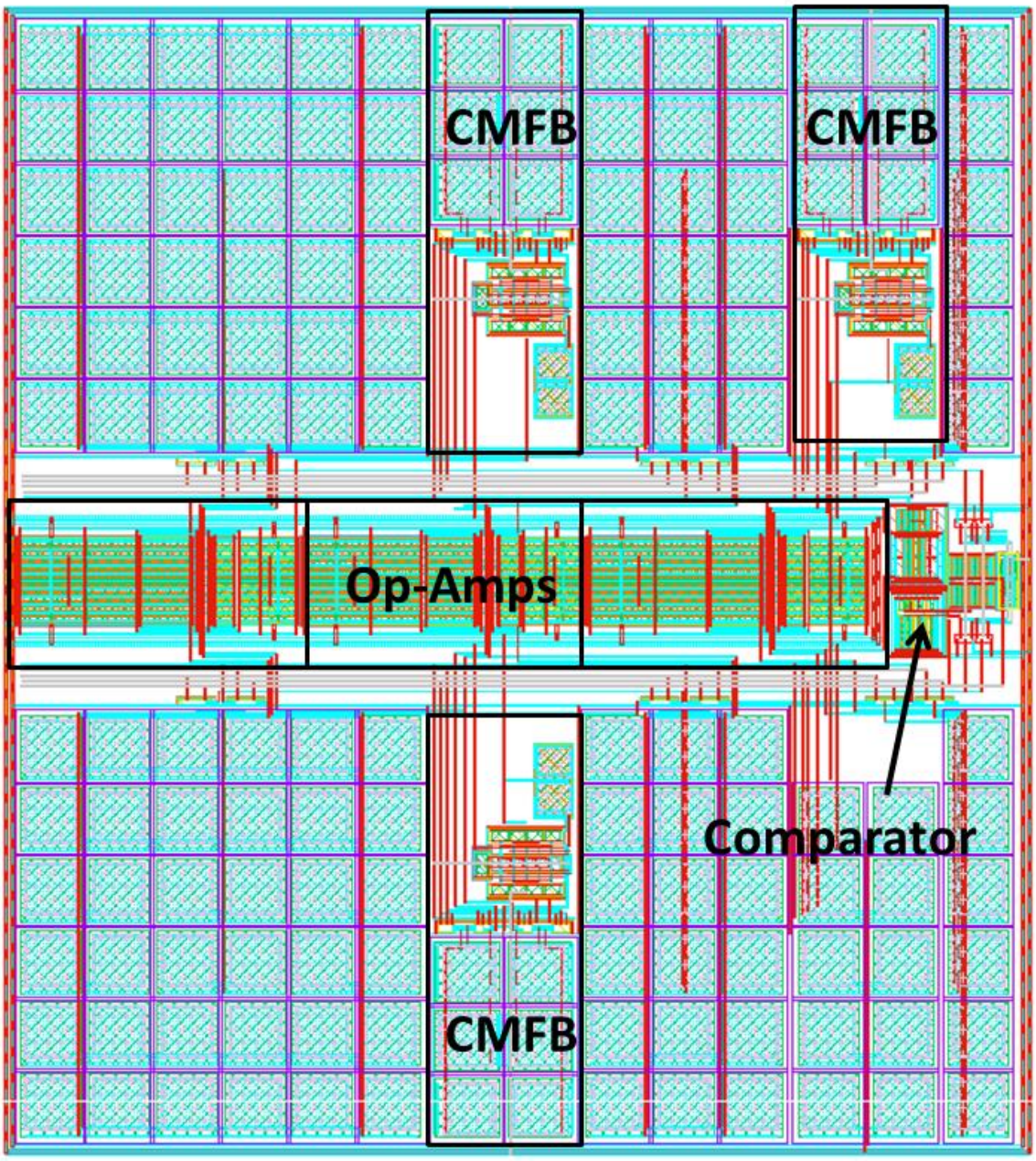

Figure 4-6: 3rd Order Modulator Layout

4.6 Simulation Results

Transient simulations for the 3rd order modulator (C) are shown in Figure 4-7 and Figure 4-8. Figure 4-9, Figure 4-10, and Figure 4-11 show the spectral output of modulators A, B, and C respectively. Using the spectral outputs for the three modulators their signal-to-noise ratios can

be computed using the Matlab code included in Appendix A. The 2nd order modulators, A and B, achieve signal-to-noise ratios of 77.9dB and 86.8dB respectively with a bandwidth of 2kHz. The 3rd order modulator achieves a signal-to-noise ratio of 88.59dB.

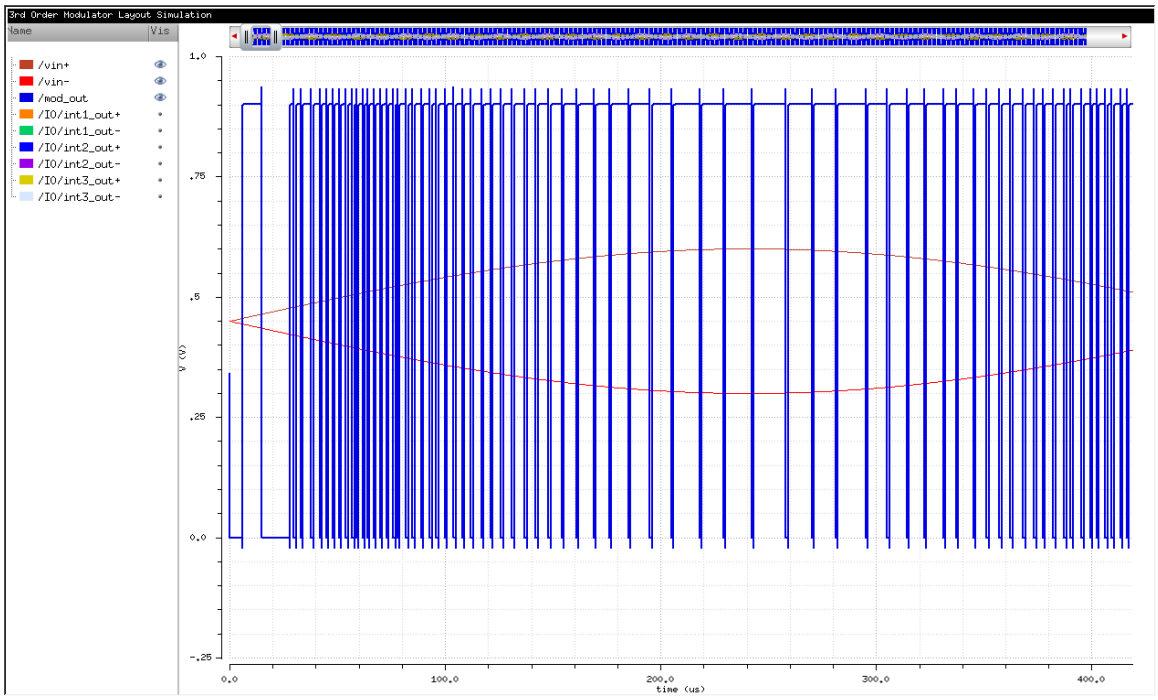

Figure 4-7: 3rd Order modulator output

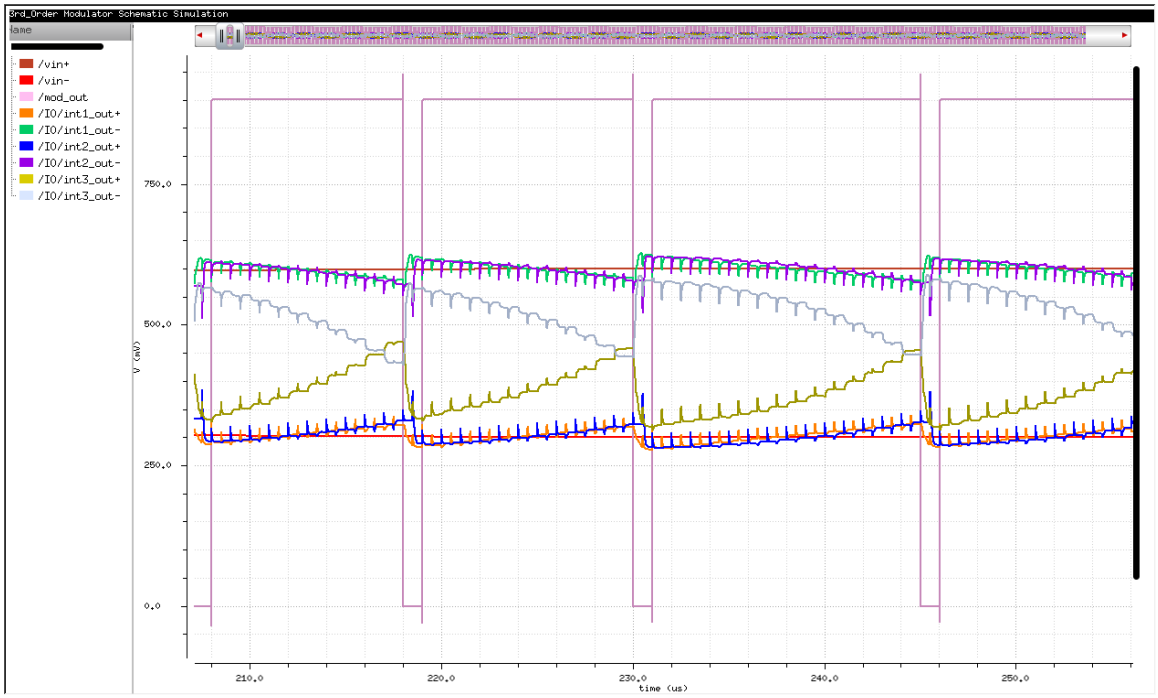

Figure 4-8: 3rd Order modulator output zoomed to show integrator outputs

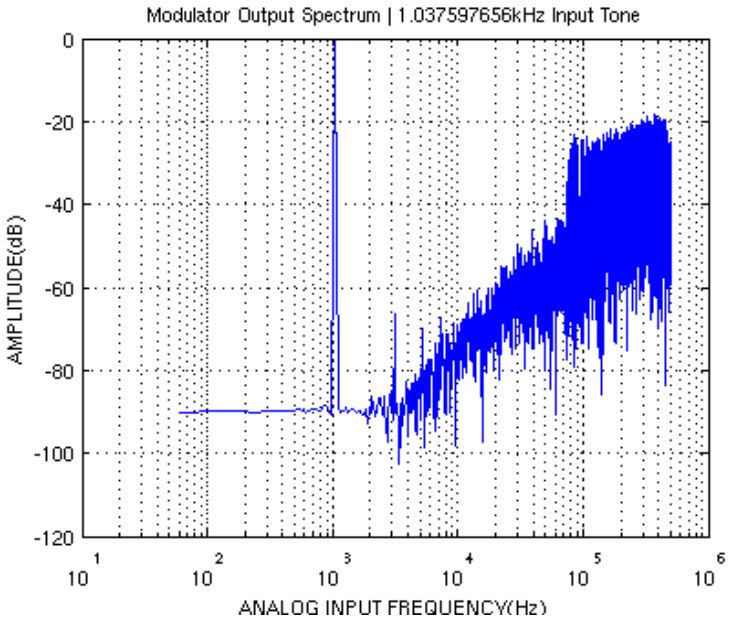

Figure 4-9: 2nd order modulator Revision A output spectrum

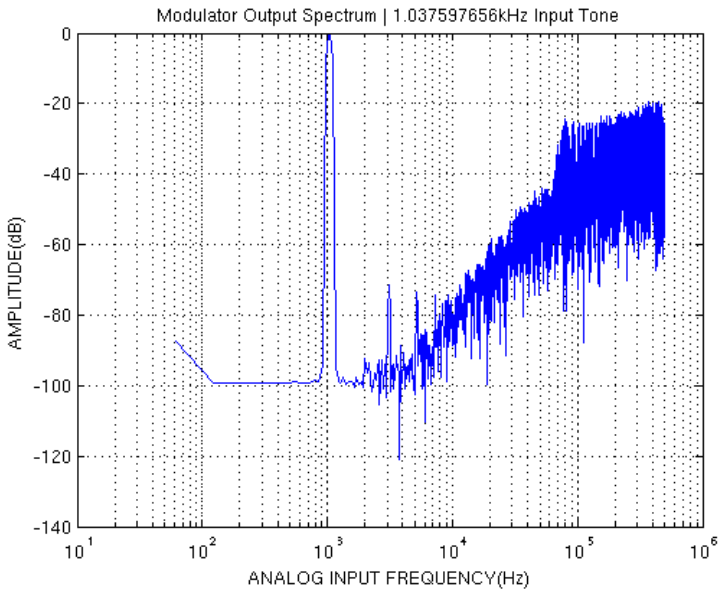

Figure 4-10: 2nd order modulator Revision B output spectrum

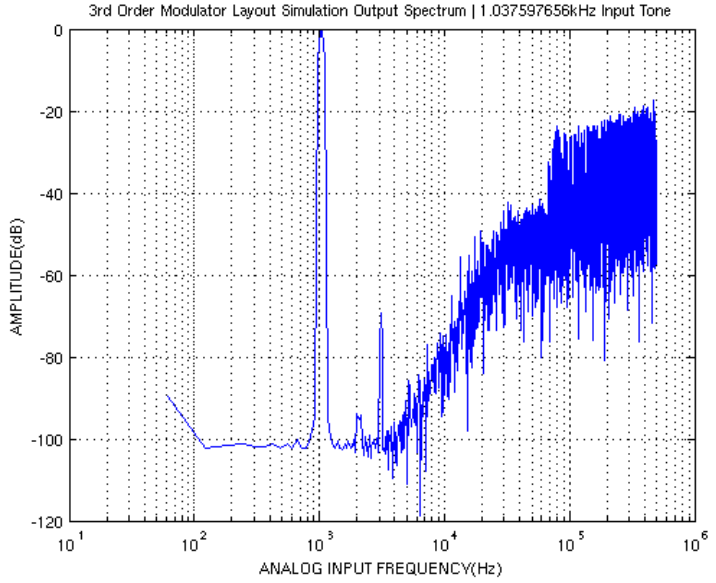

Figure 4-11: 3rd order modulator output spectrum

In order to easily compare the efficiency of different designs a figure of merit is necessary. The most widely used figure of merit to describe Sigma-Delta modulators is the Walden figure of merit which is shown in Equation 4-3.

$$FOM = \frac{P}{2^{ENOB_{SNR}} \times 2 \times BW}$$

Equation 4-3: Walden Sigma-Delta modulator figure of merit

The three proposed modulators are compared against many other designs in Table 4-3. The 2nd order modulator improved dramatically between versions A and B, with the figure of merit increasing by an order of magnitude from 762fJ/bit to 71fJ/bit. While the 3rd order modulator (C) achieves a slightly better signal-to-noise ratio than the 2nd order modulators, the extra power and area required for adding a third integrator make it much less efficient overall. Compared to other designs, Revision B of the 2nd order modulator is by far the most efficient 2nd order design, although it is bested in several cases by much more complicated 3rd and 4th order modulators.

Table 4-3: Sigma-Delta modulator design comparisons

Design	Order	SNR	BW	Power	Area mm^2	FOM fJ/bit
2nd Order Rev. A	2nd	77.9dB	2kHz	10.22µW	0.031	762
2nd Order Rev. B	2nd	86.8dB	2kHz	9.1µW	0.043	71
3rd Order	3rd	88.59dB	2kHz	10.99µW	0.067	125
[11]	2nd	68.6dB	10kHz	60µW	0.31	1130
[12]	3rd	81dB	20kHz	36µW	0.715	98
[28]	4th	76.4dB	36MHz	15mW	0.12	38.8
[29]	3rd	69dB	25MHz	8.5mW	0.23	88
[30]	5th	74.3dB	1.95MHz	8.55mW	2.72	520
[13]	3rd	84dB	100kHz	140µW	0.492	54
[31]	3rd	76dB	100kHz	4mW	0.7	3879
[32]	3rd	98dB	20kHz	2.6mW	No Silicon	991
[14]	3rd	61dB	10kHz	7.5µW	0.3375	289

Based on the simulation results, Revision B of the 2nd order modulator is the best choice for integration into the silicon biosensor. It consumes less power than either of the other

proposed designs, is the most efficient, and easily achieves the required 10-bit resolution needed by the decimation filter proposed in [26]. While the 3rd order modulator can achieve a better signal-to-noise ratio, it uses more power and takes up more area, making it a poor choice.

Chapter 5: Silicon Testing Results

5.1 Introduction

Silicon testing results for all the circuits proposed here are very promising. In this chapter, the silicon test results for each circuit will be presented. Section 5.2 discusses the physical testing station as well as limitations of the test methodology. Section 5.3 will present the test results of the main-amplifier, while Section 5.4 will discuss Revision A of the 2nd order Sigma-Delta modulator. Section 5.4 discusses the test results of the proposed 3rd order Sigma-Delta modulator, and finally section 5.5 details the performance of the main-amplifier and second generation 2nd order Sigma-Delta modulator connected together as part of the overall signal chain. Finally, Section 5.6 summarizes the test results,

5.2 Testing Setup and Microchip Size Comparisons

Two different microchips containing circuits proposed here were tested. The first microchip, shown on the far right in Figure 5-1, contained Revision A of the 2nd order Sigma-Delta modulator. This microchip uses a 40 pin package and was tested using the socket shown in Figure 5-3. The second microchip, shown in the center of Figure 5-1 contains the main-amplifier, 3rd order Sigma-Delta modulator, and a connected signal chain which includes a transimpedance amplifier, main-amplifier, and 2nd order modulator Revision B. The second microchip uses a 64 pin package and was tested using the socket shown in Figure 5-2.

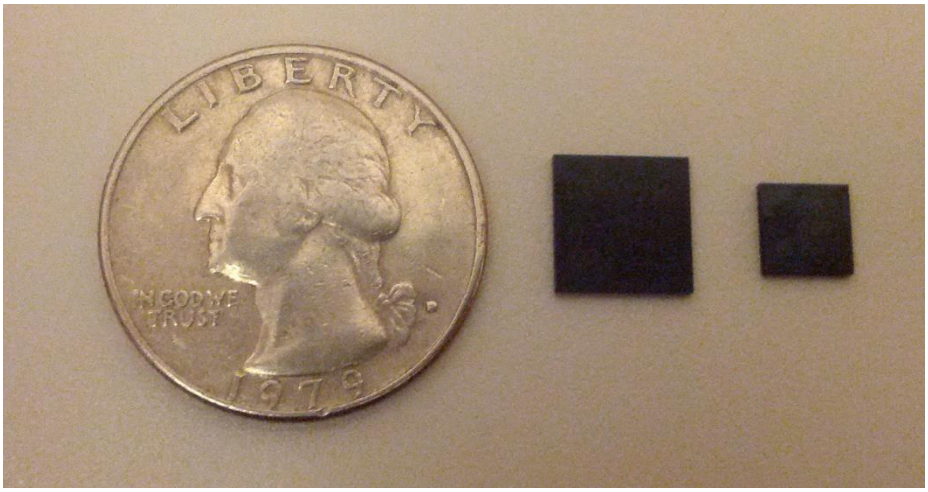

Figure 5-1: Microchip size comparison

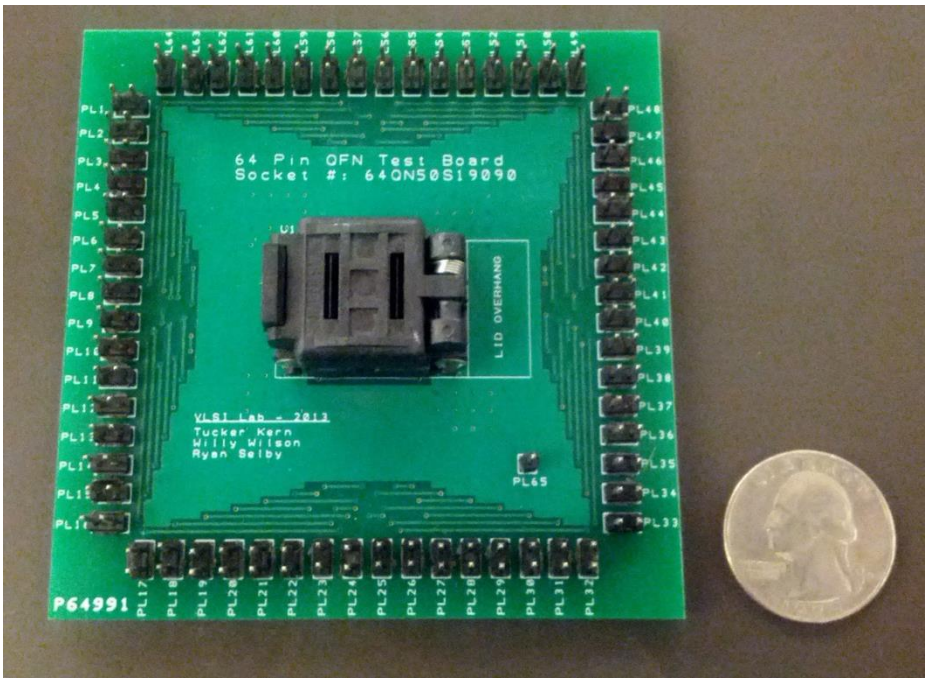

Figure 5-2: 64 pin test socket with coin for size comparison

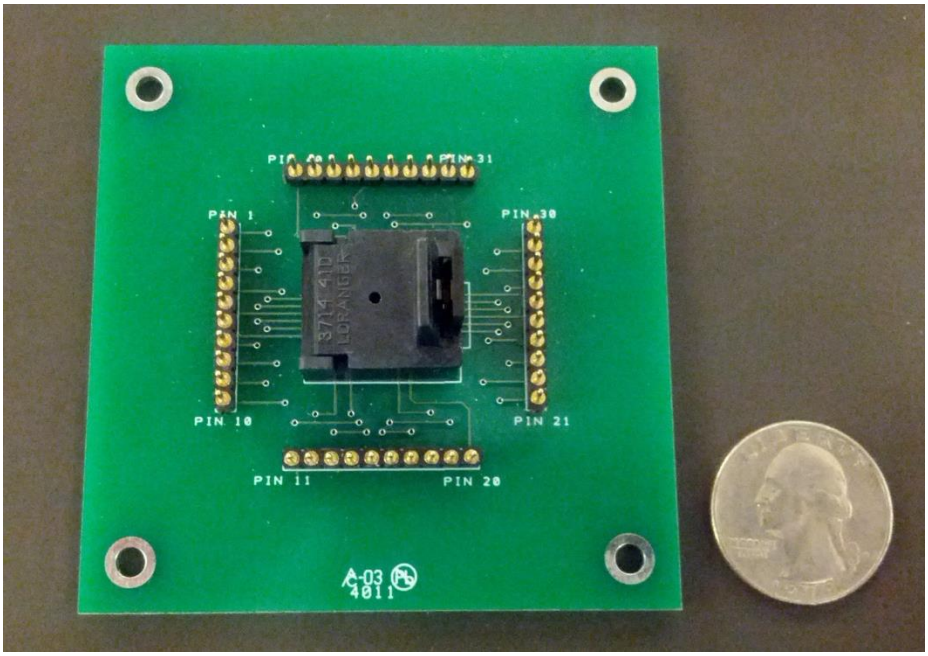

Figure 5-3: 40 pin test socket with coin for size comparison

The testing station is shown below in Figure 5-4. Multiple power supplies and function generators are used to supply power and input signals to the microchips while a digital oscilloscope is used to capture data output.

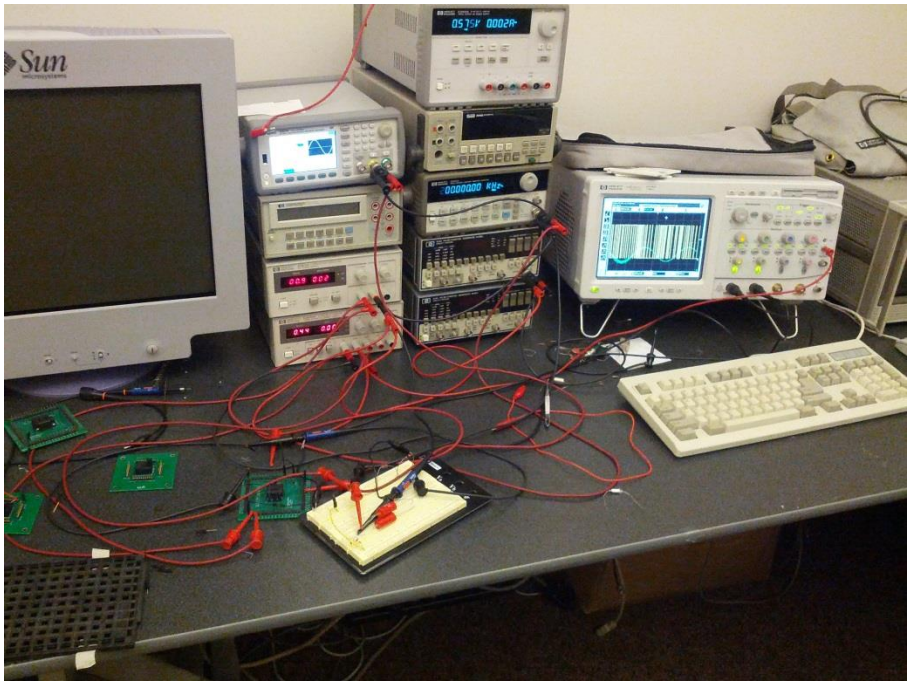

Figure 5-4: Testing bench

The main limitation of the testing station is the inability to produce fully differential input signals for use as inputs to the test circuits. In order to produce fully differential input signals, two function generators are linked together and their outputs are synced based on a common signal. The function generators currently available for testing do not function properly when synced and so fully differential inputs could not be used. For this reason single ended inputs were used for all silicon testing. Except for several isolated cases related to the Sigma-Delta modulator this had no impact on the determining the functionality of the test circuits.

5.3 Main-Amplifier

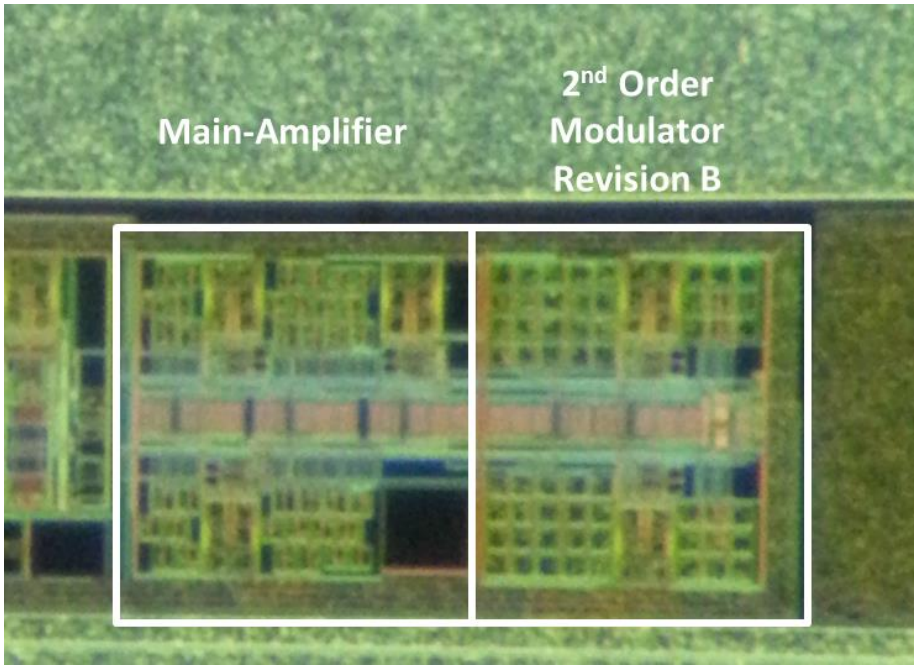

Figure 5-5: Signal-chain die photo

A die photo of the signal chain, which contains both the main-amplifier and 2nd order modulator Revision B is shown in Figure 5-5. A typical oscilloscope screen capture of the main-amplifier is shown below in Figure 5-6. Because fully differential input signals could not be generated, the positive input of the main amplifier was driven with a 6mV peak-to-peak 1kHz

input signal while the negative input was held at the common-mode voltage. For this test the clock frequency was set at 1MHz. In Figure 5-6 the purple trace is the input signal, while the green and yellow traces represent the positive and negative outputs respectively.

Figure 5-5 clearly shows that the main-amplifier performs as expected with a gain of approximately 100V/V (40dB) with the desired input and clock frequencies. The biggest challenge in determining the precise performance of the main-amplifier is the amount of noise generated by the testing station. The function generators used to provide the input for this test were not designed to produce small AC waveforms only a few millivolts in amplitude and the noise can easily be seen on the input signal.

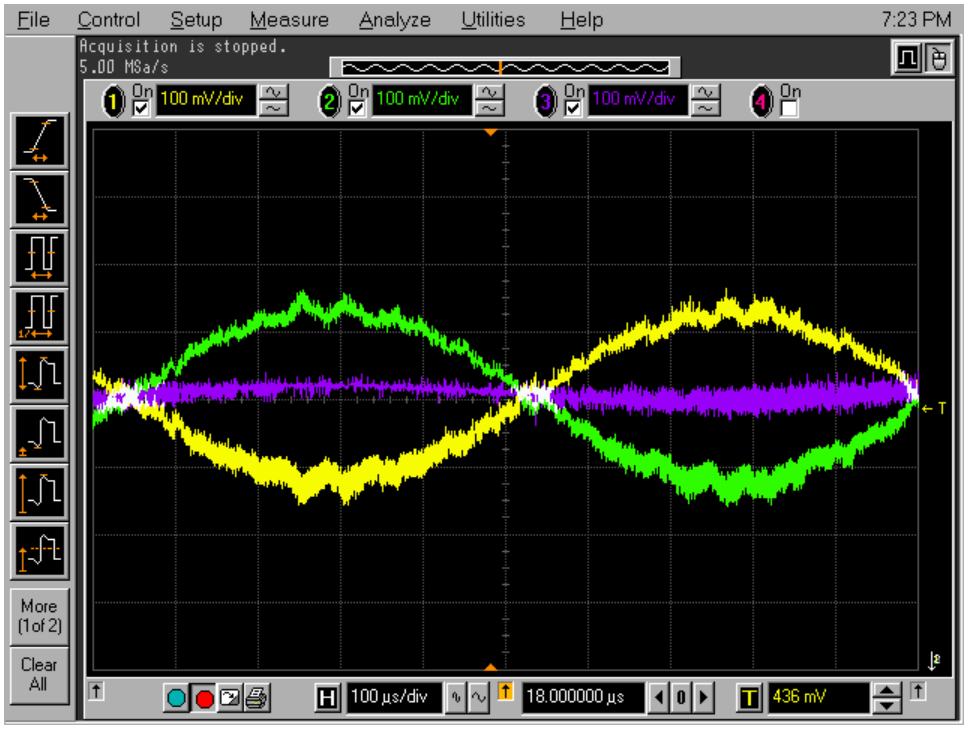

Figure 5-6: Main-amplifier output with 1 MHz clock.

While the great majority of the main-amplifiers tested performed well, several performed abnormally or simply did not work at all. One example of the main-amplifier performing

abnormally can be seen in Figure 5-7. In this case, the amplifier performs perfectly when the output voltage is less than 460mV, however above that the output clips. Analysis of the common-mode feedback voltages in these cases showed the amplifier to be performing normally, and so these results are puzzling. While it can't be definitively proven, the cause of this problem is believed to be the switching circuitry that multiplexes the main-amplifier output to the pins of the microchip.

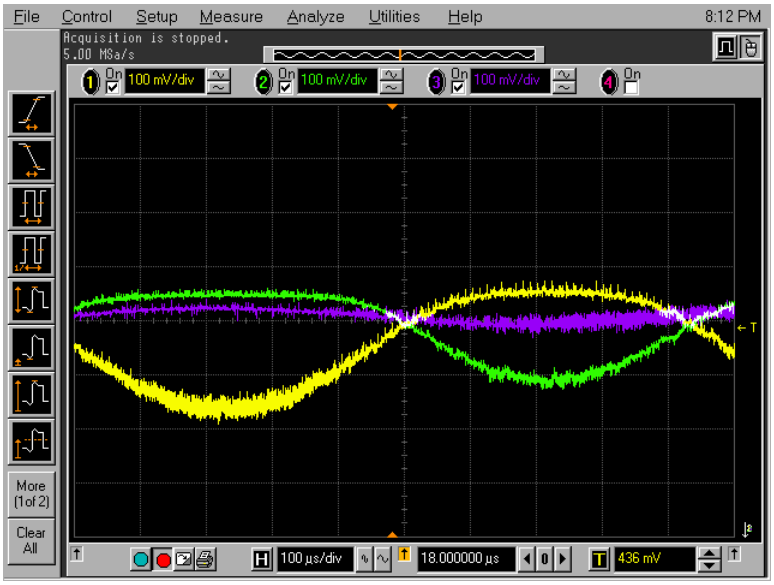

Figure 5-7: Main-amplifier output clipping due to low switch voltage

In other cases the main amplifier simply didn't function at all, as is shown in Figure 5-8. In these cases analysis of the common-mode feedback voltages showed abnormalities within the main-amplifier itself.

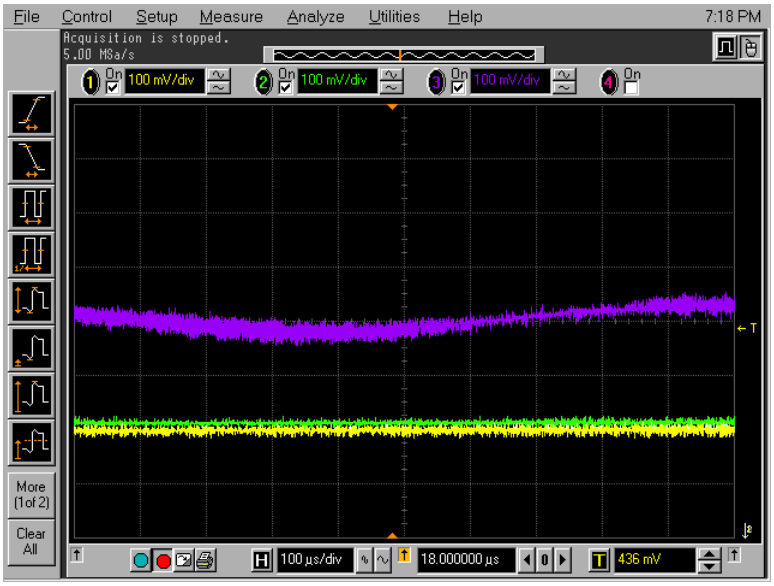

Figure 5-8: Non-functioning main-amplifier

The main-amplifier was tested in 50 microchips in order to determine the approximate yield of the circuit. The chips were separated into three categories based on if the chip was function, if it was non-functional, or if it worked but exhibited clipping behavior as shown in Figure 5-7. The results are summarized in Table 5-1.

Table 5-1: Main-Amplifier testing results

Test Result	Quantity (out of 50)
Functional	34
Clipping	6
Non-Functional	10

Overall these testing results are promising. If the yield calculation counts the main-amplifiers that clip as non-functional, then the overall yield is 68%. If the clipping is in fact caused by the multiplexing circuitry within the microchip and not the main-amplifier itself then the clipping amplifiers can be counted as functional, and the overall yield jumps to 80%, which is very good for a first generation design.

5.4 Revision A 2nd-Order Sigma-Delta Modulator

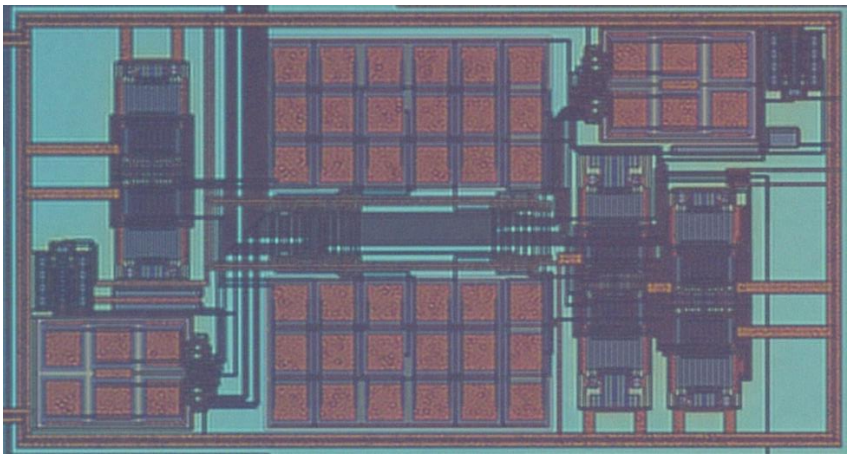

Figure 5-9: 2nd Order Sigma-Delta Modulator Die Photo

The die photo for Revision A of the 2nd order Sigma-Delta modulator is shown above in Figure 5-9, while a typical oscilloscope capture of testing the modulator is shown below in Figure 5-10. As in the testing of the main amplifier, a single ended input had to be used for the test. The positive input to the modulator was driven by a 1kHz, 600mV peak-to-peak signal while the other input was held at the common-mode voltage. In Figure 5-10, the green trace is the analog input signal while the yellow trace is the modulator's digital output. As is shown in the figure, when the input signal goes below the common-mode voltage, more zeroes occur at the output, and when the input goes above the common-mode voltage more ones occur. This is exactly the behavior that was expected based on the computer simulations of the modulator.

While the modulator performs very well at low clock speeds, it quickly became apparent that it was not able to run at its intended clock speed of 1MHz. Upon further testing and examination of the microchip layout, it was determined that the modulator output was not buffered as it should have been. The output of the modulator is a flip-flop with very low driving strength, and the pad and oscilloscope probe present a large capacitive load that it is unable to

drive at 1MHz. Figure 5-11 through Figure 5-14 below show a close-up view of the modulator output with varying clock frequencies from 100kHz to 1MHz.

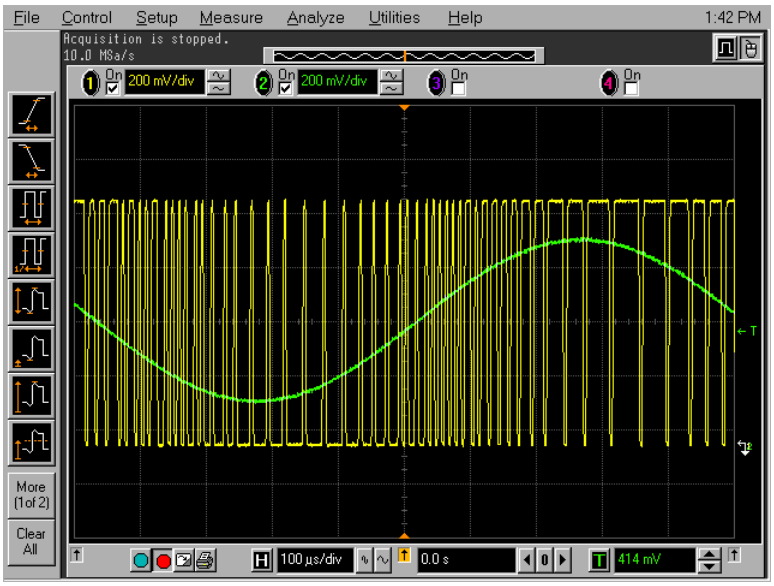

Figure 5-10: 2nd order modulator output with 200kHz clock

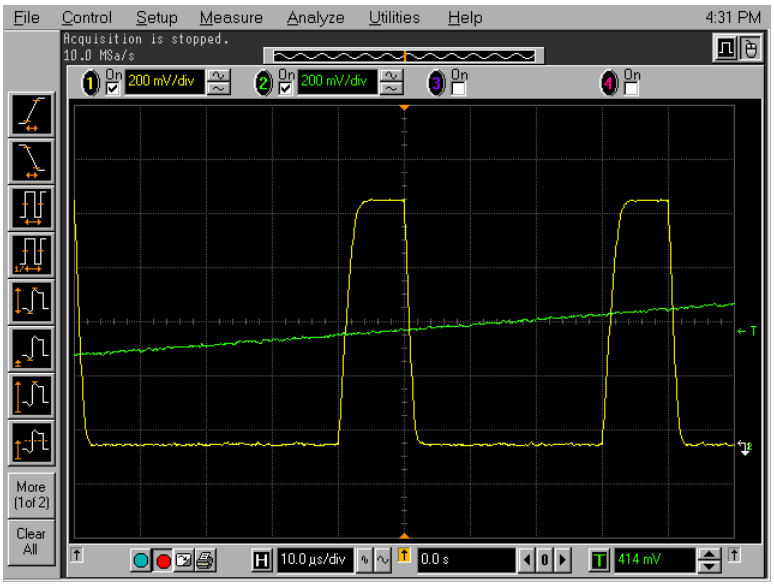

Figure 5-11: Modulator output with 100 kHz clock

Figure 5-12: Modulator output with 200 kHz clock

Figure 5-13: Modulator output with 300 kHz clock

Figure 5-14: Modulator output with 1 MHz clock

As with the main-amplifier, 50 modulators were tested to determine an approximate yield. While none of the modulator performed at the desired clock frequency of 1MHz, this wasn't a failure of the modulator itself but rather of the connection between the modulator at the pad. None of the modulators exhibited strange behavior, and so the results were grouped into two bins, either functional or non-functional. The results are shown in Table 5-2.

Table 5-2: Revision A 2nd Order Sigma-Delta Modulator Test Results

Test Result	Number (out of 50)
Functional	48
Non-Functional	2

Based on the test results the Revision A 2nd order Sigma-Delta modulator achieved a yield of 96%, which shows that the design of the modulator itself is very robust. This is not surprising given the nature of Sigma-Delta architectures, but it is still very promising. In the two cases where the modulator did not work, the entire microchip failed, not just the modulator. This indicates that these two cases were perhaps an issue with the packaging of the microchip, and not necessarily the modulator itself.

5.5 3rd Order Sigma-Delta Modulator

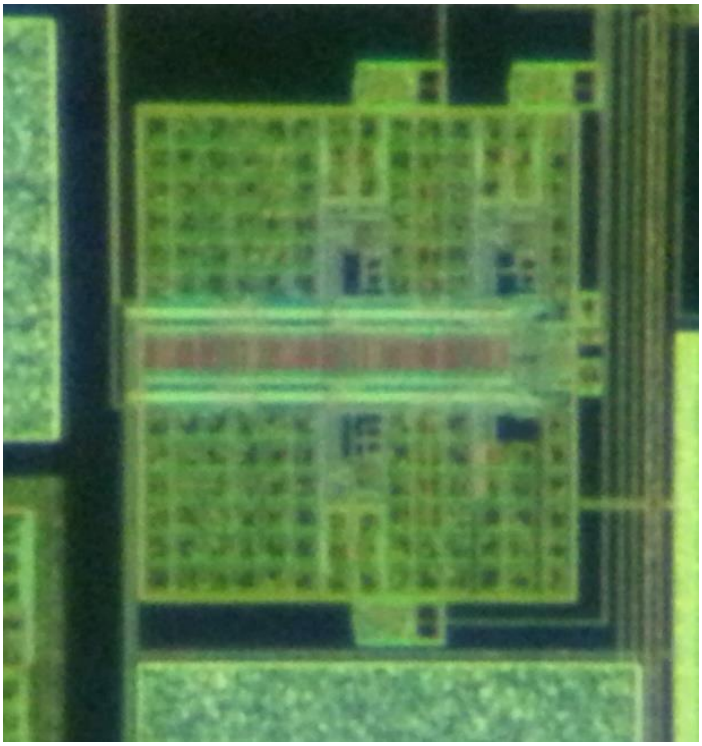

Figure 5-15: 3rd order modulator die photo

A die photo of the 3rd order Sigma-Delta modulator is shown in Figure 5-15. The testing setup for the 3rd order Sigma-Delta modulator is identical to the 2nd order Sigma-Delta modulator described in the previous section. The positive input was driven with a 600mV peak-to-peak signal while the negative input was held at common-mode. A typical screen capture of the testing of the 3rd order Sigma-Delta modulator is shown below in Figure 5-16. In this figure the yellow trace represents the analog input signal while the green trace is the modulator's digital output voltage.

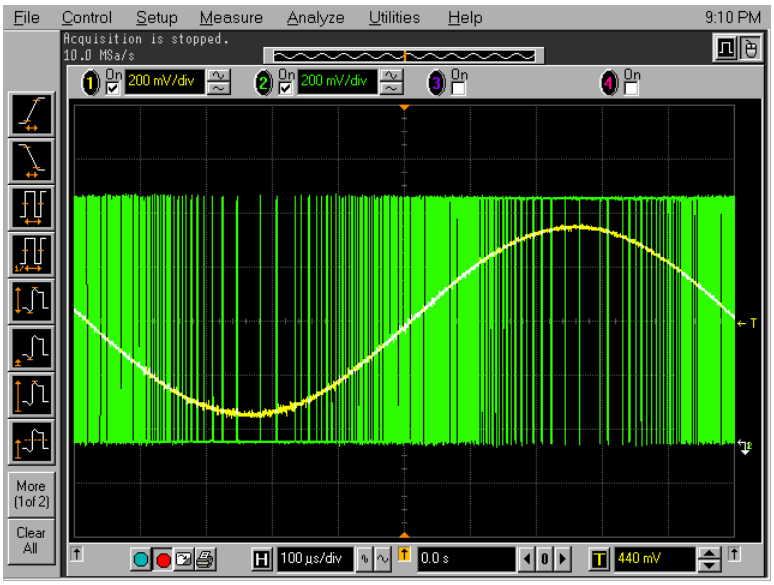

Figure 5-16: 3rd order modulator output with 1 MHz clock

Unlike the 2nd order modulator in the previous section, the 3rd order modulator was properly buffered and had no problems running at its intended clock frequency of 1MHz. Once again, the modulator functions as designed, displaying more zeroes at the output when the input signal is below the common-mode voltage, and more ones when the input signal is above the common-mode voltage.

Unfortunately, while most of the third order modulators functioned perfectly, several behaved abnormally. One example of this is shown below in Figure 5-17. In this case, the modulator performs perfectly when the input signal is less than the common-mode voltage, however as the input signal rises the modulator never outputs as many ones as it should. This problem could be caused by the use of single ended input signal. Using a fully differential input signal, the input voltage should never exceed 600mV, however using a single ended input the input voltage must reach 750mV. Since the modulator was never designed for this type of input, the input switches may not let signal properly charge the input capacitors of the modulator's first stage, causing a clipping issue as was seen in the main-amplifier.

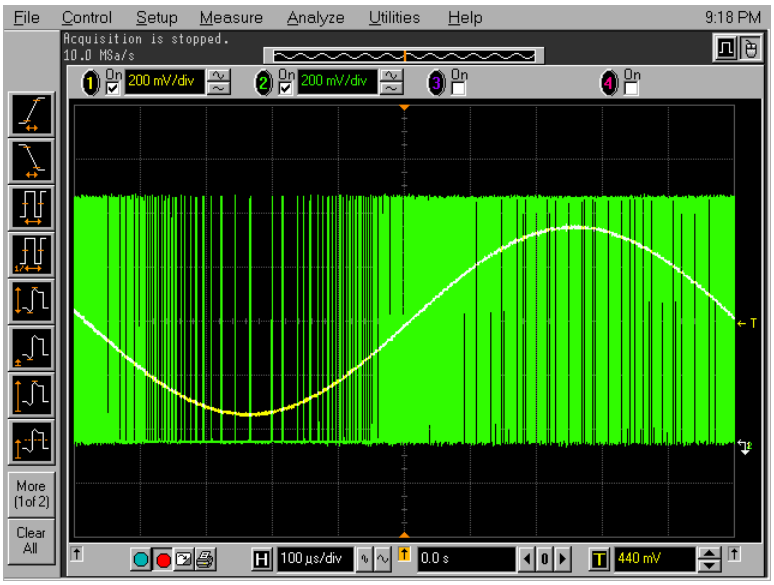

Figure 5-17: 3rd order modulator output clipping due to low switch voltage

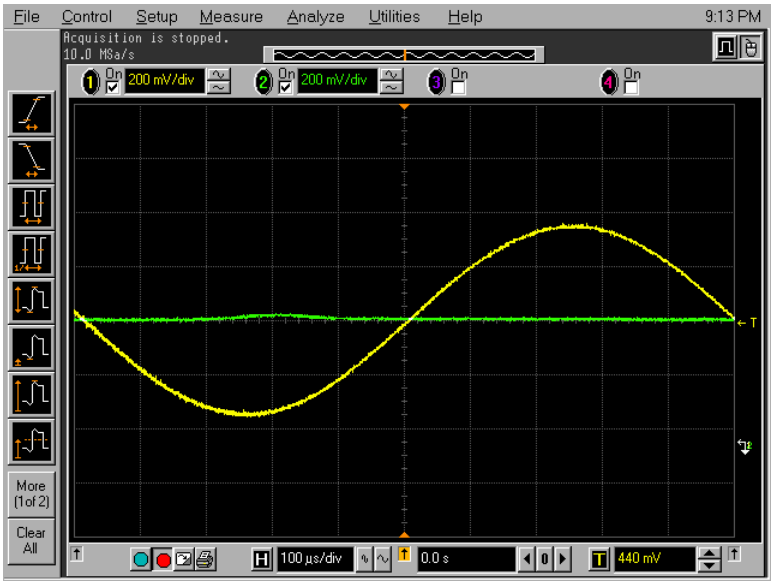

Figure 5-18: Non-functioning 3rd order modulator

Besides the modulators which exhibited clipping behavior, some simply didn't function at all. An example of this is shown in Figure 5-18 where the modulator's output is fixed at the common-mode voltage. Overall, however, the test results for the 3rd order modulator were very good. As in the case of the 2nd order modulator in Section 5.3 the test results have been separated

into three bins: functional, non-functional, and those that exhibit clipping. Once again 50 3rd order modulators were tested. The results are presented in Table 5-3 below:

Table 5-3: 3rd Order Sigma-Delta Modulator Test Results

Test Result	Number (out of 50)
Functional	22
Non-Functional	10
Clipping	18

If the modulators which exhibit clipping are counted as non-functional then the total yield for the 3rd order modulator is only 44%, however if the clipping is indeed caused by the use of a single ended input signal then the total yield increases to 80%, the same as the main-amplifier.

5.6 Main-Amplifier and Revision B 2nd Order Sigma-Delta Modulator Signal Chain

A die photo of the signal chain can be seen in Figure 5-5. The signal chain tested in this section contains all of the necessary block for the integrated biosensor system including a transimpedance amplifier, the proposed main-amplifier, and Revision B of the 2nd order Sigma-Delta modulator. Computer simulations of the transimpedance amplifier showed that it may not work correctly, and so the inputs to the main-amplifier in the signal chain were multiplexed with both the transimpedance amplifier outputs and external pads. Since the transimpedance amplifier is not a subject of this work only the external inputs were used for testing here.

The test setup for this circuit was exactly the same as what was used for testing the main-amplifier alone in section 5.3. Once again the positive input of the main-amplifier was driven with a 1 kHz, 6mV peak-to-peak input signal while the negative input was held at the common-

mode voltage. The clock frequency used was once again 1MHz. A typical oscilloscope screen capture for this test is shown in Figure 5-19.

Figure 5-19: Main-amplifier and 2nd order modulator signal chain with 1MHz clock

This screen capture shows the signal chain working as intended. As the input signal increases more ones are seen at the modulator output, and as it decreases more zeroes are seen at the output. Unfortunately there were not enough pins on the microchip package to monitor the output of the main-amplifier within the signal chain, and so the output from the main-amplifier can only be inferred by the output of the modulator. Figure 5-20 simply shows a close-up view of the modulator output, exhibiting good rise and fall times of the digital signal.

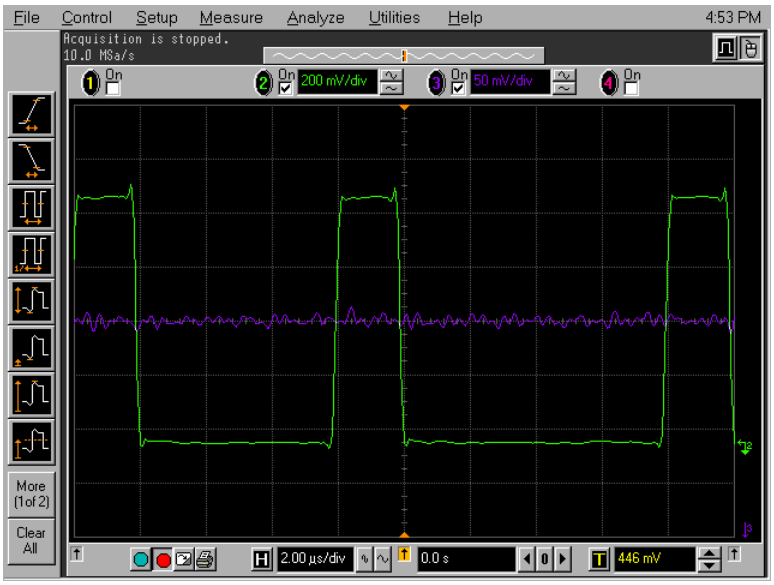

Figure 5-20: Signal chain output with 1MHz clock

Test results for the signal chain were very good, however there were some instances that did not work properly. Figure 5-21 shows one example of the signal chain performing abnormally. In this case, the output of the modulator oscillates between 250mV and 900mV regardless of the input. Figure 5-22 shows another instance of the signal chain in which the modulator output was constant at approximately 250mV.

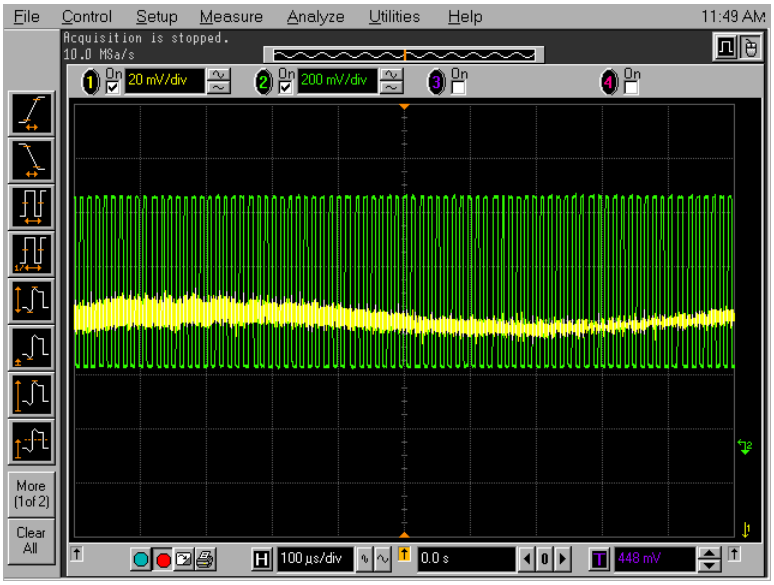

Figure 5-21: Signal chain with oscillating output

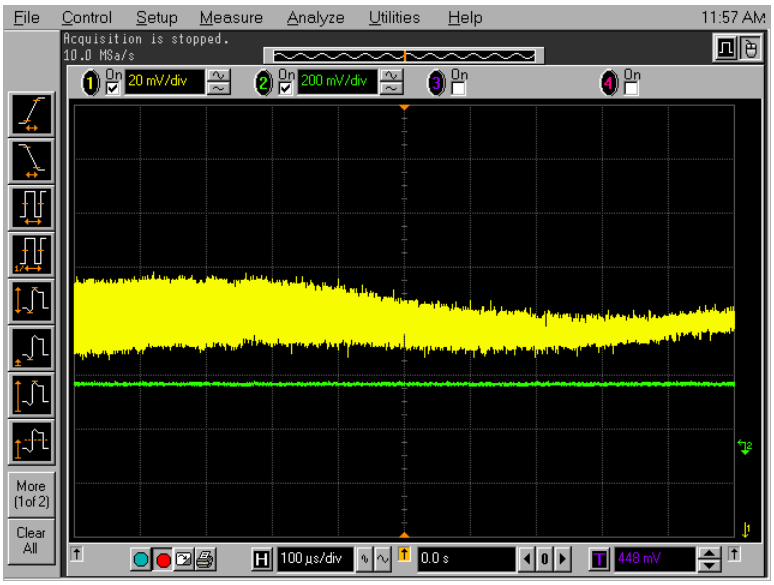

Figure 5-22: Non-functioning signal chain

Overall testing results of the signal chain were very good. None of the instances exhibited any of the clipping behavior seen with the 3rd order modulator or the main-amplifier. For this reason the testing results were placed into just two bins, either functional or non-functional. The results are summarized in Table 5-4.

Table 5-4: Signal chain test results

Test Result	Number (out of 50)
Functional	41
Non-Functional	9

These test results reveal an overall yield for the signal chain of 82% which is in line with the yield results for both the main-amplifier and 3rd order Sigma-Delta modulator.

5.7 Silicon Testing Conclusions

The overall silicon test results for the 4 circuits show great promise. Table 5-5 summarizes the yields for all four test circuits.

Table 5-5: Overall yield estimates

Circuit	Yield Estimate
Main-Amplifier	80%
Revision A 2nd Order Sigma-Delta Modulator	96%
3rd Order Sigma-Delta Modulator	80%
Main-Amplifier and Revision B 2nd Order Sigma-Delta Modulator	82%

It is interesting to note, and perhaps not surprising that the yields of the main-amplifier, 3rd order modulator, and the signal chain are all roughly 80% since all of these circuits were located on the same silicon die. What is surprising is that functioning and non-functioning circuits were consistent across multiple chips. The nine microchips tested which had non-functioning signal chains also had non-functioning main-amplifiers and 3rd order modulators. This suggests that at least across those nine microchips, something went wrong globally within the chip, or something went wrong when the die was attached to the package.

If we adjust for the behavior of these nine microchips and assume that the failure occurred globally and not within the test circuits themselves then the yield estimates for the test circuits increase to almost 100%. In the future more testing should be performed on the global chip layout at well as the package housing the microchip to try and determine what is causing these failures.

Chapter 6: Conclusions and Future Work

In order to increase our knowledge of biology and medicine, high tech advances in biological monitoring are needed. Integrated silicon biosensors provide one route in which individual cellular reactions can be observed in both the spatial and temporal domains. Silicon biosensors will require low-power, highly accurate, and physically small electrical components. While a silicon biosensor requires many components, voltage amplifiers and analog-to-digital converters are two of the most important when attempting to measure small biological signals. The circuits proposed here fill the required role and in many cases were able to exceed the design specifications. Table 6-1 and Table 6-2 compare the design requirements and the results achieved for the main-amplifier and version B of the Sigma-Delta modulator respectively.

Table 6-1: Main-amplifier specifications and results

Specification	**Desired Value**	**Value Achieved**
Gain	100V/V	100V/V
Bandwidth	1kHz	>1kHz
Resolution (THD)	10-bit	10.29-bit
Input Referred Noise	>10μV	59.2μV
Power	Minimal	6.82μW
Silicon Area	Minimal	0.076mm^2

Table 6-2: 2nd order Sigma-Delta modulator specifications and results

Specification	Desired Value	Value Achieved
Bandwidth	1kHz	2kHz
Resolution (SNR)	10-bit	14.13-bit
Power	Minimal	9.16µW
Silicon Area	Minimal	0.0437mm^2

Between the two proposed circuits, the main-amplifier input referred noise was the only specification which was not met. Together, the main-amplifier and modulator use just 15.98µW from a 900mV supply and occupy 0.1197mm^2,

The majority of future work on this project needs to focus on the integration of the proposed circuits into a fully featured biosensor. While effective electrode geometries have been presented in [1], and a working potentiostat was proposed in [2], these have yet to be fully integrated with the main-amplifier and analog-to-digital converter proposed here. The transimpedance amplifier needed to convert the electrochemical current to a voltage is also incomplete at this point. With the addition of these circuits hopefully the full integrated biosensor can be completed in the future.

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Appendix A: Matlab Code for

Calculating Signal-to-Noise Ratio

```
function [snr] = snr_calc( mod_out )
%-----------------------------------------------%
%%matlab code to calculate SNR,SNDR,THD SFDR
%%date : 7 May 2013
%%rev : 1
%-----------------------------------------------%
fclk = 0.5e+6;
numpt = 16384;
numbit = 1;
N = numpt;

no_window = 1;
hanning_window = 0;
ds_hann_window = 0;
hamming_window = 0;

span = 5;
noise_int_freq = 69;


mod_out_converted = mod_out;

%for j = 1:length(mod_out_converted),
%    if mod_out_converted(j,1) < 0.45
%        mod_out_converted(j,1) = -1;
%    else
%        mod_out_converted(j,1) = 1;untitled.png
%    end
%end

Dout = mod_out_converted;
code = Dout;

if no_window > 0
   Doutw = Dout;
elseif hanning_window > 0
```

```
   Doutw = Dout.*hanning(numpt);
elseif ds_hann_window > 0
   Doutw = Dout.*rot90(ds_hann(numpt));
elseif hamming_window > 0
   Doutw = Dout.*hamming(numpt);
else
   Doutw = Dout;
end

%performing FFT
Dout_spect=fft(Doutw,numpt);
%recalculate to dBuntitled.png
Dout_dB=20*log10(abs(Dout_spect));
%plot([1:N/2],Dout_dB(1:N/2));
%display the results in the frequency domain with FFT plot
figure;
maxdB=max(Dout_dB(2:numpt/2));
fprintf('maxdB=%g \n', maxdB)

%%for TTIMD,use the following short routine,normalized to -6.5dB
%full scale.
%plot([0:numpt/2-1].*fclk/numpt,Dout_dB(1:numpt/2)-maxdB-6.5);
semilogx([0:numpt/2-1].*fclk/numpt,Dout_dB(1:numpt/2)-maxdB);
grid on;
title('Main-Amplifier Layout Simulation Output Spectrum | 518.7988281Hz Input Tone');
xlabel('ANALOG INPUT FREQUENCY(Hz)');
ylabel('AMPLITUDE(dB)');
%a1=axis;axis([a1(1) a1(2)-120 a1(4)]);

%-----------------------------------------------%
%calculate SNR,SINAD,ENOB,THD and SFDR values
%-----------------------------------------------%
%find the signal bin number, DC=bin
fin=find(Dout_dB(1:numpt/2)==maxdB);
fprintf('fin=%g \n',fin);
fprintf('fin_value=%g \n',Dout_dB(fin));
%Span of the input freq on each side
%span = 5;
%span=max(round(numpt/2000),5);
fprintf('span=%g \n',span);
%approximate search span for harmonics on each side
spanh=2;
%determine power spectrum
spectP=(abs(Dout_spect)).*(abs(Dout_spect));
%find DC offset power
Pdc=sum(spectP(1:span));
```

```
%Pdc = 0;VarName2
%extract overall signal power
Ps=sum(spectP((fin-span):(fin+span)));
%vector/matric to store both freq and power of signals and harmonics 65.7745 +13.6438i
Fh=[];
%the 1st element in the vector/matrix represents the signal,
%the next element reps the 2nd harmonic,etc..
Ph=[];
%find harmonic freq and power components in the FFT spectrum
for har_num=1:10
   %input tones greater than fSAMPLE are aliased back into the spectrum
   tone=rem((har_num*(fin-1)+1)/numpt,1);
   if tone>0.5VarName2
      %input tones greater than 0.5*fSAMPLE(after aliasing) are reflected
      tone=1-tone;
   end
   Fh=[Fh tone];
   %for this procedure to work,ensure the folded back high order harmonics
   %do not overlap
   %with DC or signal or lower order harmonics
   har_peak=max(spectP(round(tone*numpt)-spanh:round(tone*numpt)+spanh));
   har_bin=find(spectP(round(tone*numpt)-spanh:round(tone*numpt)+spanh)==har_peak);
   har_bin=har_bin+round(tone*numpt)-spanh-1;
   Ph=[Ph sum(spectP(har_bin-1:har_bin+1))];
end

%determine the total distortion power
Pd=sum(Ph(2:5));
fprintf('Pd=%g \n',Pd);
%determine the noise power
Pn=sum(spectP(1:noise_int_freq))-Pdc-Ps;
fprintf('Pdc=%g \n',Pdc);
format;
A=(max(code)-min(code));
AdB=20*log10(A);

SINAD=10*log10(Ps/(Pn+Pd));
SNR=10*log10(Ps/Pn);
snr = SNR;
disp('THD is calculated from 2nd through 5th order harmonics');
THD=10*log10(Pd/Ph(1));
SFDR=10*log10(Ph(1)/max(Ph(2:10)));
disp('Signal & Harmonic power components:');
HD=10*log10(Ph(1:10)/Ph(1));
ENOB =(SNR-1.7)/6.0206;
%distinguish all harmonics locations within the FFT plot
```

```
hold on;
%plot(Fh(2)*fclk,0,'mo',Fh(3)*fclk,0,'cx',Fh(4)*fclk,0,'r+',Fh(5)*fclk,0,'g*',Fh(6)*fclk,0,'bs',Fh(
7) *fclk,0,'bd',Fh(8)*fclk,0,'kv',Fh(9)*fclk,0,'y^');
%legend('1st','2nd','3rd','4th','5th','6th','7th',' 8th','9th');

fprintf('SINAD=%gdB \n',SINAD);
fprintf('SNR=%gdB \n',SNR);
fprintf('Ps=%g \n',Ps);
fprintf('Pn=%g \n',Pn);
fprintf('THD=%gdB \n',THD);
fprintf('SFDR=%gdB \n',SFDR);
fprintf('ENOB=%g \n',ENOB);

end
```