DISSERTATION

PINHOLES AND MORPHOLOGY OF CdS FILMS: THE EFFECT ON THE OPEN CIRCUIT VOLTAGE OF CdTe SOLAR CELLS

Submitted by

Mohammed Abdulaziz Tashkandi

Department of Mechanical Engineering

In partial fulfillment of the requirements

For the Degree of Doctor of Philosophy

Colorado State University

Fort Collins, Colorado

Fall 2012

Doctoral Committee:

Advisor: W. S. Sampath

Susan P. James
James R. Sites
Anders Olsson

ABSTRACT

PINHOLES AND MORPHOLOGY OF CdS FILMS: THE EFFECT ON THE OPEN CIRCUIT VOLTAGE OF CdTe SOLAR CELLS

Cadmium telluride (CdTe) solar cells are among the many types of solar cells that have the potential to harness solar energy. CdTe has a band gap of ~1.5 eV that very closely matches the spectrum of the sun. In addition, being a thin film solar cell, the entire thickness of the solar device is a few microns and the energy required to manufacture thin film solar cells is much less than some of the more widely used solar cells. Nevertheless, CdTe solar cells lag behind solar cells of similar band gap materials in open circuit voltage.

This voltage deficit can be attributed to many factors among which perfecting the window layer material can be a very important key. The best window layer material in CdTe solar cells was found to be cadmium sulfide (CdS). Usually thick CdS layers on the order of 125nm are used to ensure that the voltage of the solar device is as high as possible, this thickness causes some photons to be absorbed in the window layer and thus reduce the photocurrent output of the solar device and consequently its efficiency.

The remedy is then to deposit thin CdS layers, as a result, the photocurrent is increased but the open circuit voltage of the device (V_{OC}) tends to decrease especially when the thickness of the deposited CdS film is less than 80nm. The reduction of V_{OC} as the CdS thickness is reduced may be attributed to discontinuities and defects in the window layer material. Such defects and discontinuities that go through the entire thickness of the CdS film expose the underlying Transparent Conductive Oxide (TCO) surface and thus allow the formation of weak CdTe/TCO diodes that are known

to reduce the voltage output of the device. These defects and discontinuities are otherwise known as pinholes.

Pinholes can be either of natural or artificial origin. Natural sources of pinholes include CdS grain coalescence and TCO surface roughness and artificial sources include scratches, scuffing marks, cleaning residues and dust and particulates in open lab environment. There has been no detailed study that discussed the following: (i) whether these sources of pinholes can be eliminated especially in CdS films deposited via closed space sublimation, (ii) whether these pinholes are actually the reason why CdTe solar cells made with thin CdS layers have less open circuit voltage, and (iii) estimate the size effect of pinholes in CdTe solar cells, i.e., how large an area of the device is affected compared to the size of pinholes.

This study focused on studying CdS films of different thicknesses deposited on TEC10 glass substrates cleaned with different cleaning methods. These films were then surveyed for pinholes using Blue-Light Transmission Optical Microscopy for pinhole observation and analysis of the artificial sources of pinholes. The natural sources of pinholes were analyzed and studied via Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Spectroscopy (EDS). It was possible to determine the size effect of pinholes by combining images obtained from Electroluminescence (EL) as well as Light Beam Induced Current scans (LBIC). In addition, computer models and simulations using PSpice® and MATLAB® allowed further studying the effects of varying the area of pinholes on the open circuit voltage and compare such results to literature as well as identifying possible pinhole area limits via diode voltage profiles.

The results indicated that natural sources of pinholes are not major sources of

pinholes in CdS films deposited via closed space sublimation. Cleaning residues was found to be the major source of pinholes in these CdS films. Also, cleaning the glass substrates with plasma prior to CdS film deposition is the key to significantly reduce pinholes in CdS films of thicknesses between 50nm and 200nm. Moreover, cleaning the glass substrates within a class 1 mini-environment did not reduce pinholes in CdS films due to the quality of the cleaning process inside such environment. Nevertheless, maintaining cleaned glass substrates in such environment may help reduce pinholes in CdS films deposited on glass substrates cleaned by standard cleaning or plasma cleaning. On the other hand, it was also found out that pinholes could affect an area that is a much as 15 times larger. The PSpice® and the MATLAB® models showed acceptable agreement with literature findings. Finally, diode voltage profile constructed via PSpice® simulations indicated that a total pinhole area corresponding to 0.001% of the total device area has negligible effects in terms of number of diodes being affected in the solar cell and a corresponding V_{OC} loss of about 30mV.

ACKNOWLEDGMENTS

I would like to thank ALLAH almighty for all his blessings, for providing me what it takes to pursue a PhD degree, and for all the continued magnificent blessings through out my life so far. I would like to express my sincere gratitude for my parents for all the help and support they showed and their prayers through my life so far and especially in my graduate studies. I would like to express my gratitude for the Custodian of the Two Holy Mosques King Abdullah Al Saud for giving me as well as thousands of other Saudi students the opportunity to study in the United States and earn undergraduate and graduate degrees in all branches of Science through King Abdullah Scholarships for studying abroad. I would also like to express my appreciation for the Ministry of Higher Education of Saudi Arabia and the Saudi Cultural Mission in Washington D. C. for all their help and assistance.

I would also like to thank my adviser Dr. W.S. Sampath for all his support, for allowing me to be part of his research group and all the help he provided through this wonderful PhD journey. I would like to thank the head of the mechanical engineering department, my adviser for the master's degree and committee member Dr. Susan James for all her support, believing in me and encouraging me to pursue my PhD degree. In addition, I would like to thank my remaining committee members Dr. James Sites and Dr. Anders Olsson for all the support and help and understanding that both have provided during my PhD degree.

Also, I would like to thank my fellow students at the Materials Engineering Laboratory especially Kevin, Jason, Drew and Paul as well as the students in PV lab in the Physics department especially John, Russell and Katherine. I would also like to

thank Patrick McCurdy at the Central Instrumentation Facility for his help and guidance using SEM and EDS. I would also like to thank Cecily Broomfeild at the Orthopedic Research Lab for her assistance with Blue Light Transmission Microscopy. I would also like to acknowledge the funding from the National Science Foundation (NSF) and the Department of Energy (DOE) for equipment, materials and supplies used to complete this study.

In addition, I would also like to thank all my family members and friends especially my brother Dr. Abdulhadi Tashkandi for all the guidance, understanding and support that he always showed me and hope I would be able to repay him some of that in the years to come. Finally, I would like to thank my wife and my children for being so patient, supporting and understanding through out my PhD degree and providing me with everything I needed to make this happen every step of the way and I hope to be able to show them the same support through life.

TABLE OF CONTENTS

LIST OF TABLES

Ch. 2

Ch. 3

Ch. 4

Ch. 5

LIST OF FIGURES

Ch. 1

Ch. 2

Ch. 3

Ch. 4

Ch. 5

Appendix A

Appendix B

Chapter 1

Introduction

There is an abundant source of power that we come across and benefit from (not its full potential though) everyday but we are still barely scratching the surface of this power source. That is Solar Power. Sunlight delivers about 1300W/m^2 to Earth and about 1000W/m^2 reaches the Earth's surface. It has been estimated that the US gets about $2.4x10^{16}$ kWh of sunlight energy annually[1]. If harnessed to its full potential, solar power can be the most dominant source of energy Worldwide. There are global demands and efforts to properly harness solar power.

In 2010, a total of about 16 GW of solar power capacity was installed around the globe, which is very large compared to the total capacity installed in 2009, about 7.5 GW [2]. Moreover, there were a total of about 29.7 GW of installed capacity in 2011 according to the European Photovoltaic Industry Association (EPIA) [3]. This makes the total Worldwide PV (Photovoltaic) capacity increase to about 70 GW, enough energy to meet the energy demands of more than 12 million households. According to EPIA, this makes solar cells the third most important source of renewable energy behind hydro and wind power [3]. This growth in global installed PV capacity is presented in figure 1.1 below.

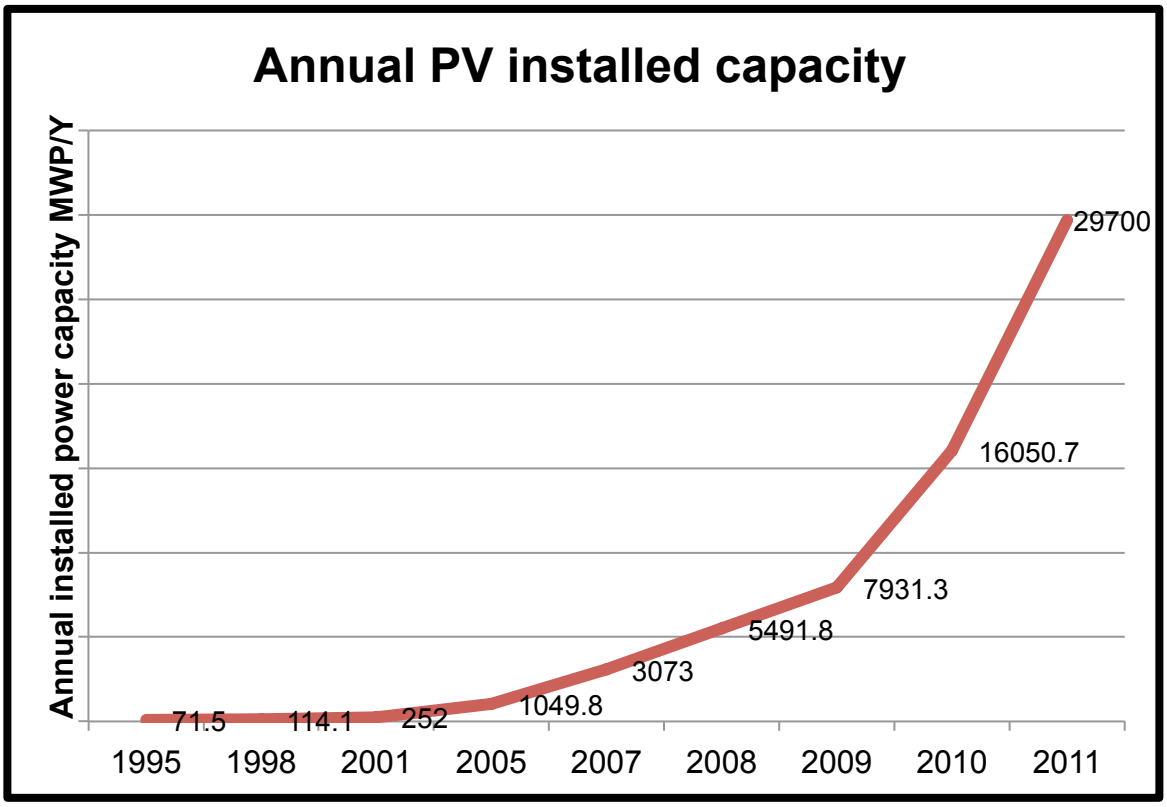

Figure 1. 1: Total Worldwide installed capacity of solar cells form 1995 to 2011.

Despite this phenomenal growth in installed PV capacity and being a major source of renewable energy, there is still much to be learned and much more to be achieved. Thin film solar cells and in particular cadmium telluride (CdTe) solar cells have a potential to be the most widely used types of solar cells. CdTe as a semiconductor material have an energy band gap of about ~1.5eV that closely match's the sun spectrum. Unlike crystalline silicon solar cells, CdTe solar cells are based on thin film technology that requires much less materials to produce, lower process temperatures and consequently much less energy of production. On the other hand, CdTe solar cells lag behind other kinds of solar cells in conversion efficiency primarily due to its low open circuit voltage (voltage deficit) [4]. Figure 1.2 illustrates this voltage deficit by comparing CdTe solar cells to gallium arsenide (GaAs) solar cells.

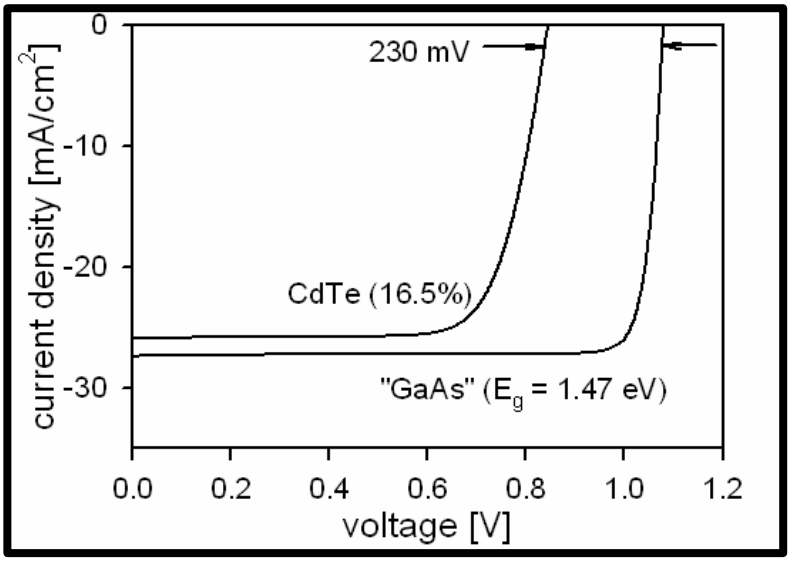

Figure 1. 2: Current- density – voltage curves of a CdTe solar cell and GaAs solar cell showing the voltage deficit of CdTe solar cells [4].

Photocurrent is produced by the absorption of photons at the CdTe/CdS junction. The properties and quality of each of these two layers among other device layers are very important factors for improving the performance of CdTe solar cells. More importantly, cadmium sulfide (CdS) has been recognized as one of the major sources of this voltage deficit. Open Circuit Voltage (V_{OC}) across the cell can be maintained by using a relatively thick CdS layer (more than 125nm) and by doing so, some of the sunlight photons that could reach the CdTe/CdS junction to help generate more photocurrent are absorbed in the CdS layer. As a result the generated shot circuit current density J_{SC} of the cell decreases. Since the conversion efficiency and fill factor of solar cells depend on both V_{OC} and J_{SC}, it is therefore significantly important to be able to maintain high voltage while increasing the photocurrent via decreased film thicknesses. But as CdS film thickness is reduced, V_{OC} is reduced as well.

Beneath CdS, there is a front contact layer made out of transparent conductive oxide (TCO). TCO areas that are not covered by the CdS layer from weak diodes with CdTe and as a result voltage drops. These uncovered area or discontinuities in CdS film are basically referred to as pinholes. There are many studies that are focused on efforts to achieve pinhole-free and continuous CdS thin film layer [5-12] but the efforts that are focused on observing and confirmation of pinholes are limited [13] as well as efforts that study the relation between CdS and the accompanying drop in V_{OC} [4, 14-18]. There has never been a clear understanding of what causes pinholes in thin CdS film layers, whether there is a tolerable level of pinhole density at which CdS thickness can be optimized so that voltage is maintained and current density is increased.

This dissertation work investigated CdS film layers deposited at the Materials Engineering Laboratory at Colorado State University. CdS films of different thicknesses were deposited on TEC10 glass substrates (3mm thick glass substrates with TCO layer that has a sheet resistance of 10Ω/□) that were cleaned with different cleaning methods. This setup helped recognize different sources of pinholes in deposited CdS films. Blue-Light Transmission Optical Microscopy (BLTOM) was used to observe pinholes at a magnification of 200X to take digital images of such defects. Pinhole area in each image was calculated using an image J software called Fiji for each surveyed sample. The data of pinholes and pinhole areas were collected and used to test various hypotheses regarding the presence in pinholes in CdS films deposited on substrates prepared via different cleaning methods.

Scanning Electron Microscope (SEM) was used to study CdS films at higher magnifications and thus confirm grain structure, grain coalescence, and surface

morphology. Energy Dispersive x-ray Spectroscopy (EDS) was used to analyze pinholes and film areas where full CdS coverage was evident to further distinguish pinholes and define elemental composition. This helped differentiate other sources of pinholes and confirm the presence and/or elimination of pinholes in CdS films that were deposited via Close Space Sublimation (CSS).

To shed some light into the effects of pinholes, electroluminescence (EL) and light beam induced current (LBIC) were used to study the size effects of pinholes. In addition, 2D PSpice® simulations were conducted to visualize the effects of different fraction of pinhole area on V_{OC}. This PSpice® model was also used in junction with a MATLAB® mathematical model to verify simulation results and compare voltage loss results to the data reported by the 1998 NREL IEC report [13]. In addition, the 2D PSpice® simulations were used to study the diode voltage profiles in the simulated solar device corresponding to different fraction of pinhole areas.

Chapter 2

Literature Review

2.1. Basics of Solar Cells

The following section is a background review of photovoltaic principles in general. It contains information about solar cells, their concepts, and the different kinds of solar cells being used or developed nowadays. This is followed by a more detailed discussion about CdTe/CdS solar cells. This includes some of the most widely used deposition methods and some emphasis on the window layer.

2.1.1. Photovoltaics

The entire technology related to solar cells manufacturing and development is known as Photovoltaics (PV). Solar cells absorb sunlight and generate electricity without pollution, noise or any moving parts in general. There is a direct relation between sunlight spectrum and solar cells.

Sunlight delivers more than 1300W (Watts) of power above the Earth's atmosphere per square meter. Due to reflection and absorption through its way to the Earth's surface, a loss of about 300W of power occurs at noon on a clear day. PV benefits very much from the intense sunlight at noon; and it would be an impractical concept if there was much less amount of sunlight around noon. Luckily, there is a plateau of time (5-7 hours around noon) during which sunlight is intense enough to benefit solar cells. The total energy available from solar cells on a typical day in the US is about 5-9 kWh/m^2 of exposed area. Denver for example gets about 8.5 kWh/m^2 on a typical day and most of the country about 6 to 8 kWh/m^2 which is more than enough for an effective PV use.

This gives a measure of how much energy can be converted to electricity. Taking into consideration land area, climate and altitude, the US receives about $2.4x10^{16}$ kWh of sunlight yearly, which is a huge source of power. [1, 19]

Sunlight is seen as yellow colored rays of light, but in reality it is made of a spectrum of colors. It would be more beneficial for solar cells if the spectrum was made of one color and it would allow much more efficient conversion of light into electricity. Different colors of the spectrum (blue, yellow and red) have different energy levels. At one end of the spectrum, ultraviolet (UV) light (blue) is basically light with energy too high for the human eye to see and most of it is absorbed by the ozone layer. On the other end, infrared light has too little energy for us to see and most of it is absorbed by water vapor and carbon dioxide in the atmosphere. The latter is the kind of light that causes the greenhouse effect. Some solar cells can benefit from the entire spectrum and others can only befit from specific regions of the spectrum. [1]

The photons from sunlight can be characterized in two ways, by their energy in units of electron volts (eV) or by their wavelength in units of nanometers. The electron volt represents how much energy a photon gains when accelerated by a force of 1 volt applied for a distance of 1 cm. For example, the energy of a photon in the visible portion of the spectrum is about 2 eV of energy and a corresponding wavelength of about 600nm. [1]

2.1.2. Solar Cells

From a structure point of view, solar cells are made of different layers that have specific roles in the process of light absorption and electricity generation. These layers namely are: glass, an anti-reflective layer, front contacts or metal grids, two

semiconductors that form a p-n junction, and the back contact as shown in figure 2.1. The most important event happens within the p-n junction. It is composed of two semiconductor materials each of which is heavily doped with dopants (impurities) that generate lots of free electrons (n-type) or lots of holes, i.e., lack of electrons (p-type). Only photons with sufficient energy (having energy higher than the band gap E_g) of the semiconductor can knock electrons loose and thus forming the electron-hole pair.

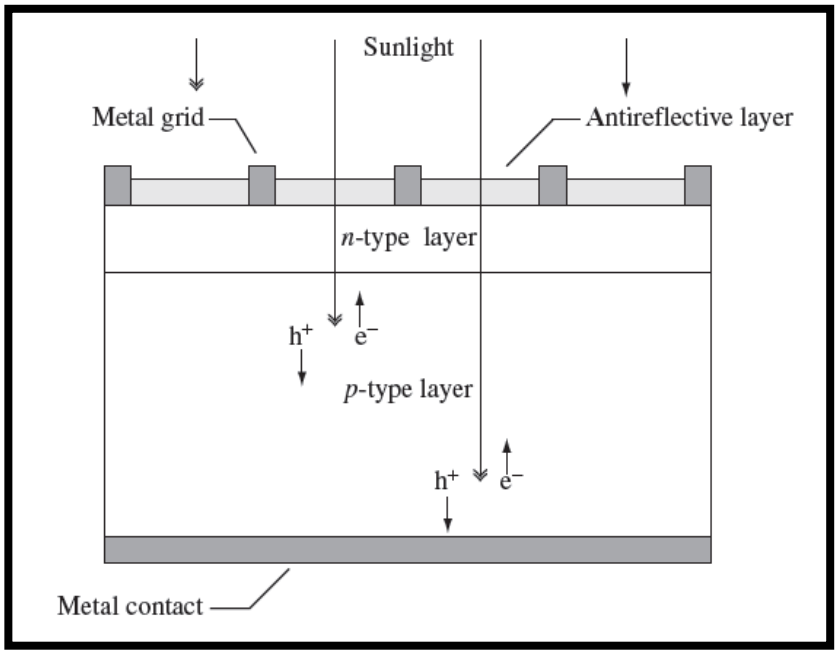

Figure 2. 1: Typical structure of a solar cell. [19]

The energy band structure of a semiconductor consists of a conduction band and a valance band. When the electrons near the maximum of the valance band are excited, they jump or move over to the conduction band leaving holes behind. The difference between the conduction band and the valance band defines the band gap of the material (Eg). The excited electrons and remaining holes in these two bands are the negative and positive mobile charges that allow the generation of current in solar cells. Figure 2.2 shows a simplified band gap diagram for direct band gap materials such as

CdTe.[19] The first level of unoccupied cation (the 5s level of Cd) forms the conduction band; and the highest level of occupied anion (the 5p level of Te) forms the upper most valance band [20].

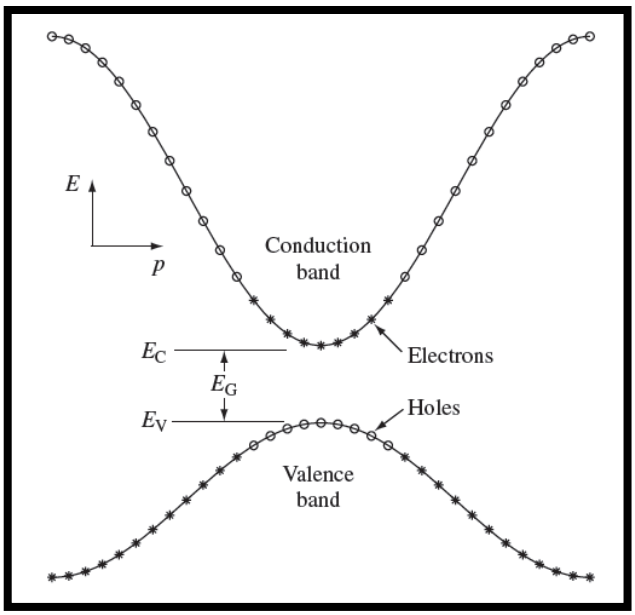

Figure 2. 2: Simplified band structure of a direct band gap material at T>0K [19]

A semiconductor can be controlled to be an n-type or a p-type material. Silicon is a good example, when Si (valance of 4) is doped with Phosphorus (P, valance of 5); four of the five electrons from phosphorus will fill the outer energy level of silicon and the fifth electron will be donated to the conduction band. For each phosphorus atom introduced, one electron is donated to the conduction band and thus making the material an n-type semiconductor that has lots of free electrons and fixed positive charges that do not move. On the other hand, when Si is doped with an element that has less valance electrons such as Boron (B, valance of 3); each Boron atom accepts one electron from the valance band to fill its outer energy level and thus leaving a hole behind and stationary negative charges that do not move. [19]

When two n-type and p-type semiconductors come together, the free electrons and holes will combine until both materials reach equilibrium and no further recombination is allowed. This forms a depletion region at which no free charges exist and an electric field is built across the cell pointing from the n-type side to the p-type side of the junction across the boundary of the dissimilar joined semiconductors [14]. As light goes through the cell, it gets past the anti-reflective layer that helps absorb photons and deliver them to the p-n junction of the cell. Photons with enough energy free electrons and holes. The freed electrons that are near the boundary of the p-n junction get pushed far away from the boundary by means of the electric field, this causes an imbalance in the cell and this electron will have to reestablish neutrality. On other hand, the freed hole gets pushed away from the junction in the other direction. If the electron were to pass through an external circuit, produce current and return back to the other side of the cell and recombine with the hole, neutrality would be reestablished. These separated pairs of electrons and holes form a photocurrent (going from the n-type side to the p-type side of the cell) across the p-n junction. [1, 14] If the formed electric field were to cover the entire p-n junction, then electron-hole separation would be expected to occur everywhere across the junction and thus increasing the effectiveness of the solar cell.

There are quite a few types of solar cells based on the semiconductor materials used for building the cell. The Worldwide market share of crystalline silicon solar cells is quite large and exceeds the other types of solar cells. On the other hand, CdTe thin film solar cells make about 10% of the Worldwide market share according to recent studies [14]. Although crystalline silicon dominates the World market, it has many disadvantages. Si crystals are very hard to grow and very brittle, the Si used for the

deposition process needs to be very pure and the deposited layers are much thicker than most thin film solar cells (about 300 microns). These factors make Si solar cells very expensive intrinsically and the cost of manufacturing is too high as compared to other more conventional power sources. Thin film solar cells on the other hand are made of much thinner film layers (2-10 microns) and fabricated at a relatively lower temperature as compared to crystalline Si solar cell. These factors reduce the cost of thin film solar cells as compared to Si solar cells and give thin film solar cell the chance of being a candidate of a major source of energy. As far as performance is considered, Si solar cells are known to have better cell performance due to the extensive knowledge of this type of semiconductors in the industry. In order for thin film solar cells to reach the same level of performance and cell properties as crystalline Si solar cells, scientists need to investigate the various film layers and their properties in order to gain the materials knowledge required [14]. Solar cell efficiency is determined by physically measuring device parameters such as the open circuit voltage of the cell, the short circuit current and some other factors. These factors are usually obtained from a current density – voltage (JV) curve of the solar device as shown in figure 2.3.

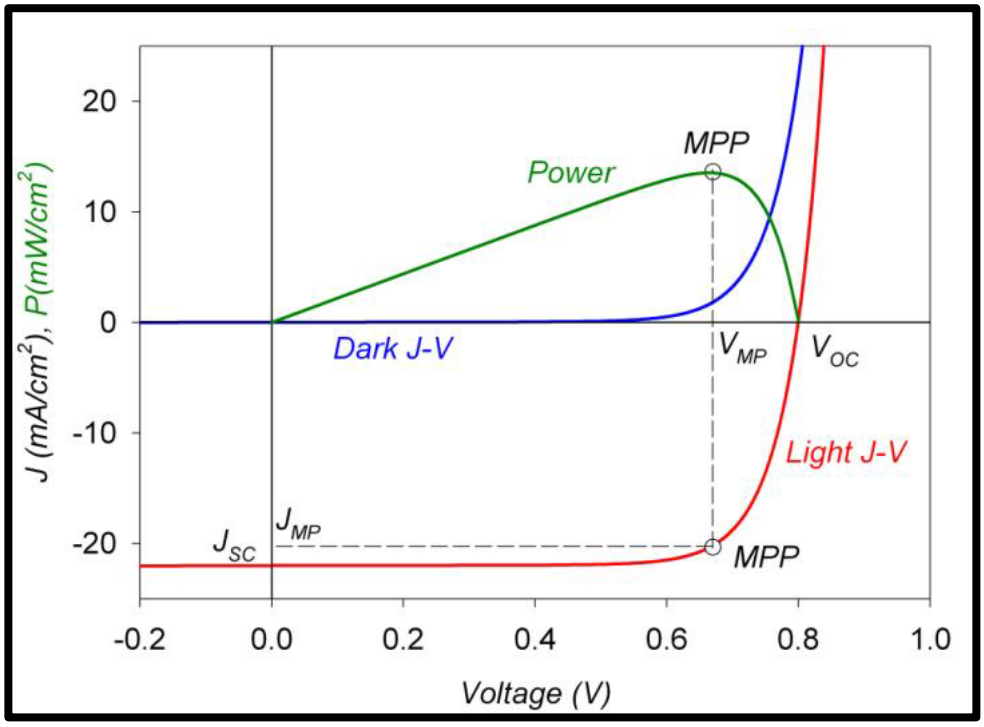

Figure 2. 3: An example JV curve of a solar cell. [21]

2.1.3. JV curve analogy

Solar cells efficiency is controlled by the parameters observed in the current-voltage curve. An example of a JV curve is shown in figure 2.3. The value of the voltage at which the red curve crosses the voltage axis (x-axis) is called open circuit voltage V_{OC}. On the other hand, the value at which the red curve crosses the current axis (y-axis) is called the short circuit current density J_{SC}. Using the power density curve (green line), one can obtain the maximum power voltage (V_{MP}) and the maximum current density (J_{MP}) corresponding to the maximum power point (MPP) of the device. Using these parameters, the fill factor (FF) of the solar cell can be calculated as shown in equation 2.1 and consequently the efficiency (η) can be calculated as shown in equation 2.2. P_{in} in equation 2.2 is the standard normally incident solar power density that is equal to 100 mW/cm^2.

An example of such parameters from an actual CdTe Small Area Device (SAD) is shown in table 2.1.

$$FF\ (\%) = \frac{V_{MP} \cdot J_{MP}}{V_{OC} \cdot J_{SC}} \times 100\% \quad (2.1)$$

$$\eta\ (\%) = \frac{FF \cdot V_{OC} \cdot J_{SC}}{P_{in}} \times 100\% \quad (2.2)$$

Table 2. 1: Basic solar cell parameters

V_{OC}	J_{SC}	V_{MP}	J_{MP}	FF (%)	η (%)
775 mV	20 mA/cm^2	570 mV	16.5 mA/cm^2	60.3	9.42

2.2. CdTe Solar Cells

CdTe thin film solar cells in particular have many aspects that make them a very promising type of solar cells. CdTe by itself is a direct band gap material with a band gap value (E_g) of ~1.5 eV which is a perfect match to the spectrum of the sun, i.e., its E_g is “nearly optimally matched to the solar spectrum for photovoltaic energy conversion” [20]. It has a high quantum yield over a wide range of wavelengths since it has a very high absorption coefficient (>5x10^5 /cm). According to McCandless and Sites, the high absorption coefficient translates into 99% absorption for photons with $E>E_g$ of the absorbable AM1.5 photons for a film thickness of 2 microns. [20]

From a history perspective, CdTe solar cells went through some major modifications. The most important was the conductive type; the early researched CdTe solar cells were n-type CdTe single crystals and polycrystalline solar cells. Ultimately, the lack of a p-type conductor that is suitable for the n-type CdTe led to considering CdTe as a p-type semiconductor (absorber layer). In these devices, the short length spectral response was influenced by a heteropartner and low resistance contact; these heteroparters (referred to as window layers) include stable oxides such as In_2O_3:Sn,

ZnO, SnO_2 and CdS. The First CdTe/CdS solar cell was made in the mid-1960s and had a conversion efficiency of about 5%. In 1977, the highest reported cell efficiency for a thin CdS film deposited on a single crystal p-type CdTe was reported by Yamaguchi et al. in [5] of about 11.7% and a V_{oc} of 670 mV utilizing a 500 nm CdS layer.[20]

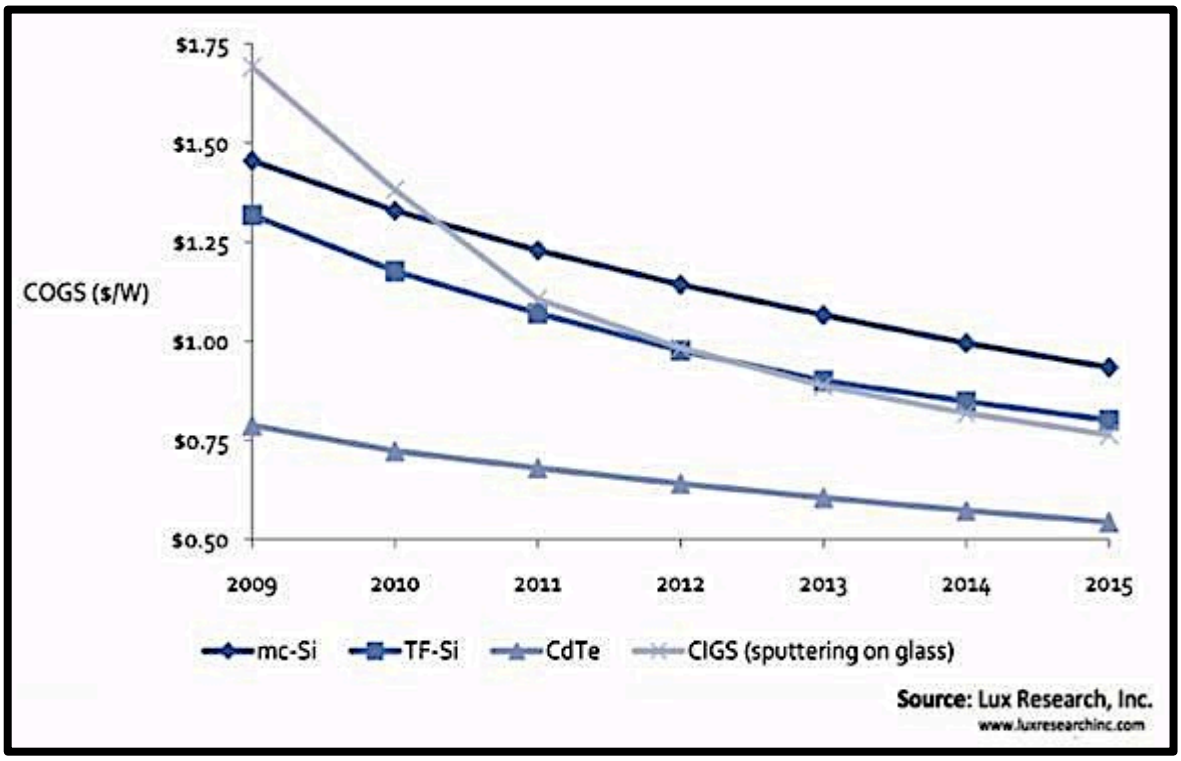

Figure 2. 4: Cost of different PV technologies current and projected.

BY taking a look at the cost of PV technologies, according to Lux Research Inc., the cost of CdTe solar cells is much less than the cost of any other PV technology and it is expected to decrease to about 0.5 ($/W) in 2015 as shown in figure 2.4 above. This means that thin film CdTe solar cells may very well be a competitive source of energy in many applications. According to a report issued by the United States Department of Energy (DOE) that compared the annual global growth of different PV technologies between 2008 and 2013 [22], the annual growth of thin film solar cells is still far behind crystalline silicon solar cells. On the other hand, the annual growth of produced CdTe

solar cells was dominant among thin film technologies. The annual global growth rate of various thin film technologies is shown in figure 2.5. It shows that CdTe solar cells have the potential to be the most widely produced thin film solar cells.

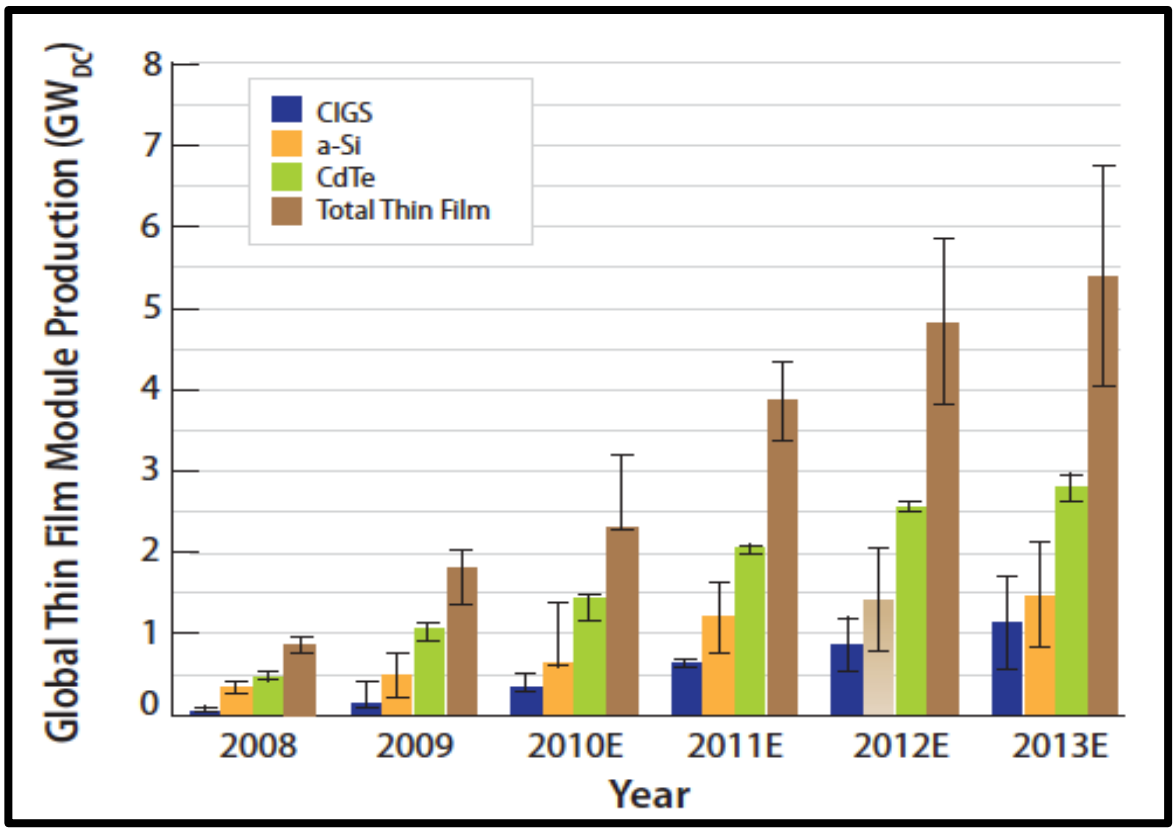

Figure 2. 5: Annual growth of different thin film PV technologies from 2008 to 2013 [22].

2.2.1. Deposition Methods

CdTe solar cells can be deposited on a superstrate or substrate configurations. The transparent conductive oxide layer (TCO), CdS and CdTe films are sequentially deposited in the superstrate configuration (as shown in figure 2.6) whereas CdTe is first deposited onto a substrate followed by deposition of CdS and TCO sequentially in the substrate configuration. In both configurations, light goes into the cell through glass, passes the TCO and CdS films and reaches the CdS/CdTe junction. The superstrate

configuration has been proved to be an aspect of high efficiency CdTe solar cells in addition to exposing the CdTe film to a Chlorine (Cl) and/or Oxygen (O_2) treatment [20]. These two aspects have led to the record conversion efficiency as of 2012 which was about 17.3% (V_{OC} of 842 mV, J_{SC} of 27.2 mA/cm^2 and a FF of 75.6%) [23].

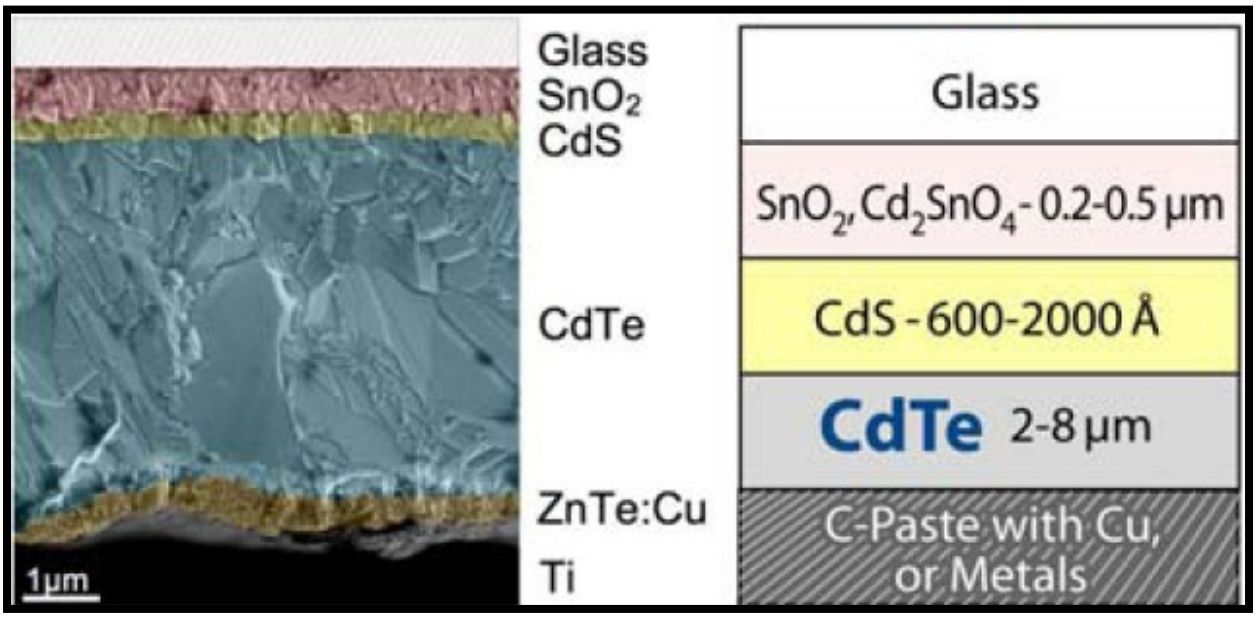

Figure 2. 6: Superstrate configuration of CdTe solar cell showing different layers and their corresponding thicknesses. [20]

There are three major deposition methods of CdTe films based on the chemical concept of the deposition process. The first concept includes Close Space Sublimation (CSS), Physical Vapor Deposition (PVD), Vapor Transport Deposition (VTD), and Sputter deposition. These processes relay on the condensation and/or the reaction of the element vapors to be deposited (for example, Cd and Te or Cd and S) on a surface. The second concept includes Electodeposition and is based on the galvanic reduction of Cd and Te ions at a surface. The third concept includes Metal Organic Chemical Vapor Deposition (MOCVD), Screen Print Deposition and Spray Deposition all of which are based on the reaction of precursors at a surface [20]. The main deposition process

used at the Materials Engineering Laboratory (MEL) at Colorado State University is based Close Space Sublimation (CSS), it is discussed in the next section while the other processes were reviewed in detail by McCandless and Sites [20].

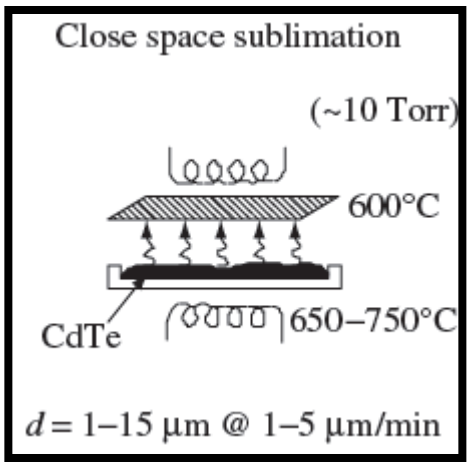

Figure 2. 7: An illustration of CSS. [20]

Close Space Sublimation (shown in figure 2.7) is usually used to deposit thin films at temperatures greater than 400°C. The deposition rate and utilization in CSS becomes limited due to the re-evaporation of the growing film. This effect can be overcome by depositing the film under higher total pressure (~1 Torr.) during which deposition becomes very diffusion-limited and both the source and substrate have to be in very close proximity; hence the name close space sublimation. In general, an insulating spacer is used to allow thermal insulation of the source and substrate and hence maintain a good temperature differential during the deposition process. Other process conditions include using a nonreactive gas as an ambient for the deposition process and also including a small O_2 partial pressure that has been shown to improve film density and solar cell quality. [20]

2.2.2. Window Layer

CdS has been identified as the perfect heteropartner for CdTe [9, 12, 18]. In general, CdS can be deposited via any of the deposition methods mentioned above, although it is favorable to maintain the same deposition method for different films (CdS, CdTe, etc.) so that compatibility is maintained throughout the cell manufacturing process. Moreover, according to Davies [15], maintaining the deposition method throughout the fabrication of the solar cell allows an in-line configuration and compactness of the cell producing equipment. Also, the waste by-products of the deposition process can be eliminated in an all-vapor deposition process for both CdS and CdTe. The ability to build the solar cell in a single vacuum chamber with adjacent deposition stations without having to lose vacuum, use extra chambers and/or equipment for the other deposition methods is also attractive. More details about the window layer and its properties will be discussed in the next section.

2.3. Thin CdS

The conversion efficiency of CdTe/CdS solar cells is lagging all other thin film solar cells despite the fact that band gap of CdTe is a perfect match for the sun spectrum [4]. There are many efforts to improve the efficiency of CdTe solar cells that include optimizing the CdS (window) layer, optimizing the CdTe layer (absorber), introducing a resistive buffer layer between the TCO and the CdS films, heat treatment of both CdS and CdTe layers in $CdCl_2$ environment and many others. This section is focused on surveying and analyzing the literature for studies that focus on optimizing the window layer, observe the morphology of CdS layers at different film thicknesses, observe and

study pinholes or discontinuities on the film surface and relate film thickness to the open circuit voltage (V_{OC}) and the short circuit current (J_{SC}) of the cell.

The maximum attainable theoretical current density from CdTe solar cells is about 30.6mA/cm^2 [17, 24, 25]. About 25% of the maximum theoretical current is lost by means of being absorbed in thick CdS films [25]. Therefore it is important to lower the CdS film thickness to minimize current losses due to window layer absorption below wavelengths of 520nm [17, 26]. Another issue that affects the performance of CdTe solar cells related to CdS is the lack of carrier collection in CdS which can be addressed by reducing the thickness of CdS and thus allowing more light particles (photons) to reach the absorber layer [18]. It has been proven that transmittance of photons that reach the absorber layer can be increased by thinning CdS; this allows more photons with energies greater than the band gap of the absorber layer to contribute to the production of photocurrent. In other words, achieve high short circuit current density in the completed solar cell by increasing the number of incident photons that reach the solar cell junction [10, 15, 16, 25]. But this improved photocurrent is not free nor is without consequences.

As it turns out, as CdS layer is thinned, many phenomena occur. As CdS is thinned, the electric field distribution becomes non-uniform [18]. It can also lead to shunting [26], and the formation of pinholes can become more probable as well as pores in the TCO/CdS interface and thus leading to the degraded film quality [6]. Moreover, weak junctions or diodes that are formed between the TCO and CdTe reduce the voltage output of the device especially at high density of pinholes in non-uniform CdS layers with large grain sizes [15]. So, formation of the window layer without any defects or with

a minimal defect density is a fundamental aspect to obtain full coverage of CdS film that is free of pinholes and empty spaces between grains as well as a uniform distribution of grain size within the film layer [7, 25]. According to Ferekides [24], one needs to control grain size and maintain it small enough to obtain pinholes free surface depending on the film thickness. Film surface roughness also affects the performance of CdTe solar cells. After the deposition of the CdS film and as the CdTe/CdS interface is formed, rough CdS particles act as recombination regions around the depletion region and thus reducing the efficiency of the solar cell [27].

Moreover, reduction of the window layer transmission and a decrease in short wavelengths quantum efficiency (QE) occurs due to the interdiffusion that is promoted between the CdS and the CdTe layers during deposition. These effects can be reduced by controlling the process conditions or heat-treating the CdS film by $CdCl_2$ and thus being able to obtain a continuous very thin film thickness and promote recrystallization of the film material [11, 20]. It was found out those CdTe solar cells which actually had no CdS layer did not perform very well either [20]. Some efforts in the area of utilizing a highly resistive transparent oxide layer (HRT or buffer layer) between the CdS and the TCO suggest that a thinner CdS layer can be used to produce the desired enhanced cell parameters [28, 29]. The direct relation between CdS film thickness, the formation of pinholes and the electrical cell properties will be discussed next.

2.3.1. V_{OC} and J_{SC}

A fundamental issue to solar cell performance and related to CdS is V_{OC}. As pinhole formation is more probable for thin CdS films, the open circuit voltage of the solar cell decreases and thus the cell and module performance suffers. According to Sites [4], the

primary reason behind the lower efficiency of CdTe solar cells as compared to other crystalline solar cells (about 3%) made of similar band gap materials is the result of a large voltage deficit. Thin CdS film cause the current density J_{SC} to increase and thus increasing the efficiency of the cell, though to certain limits. As the thickness is decreased beyond some value, CdS can become discontinuous, lead to junctions between the TCO and CdTe causing excessive shunting and lower solar cell efficiency [16]. Therefore, one need to obtain high current density J_{SC} while maintaining high V_{OC} in order to increase the efficiency of CdTe solar cells beyond current recorded efficiencies [8].

There are many research efforts related to the performance of CdTe solar cells and the drop of V_{OC} in relation to the formation of pinholes in the CdS film layer. According to Granata 1996 [17], “there seems to be a critical CdS thickness between 400 and 1000Å below which junction properties degrade significantly”. It has been also reported by Hasoon et. al. [26] that high density of pinholes and discontinuities are observed for CdS films below 100nm thick and that the change in V_{OC} was dramatic in as-deposited films as the thickness was decreased less than 80nm. This decrease in V_{OC} is usually accompanied by an increase of J_{SC} but this increase does not make up for the loss of V_{OC} and average cell parameter such as fill factor and efficiency decrease. Also, as reported in [18], the optimal thickness of CdS film is about 100nm, this is because pinholes become more probable in films less than 100nm thick and V_{OC} decreases as a result. On the other hand, films more than 100nm thick have a slightly improved V_{OC} and FF but J_{SC} decreases gradually. These reports provided plots of CdS thickness vs. V_{OC} and J_{SC} as shown in figure 2.8 and 2.9.

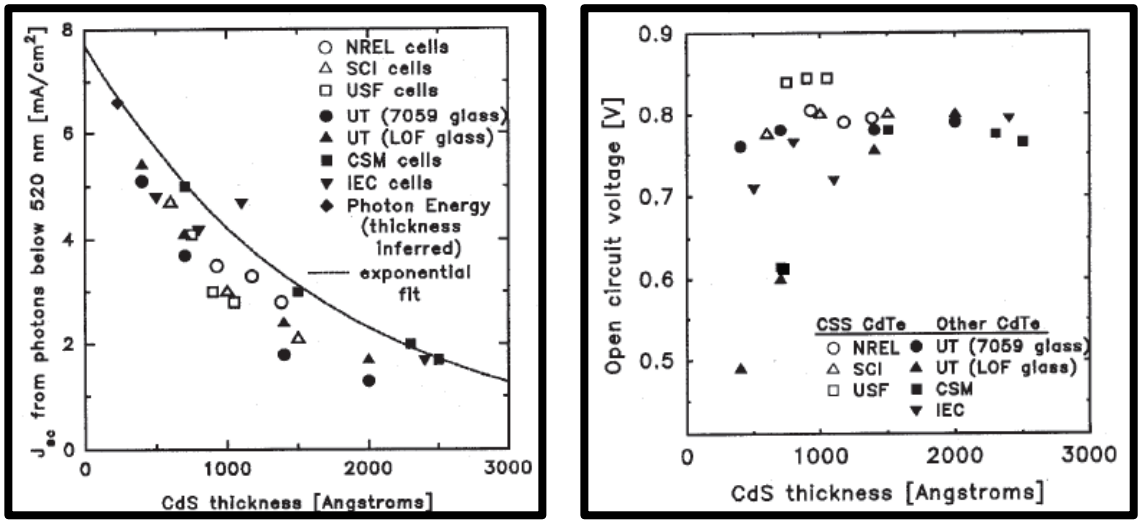

Figure 2. 8: JSC vs. CdS thickness as on the left and VOC vs. CdS thickness on the right as reported in [17] for films deposited by different techniques at NREL and different research institutions.

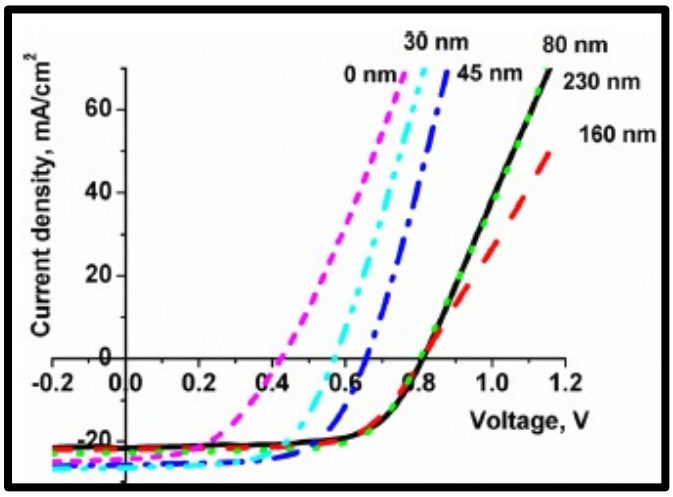

Figure 2. 9: J-V curves for different CdS thickness [18]

In his thesis, Chen 2008, [14] did similar work on CdTe solar cells that were fabricated by the Materials Engineering Lab (MEL) at CSU using an older research chamber. In his work, the TCO and CdTe thicknesses were kept constant while the CdS film thickness was varied from 0 to 250nm. Direct J-V measurement of the obtained devices were then performed and the results for V_{OC} vs. CdS film thickness as well as

J_{SC} vs. CdS film thickness were reported. These are shown in figures 2.10 and 2.11 respectively.

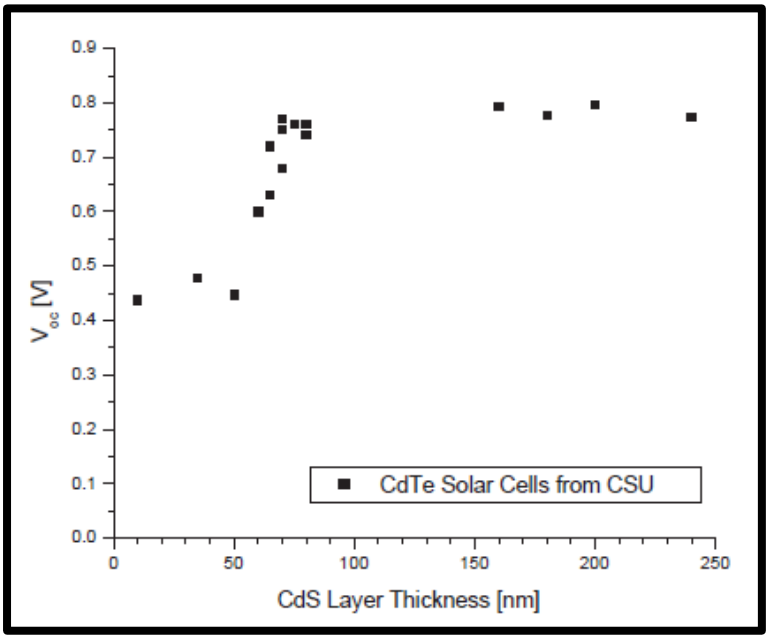

Figure 2. 10: V_{OC} as a function of CdS film thickness as reported by Chen. [14]

It was shown that there was a gradual increase of V_{OC} for the tested cells as film thickness reached 50nm thick. A more dramatic increase of V_{OC} occurred as the film thickness increased from 50 to 80nm and V_{OC} was saturated and does not change much above 80nm as shown in figure 2.10. On the other hand, J_{SC} was very high for very thin CdS film devices and it decreased dramatically as CdS thickness was increased as shown in figure 2.11. This explains why a thin CdS layer is preferred in order to reduce photon absorption in CdS and allow more photons to reach the CdTe/CdS junction [14]. One could reach high conversion efficiencies if it was possible to push down the limit at which V_{OC} decreases for thinner CdS films, obtain high J_{SC}, high fill factor (FF) and high performance solar cells.

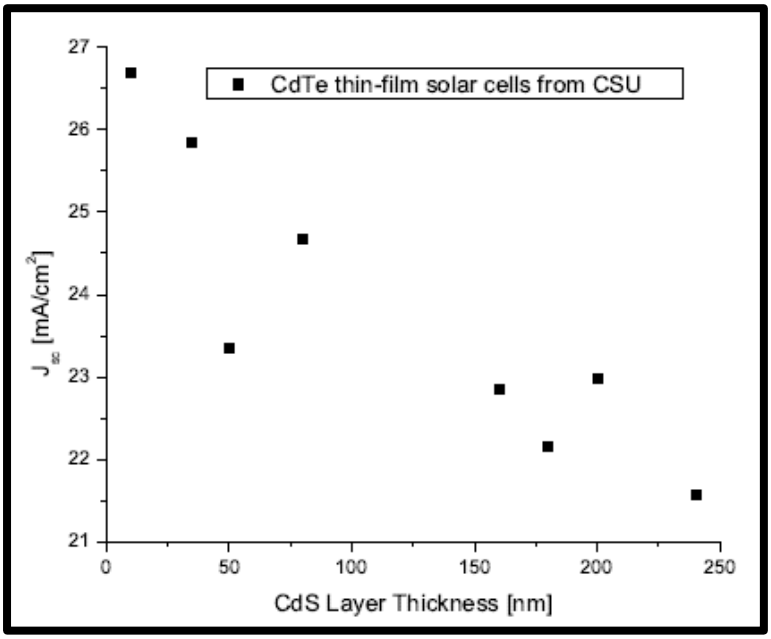

Figure 2. 11: J_{SC} as a function of CdS film thickness as reported by Chen. [14]

2.3.2. Pinholes

The steep drop in V_{OC} as CdS film thickness is reduced beyond 100nm (figure 2.10) will be referred to as "V_{OC} knee". This drop in voltage can be attributed to either electronic device properties that affect the device performance (beyond the scope of this work) or due to pinholes (figure 2.12). The latter is mainly caused by two sources: natural and artificial. Natural sources of pinholes are related to properties of the deposited CdS films as well as the properties of the transparent conductive oxide layer underneath; these are categorized into: grain coalescence of CdS and rough TCO surface. On the other hand, artificial sources of pinholes are related to pinholes in CdS films that are caused by the setup of the experiment in relation to the quality of glass substrates used, the conditions of the environment of the laboratory where the experiments were carried out and substrate handling procedures post CdS film

deposition. These include: scratches, scuffing marks, cleaning residues and dust and/or particulates in open lab environment.

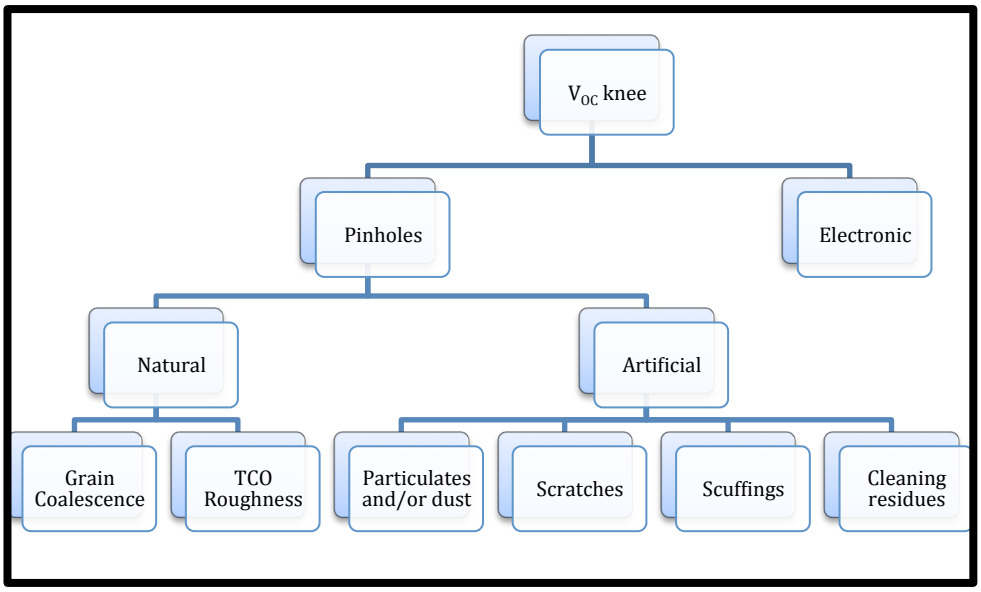

Figure 2. 12: The factors causing the V_{OC} knee.

Grain coalescence is based on the idea that nucleated CdS grains do not coalesce such that there would be empty spaces between the grains allowing junctions of CdTe/TCO to form once the absorber layer is deposited [14]. While on the other hand, TCO surface roughness is based on the idea that the surface of the TCO is relatively rough such that there are peaks and valleys within the surface of the layer. Consequently, the deposited CdS film would not entirely cover the transparent conductive oxide layer and these TCO peaks will form weak diodes with CdTe [14, 30]. The artificial sources of pinholes on the other hand are sources of pinholes that were either observed during the first stages of the research (scuffing marks and scratches on the deposited film) or sources of pinholes believed to be caused by quality of glass substrates used for CdS film deposition (cleaning residues) and the conditions of the

environment of the lab where the glass substrates were cleaned (dust and/or particulates).

Pinholes are basically discontinuities that are localized and somehow distributed randomly within the film layer. They penetrate the window layer thus allowing the formation of parallel weak diodes between the absorber layer and the TCO, this exhibits higher diode current J_O. As a result, V_{OC} is highly affected and can be reduced significantly according to the ratio of area between the CdTe/CdS junction and the CdTe/TCO junction. According to a NREL report by Birkmire et.al. (1998), CdTe/TCO junctions can be formed due to three main reasons: pinholes present in the as-deposited film, the depletion of CdS as a result of diffusion into CdTe, and the presence of broken particulate residues within the device leading to shunt paths and decrease V_{OC} as a result of the increased shunt conductance. These three causes of the CdTe/TCO weak junction are shown in figure 2.13. [13]

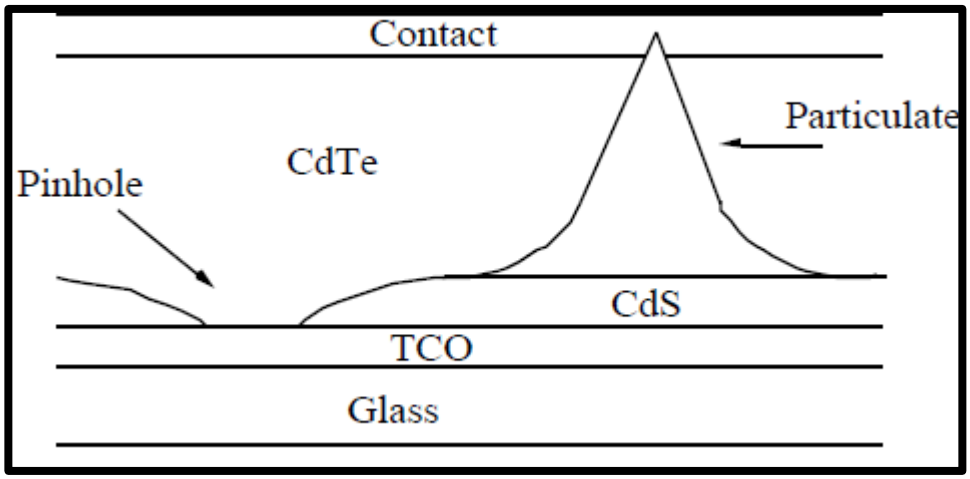

Figure 2. 13: Causes of CdTe/TCO weak junctions in CdTe solar cells. [13]

In regards to the pinhole related work, Birkmire et.al. used a Contrast Enhance Optical microscope with a band-pass filter. The filter is to reject any incoming light with energy less than the band gap of CdS (optical transmittance of the filter as compared to

a thick CdS film are shown in figure 2.14) and thus shows pinholes in the film as bright spots (figure 2.15). They made 1mm filmstrips, surveyed areas of 1cm^2 and were able to detect pinholes as small as 5μm in CdS films as thin as 50nm. Then, they categorized and counted pinholes according to size, calculate the area of pinholes in surveyed areas and finally calculated a fractional area (F) representing the fraction of area of pinholes to the total area of the surveyed filmstrips. The open circuit voltage was estimated based on the fractional pinhole area according to equation 2.3. This procedure gave a degree of quality control process for as-deposited window layer films. Table 2.2 shows a summary of the data; it shows that the open circuit voltage drops from 840mV for a perfect CdS layer device (no pinholes, 0% F) to about 570mV for a device that has a fractional area of pinholes of about 1%. According to this method, a CdS film that has 1% fractional area of pinholes can cause V_{OC} to drop by about 270mV. [13]

$$V_{OC} = \frac{AkT}{q} \cdot \ln\left[\frac{J_L}{J_{o,CdS}\cdot(1-F) + J_{o,TCO}\cdot(F)}\right] \qquad (2.3)$$

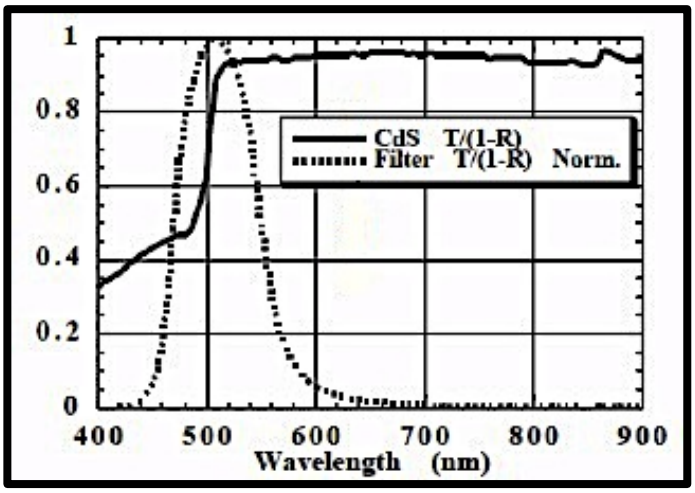

Figure 2. 14: Optical transmittance (y-axis) of the band-pass filter and a CdS film. [13]

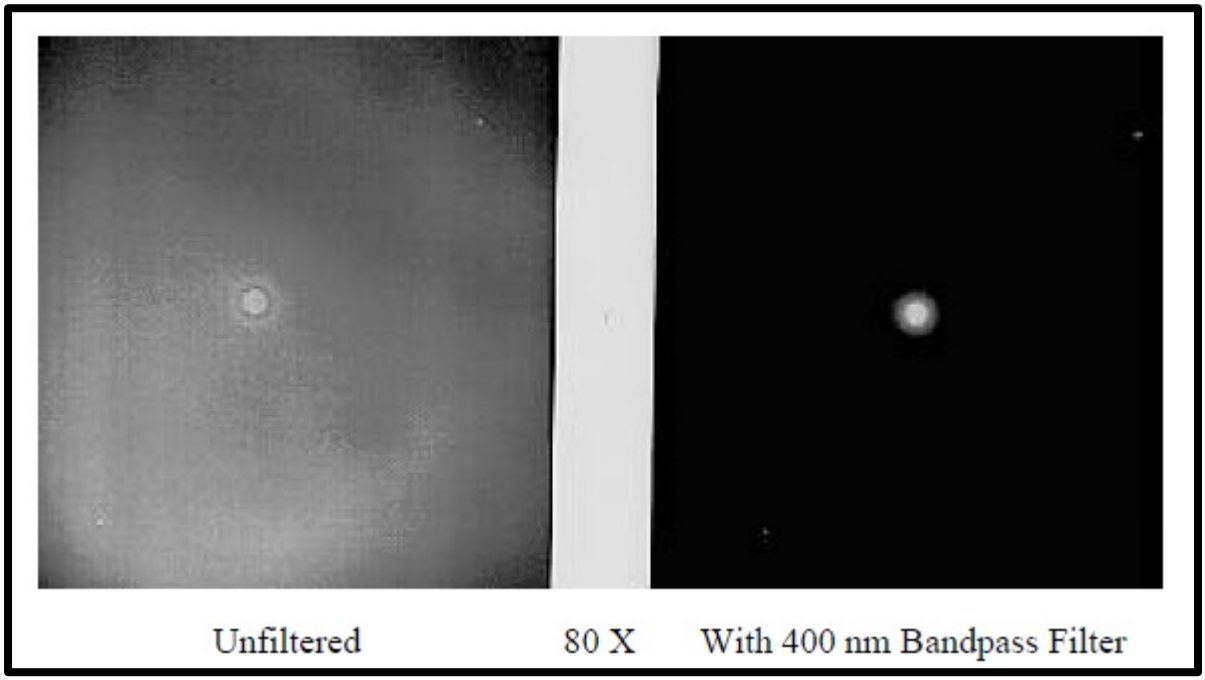

Figure 2. 15: Pinholes as shown in the 1998 NREL IEC report. [13]

Table 2. 2: Fractional area percentages of pinholes and the corresponding drop in V_{OC}.

F (holes) %	V_{OC} (mV)	ΔV_{OC} (mV)
0	840	0
0.001	830	10
0.01	786	54
0.1	687	153
1	570	270
100	330	510

Thus, this chapter included details about the literature review of CdTe solar cells with more concentration of CdS films. Based on this review, some research objectives were determined and will be investigated through the reminder of the dissertations. The next chapter discusses these objectives and the methodology by which these objectives were studied.

Chapter 3

Methodology

The objectives of the study are: a) to investigate sources of pinholes in CdS films, b) whether these sources of pinholes can be eliminated or reduced in films thicknesses ranging between 200nm to 30nm, c) the effects of pinholes on the open circuit voltage and d) area effects of pinholes. As discussed earlier, there are two main sources of pinholes: natural and artificial sources. The natural sources of pinholes (grain coalescence and TCO surface roughness) were studied by investigating surface morphology of CdS films via Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Spectroscopy (EDS). On the other hand, artificial sources of pinholes (scratches, scuffing marks, cleaning residues and dust and/or particulates) were studied by means of blue light transmission optical microscopy. Some of these sources of pinholes were further investigated by statistics to test the hypothesis that various thickness CdS films deposited on glass substrates cleaned with different cleaning methods had the same pinhole area. On the other hand, 2D PSpice® simulations as well as MATLAB® mathematical models were used to investigate pinholes effects on V_{OC}. Finally, Electroluminescence (EL) as well as Light Beam Induced Current (LBIC) were used to investigate pinhole area effects by studying Small Area Devices (SAD's). Details of the methodology implemented for studying these objectives are outlined in this chapter.

3.1. Sources of Pinholes

CdS films of different thicknesses were deposited on TEC10 glass substrates using closed space sublimation in the Advanced R&D Deposition System (ARDS) at the Materials laboratory at Colorado State University. Figure 3.1 shows an illustration of the ARDS. The ARDS chamber is maintained under vacuum (about 40mTorr) and cleaned glass substrates are loaded into the load lock. The load lock is then allowed to reach vacuum and the magnetic transfer arm transfers the glass substrates to the different stations of the ARDS for the required film deposition or specific treatments required. Normally to manufacture CdTe devices, the glass substrate is moved into the first station to heat the glass substrate, it would then be moved into the second station where CdS deposition occurs, CdTe deposition occurs when the glass substrate is moved into the third station, the fourth and fifth stations are then used to apply cadmium chloride $CdCl_2$ passivation, and the remaining stations are used to deposit the components of the back contact of the device. After all processes are complete, the glass substrate is returned to the load lock.

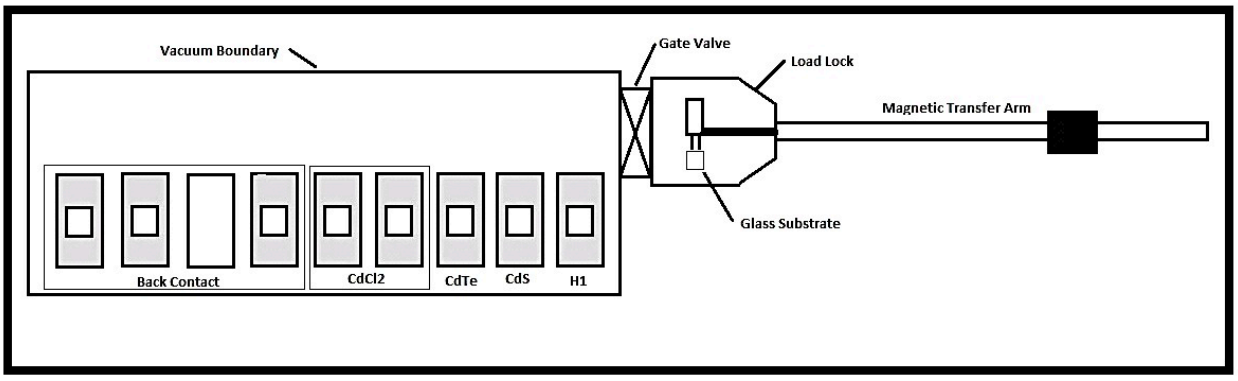

Figure 3. 1: An illustration of ARDS showing its different components and deposition stations.

All CdS films used in this study were deposited following the same procedure outlined above with the exception that the process would be interrupted after CdS is deposited and glass substrates (with deposited CdS film) are returned to the load lock. As shown in figure 2.7 in the previous chapter, close space sublimation involves two heating sources. The top source is kept at a constant temperature while the temperature of the bottom source is varied to obtain different film thicknesses. The duration of the deposition process is maintained at 110 seconds and the film thickness is controlled by the temperature of the bottom source. Consequently, relatively lower temperatures are used to obtain thinner CdS films while thick CdS films are obtained by increasing the temperature of the bottom source. For example, a bottom source temperature of 620°C was used to deposit a CdS film about 200nm thick and a bottom source temperature of 600°C was used to deposit a CdS film about 100nm thick.

These films were then used to investigate sources of pinholes both natural and artificial. As mentioned before, the natural sources include grain coalescence and TCO surface roughness. The artificial sources on the other hand include: scratches, scuffing marks, dust and particulates in open lab environment and cleaning residues. The deposited films were then divided into two groups to investigate different sources of pinholes. The first group was used to investigate the natural causes of pinholes and the second group was used to investigate the artificial sources of pinholes. Blue Light Transmission Optical Microscopy (BLTOM) was used in both groups to identify pinholes and pinhole areas. Moreover, it was used specifically with the second group to study some artificial sources of pinholes statistically.

3.1.1. Blue Light Transmission Optical Microscopy.

Blue Light Transmission Microscopy (BLTOM) basically involves using an optical microscope and a blue light filter (figure 3.2) that allows high energy bands of light to be transmitted through pinholes in CdS films making pinholes appear as bright blue spots while the rest of the film that is free of pinholes would appear as dark blue regions. BLTM has the same concept as the high contrast optical microscopy used in Ref. [13] with some modifications. These are using a blue light filter to distinguish film coverage from pinholes (transmittance of used blue filter is shown in figure 3.2) and using higher magnification, 200X. The transmittance of the blue light filter used in this study has a range between 300 and 500nm while the band pass filter used in [13] has a range of 400-600nm. As a result, the use of the blue light filter in addition to the higher magnification is expected to provide better results.

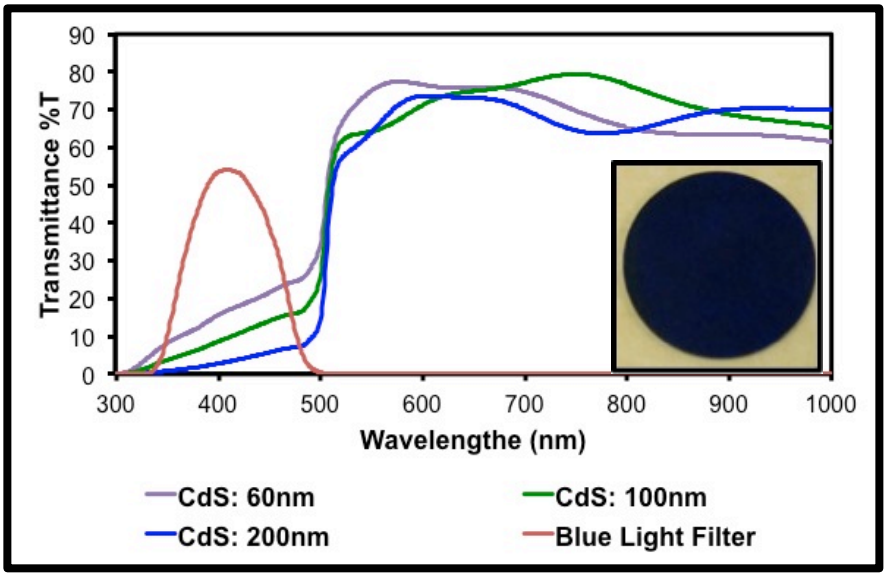

Figure 3. 2: Transmittance curves for blue filter used as well as three different CdS film thicknesses including a photo of the blue light filter.

Comparing the images that obtained in regions full of pinholes and images obtained in regions that have no CdS films indicated that both pinholes and the CdS-free areas have exactly the same color and brightness. Based on this and on the fact that the 1998 NREL IEC report showed similar images of bright spots within the CdS films as pinholes (figure 2.15); it was reasonable to treat any bright blue spot observed within the film as a pinhole. And, for the purposes of this study, all pinholes that appear in BLOTM are assumed to be defects that fully penetrated the CdS film exposing the TCO surface underneath the film. Indeed some of these pinholes are defects that penetrated the CdS film leaving the TCO surface exposed and some are areas of much thinner CdS film as compared to the rest of the film as will be shown later using Scanning Electron Microscopy (SEM).

Images obtained from BLOTM were used during the first stages of the research to identify two of the artificial sources of pinholes; these are scratches and scuffing marks. Upon refining substrate handling procedures and cleaning methods, BLTOM images of new CdS films were used to study the remaining two artificial sources of pinholes: dust and/or particulates and cleaning residues. Since dust and/or particulates as well as cleaning residues cannot be identified based on shape or patterns in BLTOM, these two sources of pinholes will be compared statistically. Figurer 3.3 shows an image of a CdS film containing some pinholes as described.

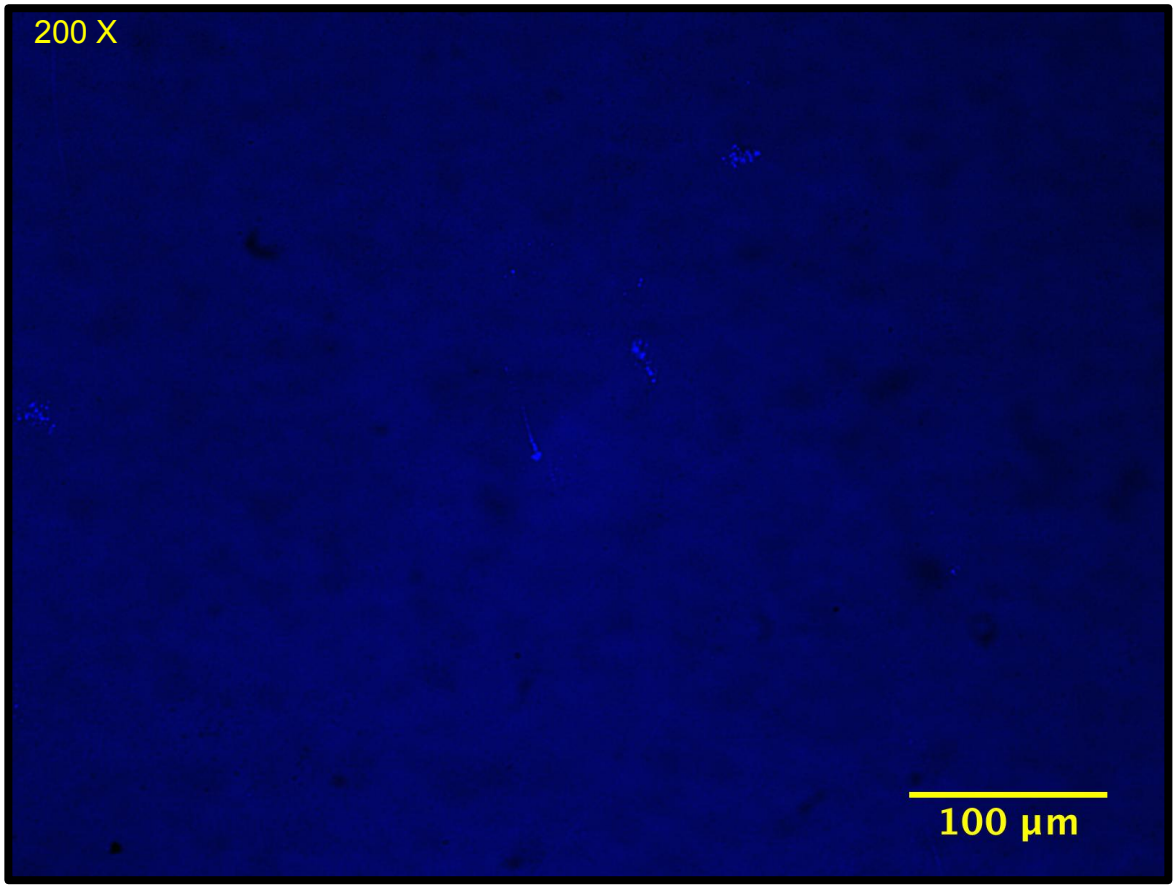

Figure 3. 3: A BLTOM image of a 200nm thick CdS film showing pinholes as bright blue spots.

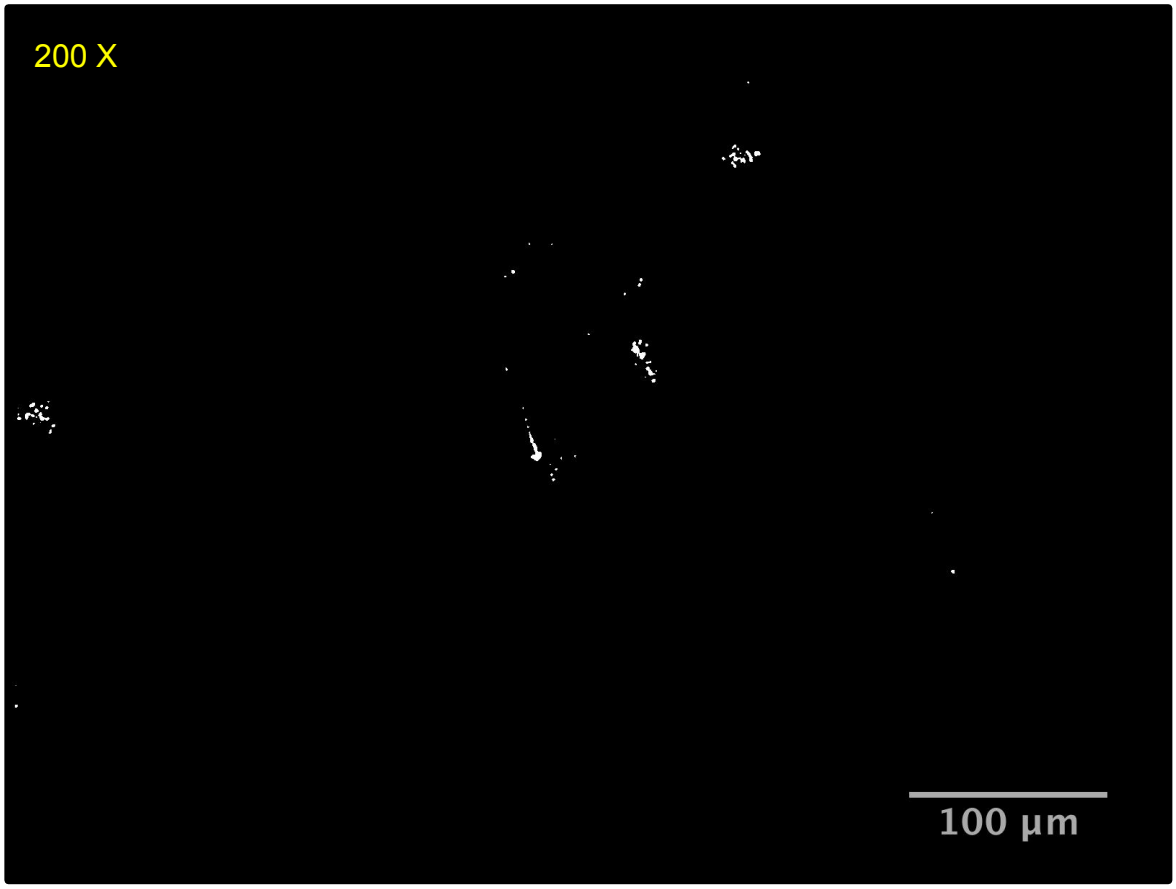

Figure 3. 4: pinholes in the same image shown in figure 3.3 after reduction to black and white using Fiji imaging software.

In order to find the total number of pinholes and the total pinhole area in each image, an image J software called FIJI [31] was used. First, the images had to be converted into black and white color images to isolate pinholes from actual film. Figure 3.4 shows the same image in figure 3.3 upon reduced to black and white to show pinholes and allowing counting pinholes and calculating total pinhole area in the image. A microscopic ruler (figure 3.5) allowed finding the scale of the microscope images at the corresponding magnification. This scale was then used in Fiji allowing automatic calculation of the area of all pinholes in each specific image in addition to counting the number of pinholes. In this specific image, there were a total of 58 pinholes occupying a

total pinhole area of about 196μm^2. The total image area is about 253,883 μm^2, and thus the pinholes would be occupying a fractional area of about 0.0007% of the total area of the film shown in the image.

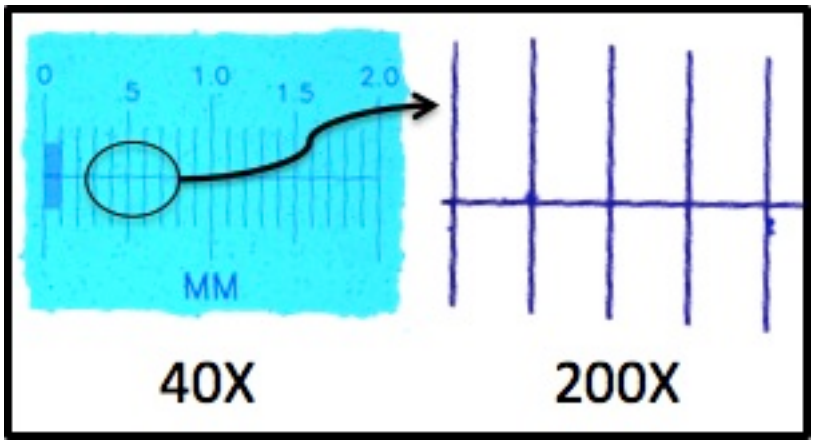

Figure 3. 5: A microscopic ruler that allowed obtaining the scale of the BLTM image.

3.1.2. Cleaning methods

As mentioned at the beginning of this chapter, three cleaning methods were studied to investigate artificial sources of pinholes. These are standard cleaning in open laboratory environment, cleaning within a class 1 mini-environment and plasma cleaning. A brief detail of each cleaning method is provided along with the justification for implementing these cleaning methods. Standard cleaning in open lab environment involves cleaning glass substrates in an ultrasonic washing machine with detergent, followed by rinsing by DI water and finally drying with isopropanol. This is the standard cleaning procedure implemented at the materials engineering lab at CSU.

Cleaning within a class 1 mini-environment on the other hand was developed due to the number of dust and particulates floating in open lab environment. Table 3.1 shows a comparison of the number of particulates and dust particles both in open lab environment as well as inside containment such as a class 1 mini-environment. From

this table, it was obvious that there were a lot of particulates floating in open lab environment and these could be collected on the glass substrates prior to film deposition and end up as sites where pinhole formation may occur. By using a class 1 mini-environment, the number of these particulates and dust particles was reduced significantly as shown in the same table.

Table 3. 1: Dust and particulates in open lab environment as well as within a mini-environment. The data was collected by Kegan Barricklow at CSU.

Location	Average particulate count (count/m^3)		
Particulate sizes (µm)	0.3	0.5	5
MEL Lab space	1.31e6	2.83e5	8.42e3
Inside mini-environment	56.5	28.2	0

Plasma cleaning on the other hand was used to verify if the glass substrates as received from the manufacturer had some residues that were not eliminated by standard cleaning. Plasma cleaning is based on the idea of implementing a wire-anode plasma discharge into a graphite source. This configuration allows maintaining low-pressure gaseous discharges at relatively low voltages (300-500V). Glass substrates are placed on top of this graphite source and plasma cleaning takes place by ion bombardment. This ion bombardment action removes residues or contaminants both by physical and chemical etching. [32]

Prior to plasma cleaning, glass substrates were cleaned with the standard cleaning procedure in open lab environment as described above. The plasma cleaner is attached to the load lock such that glass substrates are loaded into the load lock, transferred to the plasma cleaning station and then transferred to the ARDS for film deposition. The

entire process takes place under vacuum and the glass substrates were never allowed to come into contact with open lab environment prior to CdS film deposition. For the purposes of this experiment, TEC10 glass substrates were plasma-cleaned for 30 seconds with a discharge voltage of about 350V.

3.1.3. Statistics

A total of 80 CdS films were deposited on TEC10 glass substrates to test the hypothesis that CdS films of thicknesses ranging between 50nm and 200nm deposited on glass substrates cleaned with standard cleaning, cleaned within a class I mini-environment and cleaned with plasma have the same pinhole area. According to recommendations by the Statistics Lab at CSU, using five substrates per film thickness per cleaning method should provide valid statistical analysis. It was not possible to test this hypothesis for all film thicknesses and all cleaning methods by just one experiment due to the number of substrates involved and the fact that plasma cleaning was not available during the beginning of the experiment, so the hypothesis was divided into three experiments. These are:

1. Testing the hypothesis that CdS films deposited on substrates cleaned in open lab environment had equal pinhole area as those films deposited on substrates cleaned within the class 1 mini-environment. This test hypothesis allowed verifying if dust and/or particulates are a major source of pinholes in CSS CdS films deposited on TEC10 glass substrates. Three film thicknesses were considered: 200nm, 100nm, and 50nm. A total of 30 substrates were used for this experiment.

2. Testing the hypothesis that CdS films deposited on substrates cleaned in open lab environment had equal pinhole area as those films deposited on substrates cleaned within the mini-environment as well as films deposited on substrates that were plasma cleaned. This hypothesis allowed verifying whether addressing cleaning residues with plasma cleaning would help reduce and/or eliminate pinholes in CSS CdS films deposited on TEC10 glass substrates. Two film thicknesses were used: 200nm and 100nm. A total of 30 glass substrates were used for this experiment.
3. Testing the hypothesis that thin CdS films deposited on TEC10 glass substrates cleaned in open lab environment had equal pinhole area as those films deposited on plasma-cleaned TEC10 glass substrates. This experiment was conducted to study cleaning residues for thinner CdS films. Two film thicknesses were chosen: 70nm and 50nm. A total of 20 substrates per thickness per cleaning method were used for this experiment.

The overlap between film thickness and cleaning methods in the above stated experiments was based on the following. First, plasma cleaning was not available during the first experiment so only two cleaning methods were considered. The objective was to compare pinhole area on CdS films (200nm, 100nm and 50nm) deposited on TEC10 glass substrates cleaned by standard cleaning as well as TEC10 glass substrates cleaned within the mini-environment. When plasma cleaning became operational, the objective of the second experiment was to compare the three cleaning methods as well as the three CdS film thicknesses. Unfortunately this was not possible because the total number of CdS films would be 45 films and that number of CdS films

was not possible to make in one day in order to eliminate day-to-day variability. So only two film thicknesses were considered (200nm and 100nm) for the three cleaning methods. The last experiment was needed to compare pinhole area on thin CdS films (70nm and 50nm) deposited on TEC10 glass substrates cleaned with standard cleaning and plasma cleaning. Cleaning within the mini-environment was not considered in the third experiment based on the results of the first two experiments, which will be discussed in chapter 4.

3.1.3.1. Data Collection

A total of 27 images were recorded from each CdS film at pre-specified locations that were held the same across all 80 films. Images were collected at theses specific locations whether pinholes were observed or not. Figure 3.6 shows the layout of the glass substrate showing the area covered by the film (in gray color) and nine (1”x1”) squares within the substrate. The reason behind dividing the substrates into 9 squares is that normally when manufacturing CdTe devices, one small area device (SAD) is made at each of these 9 squares and thus each substrate had a potential of making nine SAD’s. The 27 blue light transmission optical microscopy images were recorded such that three images were taken at each of the nine squares where the distance between each of the three images was about 7mm. These images were then processed using Fiji. Finally, the collected pinhole area data was used to test the hypotheses stated earlier.

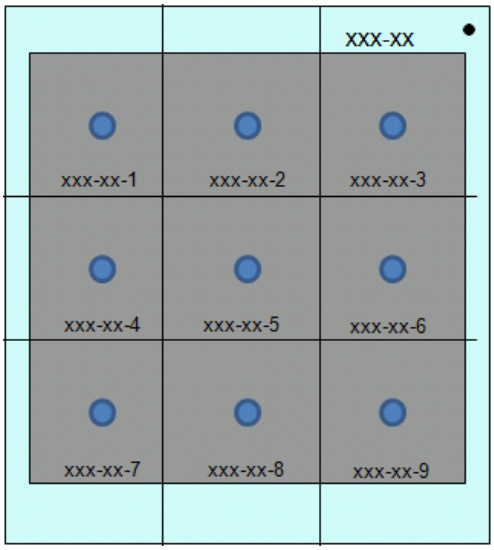

Figure 3. 6: An illustration of a glass substrate showing the nine locations of the substrate.

At first, the normal pinhole area scale was used but it turned out that the data had a very large skewness and the analysis of variance (ANOVA) could not be used on the original scale. In order to use ANOVA, three conditions have to be satisfied: independence of the data, equal variance of the dependent variable (area of pinholes) across all groups, and normal distribution of the dependent variable by checking skewness. The first condition was satisfied by the setup of the experiment but the remaining two conditions were not. Therefore, the pinhole area was transformed into a new scale to satisfy the remaining ANOVA conditions. This new scale was basically the natural logarithm of the pinhole area plus one [log(pinhole area+1)] as recommended by the Statistics laboratory at Colorado State University. The plus one part was added to account for images that had zero pinhole area. This transformed scale reduced skewness and variance significantly allowing the validity of the normal distribution assumption and the validity to use ANOVA to test the hypotheses considered.

3.1.3. SEM and EDS

Scanning Electron Microscopy is one of the most common surface morphology and characterization techniques reported in the literature. It can be used easily to verify surface morphology of the deposited film layers; it can also be used to distinguish various film properties like grain size and grain coalescence of different film thicknesses. Energy Dispersive X-ray Spectroscopy is used to obtain spectral imaging of film area being studied with SEM and provides elemental maps of different elements present in specific film areas. Combining SEM and EDS results in a powerful characterization tool that can be used to show pinholes and at the same time verify elemental composition in the film area being studied. This is especially useful to positively identify whether an observed feature is a pinhole or something else based on elemental maps detected by the software and also confirm whether a specific pinholes is caused by natural or artificial causes.

SEM and EDS were used to study the surface morphology of CdS films deposited by closed space sublimation on TEC10 glass substrates cleaned with standard cleaning in open lab environment. The objective of this experiment was to show pinholes in CdS films and verify that they are indeed pinholes. Moreover, it was a perfect tool to look for the natural causes of pinholes (grain coalescence and TCO surface roughness) and verify whether these natural causes are indeed sources of pinholes in CSS deposited CdS films. A wide range of CdS film thicknesses were studied, these thicknesses were: 200nm, 100nm, 50nm and 30nm. This range of CdS film thicknesses was chosen investigate the natural sources of pinholes in very thick CdS films (200nm) as well as very thin CdS films (30nm).

3.2. Pinhole Effects

Two effects of pinholes are of interest, these are area effects of pinholes and the effect of different fraction of pinholes area on V_{OC}. There has been no work sited in the literature up to the date of printing this thesis that investigated the size effect of pinholes in CdS films. Considering the cleaning methods used to test the different hypotheses outlined earlier in addition to an understanding of pinholes size effect, it would be possible to further understand the role of pinholes in CdS films and the reason behind the need to reduce/eliminate pinholes in CdS films. The problem was observing pinholes in complete devices. As discussed before, pinholes can be clearly identified by BLTOM and SEM in CdS only films. But when the device is complete, there was no means by which pinholes could be identified without damaging the device by either method.

Instead it was necessary to observe a pinhole or pinholes in a completed device somehow and then assess the effects of those pinholes by any means possible. Indeed, this was achieved by using Light Beam Induced Current (LBIC) scans combined with Electroluminescence (EL). In addition, 2D PSpice® [33] models were used to simulate the effect of different sizes of pinholes on the open circuit voltage of the device as well as the effect of these different pinhole sizes on the diode voltage profile of the device.

3.2.1. LBIC and EL

According to a paper by Brooks et al. in 2011 [34], it is possible to visualize defects such as pinholes in completed devise using LBIC with different wavelengths. According to the authors, photons have different penetration depths corresponding the laser beam wavelength as shown in figure 3.7. This technique allowed observing pinholes within the

window material as regions of high response at 405nm. The same pinholes would appear as regions with very low response at 658nm laser wavelength. Thus, it would be possible to observe pinholes in a complete device using LBIC with two different laser beam wavelengths. Indeed this was done using a 638nm and a 405nm laser wavelengths to look for pinholes. Moreover, LBIC scans provide an actual size of the defect being scanned. Therefore, combining LBIC with another device analysis technique such as EL allowed determining the size effects of pinholes. This was achieved by determining the sizes of the defect in the LBIC 405nm laser wavelength scan as well as EL by using Fiji. Thus, finding the ratio between the two images can be achieved provided the scale of both techniques is known.

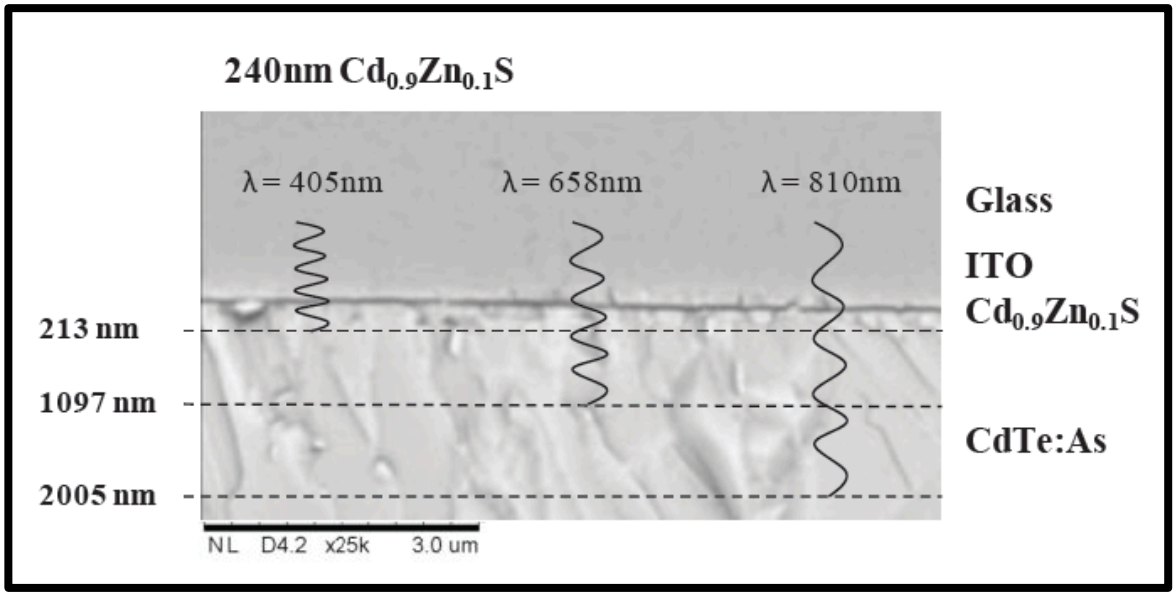

Figure 3. 7: Photon penetration depths as shown in a cross-sectional SEM image of a CdZS/CdTe device. [33]

3.2.2. 2D PSpice® Model

A PSpice® 2D model was developed by Koishiyev in his PhD dissertation to study the effects of shunts and weak diodes [21]. With reference to that 2D model and the book “Modeling Photovoltaic Systems Using PSpice®” by Castaner [35], a 2D PSpice® model was built to simulate the effects of different fractions of pinhole area of the open circuit voltage of the solar device. A 2D model involves simulating the device in both x and y directions and thus allowing obtaining more accurate simulation results as well as surface profiles of the device as the fraction of pinhole area is varied. This model simulates a small area device (SAD) having an area of $1cm^2$. The model had 21x21repeating units where each unit had the basic elements required to simulate the solar cell. These elements are: a diode to simulate the p-n junction of the device, a resistance R to simulate the sheet resistance of the TCO and current source. The entire model is connected to a voltage source in order to measure the open circuit voltage for each specific fraction of pinhole area being considered. Figure 3.8 shows a schematic of the elements of the repeating unit. The conductance G was omitted in this study since it is usually used to simulate the effects of shunts in solar cells and this is beyond the scope of this work. Figure 3.9 shows a general representation of the 2D model with the red diode in the middle as the weak diode. In this case, the dimensions L and W represent the length and width of the device being simulated and both equal 1cm. M and N are dimensionless numbers indicated the number of units in the model in each direction which is 21. The parameter a represents the length and width of the area occupied by each repeating unit, about 0.05cm.

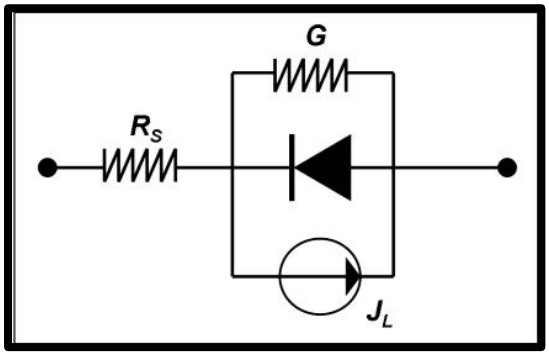

Figure 3. 8: Basic elements of the subcircuit. [21]

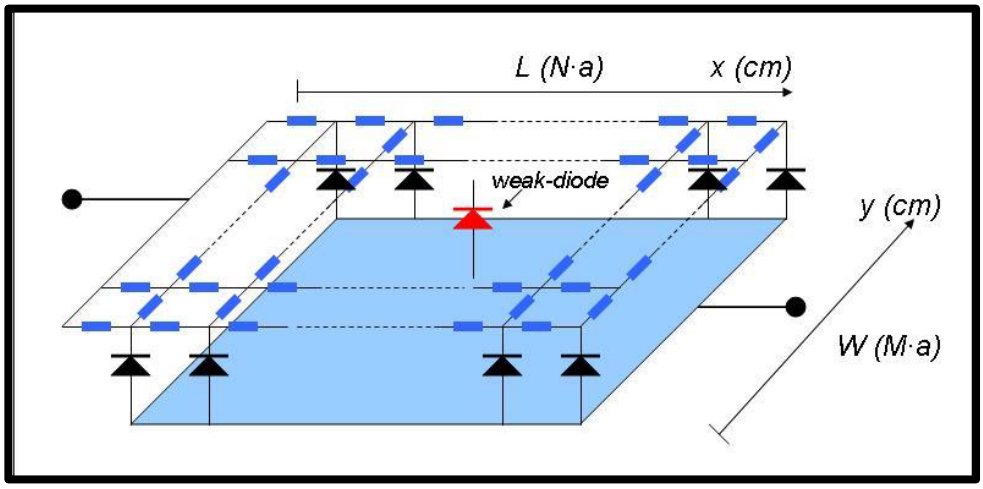

Figure 3. 9: A general representation of the 2D model including the weak diode at the center as shown in red. [21]

The weak diode (red diode) shown in figure 3.9 is used to simulate pinholes. As discussed before, discontinuities in the CdS film allow the formation of the CdTe/TCO weak diodes. Weak diodes tend to reduce the open circuit voltage of the device. The diode value in the PSpice® model depends on three factors: the saturation current density Jo, the area of the diode (A) and the quality factor of the diode (N). In order for the PSpice® model to be used to simulate devices made at the materials engineering laboratory, Jo for both the good diode and the weak diode were to be calculated from actual devices made at the lab. The open circuit voltage V_{OC} and the short circuit

current J_{SC} are two variables required to calculate Jo as indicated in equation 3.1. Two devices were used for this purpose; the first device was a complete CdS/CdTe device made with the best process conditions at the time of the experiment to obtain the best V_{OC} and J_{SC} in order to calculate Jo for the good diode (assuming that CdS in this device had no pinholes). The other device on the other hand was a device with the same exact deposition conditions as the complete device except that it had no CdS to obtain V_{OC} and J_{SC} required to calculate Jo for the weak diode. Table 3.2 shows the parameters of both the good and weak didoes. Finally, by changing the area of the diode in the PSpice® model and keeping the total device area constant, one can simulate the effects of a wide range of pinhole fraction areas.

$$J_O = e\left(\frac{q}{AkT \cdot V_{OC}}\right) \cdot J_{SC} \qquad (3.1)$$

Table 3. 2: Good diode and weak diode parameters

	V_{OC} (mV)	J_{SC} (mA/cm^2)	Jo (mA/cm^2)
Good diode	775	20	6.3 e-6
Weak diode	190	20	0.45

Two experiments were conducted; the first was to simulate devices with different fractions of pinhole area to account for the effects of specific sizes of pinholes on the open circuit voltage. The results were compared to those published in the 1998 NREL IEC report [13] as shown in table 2.3 in the previous chapter. In addition to the simulation, a MATLAB® mathematical model was built for the same purpose. This mathematical model used the V_{OC} loss equation (equation 2.3 in chapter 2) with the parameters of the saturation current density Jo for devices made in the lab. This allowed plotting a graph of the open circuit voltage as a function of the fraction of pinhole area and thus the ability to compare experiment results to those of the 1998

NREL IEC report as well as the PSpice® simulation model. This was used to verify whether the V_{OC} loss equation in the mentioned report is indeed valid for CdS films made in the lab.

The other experiment was conducted to obtain the diode voltage profile across the model for each F being considered. This allowed gaining a perspective of the range of effects of the weak diodes for each F being used, essentially providing an idea of the size effects of pinholes through PSpice simulation. Moreover, it would give an idea of what would be the smallest fraction of pinhole area that would significantly affect the solar cell.

Thus, outlined in this chapter the methodology was used in this dissertation. Sources of pinholes and related work will be presented in chapter 4. Both the natural and artificial sources of pinholes were studied and ways to eliminate/reduce some of these sources are tested by means of statistical hypotheses tests. On the other hand, pinhole effects and fraction of pinhole area simulations using PSpice® are presented in chapter 5. That chapter will discuss pinhole effects based on methods outlined within this chapter in addition to discussing the effectiveness of PSpice® simulations and MATLAB® models to predict the open circuit loss due to pinholes in CdS films according to the model reported in [13].

Chapter 4

Sources of Pinholes

The sources of pinholes discussed in chapter 2 and shown in figure 2.12 above are divided into natural and artificial sources. The natural sources of pinholes are grain coalescence and TCO surface roughness. On the other hand, artificial sources of pinholes are classified into scratches, scuffing marks, dust and/or particulates in open lab environment and cleaning residues. This chapter is focused onto studying these sources of pinholes in CdS films deposited on TEC10 glass substrates to identify these sources of pinholes and possibly eliminate them. The methods by which this objective was achieved were discussed in chapter 3. Thus, the outcomes of the methods outlined in chapter 3 are shown in this chapter. The chapter is divided into two parts; the first part was focused on investigating the natural sources of pinholes and the other part was focused on studying the artificial sources of pinholes.

4.1. Natural Sources of Pinholes

CdS films deposited on standard cleaned TEC10 glass substrates of four film thicknesses: 200nm, 100nm, 60nm and 30nm were used for studying the natural sources of pinholes. Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Spectroscopy (EDS) were used to study pinholes in the CdS films, obtain spectral imaging of film area being studied with SEM and provide elemental maps of different elements present in that specific area. An example of an SEM image is shown in figure 4.1.

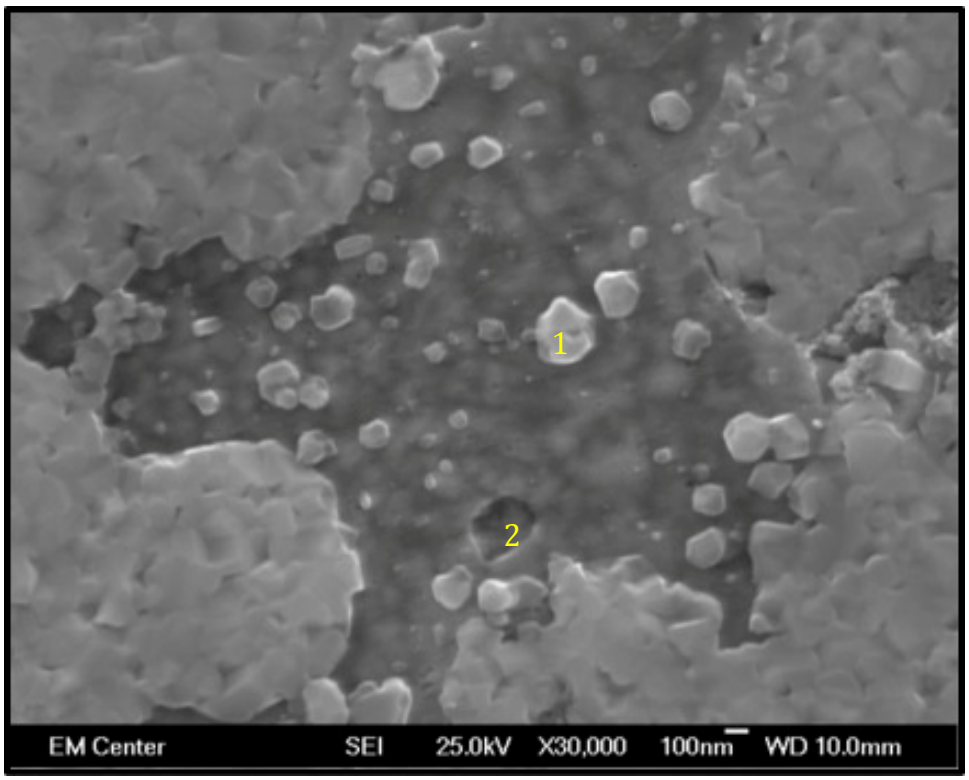

Figure 4. 1: SEM image of what appears to be a defect observed in a 100nm film.

4.1.1. Thinner CdS film

The feature shown in figure 4.1 above in a CdS film 100nm thick was thought of as being a pinhole. In order to confirm whether the observed feature is a pinhole, EDS was used for further analysis. Figure 4.2 shows a spectral image of the elements present in figure 4.1, elements with higher peaks indicate the presence of higher atomic percentages of these elements. On the other hand, the overlap between the Cd/Sn and S/Pb peaks is due to the fact that the Kα and/or Mα weighted average energies of these elements being very close. Cadmium has Kα energy of 23.1keV and tin has Kα energy of 25.1keV. Sulfur on the other hand has Kα energy of 2.3keV and lead has Mα1 energy of 2.3keV. The atomic percentages of the elements present in the feature in figure 4.1 are shown in figure 4.3. Based on figures 4.2 and 4.3, one can conclude that the

elements of the window layer (Cd and S) are present and accounted for in the SEM image in figure 4.1 but that does not show if there any areas that have more or less concentrations of Cd and S. In order to do that, EDS can be used to obtain elemental maps of the chemical elements present as shown in figure 4.4. Thus as shown in figure 4.4, there is a dark area in Cd and S maps that looks exactly as the feature shown in figure 4.1, this means that the atomic percentages of both Cd and S within these dark areas are much less than everywhere else. This is a clear indication that the SEM image in figure 4.1 shows an area of the CdS film that is thinner than original film thickness.

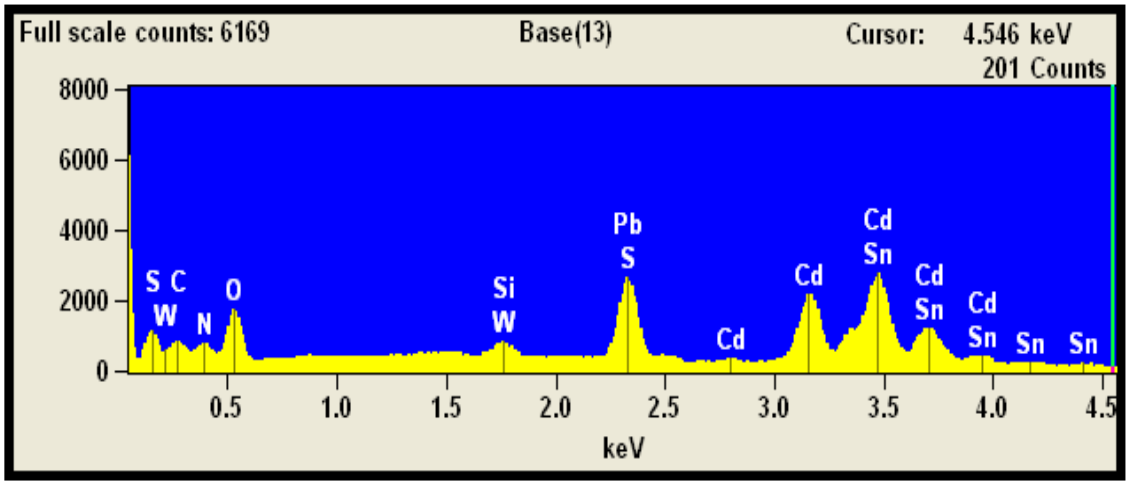

Figure 4. 2: Spectral image of the film area shown in figure 4.1.

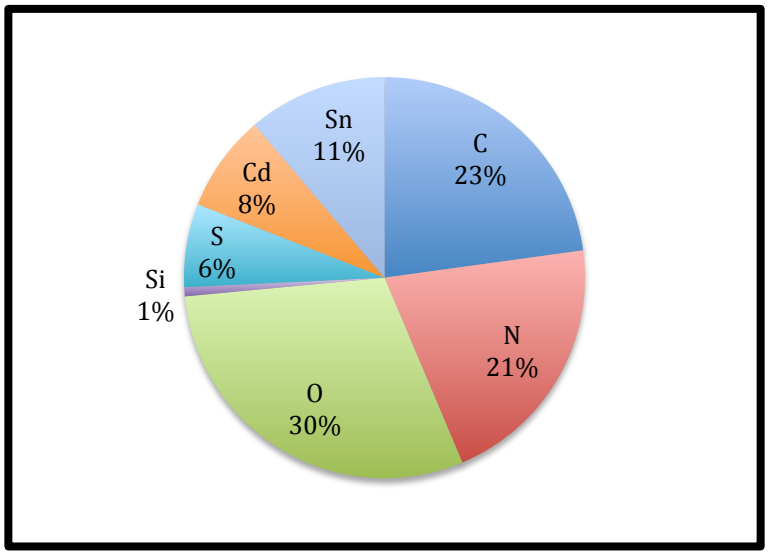

Figure 4. 3: Atomic percentages of elements detected by EDS on feaure in figure 4.1.

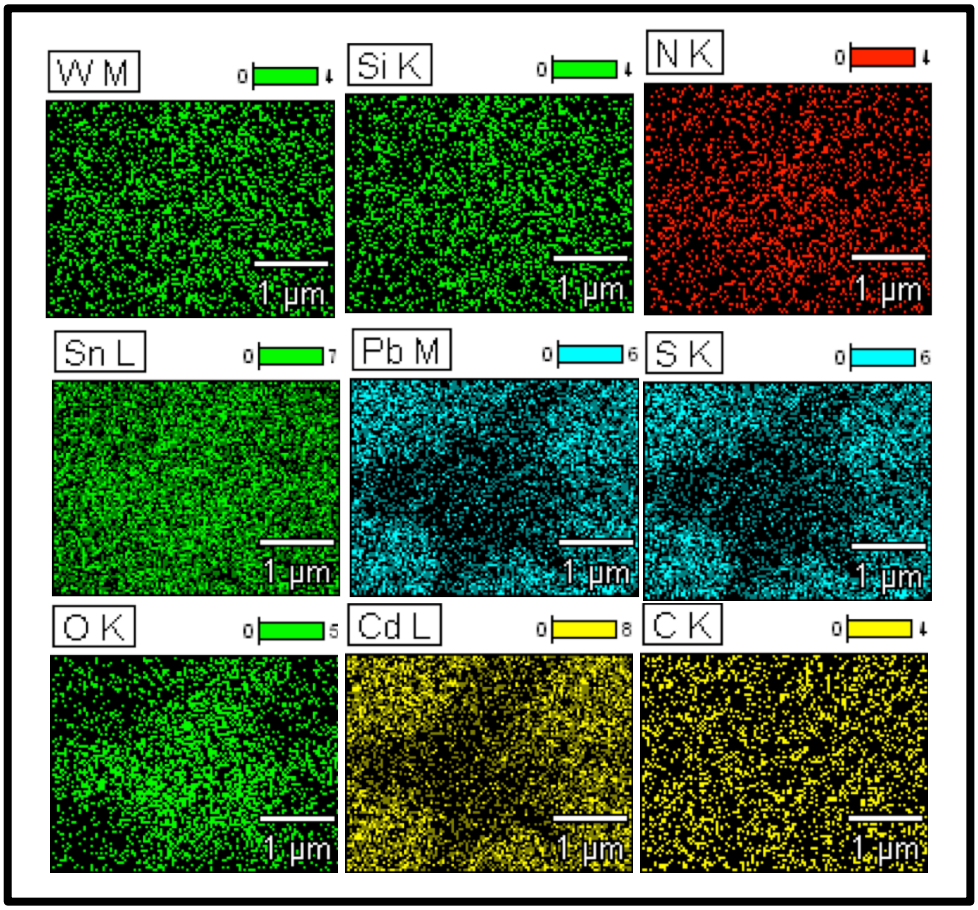

Figure 4. 4: Elemental maps of different element in the film area shown in figure 4.1 above, notice the dark areas in sulfur and cadmium maps.

The high atomic percentage of tin (Sn) as well as oxygen and the presence of silicon (Si) can be explained by the electron penetration depth of the EDS analysis. Both the SEM images and EDS analysis are done at a specific acceleration voltage in kV. The EDS analysis of the feature in figure 4.1 was done at an acceleration voltage of 10kV. The SEM image itself was taken at 25kV for the purposes of image clarity. The spectroscopy done by EDS tends to penetrate the film being analyzed in a tear-like pattern as shown in figure 4.5. The higher the acceleration voltage, the more electrons reach the bulk of the material and hence detecting higher concentrations of the bulk material. At the same time, fewer electrons detect the surface material and hence EDS shows less atomic weight of those materials at the surface. This can be shown by a Monte Carlo simulation of electron trajectory in solids [35] called CASINO, electrons distribution at 10kV is shown in figure 4.5 and electrons distribution at 25kV is shown in figure 4.6. For the sake of comparison purposes, the depth of the material shown in both images is kept constant to show the effects of the higher acceleration voltages. Thus, it is clear that acceleration voltage of 10kV or less will detect more surface materials and as the acceleration voltage increases, more of the bulk material is detected.

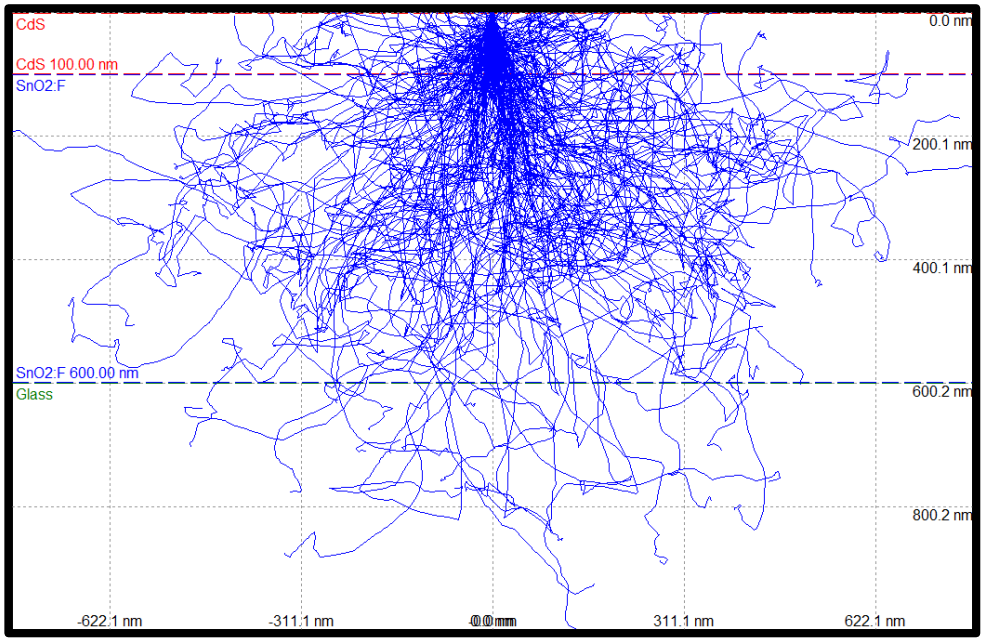

Figure 4. 5: Electron penetration in a CASINO simulation for a 100nm thick CdS film at an acceleration voltage of 10kV.

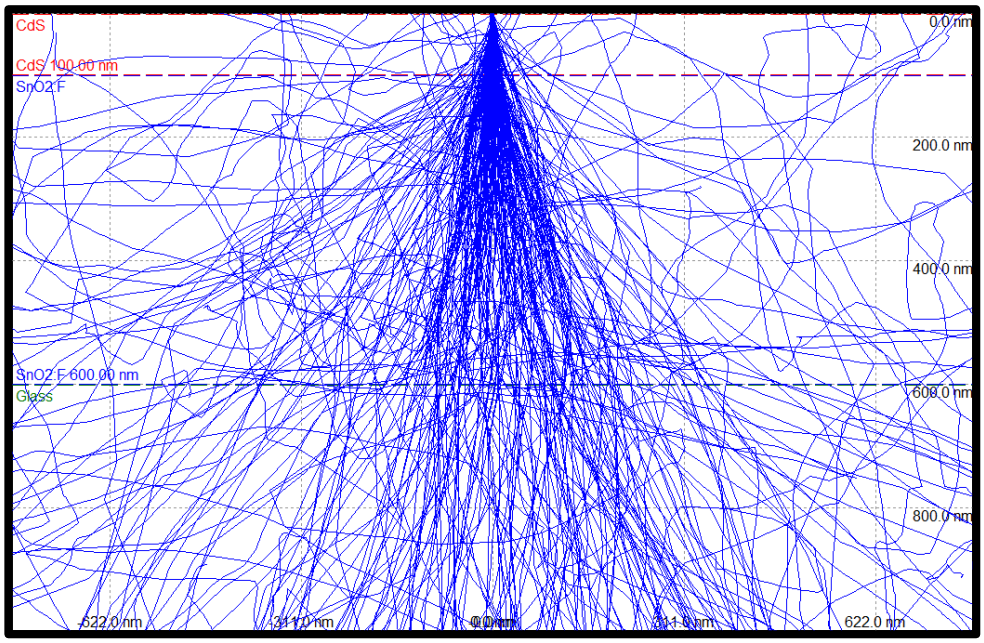

Figure 4. 6: Electron penetration simulation at an acceleration voltage of 25kV for a 100nm thick CdS film.

The SEM image in figure 4.1 can be analyzed further. There are a few interesting areas in that figure that seem to look like isolated islands of CdS and some others that look like either a thinner CdS film or even a pinhole going all the way down to the TCO. These areas are shown in figure 4.1 as spots 1 and 2 simultaneously. Spot 3 is chosen for comparison purposes. EDS has a spot analysis tool with a beam radius of 10nm that can be used to identify the materials present in such sites.

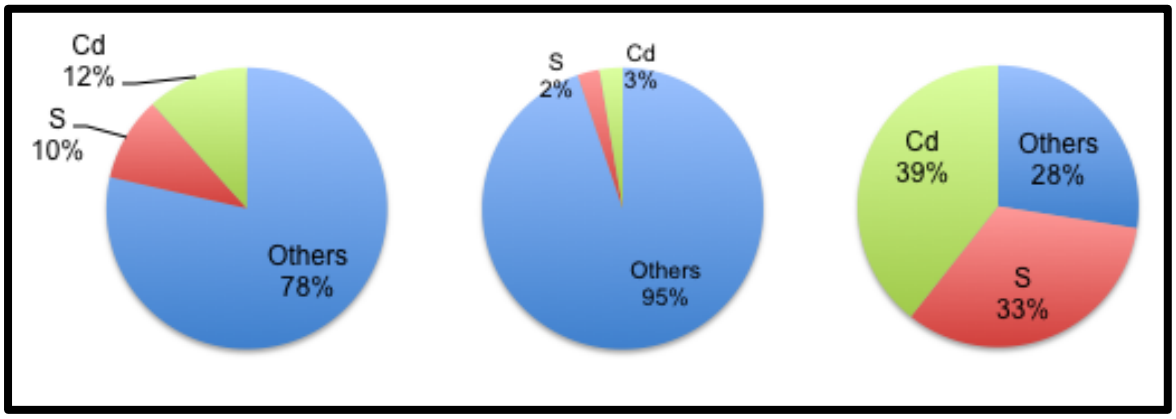

Figure 4. 7: Atomic percentages of elements present in the three spots shown in figure 4.1. Spot 1 in the left, spot 2 in the middle and spot 3 on the right.

Figure 4.7 shows a pie chart of the three spots shown in figure 4.1 with the corresponding atomic weights of elements present at each spot. The pie chart on the left shows element detected at spot 1, the pie chart in the middle shows elements detected at spot 2 and the pie chart on the right shows elements detected at spot 3. Based on that, it is clear that spot 1 that looks like an island of thick CdS in figure 4.1 is an area that is not as thick as the original film thickness (spot 3) but also not as thin as the entire feature shown in the same figure. Also, Spot 2 is an area where the film thickness is further reduced but it is still covering the TCO. If indeed a pinhole were

present at this specific location, one would expect EDS not to identify any Cd or S and show mainly tin and oxygen.

4.1.2. A Pinhole

Another example of the CdS film surface features studied with SEM images is shown in figure 4.8 at 10,000X. Increasing the magnification to 30,000X as shown in figure 4.9 shows more details of the feature and also shows what looks like TCO grains at the center of the feature. In addition, the nucleation of the CdS film in figure 4.9 is also evident, it seems that more film growth was occurring moving away from the center of the defect. The method of studying and further identifying this feature was done in the same manner detailed in section 4.1.1.

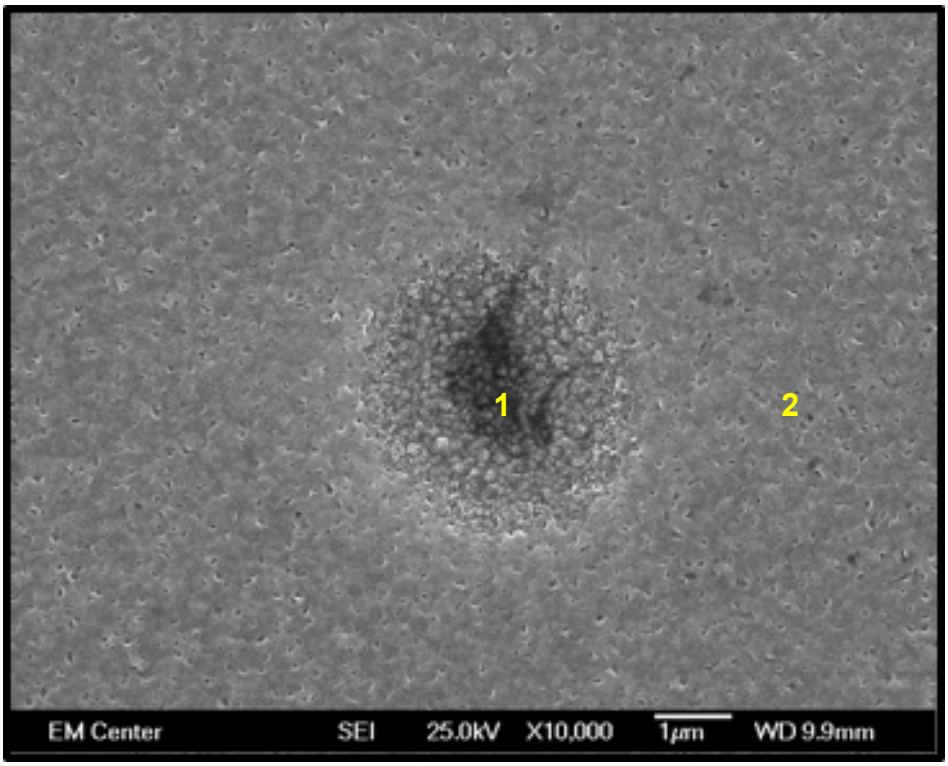

Figure 4. 8: SEM image of a pinhole in a 100nm CdS film.

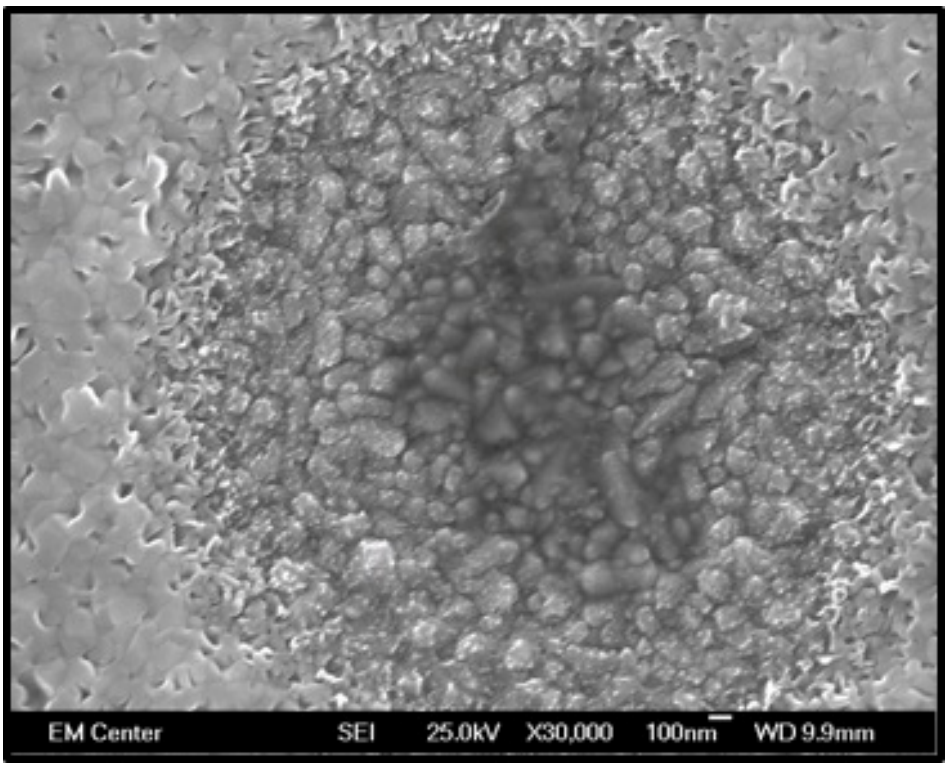

Figure 4. 9: The same pinhole shown in figure 4.8.

Similarly to what was done before, EDS analysis of the entire image as well as some spots (1 and 2 in figure 4.8) within the image was accomplished to find whether what is shown in these SEM images is indeed a pinhole. The elemental maps of Cd, S, Sn and O are shown in figure 4.10. The corresponding atomic weight percentages of these elements are shown in the pie chart on figure 4.11. Moreover, EDS spot analysis was done on two spots, the first is a spot inside the feature and the second spot is within the surrounding CdS film. The locations of these two spots are shown in figure 4.8 above and the corresponding pie charts of the elements present at these two spots are shown in figure 4.12 below.

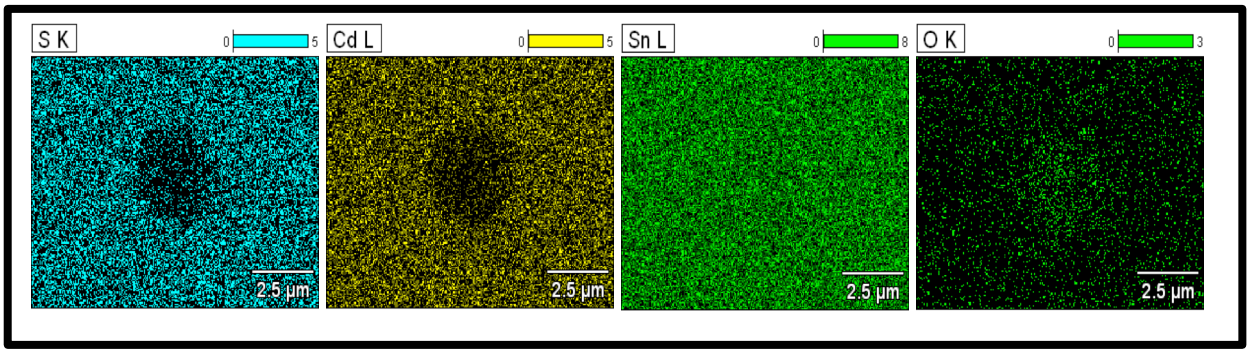

Figure 4. 10: EDS maps of elements of interest that are present in the SEM image shown in figure 4.8.

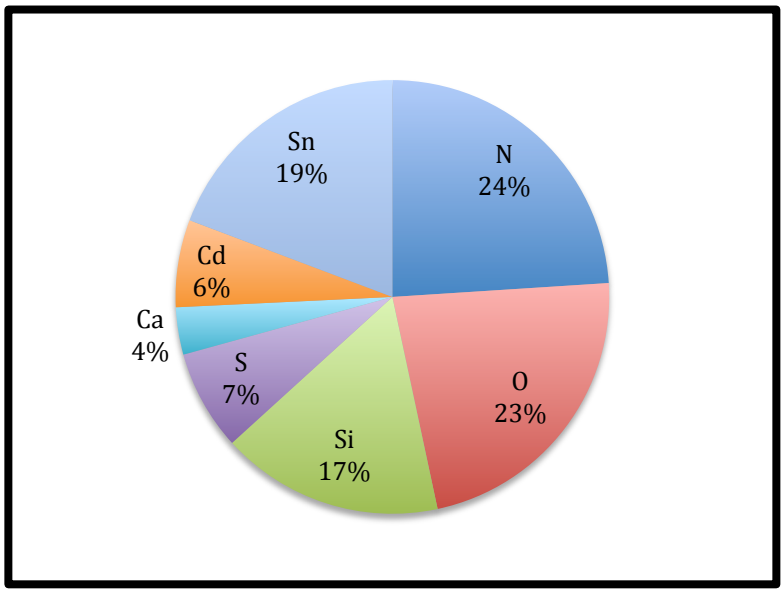

Figure 4. 11: Weight percentages of elements present in figure 4.8 above.

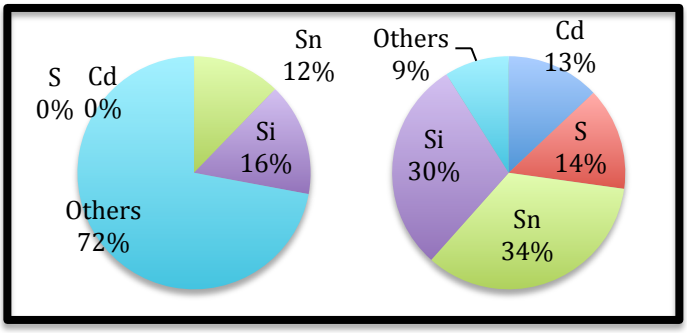

Figure 4. 12: Elements present at spots 1 and 2 in figure 4.8 above and their corresponding atomic weight percentages.

Based on the EDS analysis done and figures 4.10 and 4.12, it was concluded that the feature in figure 4.8 was indeed a pinhole. The way the pinhole was formed was interesting, it seems as if there was some sort of a dust particulate that was still occupying this specific area of the TCO when film deposition started. As more film growth was occurring, this particulate was removed allowing late film growth on the surrounding areas while leaving the TCO surface exposed and thus forming a pinhole. This is evident based on the presence of TCO grains at the center of the defect and the outward grain nucleation of the film. Thus, this was an indication that improving the cleaning methods and may be eliminating dust and particulates from being collected in the substrates may help reduce pinholes in the films. The feature shown in figure 4.8 is an example of a pinhole as observed in scanning electron microscopy, some similar pinholes were observed as well.

4.1.3. Grain coalescence and TCO roughness

Pinholes can occur naturally in CdS films mainly due to grain coalescence and TCO surface roughness as discussed in chapter 2. These two natural sources of pinholes were investigated in this study with SEM and EDS. In the same way the features in sections 4.1.1 and 4.1.2 were studied, the four film thicknesses (200nm, 100nm, 50nm and 30nm) were investigated for any indication of these natural sources of pinholes. SEM images of these CdS films as well as the TCO are shown in figures 4.13 to 4.17.

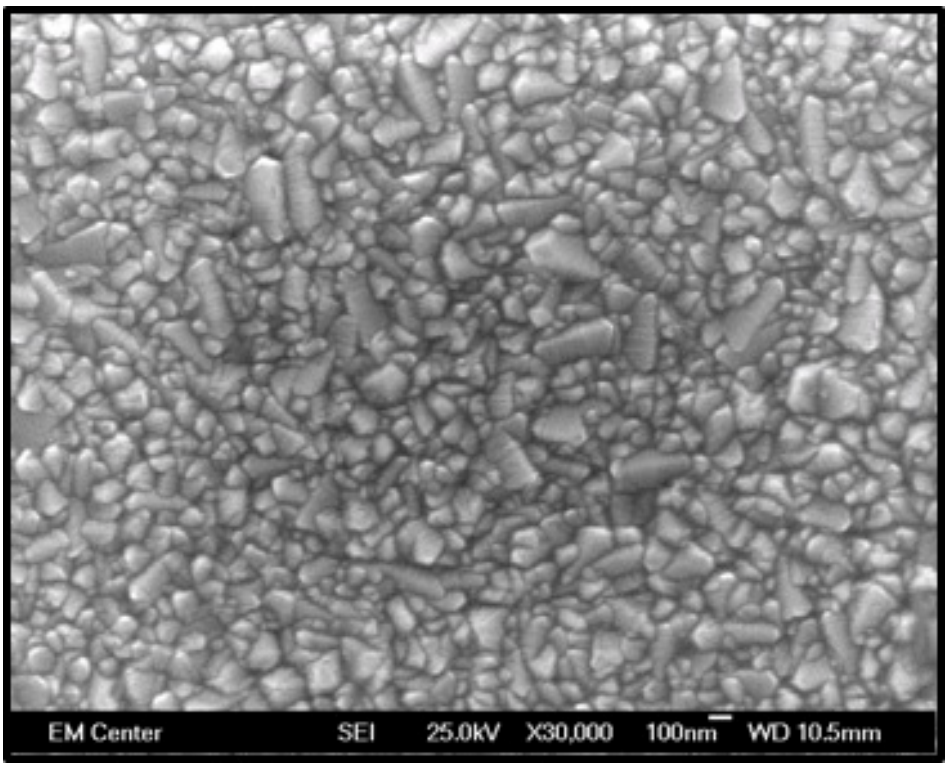

Figure 4. 13: SEM image showing the TCO grains on the surface of the substrate.

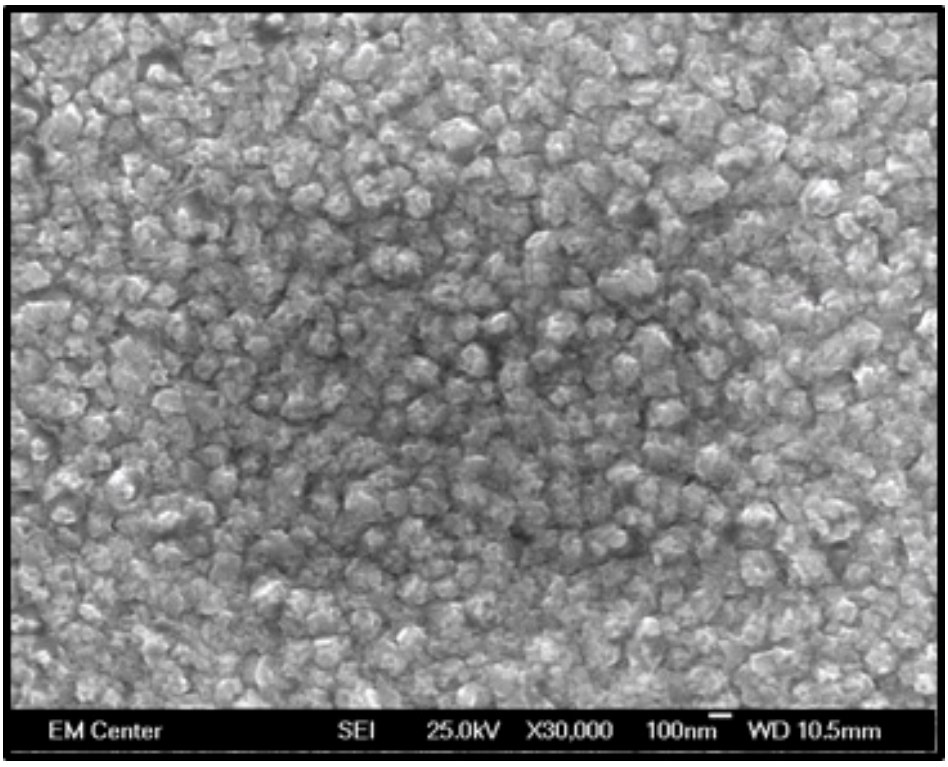

Figure 4. 14: SEM image of a 30nm CdS film.

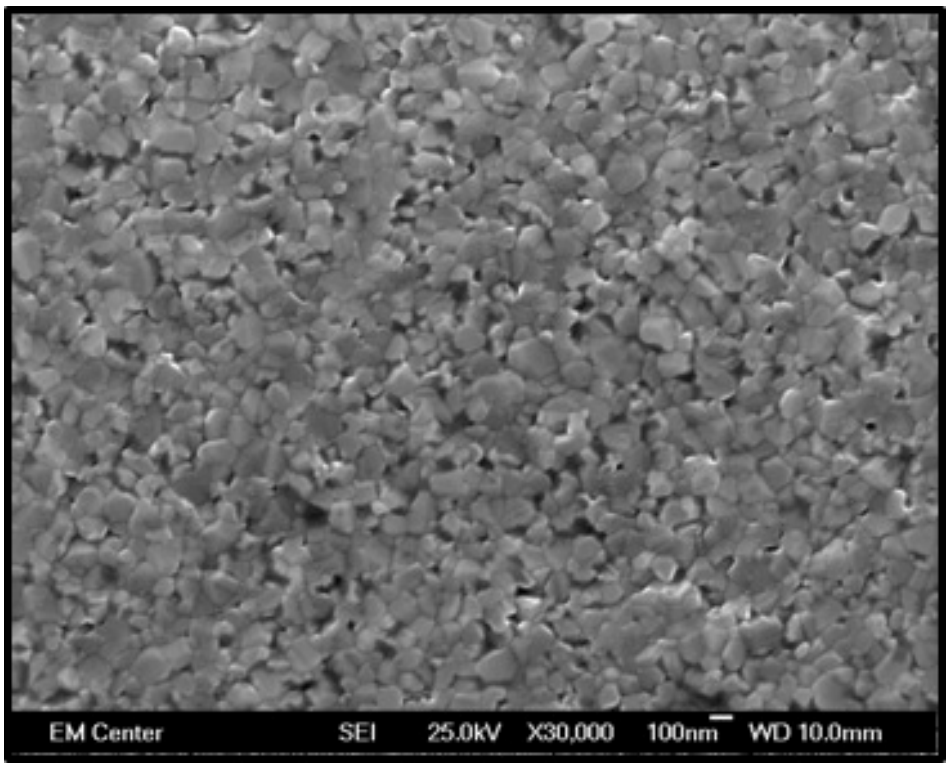

Figure 4. 15: SEM image of a 50nm CdS film.

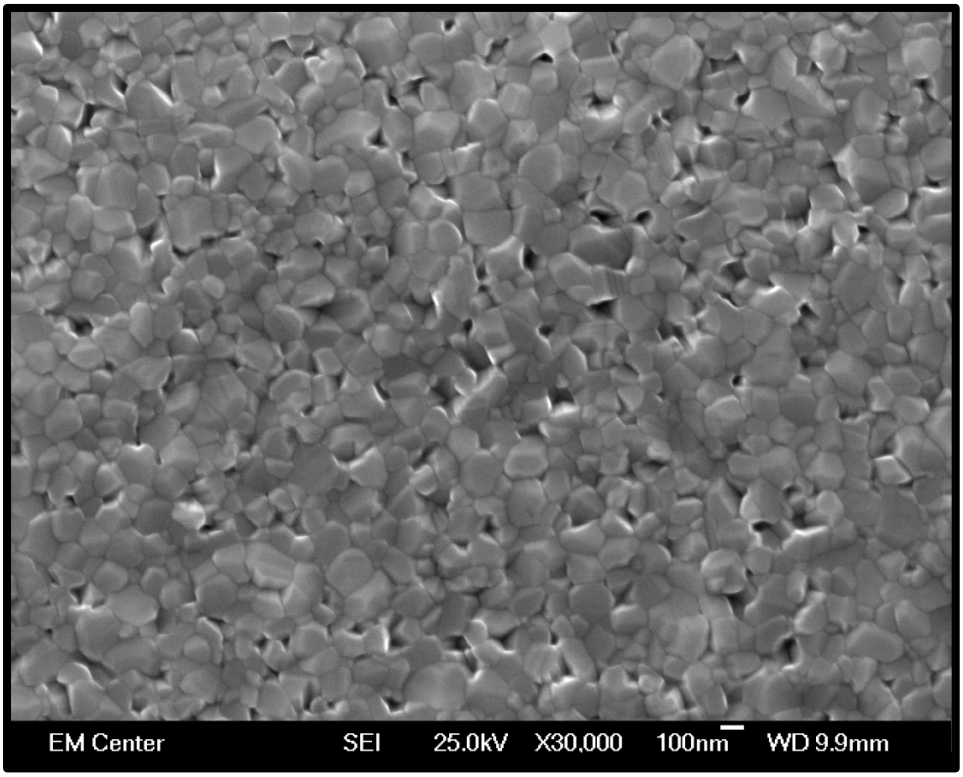

Figure 4. 16: SEM image of a 100nm CdS film.

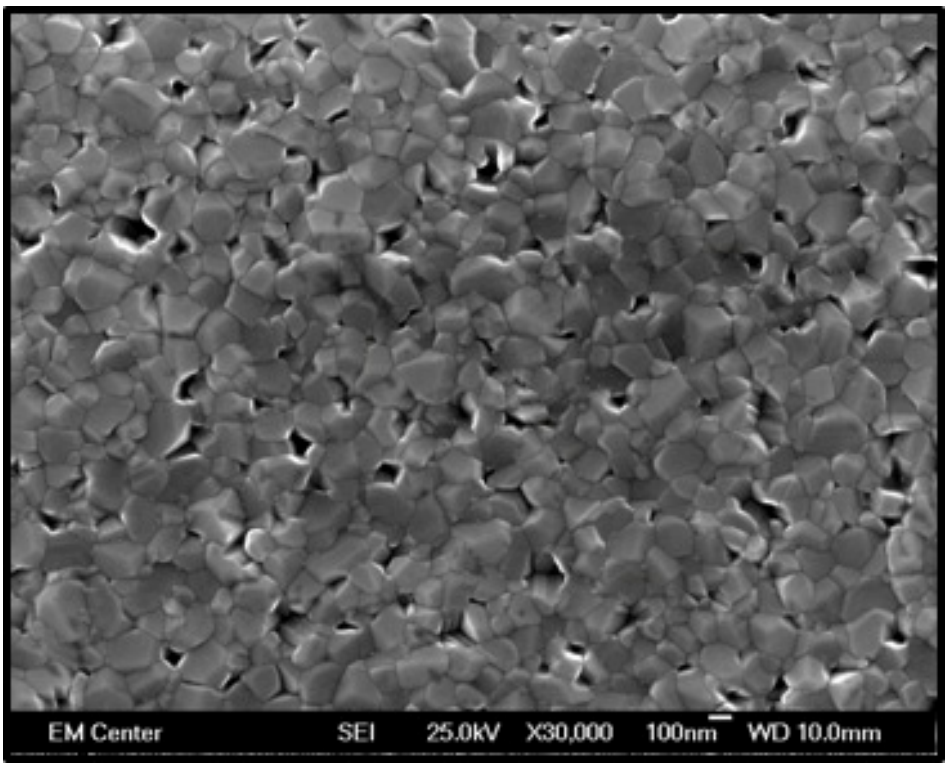

Figure 4. 17: SEM image of a 200nm CdS film.

These SEM images of the CdS films shown above for all the film thicknesses were free from the natural sources of pinholes. Grain coalescence was evident in all film thickness and there were no empty spaces between the grains that expose the underlying TCO surface allowing the formation of pinholes even for the least CdS thickness. The dark spots in figure 4.17 in the 200nm film were spaces among the grains of the top layer of the CdS film, EDS analysis revealed that the entire region even those dark spots are regions of CdS film. Even spot analysis at these specific spots did not show any lack of Cd or S indicating that there are layers of the film underneath these spots and a pinhole reaching all the way to the TCO was never formed. This was also true for the 50nm and 100nm film thicknesses. The SEM image in figure 4.14 shows a feature in a 30nm CdS film; even at 30nm, full film coverage was achieved and the TCO layer was never exposed.

Moreover, TCO surface roughness was also non evident. SEM images did not show any feature that looked like a peak of TCO coming through CdS films. EDS spectral analysis of the entire film areas as well as spot analysis did not show any region that had zero atomic percentages of Cd and S further indicating that there were no TCO peaks within the CdS film due to the TCO surface roughness. It is therefore clear that the grain coalescence and TCO surface roughness are not sources of pinholes in CdS films deposited by close space sublimation using the ARDS at the materials engineering lab. These natural sources of pinholes may occur in CdS films deposited with other deposition techniques.

4.2. Artificial Sources of Pinholes

The artificial sources of pinholes as indicated before are divided into: scratches, scuffing marks, dust and/or particulates in open lab environment and cleaning residues. Scratches and scuffing marks were observed in early samples and were due to film handling after deposition. The substrate handling procedures post film deposition were improved and these sources of artificial pinholes were not observed again. The remaining two sources of pinholes required more experiments and a systematic approach in order to further study these sources and possibly eliminate them. The issue of air and dust particulates floating in open lab environment was addressed via utilizing a class 1 Mini-environment where TEC10 glass substrates were cleaned within this containment and never allowed to come into contact with open lab environment. On the other hand, cleaning residues were addressed utilizing plasma cleaning where TEC10 glass substrates were cleaned with plasma and then CdS film deposition takes place immediately afterwards.

Neither BLTOM nor SEM and EDS can be used to identify these two sources of pinholes. Therefore, it was important to utilize a different technique by which films deposited on substrates cleaned by the different cleaning methods can be studied. This was achieved by conducting a statistical study. As indicated in chapter 3, pinholes occurring on CdS films deposited on substrates prepared by three cleaning methods were compared on four CdS film thicknesses. Three statistical experiments were conducted to test the hypothesis that the pinhole area in CdS films deposited on substrates cleaned with standard cleaning, cleaning within the mini-environment and plasma cleaning are equal. Appendix A shows images of CdS films of different thicknesses deposited on substrates cleaned with standard cleaning in open lab environment, substrates cleaned within the mini-environment and substrates plasma cleaned. These images have been reduced to black and white images to emphasize and show pinholes.

4.2.1. Mini-environment vs. Standard cleaning

A total of 30 films deposited on 30 TEC10 substrates were used for the purpose of this experiment. Three film thicknesses were considered: 200nm, 100nm and 50nm. Based on recommendations from the Statistics laboratory, 5 substrates per film thickness per cleaning method were used. Upon depositing the CdS films, pinholes and film areas were observed and recorded on 27 pre-specified locations as described earlier. The pinhole count, pinhole area and average pinhole area in all CdS films corresponding to each film thickness and cleaning method are shown in table 4.1. In this table, the pinhole count and pinhole area are the total number of pinholes and total pinhole area observed in five CdS film of the same film thickness and deposited on

substrates cleaned with the same cleaning method (135 images per film thickness per cleaning method). The average pinhole area on the other hand is the average pinhole area per image across these 135 images. The hypothesis being tested in this section is: CdS films deposited on substrates that were standard cleaned have the same pinhole area as those films deposited on substrates cleaned within the mini-environment.

Table 4. 1: Pinhole count and pinhole area from FIJI for the first experiment.

Film Thickness	Cleaning method	Pinhole count	Pinhole area (μm^2)	Average pinhole area (μm^2)
50nm	Standard	3,325	1,993	14.76
50nm	Mini-environment	3,261	2,458	18.21
100nm	Standard	7,898	22,480	166.52
100nm	Mini-environment	6,410	6,039	44.73
200nm	Standard	3,373	5,435	40.26
200nm	Mini-environment	19,598	55,838	413.62

Boxplots of the pinhole area data are shown in figure 4.18 below. These boxplots did not show any whiskers, the data was clustered within a vey small range and there was with a lot of extreme outliers indicated by stars. A more detailed explanation of statistics terms and plots used in this study is provided in appendix B. Moreover, looking at the skewness of the data, the pinhole area is extremely skewed which defies the conditions of ANOVA. So, to account for data skewness and show more meaningful boxplots, a scale transformation of the pinhole data was required. The best suitable transformation scale was found to be adding the quantity of pinhole area of $1\mu m^2$ to account for the images that had zero pinhole area and then applying a log scale to the to data. In other words, using the following scale: log(pinhole area +1). Upon scale transformation, the boxplots (figure 4.19) look more meaningful and the skewness of the data was reduced

from 23.2 to 0.9. The numbers on these figures correspond to observation numbers. For example, the number 725 on the top right corner in figure 4.18 corresponds to observation number 725.

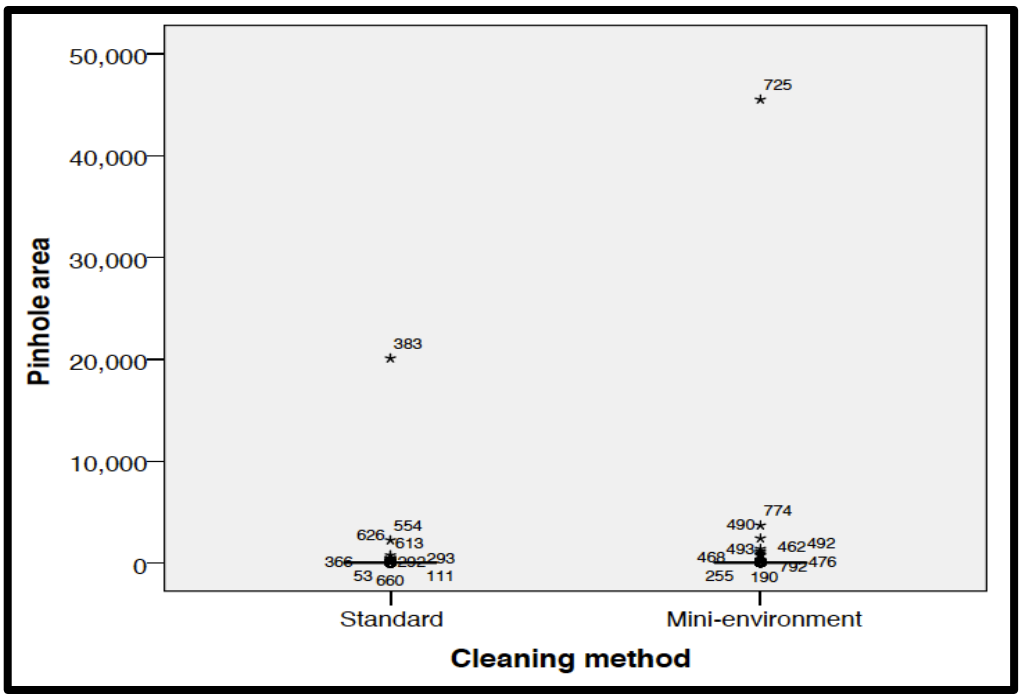

Figure 4. 18: Box plots of the pinhole area according to cleaning method.

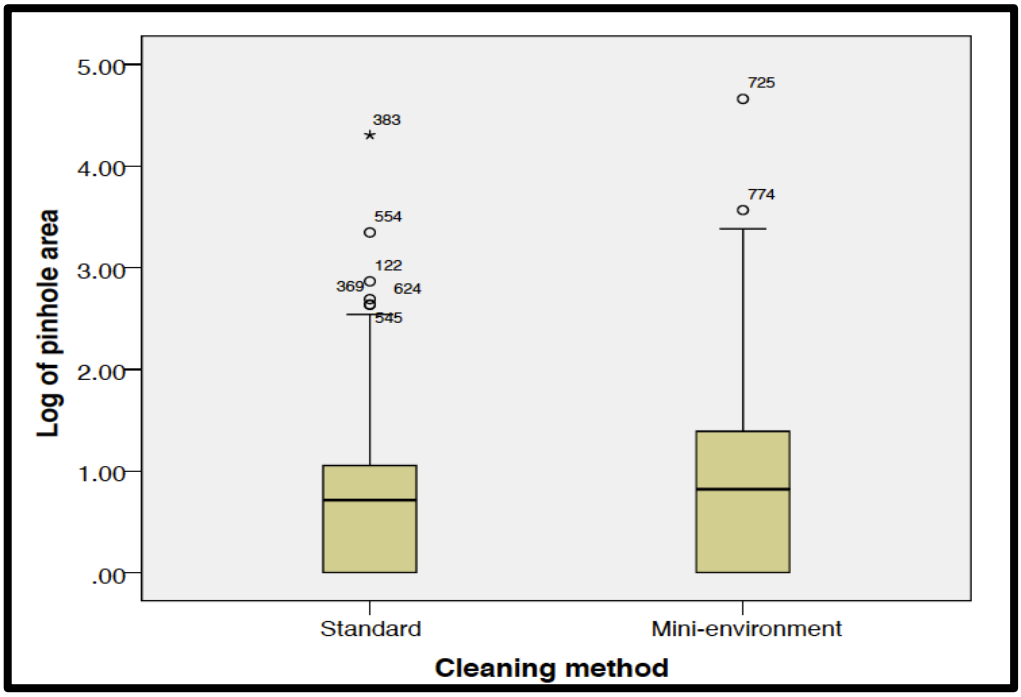

Figure 4. 19: Box plots of the transformed scale of pinhole area according to cleaning method.

The box plots corresponding to film thickness look the same as well. These are shown in figures 4.20 and 4.21 below. Similar to the box plots of the pinhole area and the transformed scale of the pinhole area corresponding to cleaning method, the box plots of the pinhole area in transformed scale according to film thickness make more sense.

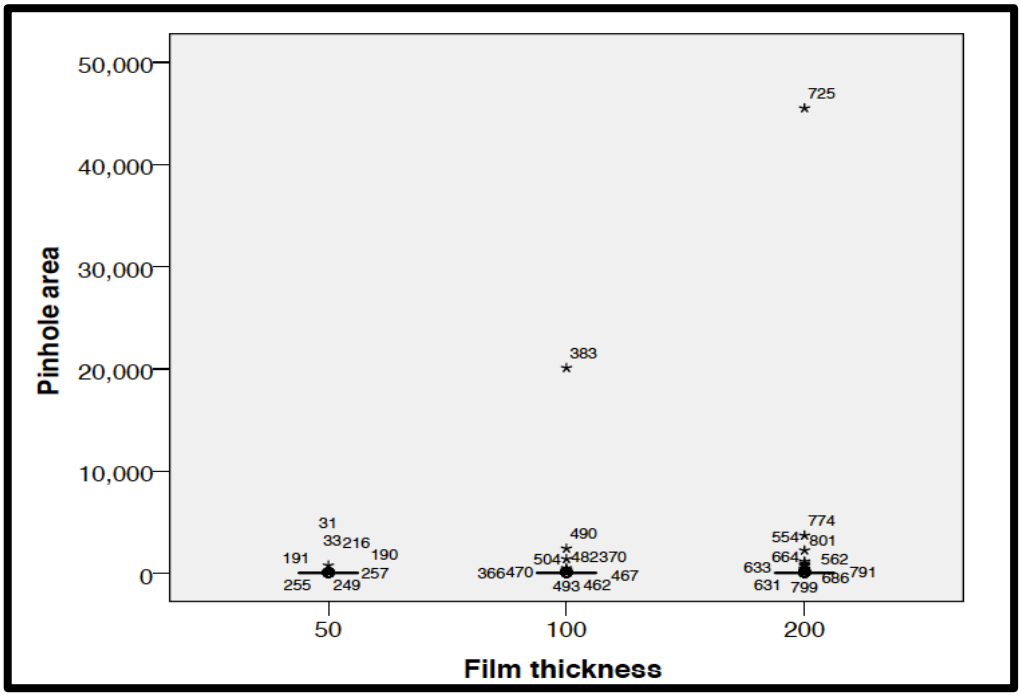

Figure 4. 20: Box plots of the pinhole area corresponding to film thickness.

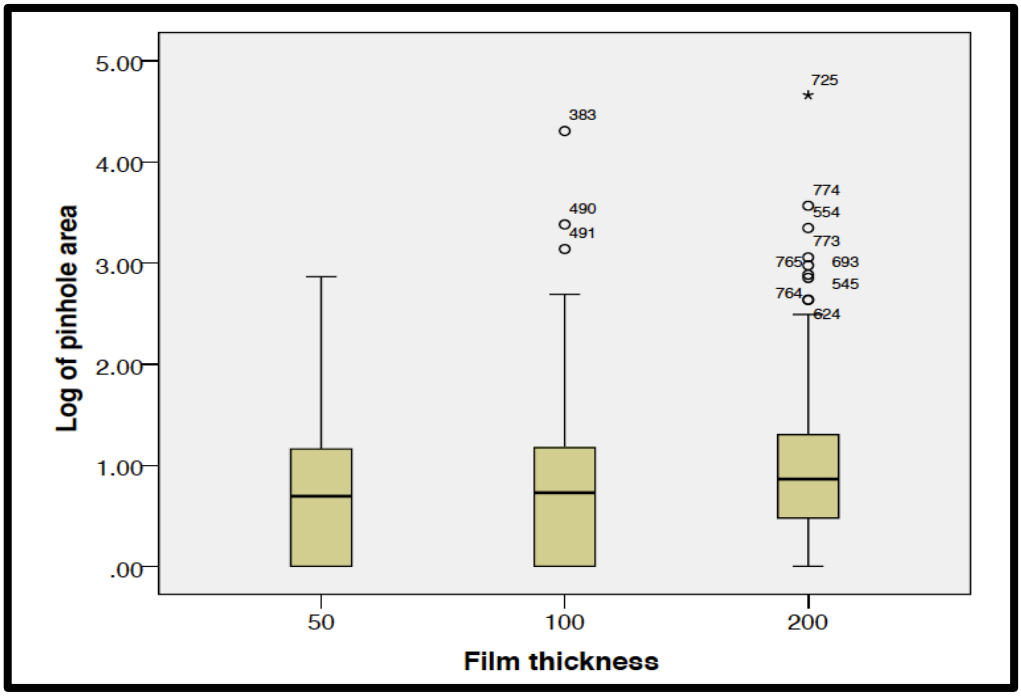

Figure 4. 21: Box plots of the transformed scale of pinhole area corresponding to film thickness.

The analysis of variance (ANOVA) for the transformed scale of pinhole area was completed at a significance level of $\alpha=0.05$. This indicates a confidence level in the statistics results of 95%. ANOVA tests the hypothesis that the pinhole areas (in the transformed scale) among the variables involved (two cleaning methods and three film thicknesses) are equal. Upon completion of the statistics, ANOVA outputs a table showing the significance of any of the variables studied and any possible interactions. A p-value is the probability of observing a test statistic that at least as extreme as the values being observed. Any p-value < 0.05 indicates rejection of the hypothesis being tested and statistical significance of the variable being considered. Usually, upon completion of the statistics of the transformed scale, one can back-transform the means to the original scale to obtain results on the original scale. But, in some cases like the transformed scale of the data in this thesis, it was not useful to back-transform the data since that did not provide meaningful values. According to [37], “if the means are statistically significant based on the transformed scale, it is reasonable to conclude that the means of the original scale are also significantly different, if the variances of the transformed scale are homogeneous”.

The hypothesis that the transformed scale of pinhole area is equal for both cleaning methods as well as film thickness was rejected with a p-value of 0.002 and a p-value <0.001 respectively. In fact, the pinhole area (transformed scale) for CdS films deposited on standard cleaned substrates had a mean value of 0.723 whereas CdS films deposited on substrates cleaned within the mini-environment had a mean value of 0.876. Based on this and the significance of the cleaning method, there is a 95% more probability that CdS films deposited on mini-environment cleaned substrates have more

pinhole than those deposited on standard cleaned substrates. Likewise, there is a 95% more possibility that the 200nm CdS films have more pinhole area than 100nm and 50nm CdS films. These means of the transformed scale of the pinhole area of both cleaning methods as well as film thickness are shown in figures 4.22 and 4.23 below. The difference between standard cleaning and cleaning in the mini-environment that may have led to these results is explained in the next section.

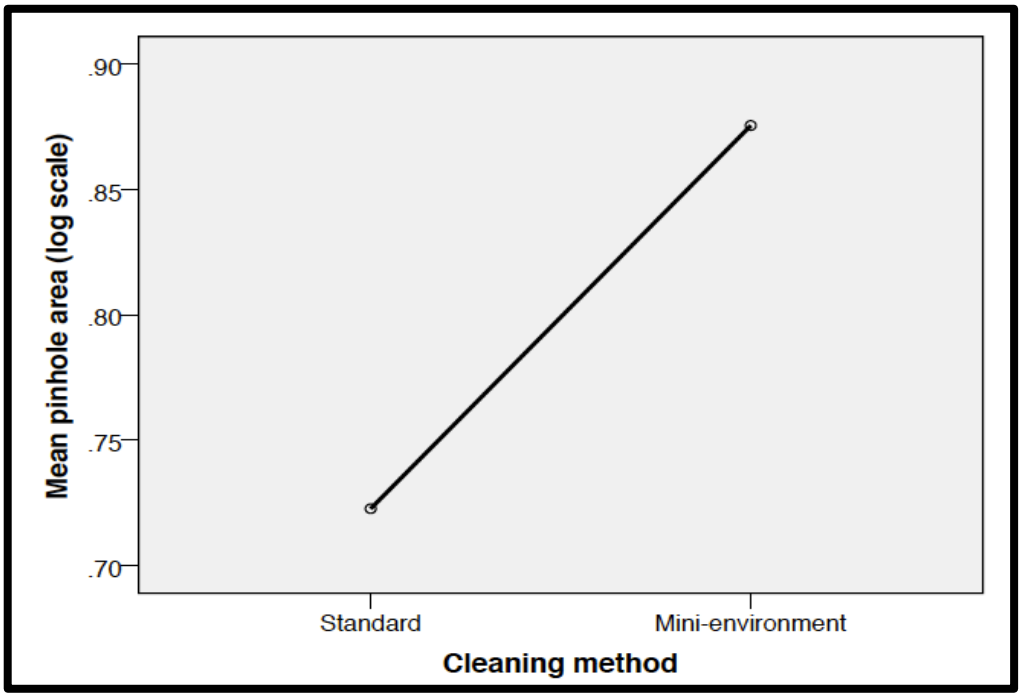

Figure 4. 22: Means of the transformed scale of pinhole area corresponding to cleaning method.

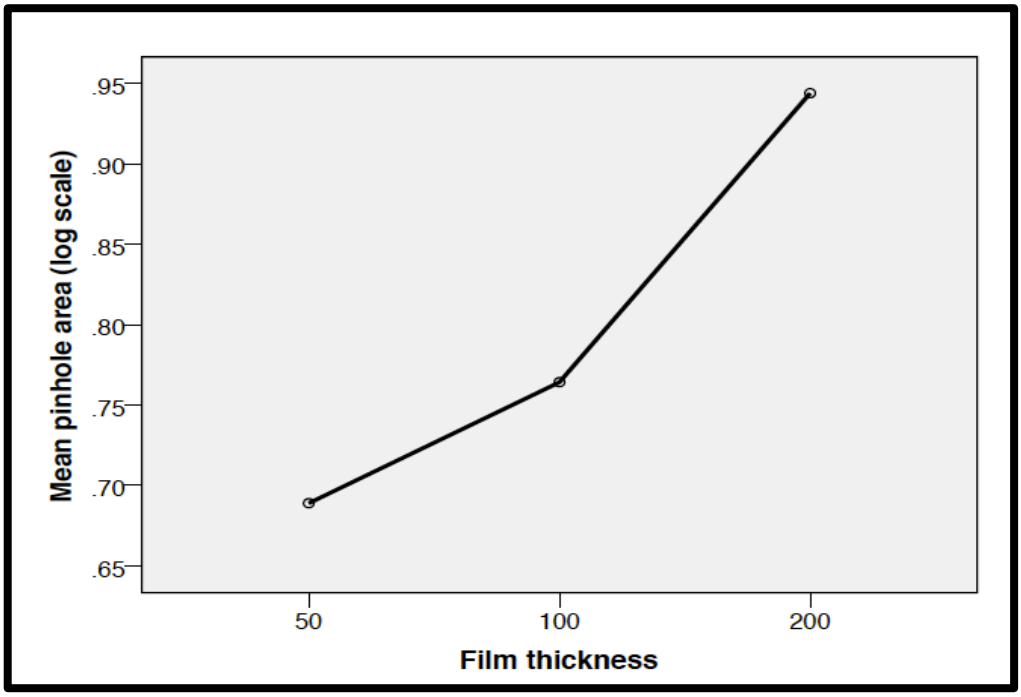

Figure 4. 23: Means of the transformed scale of the pinhole area corresponding to film thickness.

4.2.2. Mini-environment vs. Standard vs. Plasma

Upon completion of the first experiment, it was interesting to study the effects of cleaning the glass substrates with plasma as compared to other cleaning methods. Due to limitations of the number of films that can be deposited in the same day, two thicknesses were considered here (200nm and 100nm). A total of 30 substrates were used in this experiment following the same procedure as the first experiment where five substrates per film thickness per cleaning method were used. Again, these films were then observed for pinholes on 27 pre-specified locations by BLTOM and the data was then collected by FIJI. The pinhole count, pinhole area and average pinhole area in all CdS films corresponding to each film thickness and cleaning method are shown in table 4.2. In this table, the pinhole count and pinhole area are the total number of pinholes

and total pinhole area observed in five CdS film of the same film thickness and deposited on substrates cleaned with the same cleaning method (135 images per film thickness per cleaning method). The average pinhole area on the other hand is the average pinhole area per image across these 135 images.

Table 4. 2: Pinhole count and pinhole area from FIJI for the second experiment.

Film thickness (nm)	Cleaning method	Pinhole count	Pinhole area (μm^2)	Average pinhole area (μm^2)
100	Plasma	193	109	0.8
100	Mini-environment	2,304	1,638	12.1
100	Standard	5,804	6,716	49.8
200	Plasma	23	70	0.5
200	Mini-environment	5,799	6,858	50.8
200	Standard	5,768	5,600	41.5

The boxplots of the pinhole area data in the original scale corresponding to cleaning method and film thickness are shown in figures 4.24 and 4.25 respectively. In addition, the box plots of the pinhole area in the transformed scale corresponding to cleaning method and film thickness are shown in figures 4.26 and 4.27 respectively. The skewness of the data was also similar to what was observed in the first experiment (13.85 for the original pinhole area and 1.3 for the transformed scale). Once again, the transformed pinhole area scale was used in this part as well to perform ANOVA.

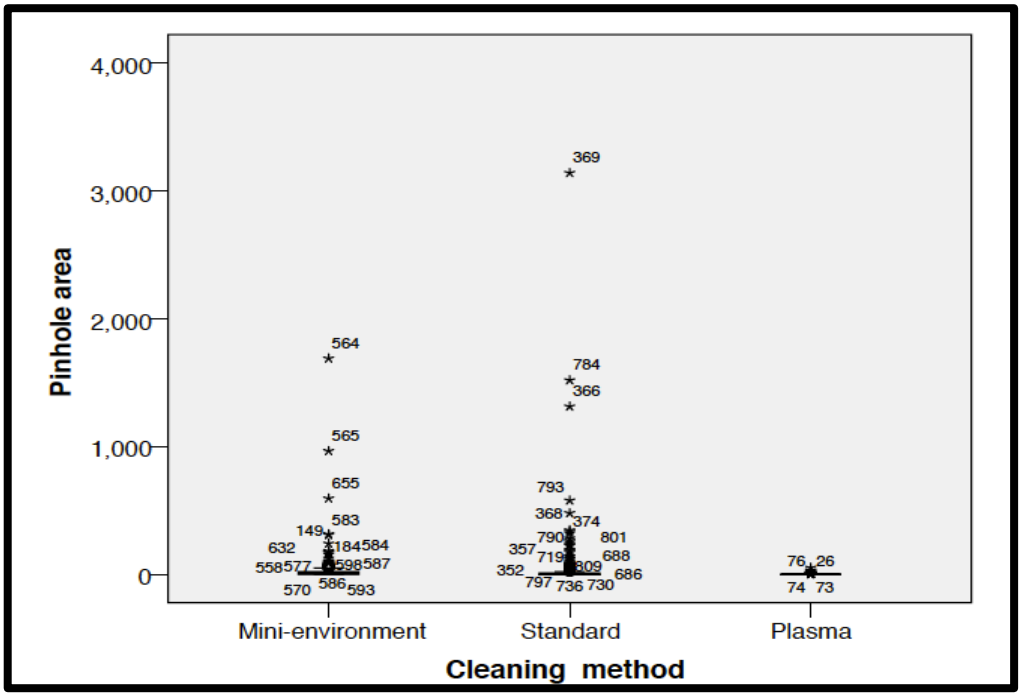

Figure 4. 24: Box plots of the pinhole area corresponding to cleaning method in the second statistic study.

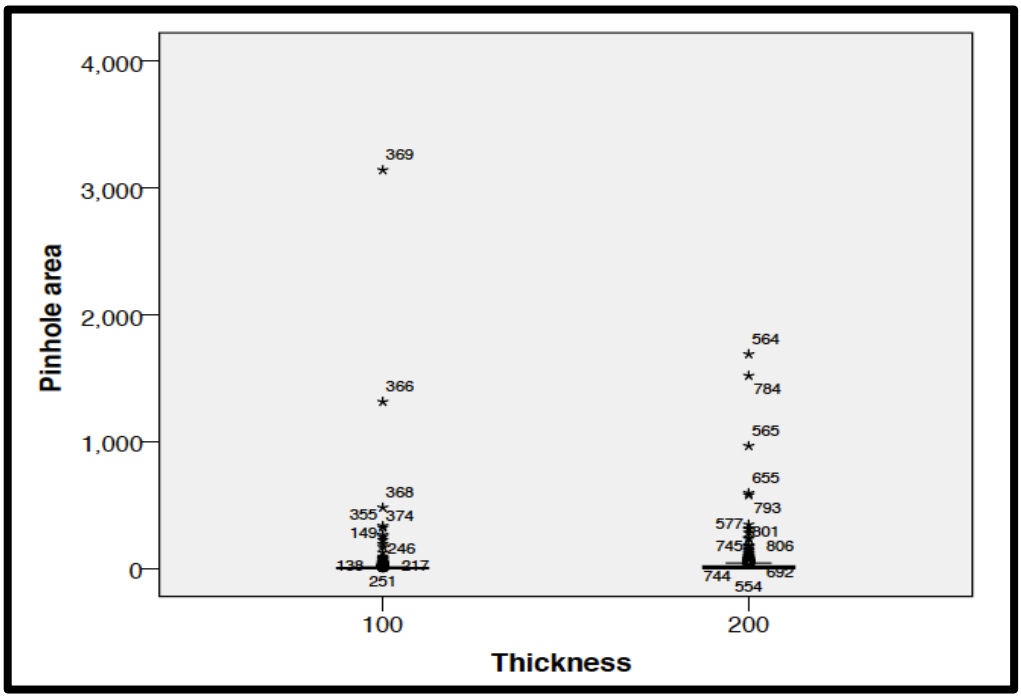

Figure 4. 25: Box plots of the pinhole area according to film thickness in the second statistic study.

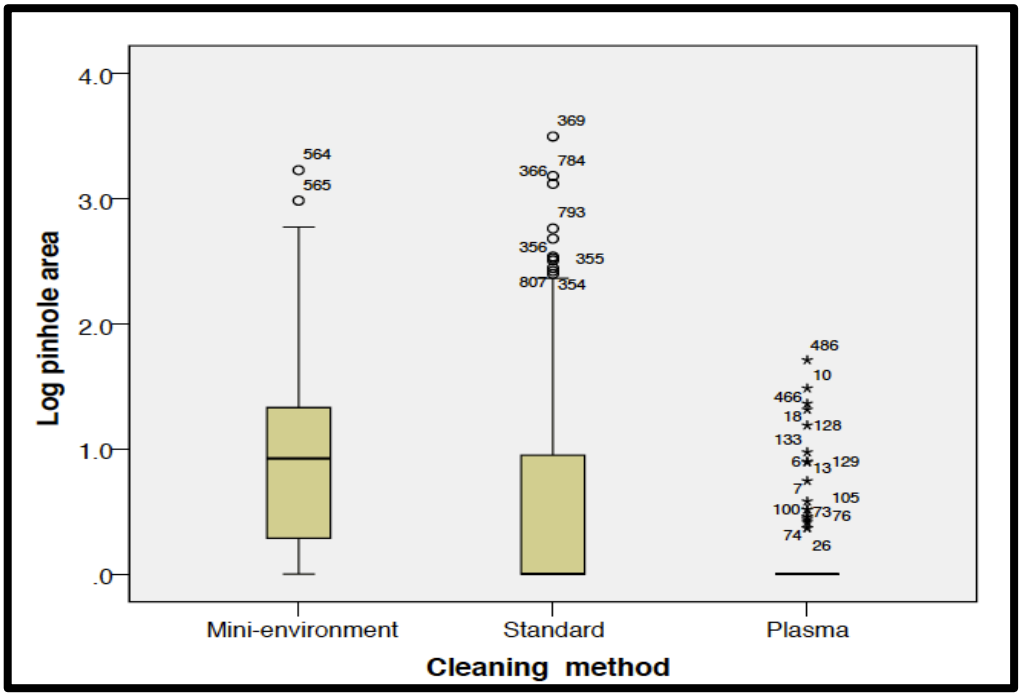

Figure 4. 26: Box plots of the pinhole area in the transformed scale according to cleaning method in the second statistic study.

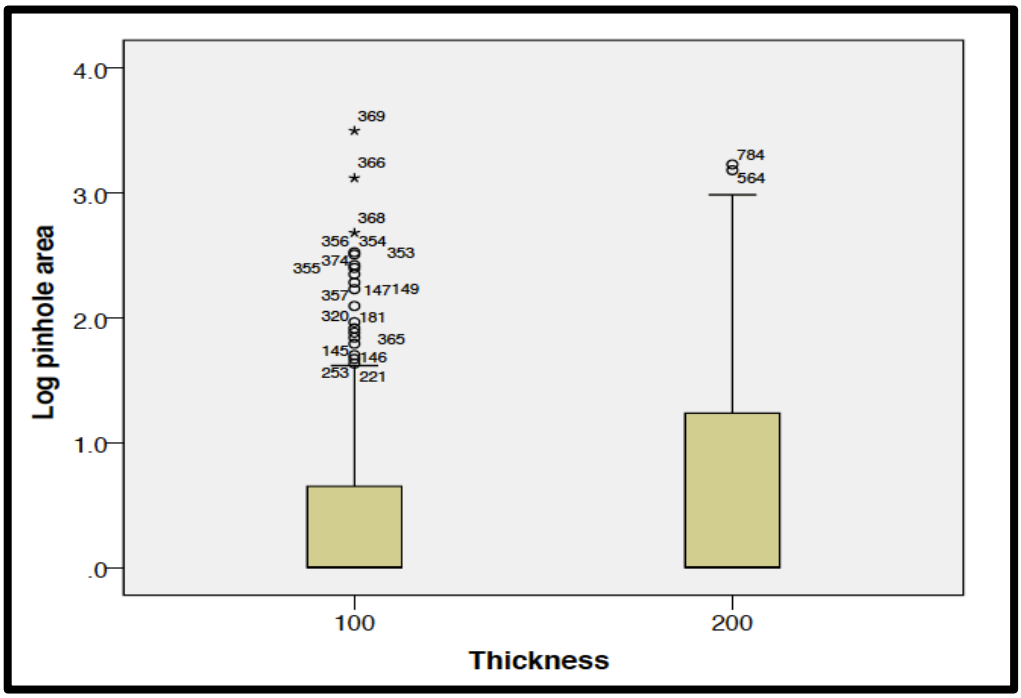

Figure 4. 27: Box plots of the pinhole area in the transformed scale according to film thickness as obtained in the second statistic study.

ANOVA results indicated the significance of both cleaning method and film thickness in addition to the significance of the combined effect of both variables. The cleaning method had the highest significance level with a test statistic F=130.5, followed by film thickness with F=39.2 and finally the combined effect of both cleaning method and film thickness with F=16.2. The p-value in all three cases was less than 0.001. The mini-environment samples (across all film thicknesses) had the worst pinhole area with a mean value of 0.9 on the transformed scale of pinhole area and the plasma-cleaned samples had the least mean value of 0.05 for all film thicknesses on the same scale. Figure 4.28 shows the means of the of the pinhole area in the transformed scale corresponding to cleaning method.

Figure 4. 28: Mean of pinhole area in the transformed scale according to cleaning method.

Furthermore, the 100nm CdS films had much less pinhole area with a mean value of 0.35 on the transformed scale while the 200nm films had a mean value of 0.62 on the

same scale. This is shown in figure 4.29. The combined effect of both cleaning method and film thickness showed significance statistical difference among all interaction for the multiple comparisons tests, the means of pinhole area on the transformed scale for the combined effects are shown in figure 4.30. Based on this combined interaction, pinhole area is significantly higher for thicker film thickness when substrates are standard cleaned or mini-environment cleaned. With plasma cleaning, the pinhole area for the 200nm film was significantly less that that for the 100nm film thickness in addition to both film thicknesses having significantly much less pinhole area than the other cleaning methods.

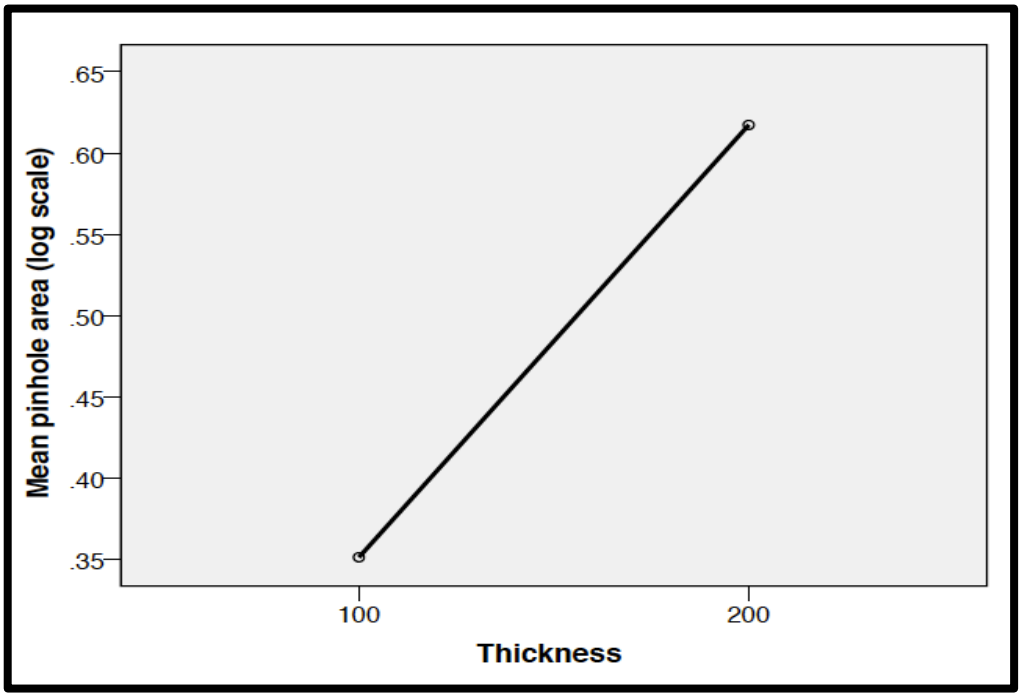

Figure 4. 29: The means of pinhole area in the transformed scale corresponding to film thickness.

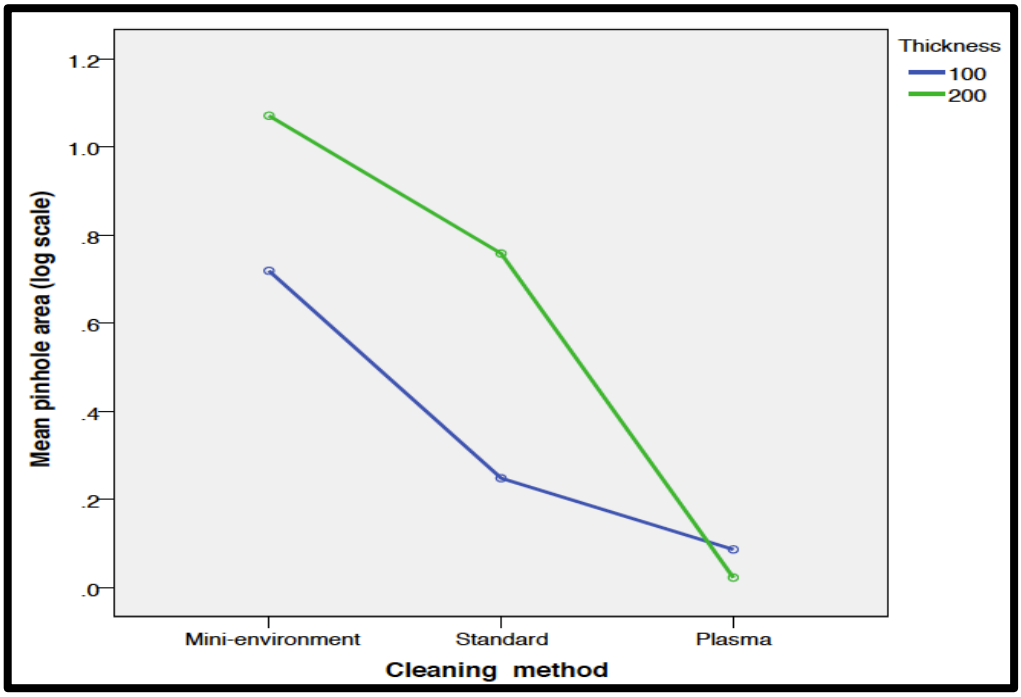

Figure 4. 30: The means of pinhole area in the transformed scale corresponding to both cleaning method and film thickness.

Using the mini-environment to control pinholes in CdS films of different thicknesses did not prove to be as effective as plasma cleaning nor standard cleaning. This outcome is the result of the quality of cleaning done within the mini-environment. Standard cleaning in open lab environment involves cleaning the substrates in an Ultrasonic washing machine with detergent, followed by rinsing the substrates with a continuous flow of DI water and finally drying with isopropanol (IPA) solution. Within the mini-environment, it was not possible to replicate the same cleaning procedure due to the confined space. The ultrasonic washer was moved inside the mini-environment and four large beakers were used within the washing machine to replicate the process of cleaning substrates in open lab environment. One beaker contained the soap detergent, two beakers contained clean DI water to rinse the substrates and a fourth beaker contained IPA solution to dry the substrates. It seemed that the ultrasonic effects in this

setup were not as effective as they are in the open lab environment setup implemented in standard cleaning. Moreover, the rinsing process did not seem good enough so that substrates still had some soap residues after cleaning and this could have caused the films deposited on these substrates to have more pinholes. The setup of cleaning the substrates within the mini-environment is shown in figure 4.38.

Figure 4. 31: Substrates cleaning setup inside the ultrasonic washing machine within the mini-environment.

4.2.3. Standard vs. plasma cleaning for thin CdS films

This experiment was conducted to investigate whether the same plasma cleaning effects seen previously would still be valid in thinner CdS films. Mini-environment cleaning discontinued since CdS films that were cleaned within the mini-environment had significantly more pinholes than those films deposited on substrates cleaned with the other cleaning methods. A total of 20 TEC10 glass substrates were used to deposit

CdS films of two film thicknesses: 70nm and 50nm. Same as before, 5 substrates per cleaning method per film thickness were used for the experiment and BLTOM images were recorded at 27 pre-specified locations; pinhole count as well as pinhole area data was complied using FIJI. The pinhole count, pinhole area and average pinhole area in all CdS films corresponding to each film thickness and cleaning method are shown in table 4.3. In this table, the pinhole count and pinhole area are the total number of pinholes and total pinhole area observed in five CdS film of the same film thickness and deposited on substrates cleaned with the same cleaning method (135 images per film thickness per cleaning method). The average pinhole area on the other hand is the average pinhole area per image across these 135 images.

Table 4. 3: Pinhole count and pinhole area from FIJI for the third experiment.

Film thickness (nm)	Cleaning method	Pinhole count	Pinhole area (μm^2)	Average pinhole area (μm^2)
50	Plasma	44	25	0.18
50	Standard	353	121	0.89
70	Plasma	84	33	0.24
70	Standard	1032	274	2.03

The boxplots of the data in the original pinhole area scale corresponding to cleaning method and film thickness are shown in figures 4.32 and 4.34 respectively. The boxplots of the transformed scale of the pinhole area corresponding to cleaning method and film thickness are shown in figures 4.33 and 4.35 respectively. Finally the skewness of the data was reduced from 10 to 3 upon implementing the transformed scale of the pinhole area.

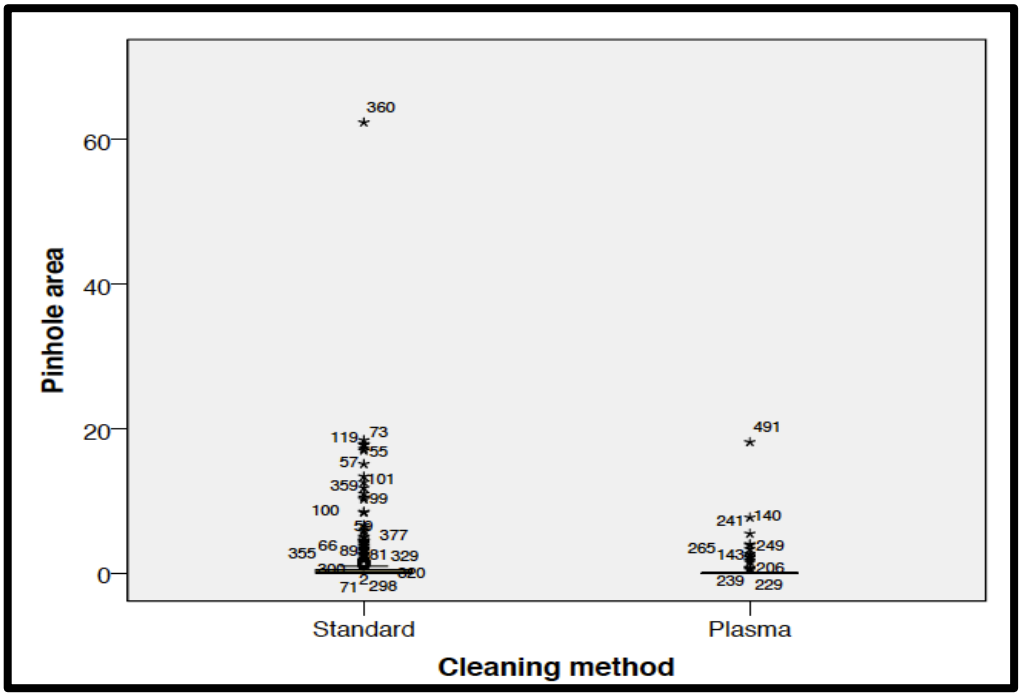

Figure 4. 32: Box plots of the pinhole area according to cleaning method in thinner CdS films.

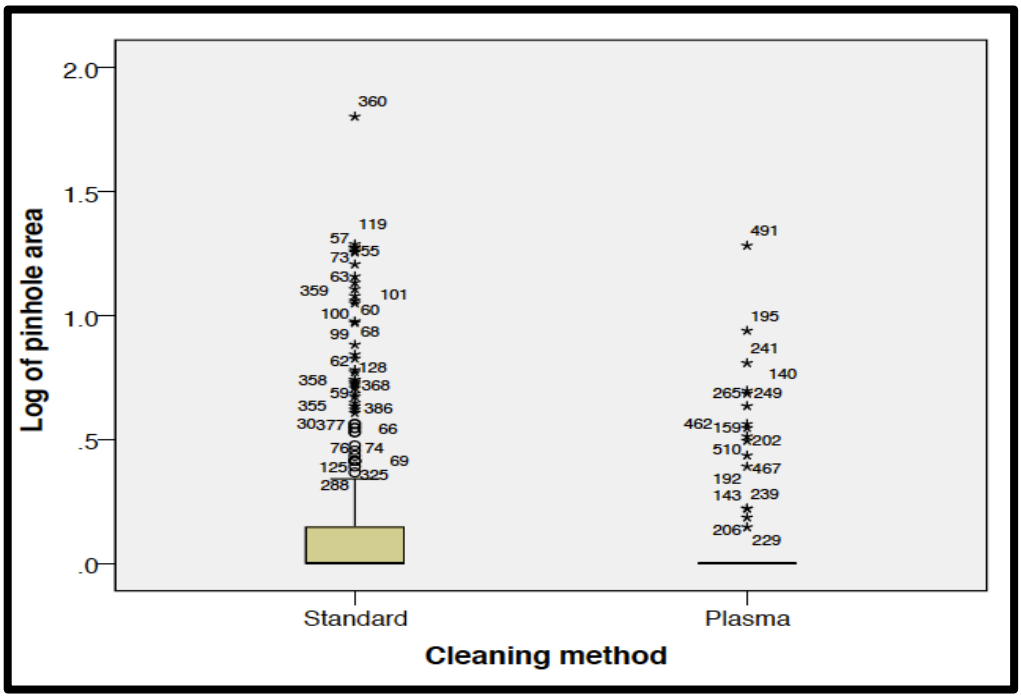

Figure 4. 33: Box plots of the transformed scale of pinhole area according to the cleaning method.

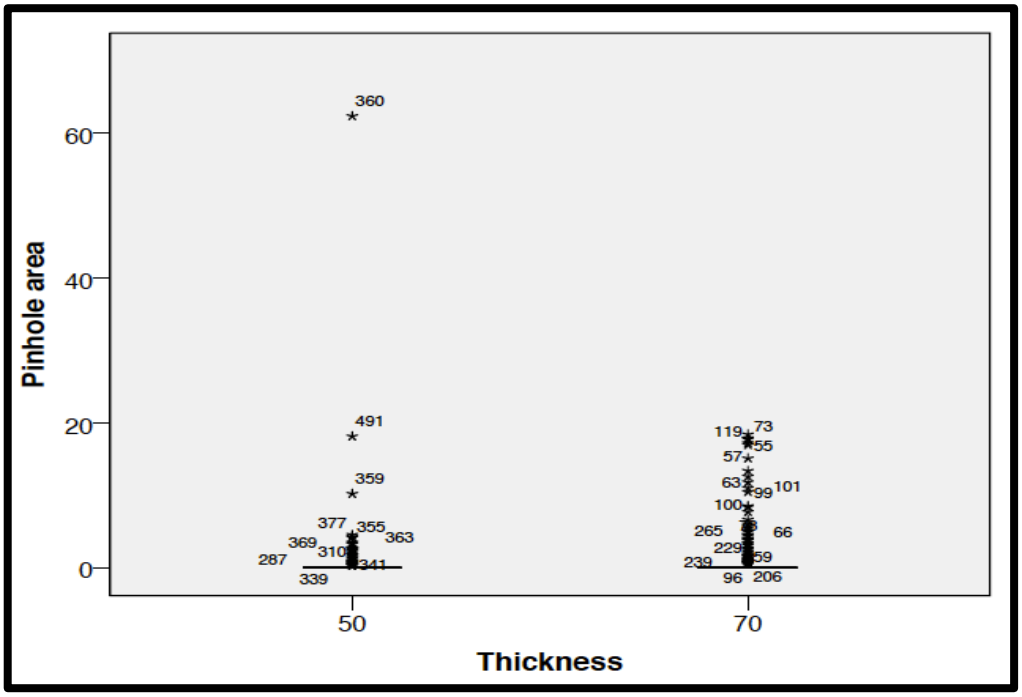

Figure 4. 34: Box plots of the pinhole area according to film thickness.

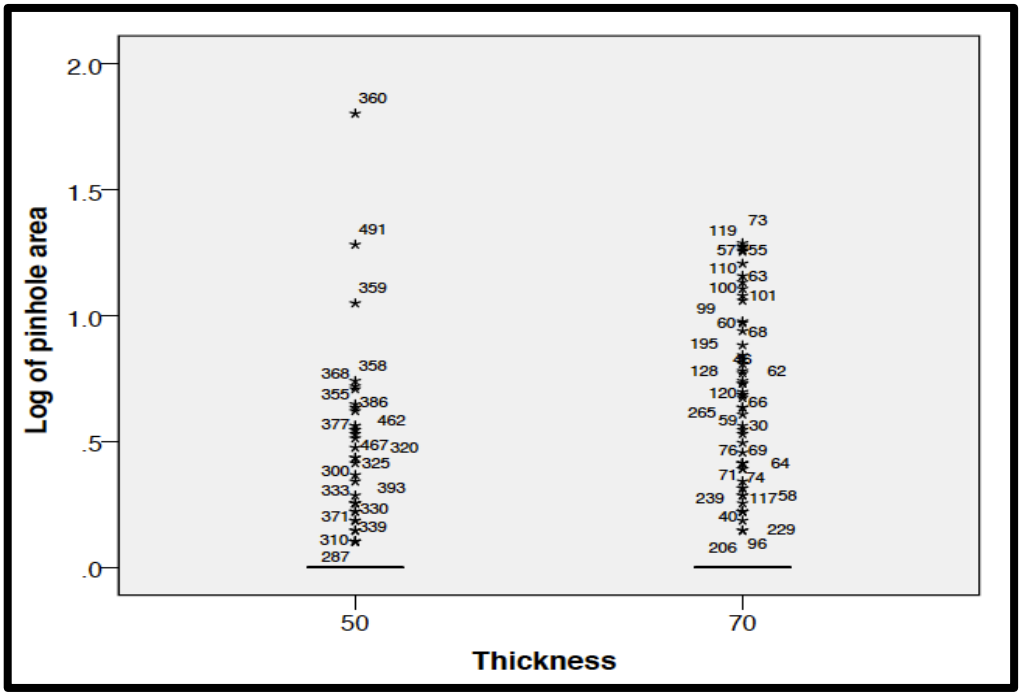

Figure 4. 35: Box plots of the pinhole area in the transformed scale according to film thickness.

Upon completing the analysis of variance on the data, it was found that the only significant factor affecting the pinhole area among the tested film thicknesses in the cleaning method with a test statistic of 15.8 and a p-value of <0.001. The film thickness factor was not statistically significant in this experiment (p=0.06). Plasma cleaning significantly reduced pinholes in both film thicknesses as compared to standard cleaning. The mean of pinhole area in the transformed scale for CdS films deposited on plasma cleaned substrates was 0.2 while the same was 1.5 for CdS films deposited on standard cleaned substrates. Although ANOVA indicated that the film thickness was not a significant factor among the sample, the mean of the pinhole area in the transformed scale was 0.5 for the 50nm films and 1.1 for the 70nm films. Figure 4.36 and 4.37 show the mean of the pinhole area in the transformed scale corresponding to cleaning method and film thickness respectively.

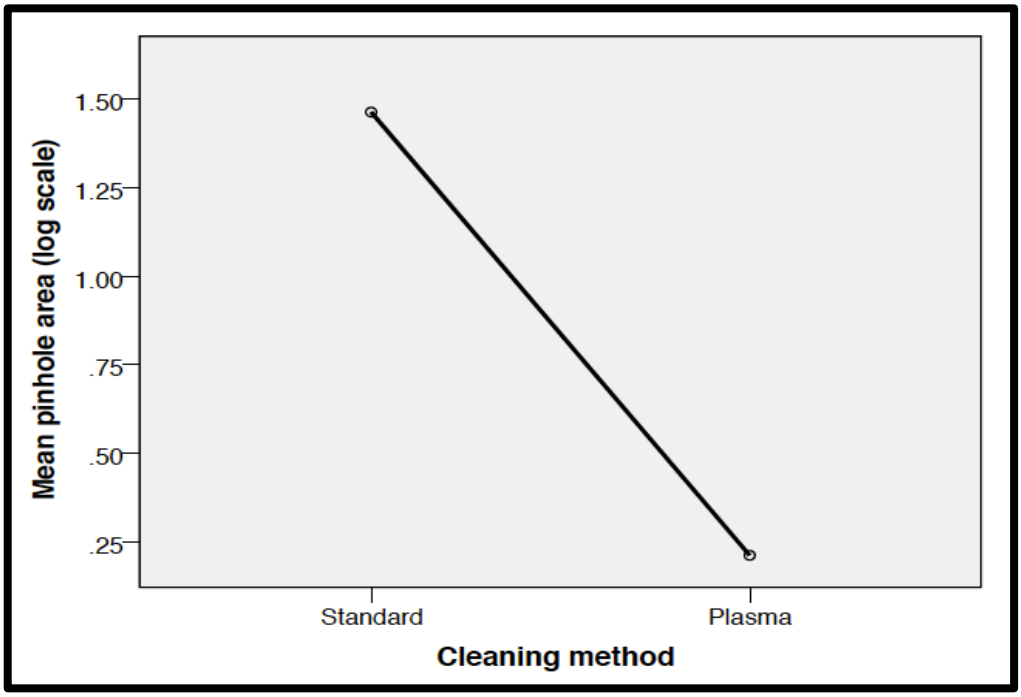

Figure 4. 36: The means of the transformed scale of the pinhole area corresponding to cleaning method.

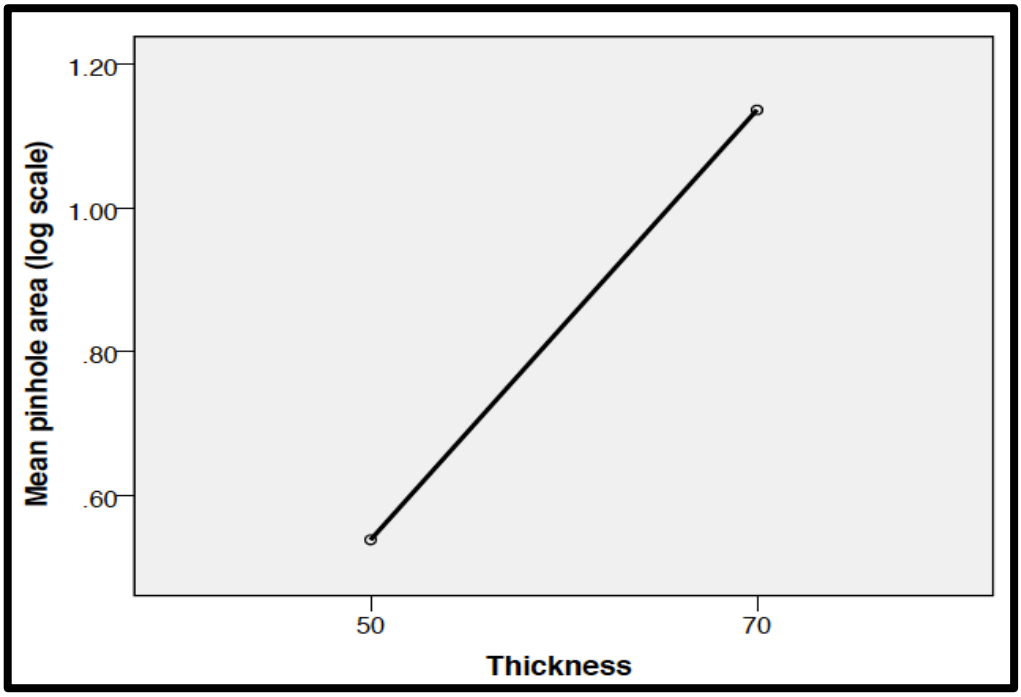

Figure 4. 37: The means of the transformed scale of the pinhole area corresponding to film thickness.

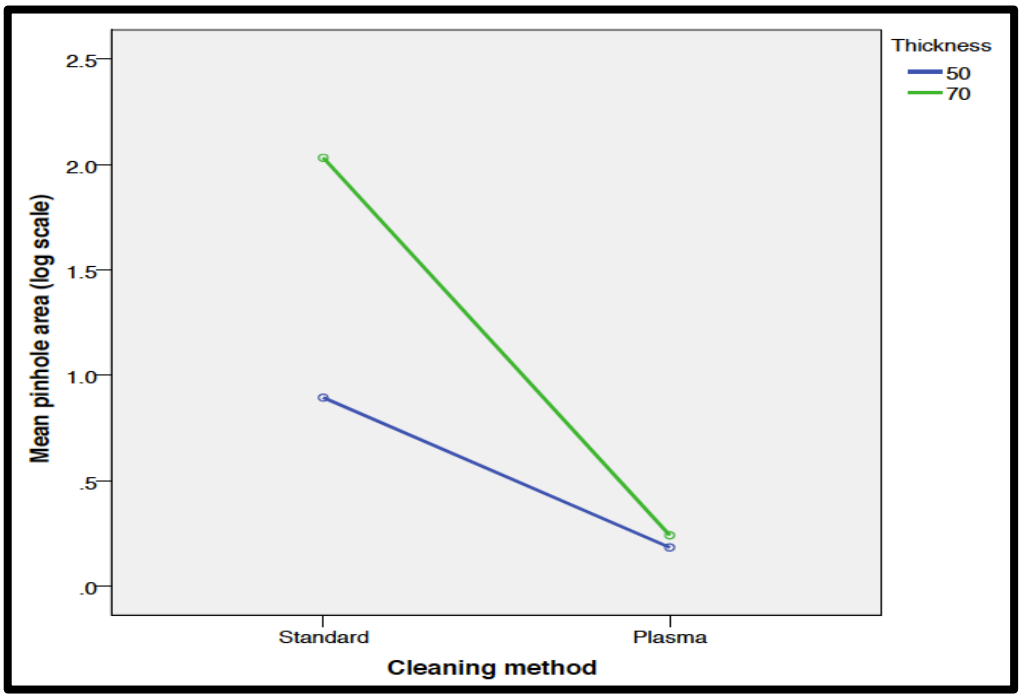

Figure 4. 38: The means of the transformed scale of the pinhole area corresponding to both cleaning method and film thickness.

Thus, it can be concluded from the results outlined within this chapter that plasma cleaning is the best way to deposit CdS films of any thickness that are almost free of pinholes. In addition, it was shown that grain coalescence and TCO surface roughness are not major sources of pinholes especially in CdS films deposited via close space sublimation. Among the artificial sources of pinholes, scratches and scuffing marks can be controlled by careful substrate handling after the films are deposited. Finally, the fact that all statistical experiments showed that thinner CdS films had less pinhole area than thick CdS films is a strong indication that film growth rate can affect the quality of CdS films. More details are provided in chapter 6.

Chapter 5

Pinhole Effects

This chapter is focused onto the effects of pinholes by means of actual devices and simulation. Some devices with POR (process of record) conditions were made along with other devices that had no CdS at all. The current-voltage (J-V) curve of one of the best devices at the time of the experiment (red curve) and the J-V curve for a device that had no CdS (green) are shown in figure 5.1. Both devices were made at the same location within the substrate, at location 5 as shown in figure 3.6 in chapter 3.

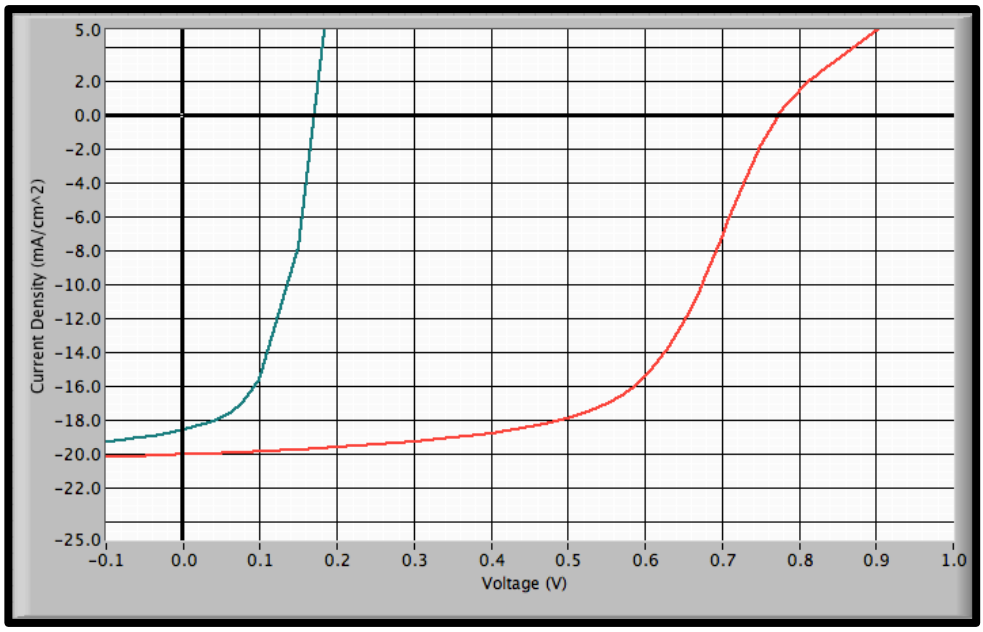

Figure 5. 1: JV curves of actual devices, the red line is a POR full device and the green line represents a device that has no CdS film.

These devices and the output V_{OC} and J_{SC} were used in various part in this chapter. The chapter is divided into two sections, the first is focused onto discussing the pinhole size effect in actual devices and the second is focused onto simulating the effects of

different fractions of pinhole area (F) on device properties through PSpice® and MATLAB®.

5.1. Pinhole size effect

As far as pinholes being the matter of discussion, it would be useful to get an idea whether a pinhole in a completed device affect the same area as the pinhole, a bigger area or even a smaller area. It was important to find a pinhole in a CdS film within the completed device, make sure that the feature observed is a pinhole and find some way to measure the size effect of that pinhole. This was accomplished by means of EL and LBIC.

The JV curves of the devices in figure 5.1 were a part of an experiment that included more devices that had an open circuit voltage ranging between 720mV and 780mV. Considering this range of V_{OC} of devices made in one substrate, some of these devices were further investigated for pinholes. As discussed in chapter 3, one can use Light Beam Induced Current of different laser wavelengths to identify defects within the widow layer in the completed device. According to [28] such a defect would have a high signal response in the 405nm LBIC scan and a shallow or very low response in the 638nm LBIC scan. Figure 5.2 shows an electroluminescence image of a device that had some defects. LBIC scans of the indicated wavelengths were completed on the same device to identify possible pinholes. The EL and LBIC images presented in this chapter were processed by John Raguse and Russell Geisthardt of the Photovoltaic lab at Colorado State University.

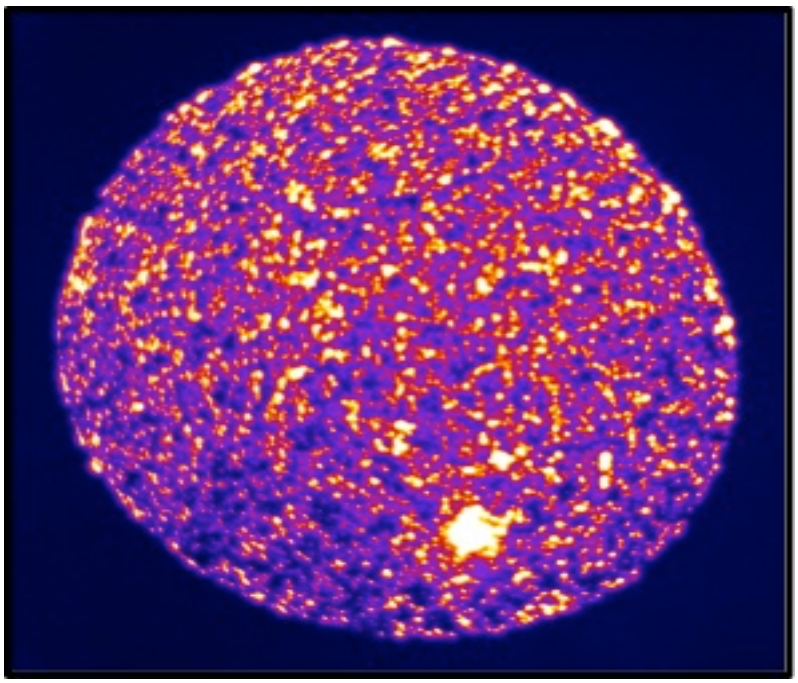

Figure 5. 2: EL image of a device that had a V_{OC} of 705mV, the lower right quadrant was further investigated for possible pinholes using LBIC.

The lower right corner of the device shown in figure 5.2 shows some big features that could be defects in the CdS layer and thus LBIC scans were completed at that region to identify possible pinholes and/or defects in the CdS layer. The LBIC 405nm laser beam wavelength scan is shown in figure 5.3 whereas the 638nm laser beam wavelength scan is shown in figure 5.4. Both of these images were done using the low-resolution scan for the purpose of choosing practical locations for the high resolution scans. Figure 5.3 show two interesting features (shown within black squares as A and B) that might be pinholes and worth investigating further. Based on these two images, both features seem to fit the description of pinholes stated in [34] where a pinhole would exhibit a high response in the 405nm scan and low response in the 638nm scan. The feature inside the top square is called feature B and the other is called feature A.

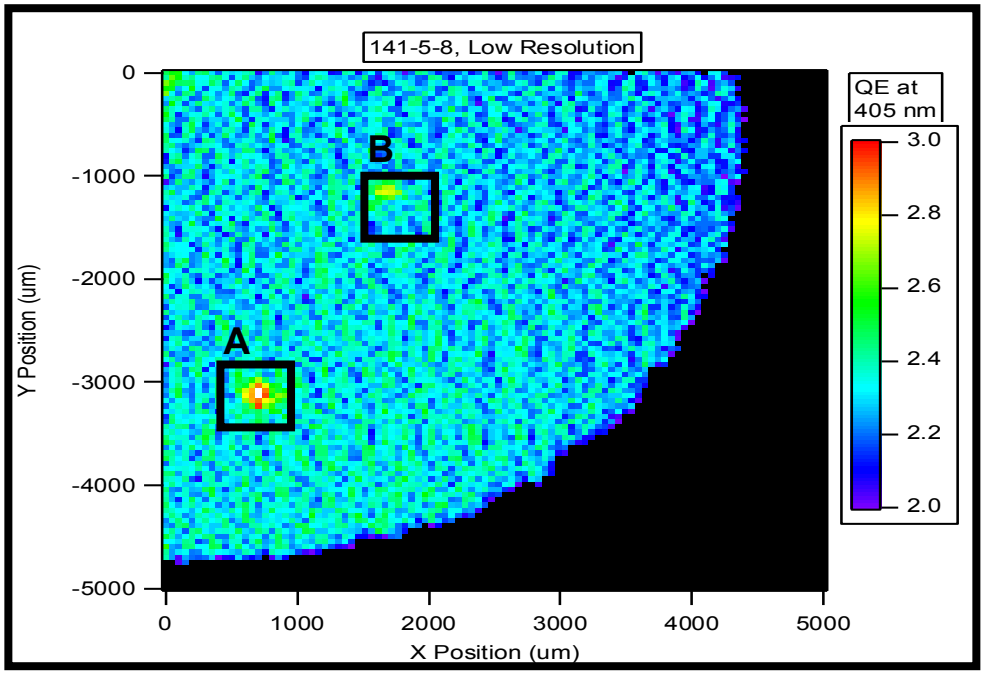

Figure 5. 3: LBIC scan of the bottom right quadrant of the SAD shown in figure 5.2 using low-resolution 405nm laser wavelength scan.

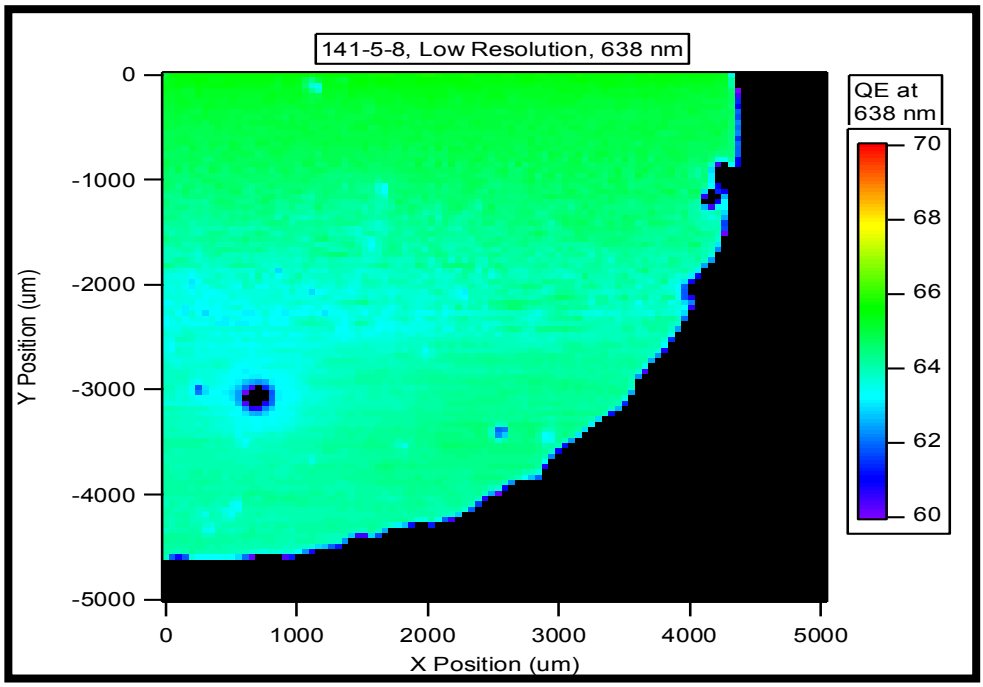

Figure 5. 4: LBIC image of the bottom right quadrant of the SAD shown in figure 5.2 suing the low-resolution 638nm laser beam wavelength scan.

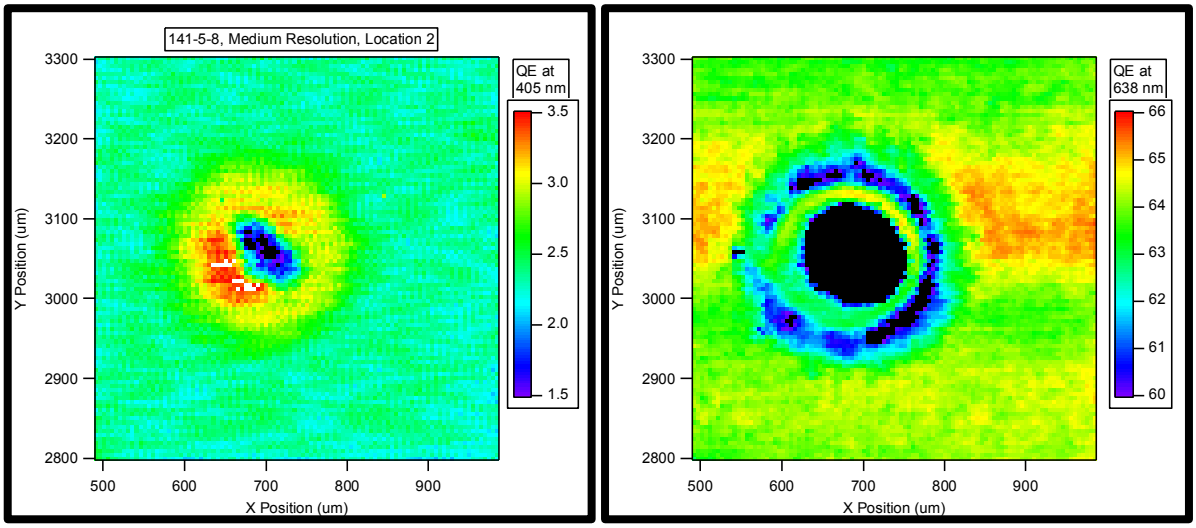

Figure 5. 5: Medium resolution LBIC scans of the defect A shown in the low-resolution LBIC scan in figure 5.3 above using both the 405nm (left) and the 638nm (right) laser beam wavelengths.

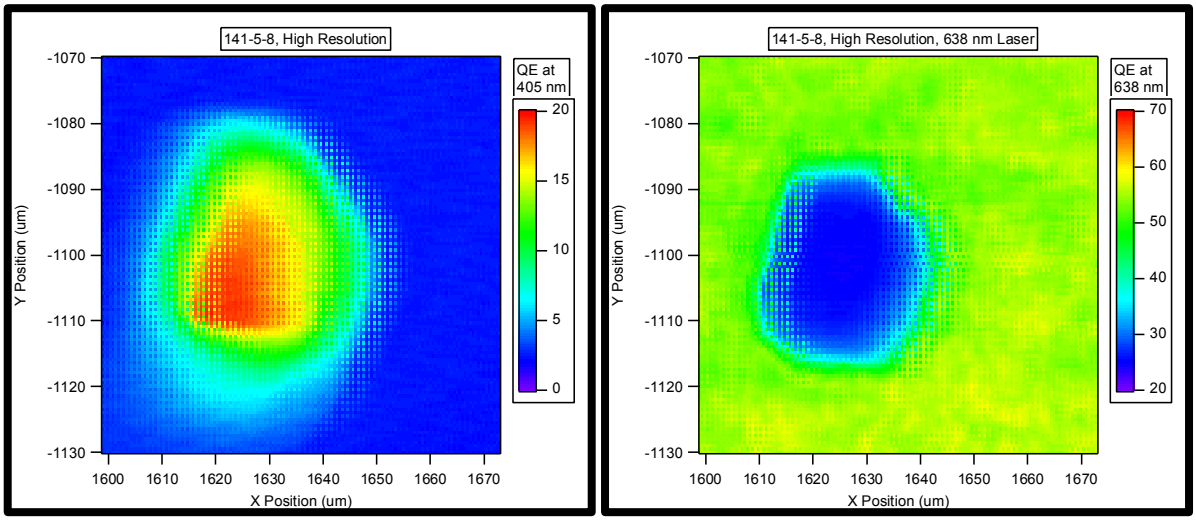

Figure 5. 6: High resolution LBIC scans of defect B shown in figure 5.3 above. The 405nm scan is shown on the left and the 638nm scan is shown on the right.

The medium and high resolution LBIC scans for feature A (figure 5.5) revealed that this feature is probably not a pinhole [34]. For this feature to be a pinhole, it should have a very high response in the 405nm LBIC scan and a very low response in the 638nm

LBIC scan. On the other hand, feature B shown in figure 5.6 satisfied those conditions, believed to be a pinhole and it can be used to identify the pinhole size effects. Comparing the size of the defect in both the LBIC 405nm laser scan (left image in figure 5.6) as well as the EL image can be used to identify the size effect of pinholes provided that the scale of the two images is known.

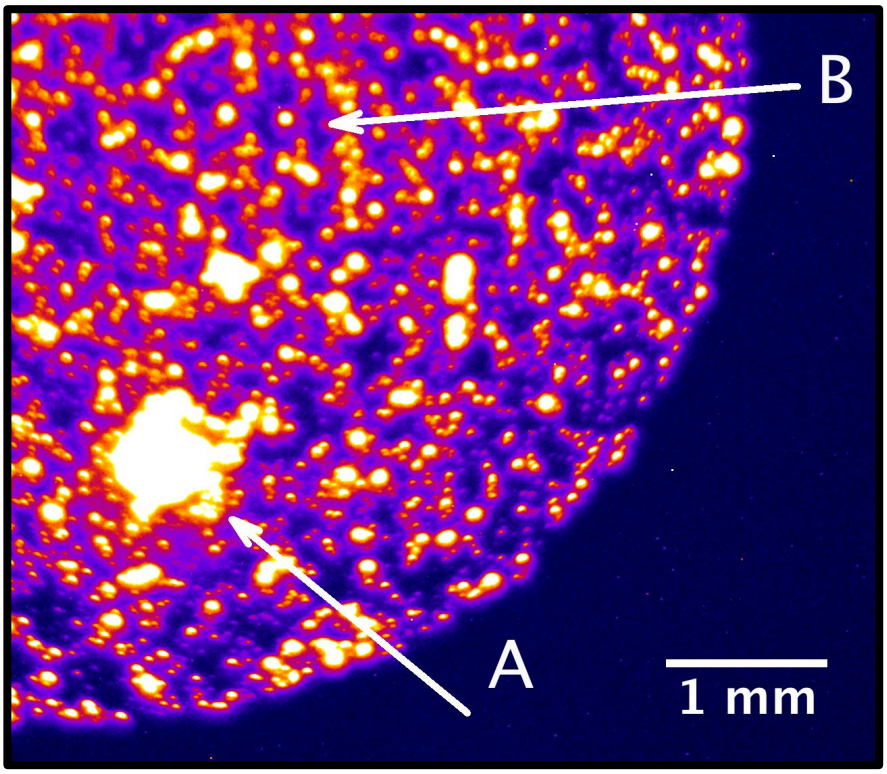

Figure 5. 7: A larger image of the SAD device shown in figure 5.2 showing the scale of the image as well as the pinhole that was identified by LBIC as defect B.

Figure 5.7 shows the same EL image in figure 5.2 emphasizing the two features discussed above. The EL image had scale of 239 pixel/mm and thus the area of defect B as measured by FIJI was about 0.02 mm^2. The scale on the LBIC image is provided in the LBIC image in figure 5.6 where the entire area of the LBIC scan is about 70 by 60 microns. The area of the pinhole as observed in LBIC is about 1300 μm^2 or 0.0013 mm^2 (measured and calculated by FIJI as well). Therefore, the pinhole size effect based on

the EL and LBIC (405nm scan) images for the shown pinhole is about 15 times the original pinhole area. In other words, a pinhole in the CdS film would affect an area of the full device that is 15 times larger than the area of the actual pinhole.

5.2. 2D PSpice® Model

2D PSpice® simulations were used to study that effects of the fractions of pinhole area (F) on V_{OC}. In addition, the same PSpice® model was used to create diode voltage profile plots. At each corresponding F, these diode voltage profile plots would give an idea of how much of the entire device area is affected corresponding to the pinhole area being considered.

5.2.1. V_{OC} vs. F

This model was built based on the parameters obtained from actual devices made at the lab. These include V_{OC}, J_{SC} and the sheet resistance of the TCO. As shown in chapter 3, V_{OC} and J_{SC} for both the full device and a device that had no CdS were used to calculate the saturation current density (Jo) required for specifying the values of both the good and the weak diodes in the model. The model contained 21x21-repeating units each containing a single diode of the device. Five diodes at the center of the model were chosen to be the location of the weak diodes. The total area of these five diodes was varied to simulate the effects of different pinhole areas on the open circuit voltage of the device while maintaining the total device area constant. Figure 5.8 shows JV curves of the simulated fractions of pinhole area. Table 5.1 shows the values of the open circuit voltage corresponding to each F and the corresponding V_{OC} loss. The same table shows the amount of V_{OC} and V_{OC} loss for each specific F as cited from the 1998 NREL IEC report [12].

Table 5. 1: V_{OC} loss corresponding to F

Open circuit voltage loss corresponding to different pinhole fraction areas as simulated in PSpice and compared to the 1998 NREL IEC report. F=0.01 means a pinhole that occupies 1% of the total device area.

F	Pinhole area (μm^2)	PSpice Simulation		1998 NREL IEC Report	
		Voc (mV)	ΔVoc	Voc (mV)	ΔVoc
F=0.00	0	774	0	840	0
F=0.000001	100	770	3	Missing	Missing
F=0.00001	1,000	744	30	830	10
F=0.0001	1.0e+4	662	112	786	54
F=0.001	1.0e+5	549	225	687	153
F=0.01	1.0e+6	431	343	570	270

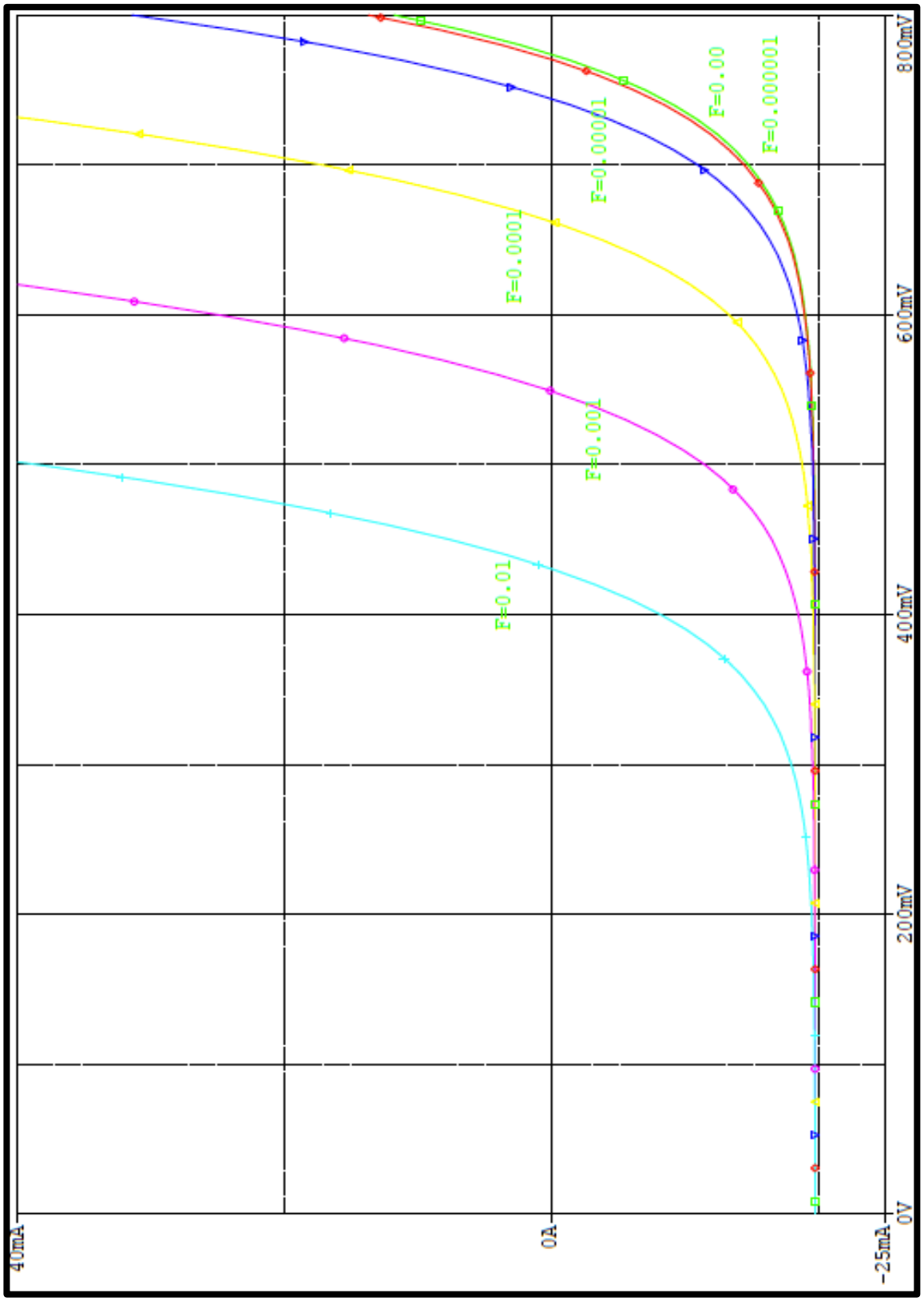

Figure 5. 8: Simulated JV curves of the PSpice® simulation where F=0.00 is a device that has no pinholes and F=0.01 is a device that has a fraction of pinhole area that is equal to 1% of the total device area.

In addition to the simulation done with PSpice® to observe the effects of pinhole of different sizes on V_{OC}, a MATLAB® mathematical model was built to test whether the V_{OC} loss model predicted by [12] would be appropriate for CdS films made at the lab. The open circuit voltage loss equation reported by the mentioned report is shown below. The MATLAB® model basically evaluated the open circuit voltage as the fraction of pinhole area to the total device area is changed from 0 to 100%. The values of Jo required for this mathematical model are the same as those values obtained from the full device (good diode) and that of the device that had no CdS (weak diode). In the equation below, $J_{o,TCO}$ corresponds to the saturation current of the weak diode and $J_{o,CdS}$ corresponds to the saturation current of the good diode. J_L is the light current and in this case J_{SC} was used as J_L. Finally MATLAB® plots a graph of the open circuit voltage as a function of F. The data from PSpice as well as the 1998 NREL IEC report can be incorporated into this MATLAB® graph to compare the three procedures. Figure 5.9 shows a plot of V_{OC} as a function of F for the three cases in the normal F scale and figure 5.10 shows the same plots in the log (F) scale.

$$V_{OC} = \frac{AkT}{q} \cdot \ln\left[\frac{J_L}{J_{o,CdS} \cdot (1-F) + J_{o,TCO} \cdot (F)}\right]$$

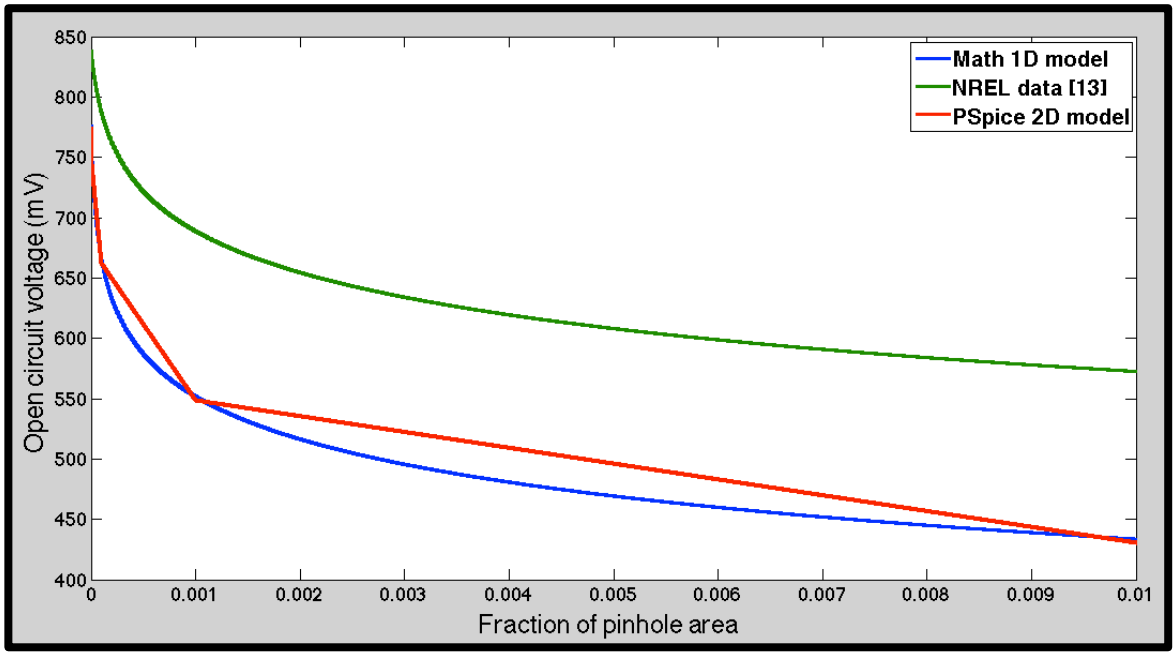

Figure 5. 9: Comparing the mathematical MATLAB® model with the 2D PSpice® model and data from [28] in the normal F scale.

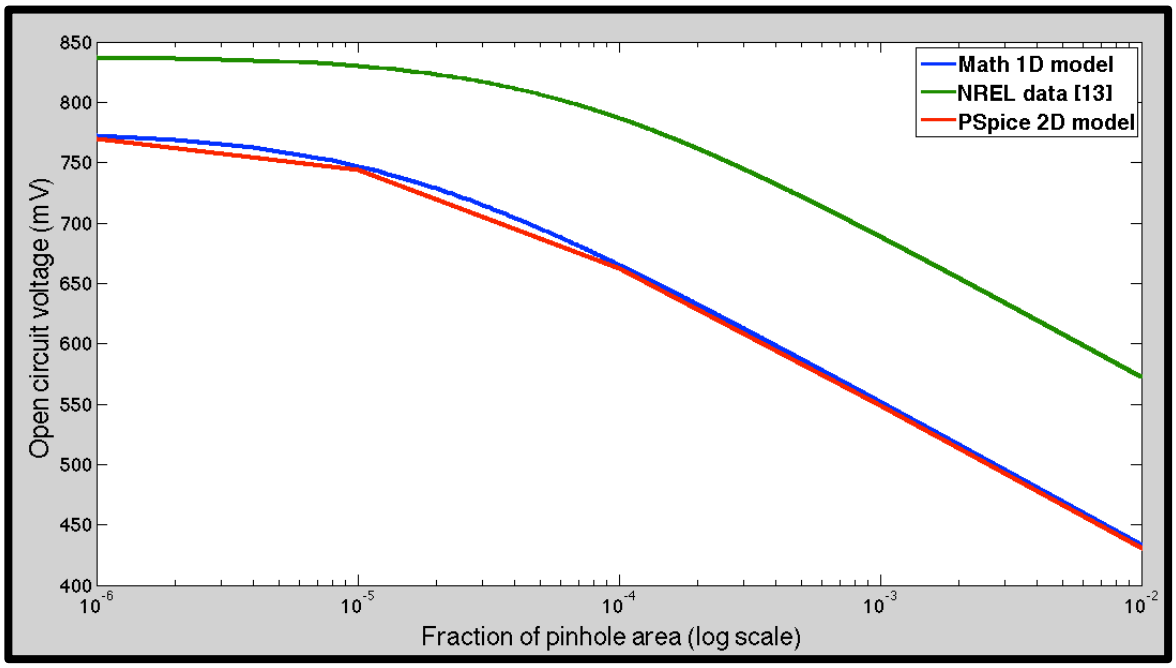

Figure 5. 10: Comparing the mathematical MATLAB® model with the 2D PSpice® model and data from [28] in the log of F scale.

Comparing the plots of V_{OC} as F changes from 0 to 0.01 (pinhole area changing from 0% to 1% of the total device area), its clear that there is an agreement among the three data sets. The NREL data (green line) seem to have higher open circuit voltage at each corresponding F. This effect might be due to the fact that the good diode in this case had a V_{OC} of 840mV and the weak diode had a V_{OC} of 330mV. Moreover, the NREL IEC data was based on devices deposited on a TCO made of Indium Tin Oxide (ITO) instead of the TCO in TEC10 substrates which is tin oxide: fluorine doped. The sheet resistance of the TCO in TEC10 glass substrates is 10 Ω/□ while the sheet resistance of ITO can vary between 10 and 100 Ω/□. The sheet resistance of the ITO used in the 1998 NREL IEC report may be very different from the sheet resistance of the TCO in TEC10 glass substrates and this might be another reason why the data from the report had higher V_{OC} at each corresponding F in addition to lower ΔV_{OC} in each case. On the other hand, the 2D PSpice® model was slightly different than the MATALB® mathematical model because the PSpice® data had only six data points at the fractions of pinhole area indicated in table 5.1 while the MATLAB® model calculated the value of V_{OC} corresponding to F between 0 and 0.01 at a rate of F=0.0001. In other words, the MATLAB® mathematical model plot had 10,000 data points and if PSpice data was done on the same number of data points, both curves would be exactly the same. The log scale of the three data sets shown in figure 5.10 shows good agreement between the MATLAB® model and the 2D PSpice® model.

5.2.2. Diode voltage profiles

The diode voltage profile plots are based on applying a voltage through the voltage source within the PSpice® model and then profiling the voltage across each diode

within the model. In some studies [29], the diode voltage profile was obtained corresponding to a voltage that is equal to the maximum voltage point (V_{MP} as shown in figure 2.3). Although, this method provides a diode voltage profile for each specific fraction of pinhole area, the diode voltage profile in each case would look similar with the only difference being the diode voltage values being different in each case corresponding to the V_{MP} at that specific F. Therefore, in addition to applying a voltage that is equal to the V_{MP} corresponding to the fraction of pinhole area being modeled, a unified voltage of 640mV that is equal to the maximum voltage point when F=0.000 was used as well for every F being modeled. This would allow better visualization of the effect of different sizes of pinholes in each case as the fraction of pinhole area changes from 0 to 1%.

Figure 5.11 shows the voltage profile across the model when no pinholes are present (F=0.000). Figures 5.12, 5.14, 5.16, 5.18 and 5.20 show the diode voltage profile of different fractions of pinhole area (F=1%, F=0.1%, F=0.01%, F=0.001% and F=0.0001%) when the applied voltage was equal to the corresponding V_{MP} in each case. Figures 5.13, 5.15, 5.17, 5.19 and 5.21 show the diode voltage profile for each F being considered when the applied voltage was 640mV in all cases. Please refer to figure 3.9 that showed a representation of the 2D model, these diode voltage profiles basically show the voltage across each diode in the model corresponding to the applied F. The voltage source is applied on the right side of the model corresponding to the side of the diode voltage profiles that with the highest voltage among the following diode voltage profiles.

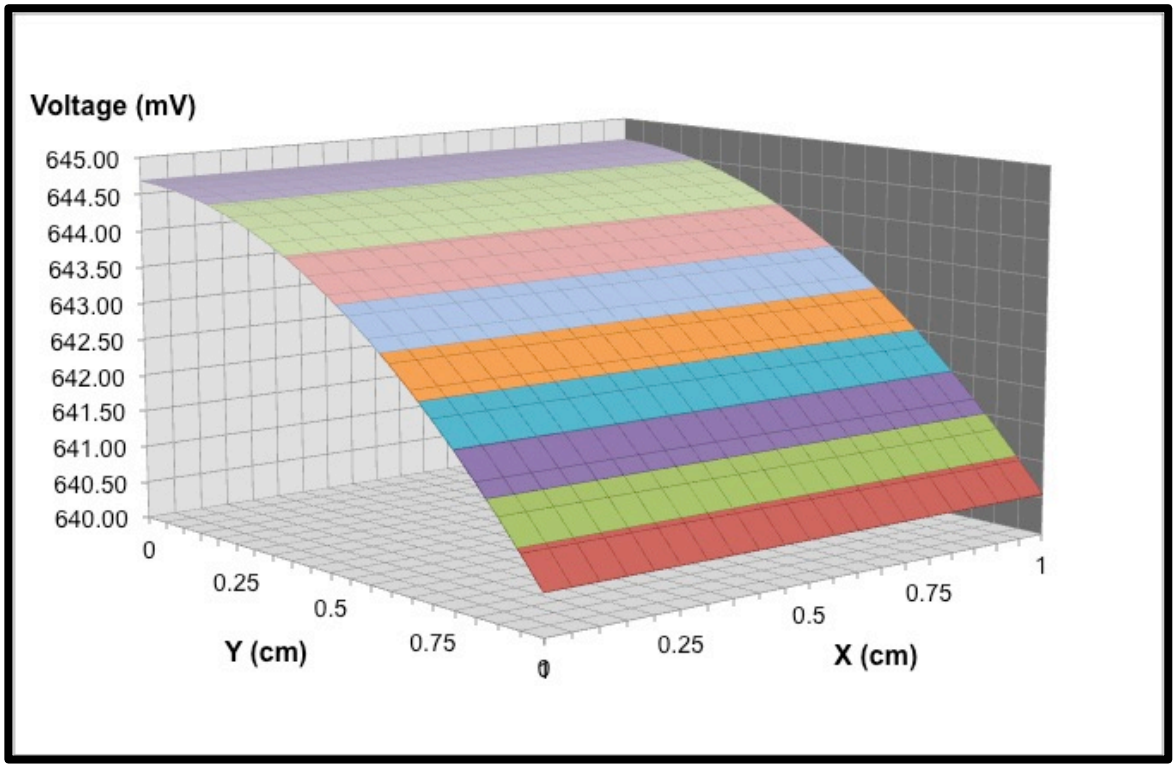

Figure 5. 11: Diode voltage profile corresponding to F=0.000, i.e., no pinholes.

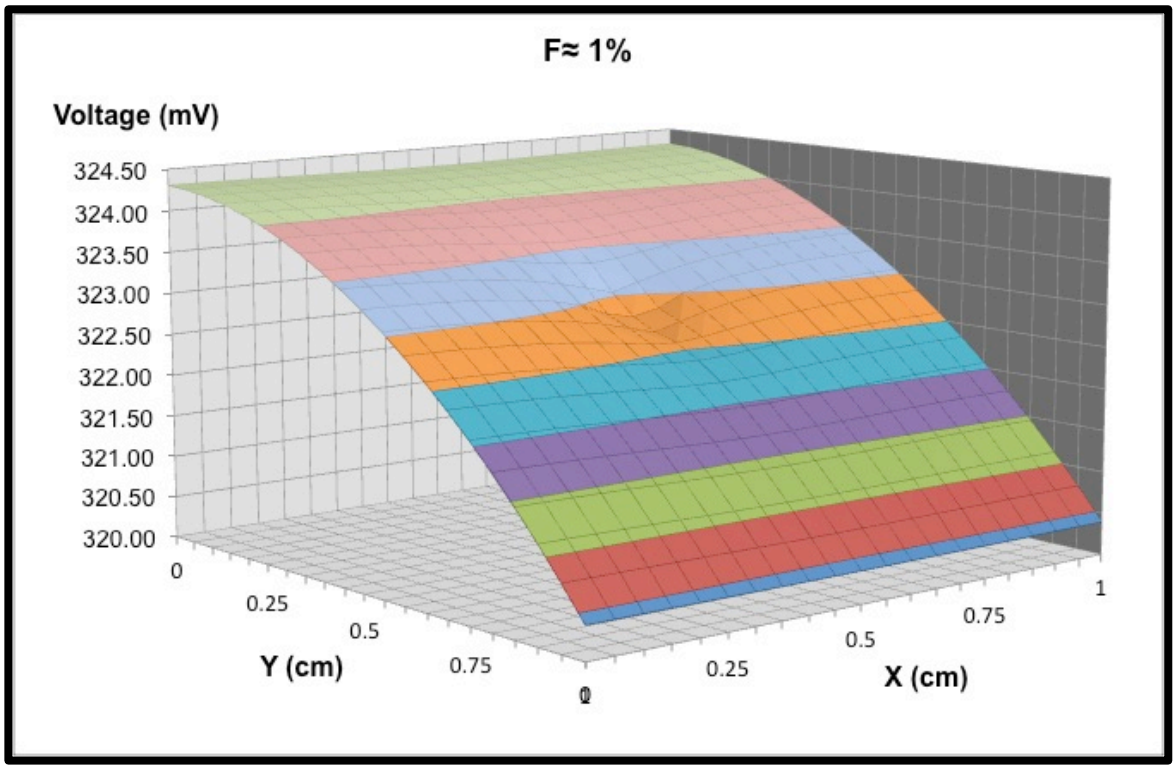

Figure 5. 12: Diode voltage profile for F=1%, biased at V_{MP}=320mV.

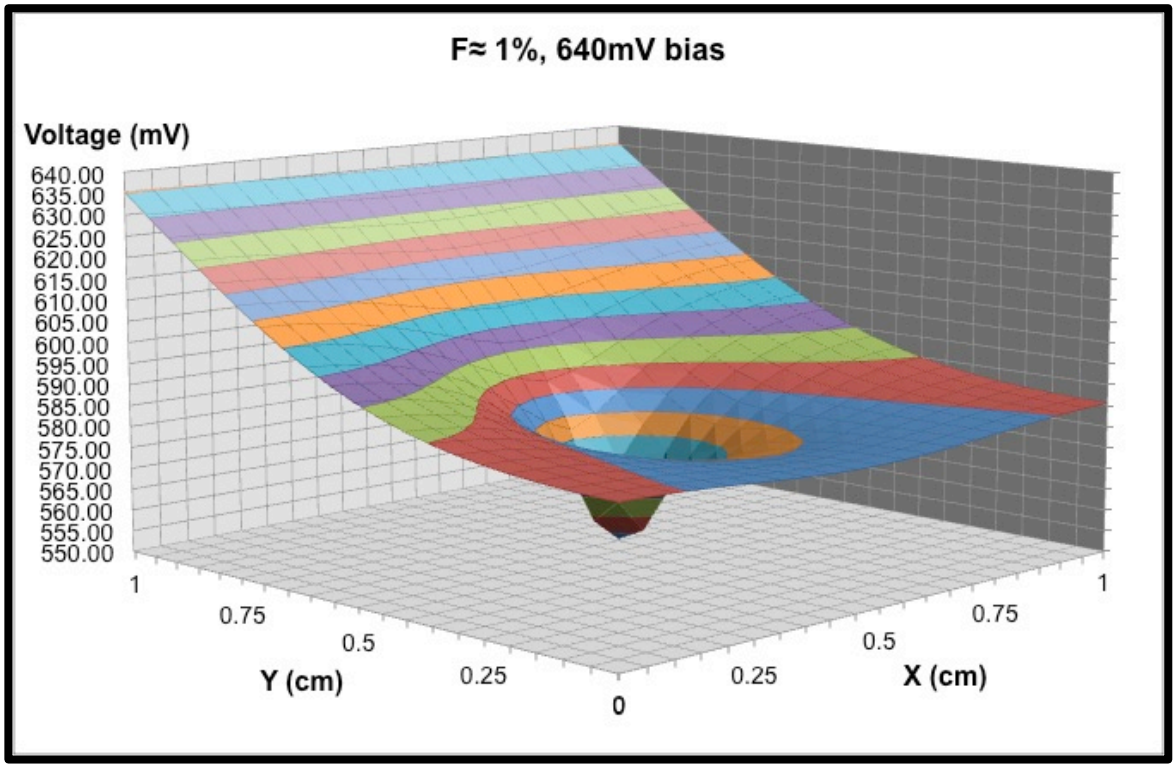

Figure 5. 13: Diode voltage profile for F=1% biased at 640mV.

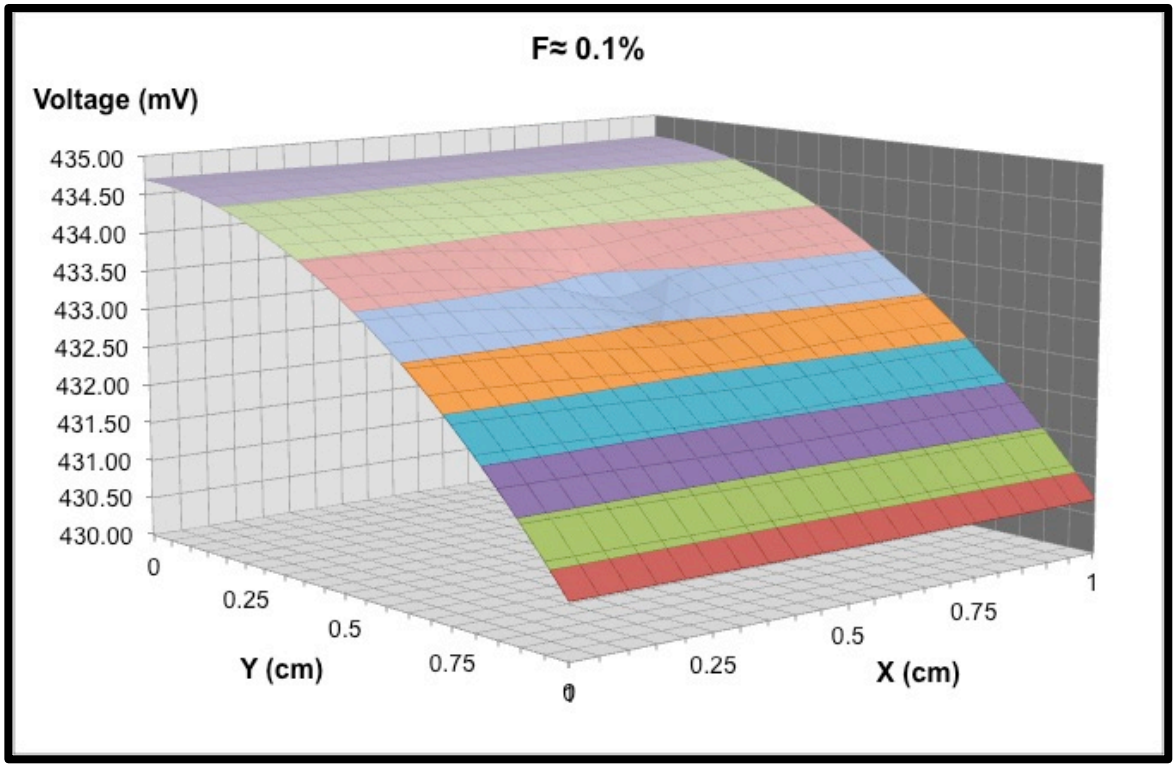

Figure 5. 14: Diode voltage profile at F=0.1%, biased at V_{MP}=430mV.

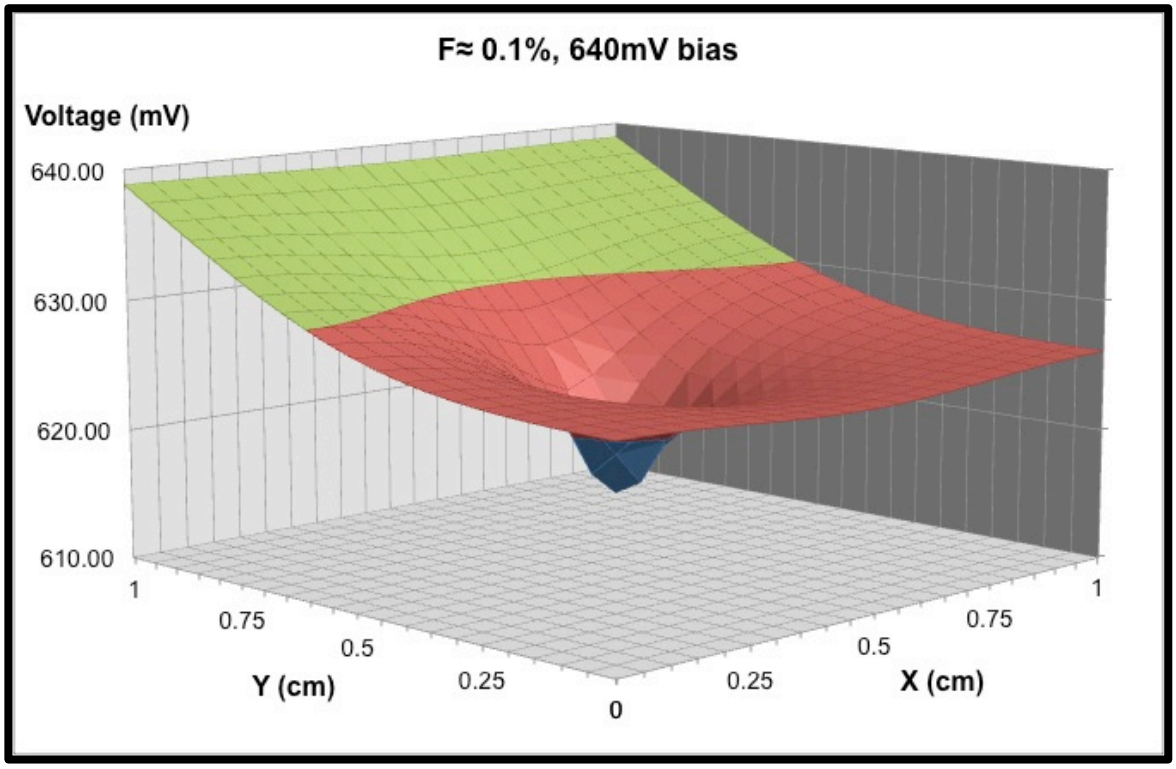

Figure 5. 15: Diode voltage profile at F=0.1%, biased at 640mV.

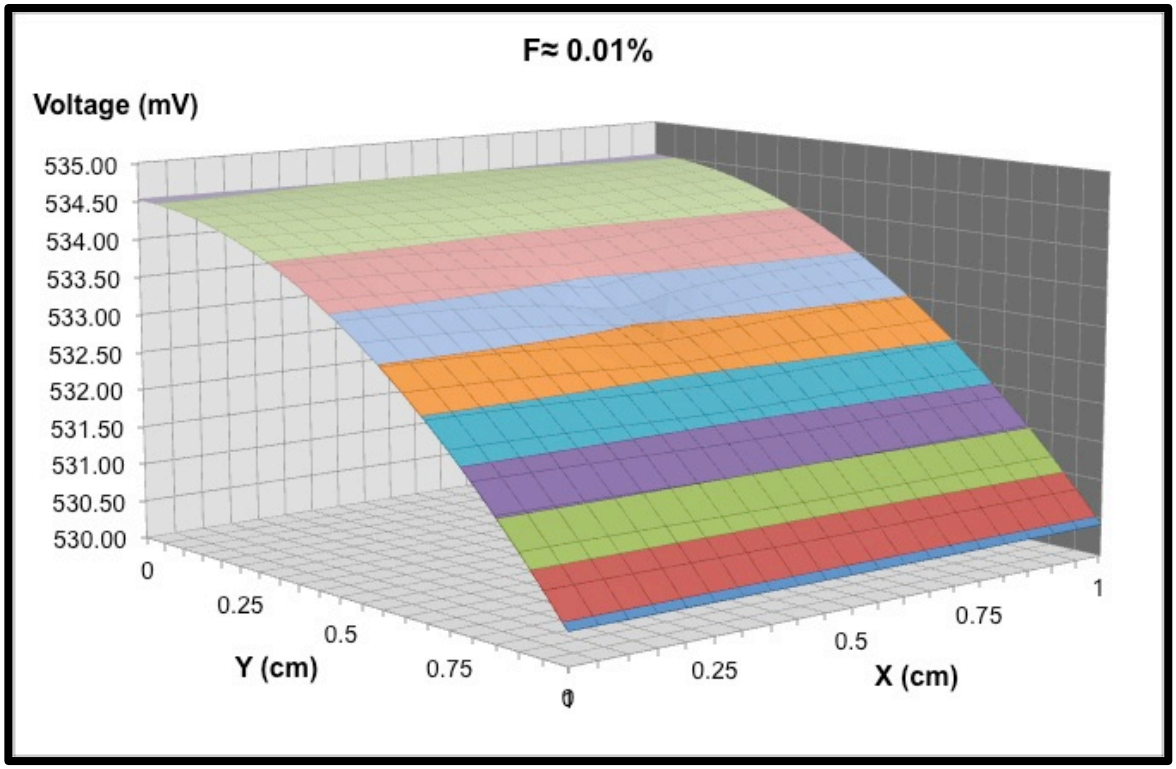

Figure 5. 16: Diode voltage profile at F=0.01%, biased at V_{MP}=530mV.

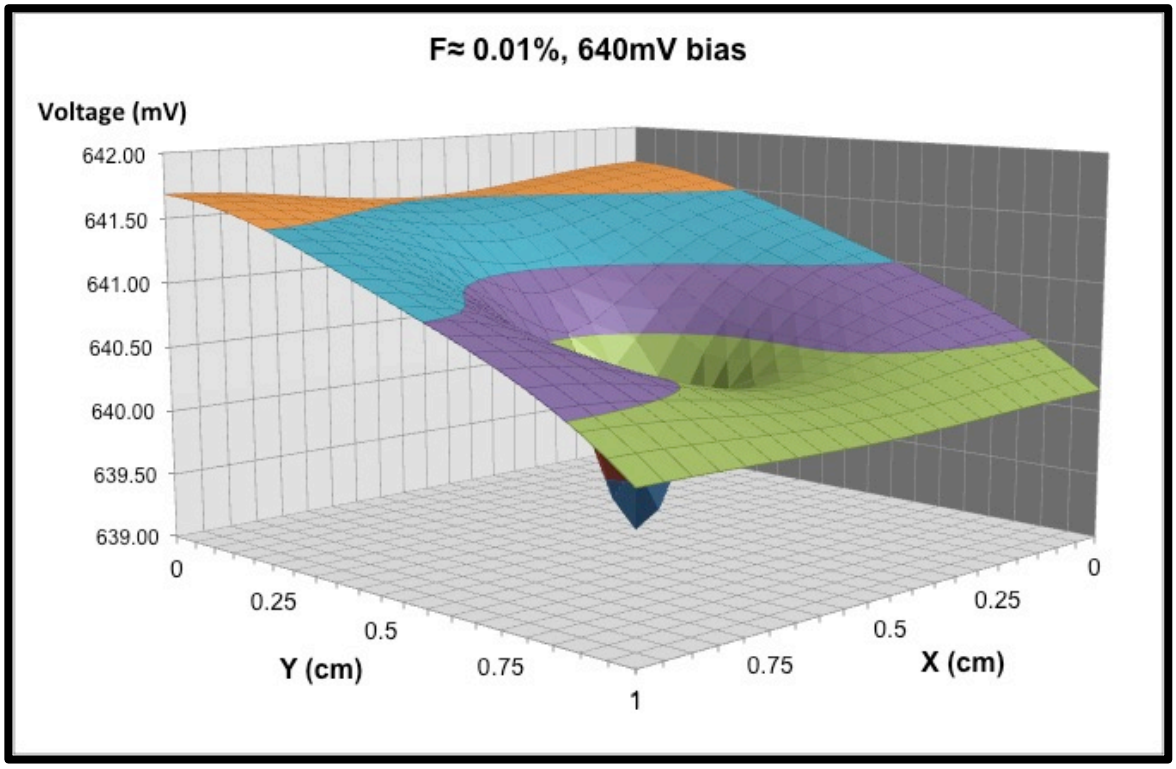

Figure 5. 17: Diode voltage profile at F=0.01%, biased at 640mV.

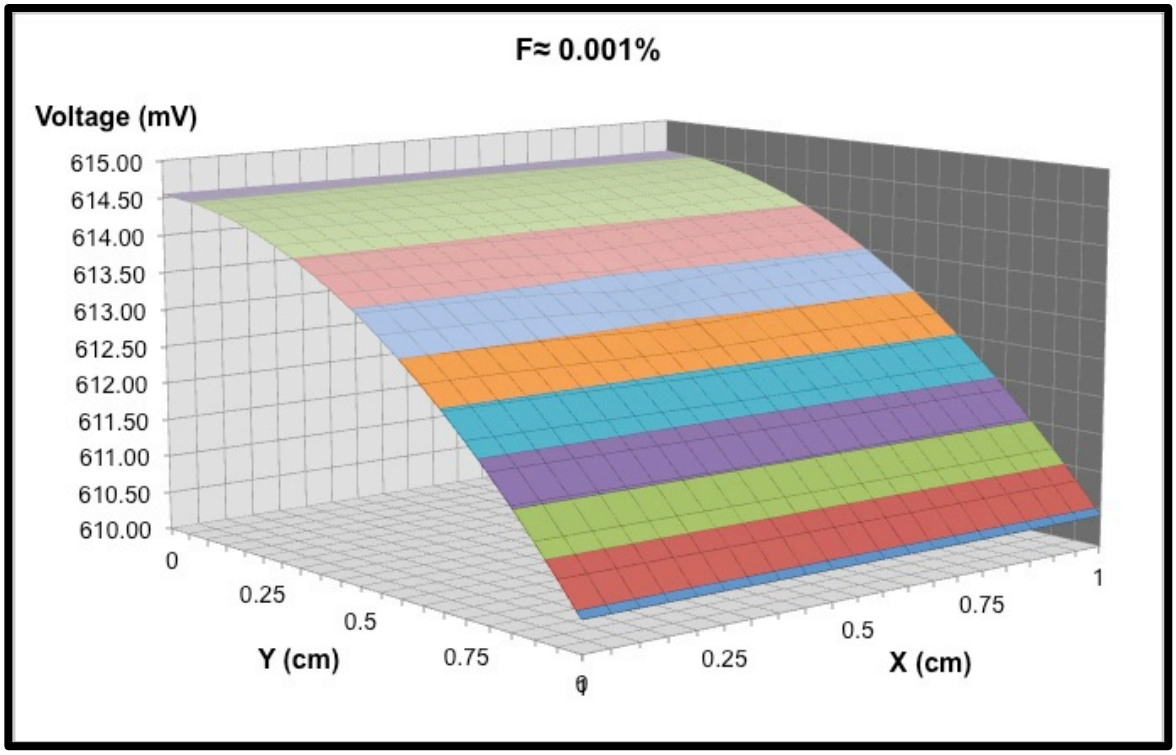

Figure 5. 18: Diode voltage profile at F=0.001%, biased at V_{MP}=610mV.

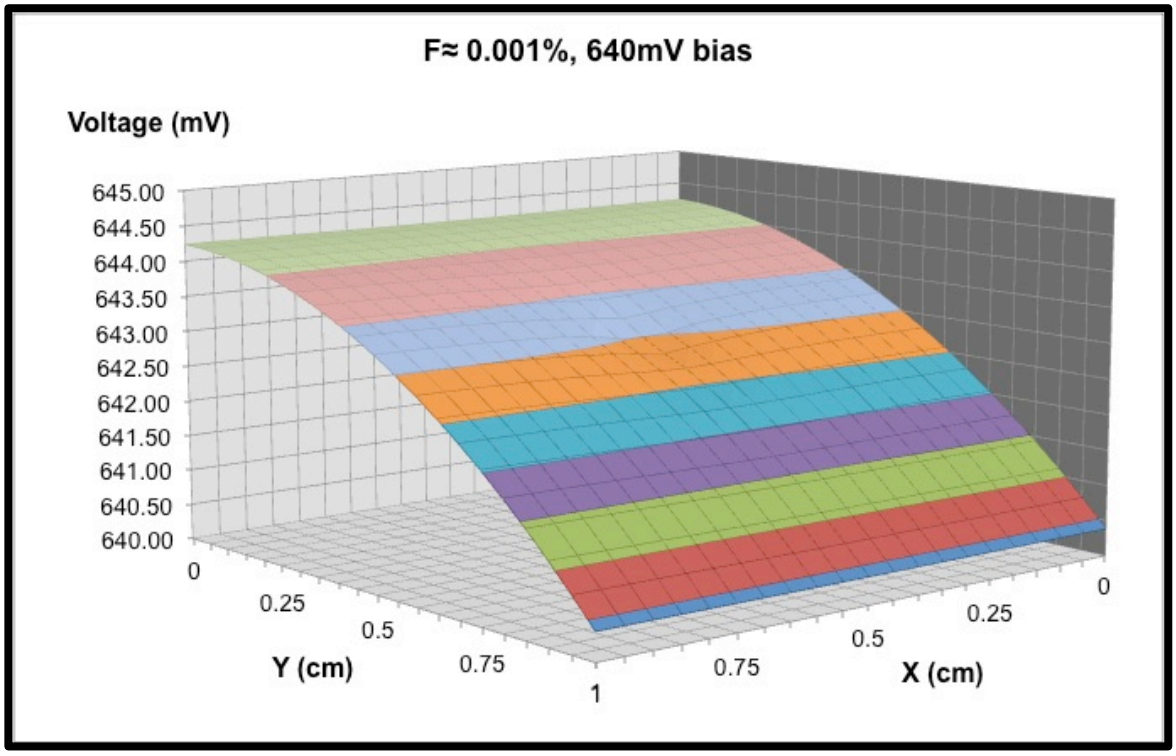

Figure 5. 19: Diode voltage profile at F=0.001%, biased at 640mV.

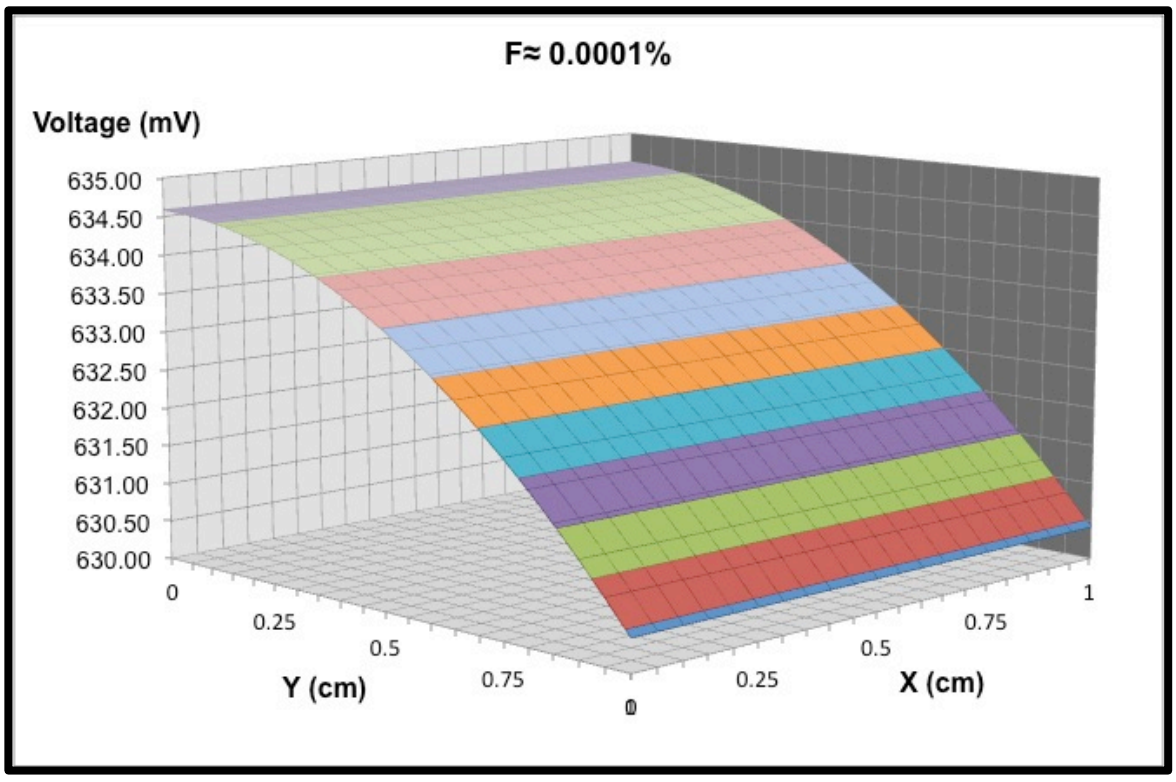

Figure 5. 20: Diode voltage profile at F=0.0001%, biased at V_{MP}=630mV.

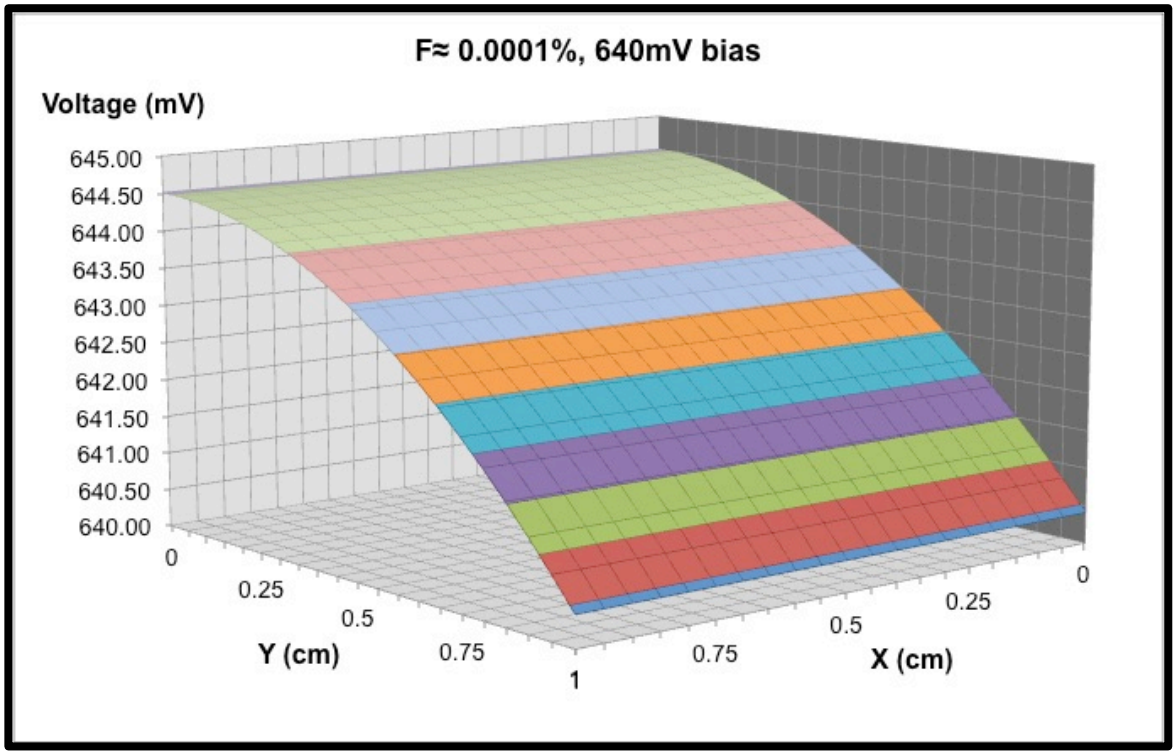

Figure 5. 21: Diode voltage profile at F=0.0001%, biased at 640mV.

Looking at figures 5.12, 5.14, 5.16 and 5.18, the diode voltage profiles look almost similar in all four cases (F=1%, F=0.1%, F=0.01%, and F=0.001%). The only difference in these figures is the values of the voltages corresponding to each F, as F becomes smaller, the voltage values of all diodes within the model increases. There is also a small dent in the diode voltage profiles corresponding to the location where the pinholes are that look almost similar in all cases. When the fraction area of pinholes reached 0.0001% as shown in figure 5.20, the dent in the diode voltage profile is not visible anymore and the profile looks similar to the diode voltage profile at F=0 with an exception. That is, the values of the voltages of the diodes across the model when F=0.0001% are lower since the voltage applied in this case corresponding to V_{MP} was 635mV.

On the other hand, considering the diode voltage profiles corresponding to each F when the applied voltage is 640mV, these profiles become completely different. Figure 5.13 shows the diode voltage profile across the model when F is 1% of the total device area. The total device area is $1cm^2$; hence the pinhole area in this case is $0.01cm^2$. The effect of this pinhole area on the diodes in the model is sever unlike figure 5.12 which shows the diode voltage profile at the same F with the voltage applied being equal to the maximum voltage point corresponding to that case (V=320mV). The effect of 1% of pinhole fraction area affects almost every diode in the model and causes sever decrease of voltage of about 90mV centered at the location of the pinhole. As the value of F becomes smaller (figures 5.15 and 5.17), the effect of the fraction of pinhole area in each case becomes less sever and the total reduction of voltage of all diodes in the model becomes less as well.

As the fraction area of pinholes becomes even less (F=0.001%), the diode voltage profile (figure 5.19) becomes similar to the diode voltage profile when F=0 with the exception of a small dent at the location of the pinholes within the model. Furthermore, reducing F even further to 0.0001% (figure 5.21), the diode voltage profile looks exactly the same as the diode voltage profile corresponding to zero pinhole area.

Based on these diode voltage profiles, one can conclude that the most tolerable fraction area of pinholes that would not affect the device severely would be a pinhole area that is equal to 0.001% of the total device area. In a $1cm^2$ device, this would a total pinhole area of $1000\mu m^2$ ($0.001mm^2$). Furthermore, if introducing deliberate pinholes was a practical and applicable approach, the smallest pinhole area that would show

significant impact on the voltage of the device would be corresponding to F=0.01%, that is a pinhole area of 10,000μm^2 or (0.01mm^2) in a device having a total area of 1cm^2.

Thus, based on the results outlined in this chapter, it can be concluded that pinholes can be observed in full devices by incorporating EL and LBIC at different laser beam wavelengths. It seemed that pinholes in completed devices could affect an area that is as large as 15 times the area of the pinholes. Moreover, it was shown that the open circuit voltage loss due to pinholes predicted by the 1998 NREL IEC report is applicable to CdS films deposited by closed space sublimation at the lab taking into consideration different parameters corresponding to the good and weak diode according to devices made in the lab. Finally, diode voltage profiles showed that any fraction of pinhole area smaller or equal to 0.001% of the total device area would be tolerable and would not affect the device severely. Some discussion about these results is provided in the next chapter.

Chapter 6

Discussion

There are some interesting and somewhat unexpected results indicated in chapter 4 and 5; some discussion about these results is provided here within. These results are: a) the finding that grain coalescence and TCO surface roughness not being source of pinholes in CdS films investigated in this study, b) the outcome that cleaning residues being the dominant source of pinholes in these CdS films, c) the statistical evidence that thicker CdS films tend to have more pinholes than thinner CdS films, d) the size effect of pinholes and e) the difference in V_{OC} as a function of the fraction of pinhole area (F) for experimental data compared to the findings of the 1998 NREL IEC report [13].

6.1. Natural sources of pinholes

Most literature about pinholes in CdS films refers to the natural sources of pinholes being the most likely cause of pinholes. However, there are many deposition methods that can be used to deposit the layers of CdTe solar cells as discussed in chapter 2. Chemical bath deposition (CBD) is one of the most widely used CdS film deposition methods. CdS films investigated in this study were all deposited via closed space sublimation (CSS). At the Materials Engineering Lab at Colorado State University, a deposition chamber referred to as the ARDS (Advanced R&D Deposition System) is used to deposit the various layer of CdTe solar cells and all films are deposited by CSS. This setup was chosen to serve as an inline continuous deposition process where all layers of the device are deposited within one chamber and within the same vacuum boundaries.

Thus, it seems that based on the SEM and EDS results indicated in chapter 4, the setup discussed above eliminates the natural sources of pinholes in CdS films and these natural sources of pinholes may be more dominant in CdS films deposited via different deposition methods. The limitation of the study on the other hand is only considering CdS films deposited by CSS. In order to make a conclusive statement about the natural sources of pinholes in CdS films, one needs to consider CdS films deposited via different deposition techniques and study these CdS films for pinholes. Nevertheless, as seen in this study, grain coalescence and TCO surface roughness being natural sources of pinholes did not cause any pinholes in CdS films deposited by CSS.

6.2. Cleaning residues

The dominant sources of pinholes as shown in chapter 4 was found to be cleaning residues. TEC10 glass substrates that are used for depositing all CdS films investigated in this study seem to have some residues that were not eliminated by the standard cleaning method. These residues believed to affect the surface quality of the TCO obstructing CdS film growth and thus allow formation of pinholes. Plasma cleaning by definition is both physical and chemical surface etching process and statistical evidence shown in chapter 4 indicates that cleaning glass substrates with plasma reduces pinhole significantly.

On the other hand, dust and particulates in open lab environment was not found to be a major source of pinholes as indicated in the same chapter although the number of dust and particulates was significantly reduced within the mini-environment. The reasoning behind this outcome is the quality of the cleaning process within the mini-

environment. Though, the mini-environment as a setup and not as a cleaning method could have an influence on the results of pinholes in CdS films deposited on standard cleaned and plasma cleaned substrates. This is explained next.

TEC10 glass substrates that were used to study the effects of standard cleaning were stored inside the mini-environment after cleaning and were transferred to the load lock for film deposition without being exposed to open lab environment prior to film deposition. On the other hand, TEC10 glass substrates that were used to study the effects of plasma cleaning were stored inside the mini-environment (after being cleaned with the standard cleaning method) and then transferred to the load lock for plasma cleaning. Film deposition again takes pace without ever exposing these substrates to open lab environment.

In this sense, it is believed that the mini-environment had an important role in the significant reduction of pinholes in CdS films deposited on substrates cleaned by the two mentioned cleaning methods. It would be interesting if one could improve the quality of the cleaning process done within the mini-environment and observe the effect of that on CdS films deposited on such substrates. It seems logical to conclude that the best way to ensure that CdS films of various thicknesses have minimal pinholes is cleaning the glass substrates by plasma cleaning and maintain these substrates in a class 1 mini-environment to eliminate any pinhole formation due to dust and particulates floating in open lab environment.

6.3. High pinhole density in thick CdS films

Another unexpected result was shown in chapter four regarding pinhole density in CdS films of different thicknesses. Statistical results showed that there was a 95%

probability that the thick CdS films have more pinholes than thin CdS films. There were two factors that may have induced this effect. These are the growth rate of thick CdS films as compared to thin CdS films and the effectiveness of the images obtained by the optical microscope for different film thicknesses.

The deposition process of the films as indicated earlier was done by CSS. Conventionally in CSS, one could control both the deposition duration and the deposition temperature to influence the growth rate of the film and consequently the film thickness. The thickness of CdS films deposited in this study was controlled by adjusting the deposition temperature while keeping the deposition time constant across all film thicknesses. A higher bottom source temperature would yield a thick CdS films and a lower temperature would yield a thinner film. As a result, thick CdS films have higher growth rates as compared to thin CdS films. Considering this fact and the statistical evidence that thicker CdS films have more pinholes indicates the possibility that higher growth rates render bad film quality. It seems that the first deposited film layer does not achieve full TCO surface coverage and subsequent film layers are deposited on top of that first layer leaving the TCO exposed and thus forming pinholes. This can be investigated by depositing both thick and thin CdS films with the same growth rate by adjusting both deposition time and deposition temperature.

On the other hand, based on the transmission curves of different CdS film thicknesses as compared to the transmission curve of the blue light filter used in this study (figure 3.2), it would be expected that identifying pinholes in thicker would be easier based on the difference in the contrast of the thin and thick CdS films. Nevertheless, this effect was averted by controlling the intensity of the transmitted light

in the optical microscope. In other words, more light was allowed to be transmitted when studying thin CdS films and the same was reduced for thick CdS films. In addition, to ensure that this outcome is not the results of optical microscope limitations or the difference in film contrasts, most thin CdS films were studied more than once and more carefully to increase the integrity of the results and ensure that the result of fewer pinholes in thin CdS films is not artificially concluded. Finally, the process of reducing images to black and white was maintained the same for all CdS films thicknesses and this should help validate the results of the study even further.

6.4. Size effect of pinholes and V_{OC} loss models

The size effect of pinholes was reported in chapter 5 where it was shown that a pinhole might affect an area of the actual device that is as big as 15 times the area of the pinhole. In addition, comparison among the 1D MATLAB® mathematical model, the 2D PSpice® model and the data from the 1998 NREL IEC report [13], showed that the cited data showed less V_{OC} loss for each corresponding fraction of pinhole area (F) as F ranged between zero and 0.01. More details about these results are discussed next.

Pinhole size effects were concluded based on studying CdTe devices that were manufactured at process of record (POR) conditions. In other words, the best-known recipe for a CdTe lab-scale solar cell at the time of the experiment was used to manufacture these devices. The open circuit voltage of the devices made on one substrate ranged between 775mV to about 720mV; both devices were studied with LBIC and EL to identify any possible pinholes. The pinhole used to estimate the size effects of pinholes was observed in the lower V_{OC} device whereas no pinholes were observed in the LBIC scans of the other device. This effort was a first step into

estimating the size effects of pinholes. In order to further validate this result and may be obtain a better understanding of the size effects of pinhole, one should consider repeating the experiment with more devices and also consider devices made with different CdS film thicknesses. This should provide a better estimation of the size effects of pinholes in addition to finding any relation between CdS film thickness and pinhole size effects.

Open circuit voltage loss as described in chapter 5 showed good agreement among the three data sets (MATLAB® 1D model, PSpice® 2D model and [13]). The two simulated models (MATLAB® 1D model, PSpice® 2D model) had almost exactly the same trend as shown in figures 5.9 and 5.10. The main difference was observed when comparing both simulated models to the 1998 NREL IEC report [13]. V_{OC} loss based on the simulated models seemed to be higher for every corresponding value of F. This was justified due to the values of V_{OC} and J_{SC} for the good and weak diodes used for the simulation as described earlier as well as the difference in the transparent conductive oxide used for devices made in this study and devices used for the results of the IEC report. In addition, the parameters for the good diode were used for a device with the best efficiency of the time and assuming that this particular device had no pinholes.

In order to get better results and possibly reduce the difference in V_{OC} as a function of F among the three data sets, one may consider the following. First, obtaining V_{OC} for the good diode from a device that is deposited on a plasma-cleaned substrate thus eliminating the assumption of no pinholes. Second, calibrating the process conditions for both the device made on plasma-cleaned substrates as well as the device that has

no CdS. This should promote the best possible good and weak diode parameters and thus show a better agreement with the data from the 1998 NREL IEC report.

Thus in this chapter, some of the results indicated in this dissertation were discussed in details. In addition, some discussion was provided as to the factors that may have influenced these results and the validity of the implemented methods. Finally, some limitations of the study that might have caused some of these results were also discussed in addition to some approaches by which better results can be achieved.

Chapter 7

Conclusions and Future Work

Being one of the best thin film solar cells, CdTe solar cells need some improvements in order to be a major type of solar cells in the World. Despite its perfect band gap that is a very close match to the sun's spectrum and all other good aspects of CdTe, the efficiency of these solar cells lag behind solar cells made of similar band gap materials. One of the main reasons of this lag is the voltage deficit of CdTe solar cells as discussed in chapter 2. Improving the open circuit voltage of the device and its short circuit current can increase the efficiency of CdTe solar cells. The window layer material (CdS) can influence these two factors tremendously. A thick (about 200nm) CdS layer insures high V_{OC} provided good properties of the remaining layers of the solar cell but limits the amount of photons that could reach the p-n junction of the solar cells and thus limiting the generated photocurrent. On the other hand, thin CdS layer allow more photons to reach the p-n junction, producing higher photocurrent but V_{OC} of the device is reduced. This reduction of V_{OC} is based on assuming that thin CdS films are full of defects and discontinuities that allow formation of parallel weak diodes between the CdTe on top and the transparent conductive oxide (TCO) layer beneath. These defects in the CdS films that allow the formation of the weak CdTe/TCO diode are known as pinholes. It was necessary to determine whether pinholes in CdS films of different thicknesses can be eliminated, whether thinner CdS film layers have more pinholes than thick ones, and whether pinhole size effect can be identified either by analytical procedures or by computer simulations.

The sources of pinholes were identified and discussed through out this thesis. Through experiment and analysis, it was concluded that the natural sources of pinholes being grain coalescence and TCO surface roughness were not sources of pinholes in the CdS film made in the lab through closed space sublimation. Furthermore, the results of the statistical tests indicated that among all artificial sources of pinholes, cleaning residues was the most dominant sources of pinholes in CSS deposited CdS films. Statistics results also suggested that the best way to get rid of these residues and eliminate pinholes in CdS films was to clean the substrates with plasma prior to film deposition. Considering the thickness of CdS and the formation of pinholes, statistical evidence showed that thinner CdS films tend to have less pinhole area than thicker CdS films. As a result, higher deposition rates of the window layer material via closed space sublimation seem to be favorable conditions for pinhole formation.

The Pinhole size effect results were discussed in chapter 5. The obstacle was observing pinholes in full devices and confirming that what is assumed to be a pinhole is actually a pinhole. Some small area devices were studied using electroluminescence (EL) and some defects were identified. Light Beam Induced Current (LBIC) scans of different wavelengths allow scanning different layers of the device and obtaining a definitive confirmation whether a certain defect is a pinhole or not. Using this method, the pinhole size effect in CdTe solar cells was estimated to be about 15 times larger than the actual area of the pinhole.

PSpice simulations were used to verify the effect of different fractions of pinhole area on the open circuit voltage of the device and to visualize the effect of these pinhole areas on the diode voltage profile across the solar cell. These simulations showed that

total pinhole area that is equal to 1% of the total device area would reduce V_{OC} by about 340mV and this V_{OC} reduction were shown to be less sever as the fraction of pinhole area became less and less. Furthermore, a MATLAB® mathematical model was built to graph the effect of the fractions of pinhole area on V_{OC} by utilizing actual device parameters (V_{OC} and J_{SC}). Subsequently, both the PSpice simulation and the MATLAB® model showed acceptable agreement with the literature.

Finally, diode voltage profiles obtained by PSpice® simulations indicated that any pinhole area that is equal or less than 0.001% of the total device area would not cause any sever damage to the diode voltage profile of the solar cell and would not cause more than 30mV of V_{OC} loss. Also, these diode voltage profiles indicated that the smallest pinhole area that would severely affect the voltage across the device would be equal to about 0.01% of the total device area by which the open circuit loss was estimated to be around 110mV.

Thus, this work discussed sources of pinholes in CSS deposited CdS films and methods to study these pinholes in addition to reducing and eliminating them by controlling the cleaning process of the glass substrates. A set of useful results and recommendations were obtained from studying CdS films of different thicknesses, parameters obtained from actual CdTe small area devices as well as simulations through PSpice® and MATLAB®.

The subjects of pinholes in CSS deposited CdS films and effects of pinholes can be further advanced by considering investigating the nature of cleaning residues in TEC10

glass substrates, by studying the effects of plasma cleaning on actual devices with varying CdS film thickness, and by studying the electronic effects that may occur in thin CdS films. It would be interesting to study the surface of the glass substrates before and after plasma cleaning and compare those results to the surface conditions of the glass substrates before and after standard cleaning. This would allow identifying the nature and source of the cleaning residues and that may allow depositing CSS CdS films of all thicknesses that are free of pinholes. Considering plasma cleaning, it would be useful and interesting to manufacture CdTe devices on plasma-cleaned substrates at various CdS film thicknesses and visualize the relation between V_{OC} and CdS film thickness.

On the other hand, the evidence that thin CdS films have less pinholes and the loss of V_{OC} as the CdS film thickness is reduced is a strong indication of electronic effects being a major reason behind this voltage loss. Future work should focus onto studying these electronic effects in thinner CdS films. Some of these electronic affects include the interface states between CdS and the TCO that causes bending of the band. It seems that there is a certain CdS film thickness at which this band bending occurs because some film thickness is affected electronically. It would be very beneficial if this can be adjusted and improved, consequently thinner CdS films can be deposited to increase the short circuit current of the device without compromising any open circuit voltage and thus increase the efficiency of CdTe solar cells.

References

[1] K. Zweibel, *Harnessing Solar Power - The Photovoltaics Challenge*. New York: Plenum Press, 1990.

[2] J. Russell. (2010, Oct. 20, 2010). *Record Growth in Photovoltaic and Momentum Builds for Concentrating Solar Power* [Article]. Available: http://vitalsigns.worldwatch.org/vs-trend/record-growth-photovoltaic-capacity-and-momentum-builds-concentrating-solar-power

[3] Solar Power at the Crossroads: Photovoltaic markets saw record growth in 2011, but industry faces short-term challenges**,** European Photovoltaic Industry Association, 2011. Available: http://www.epia.org/press-room/epia-press-releases.html

[4] J. R. Sites, "Characterization and Analysis of CIGS and CdTe Solar Cells: December 2004 - July 2008," NREL/SR-520-44811; Other: XXL-5-44205-03; TRN: US200906%%72 United States10.2172/947438Other: XXL-5-44205-03; TRN: US200906%%72Thu Apr 09 07:12:10 EDT 2009NREL; RN09031616English, 2009.

[5] D. Albin*, et al.*, "Comparison study of close-spaced sublimated and chemical bath deposited CdS films: Effects on CdTe solar cells," in *Proceedings of the 1997 IEEE 26th Photovoltaic Specialists Conference, September 29, 1997 - October 3, 1997*, Anaheim, CA, USA, 1997, pp. 367-370.

[6] M. D. Archbold*, et al.*, "Development of low temperature approaches to device quality CdS: A modified geometry for solution growth of thin films and their characterisation," *Thin Solid Films,* pp. 2954-2957, 2007.

[7] G. Contreras-Puente*, et al.*, "Micro and nano-bricklayer building process of CdS films: Their optimal applications in CdTe solar cells," in *2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, WCPEC-4, May 7, 2006 - May 12, 2006*, Waikoloa, HI, United states, 2007, pp. 457-460.

[8] S. Kumazawa*, et al.*, "15.1% highly efficient thin film CdS/CdTe solar cell," *Solar Energy Materials and Solar Cells,* vol. 49, pp. 205-212, 1997.

[9] M. A. Matin*, et al.*, "Ultra Thin High Efficiency CdS/CdTe Thin Film Solar Cells from Numerical Analysis," in *Mathematical Methods, Systems Theory and Control*, L. Perlovsky*, et al.*, Eds., ed, 2009, pp. 338-344.

[10] A. Romeo*, et al.*, "Influence of CdS growth process on structural and photovoltaic properties of CdTe/CdS solar cells," *Solar Energy Materials and Solar Cells,* vol. 67, pp. 311-321, 2001.

[11] W. Song*, et al.*, "Effect of $CdCl_2$ treatment of CdS films on CdTe/CdS solar cells," in *Proceedings of the 1996 MRS Spring Symposium, April 8, 1996 - April 11, 1996*, San Francisco, CA, USA, pp. 331-336, 1996.

[12] M. Tsuji*, et al.*, "Characterization of CdS thin film in high efficient CdS/CdTe solar cells," *Journal of Crystal Growth,* vol. 214, pp. 1142-1147, 2000.

[13] R. W. Birkmire*, et al.*, "Optimization of Processing and Modeling Issues for Thin-Film Solar Cell Devices.," Institute of Energy Conversion, University of Delaware, Newark, Delaware NREL/SR-520-25845, 1998.

[14] L. Chen, "Random Deposition Model of CdS Layer in CdS/CdTe Thin-Film Solar Cells," Master of Sceince, Department of Physics, Colorado State University, Fort Collins, 2008.

[15] A. R. Davies*, et al.*, "All-CSS processing of CdS/CdTe thin-film solar cells with thin CdS layers," in *2007 MRS Spring Meeting, April 9, 2007 - April 13, 2007*, San Francisco, CA, United states, pp. 157-162, 2007.

[16] C. S. Ferekides*, et al.*, "High efficiency CSS CdTe solar cells," *Thin Solid Films,* vol. 361-362, pp. 520-526, 2000.

[17] J. E. Granata*, et al.*, "Effect of CdS thickness on CdS/CdTe quantum efficiency," in *25th PVSC*, Washington, D.C., 1996.

[18] V. V. Plotnikov*, et al.*, "Dependence CdS/CdTe solar cells efficiency and nonuniformity on CdS layer thickness," in *Pvsc: 2008 33rd Ieee Photovoltaic Specialists Conference, Vols 1-4*, pp. 762-763, 2008.

[19] J. L. Gray, "The Physics of Solar Cells," in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Eds., ed: John Wiley & Sons, pp. 61-112, 2003.

[20] B. E. McCandless and J. R. Sites, "Cadmium Telluride Solar Cells," in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Eds., ed: John Wiley & Sons, pp. 618-662, 2003.

[21] G. Koishiyev, "Analysis of impact of non-uniformities on thin-film solar cells and modules with 2D simulations," PhD dissertation, Department of Physics, Colorado State University, Fort Collins, 2010.

[22] "2010 Solar Technologies Market Report", U.S. Department of Energy, Energy Effeciency and Renewable Energy, November 2011.

[23] M Green, K. Emery, Y. Hishikawa, W. Warta and E. Dunlop, "Solar Cell Efficiency Tables (version 40)", *Progress in Photovoltaics: Research and Applications*, Vol. 20, pp. 606-614, 2012.

[24] C. Ferekides*, et al.*, "Effect of SnO_2 roughness on the properties of CdTe/CdS solar cells," in *Proceedings of the 1997 IEEE 26th Photovoltaic Specialists Conference, September 29, 1997 - October 3, 1997*, Anaheim, CA, USA, 1997, pp. 427-430.

[25] C. S. Ferekides*, et al.*, "CDS films prepared by the close-spaced sublimation and their influence on CdTe/CdS solar cell performance," in *Proceedings of the 1996 25th IEEE Photovoltaic Specialists Conference, May 13, 1996 - May 17, 1996*, Washington, DC, USA, 1996, pp. 751-756.

[26] F. S. Hasoon*, et al.*, "The Morpgology of CdS thin films deposited on SnO_2-coated glass substrates," ed, 2007.

[27] H. Ohyama*, et al.*, "16.0% efficient thin-film CdS/CdTe solar cells," in *Proceedings of the 1997 IEEE 26th Photovoltaic Specialists Conference, September 29, 1997 - October 3, 1997*, Anaheim, CA, USA, 1997, pp. 343-346.

[28] F.-J. Kuhlmann, "Deposition of SnO_2 thin films using reactive RF sputtering," master of science, Electrical and Computer Engineering, The University of Texas, El Paso, 2004.

[29] X. Li*, et al.*, "The Effect of High-Resistance SnO_2 on CdS/CdTe Device Performance," 1999.

[30] J. J. Gandia*, et al.*, "Influence of TCO dry etching on the properties of amorphous-silicon solar cells," *Journal of Materials Processing Technology,* vol. 143, pp. 358-361, 2003.

[31] J. Schindelin, I. Arganda-Carreras, E. Frise, V. Kaynig, M. Longair, T. Pietzsch, S. Preibisch, C. Rueden, S. Saalfeld, B. Schmid, J.Y. Tinevez, D.J. White, V. Hartenstein, K. Eliceiri, P. Tomancak and A. Cardona (2012) Fiji: an open-source platform for biological-image analysis, *Nature Methods* 9(7): 676-682

[32] D. Swanson, R. Lutze, W.S. Sampath and J. Williams, "Plasma Cleaning of TCO surfaces Prior to CdS/CdTe Deposition", 2012 IEEE PVSC Conference, June 3-8, 2012, Austin, Tx, USA.

[33] OrCAD PSpice®, Electronic Design Software, EMA Design Automation, 225 Tech Park Drive, Rochester, NY 14623.

[34] W. Brooks, S. Irvine and V. Barrioz, " High-resolution laser beam induced current measurements on Cd0.9Zn0.1S/ CdTe solar cells," Energy Procedia, vol. 10, pp.

232-237, 2011.

[35] L. Castañer and S. Silvestre, "Modelling Photovoltaic Systems Using PSpice®.", John Wiley & Sons, pp. 1-99, 2002. Online version available at: http://www.knovel.com/web/portal/browse/display?_EXT_KNOVEL_DISPLAY_bookid=2113&VerticalID=0

[36] http://www.gel.usherbrooke.ca/casino/What.html

[37] R. Ott and M. Longnecker, "An Introduction to Statistical Methods and Data Analysis", Duxbury, 2001.

Appendix A: Images of CdS films

This appendix shows examples of CdS film images upon reducing these images to black and white to emphasize and show pinholes. Images of CdS films of different thicknesses (200nm, 100nm and 50nm) studied in the paper with Blue Light Transmission with optical microscopy are shown. These shown CdS film images are for films deposited standard cleaned substrates, mini-environment cleaned substrates as well as plasma cleaned substrates. Table A.1 shows a summary of the below images with corresponding film thickness, cleaning method and pinhole area. Note that the images in this appendix and data indicated in the table are just examples of the CdS film images used with the statistics procedure outlined in this dissertation where ANOVA takes into consideration the pinhole area form all images (135 image per film thickness per cleaning method).

Table A. 1: Summary of images within this appendix.

Image	Film thickness	Cleaning method	Pinhole area (μm^2)
A. 1	200nm	Plasma	20
A. 2	200nm	Plasma	50
A. 3	200nm	Standard	197
A. 4	200nm	Standard	231
A. 5	200nm	Standard	428
A. 6	200nm	Mini-environment	45.5e3
A. 7	200nm	Mini-environment	941
A. 8	200nm	Mini-environment	1130
A. 9	100nm	Plasma	30
A. 10	100nm	Plasma	14
A. 11	100nm	Plasma	8
A. 12	100nm	Standard	193
A. 13	100nm	Standard	486
A. 14	100nm	Standard	Blue image
A. 15	100nm	Standard	13e3
A. 16	100nm	Mini-environment	163
A. 17	100nm	Mini-environment	2,400

Image	Film thickness	Cleaning method	Pinhole area (μm^2)
A. 18	100nm	Mini-environment	1,370
A. 19	50nm	Plasma	3
A. 20	50nm	Plasma	18
A. 21	50nm	Plasma	2
A. 22	50nm	Standard	179
A. 23	50nm	Standard	188
A. 24	50nm	Standard	730
A. 25	50nm	Mini-environment	80
A. 26	50nm	Mini-environment	90
A. 27	50nm	Mini-environment	127

A.1. 200nm CdS films

A.1.1. Plasma cleaned substrates

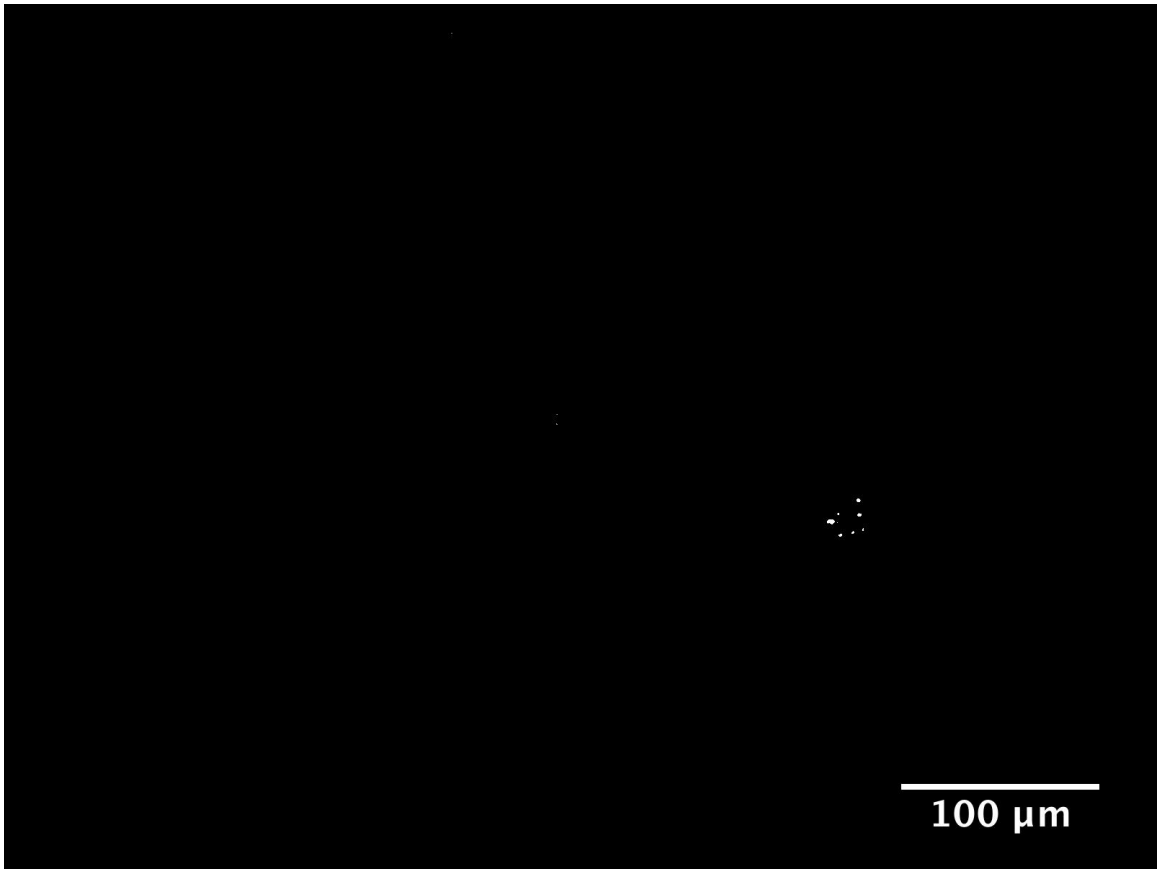

Figure A. 1: Total pinhole count is 11 and total pinhole area is about 20μm^2.

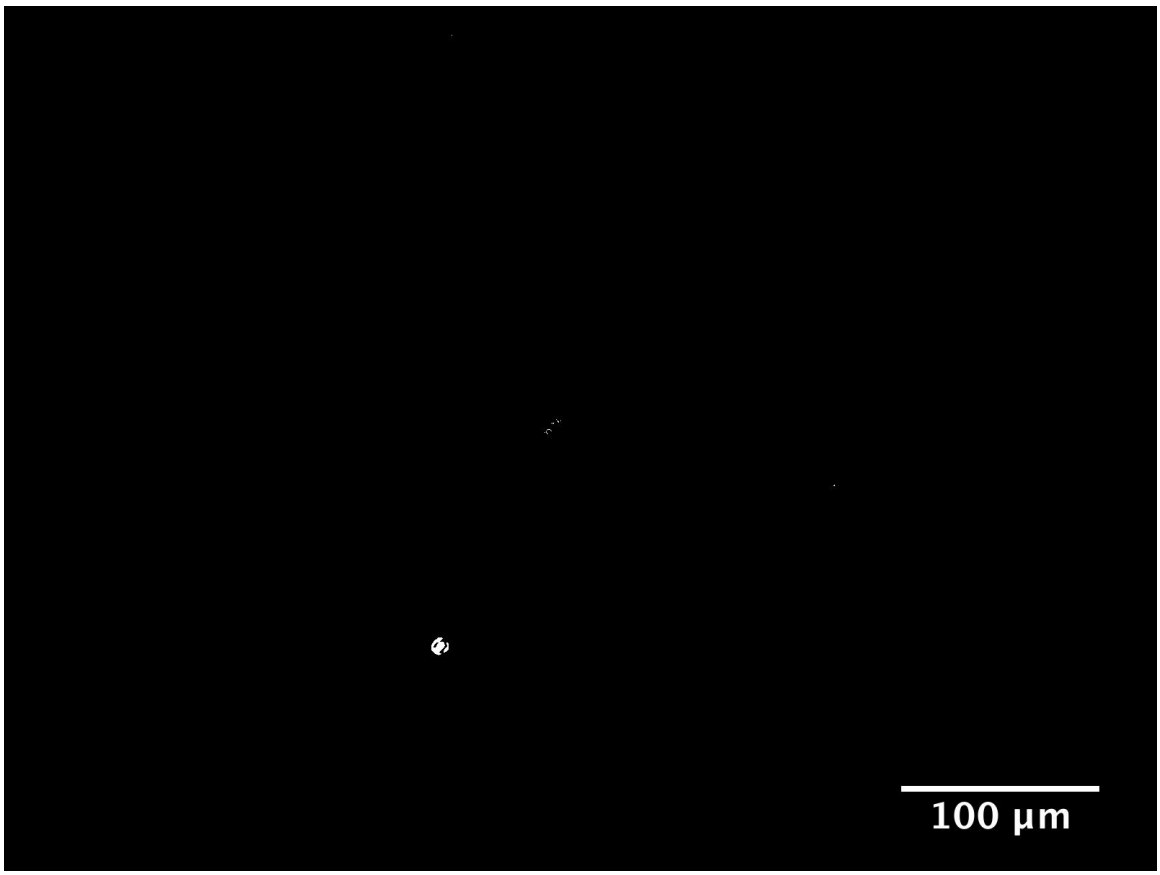

Figure A. 2: Total pinhole count is 12 and total pinhole area is about 50µm^2.

A.1.2. Standard cleaned substrates

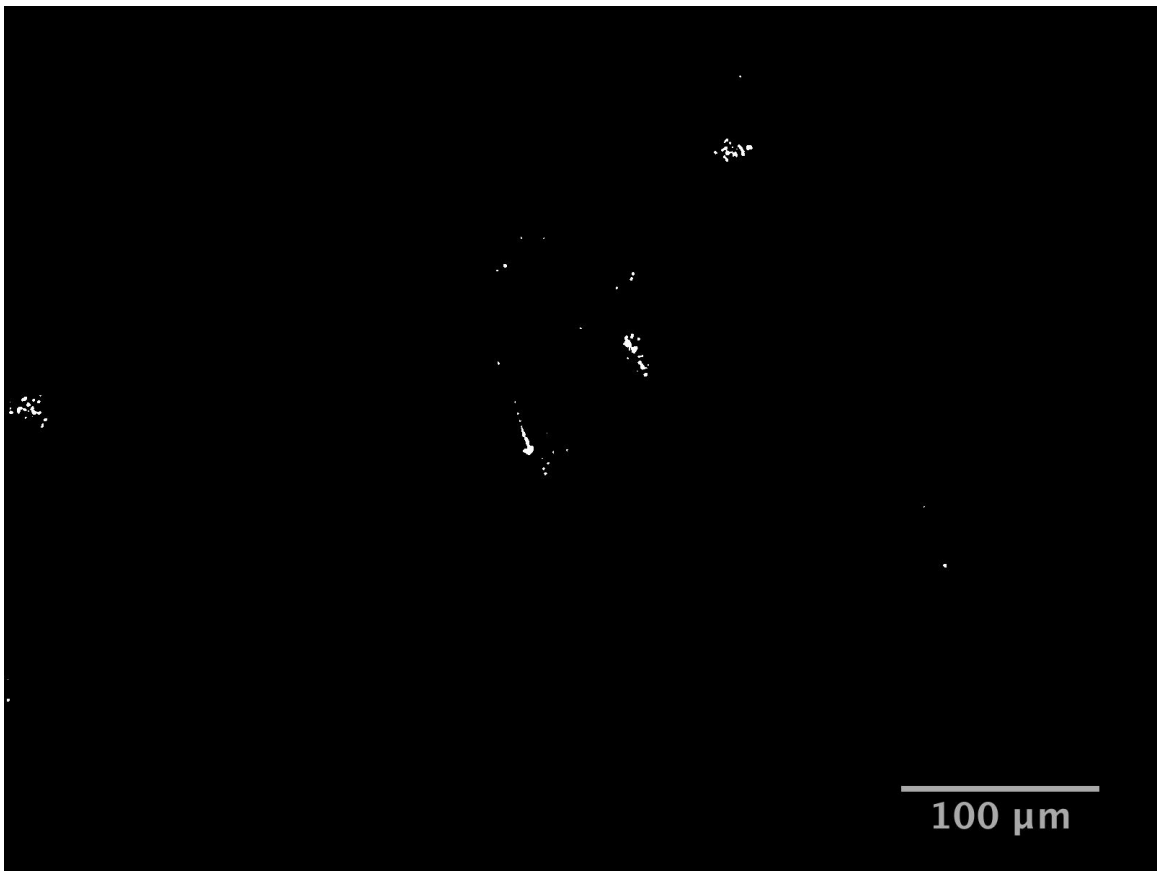

Figure A. 3: Total pinhole count is 58 and total pinhole area is about 197µm^2.

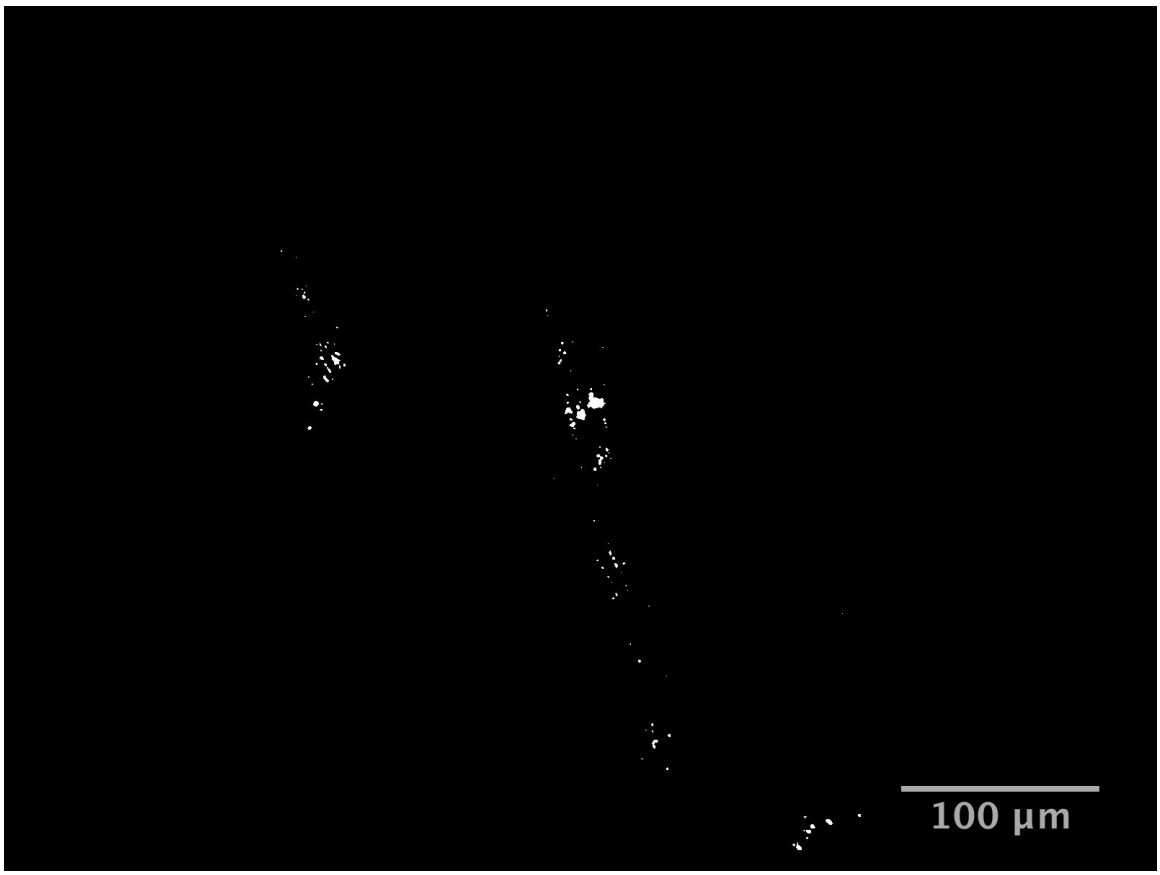

Figure A. 4: Total pinhole count is 155 and total pinhole area is about 231µm^2.

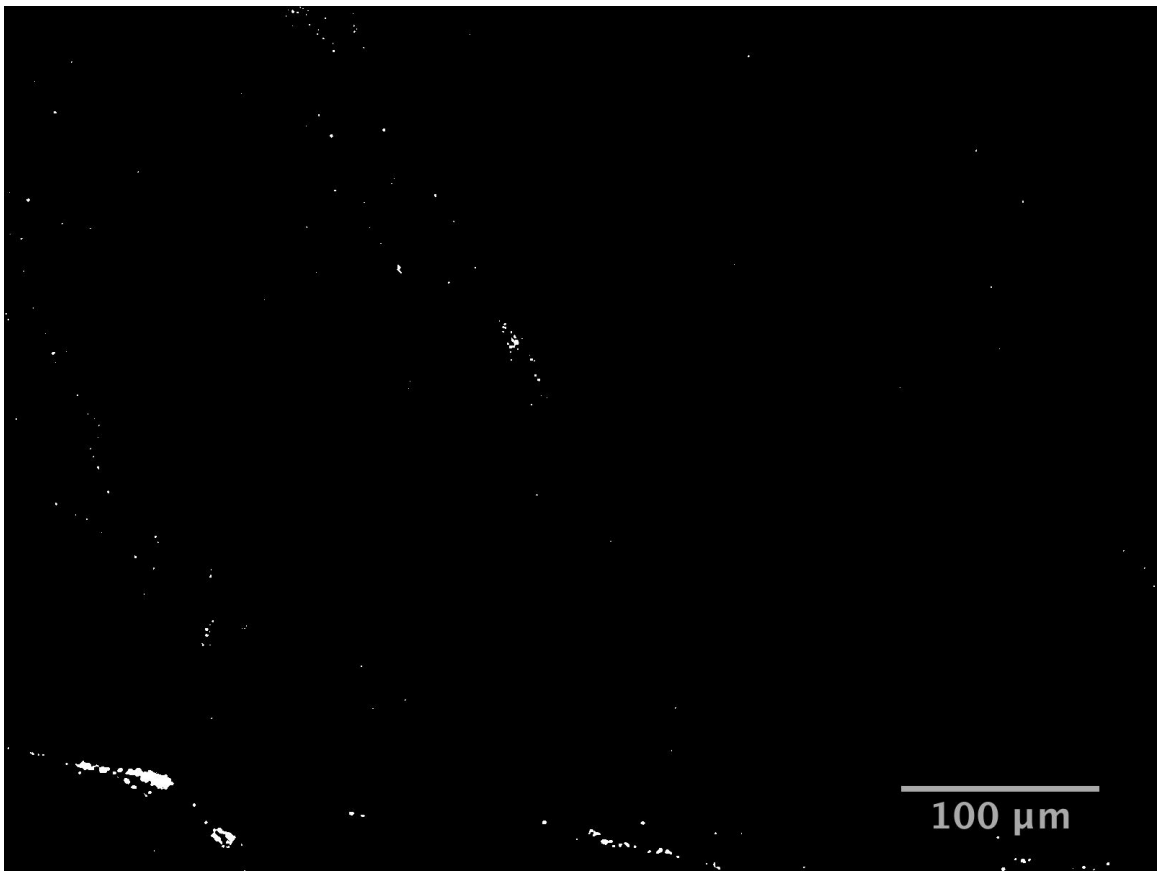

Figure A. 5: Total pinhole count is 183 and total pinhole area is about 428µm^2.

A.1.3. Substrates cleaned within the mini-environment

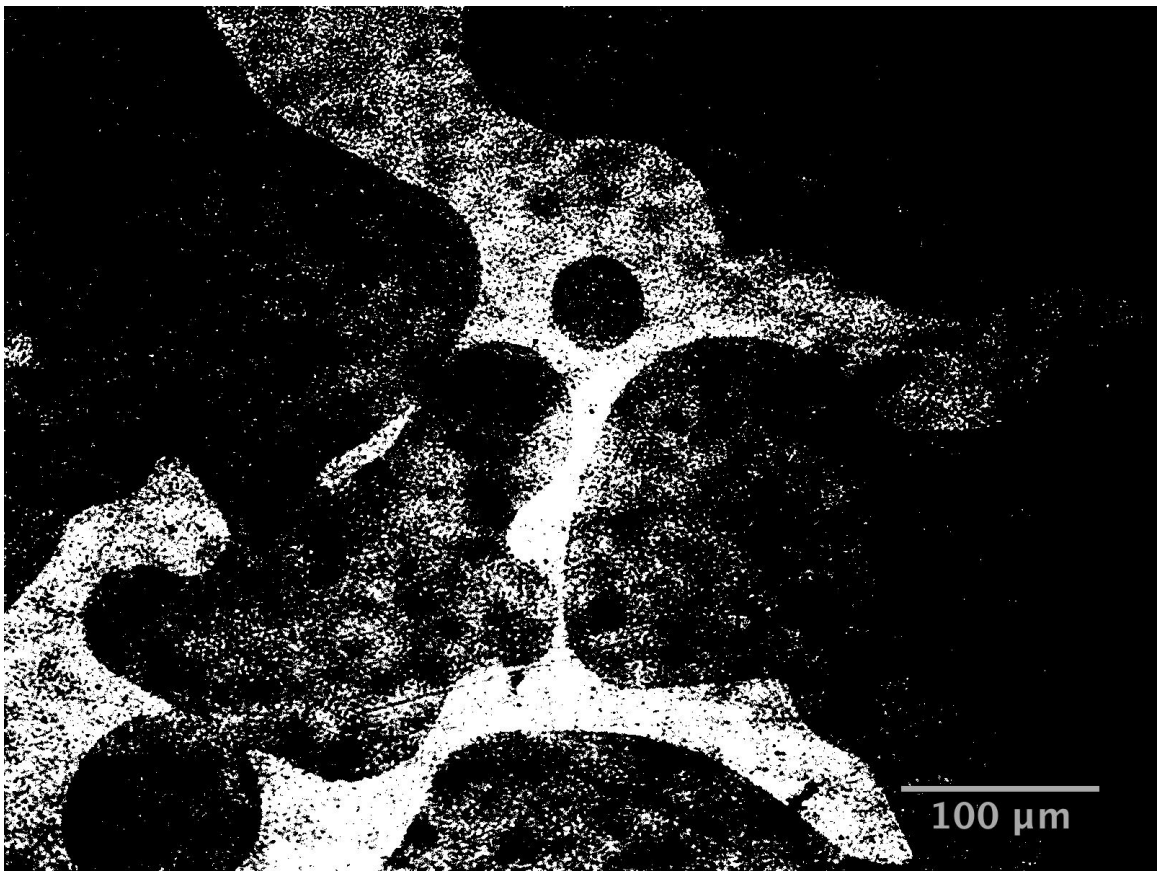

Figure A. 6: Total pinhole count is 7865 and total pinhole area is about 45.5e+3µm^2.

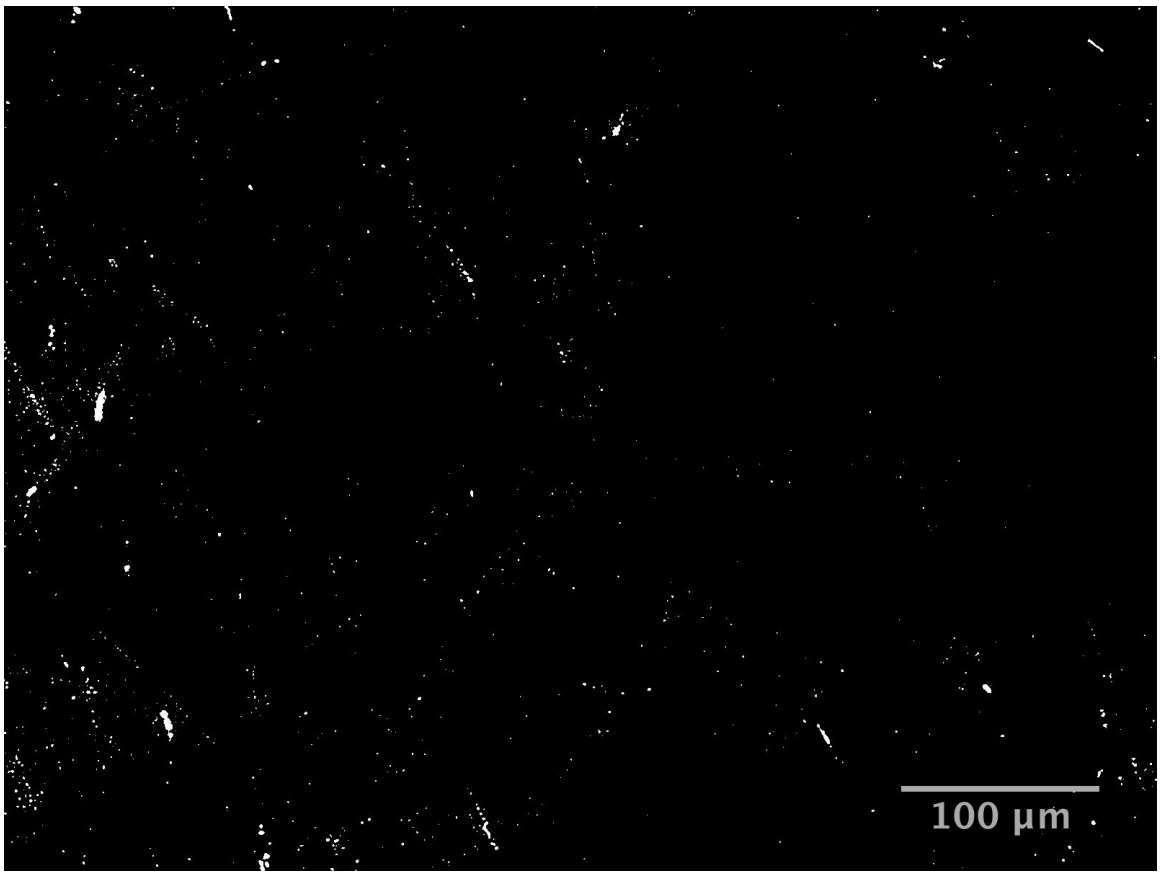

Figure A. 7: Total pinhole count is 1102 and total pinhole area is about 941µm^2.

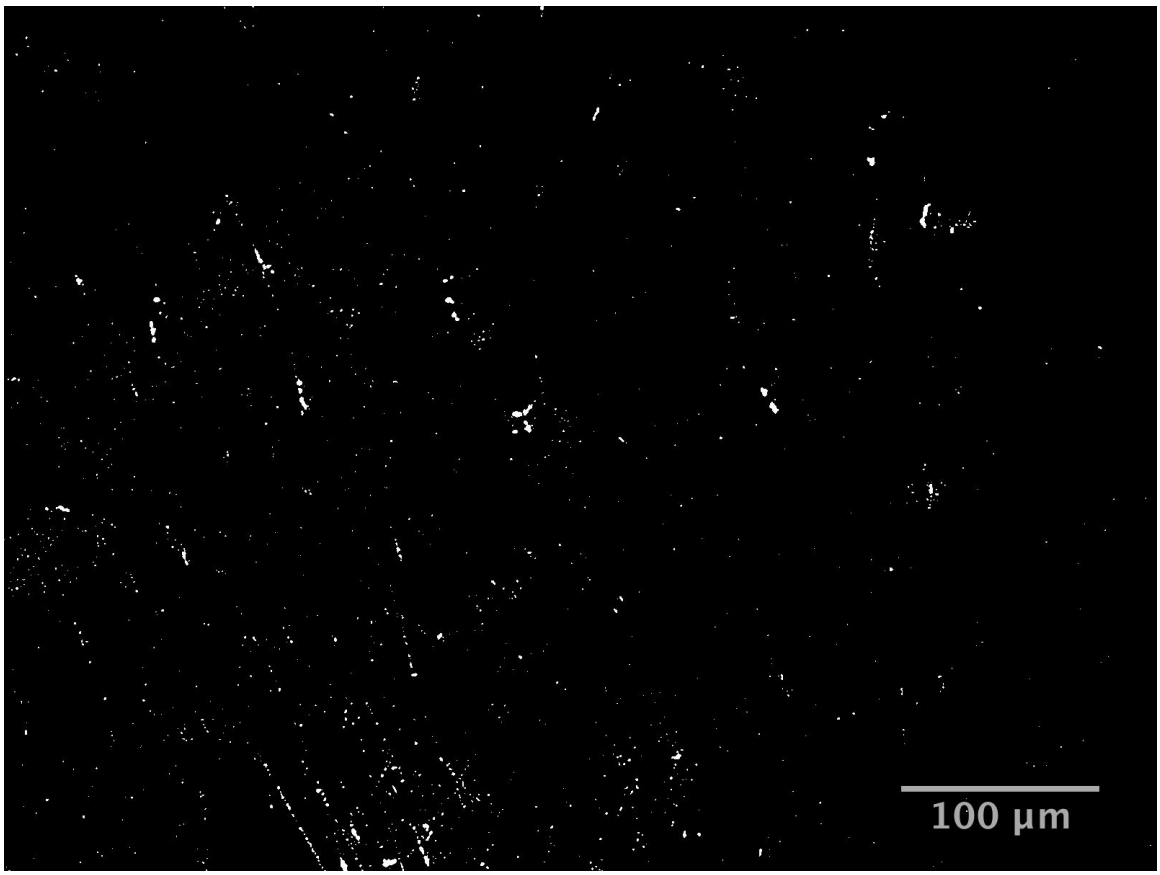

Figure A. 8: Total pinhole count is 1418 and total pinhole area is about 1130µm^2.

A.2. 100nm CdS films

A.2.1. Plasma cleaned substrates

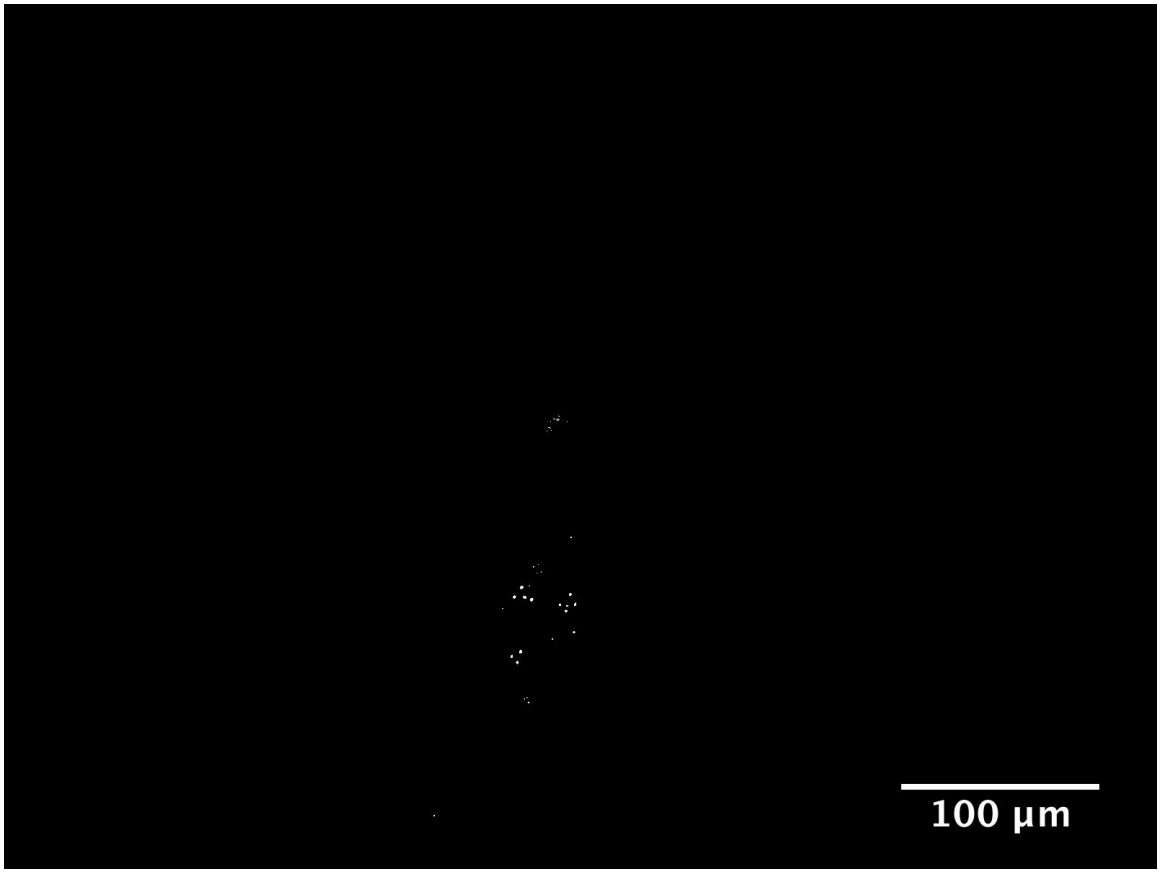

Figure A. 9: Total pinhole count is 33 and total pinhole area is about 30µm^2.

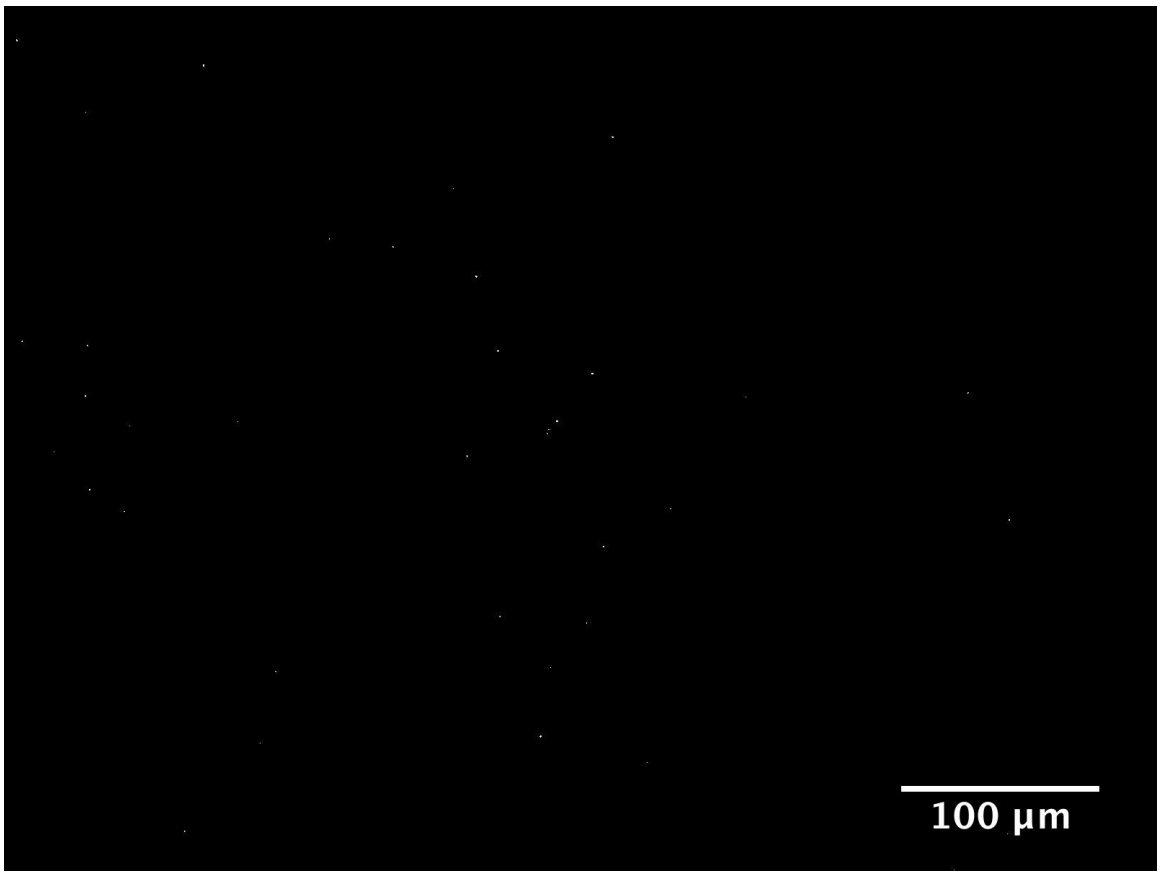

Figure A. 10: Total pinhole count is 38 and total pinhole area is about 14µm^2.

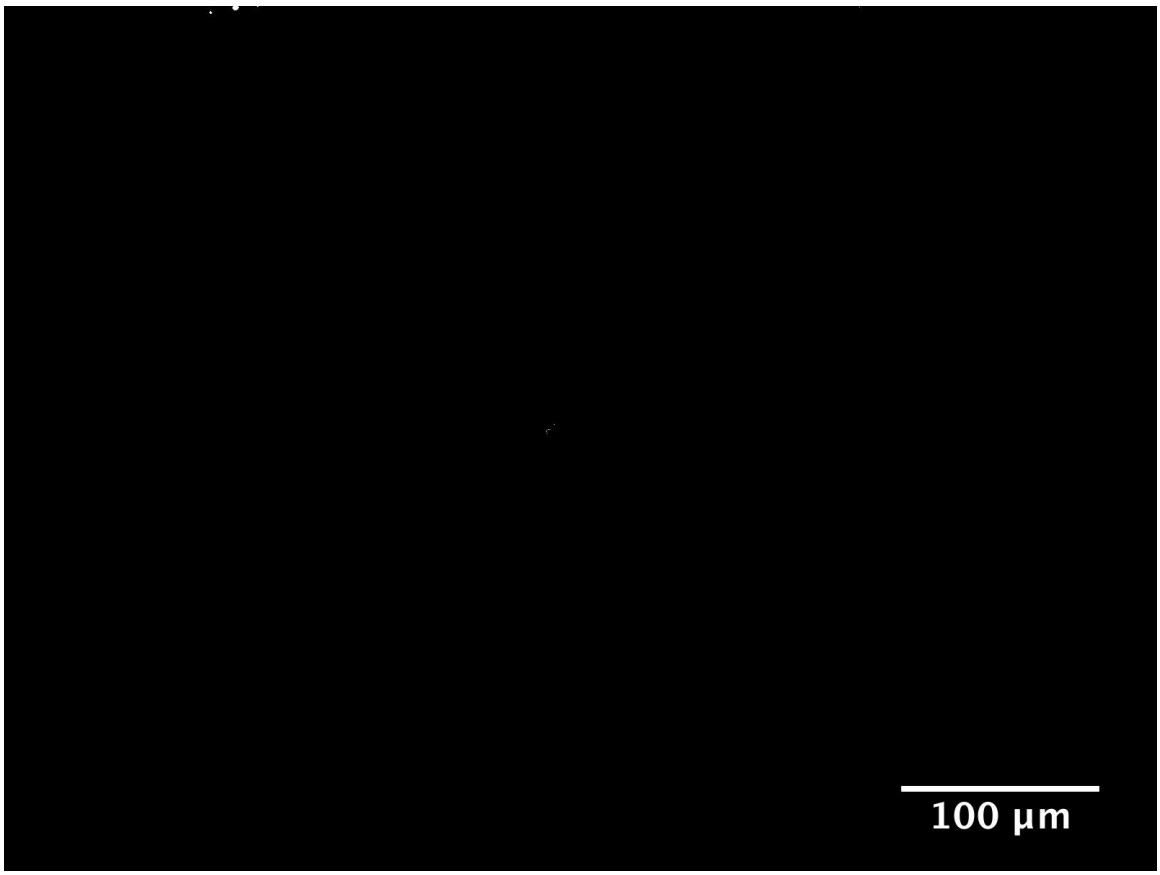

Figure A. 11: Total pinhole count is 10 and total pinhole area is about 8µm^2.

A.2.2. Standard cleaned substrates

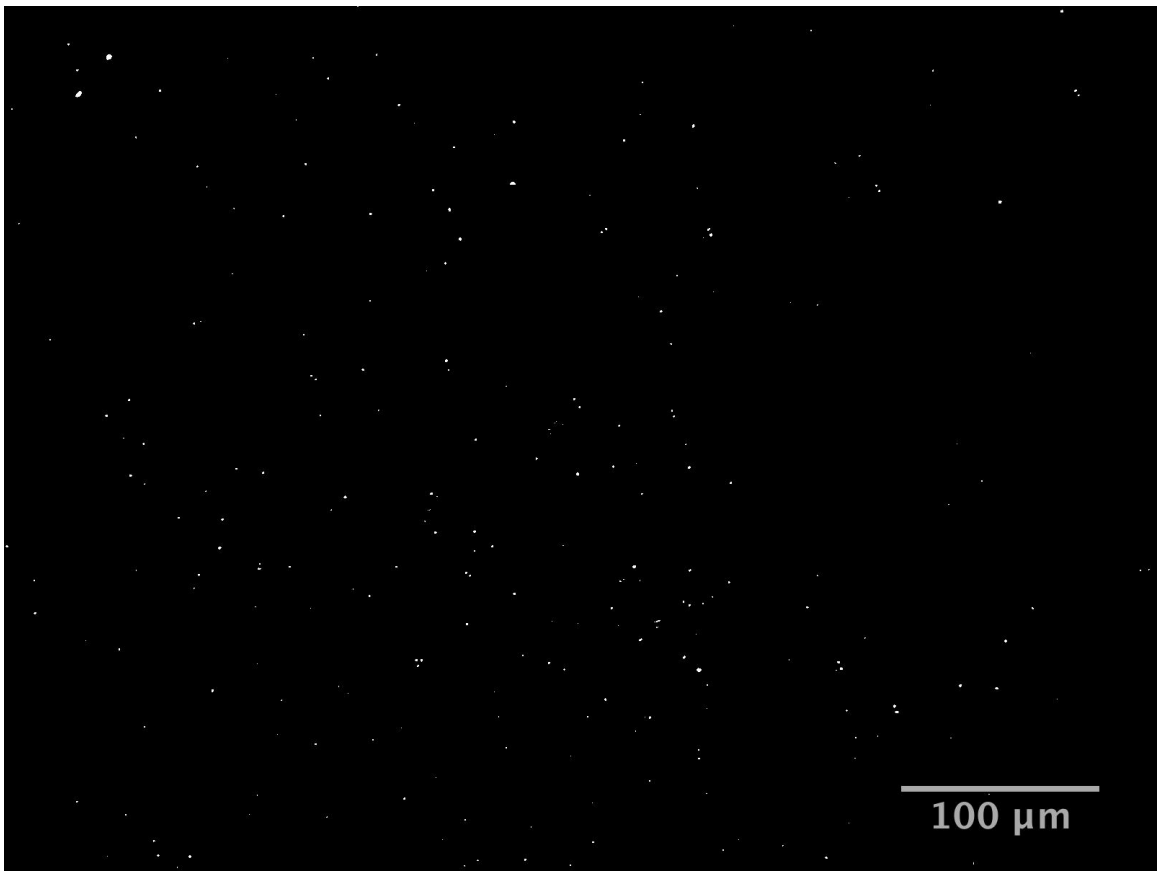

Figure A. 12: Total pinhole count is 245 and total pinhole area is about 193µm^2.

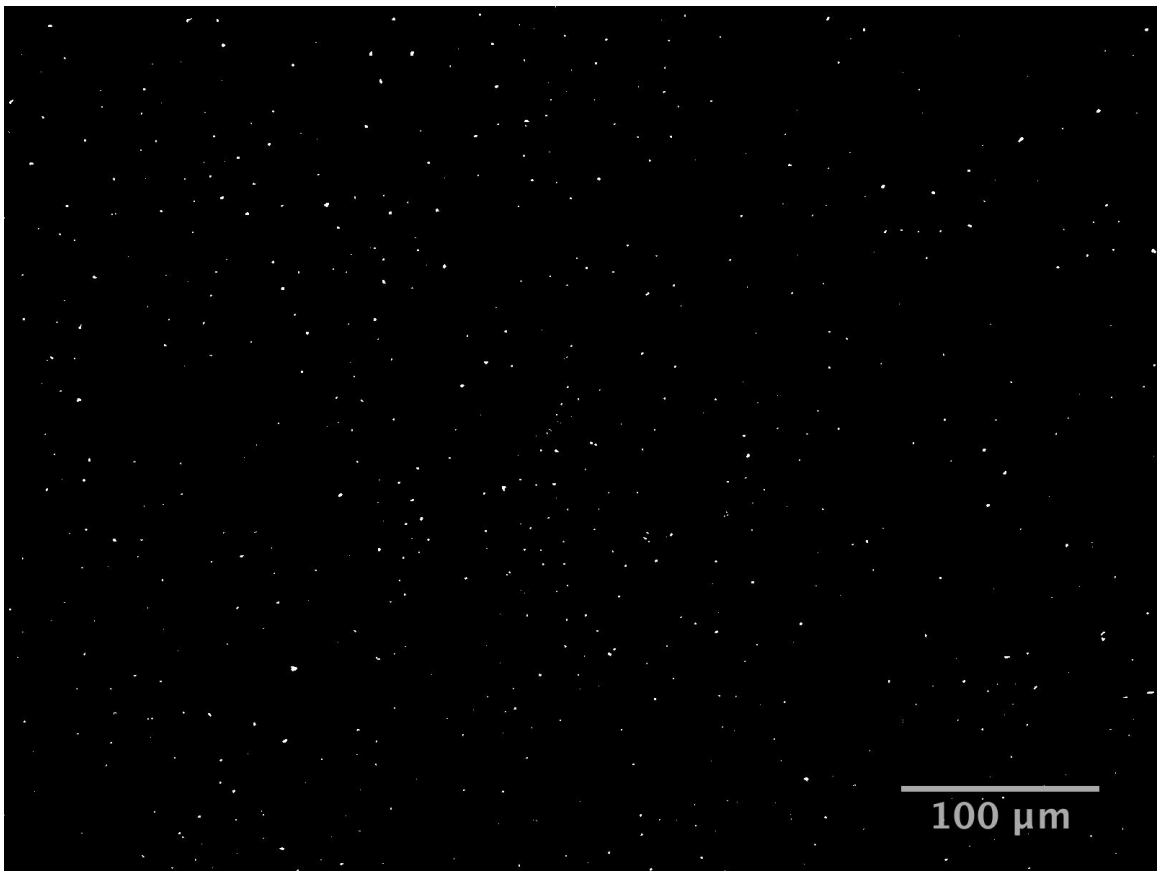

Figure A. 13: Total pinhole count is 629 and total pinhole area is about 486µm^2.

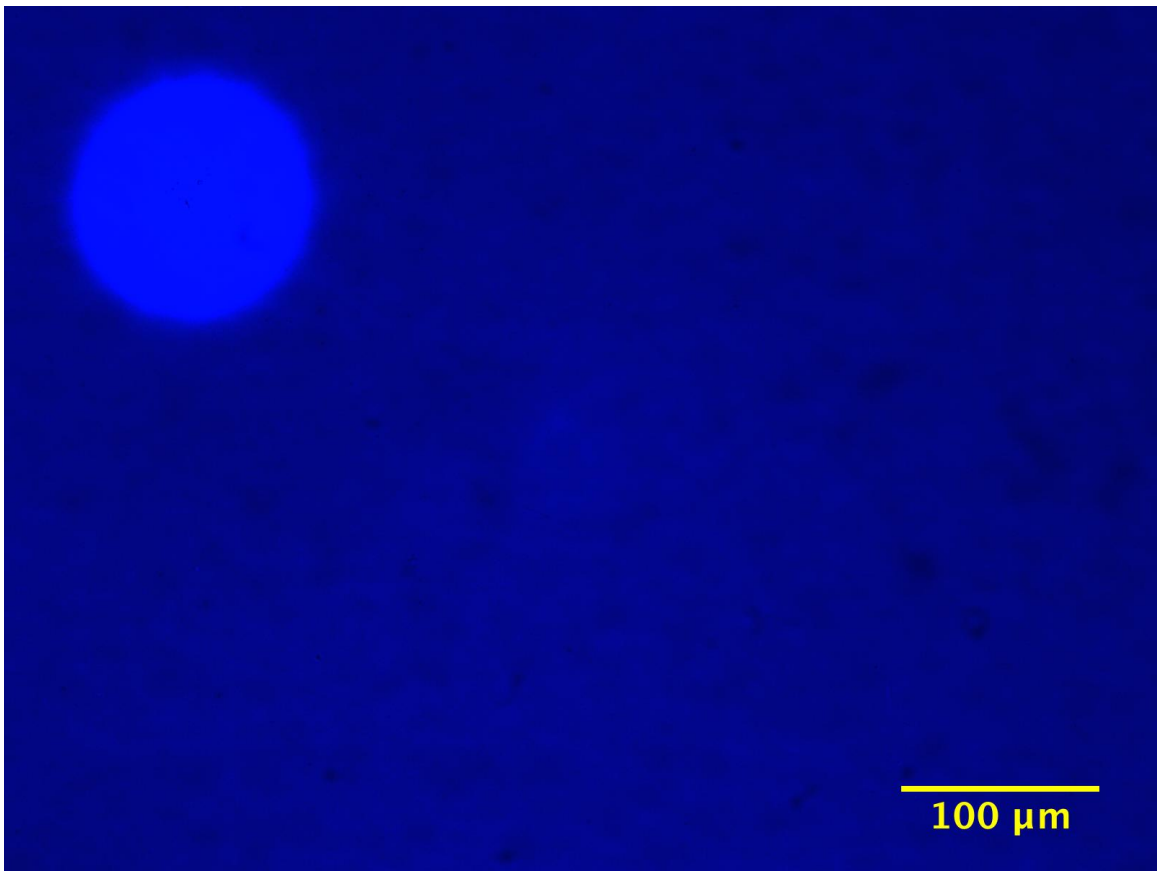

Figure A. 14: A big pinhole in the 100nm CdS film deposited on standard cleaned TEC10 glass substrate.

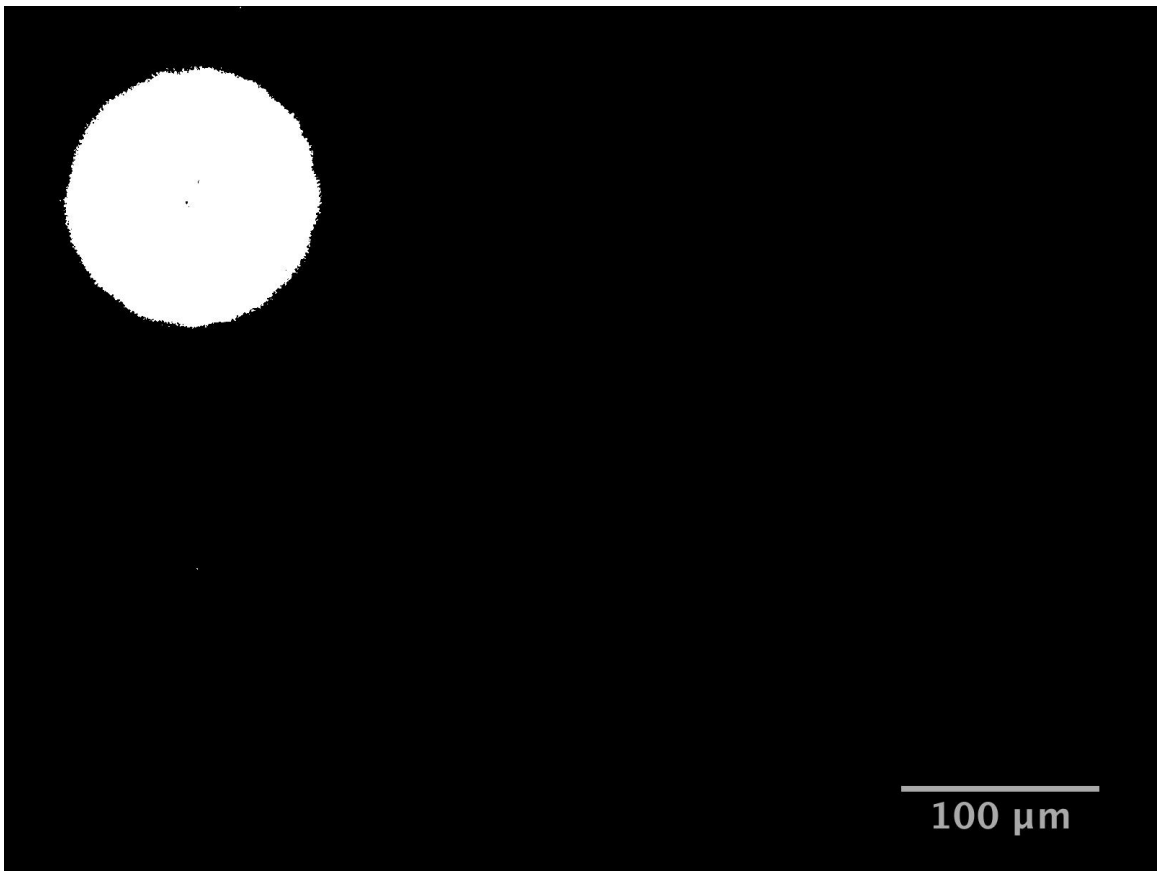

Figure A. 15: Total pinhole count is 25 and total pinhole area is about 13e+3 μm^2.

A.2.3. Substrates cleaned within the mini-environment

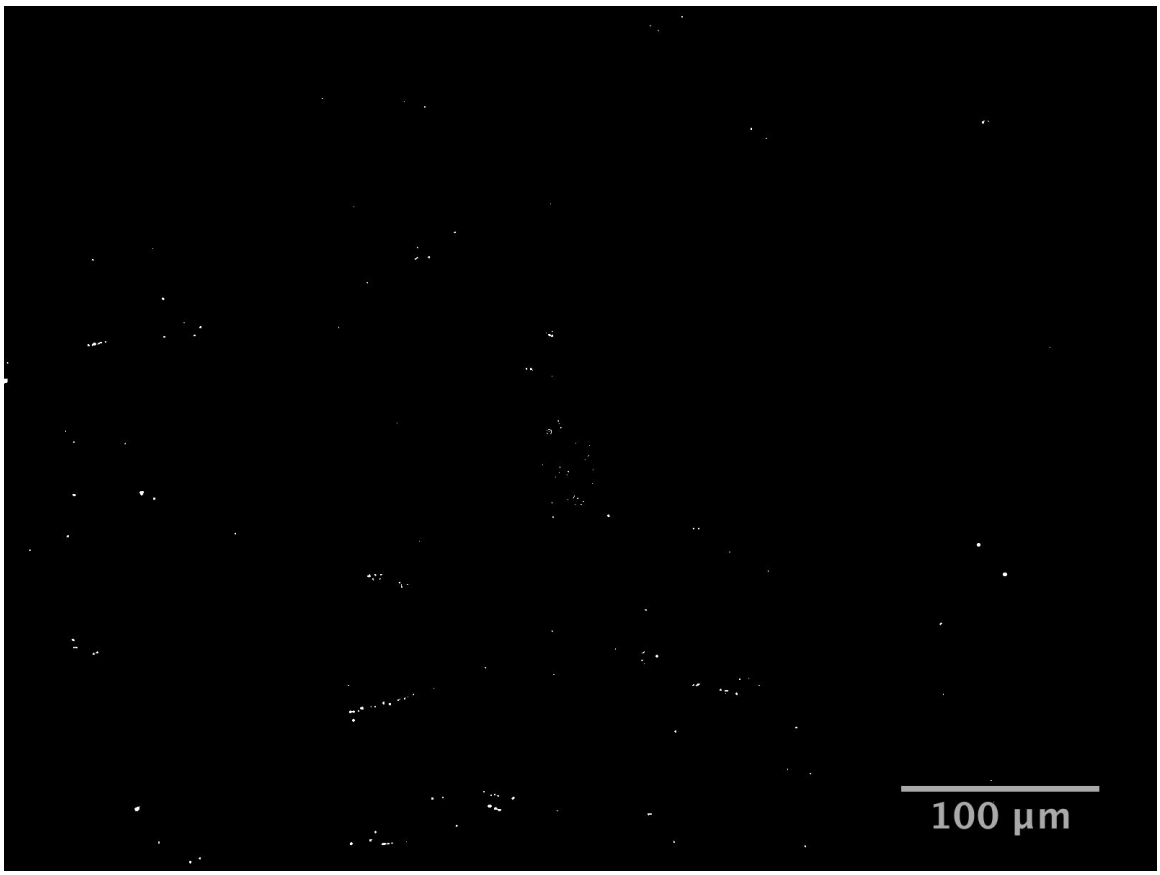

Figure A. 16: Total pinhole count is 238 and total pinhole area is about 163µm^2.

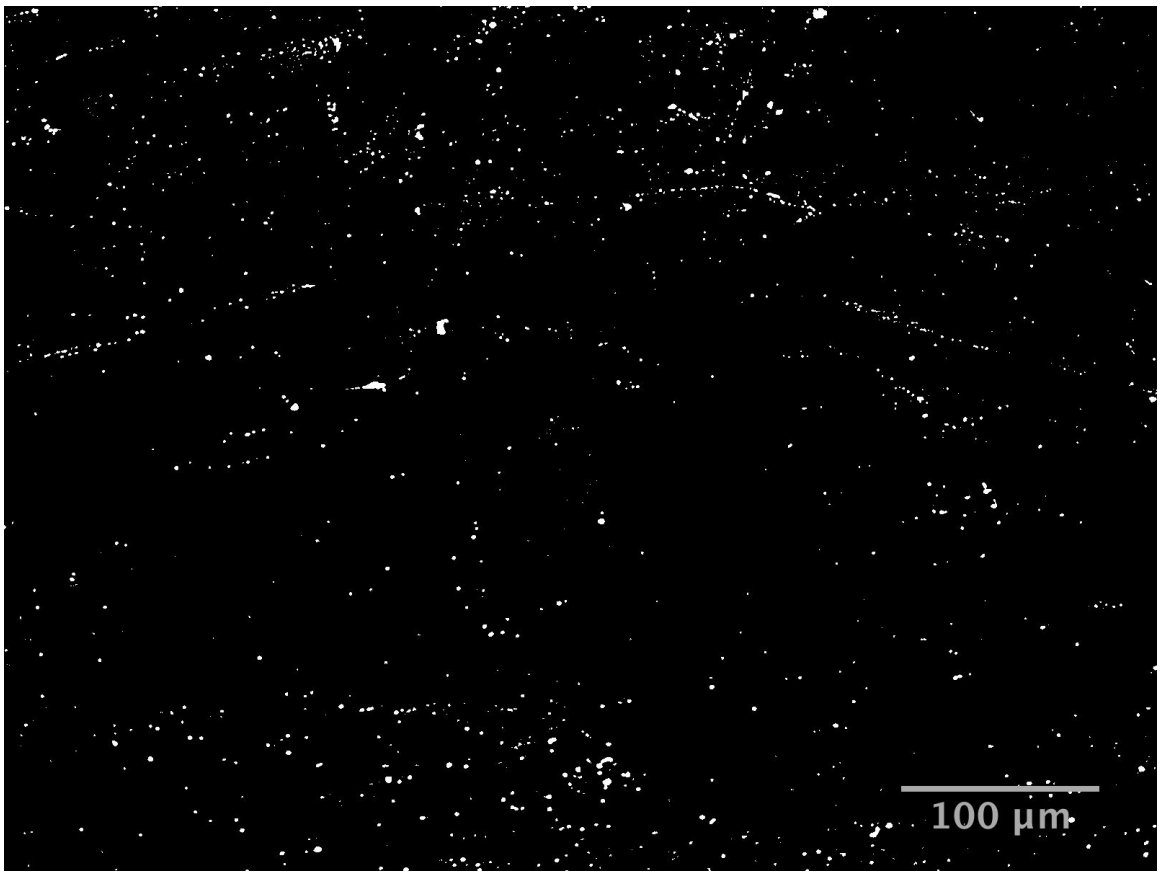

Figure A. 17: Total pinhole count is 1597 and total pinhole area is about 2400µm^2.

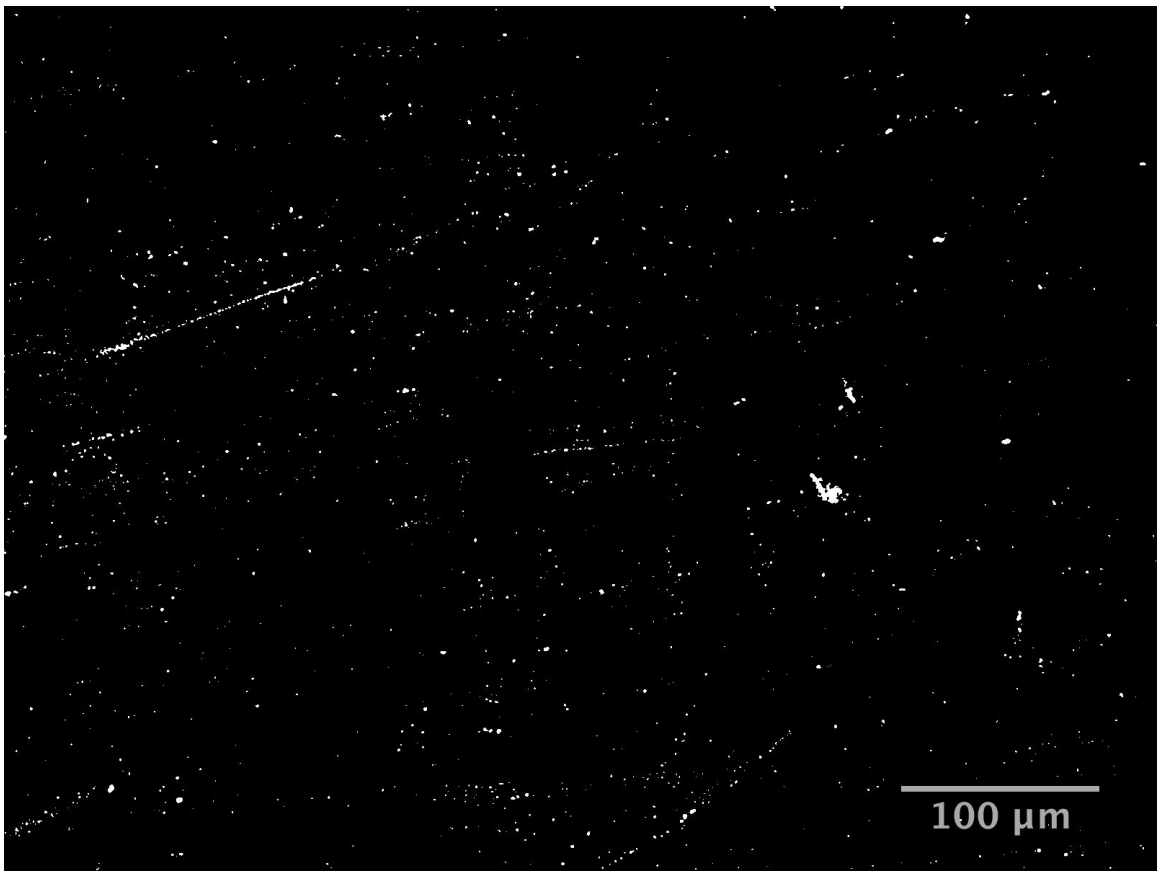

Figure A. 18: Total pinhole count is 1567 and total pinhole area is about 1370µm^2.

A.3. 50nm CdS films

A.3.1. Plasma cleaned substrates

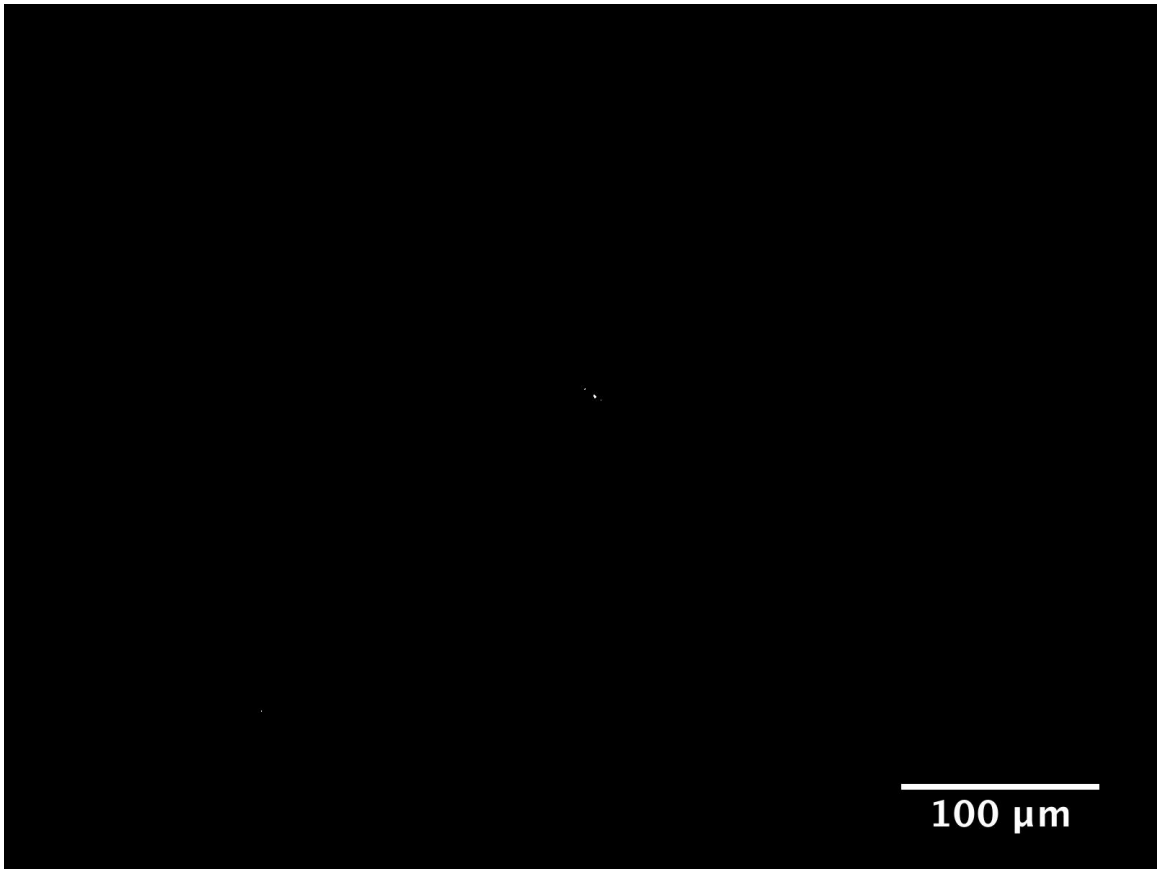

Figure A. 19: Total pinhole count is 4 and total pinhole area is about 3µm^2.

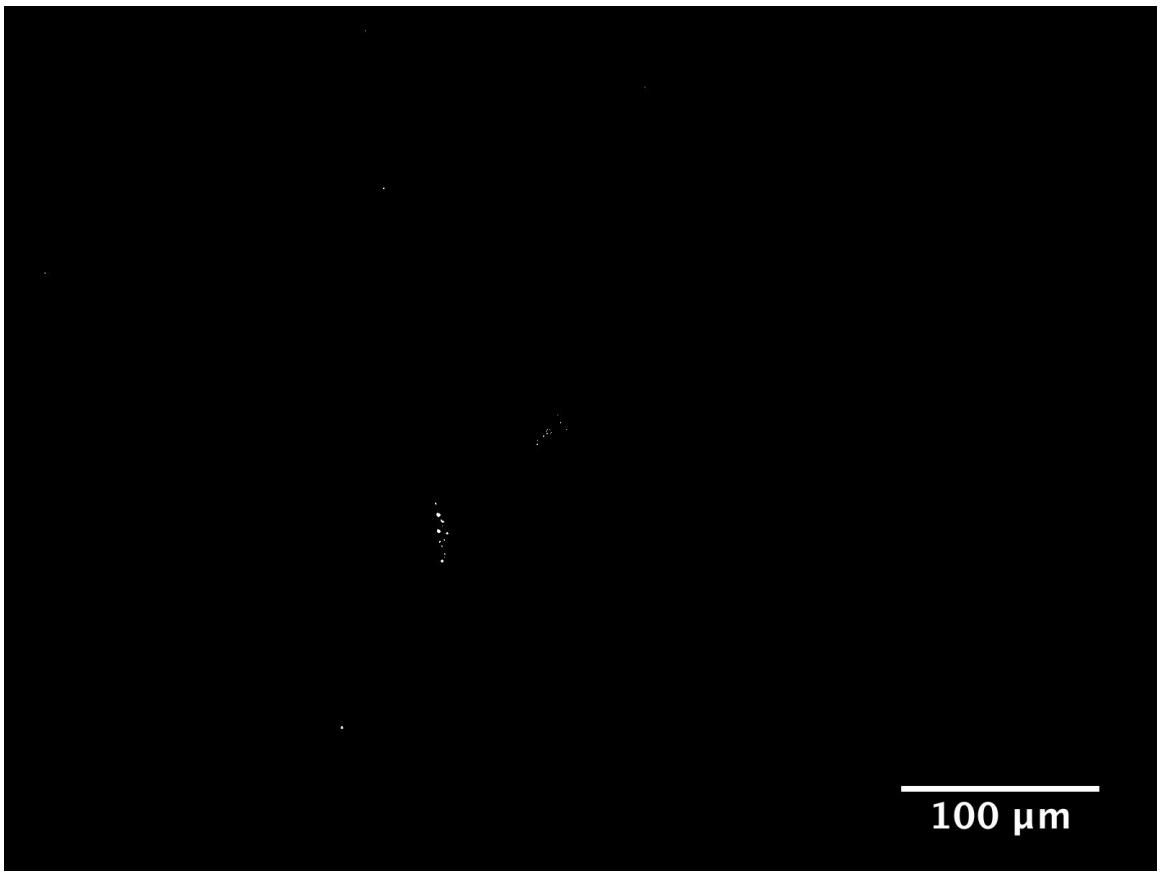

Figure A. 20: Total pinhole count is 29 and total pinhole area is about 18µm^2.

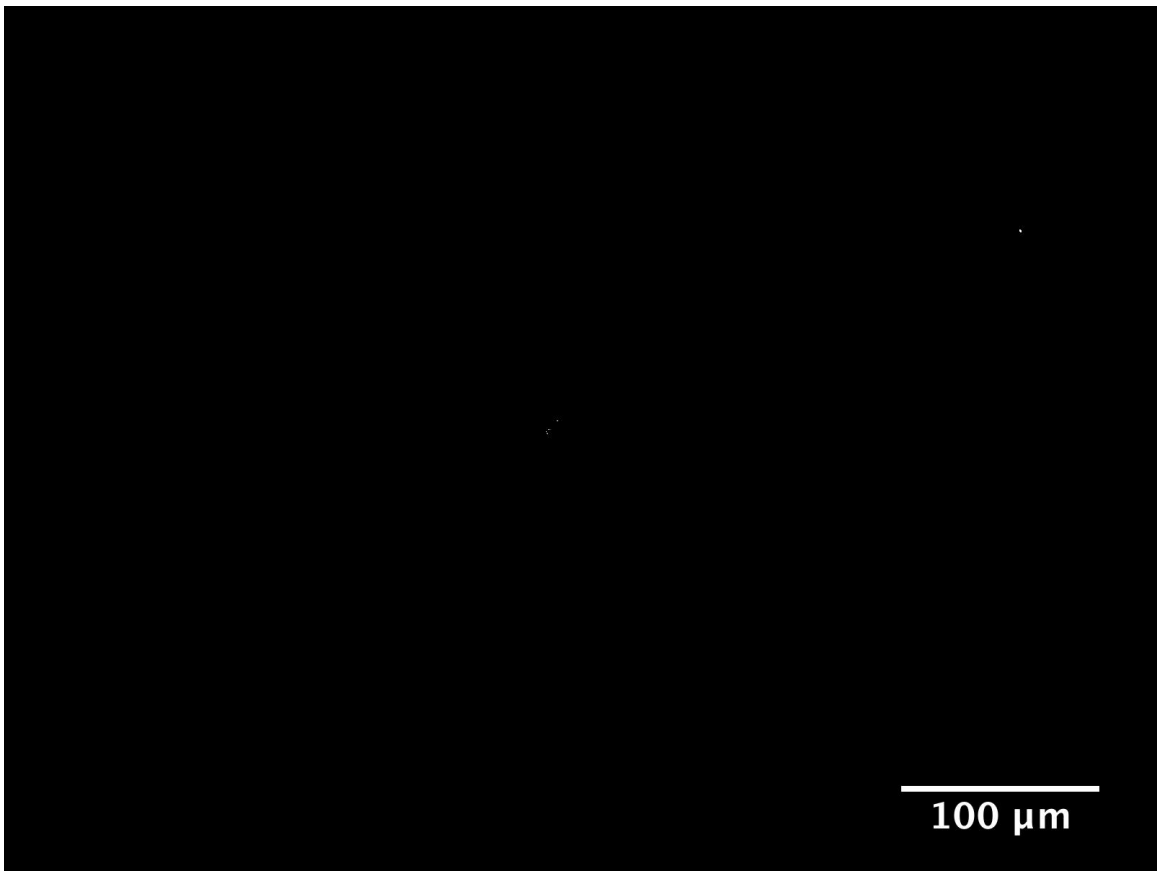

Figure A. 21: Total pinhole count is 6 and total pinhole area is about 2µm^2.

A.3.2. Standard cleaned substrates

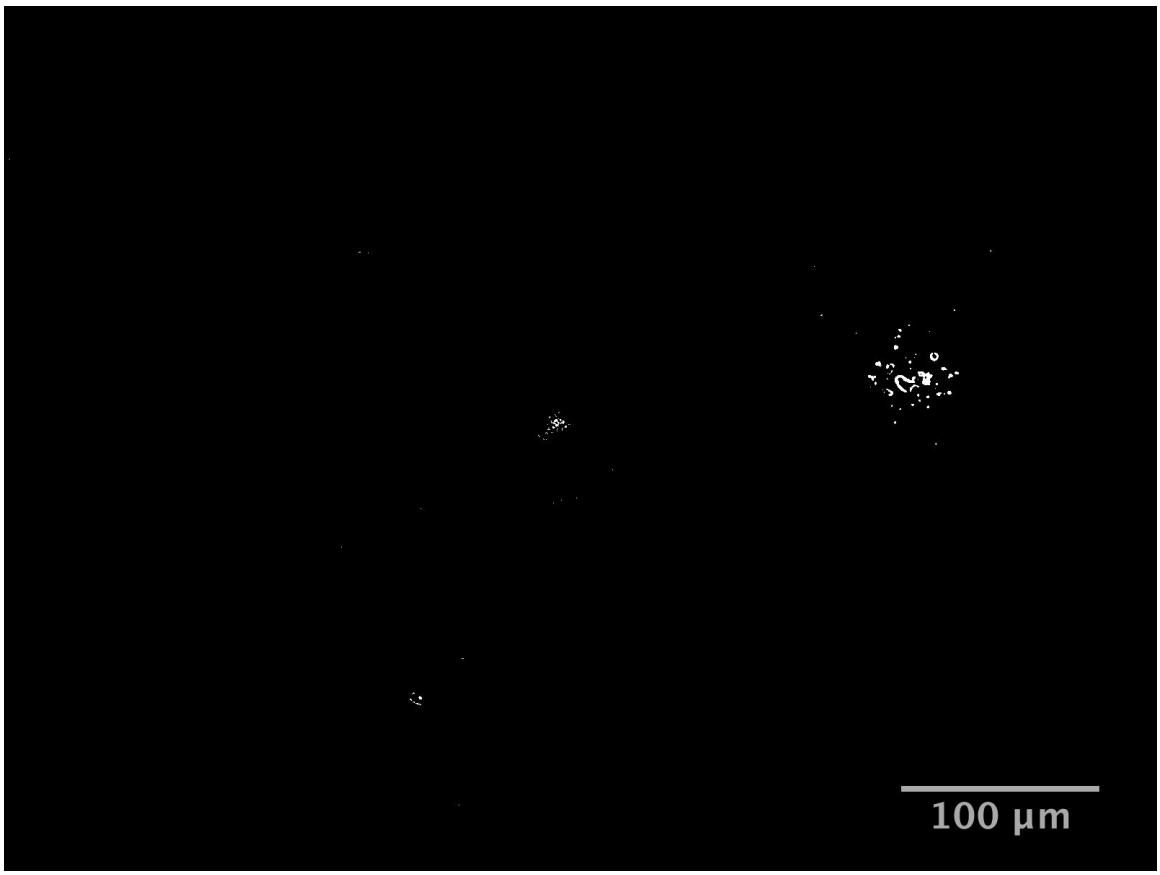

Figure A. 22: Total pinhole count is 90 and total pinhole area is about 179µm^2.

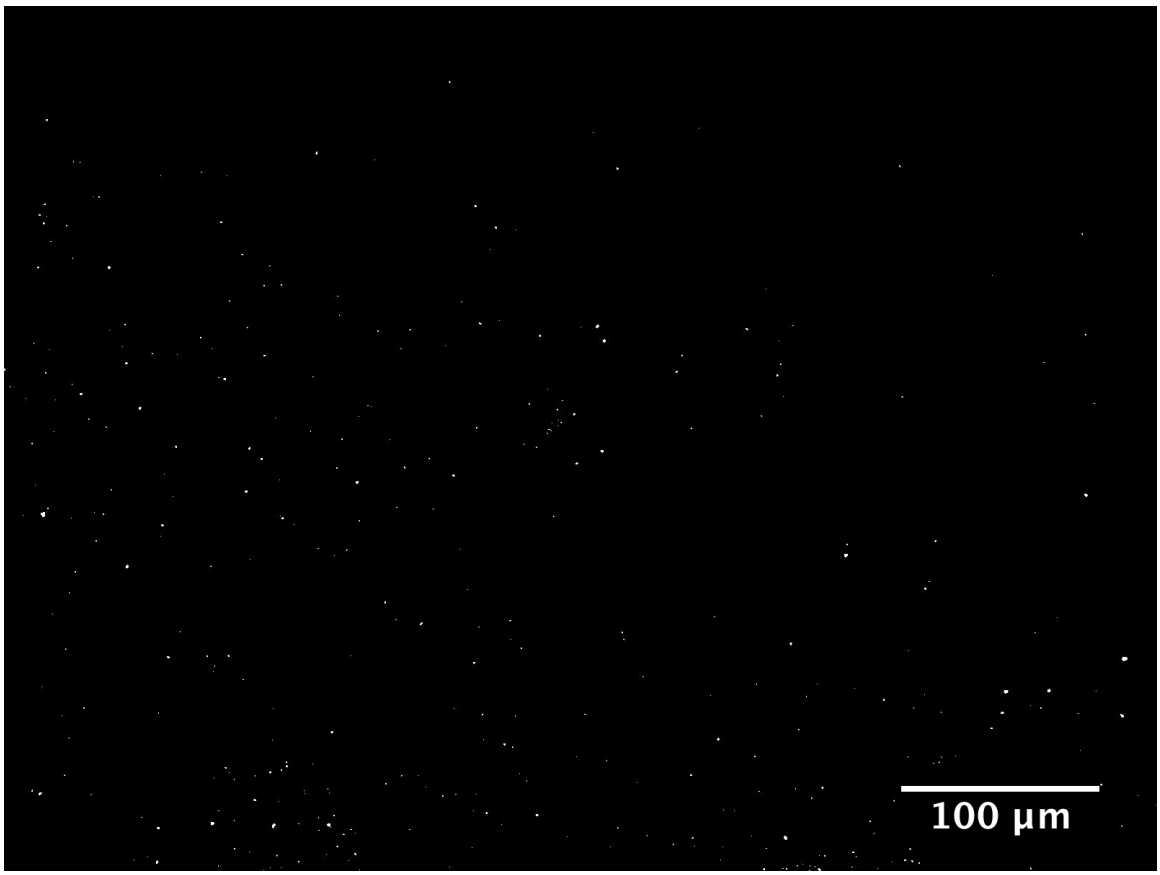

Figure A. 23: Total pinhole count is 345 and total pinhole area is about 188µm^2.

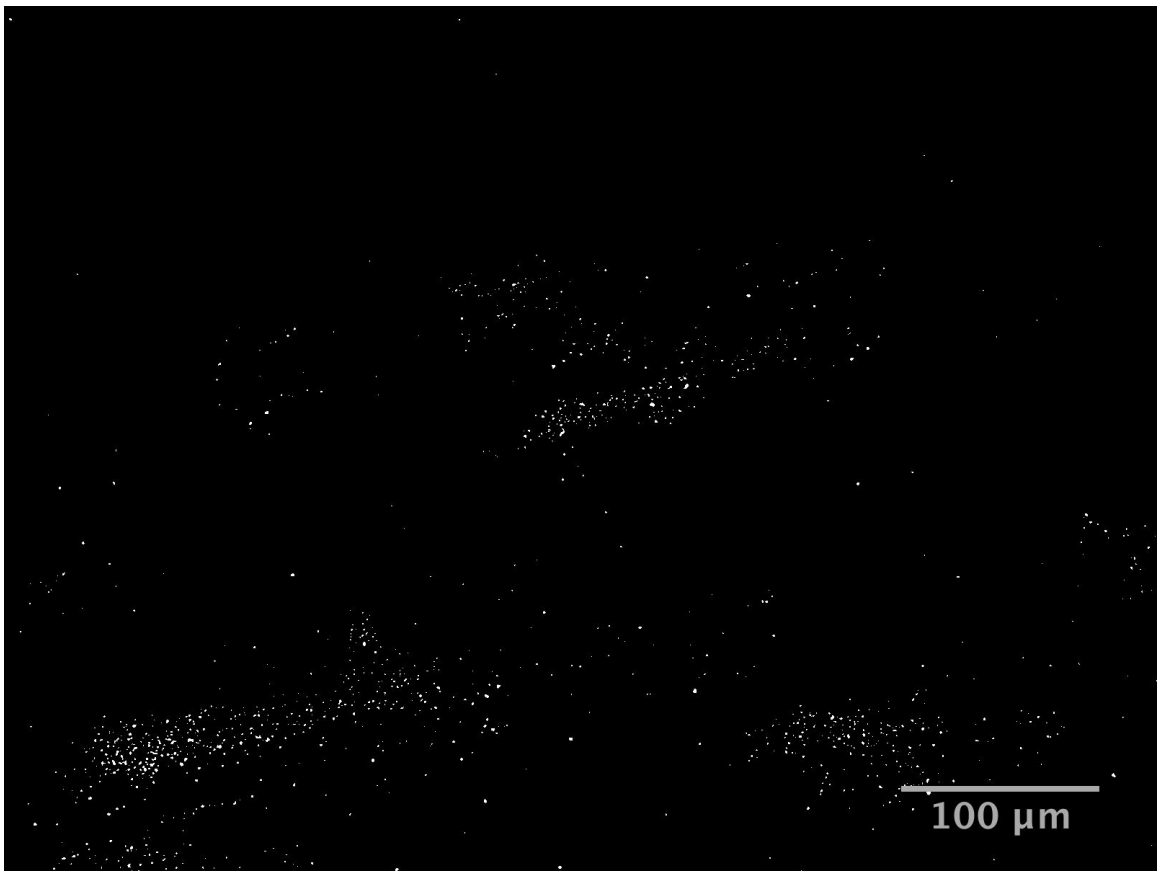

Figure A. 24: Total pinhole count is 1225 and total pinhole area is about 730µm^2.

A.3.3. Substrates cleaned within the mini-environment

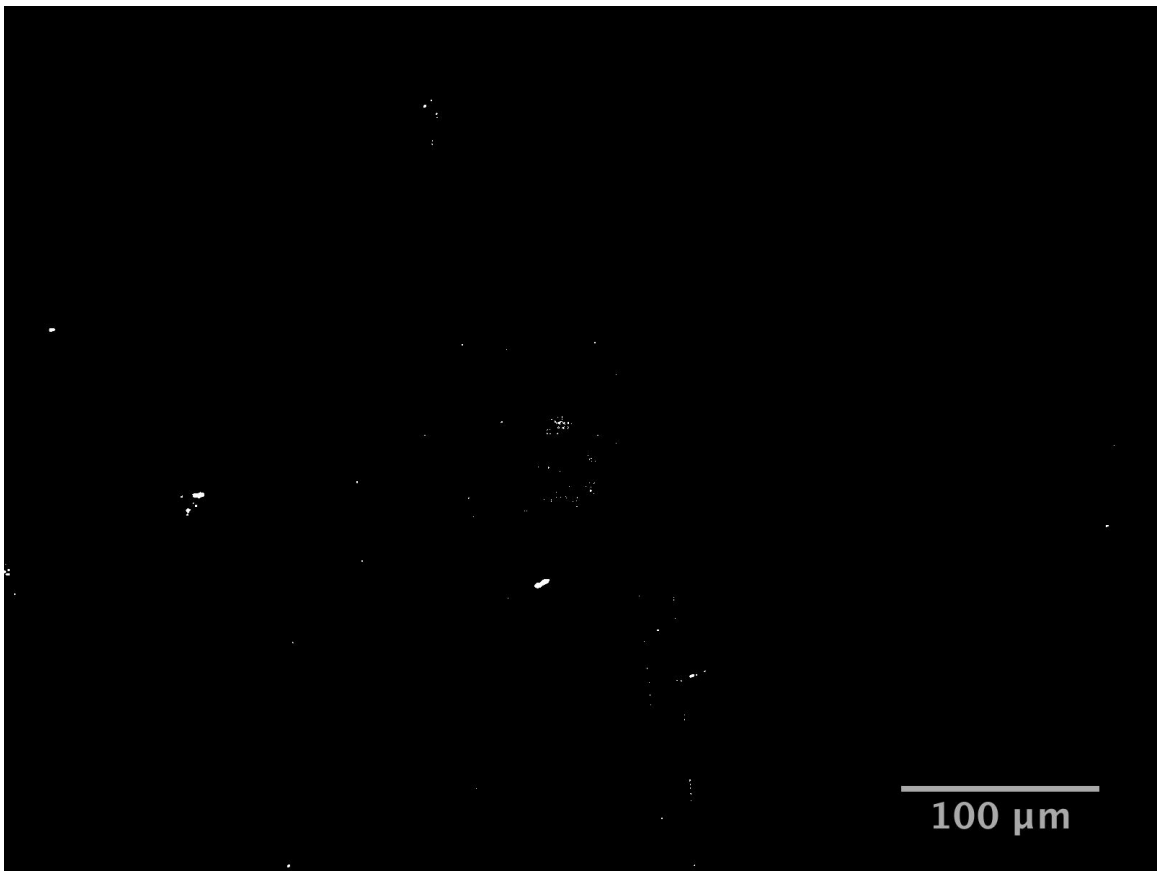

Figure A. 25: Total pinhole count is 104 and total pinhole area is about 80µm^2.

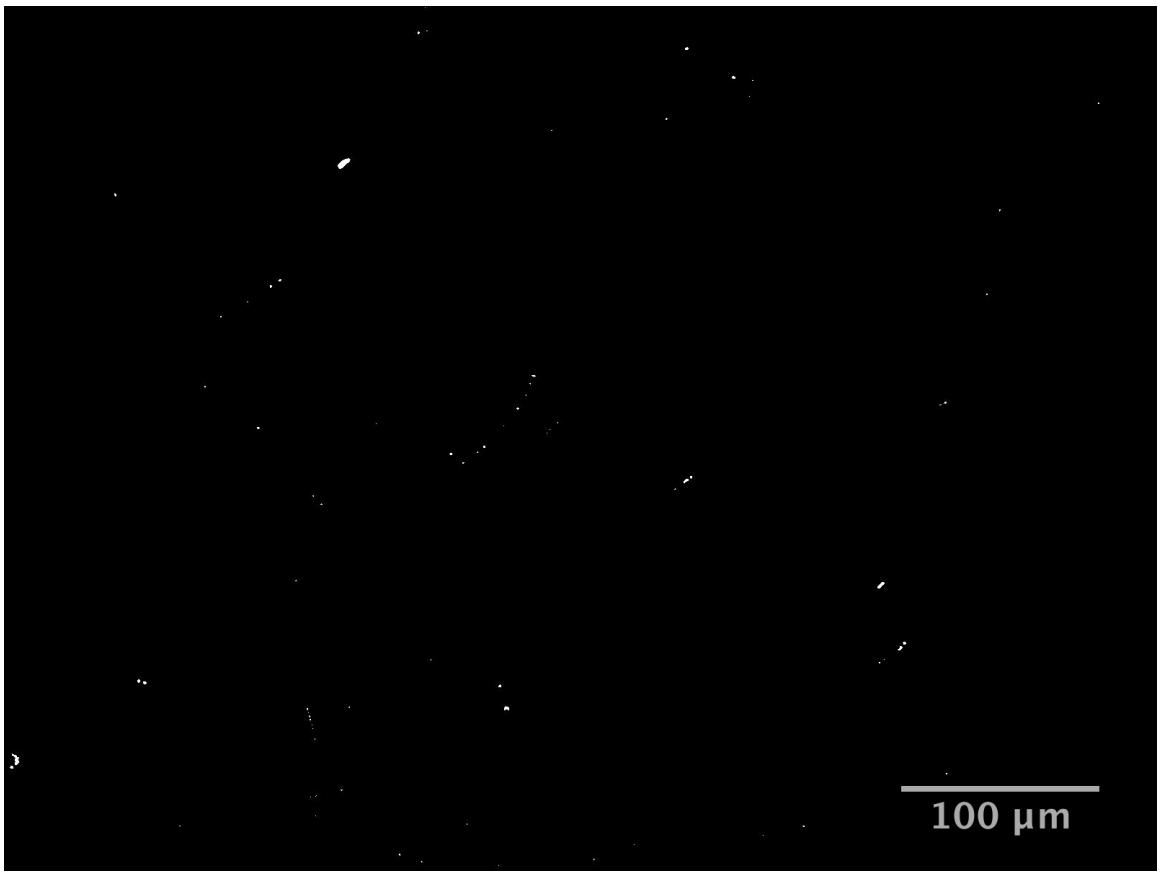

Figure A. 26: Total pinhole count is 75 and total pinhole area is about 90µm^2.

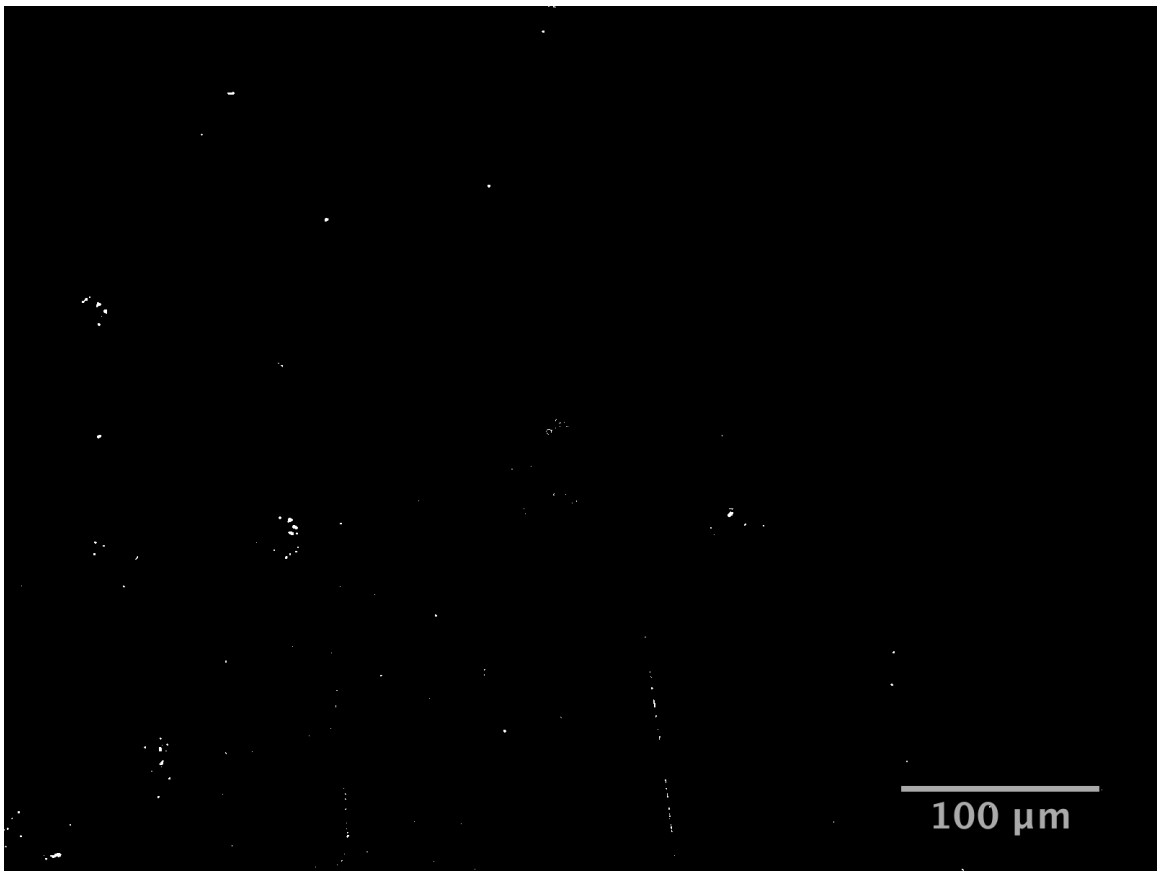

Figure A. 27: Total pinhole count is 146 and total pinhole area is about 127µm^2.

Appendix B: Statistics

The statistical terms used in this study are listed and explained in this appendix. In addition, an explanation of a boxplot and its various components is provided.

Box plots:

Definition: It is a "plot concerned with the symmetry of the distribution of the data and incorporates numerical measures of central tendency and location to study the variability of the data and concentration of data in the tails of the distribution" [37].

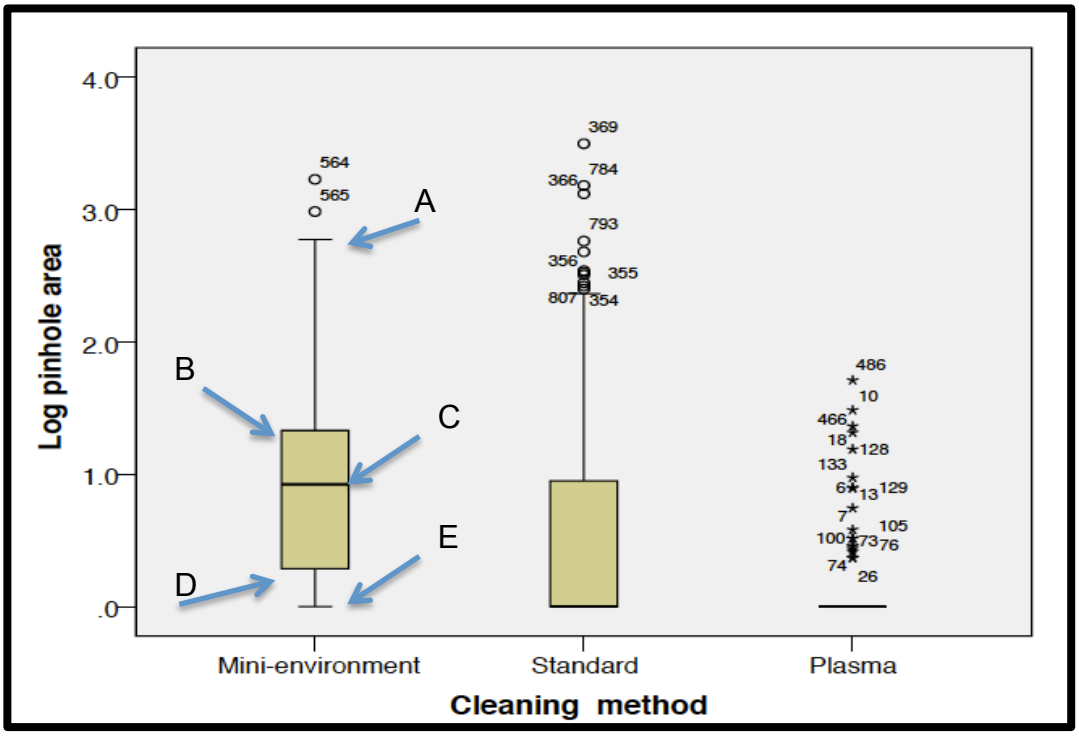

Figure B. 1: An example of a boxplot as shown earlier in chapter 4 showing the different components of boxplots.

An example of a boxplot is shown in figure A.1. A boxplot usually present 50% of the data (inside the yellow rectangle) with 25% on each side of the median of the data. These 25% ranges on each side are known as the 25th percentile and the 75th percentile (top and lower edges of the rectangular part of the boxplot respectively). The location of

the median line indicates the concentration of data in relation to the median of the data. For example, the median line in the boxplot of the mini-environment group in figure A.1 shows that the observations (among the data) with high pinhole area are much more than observations with smaller pinhole area or no pinhole area. In addition, the whiskers of the boxplot give an indication of the skewness of the data. For example, the boxplot of the mini-environment cleaning method indicate there is more skewness in the data in the upper direction. Finally, data observations shown as circles are mild outliers and data observations shown as stars are extreme outliers. These outliers represent data observations that are outside the expected range of the data. The boxplot of the mini-environment data shows the following components:

- A: Largest value of the data within 1.5 of the interquartile range (IQR) of Q3. IQR represents the distance between the 25^{th} percentile and 75^{th} percentile of the data. The IQR is about 1.0 in the transformed scale of the pinhole area for the boxplot representing the mini-environment data.
- B: Q3, the 25^{th} percentile and also known as the upper adjacent value; it is about 1.3 in the transformed scale of the pinhole area for the boxplot representing the mini-environment data.
- C: Median of the data, it is about 0.9 in the transformed scale of the pinhole area for the boxplot representing the mini-environment data.
- D: Q1, the 75^{th} percentile also known as the lower adjacent value, it is about 0.3 in the transformed scale of the pinhole area for the boxplot representing the mini-environment data.

- E: The smallest value of the data within 1.5 IQR of Q1, it is about 0.0 in the transformed scale of the pinhole area for the boxplot representing the mini-environment data.

Alpha:

Alpha is the confidence coefficient of the hypothesis being tested. In this study, alpha was set equal to 0.05 indicating that there was a 95% confidence in the test results obtained. This would be useful to determine the significance of any variable being considered (film thickness and cleaning method) and also to provide confidence intervals of the means of interest. A confidence interval indicates that there is a 95% chance that mean of the independent variable being considered (pinhole area) in the entire CdS film would be within that confidence interval. Confidence intervals were not provided in this study since the scale of the data was transformed and back transformation was not meaningful.

p-Value:

p-value is defined as “the probability of obtaining a vale of the test statistic that is likely or more likely to reject the null hypothesis as the actual observed value of the test statistic” [37]. It indicates the level of significance in the test statistic obtained in relation to the confidence coefficient (α) being considered. Therefore, any variable that has a p-value less than 0.05 is a statistically significant variable among the data.

F statistic:

The F statistic is a test statistic value that is used to determine the p-values in the analysis of the variance ANOVA for each specific variable being considered (film thickness and cleaning method). The higher the value of F indicates the higher

statistical significance that specific variable has. ANOVA outputs what is referred to as the ANOVA table that shows all variables being considered, their test statistics, and p-values. Each hypothesis tested in this study considered the effects of film thickness and cleaning method on the pinhole area in the transformed scale. ANOVA gives a value of the test statistic F for the film thickness, cleaning method and the combined effect of these two variables as well as their corresponding p-values.