

THESIS

DESIGN AND IMPLEMENTATION OF A COMPACT HIGHLY EFFICIENT 472KHZ  
RADIO FREQUENCY GENERATOR FOR ELECTROSURGERY

Submitted by

Gerald M. Eberhardt

Department of Electrical and Computer Engineering

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Master's Committee:

Advisor: George J. Collins

Howard Jay Siegel

Thomas Wei Chen

Hiroshi Sakurai

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## ABSTRACT

### DESIGN AND IMPLEMENTATION OF A COMPACT HIGHLY EFFICIENT 472KHZ RF GENERATOR FOR ELECTROSURGERY

This thesis explores the utilization of modern design practices and advance technologies to reduce the size of traditional 472kHz radio frequency generators used for electrosurgery. Achieving the reduced size requires an innovative approach to increase the overall efficiency to lower the internal heat dissipation allowing the overall package size to shrink. This thesis covers the selection and design process to achieving the final topology of an innovative approach utilizing a variation of the Class-D amplifier to produce a resonance type power saturation amplifier. While using a high-efficiency power source to control the amplifier voltage rails, and to control the amplitude of the output signal will produce a sinusoidal power source capable of driving a radio frequency surgical scalpel.

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***Introduction of Project***

The overall goal for this thesis topic was to evaluate, design, build and demonstrate a modern approach to producing a radio frequency generator suitable for electrosurgery.

Traditional electrosurgical generators (Figure 1.1) control the output power as a function of load as seen by the cutting tool to manage the types of cuts and to control bleeding.

The form factor of the commercial generator is 11.1cm (H) x 35.6 cm (W) x 43.9cm (L) and 8.1kg.



*Figure 1.1; Commercial electrosurgical generator*

Electrosurgical generators must operate at high enough frequencies to prevent neuromuscular stimulations, and to reduce the risk of electrocution. Above 100kHz [1], muscles cannot respond to the high frequency making neuromuscular stimulation a non-issue. Also at higher frequencies, the risk of electrocution is greatly reduced by the skin effect forcing current flow the exterior of the conduction path [1]. Thus, the conduction path becomes more directional. This control of the current path reduces the risk of the current crossing the heart leading to electrocution [1].

## *Design Specifications*

As a starting point, this project was provided rough specifications (Table 1.2) as a design goal. This included an output power de-rating as a function of load impedance (Table 1.3), overall output load range (Table 1.2), operating frequency (Table 1.2) and package size (Table 1.2). The rest of the details was left open and would need to be defined by the project before work could begin.

*Table 1.2; Rough design goals*

<b>Parameter</b>	<b>Specification</b>
Output Frequency	472kHz
Output Load Impedance	20 to 500 Ohms
Package size	77mm x 102mm x 51mm

*Table 1.3; Output power verses output load impedance.*

<b>Load (<math>\Omega</math>)</b>	<b>Power (Watts)</b>
20	112.0
25	93.0
50	75.0
75	58.0
100	48.0
150	33.0
200	26.0
300	18.0
400	15.0
500	13.0

In order to determine the output requirements for the voltage swing and maximum current the output power de-rating specifications (Table 1.3) was expanded to include the peak-to-peak voltage and root-means-square (RMS) current (Table 1.4). Using the expanded table of performance requirements (Table 1.4), it was determined that the



maximum output voltage swing of approximately 250 volts peak-to-peak with a maximum RMS current of 2.37 amps.

*Table 1.4; Expanded output de-rating performance verses output impedance.*

<b>Load (Ω)</b>	<b>Power (Watts)</b>	<b>Voltage (V peak-peak)</b>	<b>Current (Amps RMS)</b>
20	112.0	133.8	2.37
25	93.0	136.4	1.93
50	75.0	173.2	1.23
75	58.0	186.5	0.879
100	48.0	196.0	0.693
150	33.0	199.0	0.469
200	26.0	204.0	0.361
300	18.0	207.8	0.245
400	15.0	219.1	0.194
500	13.0	228.0	0.161

Present-day electrosurgical generators (Figure 1.5) are large heavy units mounted on carts that require precious floor space leading in operation area. This identified another key design target to reduce the package size with the ideal goal of being small enough that the electrosurgical generator could be worn on a belt or kept in a pocket.



*Figure 1.5; Example of cart mounted commercial electrosurgical generators*

This size restriction defines the next key design requirement of ultrahigh efficiency. As the package size decrease, heat and thermal management increase in difficulty.

Reduction in size limits the options of using fans and heat sinks to manage the thermal dissipation become less of a viable solution. As an example, if a power source is operating at 70% efficiency and the output power demand is 120 watts, the internal heat dissipation would be 51 watts. Dissipating 51 watts in a small package without some type of thermal management device could be difficult and could lead to the external temperature of the package being excessive to a point that handling it would be uncomfortable. If the overall efficiency is increased from 70% to 80%, than the internal power dissipation decreases to 30 watts, which can be managed easier than 51 watts. This defines the initial design target of the overall efficiency to be greater than 80% to lower the internal heat dissipation and in turn allowing a reduction in package size.

The original specifications did not require the project to meet any agency standards like Underwriters Laboratories Inc. (UL) or International Electrotechnical Commission (IEC), but does need to address safety for users. The first safety requirement is the prototype must be capable of being powered from a safe low voltage source. As defined by the IEC “Extra-Low Voltage (ELV)” [3][4] is defined as a voltage less than 35V RMS (60VDC) [4] voltage is considered to be a safe level to minimize electrical shock in dry conditions.

Another critical safety factor is to reduce electrical shock by provide isolation from the 110Vac power line and the low voltage input. The addition of isolation produces a “Separated or Safe Extra-Low Voltage (SELV)” [3][4] that furthers reduces risk of

electrical shock. The simplest solution to producing a low voltage source that meets the requirement of “safe” is to use an isolated off-the-shelf power source that is certified to by an safety agencies (UL).

Another important limitation that was not clearly specified was the allowed output frequency range. Referencing the Federal Communications Commission (FCC) frequency allocation tables [5] the maximum output frequency must not interfere with the mobile distress and calling broadcast frequency of 495kHz [5]. The lower frequency limit is not as critical as the upper frequency limit other than it must remain high enough to prevent neuromuscular stimulation [1], and will be arbitrarily chosen to be 23kHz based on the allowed upper deviation.

*Table 1.5; Summary design specifications*

<b>Parameter</b>	<b>Specification</b>
Input Voltage Range	42 to 60 VDC
Output Frequency at 50 Ohm	472kHz
Frequency Variation	±23kHz
Max output power	112 Watts at 20 Ohms
Output power derating	13 Watts at 500 Ohms
Output Load Impedance	20 to 500 Ohms
Max output voltage at no load	250 Volts peak to peak
Max output current at full load	2.5A RMS
Efficiency	>80% at full power
Package size	77mm x 102mm x 51mm

***Amplifier Topology Selection***

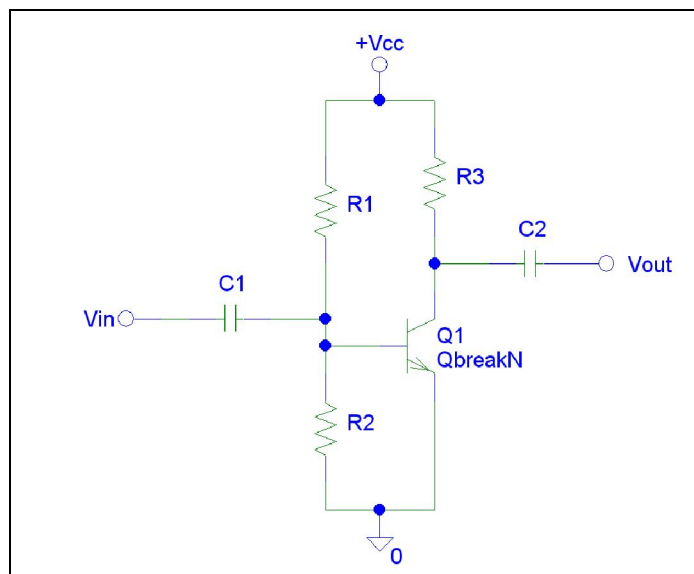
Producing a 472kHz signal at significant power levels for a wide range of load impedances requires some form of amplification. Selection of the appropriated amplifier topology is a tradeoff between amplification methods, efficiency, complexity, and safety. Most amplifier topologies require either higher power supply voltage rails in the amplifier stage or utilize an output transformer to produce the required output voltage swing.

As a starting point, it is important to determine a suitable amplifier topology for use up to 500kHz for desired efficiency target and output performance requirements. Traditional radio frequency amplifiers operate at higher frequencies greater than 500kHz and commonly start at 2MHz and go up from there. Another option, is a modified audio-type amplifier that could operate at frequencies as high as 1MHz.

***Class-A***

The Class-A amplifier is the simplest of all amplifier topologies. Shown in Figure 2.1 is a more complete diagram with the necessary biasing to operate the transistor in a linear region. A major limitation to the Class-A amplifier is it only uses one output transistor to drive the output towards the lower power supply rail and relies on a resistor to pull the output signal to the positive power supply rail. For high power applications, the resistor (R3) is required to be much smaller than the load to provide symmetrical drive and to

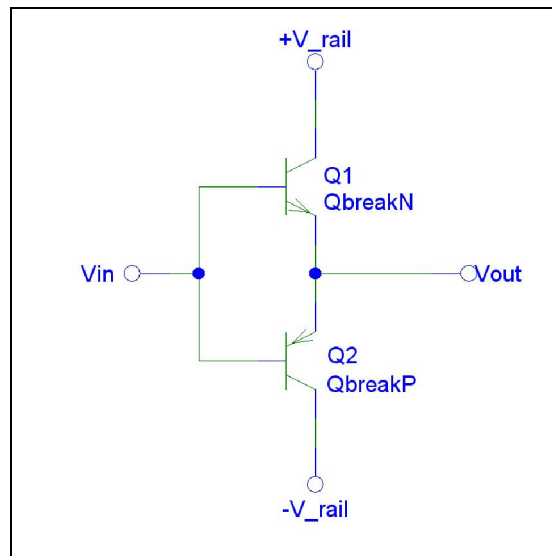
minimize distortion of the output signal. At steady state (idle) the biasing of the amplifier dissipates 50% of its power even when the output is not active. The efficiency of a Class-A amplifier configuration decreases further when operating with a maximum attainable efficiency of 25% [6]. Based on the low efficiency of the Class-A amplifier configuration, it makes it a non-suitable topology for this application and will not be considered for use.



*Figure 2.1; Simplified Class-A amplifier*

## ***Class-B and Class-AB***

The Class-B amplifier is a modification of the Class-A amplifier where the resistive element in the output stage is replaced by a second transistor (Figure 2.2). This provides a push-pull driver that allows the output to be symmetrically driven towards both power supply rails. One drawback to the Class-B amplifier is that the output exhibits inactive periods when operating at lower input signals when the conduction of the power devices are transitioning between the lower transistor (Q2) and the upper transistor (Q1). This transition is called cross-over distortion (Figure 2.3), and leads to higher total harmonic distortion.



*Figure 2.2; Simplified Class-B amplifier*

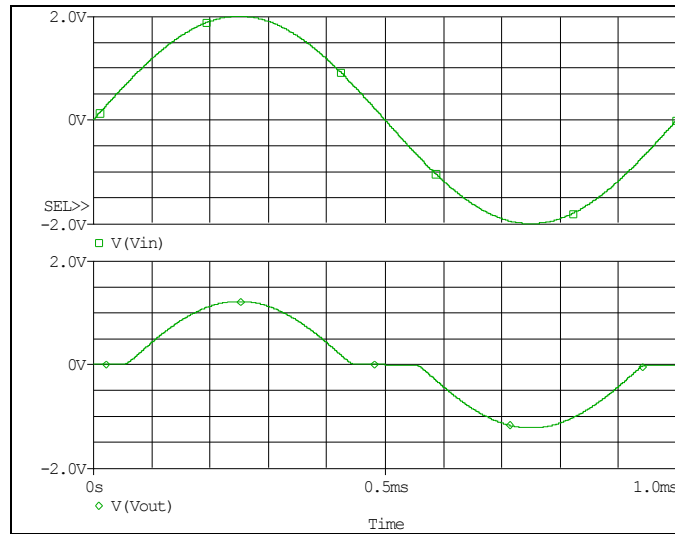


Figure 2.3; Class-B amplifier Input-Output waveform

A simple solution to the crossover distortion is to weakly bias the output stage to force the output transistors in a constant active region. This variation of the Class-B with a weak output bias is called the Class-AB (Figure 2.4). Utilizing the Class-AB, greatly reduces the output cross-over distortion resulting in an output waveform (Figure 2.5) that results in a lower total harmonic distortion.

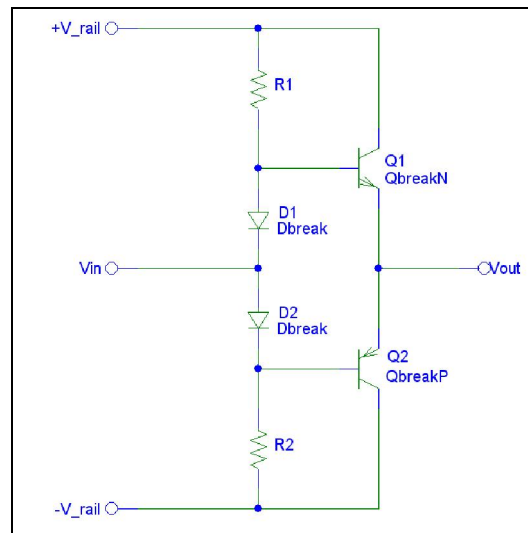
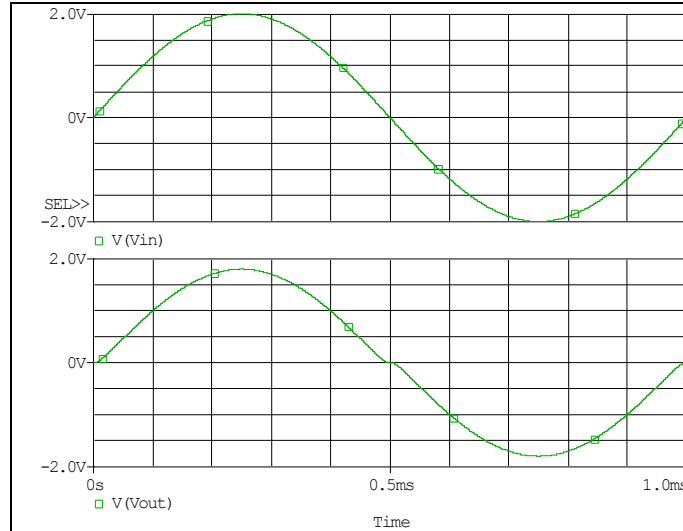


Figure 2.4; Simplified Class-AB amplifier



*Figure 2.5; Class-AB amplifier Input-Output waveform*

The Class-B and Class-AB amplifier topologies are possibly suitable for this application because of the simplicity, low distortion and symmetrical output drives, and will be covered in more detail later in this document.

### ***Class-C***

The Class-C amplifier (Figure 2.6) is a nonlinear amplifier commonly used in radio frequency applications, and has a low conduction angle less than 180 degrees [6] (Figure 2.7). The nonlinear property produces a highly distorted output that resembles nothing of a sinewave, and for this reason this topology is not suitable for this application.



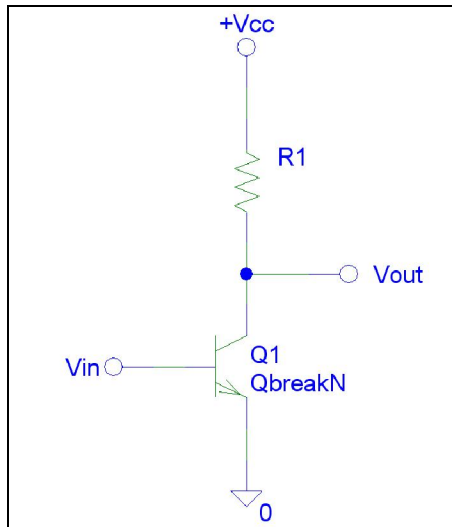


Figure 2.6; Simplified Class-C amplifier

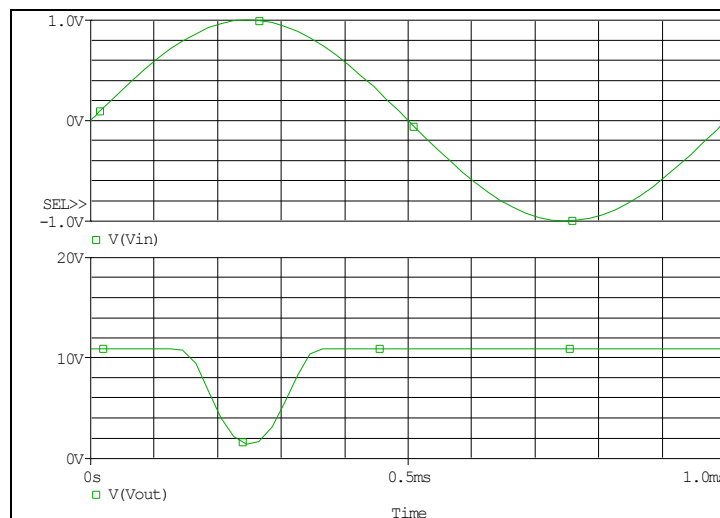


Figure 2.7; Class-C amplifier Input-Output waveform

### ***Class-D***

The Class-D amplifier is basically a high power rectangle generator that produces a Pulse Width Modulation (PWM) output signal that represents some analog signal. Following the amplifier stage is a LC low-pass filter that demodulates the PWM signal leaving the

lower frequency modulation signal. Shown in Figure 2.8 below is the relationship of the input signal (red trace labeled  $V_{in}$ ), PWM signal (green trace labeled  $V_{pwm}$ ) and output signal ( $V_{out}$ ). The Class-D amplifier topology is highly efficient, simple and capable of high power levels. This makes this topology a strong candidate and will be covered in detail further on.

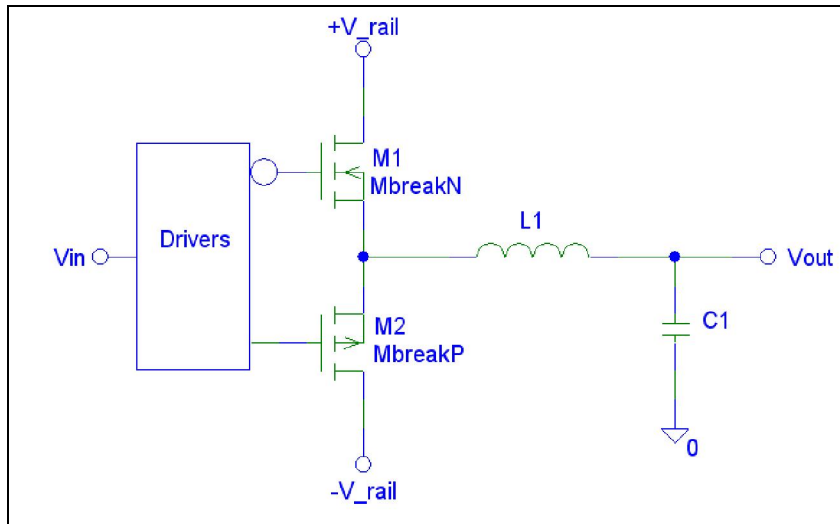


Figure 2.8; Class-D Audio amplifier

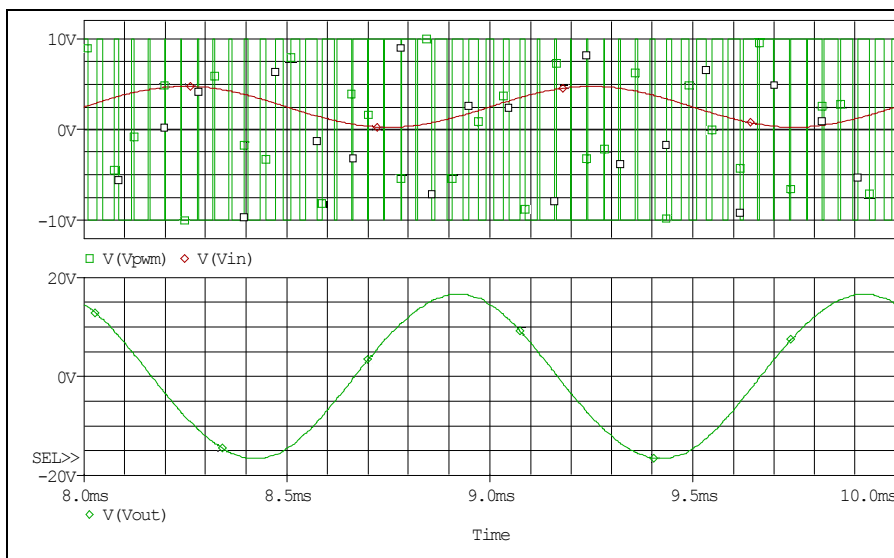
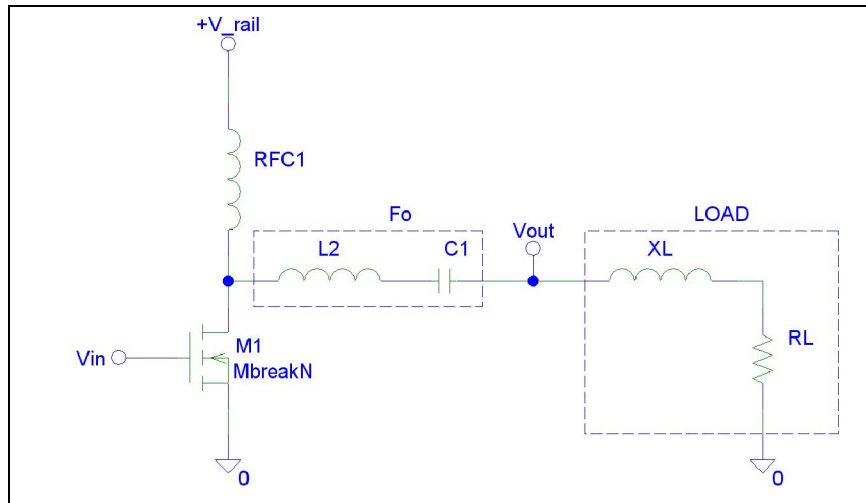


Figure 2.9; Class-D amplifier Input-Output waveform

## ***Class-E and Class-F***

These classes of amplifiers are true RF amplifiers and are designed for a limited frequency range with small variations in load impedance. The narrow range of load impedance makes these topologies not suitable for this application.



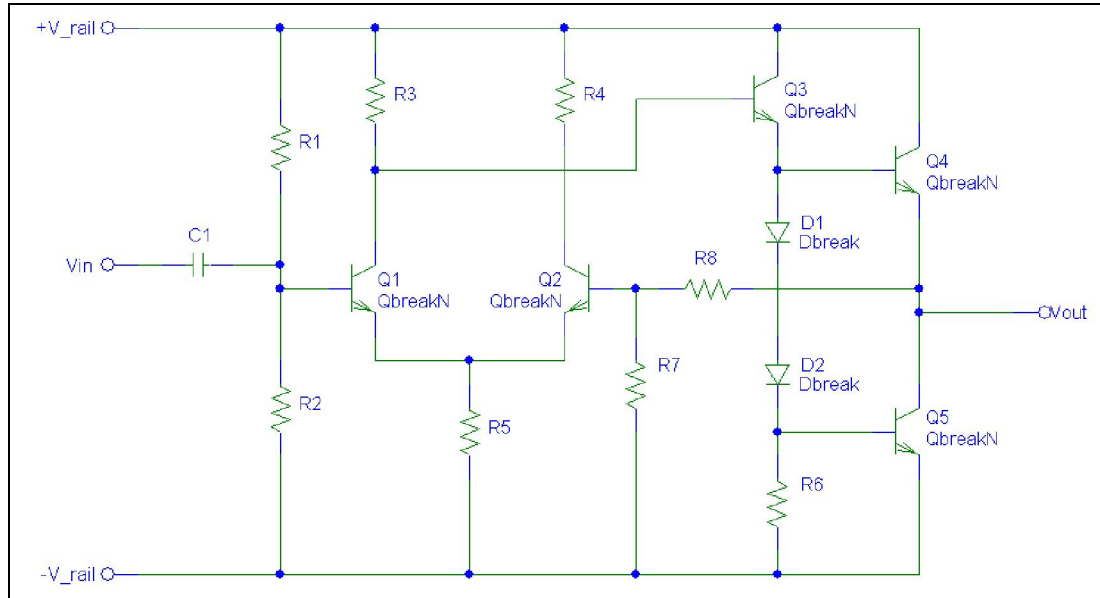
*Figure 2.10; Class E/F RF amplifier*

## ***Comparison of Chosen Amplifier Topologies***

Narrowing down the final amplifier topology will be determined by the efficiency of the proposed amplifier topologies and ease of use at 500kHz. The first task at hand is to determine the advantages and disadvantages between Class AB audio to Class AB radio frequency amplifiers.

The basic circuit configuration of audio Class AB amplifier (Figure 2.11) is an example of a direct couple amplifier with negative feedback consisting of a power stage and a

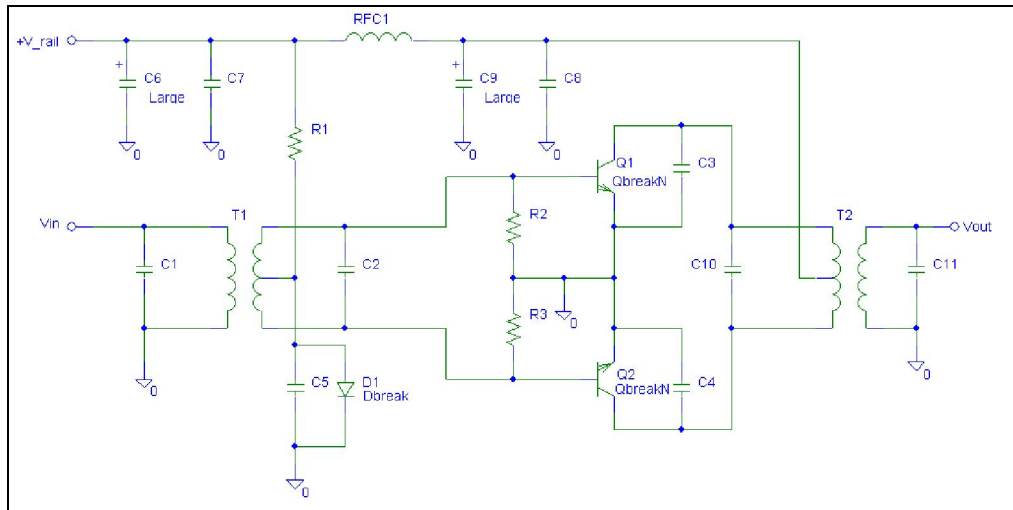
differential input stage. The overall circuitry is rather simple and can easily be designed into a smaller package based on component count and size.



*Figure 2.11; Audio Class AB Amplifier*

Reviewing the schematics for a typical radio frequency amplifier (Figure 2.12) for use at 500kHz at 140W is far more complex than the simple Class AB audio amplifier (Figure 2.11). It is clearly much more complicated than the audio counterpart, because there are three magnetic devices, and most likely each one is a custom design. The magnetic devices are an input transformer, an output power transformer and a radio frequency blocking inductor (also known as a radio frequency choke (RFC)). One other major variation between the two amplifier types is that the typical radio frequency amplifier is intended for a narrow range of output load impedance to limit the reflected power. Minimizing reflected power loss is achieved by matching the output impedance of a RF amplifier to the load impedance. A varying output load impedance over a large range increases the reflected power leading to additional stress on the power components. A

common solution for driving varying load impedances is to use a matching network, which adds complexity to the amplifier design and design of the custom magnetic. A common method of impedance matching for a narrow or fixed load is to use a transformer.



*Equation 2.13; Radio Frequency Class AB Push-Pull Amplifier*

The simplicity of the Class AB audio amplifier is an attractive quality for use in this application, but there is one major drawback, the typical overall efficiency of the Class AB amplifier is not that great. The estimated efficiency of the Class AB audio amplifier is at best 78.5% (Equation 2.13) when operating at maximum output voltage swing. To maintain the 78.5% with a varying output load and requires the power supply rails to be controlled and maintained slightly above the required peak output voltage. This enhanced variation of the Class-AB amplifier is a Class-G. In order to produce a variable power supply voltage at respectable efficiency requires the use of a switch mode power supply that has the ability to adjustable the output voltage through some command signal, and at the same time regulate the output voltage. In conjunction with controlling the

power supply rails, the input signal will have to be managed to prevent clipping or saturation of the output stage. Having two independent control loops can lead to instability under varying operating conditions, which leads to a more complex design.

$$\begin{aligned}
 P_{\text{Load}} &= \frac{1}{2} \cdot \frac{V_{\text{o\_peak}}^2}{R_{\text{Load}}} & I_{\text{Load}} &= \frac{V_{\text{o\_peak}}}{\pi \cdot R_{\text{Load}}} \\
 P_{\text{in}} = P_{\text{rail\_pos}} + P_{\text{rail\_neg}} &= 2 \cdot (I_{\text{Load}} \cdot V_{\text{ps}}) = \frac{2}{\pi} \cdot \frac{V_{\text{o\_peak}}}{R_{\text{Load}}} \cdot V_{\text{ps}} \\
 \eta = \frac{P_{\text{Load}}}{P_{\text{in}}} &= \frac{\left( \frac{1}{2} \cdot \frac{V_{\text{o\_peak}}^2}{R_{\text{Load}}} \right)}{\left( \frac{2}{\pi} \cdot \frac{V_{\text{o\_peak}}}{R_{\text{Load}}} \cdot V_{\text{ps}} \right)} \\
 \eta = \frac{\pi}{4} \cdot \frac{V_{\text{o\_peak}}}{V_{\text{ps}}} & \quad \text{if } V_{\text{o\_peka}} = V_{\text{ps}} & \eta &= \frac{\pi}{4} = 78.5
 \end{aligned}$$

*Equation 2.13; Class AB Amplifier Efficiency*

At this point in the selection process, the appropriate amplifier topology should have the simplicity and gain in efficiency of the Class-AB/G Audio Amplifier with adjustable supply rails.

### ***Amplifier Power Source***

There are three options for producing the variable power supply rails: 1) step-up the input voltage, 2) step-down the input voltage or 3) a combination of step-up and step-down.

Each topology will be briefly covered to point out the fundamental advantages and disadvantages for operation at high power. By limiting the analysis to high output power simplifies the analysis to only continuous conduction mode (CCM), which means the current in the switching inductor remains greater than zero amps. The analysis for each

converter will include deriving the transfer functions for the output voltage, the inductor current and the power loss estimation.

Deriving the output voltage transfer function will be done by evaluating the inductor volt-second balance as described in the “Fundamentals of Power Electronics, 2nd edition” [7].

At steady state, the inductor average voltage must equal zero. This means that over one complete switch cycle the energy into the inductor is equal to the energy taken out of the inductor.

$$\int_0^{T_s} v_L dt = 0$$

*Equation 2.14; Definition of inductor volt-second balance*

The time cycle is described in terms of the time the switch is on ( $T_{on}$ ) and has current flowing through it. If the cycle frequency remains constant then the switch time can be noted as duty cycle (D).

$$D = \frac{T_{on}}{T_s} = \frac{T_{on}}{T_{on} + T_{off}}$$

*Equation 2.15; Duty cycle of switch ON time*

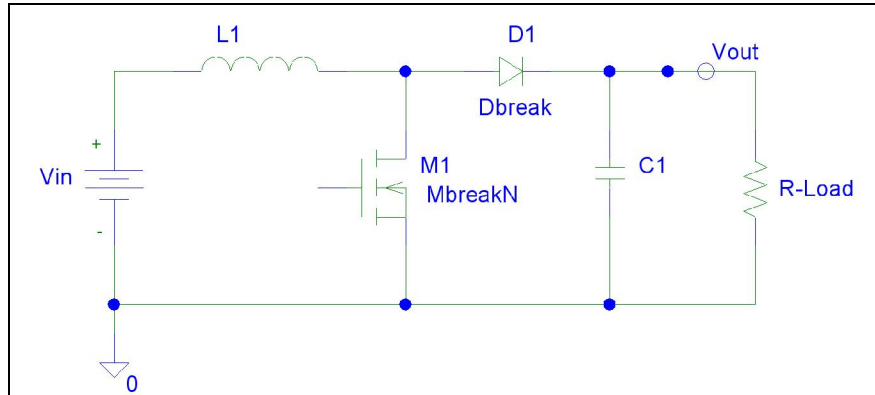
Likewise, the off time ( $T_{off}$ ) can be described in terms of D.

$$1 - D = \frac{T_{off}}{T_{on} + T_{off}}$$

*Equation 2.16; Duty cycle of the switch OFF time*

## ***Boost Topology***

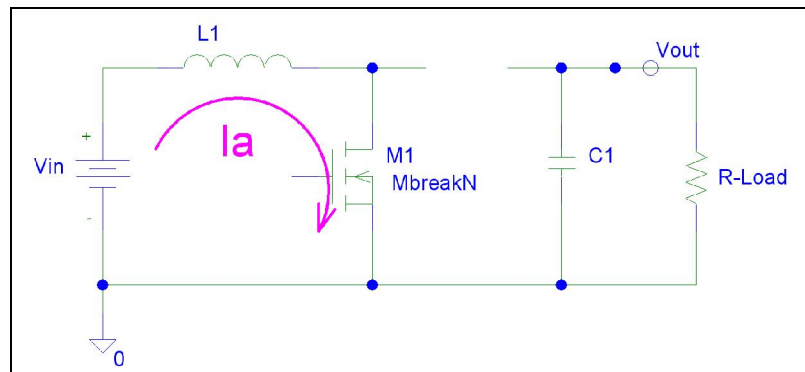
The boost topology (Figure 2.17) steps up the input voltage to produce a higher output voltage.



*Figure 2.17; Basic Boost Topology*

While the switch ( $M1$ ) is active, current flows through the inductor ( $L1$ ) and the switch for the duration of time ( $T_{on}$ ) resulting in the current waveform ( $I_{sw}$ ) (Figure 2.18).

With the switch in the active state, the voltage across the inductor is just the input voltage ( $V_{in}$ ), which provides half of the inductor volt-second balance (Equation 2.19).



*Figure 2.18; Boost current flow during the on time ( $T_{on}$ )*



$$V_{in} \cdot D$$

Equation 2.19; Volt-second for the ON time

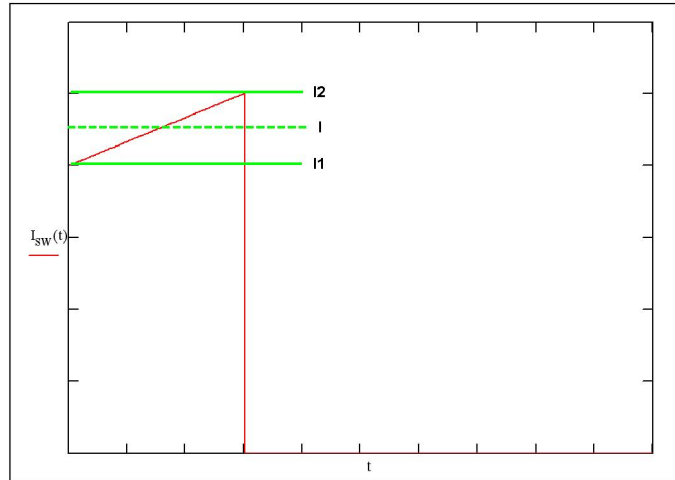


Figure 2.20; Switch current waveform during the on time ( $T_{on}$ )

When the switch is in the inactive state, the energy in the inductor is transferred to the output capacitor (C1) and to the load through the diode (D1) resulting in the current waveform (Ib). The voltage across the inductor is  $V_{in} - V_{out}$  during the switch off time.

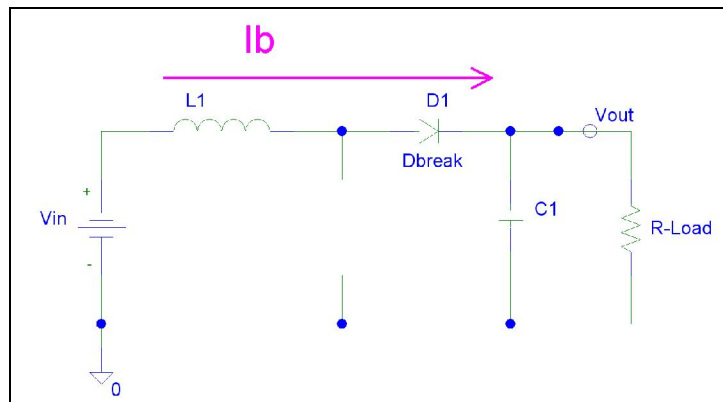


Figure 2.21; Boost current flow during the off time ( $T_{off}$ )

$$(V_{in} - V_o) \cdot (1 - D)$$

Equation 2.22; Volt-second for the OFF time

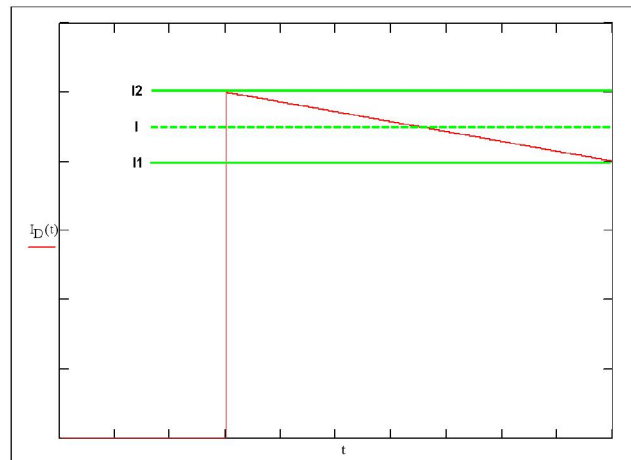


Figure 2.23; Diode current waveform during the off time ( $T_{off}$ )

The final inductor current waveform (Figure 2.25) and volt-second balance equation (Equation 2.24) for the boost converter is shown below.

$$\int_0^{T_s} v_L dt = V_{in} \cdot D \cdot T_s + (V_{in} - V_o) \cdot (1 - D) \cdot T_s = 0$$

Equation 2.24; Volt-second equation for the Boost converter

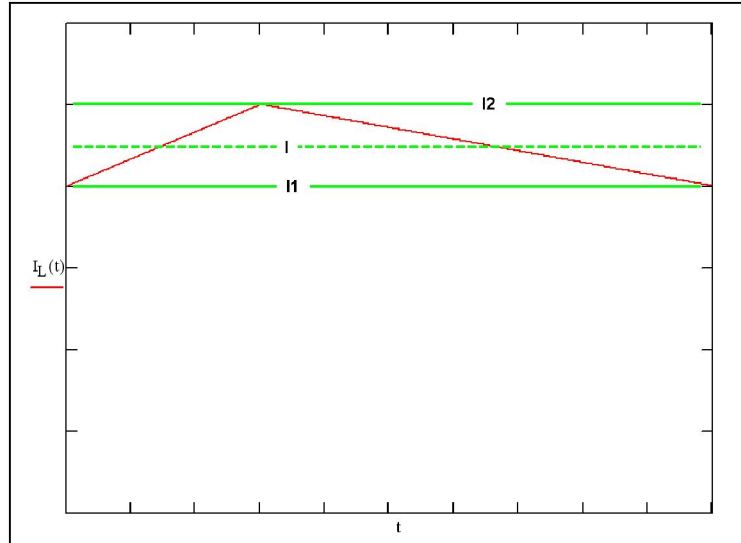


Figure 2.25; Inductor current waveform for one cycle

The output voltage transfer function for the boost converter is found by breaking down the complete volt-second balance equation to isolate the output voltage ( $V_o$ ) and input voltage ( $V_{in}$ ) in terms of duty cycle ( $D$ ) over one cycle. Since the evaluation is done for one cycle the  $T_s$  terms drop out.

$$\begin{aligned}
 V_{in} \cdot D \cdot T_s + (V_{in} - V_o) \cdot (1 - D) \cdot T_s &= 0 \\
 \text{Let } 1 - D &= D_p \\
 V_{in} \cdot D + (V_{in} - V_o) \cdot D_p &= 0 \\
 V_{in} \cdot (D + D_p) - V_o \cdot D_p &= 0 \\
 \text{Since } D + D_p &= 1 \\
 V_{in} &= V_o \cdot D_p \quad + \\
 V_o &= \frac{V_{in}}{1 - D}
 \end{aligned}$$

Equation 2.26; Deriving the output voltage transfer function from the volt-second

Using the principle of a balance current flow in the output capacitor will help derive the transfer function for the inductor current. During steady state operation, the current into the capacitor is equal to the current consumed by the load. This is similar in manner as the volt-second balance for the inductor, but for the output capacitor, and is referred to as “capacitor charge balance”.

Switch ON	$-I_o \cdot D$
Capacitor charge balance	
Switch OFF	$(I_L - I_o) \cdot (1 - D)$
Capacitor charge balance	
$\int_0^{T_s} i_C dt = -I_o \cdot D \cdot T_s + (I_L - I_o) \cdot (1 - D) T_s = 0$	
<p>Let <math>I_o = \frac{V_o}{R_{Load}}</math> and <math>D_p = 1 - D</math></p>	
$-\frac{V_o}{R_{Load}} \cdot D + \left( I_L - \frac{V_o}{R_{Load}} \right) \cdot D_p = 0$	
$-\frac{V_o}{R_{Load}} \cdot D + I_L \cdot D_p - \frac{V_o}{R_{Load}} \cdot D_p = 0$	
$I_L \cdot D_p = \frac{V_o}{R_{Load}} \cdot (D + D_p)$	
$I_L = \frac{V_o}{R_{Load}} \cdot \frac{1}{(1 - D)}$	

*Equation 2.27; Deriving the Inductor current transfer function from the charge-balance*

From the analysis of the steady state operation of the converter, the output voltage transfer function was found using the inductor volt-second and the average inductor current transfer function from the output capacitor charge balance.

$$V_o = V_{in} \cdot \frac{1}{1 - D}$$
$$I_L = \frac{V_o}{R_{Load}} \cdot \frac{1}{(1 - D)}$$

*Equation 2.28; Basic Boost SMPS equations*

Majority of the losses in a converter are related to conduction and switching of the power switches. To keep the selection process simple, only the conduction losses will be evaluated. Resistive heating is related to the RMS currents. The basic definition of root-means squared (RMS) (Equation 2.29), but this would be hard to apply to the current waveforms of a converter. A simpler method is to use the predefined equations for common converter waveforms that are provided in the Appendix of the “Fundamentals of Power Electronics, 2nd edition” [7] to find the RMS switch current (Figure 2.30), and the inductor RMS current (Figure 2.31).

$$X_{rms} = \sqrt{\frac{1}{T} \int_{t_0}^{t_0+T} X^2(t) dt}$$

*Equation 2.29; Definition of RMS*

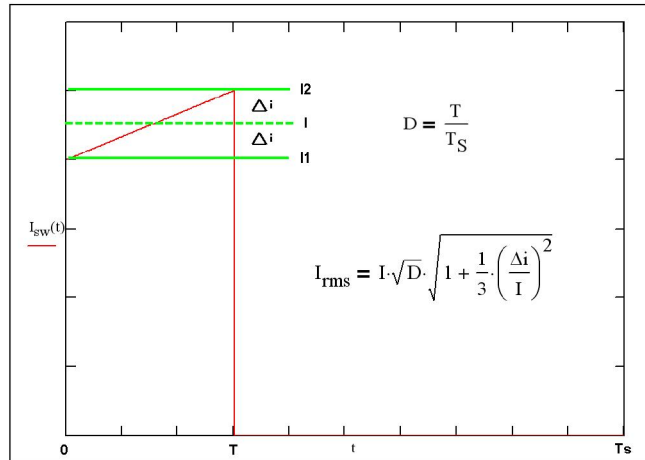


Figure 2.30; RMS Equation for diode waveform

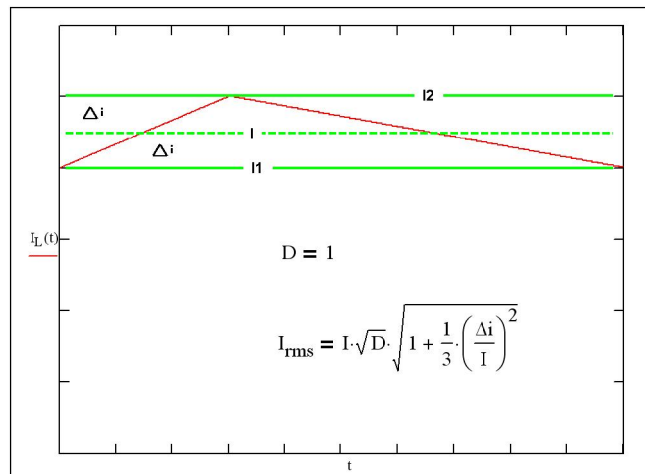


Figure 2.31; RMS Equation for inductor waveform

The RMS and average currents (Equation 2.32) for the boost converter are now known and can be used to calculate the losses in the major components.

$I_{\text{rms\_L}} := I_L \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{I_L}\right)^2}$	$I_{\text{avg\_L}} := V_{\text{in}} \cdot \frac{1}{(1-D)^2 \cdot R_{\text{Load}}}$
$I_{\text{rms\_sw}} := I_L \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{I_L}\right)^2}$	$I_{\text{avg\_sw}} := D \cdot (\Delta i + I_L)$
$I_{\text{rms\_diode}} := I_L \cdot \sqrt{1-D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{I_L}\right)^2}$	$I_{\text{avg\_diode}} := (1-D) \cdot (\Delta i + I_L)$

Equation 2.32; Average and RMS currents of basic boost supply

### ***Buck Topology***

The counter part to the boost converter is the buck converter that steps down the input voltage to a lower output voltage. Like the boost converter, the buck converter has the same basic power components, but arranged in a slightly different configuration (Figure 2.33). As a starting point for comparison the system of equations for Buck topology will be derived in the same manner as done in the previous section about the boost converter.

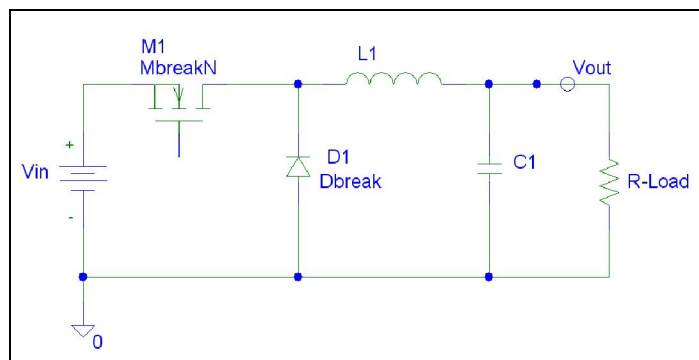


Figure 2.33; Basic Buck Topology

In the on state ( $T_{on}$ ) the switch current ( $I_a$ ) (Figure 2.34) flows through the switch and inductor to the load and output capacitor. When the switch is in the off state ( $T_{off}$ ), the inductor current ( $I_b$ ) (Figure 2.34) flows through the load and diode back to the inductor.

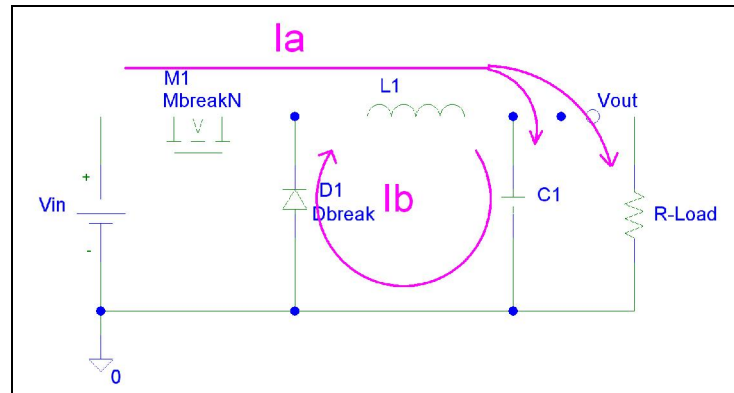


Figure 2.34; Buck converter current flows

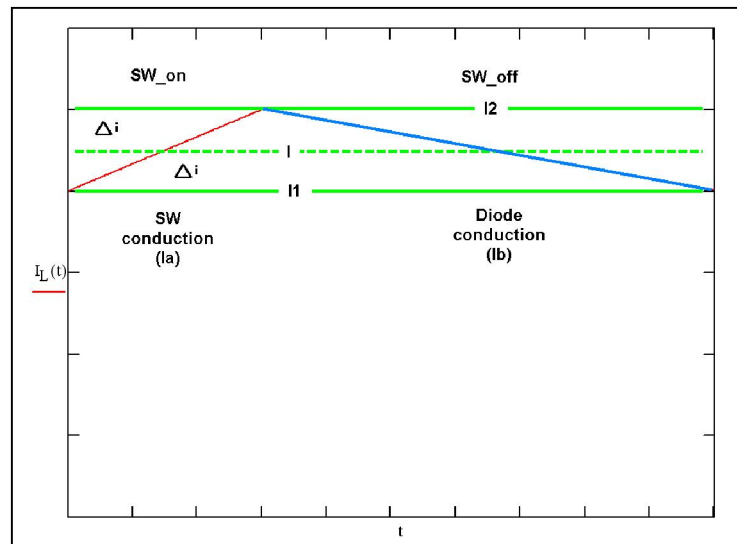


Figure 2.35; Buck converter inductor current waveform



Switch ON Volt-second balance	$(V_{in} - V_o)D$	Switch ON Capacitor charge balance	$(I_L - I_o) \cdot D$
Switch OFF Volt-second balance	$-V_o \cdot (1 - D)$	Switch OFF Capacitor charge balance	$(I_L - I_o) \cdot (1 - D)$

$\int_0^{T_s} v_L dt = (V_{in} - V_o)D \cdot T_s - V_o \cdot (1 - D) \cdot T_s = 0$ $(V_{in} - V_o)D \cdot T_s - V_o \cdot (1 - D) \cdot T_s = 0$ <p style="text-align: center;">Let <math>1 - D = D_p</math></p> $(V_{in} - V_o)D - V_o \cdot D_p = 0$ $V_{in} \cdot D - V_o \cdot D - V_o \cdot D_p = 0$ $V_{in} \cdot D - V_o(D - D_p) = 0$ <p style="text-align: center;">Since <math>D + D_p = 1</math></p> $V_o = D \cdot V_{in}$	$\int_0^{T_s} i_C dt = (I_L - I_o) \cdot D \cdot T_s + (I_L - I_o) \cdot (1 - D) \cdot T_s = 0$ <p style="text-align: center;">Let <math>I_o = \frac{V_o}{R_{Load}}</math> and <math>D_p = 1 - D</math></p> $\left(I_L - \frac{V_o}{R_{Load}}\right) \cdot D + \left(I_L - \frac{V_o}{R_{Load}}\right) \cdot D_p = 0$ $\left(I_L - \frac{V_o}{R_{Load}}\right) = 0$ $I_L = \frac{V_o}{R_{Load}}$
---	--

*Equation 2.36; Buck Volt-second and Capacitor charge balance*

### ***Buck-Boost (Flyback) Topology***

The Buck-Boost converter combines the boost and buck converters into one, creating the flyback topology. The flyback topology uses an isolation inductor, also commonly known as a flyback transformer. The flyback transformer is not really a common passive transformer, but rather a multi-turn inductor on a common core with a turns ratio from primary to secondary windings.

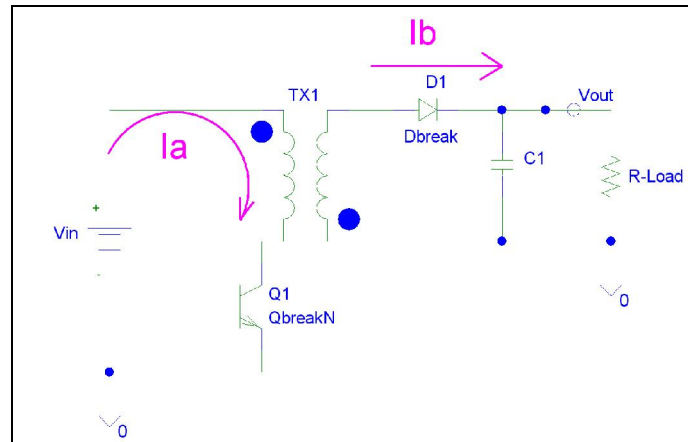


Figure 2.37; Flyback converter with current flows

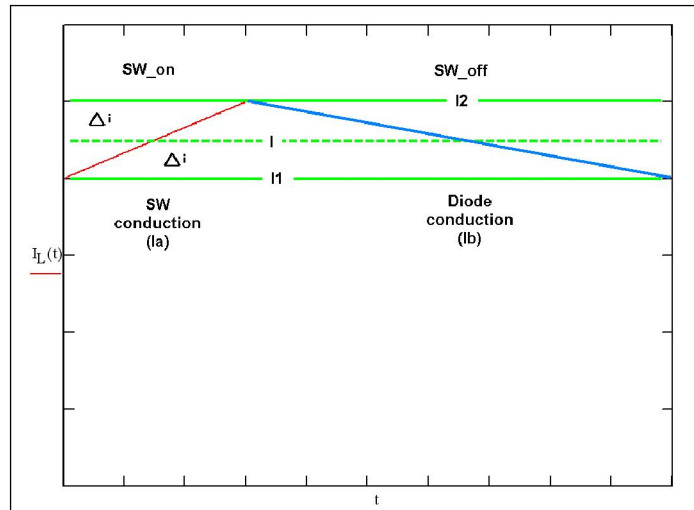


Figure 2.38; Flyback converter inductor current waveform

<p>Switch ON Volt-second balance <math>V_{in} \cdot D</math></p> <p>Switch OFF Volt-second balance <math>\left(\frac{-V_o}{n}\right) \cdot (1-D)</math></p> $\int_0^{T_s} v_L dt = V_{in} \cdot D \cdot T_s + \left(\frac{-V_o}{n}\right) \cdot (1-D) \cdot T_s = 0$ $V_{in} \cdot D \cdot T_s + \left(\frac{-V_o}{n}\right) \cdot (1-D) \cdot T_s = 0$ <p style="text-align: center;">Let <math>1-D = D_p</math></p> $V_{in} \cdot D + \left(\frac{-V_o}{n}\right) \cdot D_p = 0$ $V_{in} \cdot D = \left(\frac{V_o}{n}\right) \cdot D_p$ $V_o = V_{in} \cdot n \cdot \frac{D}{1-D}$	<p>Switch ON Capacitor charge balance <math>-I_o \cdot D</math></p> <p>Switch OFF Capacitor charge balance <math>\left(\frac{I_L}{n} - I_o\right) \cdot (1-D)</math></p> $\int_0^{T_s} i_C dt = -I_o \cdot D \cdot T_s + \left(\frac{I_L}{n} - I_o\right) \cdot (1-D) \cdot T_s = 0$ <p style="text-align: center;">Let <math>I_o = \frac{V_o}{R_{Load}}</math> and <math>D_p = 1-D</math></p> $-\frac{V_o}{R_{Load}} \cdot D + \left(\frac{I_L}{n} - \frac{V_o}{R_{Load}}\right) \cdot D_p = 0$ $-\frac{V_o}{R_{Load}} \cdot D + \frac{I_L}{n} \cdot D_p - \frac{V_o}{R_{Load}} \cdot D_p = 0$ $\frac{I_L}{n} \cdot D_p = \frac{V_o}{R_{Load}} \cdot (D + D_p)$ $I_L = \frac{V_o}{R_{Load}} \cdot \frac{n}{(1-D)}$
---	---

*Equation 2.39; Flyback Volt-second and Capacitor charge balance*

### ***Comparison of Efficiencies for Converter Types***

A simple empirical comparison for overall efficiency of each converter topology is possible by calculating the losses for each component, then summing the losses. As a starting point, the component parameters (Table 2.40) and operational points (Table 2.41) must remain consistent across all topologies. Now, a drawback to this method is that it does not take into consideration the dynamic losses such as switching loss, proximity and skin effect losses in the inductors and leakage inductance.

*Table 2.40; Component parameter assumptions*

Parameter	Value
Switch resistance	0.03 ohms
Diode drop	1.0 volts
Inductor resistance	0.01 ohms
Copper resistance	0.01 ohms

*Table 2.41; Converter operation assumptions*

Parameter	Value
Switch Duty Cycle	50 %
Output Load	100 watts
Output Voltage	20 volts

Efficiency losses are directly related to the RMS currents and not the average current that is typically used to calculate the input current, inductor current and output current. For this reason, the heating losses will be calculated for each switch state using the RMS current values of the elements in that path. To simplify the calculations, the inductor ripple current ( $2 \cdot \Delta i$ ) will be assumed to be 10% of the output current, and the duty cycle will be assumed to be 50% for all converters.

Based on the empirical comparisons (Table 2.43) and neglecting the dynamic losses, the least efficient converter is the Flyback, then the Boost, with most efficient being the Buck converter. In a practical application, the dynamic losses would contribute additional losses further decreasing the empirical efficiency.

*Table 2.42; Currents for each converter type*

	Boost	Buck	Buck-Boost
Output Voltage	20 Volts	20 Volts	20 Volts
Output Current	5 Amps	5 Amps	5 Amps
Average Inductor Current	10 Amps	5 Amps	20 Amps
RMS Inductor current	10.02 Amps	5.02 Amps	20.03 Amps
RMS switch current	7.09 Amps	3.54 Amps	14.17 Amps
RMS diode current	7.09 Amps	3.54 Amps	7.09 Amps

Table 2.43; Losses for each converter type

	Boost	Buck	Buck-Boost
Inductor	1.00 Watts	0.25 Watts	4.01 Watts
Switch	1.50 Watts	0.375 Watts	6.01 Watts
Diode	7.09 Watts	3.55 Watts	7.09 Watts
Output Copper	0.50 Watts	0.125 Watts	2.01 Watts
Input Copper	1.00 Watts	0.125 Watts	0.50 Watts
Total Losses	11.09 Watts	4.425 Watts	19.62 Watts
Empirical Efficiency (without dynamic losses)	88.9%	95.6%	80.4%

### ***Buck with Synchronous Rectification Topology***

Modern advancement of synchronous rectification combined with the switching buck topologies is achieving ever-higher efficiencies and depending on applications are approaching the high 80 percentages and low 90 percentages. Replacing the freewheeling diode (Figure 2.44) with an actively controlled switch that is synchronized out of phase with the main power switch significantly reduces the diode losses. In this example, it reduces the diode losses by one magnitude from 3.55 W to 376 mW.

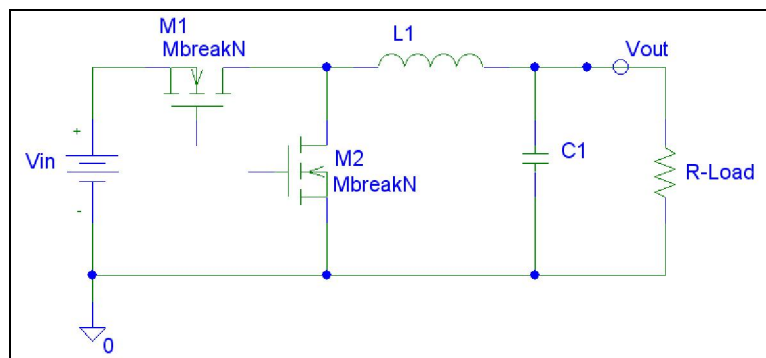
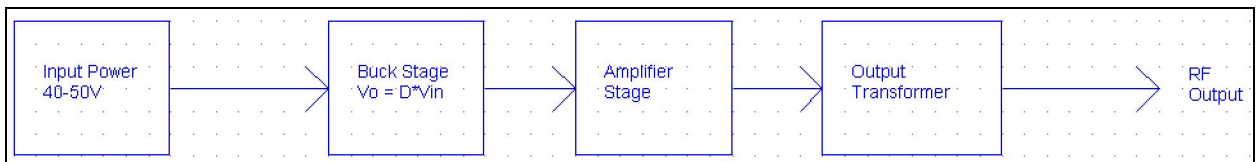


Figure 2.44; Basic Buck with Synchronous Rectification Topology

## *The Birth of the Basic System*

The downside of using a lower input voltage range and a buck converter still leaves the method of amplification open. Utilizing a passive transformer on the output of the amplifier provides a simple solution. The inefficiency of the transformer can be controlled through good design practices, which should yield an efficiency of at least 95% [8,9]. This will be covered in further depth in the next chapter as part of the design process.

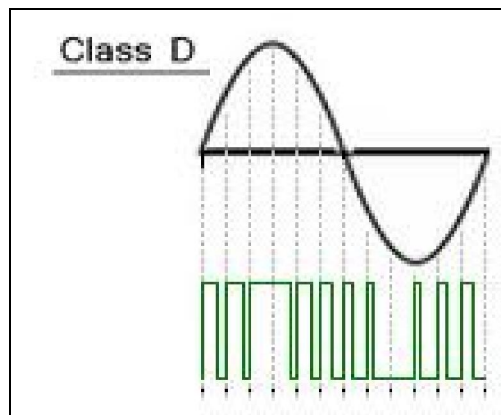
At this point in the selection process the most suitable power source and amplifier topologies for the radio frequency generator is a buck converter in combination with a transformer coupled output Class-AB/G amplifier. Using the estimated efficiencies, 92% for the Synchronous-Buck converter, 78.5% for the Class AB/G amplifier and 95% for the transformer, yields an over estimated efficiency of 68.6%.



*Figure 2.45; System Block Diagram*

The initial efficiency estimate using a Class-AB/G topology is not adequate to meet the design target of 80% total efficiency. In order to move forward, another type of amplifier topology will have to be identified. Using the total efficiency target and the estimations for the power converter stage and transformer defines the efficiency requirement for the amplifier stage to be at least 91.5%.

At 91.5%, this is a challenging design goal for any amplifier and would most likely force the topology towards a saturation-type amplifier. The most common saturation-type amplifier is a Class-D, which produces an output signal using a pair of power devices operating at full-on (saturation). To generate a nonrectangular type waveform by switching the amplifier on/off, the output is modulated using a pulse width modulation (PWM) scheme (Figure 2.46). The modulated output signal can be filtered through a low pass filter to remove the PWM signal and lower the distortion of the output signal.



*Figure 2.46; Class-D Amplifier Input to Output Modulation*

In a Class-D amplifier, the primary loss mechanisms are conduction losses and switching losses of the power devices. Modern power MOSFETs are achieving ultra-low on resistance well below 20 m $\Omega$  [10], significantly reducing the conduction losses and making the switching losses more of a concern. It is common that power devices are hard switched, which means the voltage across the device and the current through the device transitions are at the same time. This produces losses proportional to the frequency, voltage and current. Another option to reducing the switching losses is to operate the power devices in a resonant mode to force the switching mode to zero voltage

switching (ZVS) or zero current switching (ZCS). Unfortunately, Class-D amplifiers using pulse width modulation to generate a sinewave are forced to operate at a higher modulation frequency above the fundamental frequency of the output signal, which leads to hard switching.

Generating a 472kHz sinewave using a Class-D and pulse width modulated signal (Figure 2.46), would require the modulation frequency to be much higher than the desired output frequency. Even increasing the switching frequency by a factor of 5 would have a significant impact on the efficiency performance of the amplifier due to the increased switching losses of hard switching.

A compromise to achieving higher efficiencies using the Class-D amplifier would be to reduce the switching frequency and not use pulse width modulation to generate a sinewave. Instead, using a Class-D amplifier topology to generate a square wave at 50% duty cycle and then amplifying the output signal using a transformer. A major drawback to this approach is the output signal is a square wave output that will have higher distortion and potentially higher odd harmonic losses than a sinewave.

To simplify the power supply stage and avoid the requirement of producing a negative supply rail, the other input lead of the output transformer must be connected to either a second amplifier that is 180 degrees out-of-phase or some source that is one-half the supply rail. Adding either will increase complexity and impact the efficiency. A common technique in high voltage power supplies is to use a capacitive voltage divider to



generate the virtual common for the other lead of the primary transformer. This solution is simple, with low costs and low losses.

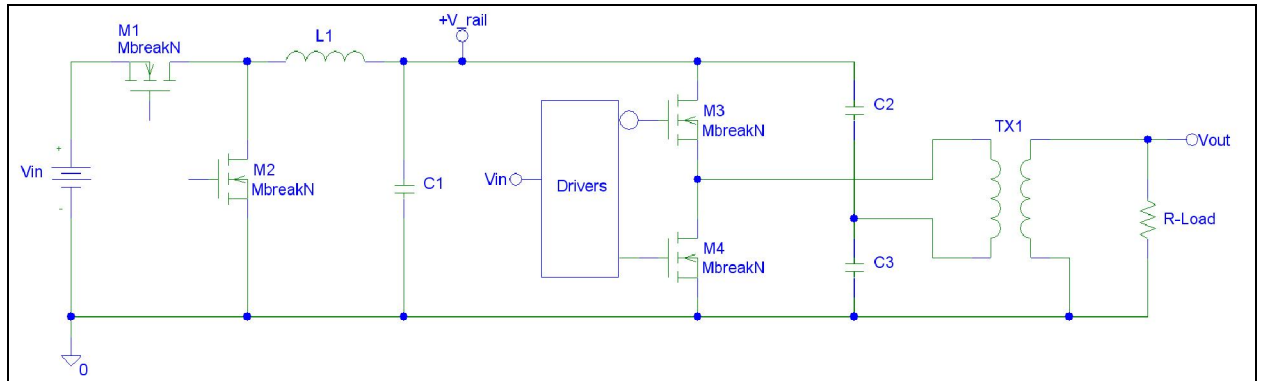
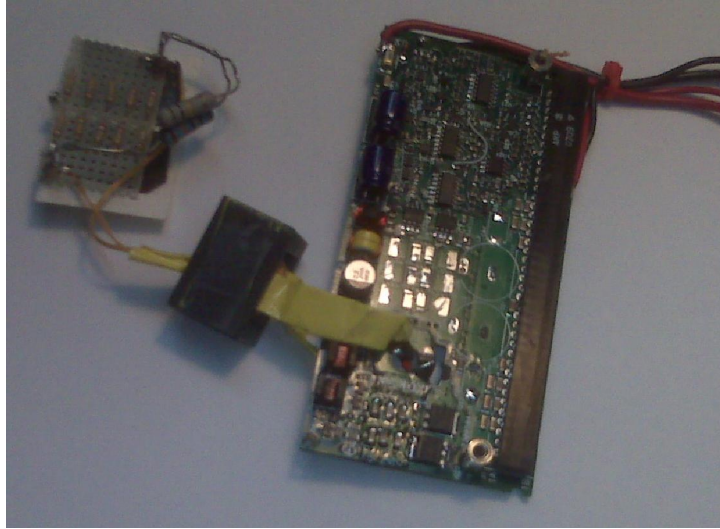


Figure 2.47; Class-D Amplifier with transformer output and buck input

### ***Class-D Transformer Coupled Output***

The Class-D amplifier with an output transformer was prototyped (called “Early Prototype”) on the bench using an existing capacitive couple half bridge DC-DC converter that was designed for 400kHz DC-DC converter. This prototype was limited in performance and was not expected to meet the design target specifications, but helps to prove the concept of generating a variable amplitude output at 472kHz.



*Figure 2.48; Prototype of Class-D with transformer output*

The output performance of the prototype was based on the early design target to produce a high voltage output at a lower current limit, but still at 50W.

*Table 2.49; Target design specifications for Early Prototype*

Input Voltage Range	42 to 50 Vdc
Output Frequency	472kHz
Max output power	50 Watts
Max output voltage	1000 Volts peak to peak 353.6 Volts RMS
Max output current	0.142 Amps RMS

The simplified schematic (Figure 2.50) of the “Early Prototype” will be used to explain the theory of operation. Generation of the output frequency is done using a free running oscillator (Clock Gen 944kHz) that drives a D-Flip-Flop to produce two drive signals at 472kHz, 180 degrees out-of-phase and at 50% duty cycle. The output signals from the D-Flip-Flop are level shifted and amplified to produce high voltage drive signals for the

power MOSFETs (M1 and M2). The output of the power MOSFETs drive one side of the transformer (TX1), and the other end of the transformer is connected to the capacitive voltage divide (C2 and C3).

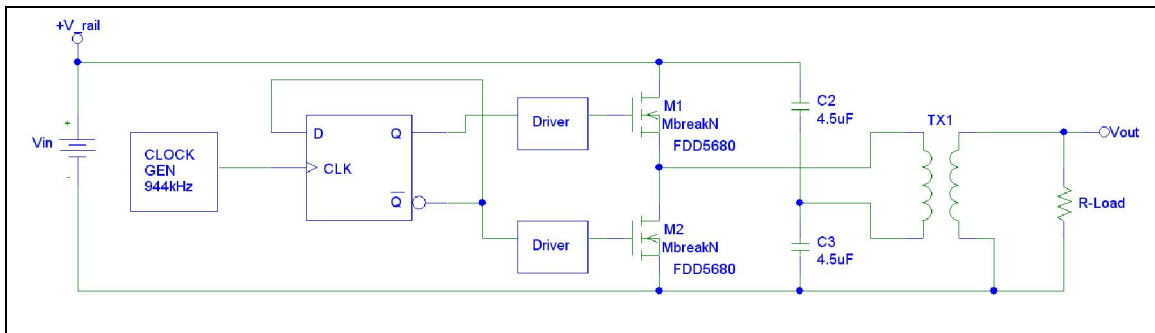


Figure 2.50; Simplified schematic of the “early prototype”

For a quick check of concept of generating a 472kHz, the transformer core of the original product was changed to a larger size and turns were added. However, the core material was not changed and not optimized for 472kHz. There are much better core materials available, and will be covered in detail later.

Table 2.51; Properties of “early prototype” transformer

Core	EQ30 – 3C96
Primary Turns	1T copper foil 0.006” thick by 0.500” wide
Secondary Turns	20T, bifilar 26 AWG wire
Primary inductance	1.62uH
Secondary inductance	640uH
Primary leakage inductance	20nH
Secondary leakage inductance	3.7uH
Secondary self resonance frequency	4.167MHz

Testing of the early prototype yielded some interesting results. First the transformer did run a bit hotter than expected, but this is was not surprising with the core material that was used (3C96) was not optimum for 472kHz and the original frequency of the modified product was around 400kHz. Another interesting result was that the output of the transformer was ringing, which indicated that using a square wave at 472kHz could be an issue. However, on the flip-side, the rapid prototype showed promise for the control method of using variable power supply rails to control the output amplitude. Using a fixed frequency and variable supply rails, the output was controllable and frequency was highly stable across loads.

### ***The Transformer Challenge***

It is clear from the results of the “early prototype” that using a transformer to achieve the desired higher output voltages leads to design complexities. At higher frequencies, the parasitic properties of the transformer becomes significant and must be addressed in the design of the transformer, and will be more pronounced with increased turns. Typically, to avoid exciting the parasitics leading to excessive ringing at higher frequencies is to use a none square wave, but rather a sine type waveform. When applying a none sinusoidal waveform to a transformer, the higher harmonic contents of the signal could excite the high frequency parasitics of the transformer leading to a under damped response and in turn a ringing output signal (Figure 2.52). The yellow trace is the primary input side of the transformer and the blue is the secondary output.

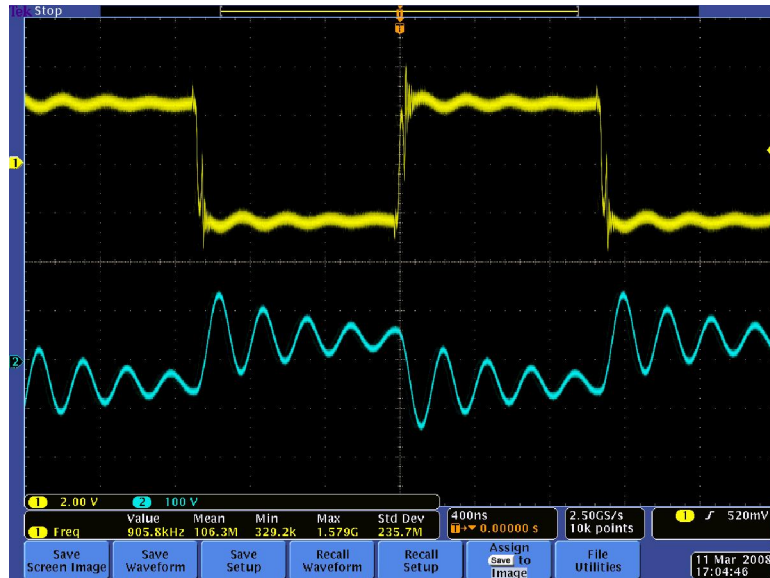


Figure 2.52, Input and Output Signal of the EQ30 transformer

A simple model of the transformer (Figure 2.53) was created as a starting point to understanding the parasitics.

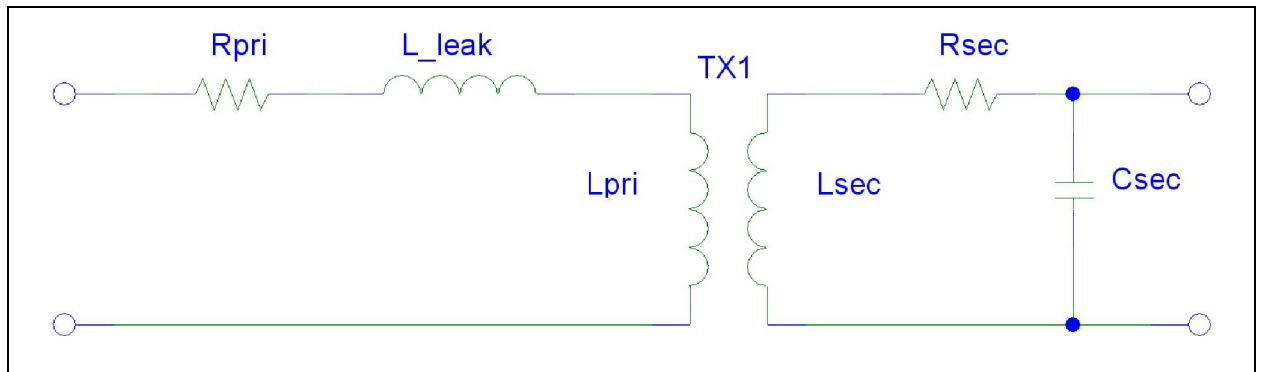


Figure 2.53; Basic Transformer Model

An impedance analyzer is required to find the parasitic properties of the transformer. The basic inductance is measured at the operating frequency, in this case 472kHz. The two main parasitic properties are the secondary winding capacitance and secondary leakage

inductance. To find these parasitic properties, the primary is shorted and the inductance of the secondary is measured, giving the secondary leakage inductance ( $L_{sp}$ ). With the primary still shorted, finding the frequency at the point the output peaks ( $Q_s$ ) is the self-resonance frequency ( $f_{sp}$ ).

$$f_{sp} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{sp} \cdot C_{sec}}} \implies C_{sec} = \frac{1}{(2 \cdot \pi \cdot f_{sp})^2 \cdot L_{sp}}$$

*Equation 2.54; Equation for winding self-resonance*

*Table 2.55; Secondary resonance properties*

Secondary leakage inductance	3.7uH
Calculated Secondary Capacitance	394pF

The small values of the parasitic properties are significant at 472kHz and could be difficult to design around or make less significant. And, as the transformer increases in size to handle higher power levels, the parasitic values will increase. This increase is related to the increase in wire length for the capacitance, and core cross-sectional area for the leakage inductance. The impacts of the parasitic values make using a passive transformer impractical for passing a 472kHz square wave.

One option to overcome the impacts of the transformer parasitics at 472KHz and to maintain a high efficiency would be to avoid using the square wave. A possibility to achieving a none-square wave output signal would be to use a passive resonant network to convert the square wave to a sinewave.

***Detailed Design Process***

This chapter expands on the concept work from the earlier chapters where Chapter 1 defined the high-level expectations and Chapter 2 used the high-level expectations to create the detailed specifications. It is typical that the detailed design phase be the lengthiest portion of the design process and can result in several iterations, and in some sever cases force the design process back to the concept stage.

Chapter 3 is broken down into the following sections.

- 1) Resonant Stage Design
- 2) Transformer Design
  - a. Core Selections
  - b. Winding Wire Selection
  - c. Turns Ratio
- 3) Series Inductor Design
- 4) Resonant Capacitor Selection
- 5) Power Device Selection
- 6) Finalizing the Resonant Stage Model (loss model)
- 7) Design Optimization
- 8) Estimation of Overall Efficiency

### ***Resonant Amplifier Stage***

The results from the testing of the early prototype using a Class-D amplifier to generate a non-square wave indicated that some type of resonant topology would be needed to pass a 472kHz signal through a transformer.

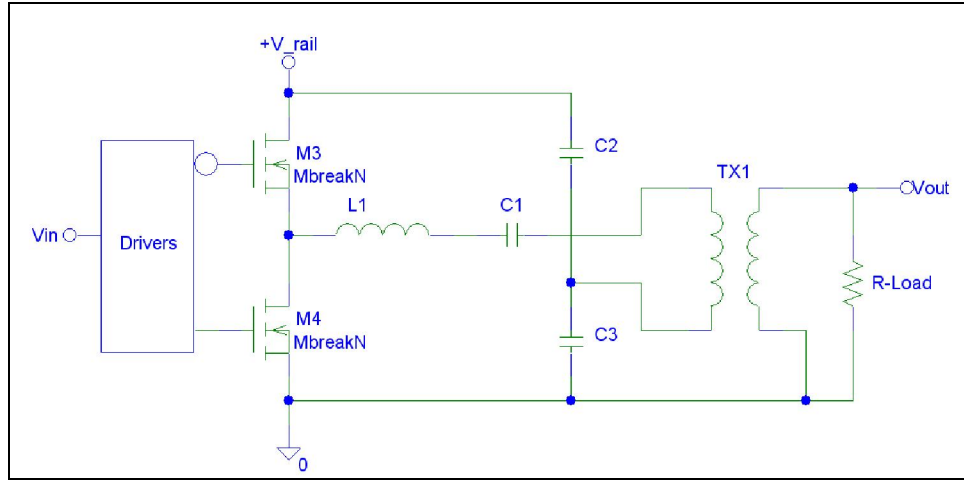
Ideally the resonant circuit will produce a low distortion sinewave and at a low enough distortion the fundamental sinewave will follow the Fourier Transformation for a square wave where the higher order harmonics are not significant. A Fourier series is a sum of sinewaves that form another type of waveform, and a square wave is made up of a sum of odd harmonics (Equation 3.1).

$$SQ_{\text{wave}} = \frac{4}{\pi} \cdot \sum_{n_{\text{odd}}} \frac{1}{n} \cdot \sin(n \cdot f_o)$$

*Equation 3.1; Fourier series for a square wave*

Converting a square wave to sinewave is achieved by using a resonant filter to produce a low distortion sinewave. One option is to add a series inductor and capacitor to the primary side of the transformer to convert the square wave output from the power MOSFETs to a sinewave in order to prevent exciting the parasitics of the transformer and prevent the output from having the high frequency ringing. As seen in the simplified schematic (Figure 3.2) the primary resonant components of the diagram below are L1 and C1 that must work in conjunction with the properties of the transformer, mainly the leakage and magnetizing inductances.





*Figure 3.2; Class-D amplifier with resonant output*

This configuration closely resembles that of a series-resonant LCL converter (Figure 3.3) [7], which typically has a rectification stage on the output of transformer to generate a direct current voltage (VDC). Replacing one-half of the H-bridge by a capacitive link, and removing the bridge rectifier creates the Class-D Amplifier with a resonant stage (Figure 3.2). Operating the modified topology (Figure 3.2) in Continuous Conduction Mode (CCM) the transfer function (Equation 3.4) is simply a voltage divider made up by the reflected output impedance and the input impedance of resonant stage, and multiplied by the fundamental frequency of the Fourier series (Equation 3.1).

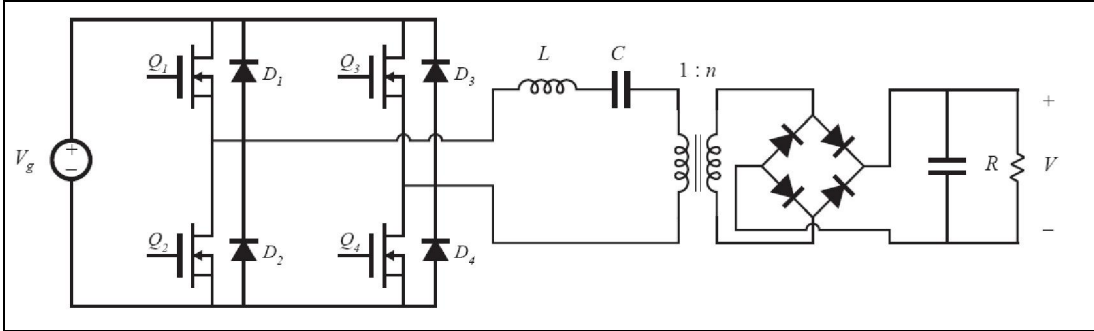


Figure 3.3; Series LCL resonant converter

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{4}{\pi} \cdot \frac{Z_{\text{reflected}}}{Z_{\text{reflected}} + Z_{\text{in}}}$$

Equation 3.4; Transfer function of Class-D resonant amplifier

The addition of C1 in the simplified schematic results in increased losses that is related to the equivalent series resistance (ESR) and contributes to the losses related to C2 and C3. A good compromise is to size C2 and C3 to have the total value of C1 that would eliminate C1 all together (Figure 3.5).

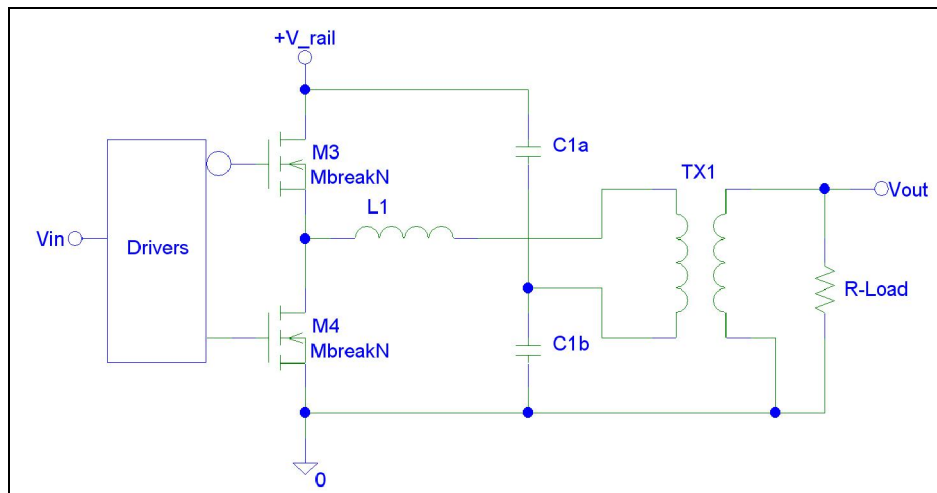


Figure 3.5; Simplified resonant amplifier

Now C1 is made up the total value of C1a and C1b as seen by the current through the primary of the transformer (TX1) (Figure 3.6).

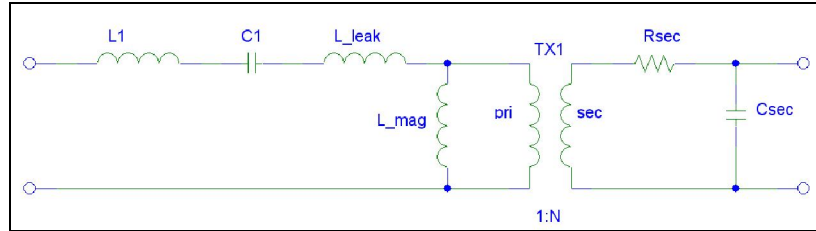


Figure 3.6; Model for Resonant Circuit

By further simplifying the diagram to replace the transformer with the reflected load impedance as a function of the turns-ratio (N), it puts the reflected load in parallel with the magnetizing inductance (Figure 3.7).

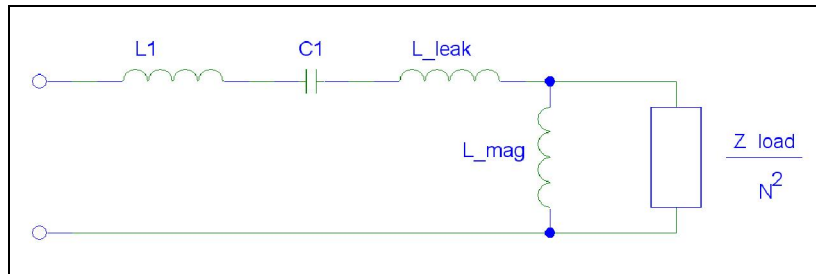


Figure 3.7; Simplified Model for Resonant Circuit

Using the simplified diagram of the resonant circuit yields the following equation (Equation 3.8) that shows the resonant frequency assuming no output load ( $Z_{load} = \text{infinity}$ ).

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (L_1 + L_{leak} + L_{mag})}}$$

Equation 3.8; No load resonant frequency

As the load impedance decreases the effects of the magnetizing inductance becomes less influential on the resonant frequency (Equation 3.9).

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (L_1 + L_{leak})}}$$

*Equation 3.9; Full load resonant frequency*

To minimize the frequency shift with varying loads, the series inductor (L1) can be made much larger than the transformer inductance, making the magnetizing inductance less influential on the resonant frequency. However, there is a trade off with the inductance and capacitance that will be covered more in depth later on in this chapter. Assuming that the L1 is dominant at higher output loads, the resonant frequency equation is simplified (Equation 3.10).

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot L_1}}$$

*Equation 3.10; Full load resonant frequency*

It may be simple to determine the resonant frequency, but it is only one part of the challenge. Next is to determine the optimum transformer turns-ratio for given specifications. This requires one additional component to consider and that is the inherent resistive element that represents the resistance of the traces, transformer windings and AC resistances, such as skin-effect and proximity effect. To simplify the transfer function, the output impedance ( $Z_{load}$ ) is shown as  $R_o$ , and is a function of the turns-ratio (Figure 3.11).

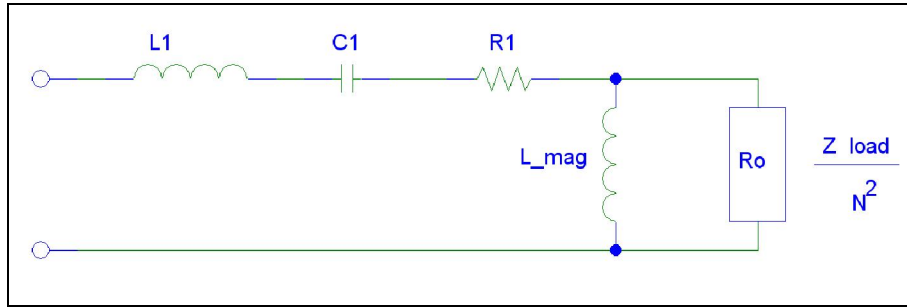


Figure 3.11; Simplified model for resonant circuit with loss resistance

The simplified model can be converted to a series equivalent by solving for the parallel impedance made of the magnetizing inductance and the reflected load impedance.

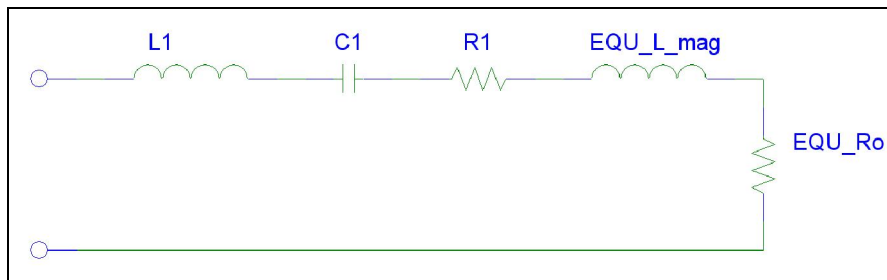


Figure 3.12; Simplified model converted to a series resonant circuit

$$Z_T = \omega^2 \cdot L_{\text{mag}}^2 \cdot \frac{R_o}{(R_o^2 + \omega^2 \cdot L_{\text{mag}}^2)} + i \cdot \omega \cdot L_{\text{mag}} \cdot \frac{R_o^2}{(R_o^2 + \omega^2 \cdot L_{\text{mag}}^2)}$$

Equation 3.13; Complex transformer input impedance

The input impedance ( $Z_{\text{in}}$ ) is:

$$Z_{\text{in}} = R_1 - \frac{i}{\omega \cdot C_1} + i \cdot \omega \cdot L_1 + \frac{i \cdot \omega \cdot L_{\text{mag}} \cdot R_o}{i \cdot \omega \cdot L_{\text{mag}} + R_o}$$

Equation 3.14; Input impedance to resonate circuit

Split into real and imaginary terms:

$$Z_{in} = R_1 + \omega^2 \cdot L_{mag}^2 \cdot \frac{R_o}{(R_o^2 + \omega^2 \cdot L_{mag}^2)} + i \left[ \frac{-1}{\omega \cdot C_1} + \omega \cdot L_1 + \omega \cdot L_{mag} \cdot \frac{R_o^2}{(R_o^2 + \omega^2 \cdot L_{mag}^2)} \right]$$

*Equation 3.15; Input impedance to resonate circuit split into real and imaginary terms*

At resonant, the input of the circuit looks purely resistive since the imaginary term is 0.

$$Z_{in\_real} = R_1 + \omega^2 \cdot L_{mag}^2 \cdot \frac{R_o}{(R_o^2 + \omega^2 \cdot L_{mag}^2)}$$

*Equation 3.16; Real term of input impedance to resonant circuit*

$$Z_{in\_real} = R_1 + R_o$$

*Equation 3.17; Real term with reflected the dominate resistant*

By solving the imaginary term for the radian frequency provides a more accurate resonant frequency, showing the interactions between the other parameters.

$$Z_{in\_imaginary} = \frac{-1}{\omega \cdot C_1} + \omega \cdot L_1 + \omega \cdot L_{mag} \cdot \frac{R_o^2}{(R_o^2 + \omega^2 \cdot L_{mag}^2)}$$

*Equation 3.18; Imaginary term of input impedance to resonant circuit*

Interestingly, the reflected output impedance influences both the real (Equation 3.16) and imaginary (Equation 3.18) terms, and at resonance, the imaginary term is 0, leaving only the real term. The question is how much effect the magnetizing inductance and turns ratio has on the input impedance to the resonant stage. To help clarify the interaction between

turns ratio and magnetizing inductance of the real term of the input impedance ( $Z_{in\_imaginary}$ ), it can be separated into a resistive component ( $R_1$ ) and the primary input of transformer ( $R_o$ ).

Ideally, the reflected output impedance term should dominate the  $R_1$  term and the magnetizing inductance in order to achieve high efficiency. In order to graphically show the effect a couple of rough approximations will have to be made. One would be the turns ratio, which is known to be something greater than one and should be kept to a minimum to help reduce the transformer parasitics. First, the turns ratio can be approximated by using the peak required output voltage and the expected maximum expected DC bus voltage, taking into consideration the Fourier transformation for the first sine wave harmonic of a square wave (Equation 3.20).

$$V_{out\_pk\_pk} = V_{bus\_dc} \cdot \frac{4 \cdot N}{\pi} \cdot \frac{R_L}{N^2 \cdot R_1 + R_L}$$

*Equation 3.19; Basic system transfer function*

$$\begin{aligned}
V_{\text{sine}} &= \frac{4}{\pi} \cdot V_{\text{square}} \\
V_{\text{out\_pk\_pk}} &= N \cdot \left( \frac{4}{\pi} \cdot V_{\text{bus\_max}} \right) \\
V_{\text{out\_pk\_pk\_max}} &:= 250 \quad V_{\text{bus\_max}} := 50 \\
N &:= \frac{V_{\text{out\_pk\_pk\_max}}}{\frac{4}{\pi} V_{\text{bus\_max}}} \\
N &= 3.927
\end{aligned}$$

*Equation 3.20; Estimation of transformer turns ratio*

The magnetization inductance is known to be less than the L1 in order to minimize frequency shift with load change. Based on the magnetics used on the early prototype, it will be assumed to be between 1uH and 3uH Henry.

Given specified operating parameters of the resonant frequency, it is expected to be around 472kHz, and the output impedance is expected to be between 20 ohms to 500 ohms.

$$R_{\text{pri}}(L_{\text{mag}}, \omega, Z_{\text{o}}, N) := \omega^2 \cdot L_{\text{mag}}^2 \cdot \frac{\frac{Z_{\text{o}}}{N^2}}{\left[ \left( \frac{Z_{\text{o}}}{N^2} \right)^2 + \omega^2 \cdot L_{\text{mag}}^2 \right]}$$

*Equation 3.21; Transformer input impedance at resonant*

The plot (Figure 3.22) shows that the input resistance to the transformer is not linear because the reflected output impedance is in parallel with reactance of the magnetizing, which will impact the efficiency.



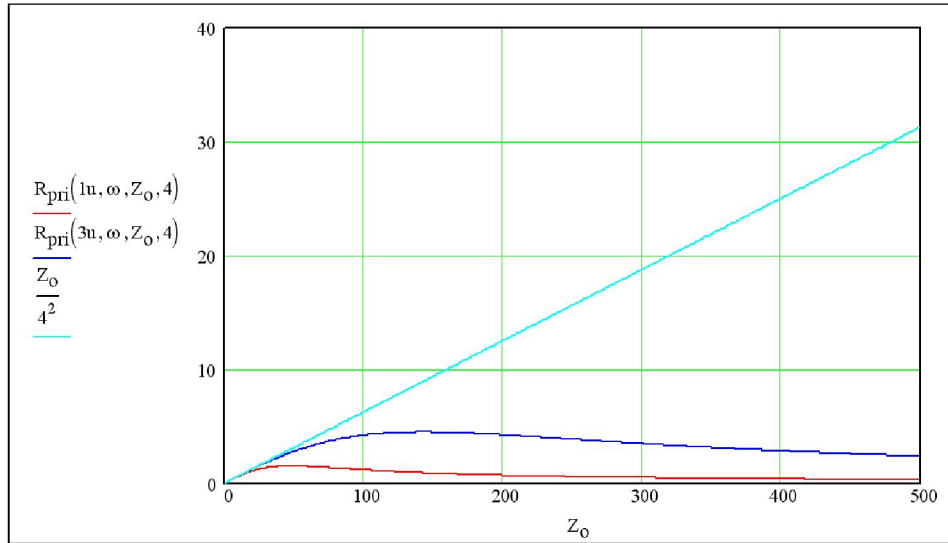


Figure 3.22; Plot of the transformer input impedance as a function load and turns ratio

Using the same plot (Figure 3.22) and decreasing the range of the output impedance to less than 100 ohms shows that even at the maximum load rating for maximum efficiency there is a potential loss caused by the reactance of the primary side magnetizing inductance (Figure 3.21).

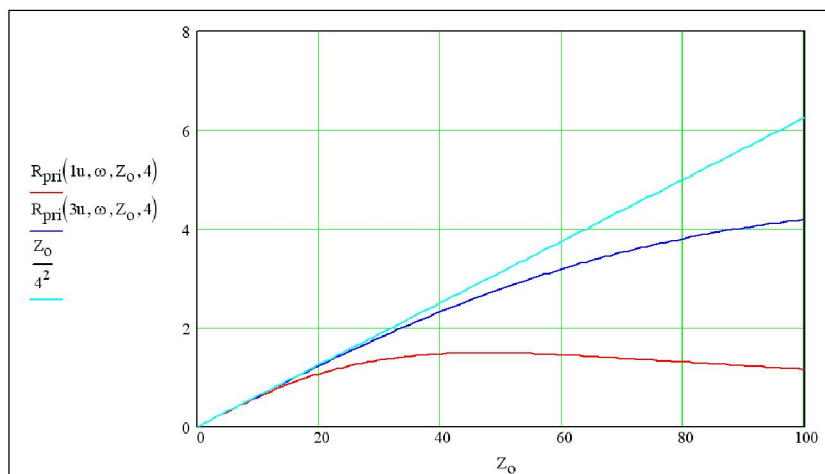


Figure 3.23; Close in plot of the transformer input impedance

At this time, it would be best to look at the details of the transformer design.

## ***Transformer Core Material***

The design process for a transformer is complex and is a constant tradeoff between turns, turns ratio, wire size, cores, winding technique and core material. This section will address the process and method of reaching the final design for the practical transformer for use at 450 kHz to 500 kHz.

The fundamental challenge for any transformer design is to balance the losses with performance. Ideally, by the maximum power theory, the copper losses should be equal to the core losses for maximum power transfer. However modern design techniques [36] high frequency transformer losses are 20/80, where 20% is copper and 80% is core.

Core selection is more of a challenge than one would expect because as operation frequency increases the options of core material decreases, and compounding this is the increasing size. Magnetic core material is commonly some manmade compound that improves the stability of the magnetic permeability and core losses. Losses in the core are related to residual magnetism, also known as hysteresis loss and circulating currents in the core known as eddy losses.

Hysteresis losses are proportional to the amount of B-field and the rate of change in terms of frequency. Figure 3.24 shows that typical BH-curve of a transformer core, which the plot shows the relationship between B-field (magnetic flux density) and H-field (magnetic field strength). The area of the BH-curve is energy remaining in the core after each cycle and this is the Hysteresis loss.

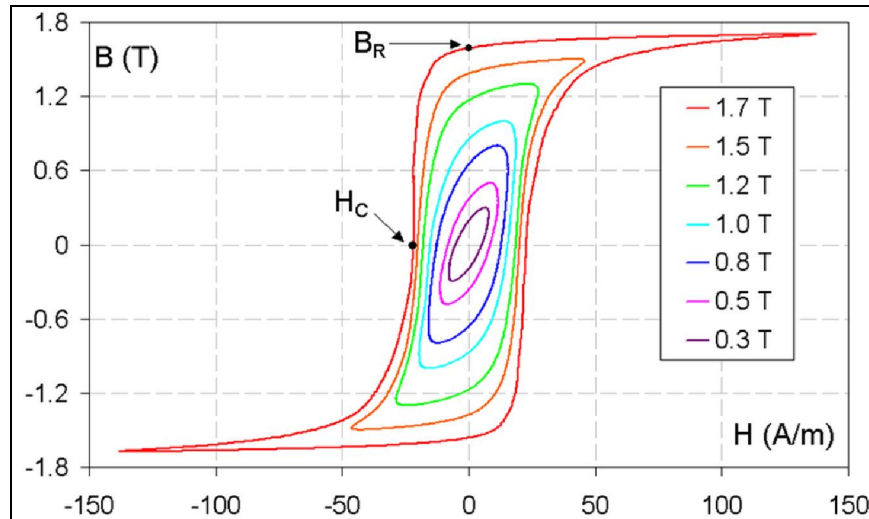


Figure 3.24; Typical BH-curve for a magnetic material

Eddy current losses are actually conduction losses, same as in wires and conductors. Currents are induced in the cores that flow through the core causing heating and in turn additional heating losses.

Selection of the core material is done to primarily address the core losses. Table 3.25 below summarizes the selection of ferrite core material from Ferroxcube that was considered for this application.

Table 3.25; Magnetic and frequency properties for different core material

Material	Frequency range (MHz)	Relative Permeability ( $\mu_i$ )	Saturation Flux Density (mT)
3C96	<0.4	2000	500
3F3	0.2 to 0.5	2000	440
3F35	0.5 to 1.0	1400	500
3F4	1.0 to 2.0	900	410
3F45	1.0 to 2.0	900	420

Based on the target frequency of 500kHz, there are two options that could work at 472kHz, one being the 3F3 and the other the 3F35 material. The testing of the “early prototype” showed that transformer was running hotter than acceptable, which makes sense now knowing that core material is not intended for use above 400kHz. For comparison, the 3C96 material used for the “early prototype” will be added to the list of possible core materials.

Most manufacturers of ferrite core material provide loss curves that show the core loss in power per volume at different frequencies and flux densities. These loss curves can be used to narrow down the selection by examining the core losses around 500kHz at the same flux density and operating temperature. The following curves for each core material is shown in Figure 3.26 for the 3C96, Figure 3.27 for 3F3 and Figure 3.28 for 3F35 that gives a core loss in watts as a function of peak flux density.

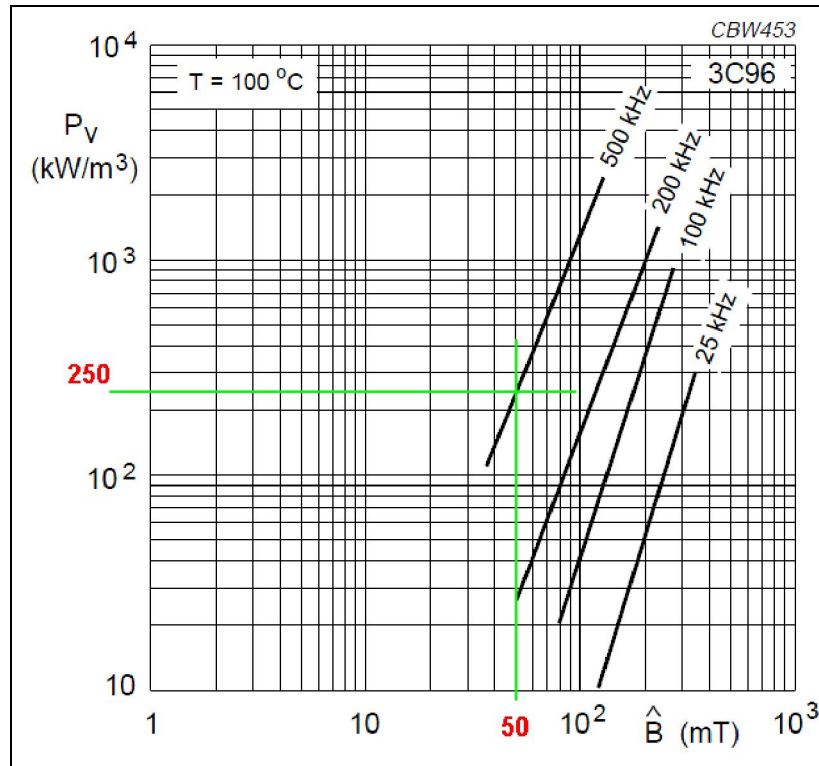


Figure 3.26; Core losses for the 3C96 core material

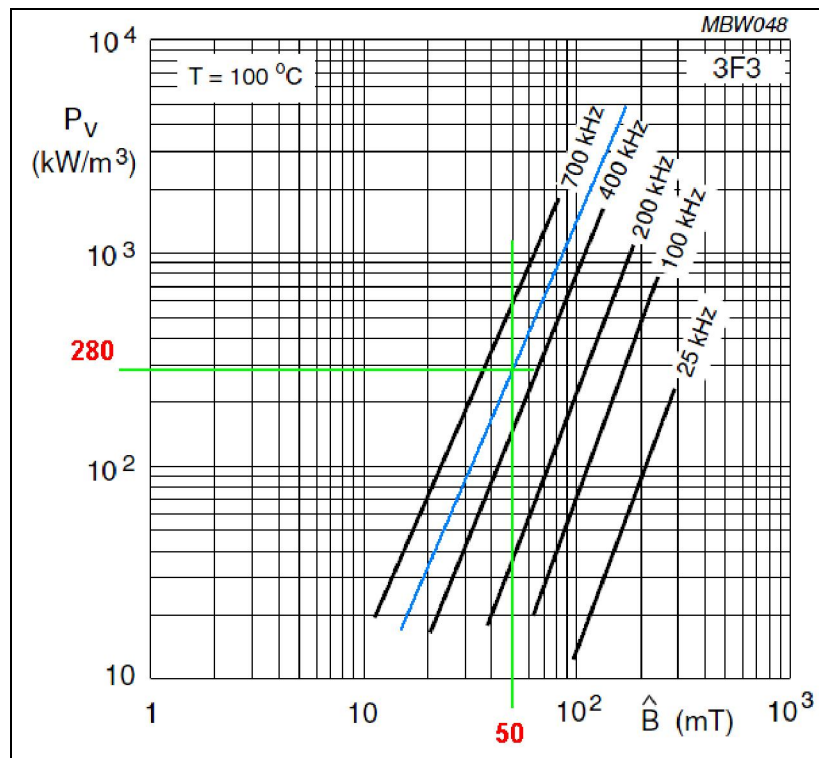


Figure 3.27; Core losses for the 3F3 core material

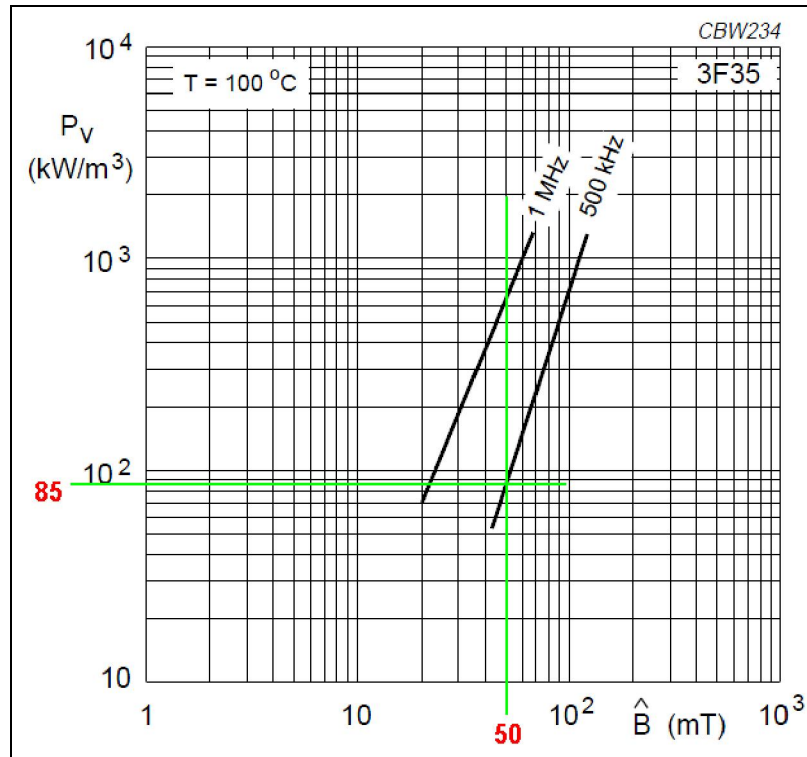


Figure 3.28; Core losses for the 3F35 core material

Based on the published loss curves for the possible core materials at 100C, 50 mT and 500kHz, it appears that the 3F35 material would be optimum at an estimated loss of 85 kW/m<sup>3</sup>, when the 3C96 and 3F3 core material show losses above 250 kW/m<sup>3</sup>. Before the core losses can be fully calculated, the effective volume of the core volume (m<sup>3</sup>) must be known. Choosing the actual core is more of a guessing game that ensures that the windings can fit in the allowed area for the wires, while knowing that the core increases causes a decrease in available selection.

The chosen core form factor was the Ferroxcube ETD34/17/11 because of the larger size and the increased options of core material that is available. Table 3.29 lists the available core material options for the ETD34 cores.

Table 3.29; Core properties for the ETD34/17/11 form factor

GRADE	A <sub>L</sub> (nH)	μ <sub>e</sub>	AIR GAP (μm)	TYPE NUMBER
3C90	2700 ±25%	≈ 1740	≈ 0	ETD34/17/11-3C90
3C94	2700 ±25%	≈ 1740	≈ 0	ETD34/17/11-3C94
3C95 <small>des</small>	3270 ±25%	≈ 2110	≈ 0	ETD34/17/11-3C95
3C96 <small>des</small>	2500 ±25%	≈ 1610	≈ 0	ETD34/17/11-3C96
3F3	2500 ±25%	≈ 1610	≈ 0	ETD34/17/11-3F3
3F35 <small>des</small>	1850 ±25%	≈ 1190	≈ 0	ETD34/17/11-3F35

The ETD34 datasheet provides core losses for the ETD34 core in terms of watts for various frequencies and flux density for several core materials. For the chosen 3F35 core material the core loss is <1 watts at 500kHz and 50 mT and <8 watts at 500kHz and 100 mT (Table 3.30).

Table 3.30; Core loss for the ETD ETD34/17/11 form factor for various core materials

GRADE	B (mT) at	CORE LOSS (W) at		
	H = 250 A/m; f = 25 kHz; T = 100 °C	f = 500 kHz; B = 50 mT; T = 100 °C	f = 500 kHz; B = 100 mT; T = 100 °C	f = 1 MHz; B = 30 mT; T = 100 °C
3C90	≥330	–	–	–
3C94	≥330	–	–	–
3C95	≥330	–	–	–
3C96	≥340	≤ 2.8	–	–
3F3	≥320	–	–	–
3F35	≥300	≤ 1.0	≤ 8.0	–

Surprisingly, the 3F3 core material was not listed for use at 500kHz in the ETD34/17/11 datasheet. However, the 3C96 was shown for use at 500kHz. Using the loss curves for the core materials and the effective volume for the ETD34 core form factor gives the following estimated losses at the operating temperature of 100C and flux density of 50mT and 100mT.

Table 3.31; Comparison of core material losses for the ETD34/17/11 form factor

Core Material $V_e = 7.64e-6 \text{ m}^3$	Loss at 100C 50mT	Loss at 100C 100mT
3C96	1.91 Watts	8.40 Watts
3F3	2.14 Watts	9.17 Watts
3F35	0.65 Watts	5.42 Watts

### ***High Frequency Windings***

With the transformer form factor and core material chosen, the remaining challenge is the windings. The losses associated with windings are AC-resistance, skin effect and proximity effects. Skin effect are directly related to the frequency, whereas, the frequency increases the effective area of the conductor which becomes smaller caused by the internal circulating eddy currents. As an AC current flows through a conductor, it creates a H-field that leads to circulating eddy currents that oppose the flow of the current at the center of conductor and forces the majority of the current flow to the outer surface (Figure 3.32). With that current flow forced to the outer surface, it causes the effective cross sectional area to decrease and in turn raises the current density and increased heat losses.



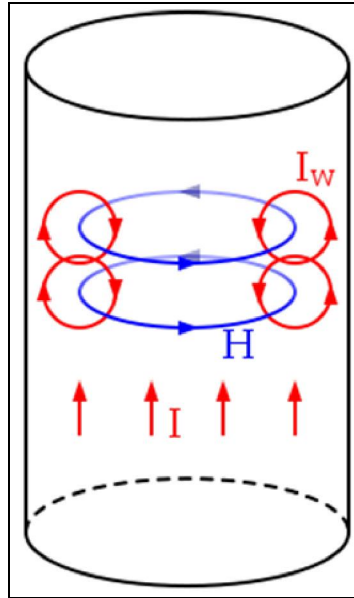


Figure 3.32; Effects of eddy currents leading to skin effect

Skin effect is a function of the permeability ( $\mu_r$ ), resistivity ( $\rho$ ) and frequency of the conductor (Equation 3.33). What is not obvious is the temperature dependence, which affects the resistivity of the material. In the case of copper wire, the resistivity at 25C is about  $1.72 \cdot 10^{-8} \Omega \cdot m$  (Ohms-meter) and increases to  $2.266 \cdot 10^{-8} \Omega \cdot m$  at 100C, which will cause the skin effect depth to change from 96.1  $\mu m$  (micro-meters) to 110.3 $\mu m$ . For all remaining calculations concerning wire resistance or skin effect, the operating temperature will be assumed to be around 100C and all conductors will be assumed to be annealed copper.

$$\delta = \frac{1}{\sqrt{\pi \cdot \mu_0}} \cdot \sqrt{\frac{\rho}{\mu_r \cdot f}}$$

Equation 3.33; Equation for skin effect

Limiting the operating temperature for all future calculations allows the skin effect equation to be simplified to the following, showing the relationship between frequency in hertz and skin depth in meters (Equation 3.34).

$$\delta_{100c\_cu}(f) := \frac{0.07576}{\sqrt{f}}$$

*Equation 3.34; Simplified skin effect equation based on application*

At 500kHz the skin depth is approximately 107 um (micro meters), which is close to the radius of a 31 AWG wire. What does this mean in terms of selecting the wire size? Skin depth limits the overall cross-sectional area of the wire as a function of frequency. At 0 Hz, the wire has a direct current (DC) resistance that is purely related to the cross-sectional area and material of the conductor. As the frequency increases the resistance of the conductor increases and is known as the alternating current (AC) resistance. In the “Fundamentals of Power Electronics” by Erikson, the recommended relationship between the DC resistance and the AC resistance is 1.33 (Equation 3.35).

$$R_{dc\_ac\_ratio} = \frac{A_{outer}}{A_{outer} - A_{inner}} = \frac{\pi \cdot r^2}{\pi \cdot r^2 - \pi \cdot \left(r - \frac{S}{2}\right)^2}$$

r is wire radius  
S is skin effect depth

*Equation 3.35; Skin effect leading ratio of DC to AC resistance*

Solving for the radius of the wire gives the relationship between skin depth and wire radius in terms of the ratio of the DC resistance to the AC resistance.

Substituting in  $R_{dc\_ac\_ratio}=1.333$  gives the optimum wire radius to be equal to the skin effect depth, which results in an overall wire diameter of 215um.

$$\begin{array}{l}
 R_{dc\_ac\_ratio} := 1.333 \\
 r := \frac{1}{2} \cdot \left( R_{dc\_ac\_ratio} + \sqrt{R_{dc\_ac\_ratio}^2 - R_{dc\_ac\_ratio}} \right) \cdot S \\
 r = 1 S
 \end{array}$$

*Equation 3.36; Ideal wire radius (r) to skin effect depth (S)*

Using the standard table for the American Wire Gauge (AWG) and the wire calculated diameter shows the nearest wire size for the optimum ratio of 1.33 to be 31 AWG.

The analysis of the ideal conductor size based on the skin effect only answers one part of the requirements for the transformer windings. Sizing of the overall conductor size is based on the required input current and output current and a current density in order to control heating of the conductor. Commonly, the current density is between 500 and 750 circular mils per amp (CM/A), or 400 A/cm<sup>2</sup> and 260 A/cm<sup>2</sup>. For this design, the target current density will be on the lighter side of 750 CM/A (260 A/cm<sup>2</sup>). The design specifications discussed earlier showed the required output current is approximately 2.5 A RMS and at 750 CM/A the total required conductor area would be 1875 CM, which is approximately an 18 AWG wire. In order to minimize the skin effect, the total conductor would have to be constructed using strands of the optimum wire size (31 AWG

= 70.56 CM), which at the required 1875 CM means that 27 parallel strands of 31 AWG would be required. Unfortunately, at higher frequencies this method of using parallel strands falls apart as the strand count increases because of the proximity effect.

Proximity effect is basically the same as skin effect, but it is caused by current flow in parallel conductors. The basic explanation for proximity effect is as the number of conductors increases from 1, the ratio of the AC resistance to DC resistance greatly increases. The plot below (Figure 3.37) shows the relationship of the skin effect AC resistance to DC resistance ratio ( $h/\delta$ ) on the independent axis to the resulting AC resistance to DC resistance ratio ( $R_{AC}/R_{DC}$ ) on the dependent axis for a different number of conductors. For 27 parallel strands, the curve is off the graph for a skin effect AC resistance to DC resistance ratio of 1.33 ( $h/\delta=1.33$ ). This implies that the proximity losses would be dominant and would greatly impact the efficiency.

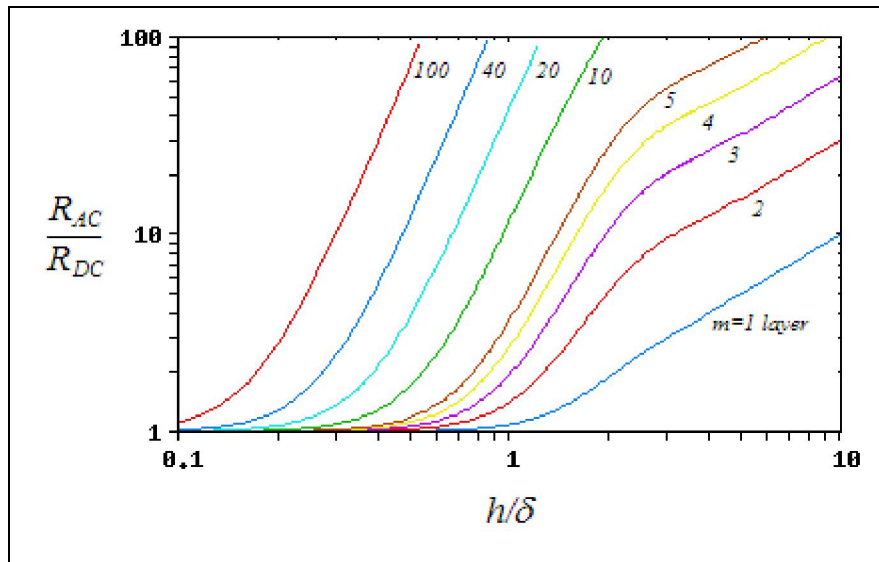


Figure 3.37; Proximity effect as a function of skin effect and number of conductors

The battle between skin effect and proximity effect has a simple solution and that is Litz wire. Litz wire is made up of multiple conductors that are insulated from each other and woven in a pattern that minimizes skin and proximity effects. Choosing the proper Litz wire is done using the manufacturers recipe based on frequency and overall current.

The selection of the Litz wire will be done using the table provided by the New England Wire Company for their brand of Litz wire. Based on the operating frequency range of 450kHz to 550kHz, the proper wire would use 44 AWG strands. In order to find the overall bundle size, the equivalent wire gauge will have to be found using the target current density and turns ratio for the transformer.

Using the ideal transformer equations (Equation 3.38) and the estimated output current of 2.5 Amps RMS, along with the turns ratio of  $N=4$ , gives the primary current of 10.0 Amps RMS.

$$\text{Turns\_Ratio} = N = \frac{V_s}{V_p} = \frac{I_p}{I_s}$$

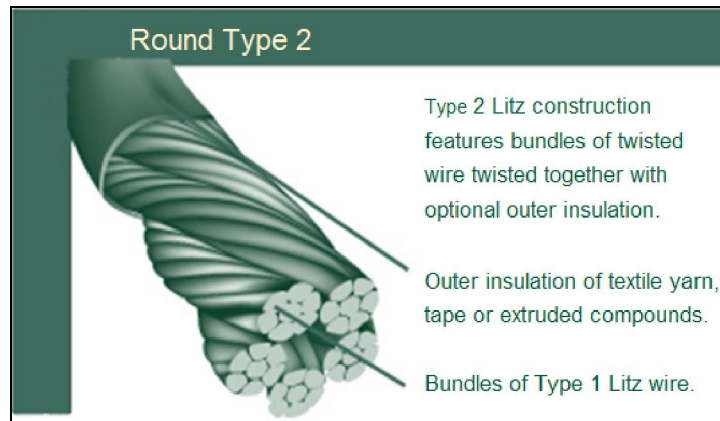
*Equation 3.38; Ideal transformer equation*

At a current density of 750 CM/A at 10.0 Amps would require a total Circular Mil area of 7500 mils, which is close to 12AWG. Along with the wire size, the DC resistance is also provided in Ohms per 1000 feet and will be needed later to calculate the winding losses.

*Table 3.39; Summary of primary and secondary current and Litz wire*

Winding	Maximum RMS current	Equivalent wire size	Litz Wire Size Outside diameter (O.D)	DC resistance Ohms per 1000 feet	New England Wire part number
Primary	10.0 Amps	12 AWG	0.120 inches (3.08 mm)	1.920	5X5X3/22/44
Secondary	2.50 Amps	18 AWG	0.058 inches (1.47 mm)	7.600	5X3/27/44

Even though Litz wire is designed to minimize the AC resistance, it doesn't fully eliminate it. There is still some AC resistance that is related to the weaving pattern and number of individual parallel strands. For the chosen Litz wire, the configuration is called a Round Type 2 (Figure 3.40) and is used to define the building process in terms of cabling and bunching operations.



*Figure 3.40; Example of Type-2 Litz wire*

A bunching operation is a set of strands that are used to make a smaller cable that is then used with other smaller cables to make the overall Litz cable. The process of bunching and cabling is used to calculate the AC to DC resistance ratio (Equation 3.41).

$$\text{Ratio}_{AC\_DC} = H + K \cdot \left( \frac{N_S \cdot D_I}{D_o} \right)^2 G$$

Equation 3.41; Litz wire AC to DC ratio

Where the input variables are:

Table 3.42; Summary of variable for Litz wire AC to DC ratio calculation

H	Is the AC to DC resistance ratio of the individual strands.
K	Is a constant based on the number of individual strands, above $N_S = 27$ K is 2
$N_S$	Number of individual strands that make up the Litz cable
$D_I$	Diameter of one individual stand
$D_o$	Overall diameter of the Litz cable
G	Is the Eddy current basis factor for one individual stand as a function of frequency

The properties for the individual strand chosen Litz cable are the same for the primary and secondary windings, which is 44AWG;  $D_I = 0.0019$  inches. The Eddy Current Bias Factor is calculated to be  $G = 2.743 \cdot 10^{-4}$  for a 44AWG wire at 500kHz based on the equation in Equation 3.43. According to the datasheet for the chosen cabling, the AC to DC resistance ratio for the individual strands of 44AWG is 1.0003 ( $H = 1.0003$ ).

$$G = \left( \frac{D_I \sqrt{F}}{10.44} \right)^4$$

*Equation 3.43; Litz wire Eddy Current Bias Factor equation*

Now all that remains to affect the AC to DC resistance ration of the Litz cable is the cabling properties K, N<sub>s</sub>, and D<sub>o</sub>. K is the simplest and is related to the number of parallel strands, and for any amount over 27 K is fixed at 2 (K=2).

*Table 3.44; Summary of winding resistance using Litz wire*

Winding	New England Wire part number	Litz Wire Size Outside diameter (D <sub>o</sub> )	Number of strands (N <sub>s</sub> )	DC resistance Ohms per 1000 feet	AC to DC ratio
Primary	5X5X3/22/44	0.120 inches (3.08 mm)	1650	1.920	1.375
Secondary	5X3/27/44	0.058 inches (1.47 mm)	405	7.600	1.097

Before the actual winding resistance can be calculated, the total winding length must be known. This is a function of the core winding area and the number of turns for each winding. The Ferroxcube datasheet for the ETD34/17/11 form factor list is the average turn length to be 60mm (2.36 inches) per turn. This will be used later along with the number of turns of each winding to calculate the resistance of each winding.



## ***Transformer Windings***

Defining the primary turns is based on the desired input inductance, and in this case, the target is between 1uH and 3uH, with the ideal target being closer to the 3uH. When using commercially available cores, the manufacturer will provide a normalized inductance (AL) for the core geometry, core material and core gap (if any), and typically is in nano-Henries per turns squared (nH/N<sup>2</sup>). The normalized inductance factor makes calculation of the inductance much simpler by replacing the core properties with a simple constant.

$$AL = \frac{L}{N^2}$$

*Equation 3.45; Normalized inductance equation*

$$N = \sqrt{\frac{L}{AL}} \quad \text{or} \quad L = N^2 \cdot AL$$

*Equation 3.46; Variations of normalized inductance equation*

For the Ferroxcube 3F35 ETD34/17/11 core, the ungapped AL is 1850nH ±25%, which yields 1.85uH for 1 turn or 7.4uH for 2 turns (Figure 3.47).

$$\begin{aligned} 1^2 \cdot 1850 &= 1.85 \times 10^3 \text{ nH} \\ 2^2 \cdot 1850 &= 7.4 \times 10^3 \text{ nH} \end{aligned}$$

*Figure 3.47; Inductance for 1-turn and 2-turns on the ETD34/17/11 core*

As shown earlier, the magnetization inductance limits the efficiency at lighter loads because of the parallel inductive reactance with the reflected output impedance. So why not use the 2-turns for the higher inductive reactance and gain the upper-end efficiency? The simple answer is there is a balancing act or trade-off between the frequency shift dependence on load and the series inductor size that boils down to a relationship between the magnetization inductance and the series inductor inductance. This will be covered more later on in more detail. For now, the important thing is to understand that the primary turns are  $T_{pri}=1$ .

At this point, the design of the transformer is completed with the core material, form factor, primary winding, secondary winding, primary inductance and secondary inductance. These are all defined, along with a turn ratio, as summarized in the Table 3.48.

*Table 3.48; Summary of transformer windings*

Core material	Ferroxcube 3F35
Form factor	Ferroxcube ETD34/17/11
Primary wire	Litz 5X5X3/22/44
Secondary wire	Litz 5X3/27/44
Turns Ratio	$N = 4$
Primary Turns	$T_{pri} = 1$
Secondary Turns	$T_{sec} = 4$
Primary Inductance	$L_{pri} = 1.85 \mu\text{H} \pm 25\%$
Secondary Inductance	$L_{sec} = 29.6 \mu\text{H} \pm 25\%$
Primary AC resistance	2.279 mOhms
Secondary AC resistance	12.112 mOhms

The winding resistance can now be found using the number of turns and the published average turn length from the Ferroxcube ETD34/17/11 datasheet. This application is using a flying lead connection to the transformer instead of the pins provided on the Ferroxcube form factor/bobbin. This will require up to an additional 8.0 inches of length for each winding. Using the overall winding lengths, the published DC resistance for the chosen Litz cable and the calculated AC to DC resistance ratio for the list wire completes the last of the transformer design (Table 3.48 and Table 3.49).

*Figure 3.49; Summary of transformer winding properties*

Primary Turns	$T_{pri} = 1$
Primary Length	$2.36 + 8.0 = 10.36$ inches
Secondary Turns	$T_{sec} = 4$
Secondary Length	$4 * 2.36 + 8.0 = 17.44$ inches
Primary DC resistance	1.658 mOhms
Primary AC-DC resistance ratio	1.375
Primary AC resistance	2.279 mOhms
Secondary DC resistance	11.043 mOhms
Secondary AC-DC resistance ratio	1.097
Secondary AC resistance	12.112 mOhms

## ***Series Inductor Design***

By using the same process that was used for the transformer, and the same Ferroxcube ETD34/17/11 form factor and 3F35 cores, makes designing the series inductor simple and quick. The only missing part is what the final inductance needs to be calculated. As mentioned earlier, the relationship of the resonant frequency and the variation is caused by the change in output load (Equation 3.50).

$$f_{o\_open\_load} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (L_1 + L_{mag})}}$$

$$f_{o\_full\_load} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot L_1}}$$

*Equation 3.50; Resonant frequency at full load and no load*

To limit the range of resonant frequency, the series inductor ( $L_1$ ) could be made by a multiple of the magnetization inductance ( $L_{mag}$ ) (Equation 3.51).

$$\text{Let } L_1 = X \cdot L_{mag}$$

$$f_{o\_open\_load} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (X \cdot L_{mag} + L_{mag})}} \quad f_{o\_full\_load} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (X \cdot L_{mag})}}$$

$$f_{o\_open\_load} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot L_{mag} \cdot (X + 1)}}$$

*Equation 3.51; Defining the series inductor ( $L_1$ ) as a multiple of the magnetization inductance ( $L_{mag}$ )*

Taking this approach to limit the change in the resonant frequency provides a relationship in change from no load to full load in terms of percentage of change (Equation 3.52).

$$\Delta\%f_o = 100 \cdot \frac{f_{o\_full\_load} - f_{o\_open\_load}}{f_{o\_open\_load}}$$

*Equation 3.52; Percentage of frequency shift from no load to full load*

This simplifies to Equation 3.53.

$$\Delta\%f_o = 100 \cdot \frac{\sqrt{(X+1)} - \sqrt{X}}{\sqrt{X}}$$

*Equation 3.53; Simplified percentage of frequency shift based on no and full load*

As a comparison, the table below shows different percentages of change for different multiplication factors for the magnetization inductance (X) (Table 3.54). The multiplication factor (X) is limited by the specified maximum frequency change defined in the work done in the first chapter to define the design targets, which was the variation in frequency from 472kHz is  $\pm 23$ kHz or  $\pm 4.9\%$  (9.8%).

*Table 3.54; Percentage of frequency shift verses inductance multiplier*

X	% Change in Frequency
1	41.4%
2	22.5%
3	15.5%
4	11.8%
5	9.5%
6	8.0%
7	6.9%

Based on the design target of 472kHz  $\pm$ 4.9%, means that total frequency range is 449kHz to 495kHz at most. This falls in the multiplication factor of X=4 and for additional margin the actual multiplication factor should increase to X=5. Using a multiplication factor of X=5 gives the frequency range of 450.3kHz to 493.7kHz, which is well within the design target limits. This means that the series inductance is 5-times the magnetizing inductance or 9.25uH  $\pm$ 25%.

The series inductor has the same current flow as the primary side of the transformer and uses the same Ferroxcube form factor and core. This similarity allows the same method used for the primary side of the transformer inductance and turns using the ungapped  $AL=1850 \text{ nH/N}^2$ , which resulted in fractional number of turns (Figure 3.55). Fractional number of turns is not practical and must be rounded to a whole number, which causes a shift in the final inductance leading to either an inductance that is too low or higher than desired (Equation 3.55).

$$\begin{aligned}
L_{\text{desired}} &:= 9250 \text{ nH} \\
AL &:= 1850 \text{ nH/N}^2 \\
N &:= \sqrt{\frac{L_{\text{desired}}}{AL}} & N = 2.236 \\
L(N) &:= N^2 \cdot AL \\
L(2) &= 7.4 \times 10^3 \text{ nH} \\
L(3) &= 1.665 \times 10^4 \text{ nH}
\end{aligned}$$

Equation 3.55; Calculating the inductance based on the inductance factor (AL)

Comparing the possible inductance values for the series inductor shows that a turns N=2 would just barely produce enough inductance to meet the frequency range specification of 472kHz  $\pm$ 5.9%, leaving no head room for variations in component values. On the latter side, using a turns N=3 would result in a much smaller frequency variation than required, which would be about 9 times the transformer magnetization inductance.

Table 3.56; Summary of the final series inductor ( $L_1$ )

Core material	Ferroxcube 3F35
Form factor	Ferroxcube ETD34/17/11
Winding wire	Litz 5X3/27/44
Inductance	16.65uH
Turns	T <sub>pri</sub> = 3
Wire Length	7.1 + 8.0 = 15.1 inches
DC resistance	2.414 mOhms
AC-DC resistance ratio	1.375
AC resistance	3.318 mOhms

Using a much higher inductance than needed narrows the frequency variation to about 5.5% ( $\pm$ 2.71%), which is 472kHz  $\pm$ 2.71%, 459.2kHz to 484.8kHz (Equation 3.57).

$$\begin{aligned}
 X &= 9 \\
 \Delta\%f_o(X) &:= 100 \cdot \frac{\sqrt{(X+1)} - \sqrt{X}}{\sqrt{X}} \\
 \Delta\%f_o(X) &= 5.409 \quad \% \\
 P &:= \frac{\Delta\%f_o(X)}{2} \\
 P &= 2.705 \quad \% \\
 472 \cdot \left(1 - \frac{P}{100}\right) &= 459.234 \quad \text{kHz} \\
 472 \cdot \left(1 + \frac{P}{100}\right) &= 484.766 \quad \text{kHz}
 \end{aligned}$$

*Equation 3.57; Upper and lower frequency limits based on no and full load*

### ***Capacitor Selection***

With all the inductance and winding resistance known, the only remaining part of the resonant circuits is the capacitance ( $C_1$ ). Selection of the capacitor is important to maintain frequency stability as well as efficiency. All capacitors have a resistive loss element called equivalent series resistance (ESR) and another not so straightforward variation is the capacitance with voltage and temperature. All these variations are related to the physical construction and dielectric properties of the capacitors.

The ideal dielectric that produces the most stability is mica or glass plate capacitors, which unfortunately the size in terms of capacitance per volume and cost are both a major disadvantage. The next choice is the ceramic capacitors, which are readily available and also available in several types of dielectrics. The choice of dielectric type comes down to



performance and cost. The types of dielectric material are given in classes 1 to 4 based on EIA standards, where class-1 is most stable and class-4 is the least desirable but ultra-low cost.

Only two of the classes will be considered for use in this application; Class-1 NP0/C0G material and Class-2 X7R materials. The main tradeoff between the two types of dielectric material is the capacitance per volume, and typically the X7R material allows more capacitance for the same volume than the NP0/C0G material, and is typically 10-15 times more capacitance per volume.

As a capacitor operates close to the maximum rated voltage, there are changes in the dielectric material that could lead to variation in the capacitance. Typically the capacitance value of a X7R capacitor decreases to 70-80% of the original value. At this great of a change, it would be nearly impossible to maintain stable operation, while the NP0/C0G dielectric material remains highly stable and shows little change in capacitance. Table 3.58 below was taken from a manufacturers application note on capacitor selection showing bias voltage effects on capacitance.

*Table 3.58; Percentage of capacitance change verses bias voltage*

Capacitance of Ceramic Capacitors at 10%, 50% and 100% of Rated Voltage (DC), "Typical"			
Dielectric:	C0G	X7R	Z5U
%C at 10%:	100%	105%	120%
%C at 50%:	100%	95%	50%
%C at 100%	100%	70%	30%

Thermal stability across temperature is another important criterion. Comparing the two dielectric materials, it is clear based on the datasheets that the NP0/C0G material is relatively flat from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; whereas, the capacitance of the X7R decreases as the temperature increases. This could lead to additional frequency instability that could shift with the operating temperature, as well as, the additional error self-heating of the capacitor due to the current and the ESR.

A simple solution for achieving stable operation is to choose the better dielectric material such as a C0G or NP0 type, and use high voltage rated capacitors to minimize voltage stress on the dielectric material.

Managing the loss element of the capacitor, also known as the equivalent series resistance (ESR), is also a function of the operating frequency and capacitance. Manufacturers of capacitors provide the loss parameter in either a dissipation factor (DF) or tan-delta ( $\tan \delta$ ), which both represents the angle between the ESR and reactance of the capacitor (Equation 3.59).

$$\text{DF} = \tan \delta = \frac{\text{ESR}}{|X_C|}$$

*Equation 3.59; Dissipation Factor (DF) relationship to ESR and reactance of a capacitor*

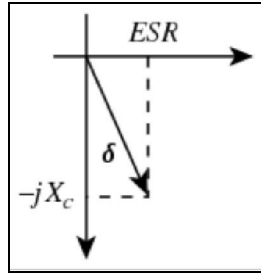


Figure 3.60; Phase form of Dissipation Factor (DF)

The ESR is calculated off the Dissipation Factor (DF) and the reactance of capacitor (Equation 3.61).

$$ESR = DF \cdot |X_C| = \frac{DF}{2 \cdot \pi \cdot f_{sw} \cdot C}$$

Equation 3.61; calculation of ESR based on Dissipation Factor (DF) and reactance

An interesting relationship of quality of the capacitor and ESR is the quality factor (Q), which increases as the ESR decreases. It is rare, but sometimes a manufacturer of RF capacitors will also list the Q-factor of the capacitor in place of the Dissipation Factor or the tan-delta. The Q-factor is the inverse of the Dissipation Factor (Equation 3.62).

$$Q = \frac{1}{DF} = \frac{1}{\tan \delta} = \frac{|X_C|}{ESR}$$

Equation 3.62; Quality factor (Q) and Dissipation Factor (DF) relationship

With all this concern around the ESR, it is important to realize that the NP0/C0G typically has 1/10th the Dissipation Factor of the X7R capacitors. And, to really minimize the overall losses due to the capacitance is to focus on lowering the ESR by selected capacitors that lower ESR.

Calculating the required total capacitance is easily done using the idea resonant equation, the known inductance, and solving for the capacitance ( $C_1$ ). The total inductance is the sum of the series inductance (16.65uH) and magnetization inductance of the primary winding (1.85uH) along with the unloaded frequency (459.234kHz) (Equation 3.63) and 3.64).

$$f_{o\_open\_load} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (L_1 + L_{mag})}} \quad \text{becomes} \quad C_1 = \frac{1}{(L_1 + L_{mag}) \cdot (2 \cdot \pi \cdot f_{o\_open\_load})^2}$$

*Equation 3.63; Resonance capacitance formula*

$$C_1 = \frac{1}{(16.65\text{u} + 1.85\text{u}) \cdot (2 \cdot \pi \cdot 459.234\text{k})^2}$$

$$C_1 = 6492 \text{ pF}$$

*Equation 3.64; Final capacitance value*

As mentioned in the early part of this chapter, the total capacitance is split between two capacitors  $C_{1a}$  and  $C_{1b}$ , and the total parallel capacitance becomes  $C_1$ . This means that each capacitor must be half of the calculated capacitance of  $C_1$ , which means that each capacitor needs to be 3246pF. Selecting capacitors of the ultra-stable type NP0/C0G type for a lower Dissipation Factor (DF), and in turn a lower ESR. NP0/C0G capacitors typically have a tolerance of  $\pm 10\%$  and a Dissipation Factor of 0.1% ( $Q=1000$ ). For comparisons, the table below shows the total number of required capacitors and total ESR if 220pF, 470pF and 1000pF capacitors are used at 472kHz (Table 3.61).

*Table 3.65; Reactance and ESR for various capacitor values*

Capacitance	220pF	470pF	1000pF
Reactance	1533 $\Omega$	717 $\Omega$	337 $\Omega$
ESR	1.53 $\Omega$	0.72 $\Omega$	0.34 $\Omega$

*Table 3.66; Total reactance and ESR for the target capacitance value*

Capacitance	Total Capacitors Required	Total Reactance ( $X_C$ in $\Omega$ )	ESR ( $\Omega$ )
220pF	30	51.1 $\Omega$	51 m $\Omega$
470pF	14	51.2 $\Omega$	51 m $\Omega$
1000pF	7	48.1 $\Omega$	48 m $\Omega$

As seen by the quick comparison, the choice of capacitance does not have a significant effect on the total reactance or ESR (Table 3.66). However, the ESR of each individual capacitor leads to self-heating at higher RMS currents; in this case, the primary current is 10.0A. The table below summarizes the ESR, current and power dissipation for each type capacitance for a NP0/COG (Table 3.67).

*Table 3.67; Power losses per capacitor*

Capacitance	220pF	470pF	1000pF
ESR	1.53 $\Omega$	0.72 $\Omega$	0.34 $\Omega$
Current	0.333 A	0.714 A	1.43 A
Power	0.170 W	0.364 W	0.729W

## Power Devices

The power switches used to generate the square-wave for the input to the resonant stage are power MOSFETs. Power MOSFETs have two loss elements: conduction losses, also known as the  $I^2R$ , and the switching losses. At higher frequencies, switching losses become dominant and can easily exceed the conduction losses. When the resonant stage is operating at resonance, the current will be near 0 Amps at the time the power switches change states, which is Zero Current Switching (ZCS). Operating in zero current switching greatly reduces the switching loss. For this reason, they can be excluded from the analysis as long as the resonant stage is operating at resonance. Taking this into consideration for the loss model, only the conduction losses will be used, and the MOSFET on-resistance ( $R_{ds\_on}$ ) will be assumed to be no worse than 15mOhm each when operating at maximum power and temperature.

## Finalizing the Loss Model

Putting all of this together with realistic values for the capacitance, along with its ESR, forms the loss model for the resonant stage that will be used to calculate the overall estimated efficiency (Figure 3.68).

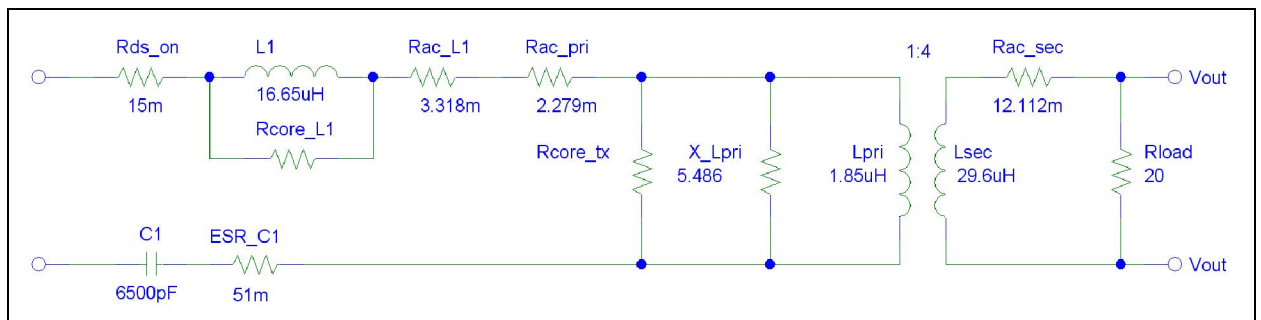


Figure 3.68; Final model for the resonance stage

Notice the resistors representing the core losses have no values. This is because the core losses cannot be simply represented as a fixed resistance, but more a variable resistance that is a function of the flux density. Manufacturers of the ferrite cores provide either curve fitting constants and equations or loss charts that relate the flux density to estimate the core loss. The manufacturer of the selected cores is Ferroxcube, and they only provide a loss chart, as seen in Figure 3.69 below, that gives the core loss in watts per volume ( $\text{kW/m}^3$ ) versus the peak flux density ( $B_{pk}$ ).

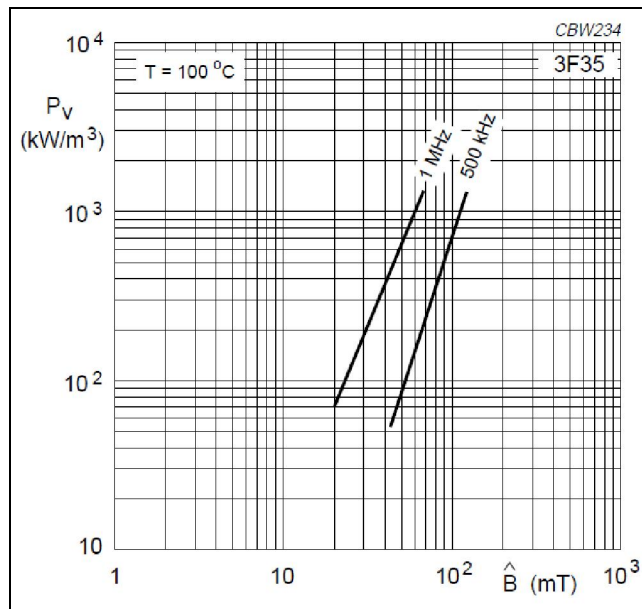


Figure 3.69; Core power loss chart

The equation below (Equation 3.70) shows the relationship between the peak flux density in Tesla ( $B_{pk}$ ) to the applied RMS voltage ( $E_{RMS}$ ), frequency in Hz ( $f$ ), turns ( $N$ ), and the effective area of the core in  $\text{cm}^2$  ( $A_e$ ). Everything is known except for the input RMS voltage ( $E_{RMS}$ ), which in this application is a DC voltage that is controlled from the input Buck regulator.

$$B_{pk} = \frac{E_{RMS} \cdot 10^4}{4.44 \cdot A_e \cdot N \cdot f}$$

*Equation 3.70; Formula for finding the peak flux density*

Based on the core manufacturers datasheet, the effective area of the core ( $A_e$ ) is  $97.1 \text{ mm}^2$  ( $0.971 \text{ cm}^2$ ). Assuming the frequency change is relatively small and is centered on  $472\text{kHz}$ , allows the frequency variable to be fixed at one value that does not change with load. The primary turns were found earlier, and to be ( $N=1$ ). Applying all the known to the flux density equation simplifies it down to only one unknown and a constant (Equation 3.71).

$$B_{pk} = E_{RMS} \cdot 0.004914$$

*Equation 3.71; Simplified equation for finding the peak flux density*

The input RMS voltage ( $E_{RMS}$ ) to the transformer is a DC voltage ( $V_{BUS}$ ), which is a function of the output load. Table 1.4 in the first chapter lists the relationship between the output voltage and load resistance and is copied below for updating. The input voltage ( $V_{BUS}$ ) to the transformer will be calculated for Table 3.73 and the Fourier transformation equation along with the known turns ratio ( $N=4$ ) (Equation 3.72).

$$V_{bus} = \frac{V_{out\_pk\_pk}}{2} \cdot \frac{\pi}{4} \cdot \frac{1}{N}$$

*Equation 3.72; DC bus voltage to output voltage*



*Table 3.73; Summary of the transformer core losses as a function of output load*

<b>Load (Ω)</b>	<b>Power (Watts)</b>	<b>Output Voltage (V peak-peak)</b>	<b>V<sub>BUS</sub> (V DC)</b>	<b>B<sub>pk</sub> (mT)</b>	<b>P<sub>core</sub> (kW/m<sup>3</sup>)</b>	<b>P<sub>core</sub> (Watts)</b>
20	112.0	133.8	9.30	46	80	0.611
50	75.0	173.2	17.00	84	400	3.06
100	48.0	196.0	19.24	95	600	4.58
200	26.0	204.0	20.03	98	650	4.97
500	13.0	228.0	22.38	110	6000	45.8

The core loss can be estimated for each load condition using the manufacturers chart (Figure 3.69) that gives the volume power loss (kW/m<sup>3</sup>) with respect to the peak flux density (mT) and the manufacturer effective core volume of 7640 mm<sup>3</sup> (7.64 x 10<sup>-6</sup> m<sup>3</sup>). Based on the estimations, core loss is more significant at lighter loads since the input voltage is high, so at the maximum output load of 112W, the core loss in the transformer is only 611mW. This value will be used in place of the resistors, representing the transformer core loss.

Finding the core loss of the series inductor is a bit more difficult, since the applied voltage is not as straightforward. Looking at the loss model, the only way to find the core loss is to use the series current through the inductor to find the flux in terms webers (Wb) in conjunction to the effective core area to find the flux density (Wb/m<sup>2</sup>). The primary current can be estimated based on the output power and input DC voltage required to produce that power (Equation 3.74).

$$I_{pri} = \frac{P_{out}}{V_{bus}}$$

*Equation 3.74; Transformer primary current as a function of output power and DC bus voltage*

$$B_{pk} = \frac{\phi}{A} = \frac{I \cdot L}{N \cdot A} \quad \begin{array}{l} A \text{ is in m}^2 \\ B \text{ is in Tesla} \end{array}$$

Equation 3.75; Peak flux density as a function of current, inductance, turns and core area

Table 3.76; Summary of the series inductor core losses as a function of output load

Load (Ω)	Power (Watts)	V <sub>BUS</sub> (V DC)	I <sub>pri</sub> (A RMS)	B <sub>pk</sub> (mT)	P <sub>core</sub> (Watts)
20	112.0	9.30	12.04	688	54.7
50	75.0	17.00	4.41	252	18.1
100	48.0	19.24	2.50	143	8.89
200	26.0	20.03	1.30	74	3.08
500	13.0	22.38	0.58	33	0.076

Using the same approach for the series inductor core loss and a turns of N=3 at maximum output power, yields a core loss of 54.7 watts (Table 3.76), which is not acceptable.

**Optimizing the Series Inductor Losses**

A common trick to managing the core loss is to limit the peak AC swings in the core by gapping. Gapping a core basically places two reluctances in series (Figure 3.78); one representing the core and the other the gap. This will reduce the amount of flux density (B-field) in the core for the same given Magnetic field intensity (H-field). This also effectively increases the amount of current that it takes to saturate the core and lower the amount of flux swing in the core lowering the hysteresis losses in the core material. As seen in the diagram below (Figure 3.77), the gapping of the core reduces the H-field to B-field gains and flattens the B-H curve with an increase of gap length.

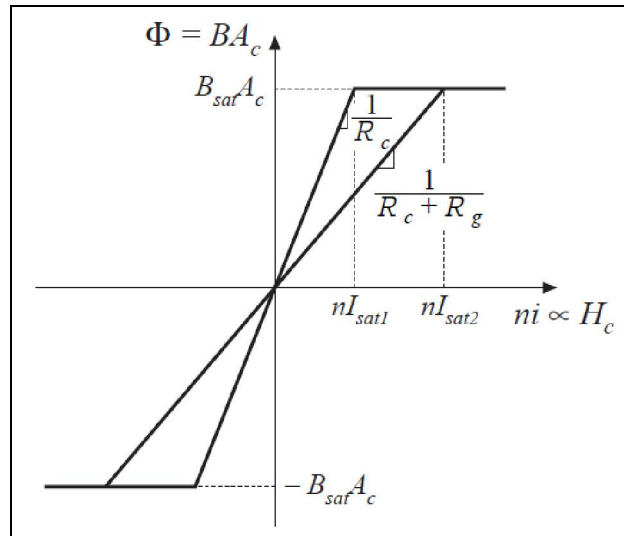


Figure 3.77; Effects of gapping core on core flux density

Ferrite cores are available already gapped from the manufacturer. However, at a low volume, the pricing per core set is not feasible. A common trick used to gap a core set is to use a nonconductive spacer, such as Kapton tape, Mylar or even paper, to produce a small gap. This method allows the adjustment of the core gap without ordering newer cores and saves time in the development and testing.

Modeling the gap is simply done using the reluctance model and the magnetomotive force in terms of amp-turns ( $n \cdot i$ ). Each portion of the magnetic circuit can be modeled as resistors and the magnetomotive force as a supply.

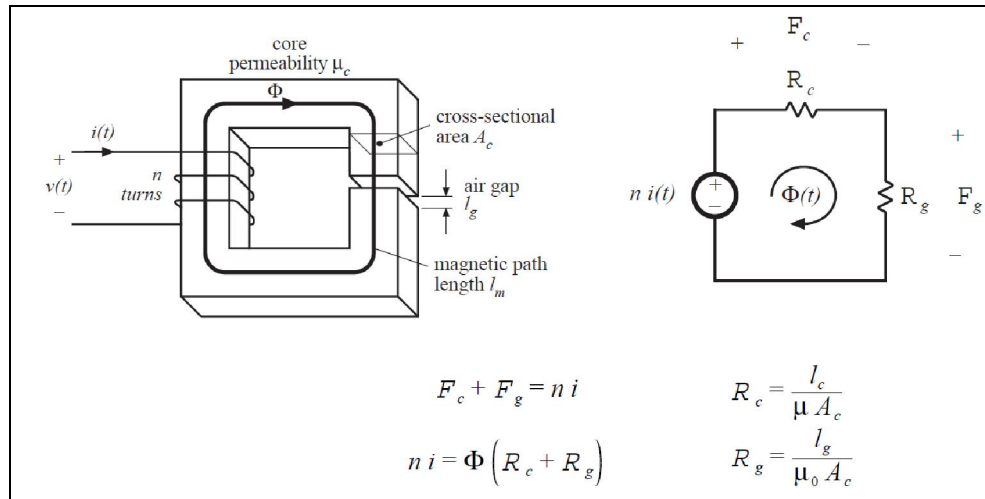


Figure 3.78; Reluctance mode for a gapped core

Finding the reluctance of the core and air gap is done using the core effective area ( $A_e$ ) and effective magnetic path length ( $l_e$ ) that is provided on the datasheet for the core (Equation 3.79).

$$L = \frac{n^2}{R}$$

$$R_{\text{core}} = \frac{l_e}{A_e \cdot \mu_r \cdot \mu_0} \quad R_{\text{gap}} = \frac{l_g}{A_e \cdot \mu_0}$$

$$L = \frac{n^2}{R_{\text{core}} + R_{\text{gap}}}$$

Equation 3.79; Core and gap reluctance calculations

The Magnetomotive force of the core ( $F_{\text{core}}$ ) is calculated using the reluctances for the core and air gap along with the turns and current (Equation 3.80).

$$F_{\text{core}} = n \cdot i \cdot \frac{R_{\text{core}}}{R_{\text{core}} + R_{\text{gap}}}$$

Equation 3.80; Magnetomotive force of the core based on reluctance

Knowing the magnetomotive force of the core leads to the flux density of the core that will be used to find the core losses.

$$B_{\text{core}} = \frac{F_{\text{core}}}{R_{\text{core}} \cdot A_e}$$

*Equation 3.81; Flux density of core*

Tying all of this together leads to the complete equations for the core flux density and the inductance in terms of the core properties and air gap (Equation 3.82).

$$B_{\text{core}} := n_{L1} \cdot I_{\text{pri}} \cdot \mu_r \cdot \mu_o \cdot \frac{1}{(l_{e\_m} + l_{g\_m} \cdot \mu_r)}$$

$$L := n_{L1}^2 \cdot A_{e\_m} \cdot \mu_r \cdot \mu_o \cdot \frac{1}{(l_{e\_m} + l_{g\_m} \cdot \mu_r)}$$

*Equation 3.82; The complete equations for core flux density and inductance based on core properties*

Selecting a suitable gap width is a tradeoff between inductance and core flux density. Earlier it was determined that the minimum allowed inductance of the series inductor was 9.25uH. Setting the inductance equation above to the minimum desired inductance and solving for the turns ( $n_{L1}$ ) and substitution the turns ( $n_{L1}$ ) into the flux density equation allows the required turns ( $n_{L1}$ ) (Equation 3.83) and the flux density in the core ( $B_{\text{core}}$ ) (Equation 3.84) to be plotted with respect to the gap ( $l_{\text{gap}}$ ) (Figure 3.85 and 3.86).

$$n_{L1}(L_{\text{gap}}) := \sqrt{\frac{L_{\text{desired}} \cdot (l_{e\_m} + L_{\text{gap}} \cdot \mu_r)}{(A_{e\_m} \cdot \mu_r \cdot \mu_o)}}$$

Equation 3.83; Turns required based on core properties, air gap and desired inductance

$$B_{\text{core}}(L_{\text{gap}}) := \sqrt{\frac{L_{\text{desired}} \cdot (l_{e\_m} + L_{\text{gap}} \cdot \mu_r)}{(A_{e\_m} \cdot \mu_r \cdot \mu_o)}} \cdot I_{\text{pri}} \cdot \mu_r \cdot \mu_o \cdot \frac{1}{(l_{e\_m} + L_{\text{gap}} \cdot \mu_r)}$$

Equation 3.84; Core flux density as a function of all input variables

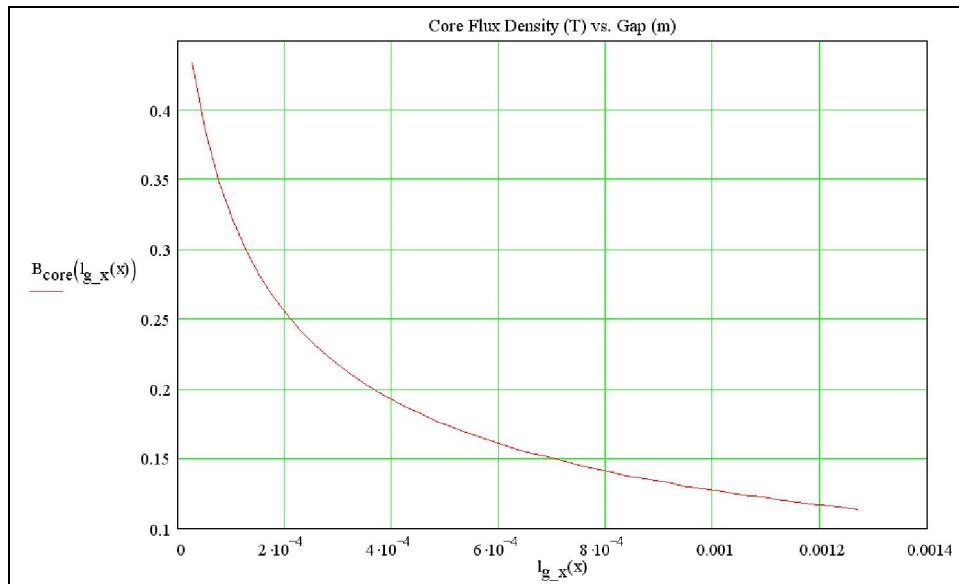


Figure 3.85; Plot of core flux density verses core gap

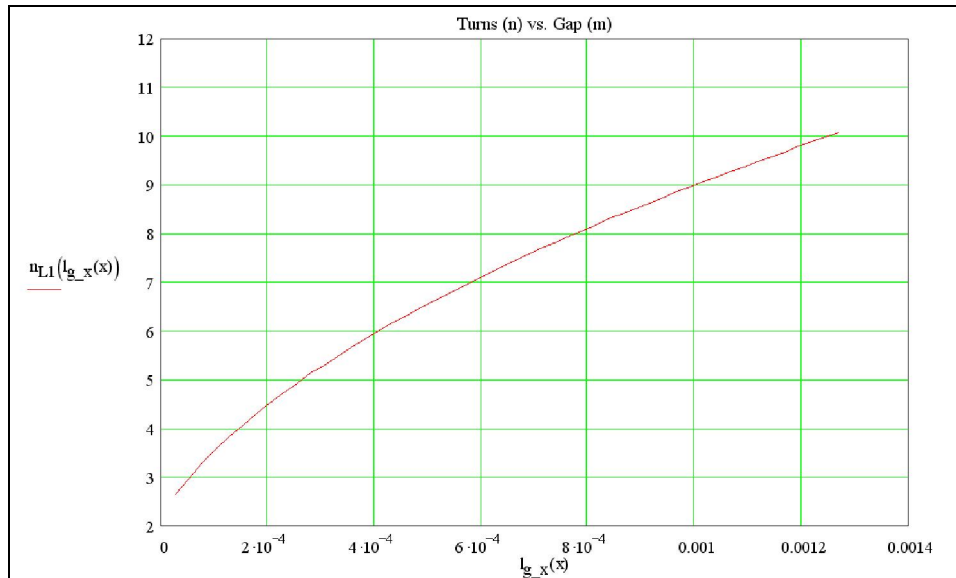


Figure 3.86; Plot of turns versed core gap

Based on the plots (Figures 3.85 and 3.86), 10 turns and a total gap of 1.26mm would be a good compromise and will be used. The actual gap is half that of the total gap because the core is an E-core meaning that the gap is shared with the internal leg as well with the outers. However, if the core were to be ground instead of shimmed, the total gap would be in the center leg. At 10 turns, the core flux density is lowered from 688mT to 114mT, and the core losses from 54.7 watts to 6.45 watts (Table 3.87). The downside is that the increased turns will result in higher winding losses. The changes are shown below (Table 3.88) and will be used to update the loss model (Figure 3.91).

Table 3.87; Revised summary of the series inductor core losses as a function of load

Load ( $\Omega$ )	Power (Watts)	$V_{BUS}$ (V DC)	$I_{pri}$ (A RMS)	$B_{pk}$ (mT)	$P_{core}$ (Watts)
20	112.0	9.30	12.04	114	6.45
50	75.0	17.00	4.41	42	0.39
100	48.0	19.24	2.50	24	<0.39
200	26.0	20.03	1.30	12	<0.39
500	13.0	22.38	0.58	5	<0.39

Table 3.88; Revised series inductor properties

Core material	Ferroxcube 3F35
Form factor	Ferroxcube ETD34/17/11
Winding wire	Litz 5X5X3/22/44
Inductance	9.25uH
Turns	T <sub>pri</sub> = 10
Gap total	1.26mm (0.0496 inches)
Gap shimmed	0.63mm (0.0248 inches)
Wire Length	7.1 + 8.0 = 15.1 inches
DC resistance	5.06 mOhms
AC-DC resistance ratio	1.375
AC resistance	6.955 mOhms

### Revising the Loss Model

The change in inductance impacts a few things; span of frequency change with load, the capacitance value and the total ESR of the capacitor (C<sub>1</sub>). Based on the no-load operation frequency, the new series capacitor (C<sub>1</sub>) value is 11.294nF (Equation 3.89), and if made up using parallel 470pF capacitors, a total of 24 will be needed resulting in a total ESR of 30mOhm.

Ratio of magnetization inductance to series inductance (L1)	$X := \frac{9.25 \text{ uH}}{1.85 \text{ uH}}$	
		$X = 5$
	$\Delta\%f_o(X) := 100 \cdot \frac{\sqrt{(X+1)} - \sqrt{X}}{\sqrt{X}}$	$\Delta\%f_o(X) = 9.545 \%$
	$P := \frac{\Delta\%f_o(X)}{2}$	$P = 4.772 \%$
	No Load Frequency	$472 \cdot \left(1 - \frac{P}{100}\right) = 449.475 \text{ kHz}$
	Full Load Frequency	$472 \cdot \left(1 + \frac{P}{100}\right) = 494.525 \text{ kHz}$

Equation 3.89; Revised percentage of frequency shift from no to full load



$$C_1 = \frac{1}{(9.25\mu + 1.85\mu) \cdot (2 \cdot \pi \cdot 449.5\text{k})^2}$$

$$C_1 = 11294 \text{ pF}$$

Equation 3.90; Revised capacitance value

This completes the loss model (Figure 3.91), and now can be used to calculate the estimated efficiency of the RF resonance stage. Combining the resistances greatly simplifies the model. The updated simplified model is reduced to one AC resistance ( $R_{ac}$ ), series inductor ( $L_1$ ), series capacitor ( $C_1$ ), and the reflected secondary side of the transformer.

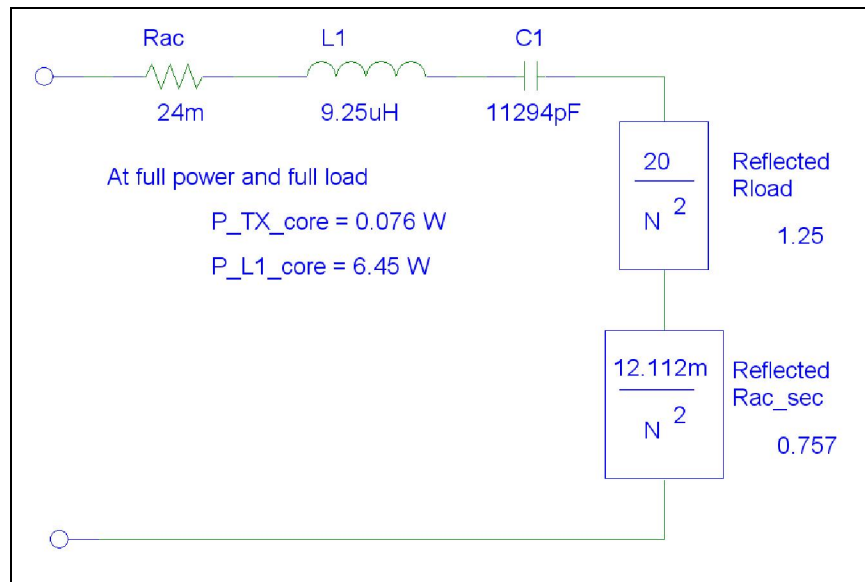


Figure 3.91; Revised loss model

The earlier analysis showed at resonance the reactive terms cancel out leaving just the resistive elements and yields the resistive model (Figure 3.92).

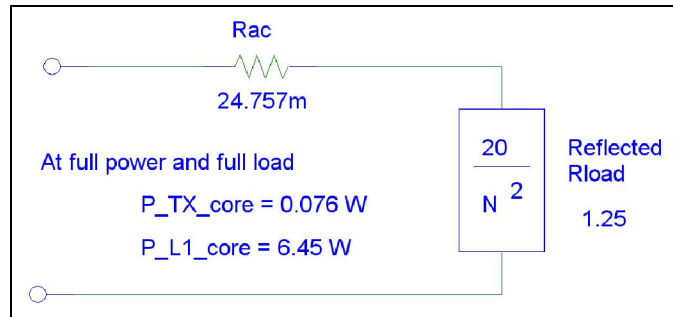


Figure 3.92; Real losses as resonance

### Overall Estimation in Efficiency

The revised overall efficiency could be as high as 92.794% (Equation 3.94) based on the revised loss models operating at resonance (Figure 3.92).

if the primary current is $I_{pri} := 9.5$ Amps RMS	
$P_{in} := I_{pri}^2 \cdot (R_{ac} + R_{Load}) + P_{TX\_core} + P_{L1\_core}$	$P_{in} = 121.573$ Watts
$P_{out} := I_{pri}^2 \cdot R_{Load}$	$P_{out} = 112.813$ Watts

Equation 3.93; Resonance circuit maximum input and output power

$\eta_{RF} := 100 \cdot \frac{P_{out}}{P_{in}}$	$\eta_{RF} = 92.794 \%$
---	-------------------------

Equation 3.94; Estimated efficiency of resonance stage

Based on the analysis of the resonance, RF stage should be able to achieve about 92% efficiency at full load as long as the stage is operating at the resonance point (Equation 3.94). The overall system efficiency must include the efficiency of the input power stage,

which was chosen to be a Synchronous rectification buck converter in Chapter 2. If the efficiency of the buck converter stage is at least 90% efficiency, it should result in a total system efficiency greater than the targeted 80%, and as high as 83.5% (Equation 3.95).

$$\begin{aligned} \eta_{RF} &= 92.794 \% \\ \eta_{DC} &:= 90 \% \\ \eta_{total} &= \eta_{RF} \cdot \eta_{DC} \\ \eta_{total} &= 83.515 \% \end{aligned}$$

Equation 3.95; Estimation of the overall system efficiency

### Auxiliary System Control

At this point in the design and analysis process, the input power source has been defined and the RF stage designed (Figure 3.96).

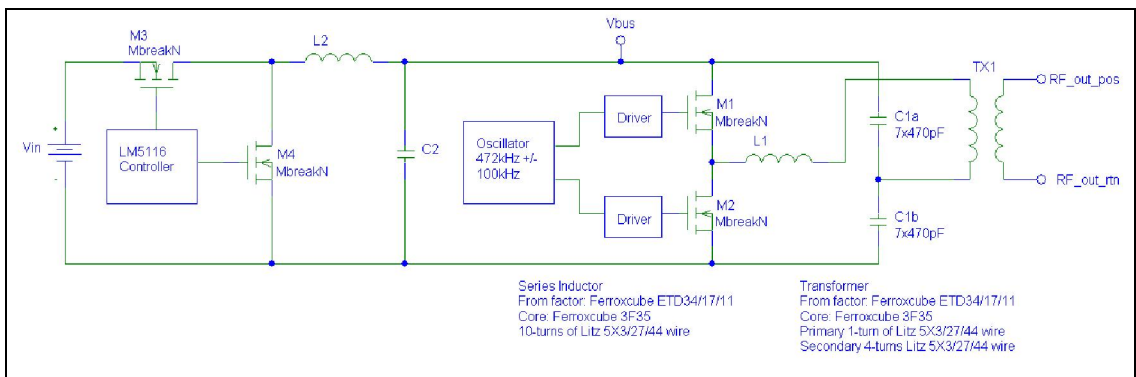
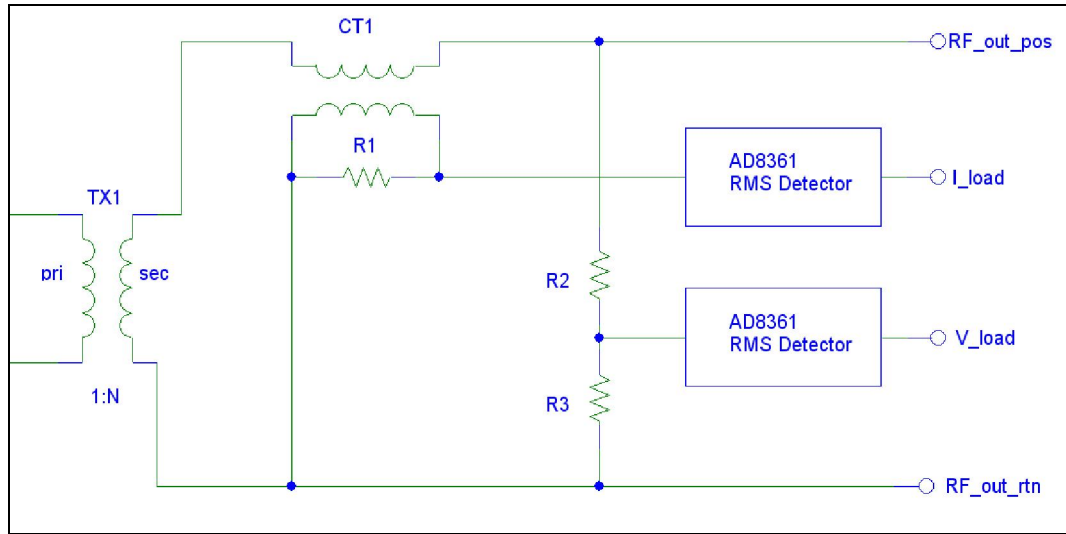


Figure 3.96; Simplified schematic of the system showing the power stages

The next challenge is controlling the frequency of the resonant stage with a varying load leading to two major hurdles. First being the method of sensing, if the output stage is operating in resonance or not. Second is how to shift the frequency to force resonance operation.

One of the simplest ways to control the output stage in order to operate at resonance would be to use a microprocessor to monitor the output and digitally control the oscillator. There are many ways of creating a continuous adjusting algorithm and that could monitor the phase relationship of the input current and voltage to the resonance stage, but at 500kHz the sampling and measurement methods become very complex. One of the simplest sensing methods would be to sense the output voltage and current, and then calculate the load impedance. The output frequency is adjusted through a look-up table based on the load impedance. Creation of the table requires extra work at the calibration of the system. By choosing this method allows the use of a lower cost microcontroller, lower cost simple voltage and current sensing circuitry.

Sensing the output voltage and current will be done using a resistive voltage divider and a current sense transformer that feeds into RMS detectors (Figure 3.97). The RMS detector provides a DC output voltage that is proportional to the RMS input value. Then, the DC signal is sampled by the microcontroller through analog-to-digital-converters (ADC) inputs, which then, can be used by the control software to calculate the output impedance and in turn control/adjust the output frequency to maintain operation at resonance.



*Figure 3.97; RF output voltage and current monitoring*

Besides monitoring and controlling the output operation point, the microcontroller will also control the output voltage of the DC-DC converter to adjust the peak output voltage. And, as an added bonus of the flexibility of using a microcontroller, the input voltage, input current, DC-DC output voltage and DC-DC output current can be monitored for little additional cost. This allows the efficiencies of the DC-DC stage and RF stage to be calculated. The finite details of the circuitry design will not be covered beyond the RF stage, but for reference, the complete schematic is provided in Appendix A.

***Expectations of Testing***

The high level view of the expectations from testing is to show that the design can meet the design targets, and mainly the overall efficiency. In order to fully evaluate the design the testing is split into sections:

- Efficiency of the DC-DC stage
- Efficiency of RF stage
- Efficiency of the whole system
- Performance with resistive loads
- Performance with reactive loads

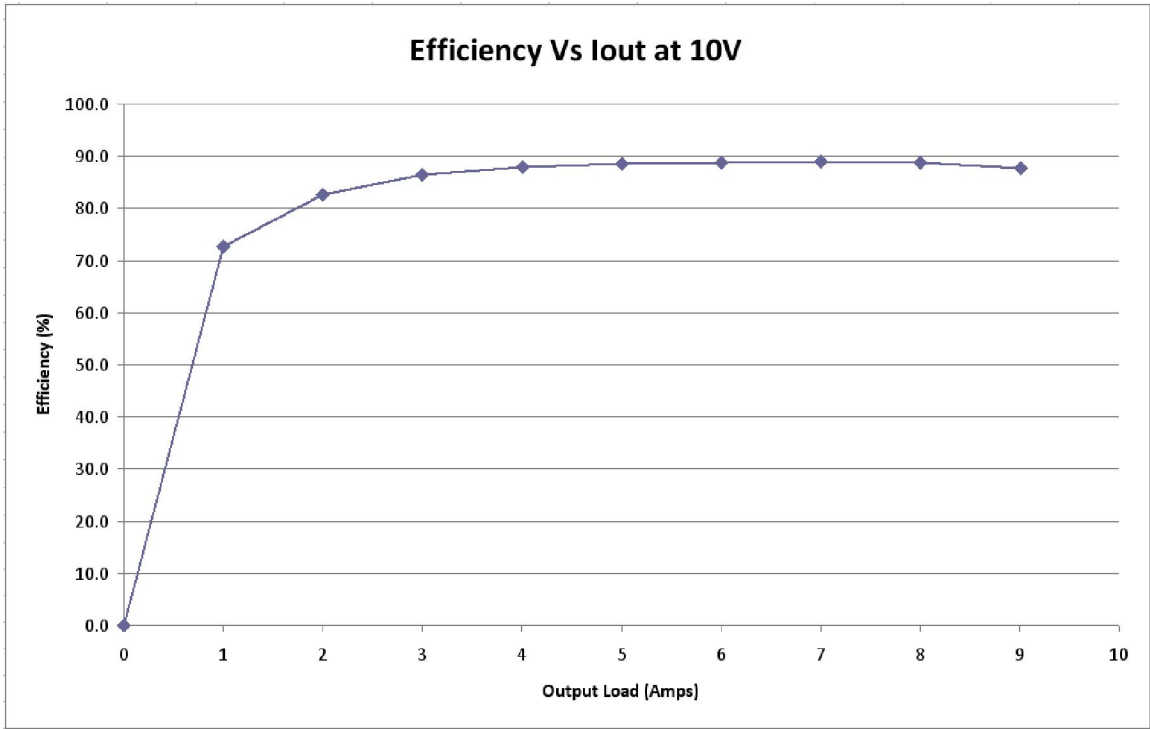
***DC-DC Stage Performance***

The DC output performance was tested at two output voltages, 10V and 35V with the input at the nominal level of 48V. To find the efficiency, the input voltage, input current, output voltage and output current were collected at 10V and 35V output voltage (Table 4.1). Then using this data to calculate the efficiency of the converter stage both 10V output voltage (Figure 4.2) and 35V output voltage (Figure 4.3).

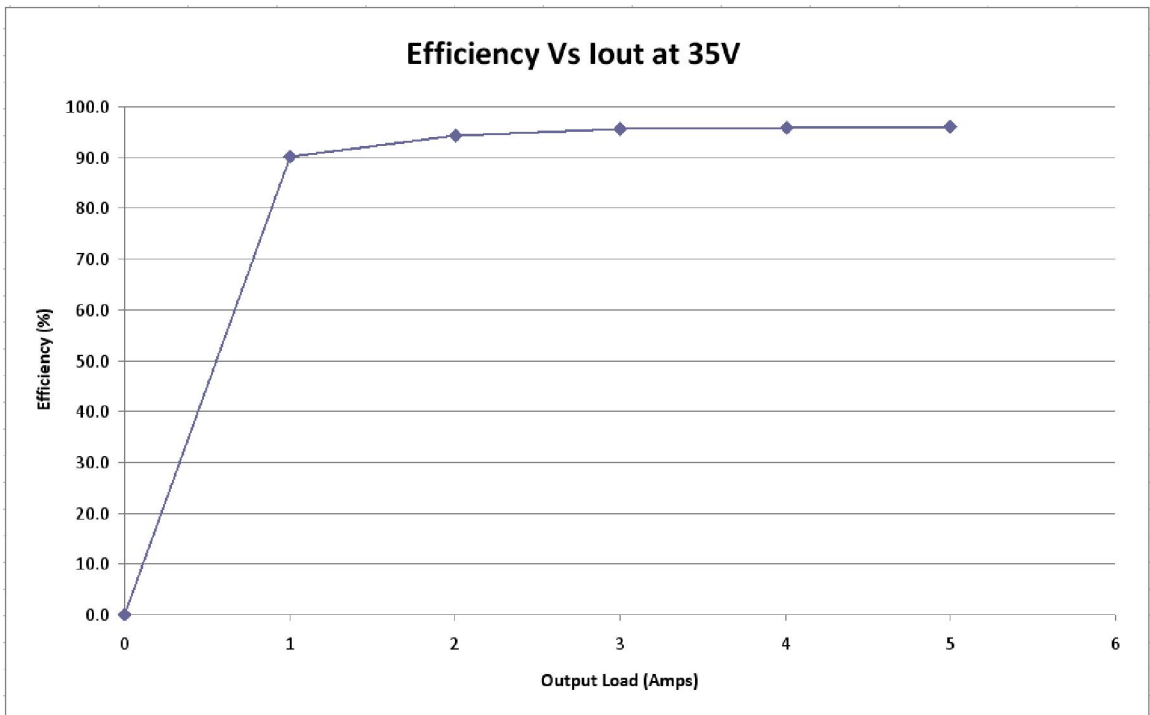
Based on the results, the DC-DC stage is capable of 87% efficiency at 10V out at 90 watts output and 95% at 35V at 100 watts. These results are expected, where the efficiency decreases at lower output voltage and improves at higher output voltage because the switching losses of the main switch vary proportional with the output voltage.

Table 4.1; Data from testing

Vin	Iin	Vout	Iout_10V	Pin	Pout	Eff
48.5	0.063	10.00	0.000	3.06	0.00	0.0
48.5	0.284	10.00	1.000	13.77	10.00	72.6
48.5	0.498	9.99	2.000	24.15	19.98	82.7
48.5	0.715	9.99	3.001	34.68	29.98	86.5
48.5	0.937	9.98	4.006	45.44	39.98	88.0
48.5	1.161	9.98	5.000	56.31	49.90	88.6
48.5	1.388	9.97	6.000	67.32	59.82	88.9
48.5	1.619	9.97	7.000	78.52	69.79	88.9
48.5	1.852	9.96	8.000	89.82	79.68	88.7
48.5	2.107	9.95	9.010	102.19	89.65	87.7
Vin	Iin	Vout	Iout_35V	Pin	Pout	Eff
48.5	0.068	35.00	0.000	3.30	0.00	0.0
48.4	0.803	35.00	1.000	38.87	35.00	90.1
48.3	1.535	34.90	2.003	74.14	69.90	94.3
48.3	2.275	35.00	3.001	109.88	105.04	95.6
48.2	3.026	34.90	4.006	145.85	139.81	95.9
48.1	3.774	34.90	5.000	181.53	174.50	96.1



*Figure 4.2; Efficiency at 10V output*



*Figure 4.3; Efficiency at 35V output*



### ***RF Stage Efficiency Performance***

Initial testing of the RF power stage yielded less than favorable results in efficiency and stability. It was quickly noticed that the magnetic core of the series inductor and transformer were running extremely hot, and was an indication of high core losses. Both the efficiency and stability are a direct result of the high core losses and excessive heating. As ferrite core material heats, there is a decrease in the relative permeability of the core, which results in a decrease in inductance. These early results showed that the cores were not thermally stable, and to a point, if left uncorrected, the power magnetics would experience irrevocable damage to the windings and form factors (Bobbins). The quickest and simplest solution was to aid in the cooling of the power magnetics using forced air from a small fan. With the addition of the cooling fan, testing commenced, but only to find that the transformer core was still excessively overheating. At this point any testing would not be viable and the design was in jeopardy of failing, and could be forced to a redesign.

In an attempt to stabilize the power losses in the transformer core without severely impacting the primary magnetization inductance, the core was shimmed to produce a small gap of 0.1mm. This gap size was chosen more on convenience than analysis, simply because using 20 pound typing paper for shimming would produce about a 0.1mm gap per sheet, which will result in an effective gap of 0.2mm. Using the core gap equations from Chapter 3 (Equation 4.4), the resulting impacts the flux density and inductance can be found.

$$B_{\text{core}} := n_{L1} \cdot I_{\text{pri}} \cdot \mu_r \cdot \mu_o \cdot \frac{1}{(l_{e\_m} + l_{g\_m} \cdot \mu_r)}$$

$$L := n_{L1}^2 \cdot A_{e\_m} \cdot \mu_r \cdot \mu_o \cdot \frac{1}{(l_{e\_m} + l_{g\_m} \cdot \mu_r)}$$

*Equation 4.4; Complete equations for core flux density and inductance based on core properties*

At the maximum primary current of 9.5 Amps RMS, the flux density of the core decreased from 0.181 Tesla to 0.045 Tesla, which is about a factor of four. The negative side of adding the 0.1mm gap is that the primary magnetization inductance decreases from 1.847 uH to 0.459 uH. As pointed out in Chapter 3, the decrease in inductance will impact the efficiency of the transformer at lighter loads.

The combination of the proposed solutions of forced air cooling and gapping the transformer greatly improved the thermal stability of the resonance power stage. The next step was to tune the resonance frequency verses load impedance. Tuning is done in two steps, first adjust the capacitance value to achieve the desired resonant frequency (approximately 472kHz) at maximum output power and load resistance (20 Ohms). Then, adjust the frequency for the other load values and record the frequency values in the look-up table for use by the software for managing the output frequency. Selection of the frequency for each load is done by adjusting the output frequency for each load value until the switch voltage and current were in phase (Figure 4.6) or slightly capacitive (leading current) (Figure 4.7). By slightly tuning the resonant network capacitive, it allows the resonance stage to become more stable as the inductance decreases due to

heating. Decrease in inductance is common for magnetic cores, and can be as high as 20% under normal operation. On the flip side, if the resonance stage is operating more inductive (Figure 4.8) then heating of the inductive devices could lead to instability.

The tuning process results yielded a total capacitance of 22000pF at maximum output power at 463kHz and 25 Ohm load. The final tuning results are shown in Table 4.5. The total required capacitance was significantly higher than expected, indicating that the effective inductance was lower than the targeted 9.25uH. By calculating the effective inductance based on the final capacitance of 22000pF, it showed the effective inductance was lower than the target value (Equation 4.9) and closer to 5.4uH. This error is contributed to the tolerance of the core permeability, shift in permeability with increase flux, and tolerance of the gapping materials.

*Table 4.5; Tuning results*

Load (Ohm)	Frequency (kHz)
20	464.5
25	463.0
50	461.5
75	460.0
100	460.5
150	459.0
200	458.0
300	458.0
400	458.0
500	457.5
OPEN	456.0

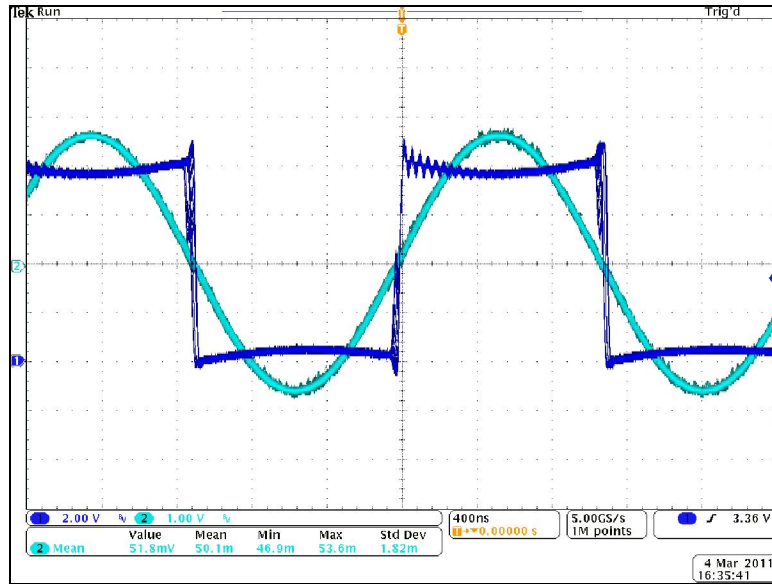


Figure 4.6; Switch current and voltage operating at resonance

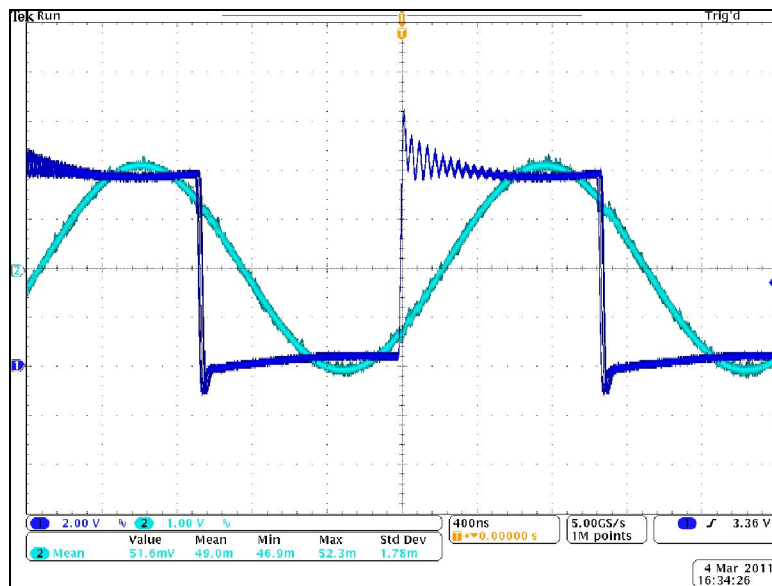


Figure 4.7; Switch current and voltage operating slightly capacitive

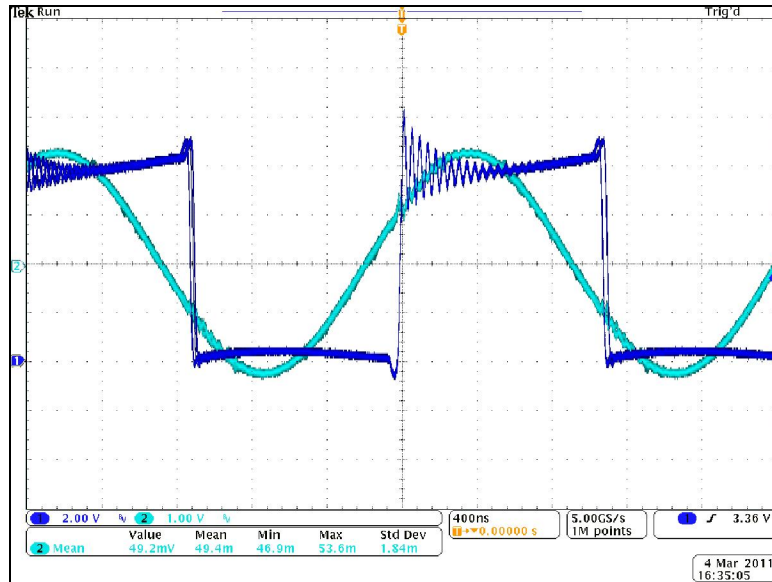


Figure 4.8; Switch current and voltage operating slightly Inductive

$$f := 463\text{k Hz} \quad C := 22000\text{p F}$$

$$f = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$

$$L := \left( \frac{1}{2 \cdot \pi \cdot f} \right)^2 \cdot \frac{1}{C}$$

$$L = 5.371 \times 10^{-6} \text{ H}$$

Equation 4.9; Finding the effective inductance

It was quickly noticed during tuning that the performance of the resonance stage was greatly improved, stable, and more efficient, but was still not meeting expectations in efficiency and that further improvements will be needed. The maximum output power level was at least 50% off the expected and the efficiency was extremely low. For comparison, the target output power and the actual output power is shown in Figure 4.10, and efficiency is shown in Figure 4.11.

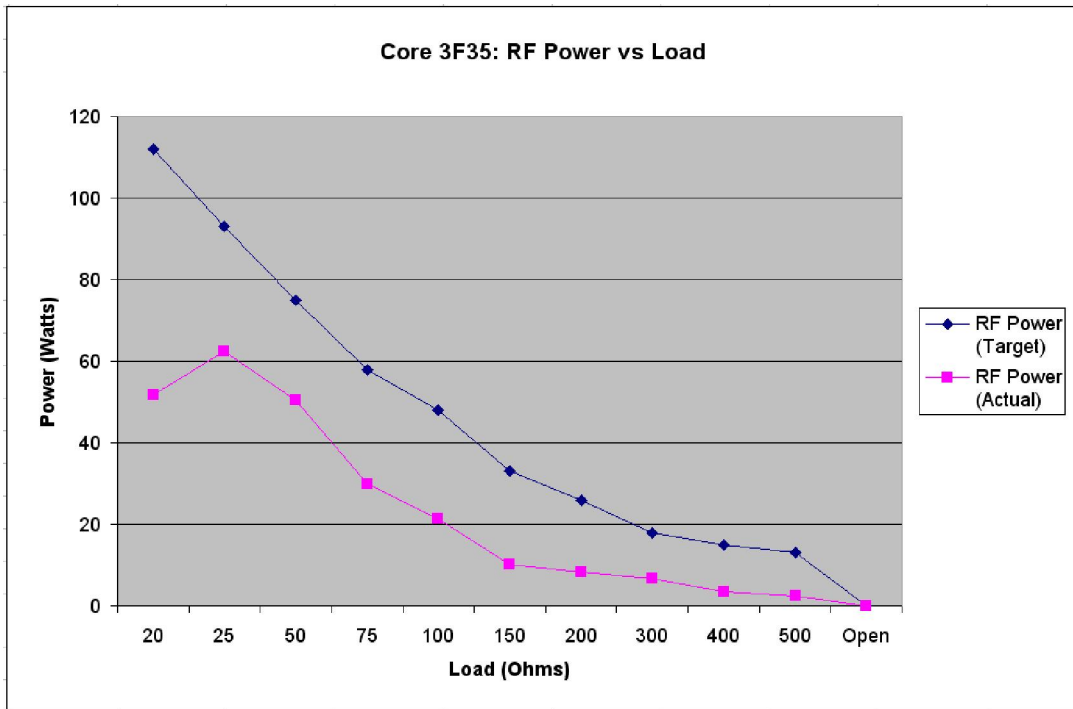


Figure 4.10; Comparison plot of the actual and target output power

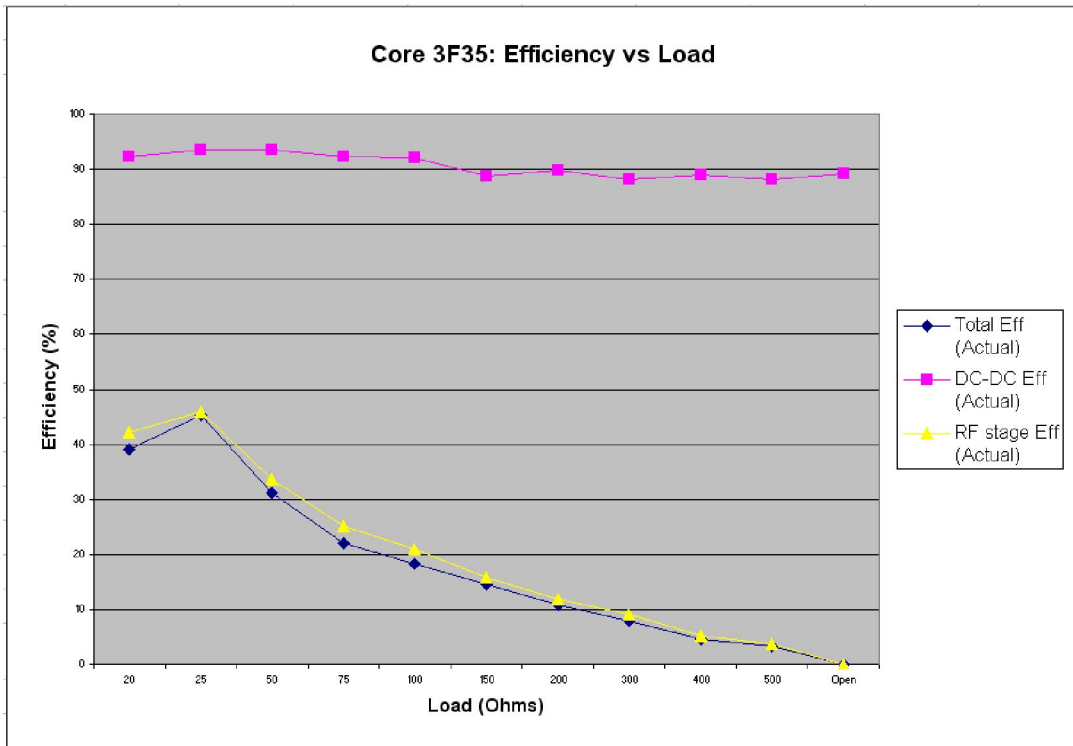
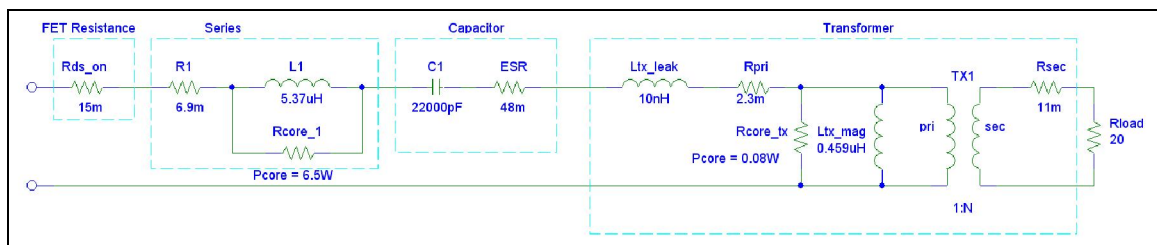


Figure 4.11; Efficiency of the first round of testing

Using a simple and basic technique of chasing the heat (selecting the hottest component) to isolate the main contributor to the decreased efficiency quickly identified the series inductor to be a concern. The core of the series inductor was almost too hot to the touch, but the windings were acceptable. At first thought, the core gapping could have been miscalculated leading to a higher core loss than anticipated. Review of the calculation in Chapter 3 yielded no errors.

In an attempt to understand the loss mechanisms, the “loss model” of Chapter 3 was updated to include the core losses as resistance instead of a simplified power. The focus will be to convert the parallel-series combination of passive elements to one series chain of resistors, inductors and capacitors starting from complete model (Figure 4.12).



*Figure 4.12; Loss Model from Chapter 3*

Simplifying the inductor model to include the core resistance expected at the maximum power operating point, showed that at 6.5 Watts the core resistance is approximately 7400 Ohms (Equation 4.13).

$$P_c = \frac{V^2}{R_c} = \frac{(I_{pri} \cdot X_L)^2}{R_c} \quad X_L := 2 \cdot \pi \cdot f \cdot L_1$$

$$X_L = 23.132 \quad \text{Ohms}$$

$$R_c := \frac{(I_{pri} \cdot X_L)^2}{P_c} \quad R_c = 7.43 \times 10^3 \quad \text{Ohm}$$

Equation 4.13; Inductor core resistance at max power point

Similarly, the transformer core loss can be represented as 810 Ohms, but with reference to the secondary side of the transformer in order to find the primary side voltage (Equation 4.14).

$$I_{Load} := \sqrt{\frac{P_{Load}}{R_{Load}}} \quad I_{Load} = 1.609 \quad \text{A}$$

$$V_{sec} := I_{Load} \cdot (R_{Load} + R_{sec}) \quad V_{sec} = 32.205 \quad \text{V}$$

$$V_{pri} := \frac{V_{sec}}{N} \quad V_{pri} = 8.051 \quad \text{V}$$

$$P_{c\_tx} = \frac{V_{pri}^2}{R_{c\_tx}} \quad R_{c\_tx} := \frac{V_{pri}^2}{P_{c\_tx}}$$

$$R_{c\_tx} = 810.266 \quad \text{Ohm}$$

Equation 4.14; Transformer core resistance at max power point

Using the impedance transformations for parallel to series (Equation 4.15) and vice versa quickly reduces the model (Figure 4.12) to one series chain of resistors, inductors and capacitors (Figure 4.16).



$$Q = \frac{R_p}{X_p} = \frac{X_s}{R_s} \quad R_p = (Q^2 + 1) \cdot R_s \quad X_p = X_s \cdot \frac{Q^2 + 1}{Q^2}$$

Equation 4.15; Parallel and Series relationship transformations

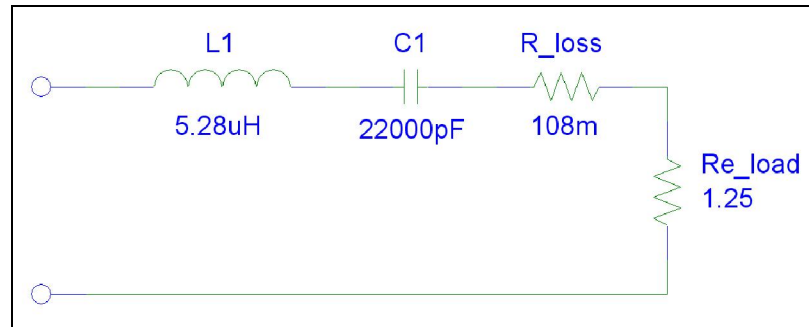


Figure 4.16; Simplified Loss Model

Using the revised model (Figure 4.16), and based on operating at resonant, the overall efficiency should be 92.05% (Equation 4.16).

$$P_o = R_L \cdot I^2 \quad P_i = R_T I^2$$

$$\eta_{RF} = 100 \cdot \frac{P_o}{P_i} = 100 \cdot \frac{(R_L \cdot I^2)}{(R_T I^2)}$$

$$R_L := 1.25 \quad R_T := 1.25 + 0.108$$

$$\eta_{RF} := 100 \cdot \frac{R_L}{R_T}$$

$$\eta_{RF} = 92.047 \quad \%$$

Equation 4.16; RF stage efficiency

Based on the simplified model and efficiency calculations, the core losses should not be sufficient enough to cause the unexpected decrease in efficiency. The only other possible explanation to the inducing heating in the series inductor would be proximity loss, and the additional impacts to the proximity losses related to the core eddy currents. A simple experiment to identify this would be to replace the series inductor with an air core inductor.

Using an air core inductor has two major disadvantages including no core to contain the flux (uncontained magnetic fields could couple in to other components) and an air core inductor is larger in size to achieve the inductance when compared to a ferrite-cored inductor. To minimize retuning, the inductance of the air-core inductor should be closer to that of the effective inductance of 5.4uH (Equation 4.9), but this is limited by the available area on the circuit board for the inductor. The area on the circuit board is about 40mm by 40mm with a high restriction of about 50mm. Based on these requirements, the inductor would require a significant number of turns and most likely be a multi-layer solenoid type. Using the formulas developed by Harold A. Wheeler [14] (Equation 4.17) for a multi-layer inductor, the resulting inductance is 5.6uH (Equation 4.18) for parameters shown in Table 4.19.

$L = \frac{0.8 \cdot r^2 \cdot N^2}{6r + 9l + 10d}$	All in inches r = coil mean radius l = coil length d = depth of coil (OD - ID) N = number of turns
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*Equation 4.17; Wheeler equation for multi-layer air core solenoid*

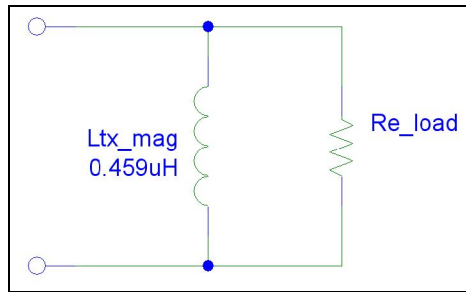
$N := 27$	3 layers of 9 turns
$l := 1.5$	inches
$OD := 1.25$	inches
$ID := 0.5$	inches
$r := \frac{OD + ID}{2} \cdot \frac{1}{2}$	$r = 0.438$ inches
$d := \frac{OD}{2} - \frac{ID}{2}$	$d = 0.375$ inches
$L := \frac{0.8 \cdot r^2 \cdot N^2}{6r + 9l + 10d}$	$L = 5.617$ uH

Equation 4.18; Calculations of the air-core inductor inductance

Table 4.19; Parameters of the multi-layer inductor

Outer Diameter	31.75 mm
Inner Diameter	12.70 mm
Overall Length	38.10 mm
Turns per Layer	9
Layers	3

A second area of potential improvement was also identified while updating the loss model. This was the magnetization inductance of the transformer, which was lowered by a factor of four due to the gapping of the transformer core for thermal stability. Lowering the magnetization inductance, impacts the overall efficiency at lighter loads, since the parallel reactance of the magnetization inductance becomes more dominate, shunting the current from the reflect load (Figure 4.20).



*Figure 4.20; Magnetization reactance in parallel with reflected load impedance*

The reactance of the magnetization inductance at 0.459uH is only 1.35 Ohm at 470kHz, which will greatly impact the amount of energy that is transferred to the load. By increasing the primary turns from one to two, the inductance and reactance will increase by a factor of four, allowing more energy to transfer to the load. The drawback to increasing the primary turns is that the secondary turns will have to be increased in order to maintain the turns ratio ( $N=4$ ). This results in a total number of turns on the bobbin to be 10-turns, resulting in an overfilled bobbin, making it impossible to build the transformers. A compromise is to reduce the turns ratio ( $N=3$ ), so that the transformer can be manufactured without changing the bobbin size. The negative effect is that this will impact the maximum output power at the maximum specified load, but at the same time greatly improving the efficiency at lighters.

### ***Improved RF Stage Efficiency Performance***

The overall efficiency and performance was greatly improved with the final changes to the series inductor (Table 4.21) and transformer (Table 4.22).

*Table 4.21; Final series inductor*

Inductance	5.6 uH
Outer Diameter	31.75 mm
Inner Diameter	12.70 mm
Overall Length	38.10 mm
Turns per Layer	9
Layers	3

*Table 4.22; Final transformer*

Primary Turns	2
Primary Inductance	1.8 uH
Secondary Turns	6
Secondary Inductance	8.12 uH
Turns Ratio	3
Core Gap	0.1 mm

The improvements increased the overall efficiency into the low 70% (Figure 4.23) and the output power exceeded the specified range with some margin (Figure 4.24). Testing also showed that the output voltage was a low distorting sinewave (Figure 4.26), that never exceeded the upper limit of 250 volts peak-peak (Figure 4.25).

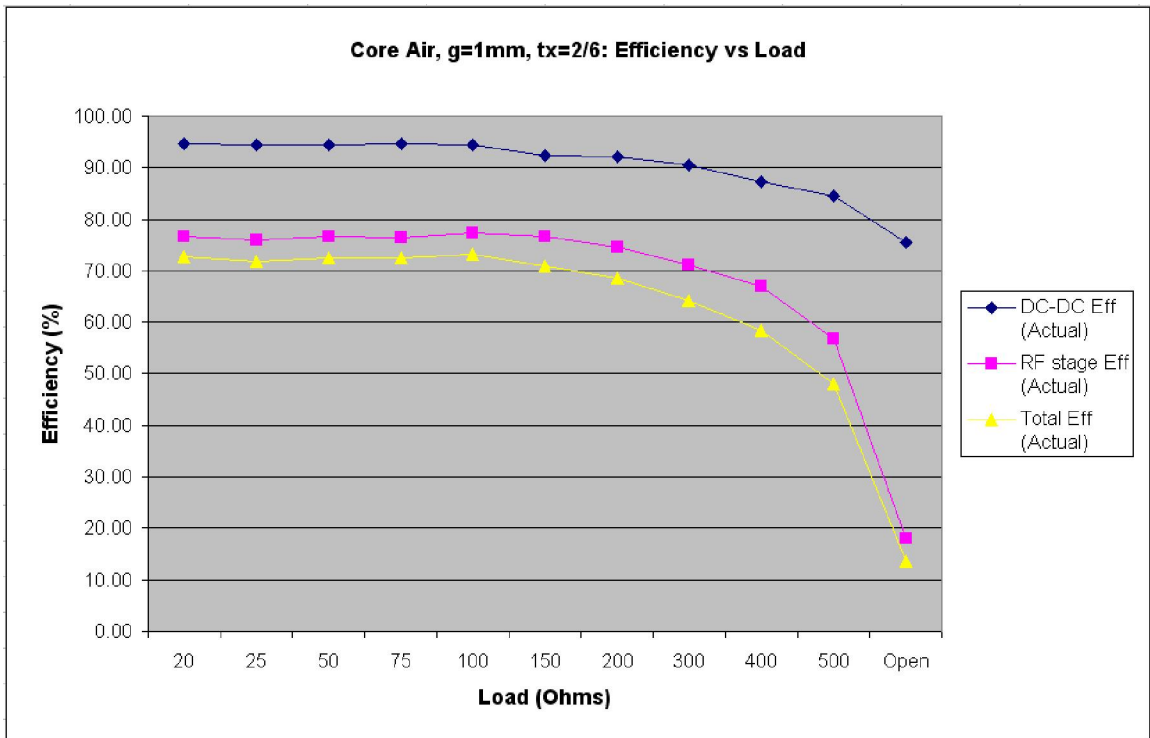


Figure 4.23; Efficiency testing of final design

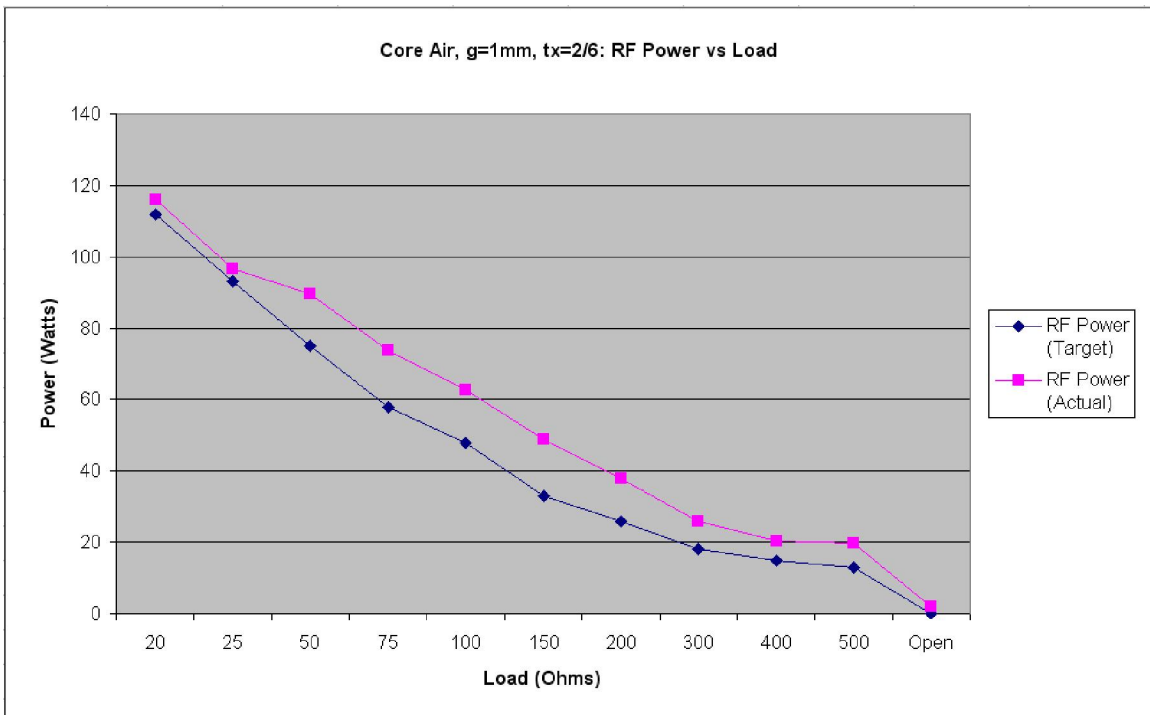


Figure 4.24; Output power testing of final design

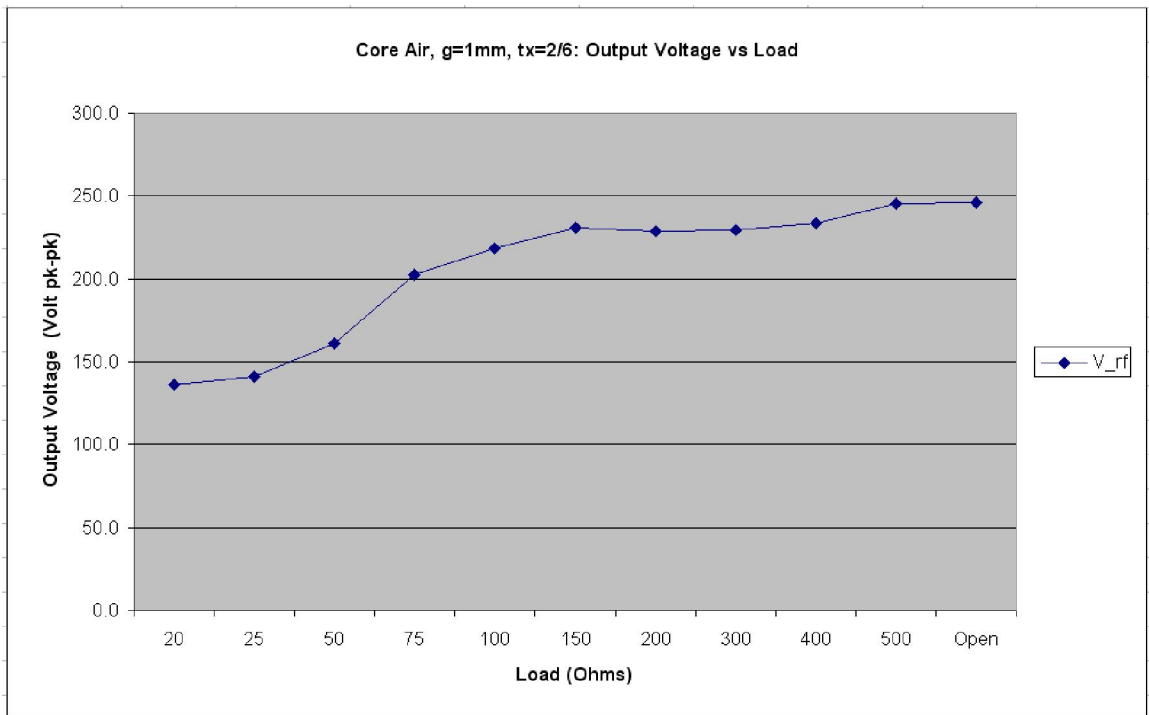


Figure 4.25; Peak-Peak output voltage verses load

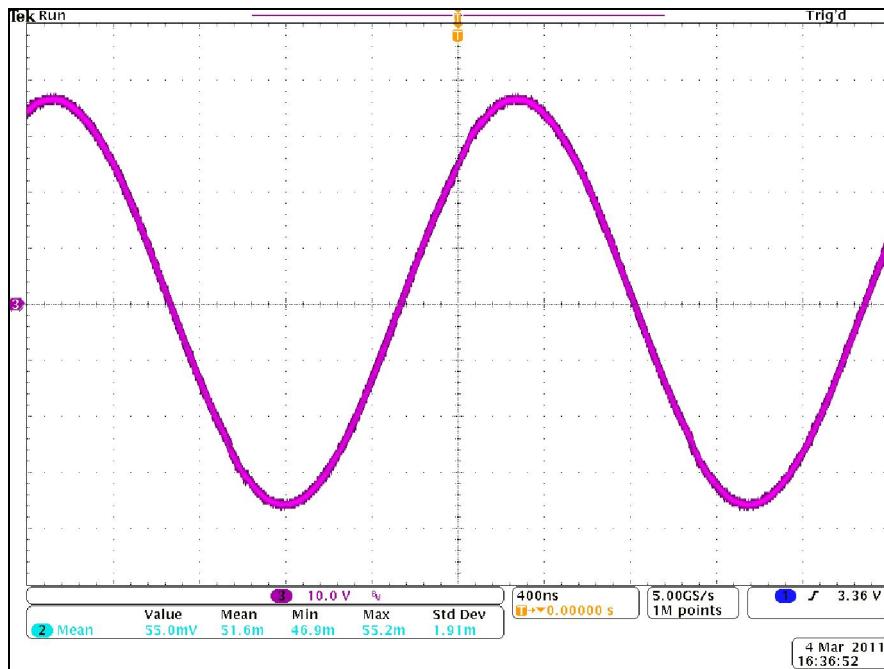


Figure 4.26; Waveform of voltage at load

Overall, the project was a success with two exceptions, which is summarized in table (Table 4.28). The first shortcoming is the overall package size is 212% greater than the target volume of 400 cm<sup>3</sup>. The actual volume was 1229 cm<sup>3</sup>. Second is the output efficiency is lower than expected with more reactive loads. As the load impedance shifts, less resistive and more reactive the output power capability is impacted resulting in a lower output level. This is more appearance with purely inductive loads, such as in the case of driving a step-up transformer.

*Table 4.27; Tuning, Output Power and Output Voltage results verses load*

Load (Ohm)	Frequency (kHz)	Output Voltage (Volts pk-pk)	Output Power (Watts)	Total Efficiency (%)
20	493.0	136.5	116.19	72.74
25	491.0	141.3	96.83	71.74
50	473.0	160.9	89.50	72.61
75	460.0	202.3	73.81	72.42
100	451.0	218.3	62.76	73.14
150	443.0	230.8	48.76	70.92
200	437.0	229.0	37.81	68.69
300	433.0	229.2	25.93	64.27
400	431.5	233.5	20.49	58.34
500	431.0	245.5	19.82	47.95
OPEN	431.0	246.0	1.81	13.62



*Table 4.28; Comparison between target and actual*

Parameter	Target	Actual
Input Voltage Range	42 to 60 Vdc	42 to 55 Vdc
Output Frequency at 50 Ohm	472kHz	473kHz
Frequency Variation	±23kHz ( $\Delta F = 46\text{kHz}$ )	+20kHz –42kHz ( $\Delta F = 62\text{kHz}$ )
Max output power	112 Watts at 20 Ohms	116 Watts at 20 Ohms
Output power derating	13 Watts at 500 Ohms	19.8 Watts at 500 Ohms
Output Load Impedance	20 to 500 Ohms	20 to 500 Ohms
Max output voltage at no load	250 Volts peak to peak	246 Volts peak to peak
Efficiency	>80% at full power	72.7% at 116 Watts
Package size	77mm x 102mm x 51mm (Volume 400 cm <sup>3</sup> )	127mm x 152.4mm x 63.5mm (Volume 1229.0 cm <sup>3</sup> )

### ***High Voltage Output***

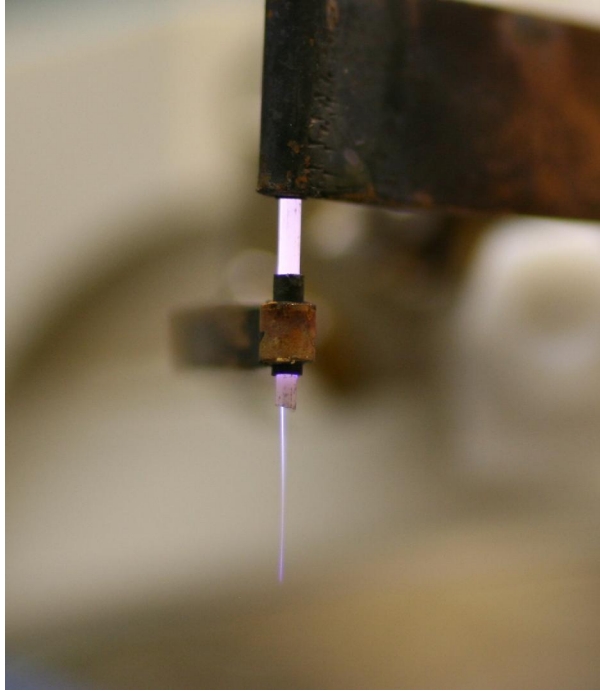
Late in the project, an additional requirement was introduced that would require the output to be able to drive a high voltage set-up transformer to produce a 1000 Volt source for generating plasmas. This requirement was not part of the original scope of the project, but was deemed valuable. One major concern about driving a plasma source, is that the impedance of the plasma is purely capacitive and the primary side of the step-up transformer is purely inductive when it's secondary is an open circuit.

The high voltage transformer was constructed using the same core set used in the output transformer of the RF Gen (Table 4.29), using the same design process as described earlier.

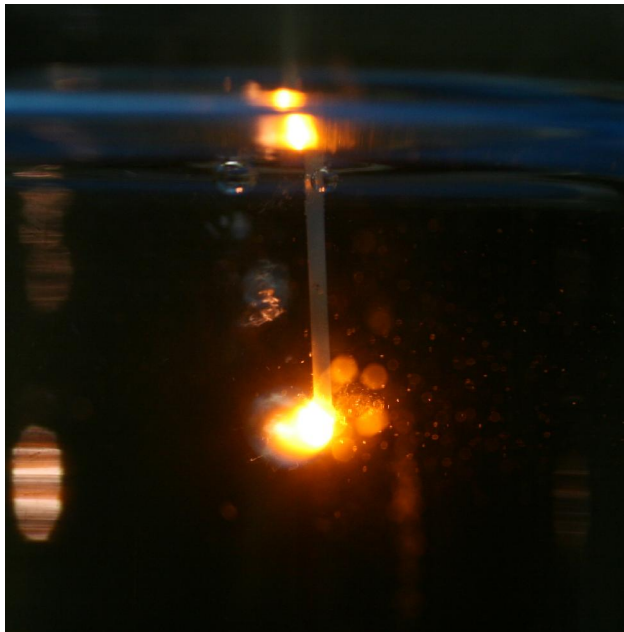
*Table 4.29; High voltage transformer*

Core material	Ferroxcube 3F35
Form factor	Ferroxcube ETD34/17/11
Insulating Tape (between layers)	3M 1205 Tape
Turns Ratio	15
Primary Turns	4
Primary Wire	4 parallel strands of 24AWG ESSEX H Ultrashield Plus
Primary Inductance	3.6 uH
Secondary Turns	60
Secondary Wire	1 strand of 24AWG ESSEX H Ultrashield Plus
Secondary Inductance	1665 uH
Core Gap	0.1 mm

Laboratory testing showed that the RF Gen was capable of driving the high voltage transformer and producing the 1000 volt secondary output signal sufficient enough power to produce and sustain plasma in both a gas (Figure 4.30) and liquid (Figure 4.31) media. However, the sensed output impedance of the transformer forced the output frequency to operate lower than optimum. This caused a lower output power resulting in lower efficiency.



*Figure 4.30; Plasma torch in gas media*



*Figure 4.31; Plasma torch in liquid media*

Based on the test results there is four potential areas of improvements.

- Improved dynamic frequency tuning for improved efficiency control
- Design a variation of the Electrosurgery Generator for uses as Plasma Generator
- Implement high voltage dynamic load impedance matching for maximum power transfer
- Further reduction in overall size to meet the design target of 400 cm<sup>3</sup>

### ***Improved Dynamic Frequency Tuning***

The phase of the voltage and current in the power switches of a modified Class-D amplifier stage is affected by the type of load. For a purely resistive load the voltage and current are in phase (Figure 5.1), and for a reactive (inductive or capacitive) load the current lags the voltage (Figure 5.2).

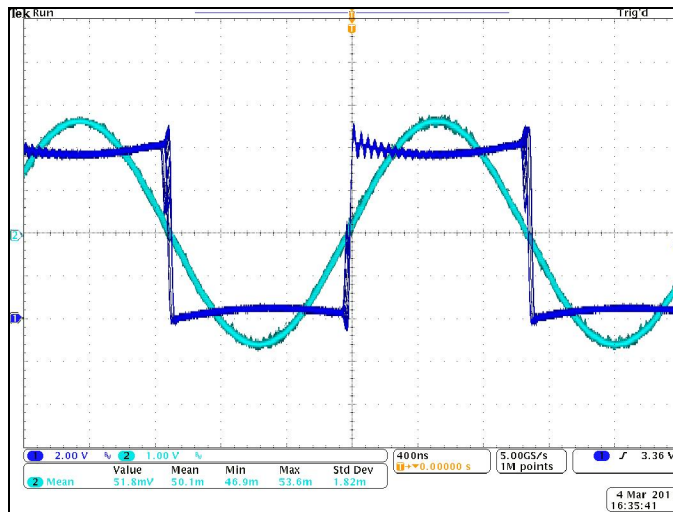


Figure 5.1; Switch voltage and current for resistive load

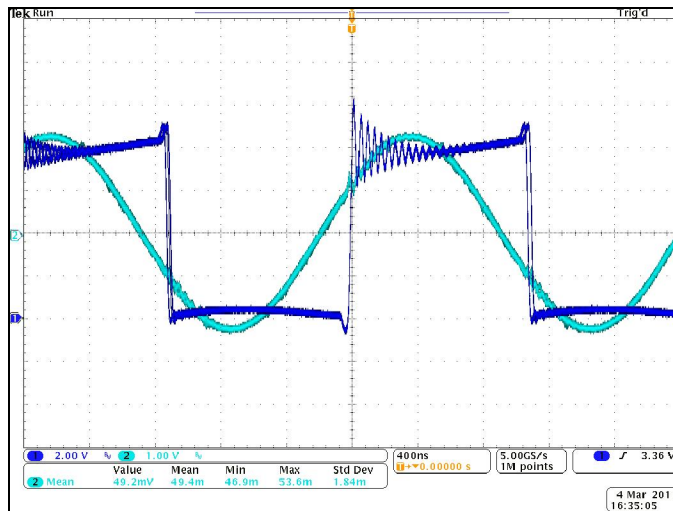


Figure 5.2; Switch voltage and current for reactive load

Sensing the switch voltage is rather simple, and can be easily done using a resistive divider followed by some comparator to produce a logic level rectangle waveform. However sensing the sinewave switch current is not as simple. First off it is a sinewave, second it varies in amplitude as a function of the load impedance. One solution is to use a current sense transformer to produce a lower power signal that represents the current

that can be converted to a rectangle waveform using another comparator circuit. This concept was tested through simulation (Figure 5.3), which produced two logic level signals representing the switch voltage and switch current (Figure 5.4).

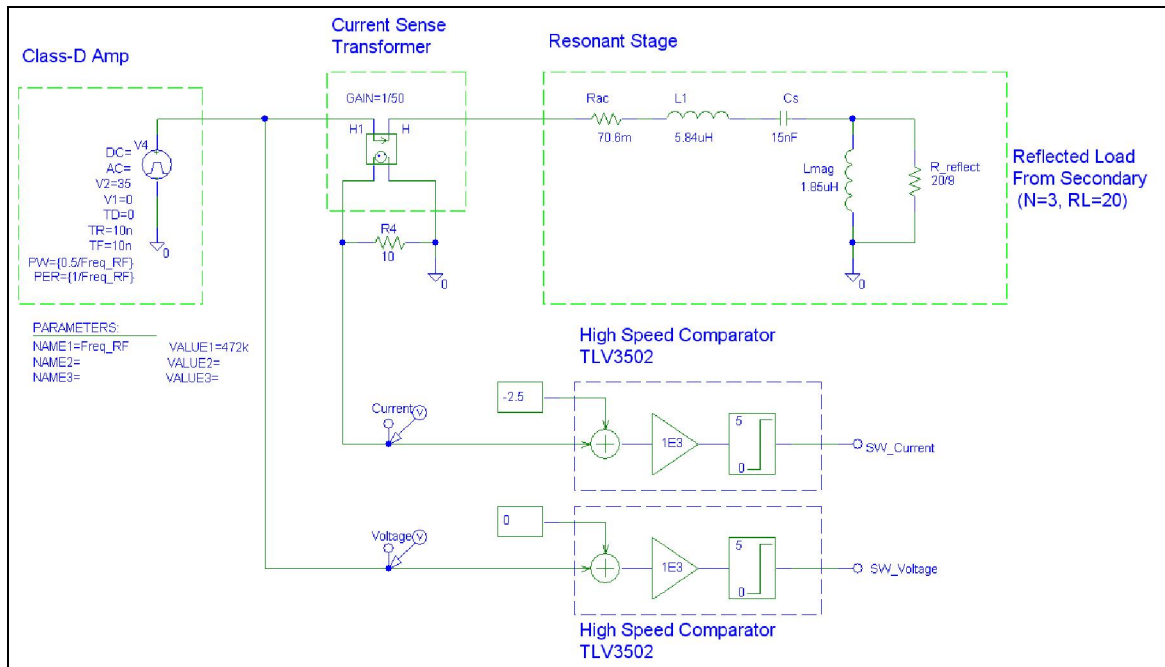


Figure 5.3; Simulation model for switch voltage and current sensing

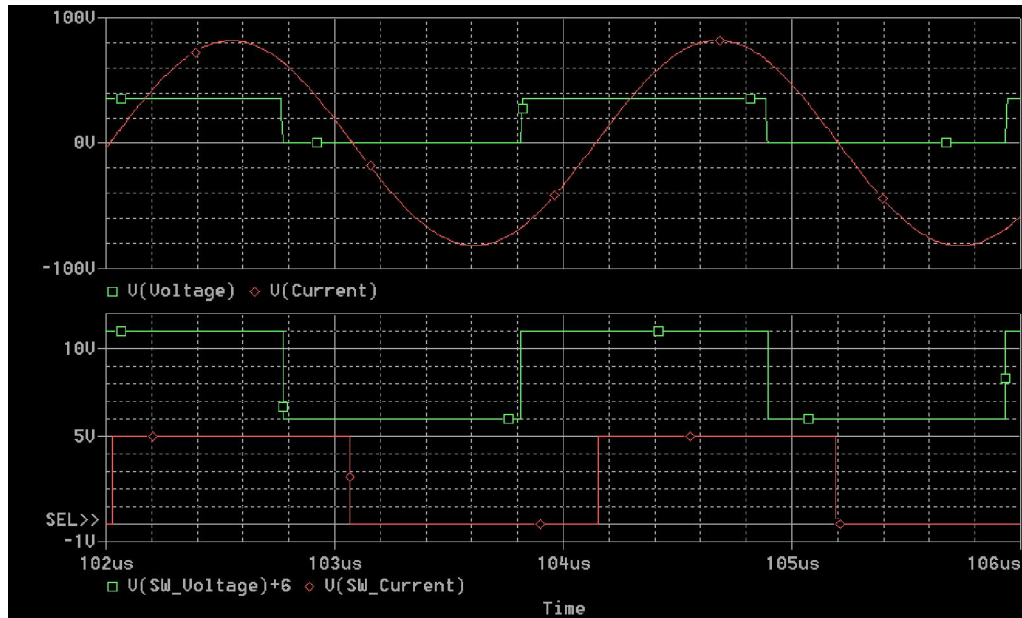


Figure 5.4; Simulation output for switch voltage and current sensing

By comparing the two logic signals representing the switch voltage and switch current through an edge-trigger set-reset (SR) flip-flop (Figure 5.5) produces a variable duty cycle signal that is proportion to the phase difference. The output signal is pulse width modulation (Figure 5.6) that can be filtered through a 2-pole low pass filter (Figure 5.5) to produce an analog voltage that is proportional to the phase delay (Table 5.7).

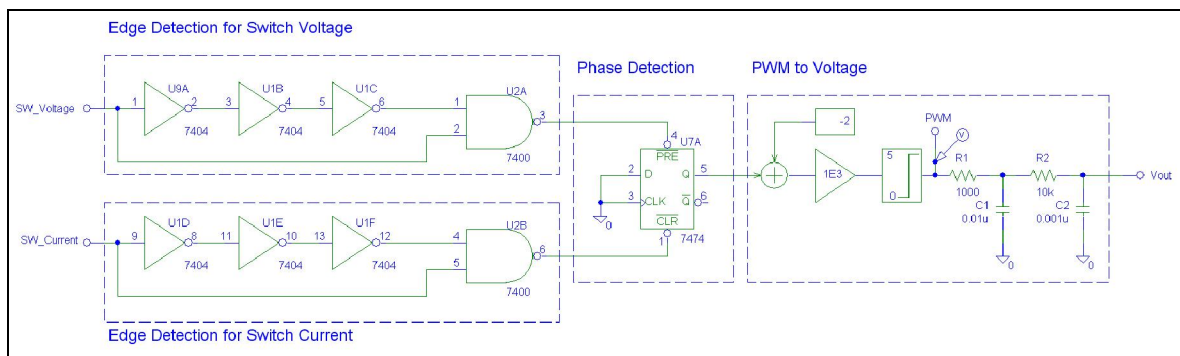


Figure 5.5; Simulation model for the phase detection circuit

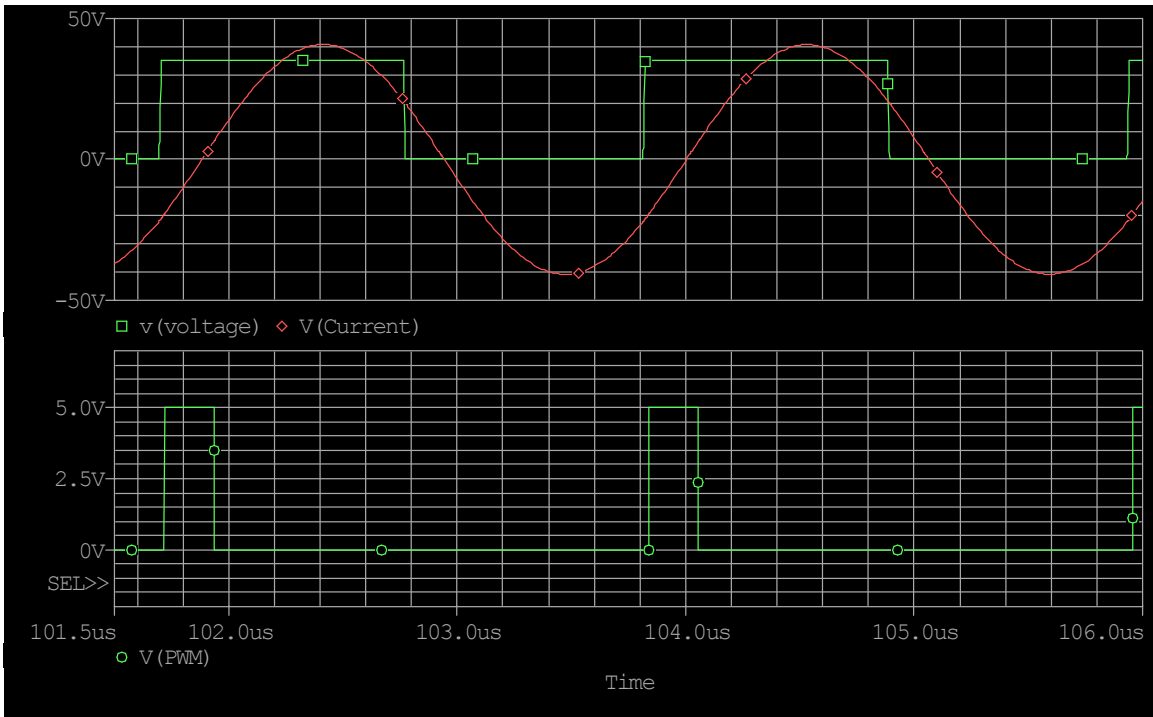


Figure 5.6; Simulation output for phase detection

Table 5.7; Phase detector simulation results

Phase Shift (Degrees)	PWM Duty Cycle (%)	Output Voltage (Voltage)
0	2.2	0.108
45	12.9	0.645
90	25.4	1.272
135	37.9	1.895
180	50.4	2.522
225	62.9	3.145
270	75.4	3.768
315	87.9	4.395
351	97.9	4.895



### ***Plasma Generator Version***

Testing showed that the high voltage version for driving plasma torches was a prospective and a valuable avenue that should be pursued further. In doing so the design of the printed circuit board (PCB) needs updating in order to handle the higher output voltages. Mainly addressing two issues; first being the physical spacing between the output traces, currently the spacing is only enough for 500V. Second the method of sensing the output current needs higher isolation voltage rating. The current part used in the design is only rated for 500 V RMS.

### ***Dynamic Impedance Load Matching***

With the additional design changes for handling the higher voltages needed for use as a plasma generator, the output stage should be redesign to provide some type of impedance matching to address the reactive impedance of a plasma load. One possible solution would be to use a phase/gain sensing circuit to detect the phase, and some type of RF switching network such as a P-I-N diode network to perform the matching.

### ***Reduction in Size***

The last future improvement would be to redesign the buck stage to handle other voltage ranges to eliminate the current requirement of having an external 48V power supply. There are two options that should be considered. First, design the input voltage to be compatible with 110/220VAC wall power. Second, change the design to be compatible with battery power to produce a portable version for use by emergency medical response personnel.

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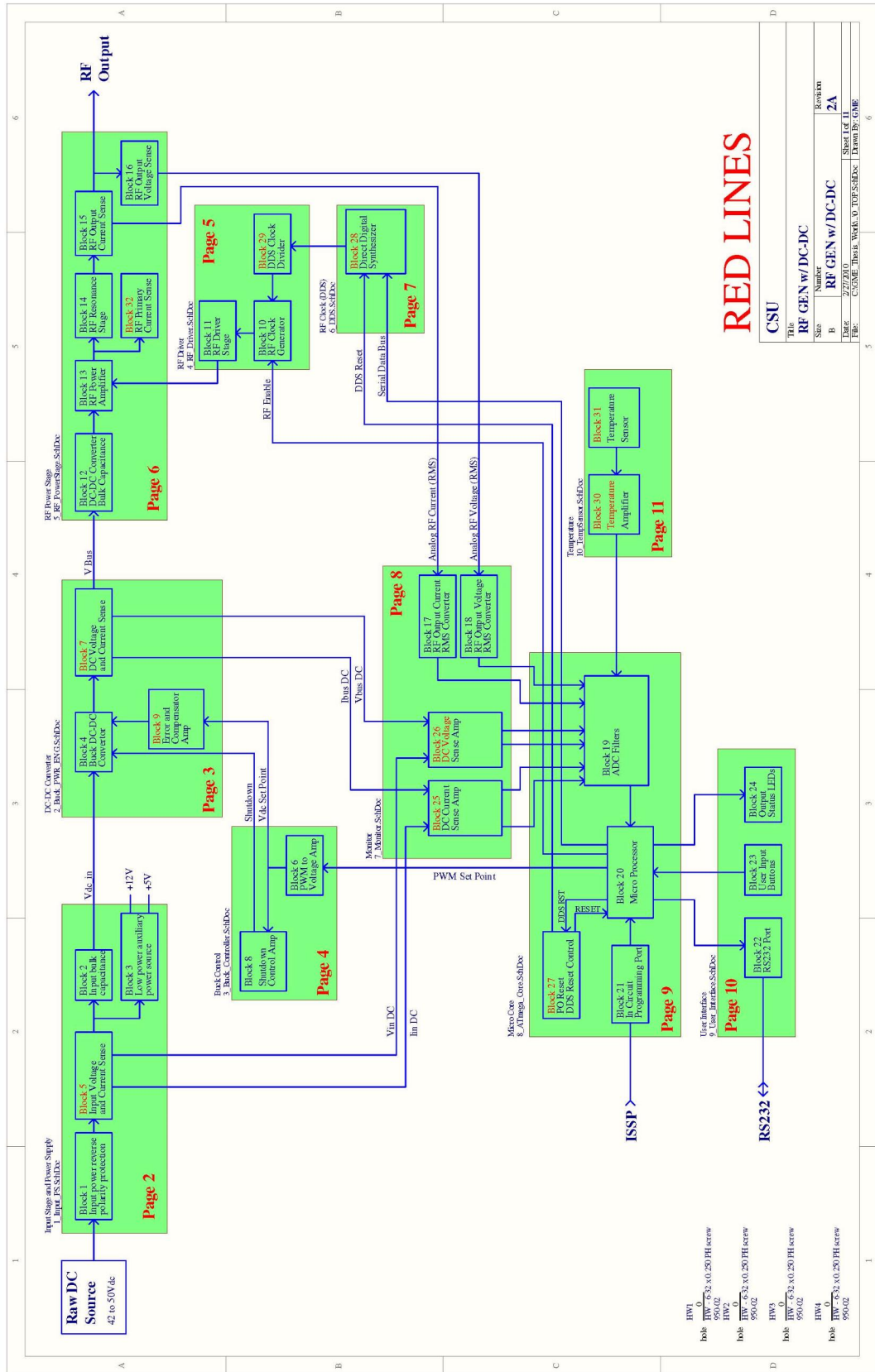
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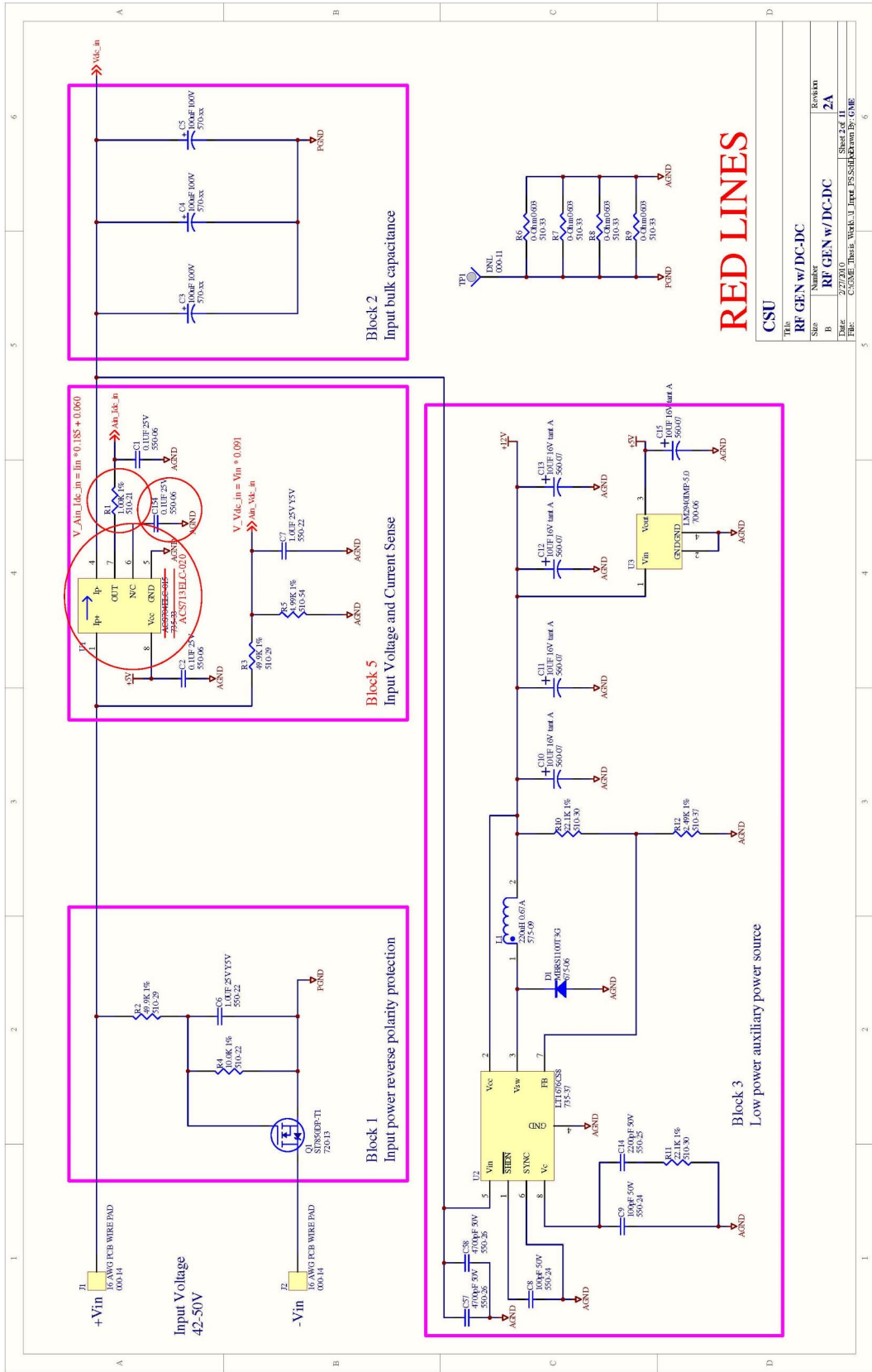
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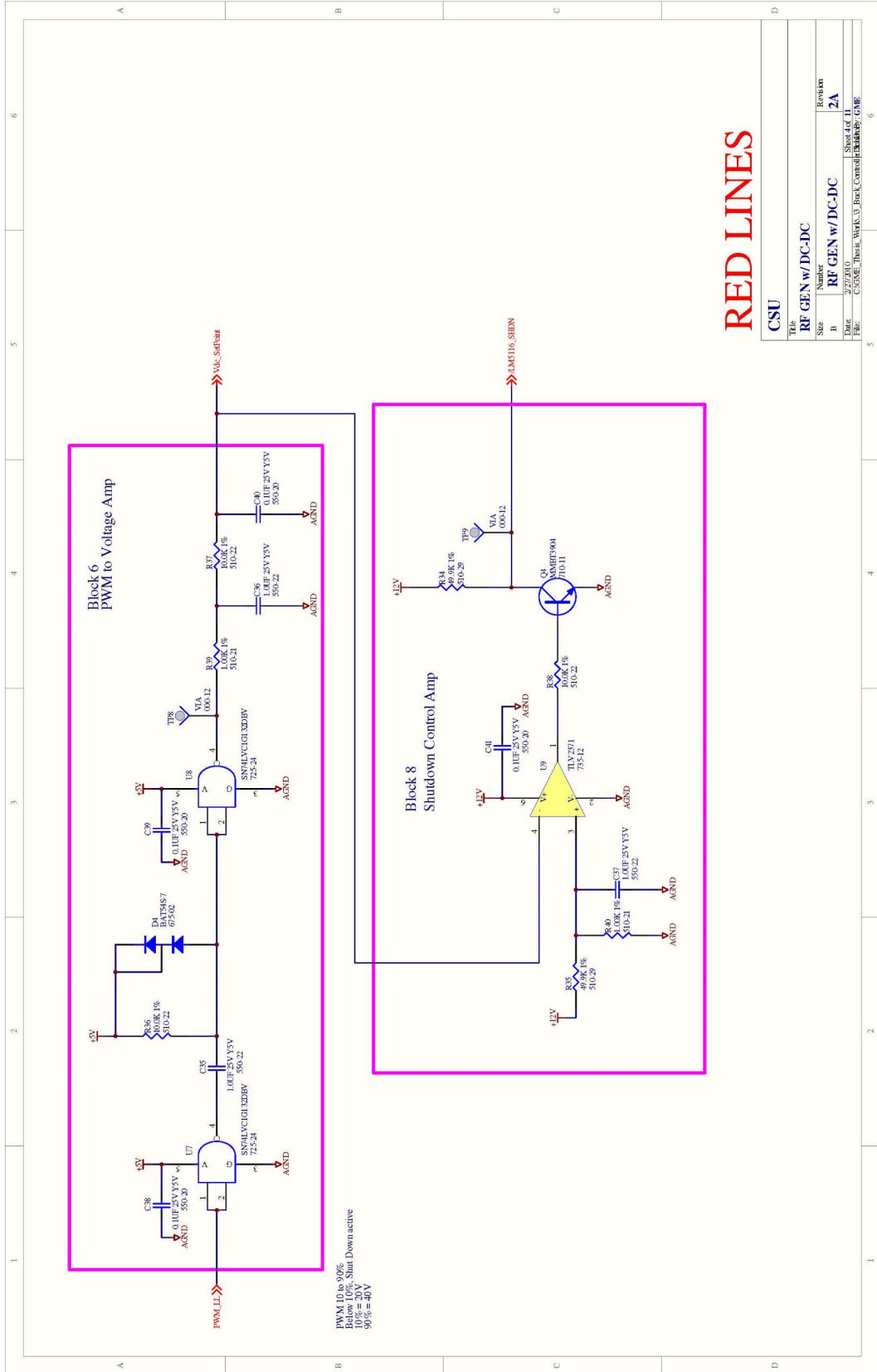


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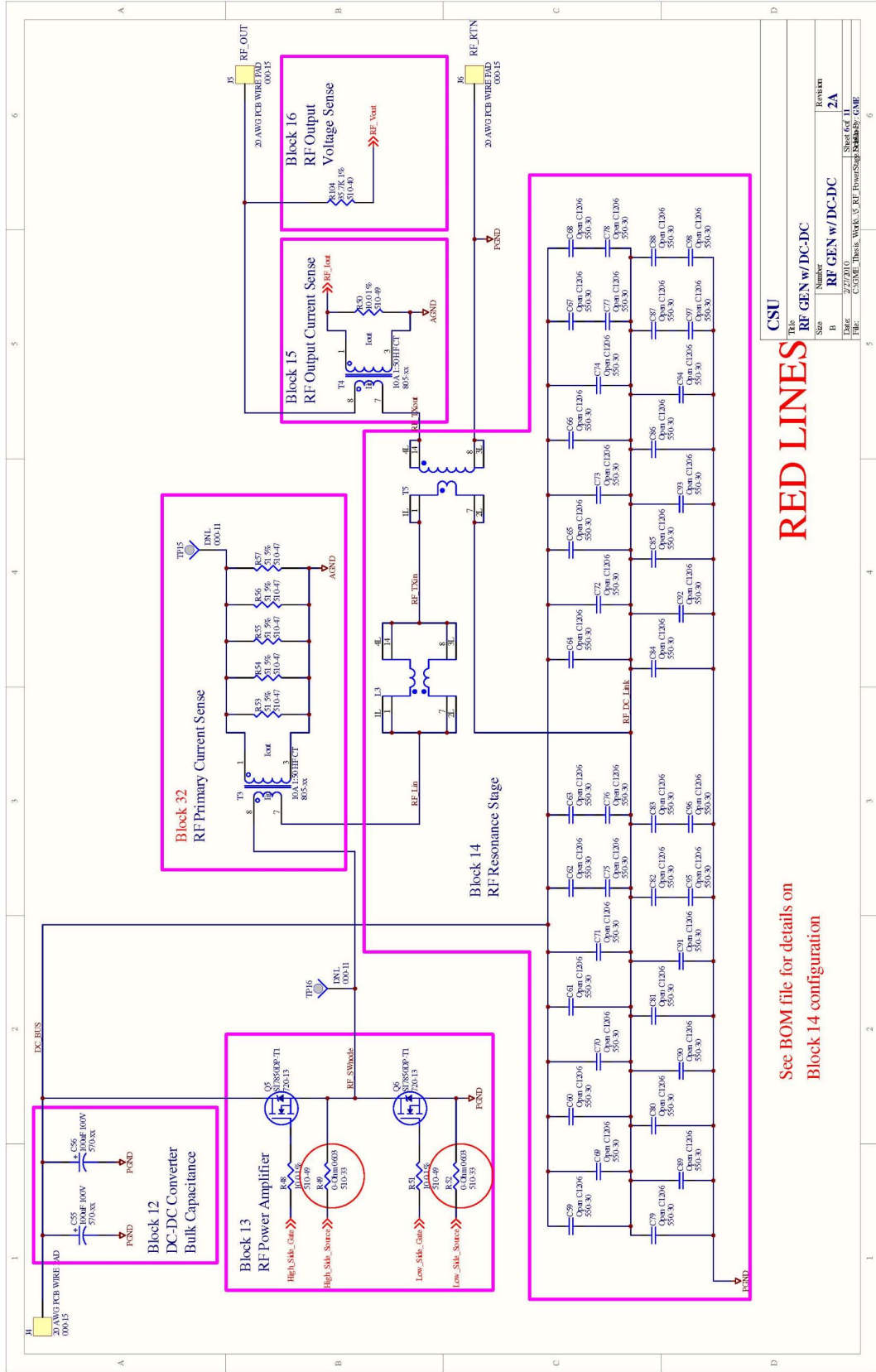






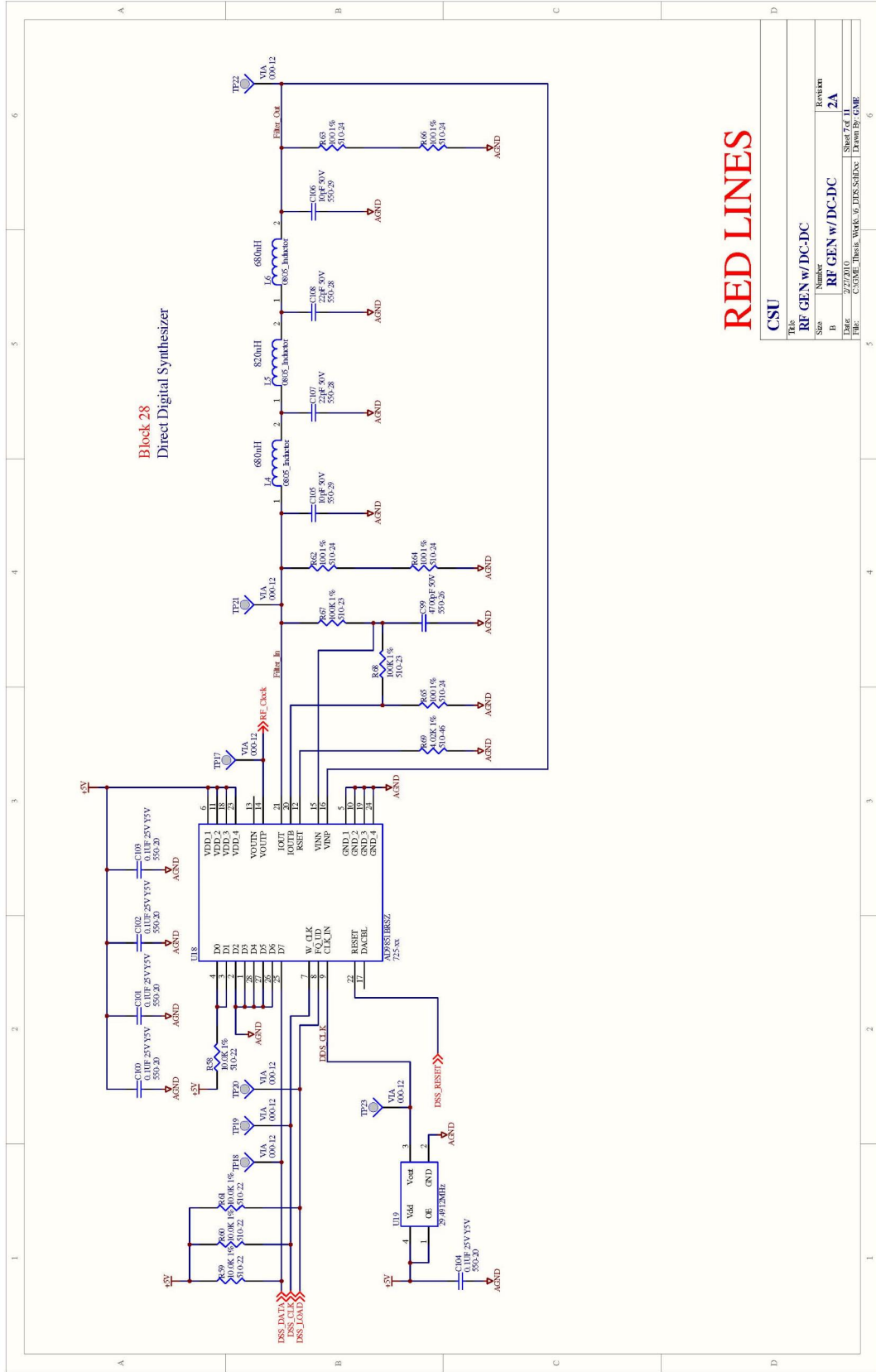
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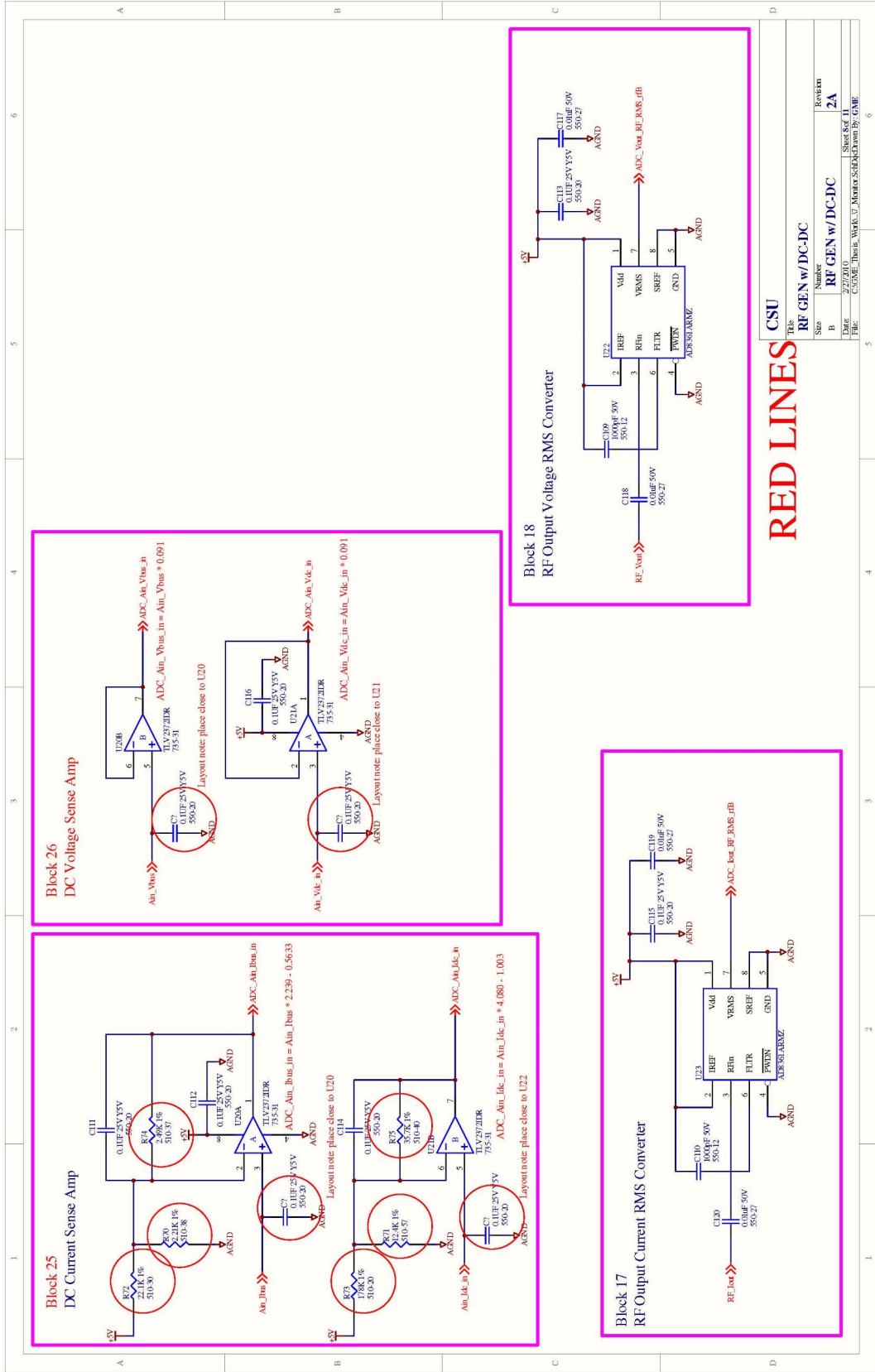
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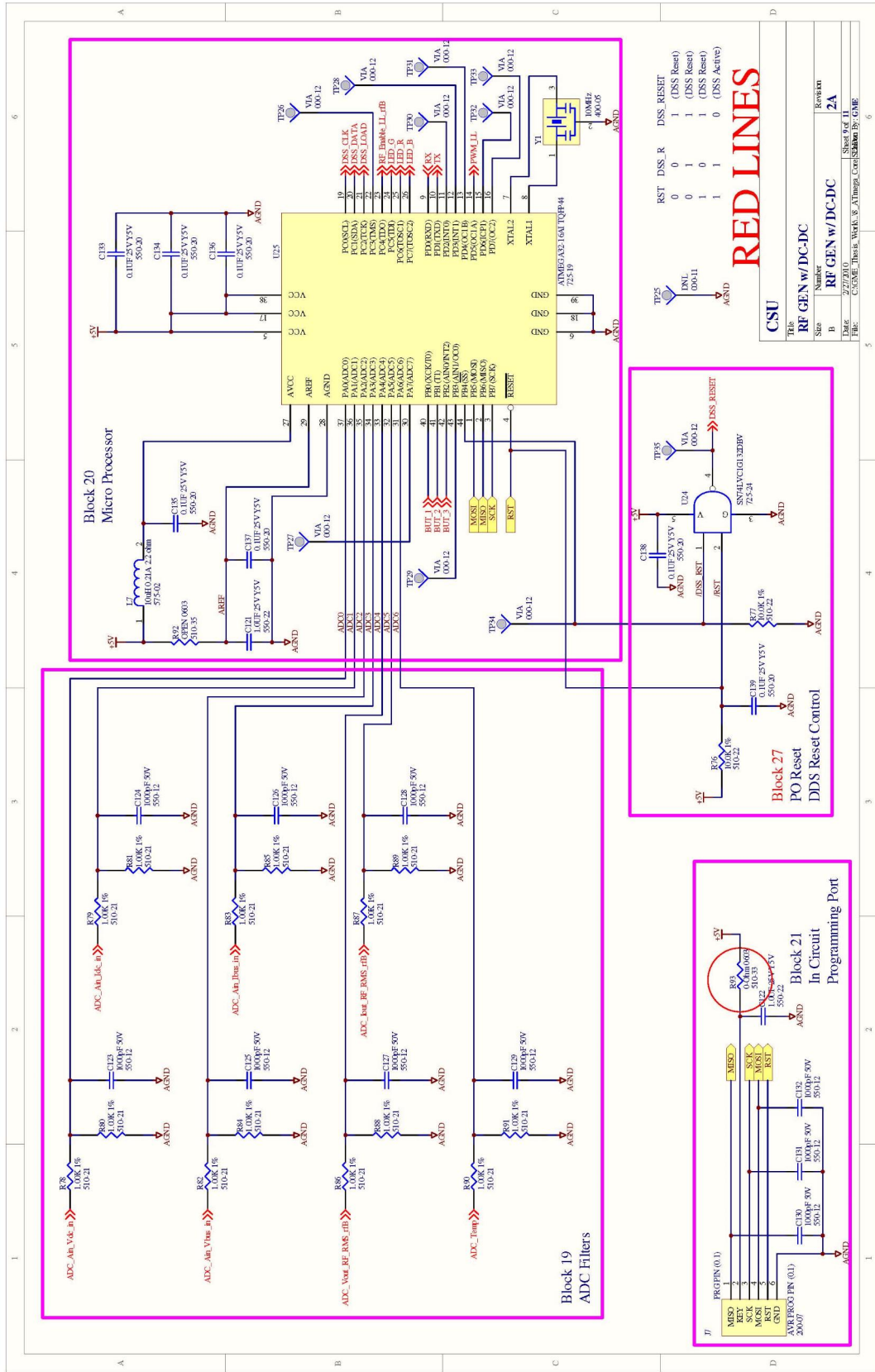
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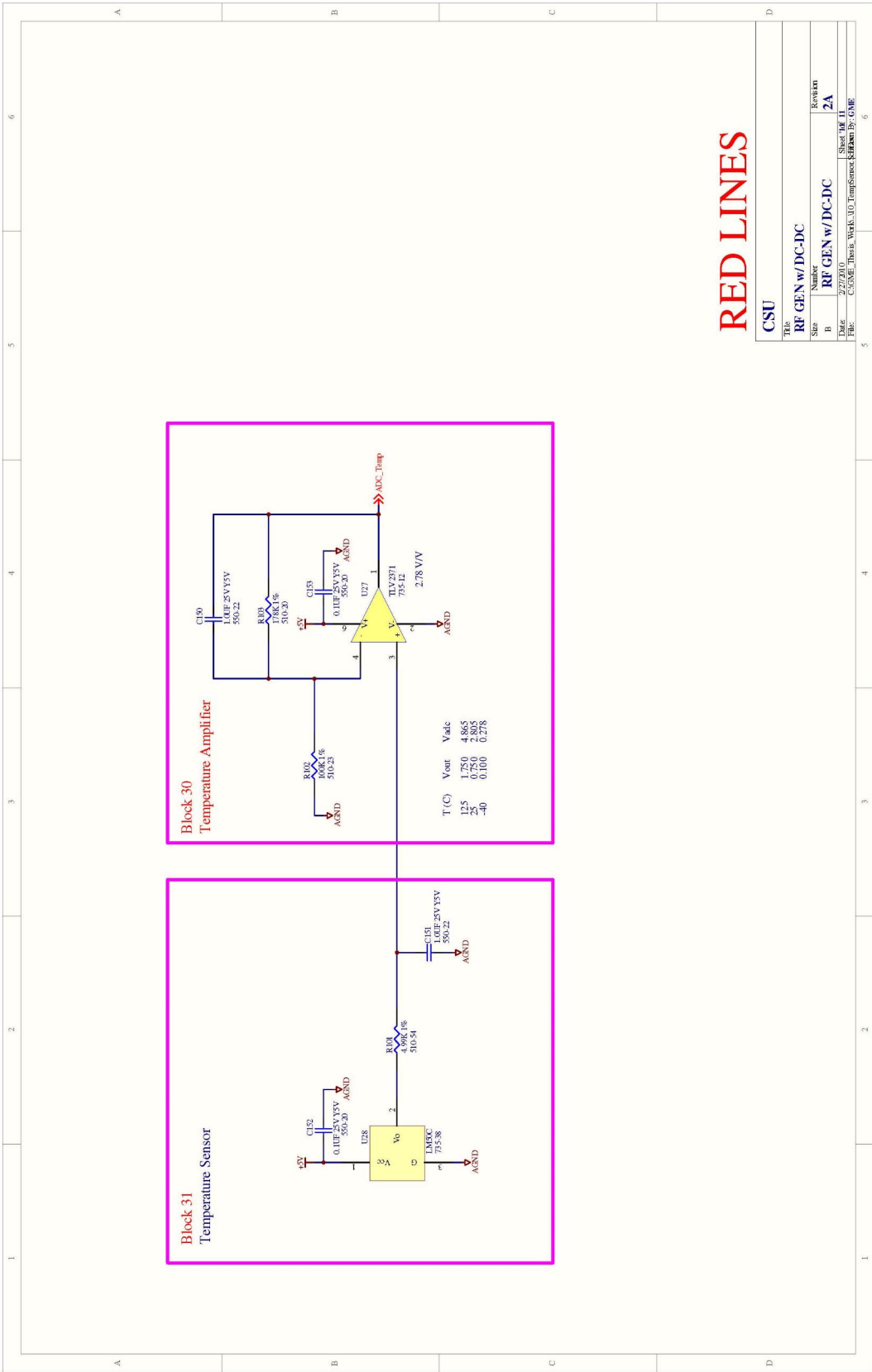


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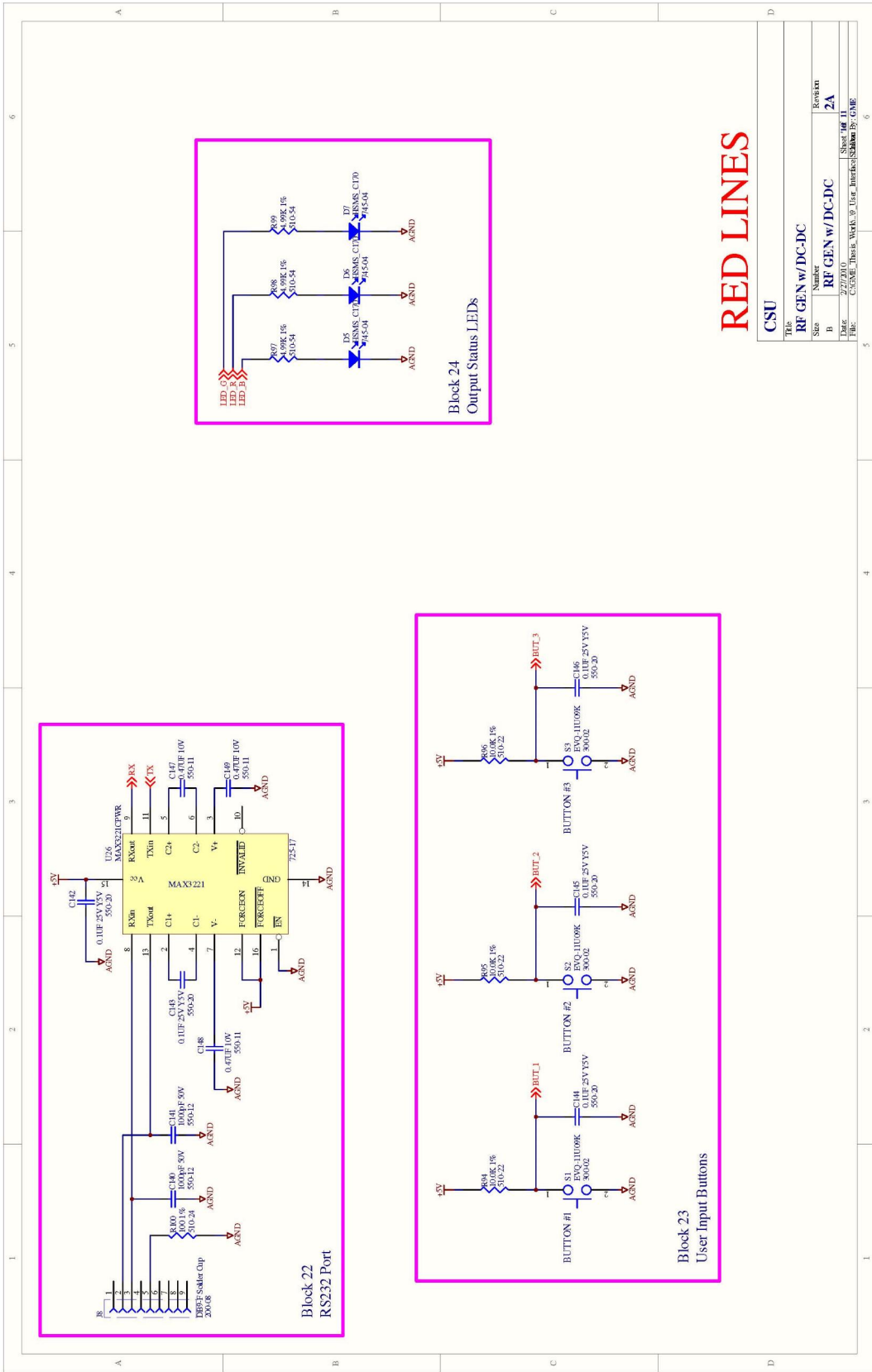
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