DISSERTATION

PERFORMANCE AND METASTABILITY OF CdTe SOLAR CELLS WITH A Te BACK-CONTACT BUFFER LAYER

Submitted by

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ABSTRACT

PERFORMANCE AND METASTABILITY OF CdTe SOLAR CELLS WITH A Te BACK-CONTACT BUFFER LAYER

Thin-film CdTe photovoltaics are quickly maturing into a viable clean-energy solution through demonstration of competitive costs and performance stability with existing energy sources. Over the last half decade, CdTe solar technology has achieved major gains in performance; however, there are still aspects that can be improved to progress toward their theoretical maximum efficiency. Perhaps equally valuable as high photovoltaic efficiency and a low levelized cost of energy, is device reliability. Understanding the root causes for changes in performance is essential for accomplishing long-term stability.

One area for potential performance enhancement is the back contact of the CdTe device. This research incorporated a thin-film Te-buffer layer into the contact structure, between the CdTe and contact metal. The device performance and characteristics of many different back contact configurations were rigorously studied. CdTe solar cells fabricated with the Te-buffer contact showed short-circuit current densities and open-circuit voltages that were on par with the traditional back-contacts used at CSU. However, the Te-buffer contact typically produced $\sim$2% larger fill-factors on average, leading to greater conversation efficiency. Furthermore, using the Te buffer allowed for incorporation of $\sim$50% less Cu, which is used for p-type doping but is also known to decrease lifetime and stability. This resulted in an additional $\sim$3% fill-factor gain with no change in other parameters compared to the standard-Cu treated device.

In order to better understand the physical mechanisms of the Te-buffer contact, electrical and material properties of the Te layer were extracted and used to construct a simple energy band diagram. The Te layer was found to be highly p-type ($>10^{18}$ cm^{-3}) and possess a positive valence-band offset of 0.35-0.40 eV with CdTe. An existing simulation model incorporating the Te-layer properties was implemented and validated by comparing simulated

results of CdTe device performance to experimental values. The Te layer improves performance is attributed to a reduction in the downward energy band bending between the CdTe and typical contact metals.

The stability, or rather the metastability, of CdTe solar cells was also studied with a focus on the Te back contact. A metastable device has a series of quasi-stable local energy-minimuma which the device may transition among. This work primarily focused on changes, both beneficial and detrimental, caused by diffusion and drift of atoms in the CdTe lattice. As atoms moved and/or became ionized their defect states were shifted, which resulted in changes in the CdTe doping and recombination.

Changes in performance for devices in equilibrium and under stress conditions were analyzed by electrical and material characterization. Mobile impurities and mechanisms responsible for the changes were identified—primarily the migration of interstitial Cu and Cl. The stability of CdTe solar cells with different back contacts were compared. It was found that any contact that included the Te layer was almost always more stable than the traditional contact used at CSU, most likely because of less sensitivity to the impurity profiles in the CdTe. Moreover, the Te contact configuration that introduced the least amount of Cu into the CdTe was discovered to be the most stable, both in storage and under stress conditions.

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INTRODUCTION

1.1 Motivation

Over the past century, the earth has seen a significant increase in average global temperature. The International Panel on Climate Change (IPCC), an intergovernmental body tasked with assessing the impact of climate change (comprised of thousands of scientists from across the globe), has reported that the continued rise in temperature will have an exceedingly detrimental impact on water supply, food production, and the overall well-being of society as a whole [1]. Additionally, the IPCC concluded that it is "*virtually certain* [99% probability] that human influence has warmed the global climate system," greatly due to the emission of CO_2 and other greenhouse gases (GHG) from the combustion of fossil fuels for energy sources [2].

Humans have very likely already caused irreversible damage to the planet. However, in order to prevent major deleterious consequences, the average global temperature increase must remain below 2°C relative to the pre-industrial era. Common scenarios to realistically meet this guideline require decreasing carbon emissions to 40 - 55% of 2010 levels by 2050 and to 90-100% of 2010 levels by 2100 [3]. This may be employed by replacing existing GHG-producing energy sources with significantly-reduced or, ideally, zero GHG emission energy sources, such as photovoltaic (PV) solar cells.

PV devices produce energy by directly converting photons into electricity. Energy generated from PVs produces no GHGs and requires zero moving parts. However, for solar cells to be a feasible energy source they need to demonstrate competitive cost and performance stability compared to existing energy sources [4, 5]. This work will discuss various studies with the purpose of gaining a new understanding of performance enhancement and metastability in PV solar cells based around a CdTe absorber layer.

1.2 PV Basics

To begin, a review of basic concepts helpful for understanding the physics of a photovoltaic device will be presented. This section introduces the fundamental building blocks of solar cells and the mechanisms by which light is converted to useful electricity.

1.2.1 Semiconductors

Semiconductor materials are crystalline solids that have bands of continuous energy states as a result of their repeating lattice structure. These energy bands are made up of closely spaced electron states. For any semiconductor there exists an energy range with no allowed states. The energy bands below this range are called the valence bands and the bands above are the conduction bands. The difference between the highest point on the valence band (E_V) and the lowest point on the conduction band (E_C) is called the band gap (E_g) (see Fig. 1.1).

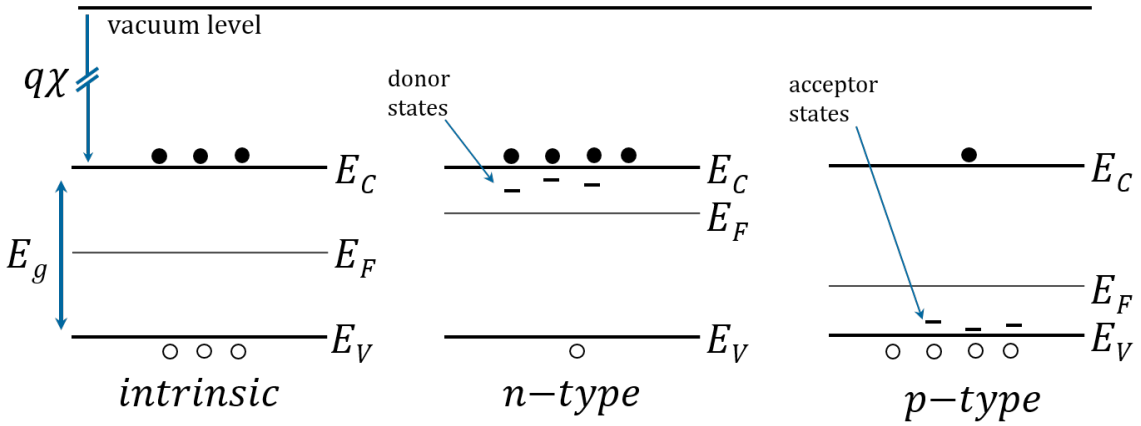

Figure 1.1: Energy band diagrams of (a) intrinsic, (b) n-type, and (c) p-type semiconductors. E_V is the valence band maximum, E_C is the conduction band minimum, E_F is the Fermi level, E_g is the band gap, and χ is the electron affinity. Hypothetical donor and acceptor states are also shown.

For a given temperature, electrons may occupy energy states in the valence and conduction bands. When an electron moves from one state to another, it leaves behind an empty

space called a hole. Holes are treated as pseudo-particles with opposite charge as electrons. The Fermi level (E_F) controls the probability energy states will be occupied by these charge carriers and is defined as the level of energy at which states have a 50% probability of being filled with an electron. The relationship between the concentrations of electrons (n) (holes (p)) and the Fermi energy is given in Eq. 1.1 (1.2),

$$n = N_C \exp\Big(- \frac{E_C - E_F}{kT} \Big), \tag{1.1}$$

$$p = N_V \exp\Big(- \frac{E_F - E_V}{kT} \Big), \tag{1.2}$$

where k is the Boltzmann constant, T is absolute temperature, and $N_{C,V}$ are the density of states for the conduction and valence bands, respectively [6]. Note that Eq. 1.1 (1.2) were calculated by approximating the Fermi-Dirac integral for $E_F - E_C > -kT$ ($E_V - E_F > -kT$).

For a semiconductor with negligible crystal defects and impurities, the number of holes and electrons are equal and the Fermi level is near the middle of the energy band gap (Fig. 1.1a). Adding impurity atoms will create additional energy states that may be present within the forbidden energy gap. A state that is unoccupied when neutral and a couple factors of kT near E_V will likely accept an electron and create a mobile hole in the valence band, which increases p and shifts E_F closer to E_V (Fig. 1.1b). Similarly, a state that is occupied when neutral and a couple factors of kT near E_C will likely donate an electron and add a mobile electron to the conduction band, which increases n and shifts E_F closer to E_C (Fig. 1.1c). Impurity states that increase p (n) are called acceptor (donor) dopants and create a p-type (n-type) semiconductor.

The electron affinity (χ) is also labeled in Fig. 1.1, which is the energy required to move an electron from the conduction band to the vacuum level (outside of the semiconductor). This is similar to the work function (Φ_M) in metals, which is the energy to move an electron from the Fermi level to the vacuum level, however the Fermi level and conduction band coincide at the same position in metals. These values are useful when constructing energy band diagrams with different materials.

1.2.2 P-N Junction Diode

Putting an n-type and p-type semiconductor in contact with each other forms a p-n junction diode, which is the basis for most photovoltaic solar cells. This can either be a homojunction, where both the n-type and p-type materials are the same, or a heterojunction, where they are different materials. Due to the difference in electron concentration of the materials, the electrons from the n-type side will diffuse towards and recombine with holes on the p-type side. This leaves behind positively charged ion cores on the n-type side and creates an electric field pointing towards the p-type side. Diffusion occurs until the Fermi levels of the materials align, i.e. the created electric field is strong enough to negate any further electron diffusion (Fig. 1.2).

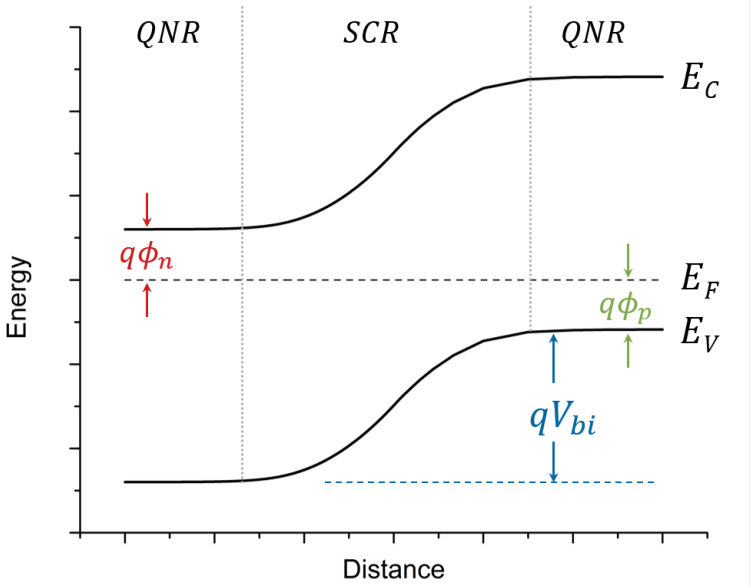

Figure 1.2: Energy band diagram of a p-n junction at equilibrium. V_{bi} is the built-in potential due to the band bending from equating Fermi levels. ϕ_n is the difference between E_C and E_F on the n-type side and ϕ_p is the difference between E_F and E_V on the p-type side. The space-charge region (SCR) and quasi-neutral regions (QNR) are also labeled.

Any charged particle in the field is quickly swept out, ideally for a solar cell electrons in the conduction band move towards the n-type side and holes in the valence band move towards the p-type side. This area is called the space-charge region (SCR) or depletion

region. The built-in potential from the SCR of a homojunction is shown in Fig. 1.2 and represented by Eq. 1.3,

$$V_{bi} = \frac{E_g}{q} - (\phi_n + \phi_p), \tag{1.3}$$

where ϕ_n is the potential difference between E_C and E_F of the n-type side and ϕ_p is the potential difference between E_F and E_V of the p-type side. In terms of carrier densities of the semiconductors,

$$V_{bi} = \frac{kT}{q}\ln\Big(\frac{n_n p_p}{n_i^2}\Big), \tag{1.4}$$

where n_n is the majority (electron) carrier density from the n-type material, p_p is the majority (hole) carrier density from the p-type material, and n_i is the intrinsic carrier density of the undoped material. The remaining area without an electric field is referred to as the quasi-neutral region (QNR).

Making electrical contact to the p-n junction and applying a voltage bias will inject additional carriers into the material. The p-n junction is no longer in equilibrium and each carrier now has its own quasi-Fermi level, designated E_{Fn} for electrons and E_{Fp} for holes. This effectively changes the built-in potential of the SCR. At zero voltage bias, recombination of electrons and holes is equal, and zero net current flows. A forward bias on the junction reduces the barrier to carriers, and current increases exponentially with bias. Reverse bias increases the depletion width, which decreases recombination, and the current approaches the saturation current density (J_0). The recombination current or diode current (J_d) in a p-n junction at a given voltage bias (V) is expressed by the diode equation (Eq. 1.5),

$$J_d(V) = J_0\Big[\exp\Big(\frac{qV}{AkT}\Big) - 1\Big], \tag{1.5}$$

where q is the elementary charge, k is the Boltzmann constant, T is absolute temperature, J_0 is the saturation current, and A is the diode ideality factor, which is related to the dominant recombination process (J_0 and A will be discussed in more detail later) [7].

Whenever light is incident on a p-n junction, photons with energy of at least E_g can excite an electron from the valence band into the conduction band, creating an electron-hole pair. This also creates non-equilibrium conditions and causes the respective carriers to have their own quasi-Fermi level. Ideally, for a solar cell, these photogenerated carriers will be separated by the internal field and recombine through an external circuit. The collection of photogenerated carriers is the light generated current (J_L) and is in the opposite direction as the diode current. The total current is then $J(V) = J_d(V)$ - $J_L(V)$.

Electrons and holes can recombine in many ways before they reach their respective contacts. The rates of recombination mechanisms can greatly affect the diode and light-generated current. There are three main types of recombination in semiconductors: radiative, Auger, and defect-related. Radiative recombination occurs when an electron relaxes from the conduction band to the valence band and emits a photon. Auger recombination is a non-radiative process by which energy from one carrier is transferred to another carrier in its respective band. Defect recombination is when carriers recombine (non-radiatively) through defect states near the middle of the band gap and is typically categorized by the region in the device where the defect occurs: SCR, QNR, or interfacial [6, 7]. In polycrystalline CdTe heterojunction solar cells, defect recombination is the dominate process and is a critical mechanism for loss of performance [8, 9].

The diode ideality factor (A) is related to the region in the material where the recombination is occurring. A value of 1 indicates that majority of the recombination takes place in the QNR. As recombination in the SCR becomes dominant, the value of A approaches 2 [7, 10]. The saturation current (J_0) is also affected by recombination. It can be expressed by,

$$J_0(V) = J_{00}\exp\Big(-\frac{E_a}{AkT}\Big), \tag{1.6}$$

where E_a is an activation energy and J_{00} is the reference current density [7]. The activation energy is associated with interface recombination, which is typically only a problem in heterojunction devices where the n- and p-type semiconductors are different materials. If the

value of E_a is near the E_g, bulk recombination is the primary mechanism. For values of E_a that deviate from E_g, then interface recombination due to band alignment and/or interfacial defects are the dominate processes [7].

To summarize, the fundamental structure needed for a photovoltaic solar cell has been outlined along with the processes for current generation, recombination and transport. Next, the detailed device structure, materials, and processes used to fabricate the CdTe solar cells studied in this work will be covered.

1.3 CdTe Solar Cells

CdTe-based solar cells are an appealing technology due to their low cost, low energy payback time (EPBT), and relatively quick and simple fabrication processes [4, 11, 12]. In comparison to crystalline Si (c-Si), which makes up majority of the global market share, the cost of CdTe modules is less per watt (0.65 $/W versus 0.51 $/W, respectively, as of 2015) [4]. The EPBT is the time required to produce the equivalent energy that was invested in the solar cell throughout its lifetime, including manufacturing, installation, and decommission. For c-Si modules, the EPBT is ∼2 years, whereas it is only a half a year for CdTe modules [11]. In comparing the fabrication processes of c-Si and CdTe, the full process time for a c-Si panel is ∼3 days, as compared to only ∼3.5 hours for a CdTe panel [13]. These are just a few of the attractive advantages of CdTe solar cells.

The following sections give details about the device structure and important fabrication process steps of the CdTe solar cells discussed in this work. Physical layers and processing treatments will be outlined and their effects on device performance will be discussed. The devices for this work were fabricated by the author unless otherwise noted.

1.3.1 CdTe Device Structure

All of the semiconductor layers in the devices are polycrystalline, meaning they are composed of numerous *grains* of the a crystalline material, in a various crystallographic

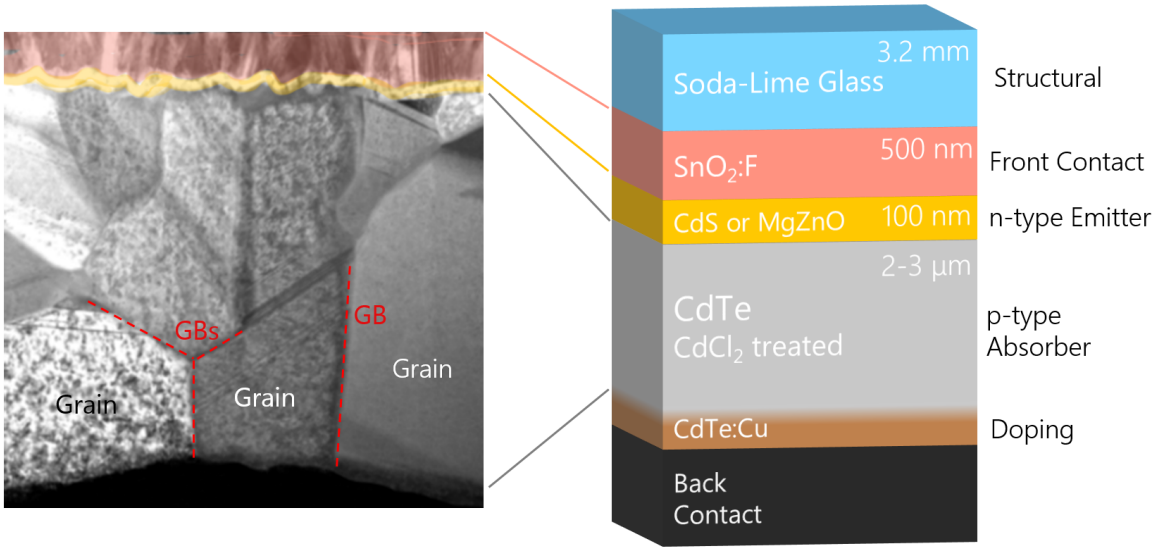

Figure 1.3: Cross sectional TEM image (provided by Amit Munshi) with selected grains and grain boundaries (GB) of the polycrystalline CdTe labeled (left). Illustrated diagram (not to scale) of CdTe solar cell structure (right). The SnO_2:F, MZO, and CdTe layers are shaded correspondingly on the image (left) and diagram (right).

orientations, that are adjacent to each other (see Fig. 1.3). The grains are separated by a *grain boundary* (GB) which is the interface where crystallites of different orientations meet. The solar cells discussed in the work are p-n heterojunctions with CdTe serving as the p-type absorber and either CdS or MgZnO (MZO) as the n-type window layer. The devices were fabricated in superstrate configuration, in which the layer that light enters also serves as the structural support. Fig. 1.3 (right) illustrates the basic device structure. Each of these layers will be discussed in the following sub-sections.

Glass/Transparent Front Contact (SnO_2:F)

The glass and transparent front-contact layers are coupled together since the glass used in this work is pre-coated with a transparent conducting oxide (TCO) that serves as the front contact. The product is commercially available from Pilkington as TEC glass. The glass is 3.2-mm-thick low-iron, soda-lime glass. The TCO is fluorine-doped tin oxide (SnO_2:F)

which is a highly-transparent ($E_g > 3.5\ eV$) n-type semiconductor with relatively low sheet resistance (10-12 $\Omega/\square$) [14, 15, 16]. Thus, SnO_2:F serves as a good material for a transparent front contact in the superstrate configuration.

n-type Layer (CdS or MgZnO)

The emitter (or window) layer has the primary function of being the n-type semiconductor for the p-n junction. Due to limits in doping CdTe (see section 1.3.1), the n-type carrier density is generally a few orders of magnitude higher than the p-type CdTe layer. From charge balance, the majority of the depletion layer (i.e. the internal field) resides in the CdTe [6]. Photogenerated carriers created from absorption in many emitter layers are very unlikely to be collected, therefore the emitter layer should be as transparent to the solar spectrum as possible. Additionally, since the heterojunction interface will have many defects and be prone to recombination, the conduction band offset (CBO) is important. A negative CBO will lower the energy difference between the emitter conduction band and the absorber valence band. This facilitates recombination at the interface before the carriers can be collected by the TCO. Having no or a small (<0.3 eV) positive CBO, will greatly reduce interface recombination and increase performance [17]. In this work, devices fabricated with one of two emitter layers will be discussed.

CdS has been the standard emitter layer in CdTe-based solar cell research for over 30 years [18]. However, CdS limits device performance due to its band gap of 2.4 eV, which allows absorption of wavelengths of less than 520 nm [7]. It also has a negative CBO of ∼-0.1 eV with CdTe [19]. In recent years there has been much effort to replace the CdS with a wider band gap material with a more favorable CBO. However, many of the devices in this work utilize a CdS emitter layer.

Using the MZO layer is a relatively recent advancement in CdTe solar cells. Based on the work of Kephart et al. [20], MZO both has a wide band gap (∼3.5 eV) and a positive CBO with CdTe (∼0.2 eV), which allows for greater absorption of photons in the CdTe and

less interface recombination. The MZO is less n-type than CdS and is better classified as a buffer layer rather than an emitter layer.

p-type Absorber Layer (CdTe)

CdTe is favorable material to use as an absorber in a photovoltaic device due to its high absorption coefficient and band gap of 1.5 eV. Based on Shockley-Queisser analysis of the limits on PV conversion efficiency, the CdTe band gap is near to the maximum theoretical value (1.4 eV is ideal) for the solar spectrum [21]. The high absorption coefficient means that less material is required for full absorption of the solar spectrum. Figure 1.4 (red curve) shows the CdTe absorption coefficient (α) verses wavelength. Also plotted is the thickness of CdTe required for 99% photon absorption at a given wavelength (blue curve). A thickness of only 2.5 μm is required to absorb a vast majority of sub-band gap photons.

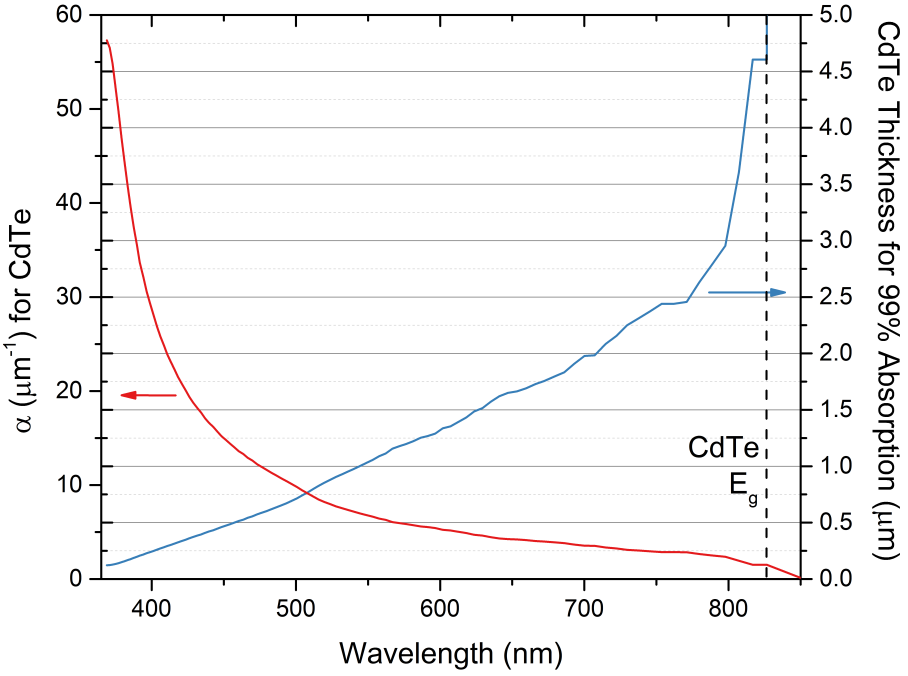

Figure 1.4: Absorption coefficient (α) of CdTe (left axis, red curve) and thickness of CdTe required for 99% absorpton of photos (right axis, blue curve) at each wavelength.

For intrinsic CdTe material, a vacant Cd (V_{Cd}) site in the lattice creates an acceptor state. Typically p-type CdTe is formed with Te-rich process conditions, to promote V_{Cd}.

However, a downside to Te-rich processing is the formation of the Te anti-site (Te_{Cd}), a non-shallow donor, which has been shown to be the most efficient recombination center of intrinsic defects in CdTe [22, 23]. CdTe typically requires post-depositions treatments to improve crystalline structure, passivate defects, and increase doping which will be discussed in the following sections.

Passivation (Cl Treatment)

The Cl treatment of CdTe is essential for good device performance under illumination. It is typically done at elevated temperature and/or in conjunction with an anneal to promote Cl diffusion and CdTe grain recrystallization. As-deposited CdTe at CSU has a very low photogenerated current, typically less than 1 mA/cm^2. After Cl treatment, the photogenerated current increases to greater than 20 mA/cm^2. Studies have shown that minority carrier lifetime is increased after Cl treatment [24, 25], however the exact mechanisms for the improvement are unclear. Additionally, many studies have shown that majority of the Cl segregates to the grain boundaries [26, 27, 28, 29, 30, 31, 32, 33, 34]. Abbas el at. showed that optimal Cl treatment and anneal removed numerous stacking fault defects in grain interiors and any remaining defects were twin boundaries [28, 29, 30, 31, 32, 33]. Yoo et al. found that stacking faults will act as hole traps [35], thus their removed would be beneficial. C. Li et al. found that Cl subsitutes for a large portion of Te within a few unit cells of the grain boundary and effectively dopes the grain boundaries n-type [36]. H. Li et al. found that n-type (Cl-doped) GBs, including twin boundaries in grains, enhanced charge separation and electron transport to the front contact [37]. Krasikov et al. showed that the pairing of an intersitial Cl atom with the Te anti-site ($\mathrm{Cl_i} - \mathrm{Te_{Cd}}$) is one of the most stable complexes after Cl treatment. It has been postulated that this complex has a much lower recombination efficiency than that of the dominate recombination center of $\mathrm{Te_{Cd}}$ [22]. To summarize, the Cl treatment reduces large-scale, lifetime-killing defects in grains, segregates to the grain boundaries and dopes them n-type which aids in charge separation, and potentially passivates the Te anti-site recombination center.

Extrinsic Doping (Cu)

The Cu treatment is done to improve the bulk CdTe doping along with highly-doping the back of the device (more on this in the next section). As opposed to Cl, Cu does not greatly segregate to the grain boundaries. Mao et al. measured the Cu distribution to be uniform in polycrystalline CdTe that was not Cl-treated [26]. In Cu- and Cl-treated CdTe, Poplawsky et al. found some evidence of Cu segregation in the grain boundaries but only near the back of the device [38]. Cu is a group IB dopant and will substitute for Cd (Cu_{Cd}) as a non-shallow acceptor, with reported energies of $0.22 - 0.31$ eV above E_V [39, 40]. After Cu treatment at CSU, the atomic concentration in the bulk CdTe is on the order of $10^{17} - 10^{18}$ cm^{-3}, however the CdTe carrier concentration is typically on the order of 10^{14} cm^{-3}. This is typically attributed to self-compensation with interstitial Cu (Cu_i) [25, 41, 42], which is a shallow donor [39]. Cu_i has also been found to be highly mobile in CdTe, even at room temperature [40], which leads to stability issues. In addition to self-compensation, Cu_{Cd} is also compensated by Cl_i, which forms the energetically favorable and most stable Cu complex in CdTe: $(Cl_i - Cu_{Cd})^{2+}$—a double donor [22]. Thus, p-type Cu-doping in CdTe, especially in Cl-treated samples, should be severely limited.

Another downside to Cu inclusion in CdTe is the reduction in carrier lifetime [25, 41, 43, 44]. Conventional wisdom says that midgap defects formed by complexes with Cu are the source of lower lifetime. However, Kuciauskas et al. found that the non-shallow, acceptor state of Cu_{Cd} can also limit lifetime [44]. Despite all of the issues with Cu in CdTe, the best performing CdTe devices have been fabricated with this method of doping.

Back Contact

A few different materials and schemes were used in the work to form the back contact and will be discussed in more detail in Section 2.2. This section outlines the problems of forming the back contact and common methods to mitigate these issues.

Making a low-resistance, ohmic contact with CdTe is a challenge. Whenever a metal has contact with a semiconductor an energy barrier is typically formed at the interface. The size of the barrier is given by:

$$\phi_b = \chi + \frac{E_g}{q} - \Phi_M, \tag{1.7}$$

where ϕ_b is the barrier height, χ is the electron affinity of the semiconductor, E_g is the band gap energy and Φ_M is the work function of the metal [6]. Due to CdTe's electron affinity (4.3 eV) and band gap (1.5 eV), a metal with a work function of 5.8 eV or higher is required for ohmic contact (see Fig. 1.5a) [45]. Essentially all feasible metals have a work function below 5.8 eV, which causes downward band bending. Typical contacting metals, such as Ni or Au, have work functions of ∼5.2 eV, which will create a Schottky barrier of ∼0.6 eV as shown in figure 1.5b. This can impede photogenerated hole current and increase the forward electron current, both of which are detrimental to performance.

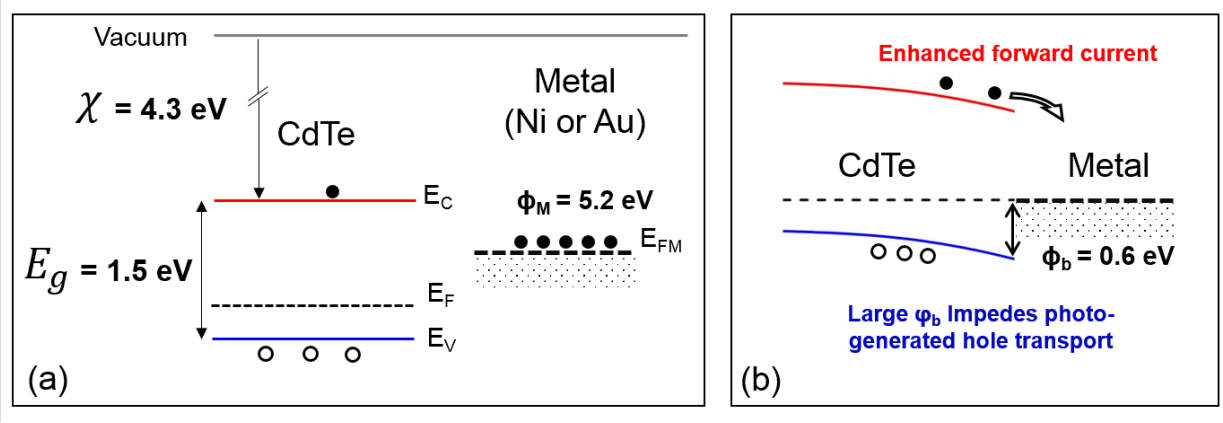

Figure 1.5: Energy diagrams of CdTe and a typical back contact metal (a) before contact. The electron affinity (χ) and band gap (E_g) of CdTe are labeled along with the work function (ϕ_m) of a typical contact metal (Ni or Au). Schottky barrier formation at the interface of the CdTe and metal (b). (Figures modified from Tao Song)

In addition to downward band bending at the back from the metal/semiconductor junction, the CdTe surface is typically riddled with defects much like the GBs, thus is a source for much recombination and likely pins the Fermi level further away from the valence band.

Two main techniques are used make a good back contact are: highly doping the back of CdTe and/or using a buffer layer that has a favorable band alignment with CdTe and the metal. The high doping at the back will raise the bands and reduce the forward electron current. An ideal buffer material should have no or a small VBO and a positive CBO and/or high p-type doping to reduce band bending. Many of the devices discussed in this work will have a C and Ni back contact on Cu-treated CdTe. The bulk of this work also discusses using a Te buffer layer deposited on the back of CdTe (discussed in detail in chapter 2).

1.3.2 Device Fabrication

The devices used in this work were fabricated at Colorado State University in the Materials Engineering Lab. The majority of the process occurred inside a single vacuum chamber with multiple close-space-sublimation (CSS) sources, to house the CdS, CdTe, $CdCl_2$, CuCl and appropriate anneal stations. The chamber is in a nitrogen environment at an operating pressure of 40 mTorr. The process begins with the deposition of 100 nm of either CdS or MZO on the 3.1" x 3.6" glass/SnO_2:F substrate. The MZO layer is deposited via sputtering, described in detail by Munshi et al. [46], whereas the CdS would be done in the CSS vacuum chamber. Next the CdTe absorber layer of approximately 2-3 μm is deposited by CSS.

Immediately following the CdTe deposition, Cl is introduced into the film with a vapor treatment from a $CdCl_2$ source at 435°C for 3 minutes and a 400°C anneal for an additional 3 minutes. After this treatment the device is cooled and brought out of vacuum to rinse (with deionized (DI) water) the excess $CdCl_2$ that condensed on the surface as the substrate cooled in the $CdCl_2$ vapor. All devices in this work received the $CdCl_2$ as described. The sample returns to the same vacuum chamber for Cu treatment, which consists of a reheating at 330°C for 75 seconds, a reactive treatment of CuCl at 190°C for 110 seconds, and an anneal at 200°C for 220 seconds. These times and temperatures are referred to as the "standard Cu treatment" at CSU. However, in some of this work, the CuCl treatment time will be varied and will be noted if so. The sample is also rinsed in DI water following the Cu treatment.

Devices that received the Te buffer layer are transfered to a high-vacuum chamber with a pressure of less than 10^{-5} Torr. The Te is evaporated from a heated tungsten boat at a rate of $\sim$1 nm/s on a room temperature substrate. The device is completed by adding a layer of C paint (optional with the Te layer) followed by a layer of Ni paint for the back contact. Ni paint alone has difficulties adhering to the CdTe surface, whereas the C does not. The C behaves like carbon-black materials which have work functions in the range of $5.3 - 5.65$ eV [47], thus greater than Ni (5.2 eV). The Ni creates a thicker contact, with lower sheet resistance, that is mechanically robust and can handle being repeatedly measured numerous times. In one case, sputtered metallic nickel was used as the back contact. Lastly, the substrate is generally delineated into 9 or 25 small area devices of approximately 0.6 cm^2 each.

Samples used for materials characterization, such as secondary ion mass spectrometry (SIMS), omitted the paint contacts on a subset of cells. The Te films used for Hall measurements were deposited to CdTe/MZO/plain glass, Cu-treated CdTe/MZO/plain glass, and glass only.

A more detailed discourse of the fabrication process can be found in the article by Swanson et al. [48].

1.4 Solar Cell Characterization

This section gives an overview of the relevant measurements used to characterize electronic and material properties of a CdTe solar cell.

1.4.1 Current Density versus Voltage (J-V)

Measurement of the current density over a span of applied DC voltage (J-V) is the fundamental measurement to analyze solar cell performance. It is typically measured at 25°C in the dark and under standard illumination. Standard illumination conditions consist of an AM1.5G light source with a power density of 100 mW/cm^2 [49]. Figure 1.6 shows the

dark (solid green) and light (dashed green) J-V curves of a typical CdTe solar cell fabricated at CSU.

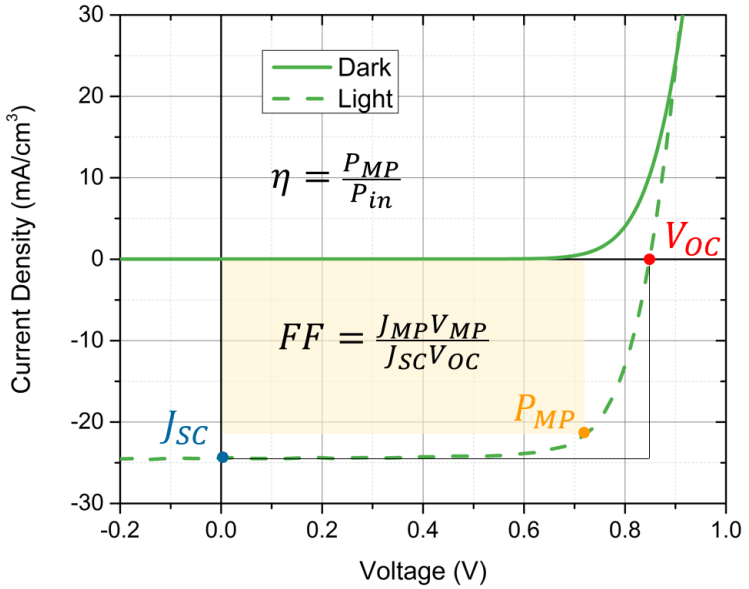

Figure 1.6: Dark (solid green) and light (dashed green) J-V curves of typical CdTe solar cell. The short-circuit current (J_{SC}), open-circuit voltage (V_{OC}), and maximum power point (P_{MP}) are labeled along with relations for fill factor (FF) and efficiency (η)

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There are several parameters that are cataloged for each device: open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), fill factor (FF), and the conversion efficiency (η). The J_{SC} is the current measured under illumination at zero voltage bias. For a well-behaved device, J_L is independent of voltage and equal to J_{SC}, (discussed further in Section 1.4.2). V_{OC} is the bias voltage at which no current flows and is directly related to V_{bi} (Eq. 1.3). The FF is the ratio of the maximum power point (P_{MP}) to the product of J_{SC} and V_{OC}. Visually, in Fig. 1.8, the FF is the area fraction of the yellow rectangle compared to the outlined rectangle. Parasitic resistances, in series R_s and/or parallel (shunt) r_{sh} to the junction, and defect recombination will negatively affect the FF. The efficiency is simply the ratio of P_{MP} to the input power density (P_{in}) of the light source. Putting all of this together, Eq. 1.8 can be used to describe the behavior of the measured J-V of a solar cell,

$$J = J_0 \exp\left[\frac{q(V - JR_s)}{AkT} - 1\right] - J_{SC} + \frac{V - JR_s}{r_{sh}}. \tag{1.8}$$

A comprehensive procedure for analyzing J-V data based on Eq. 1.8 to extract R_s, r_{sh}, A, and J_0 is found in Hegedus and Shafarman [49].

Temperature Dependent J-V

Measuring J-V at various temperatures (J-V-T) can reveal additional information about the device characteristics. By combining Eq. 1.8 and Eq. 1.6, for $V_{OC}/r_{sh} \ll J_{SC}$, the V_{OC} is:

$$V_{OC} = \frac{E_a}{q} - \frac{AkT}{q} \ln\Big(\frac{J_{00}}{J_{SC}}\Big). \tag{1.9}$$

From Eq. 1.9, we see the V_{OC} is temperature dependent. Extrapolating V_{OC} versus T to $T = 0$ will yield E_a for the device, i.e. information about interface recombination. Deviations of the V_{OC} versus T data from linearity, is an indication of temperature dependent ideality factor or reference current [7].

J-V-T analysis can also be used to extract the size of the back contact barrier of the device. The back barrier can have the effect of limiting hole current in forward bias and will become more pronounced as temperature is decreased. This behavior can be described by a model of two diodes in series, with the back diode in opposite polarity to the main junction [50]. The point where the current of the main junction is limited is called the *roll-over* point or turning current (J_t) and is approximately equal to the saturation current of the back diode (J_{b0}). Assuming thermionic emission is the dominate transport mechanism, J_{b0} can be written as,

$$J_{b0}(V) = A^* T^2 \exp\Big(-\frac{q\phi_b}{kT}\Big), \tag{1.10}$$

where A^* is the effective Richardson coefficient and ϕ_b is the back barrier, which can be extracted using the method by Koishiyev et al. [51].

1.4.2 Quantum Efficiency (QE)

The quantum efficiency (QE) at a given wavelength measures the ratio of collected electrons per incident photon on the device. It is useful for determining collection losses in the light-generated current. Losses can come from reflection at any surface, absorption in the glass, TCO, or window layer, incomplete absorption in the absorber layer, and incomplete collection of photogenerated carriers in the absorber. Figure 1.7 shows the QE of a typical MZO/CdTe device over a range of wavelengths. The losses from reflection and absorption from the layers prior to the absorber (glass, TCO, MZO) are labeled. From Fig. 1.7, for a typical solar cell made at CSU, ∼15% of the incident light does not reach the CdTe. Additional losses from unabsorbed photons due to insufficient CdTe thickness are shown in Fig. 1.7 (purple), as well as the losses due to recombination of photogenerated carriers in the device (dark blue). The sharp cut-off around 825 nm gives a good estimation of the CdTe band gap.

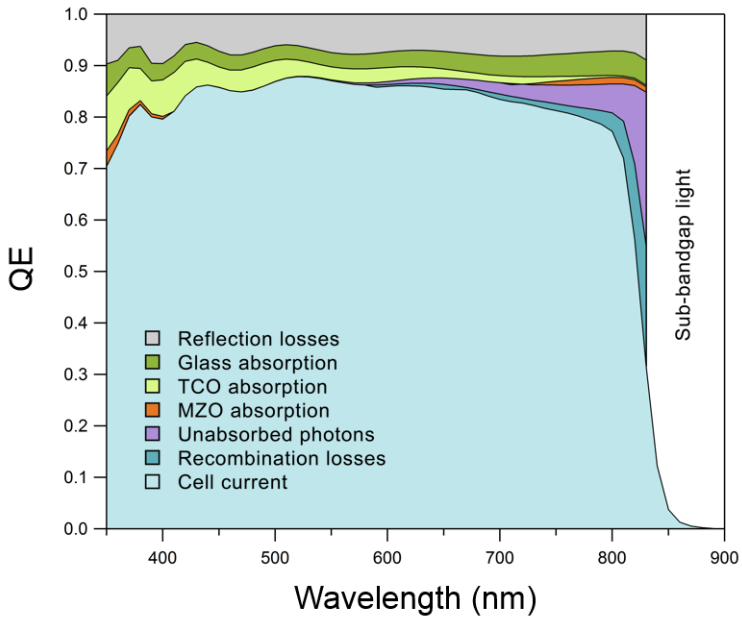

Figure 1.7: Quantum efficiency (QE) versus the wavelength for a MZO/CdTe solar cell with loss mechanisms labeled (data and figure from Anna Wojtowicz).

Based on the absorption coefficient of CdTe (Fig. 1.4), QE can be correlated to depth in the absorber region. For example, longer wavelength photons have a lower absorption and tend to get absorbed nearer the back of the CdTe, thus if there is a gain/loss in QE in the longer wavelength region (and there is sufficient absorber material) then there is likely a collection problem/enhancement near the back of the device

Furthermore, the J_{SC} of a device can be calculated by integrating the QE response multiplied by the AM1.5 solar spectrum (in units of photo-flux), shown in Eq. 1.11.

$$J_{SC} = q \int_0^{\infty} QE(\lambda) AM1.5(\lambda)\, d\lambda \tag{1.11}$$

1.4.3 Capacitance-Voltage (C-V) Profiling

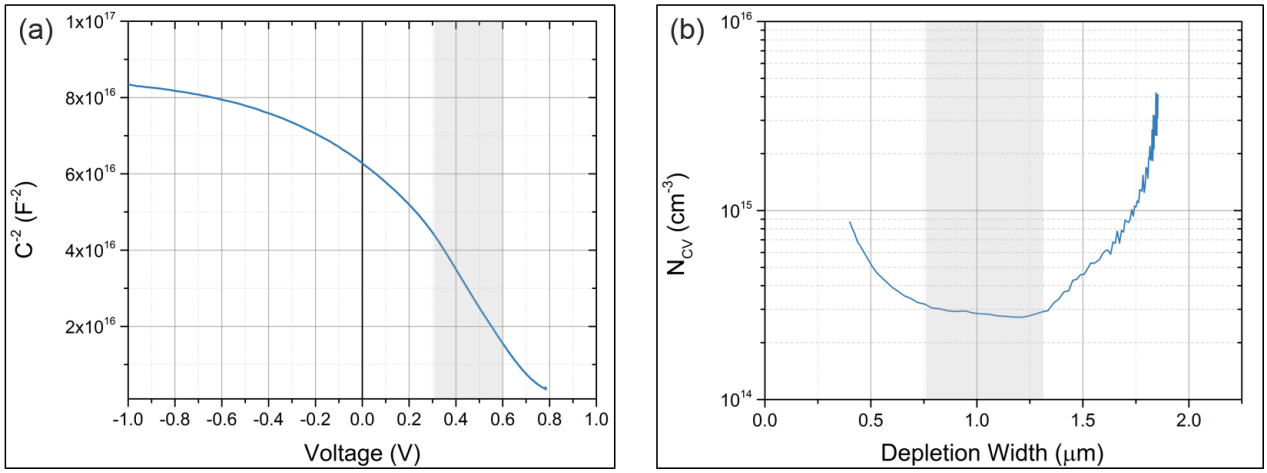

Figure 1.8: Plots of the (a) inverse capacitance squared (C^{-2}) versus voltage (V) and (b) the carrier density (N_{CV}), as calculated from C-V data, versus the depletion width W. The shaded portion of each plot indicated the region where the carrier density analysis fits the model.

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Capacitance-voltage (C-V) profiling is a useful characterization tool that allows the calculation of the carrier density over the depletion width of the absorber. The model is based on a parallel plate capacitor and assumes: a one-sided junction, the depletion width does not approach the film thickness, the material only has shallow defect states, and the back

contact barrier is negligible [10, 52]. For thin-film CdTe solar cells, only the approximation of a one-sided junction typically holds true, thus there are numerous artifacts introduced in analysis caused from deep-level defects, voltage-sharing with the back contact, and a fully-depleted absorber at zero bias. Nevertheless, it returns a good approximation of the bulk carrier density and the size of the depletion width at various voltage biases.

The capacitance effect originates from the charges at the depletion edge. For each DC-bias voltage, a small AC modulation voltage (20 mV, 100kHz) is applied and the impedance is analyzed. Like a good diode, in order to accurately measure capacitance a small series resistance and large parallel resistance is ideal. The capacitance (parallel plate model) is given as:

$$C = \frac{\epsilon\epsilon_0 A}{W}, \tag{1.12}$$

where ϵ is the dielectric constant of the material, ϵ_0 is the permittivity of free space, A is the area of the device, and W is the depletion width, which is given by

$$W = \left[\frac{2\epsilon\epsilon_0(V_{bi} - V)}{qN_{dp}}\right]^{\frac{1}{2}}, \tag{1.13}$$

where V is the bias voltage, q is the elementary charge, and N_{dp} is the carrier density in the depletion width [10]. Inserting Eq. 1.13 into 1.12 and rearranging yields,

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{\epsilon\epsilon_0 q A^2 N_{dp}}, \tag{1.14}$$

which, in ideal circumstances, should be linear over the entire voltage range. However, this is rarely the case for $\sim$2.5-μm CdTe, as shown in Fig. 1.8(a). For a typical, CdTe device the carrier density is 1×10^{14} cm^{-3} and the built-in potential is $\sim$0.8 V. For those values, the depletion width should be $\sim$3 μm, which is larger than the CdTe thickness of any device discussed in this work. A fully depleted absorber manifests itself in the $C(V)^{-2}$ plot as a small change (or even no change) in capacitance as voltage is changed. This effect is more amplified in devices with lower absorber doping. Additionally, if a back-contact barrier

is present, a forward bias with cause it to increase while the front junction is decreasing. Therefore, voltage sharing with the front and the back will result in a small change in $C(V)^{-2}$ as voltage is pushed further into forward bias [52].

The $C(V)^{-2}$ versus voltage plot can also provide information about additional potential barriers in the device along with interface/surface charges. A downward (or leftward) shift of $C(V)^{-2}$ without a change in slope indicates a reduction in a secondary potential drop in the device and/or an increased negative surface charge and vice versa [7, 53].

The area of the device is also crucial to the analysis. The area will affect the measured capacitance as seen from Eq. 1.12. It is also input in the calculations of carrier density and depletion width, thus if an incorrect value is assumed these value will be inaccurate.

Despite these issues with thin-film CdTe devices, the plot of Eq. 1.14 will show the voltage regions where the device does fit the model, i.e. when $C(V)^{-2}$ is linear and results in a uniform calculated carrier density, shown by the shaded region in Fig. 1.8(a). Changes in the slope of $C(V)^{-2}$ indicates a change in carrier density, e.g. a smaller slope corresponds to a larger carrier density. However, midgap states, that do not contribute to the free carriers in the device, may affect the measurement if they become occupied by a carrier during the measurement [52]. Eq. 1.14 is also in a convenient form to take a derivative with respect to voltage in order to extract the C-V carrier density (N_{CV}) (Eq. 1.15).

$$N_{CV} = -\frac{2}{\epsilon\epsilon_0 A^2}\left[\frac{d(C^{-2})}{dV}\right]^{-1} = -\frac{C^3}{\epsilon\epsilon_0 A^2}\left[\frac{dC}{dV}\right]^{-1} \tag{1.15}$$

The distinction between N_{dp} and N_{CV} comes from the model assumptions that thin-film CdTe does not meet. Generally, N_{CV} in the linear portion of the forward bias data will give an upper limit to the bulk carrier density. N_{CV} is typically plotted against W as calculated by rearranging Eq. 1.12, as shown in Fig. 1.8b. The shaded portion of Fig. 1.8b is the same range as Fig. 1.8a.

1.4.4 Hall Measurement

Hall measurements were performed at room temperature using an Ecopia HMS-3000 system with a 0.55-Tesla magnet. All samples were cut into 1.5 x 1.5 cm^2 squares for measurement. Probe currents of 1 and 10 μA were used. The van der Pauw method was used to extract the carrier concentration, hall mobility, and resistivity of the thin-films [54].

1.4.5 Secondary Ion Mass Spectrometry (SIMS)

SIMS measurements were done to measure atomic concentration depth profiles through the film stack. SIMS is a destructive measurement technique in which the counts of mass-to-charge ratio of ions sputtered off a sample (secondary ions) by a probing beam of ions (primary ions) are measured. The selected primary ion gives different probabilities of ionization of specific atom species, and thus it is chosen based on the bulk material composition and desired impurity species. For a CdTe matrix, O_2^+ is used to produce positive ions which are optimal to analyze Cu, and Cs^+ is used to produce the negative ions which are optimal to analyze Cl, O, and S. Ion counts can be converted to atomic concentration using a relative sensitivity factor (RSF) determined from a pure matrix of CdTe implanted with a known amount of the desired impurity element. The calculated concentration value from the RSF is only accurate in the bulk of the CdTe. Near the back surface and through of the emitter layer, the sputter rate is different and will have a different RSF value. However, comparison of raw ion counts can be made within the regions. The depth of the sputter crater is measured via step profilometry and the data is plotted as atomic concentration versus depth. All SIMS data presented in this work was measured by First Solar, Inc.

1.4.6 Spectral Photoluminescence (PL)

Spectral photoluminescence (PL) is the measurement of the light spectrum emitted from a device after exciting charges with a probing light source. The spectrum will give information about the radiative recombination in the device. Types of recombination likely to be seen

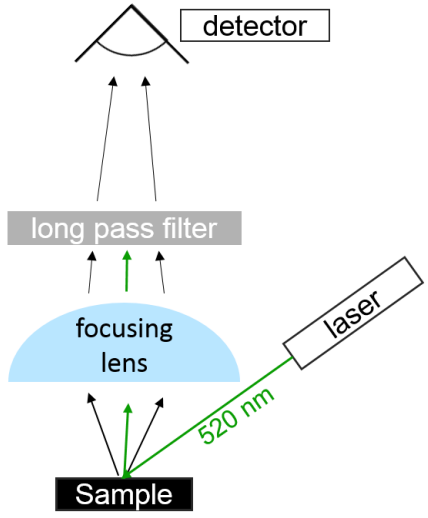

Figure 1.9: Illustrated diagram of CSU's spectral photoluminescence (PL) set-up. A laser excites the sample and a focusing lens collects the emitted PL photons. The light then passes through a long pass filter, to reduce noise from the probe laser, and is collected by the detector.

near room temperature are band-to-band, conduction-band-to-acceptor-state, donor-state-to-valence-band, and donor-state-to-acceptor-state. The intensity of the peaks in the spectra correlates to the number of charges recombining through that energy transition. The energy of the probing photons determines the depth of the material that is examined. For most cases, the probe depth is given by the inverse of the absorption coefficient ($\alpha(\lambda)^{-1}$) or the diffusion length of minority carriers (which ever is larger) [10]. In this work 520-nm and 660-nm light was used; giving a probe depth of approximately 125 nm and 240 nm, respectively. The diffusion length in polycrystalline CdTe has been measured between 400-500 nm [55, 56]. In higher lifetime devices, the diffusion length may even approach 1 μm, but regardless, this technique favors defects in the bulk and near the front interface with some possibility of capturing recombination towards the back of the device. Figure 2.24 show examples of PL spectra for CdTe devices fabricated in this work.

The PL set-up at CSU is shown in Fig. 1.9. The probing light is a 520 nm (2.38 eV) laser diode (Thorlabs L520P50) with a spot size of approximately 1 mm^2. It operates at

a power of ∼40 mW, which translates to an intensity of ∼4000 mW/cm^2 (∼40 suns). The luminescence is collected by a focusing lens and directed to a spectrometer (Ocean Optics IRRAD2000). Before reaching the spectrometer, the light passes through a 570 nm long pass filter to reduce the amount of the excitation signal in the data. All of these components are housed in a light-tight enclosure.

1.4.7 Electroluminescence (EL) Imaging

Electroluminescence (EL) is the emission of a photon by a semiconductor from the injection of charge carriers. EL will occur in CdTe solar cells by putting the cell in forward voltage bias. A fraction of the injected charges will recombine radiatively and emit a photon. The spatial EL response can be measured with an appropriate camera set-up. An EL image will essentially provide a map of the V_{OC} of the device. It is very useful for identifying non-uniformities defects from processing. A thorough discussion of EL imaging of CdTe solar cells and the experimental set-up at CSU can be found in work by Raguse [57].

EL measurements on CdTe solar cell discussed in this work were performed with the device operating in constant current mode at 40 mA/cm^2. The cells were imaged using a silicon CCD that was cooled to -25°C to reduce thermal noise. Using ImageJ software, the images were processed as follows: background subtraction, normalization by the current density and measurement time, set to a base 10 logarithmic scale, and a false color-map of the intensity was applied. Figure 2.7 shows examples of the processed El images of CdTe devices.

Chapter 2

TE BUFFER LAYER FOR THE BACK CONTACT OF CDTE SOLAR CELLS

This chapter provides an in-depth analysis of the physical mechanisms of the thin-film Te layer used in the back contact of CdTe solar cell devices. To begin, electron microscopy images will be presented to show the structure and continuous spatial coverage of the Te layer on the CdTe back surface. Next, the device performance and characteristics of many different back contact schemes will be studied in detail using J-V-(T), QE, C-V, EL, SIMS and PL measurements. The electrical and material properties of the Te layer will be extracted by measurement and calculation, discussed in detail, and used to construct a simple energy band diagram of the Te layer. Finally, a simulation model incorporating the Te-layer properties, which was used to validate itself by comparing simulated results of CdTe device performance to experimental values, is presented.

2.1 Microscopy of Te Layer

Figure 2.1 shows cross-sectional transmission electron microscopy (TEM) images along with electron dispersive spectroscopy (EDS) maps of Te and Cd for a typical SnO_2:F/MZO/CdTe/Te solar cell fabricated at CSU (by Amit Munshi). The TEM and EDS work was performed at Loughborough University, UK. The layer of Pt above the Te surface is required for sample preparation and was not part of the device structure. For details about sample preparation and the TEM/EDS measurement of CdTe solar cells, see work by Abbas [28].

The EDS atomic map of Te (Fig. 2.1b) clearly shows a continuous layer of Te (blue) at the back of the CdTe. The false Te signal in the SnO_2:F layer is from peak overlap of the Sn and Te signal. Comparing the Te atomic map to the Cd atomic map (Fig. 2.1c), there is no apparent interdiffusion at the CdTe/Te interface. A magnification of the CdTe/Te interface, shown in 2.1d, better renders the continuous, polycrystalline structure of the Te layer.

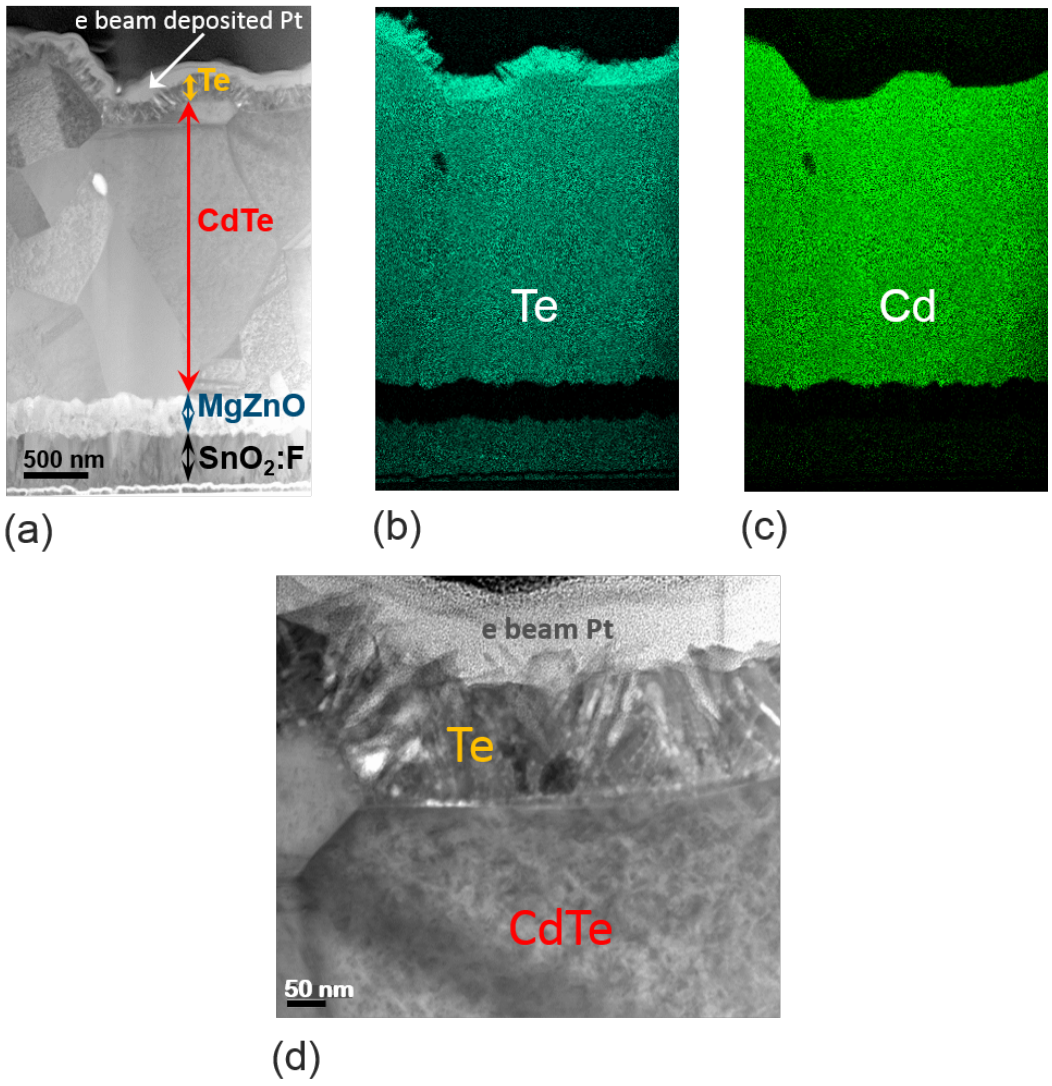

Figure 2.1: Cross-sectional transmission electron microscopy (TEM) and electron dispersive spectroscopy (EDS) atomic maps of an MZO/CdTe device with Te layer. (a) Cross section of full device with each layer labeled, (b) Te atomic map of full device, (b) Cd atomic map of full device, (d) magnified CdTe/Te interface cross section from (a). (Images rendered at Loughborough University, UK and modified from Amit Munshi)

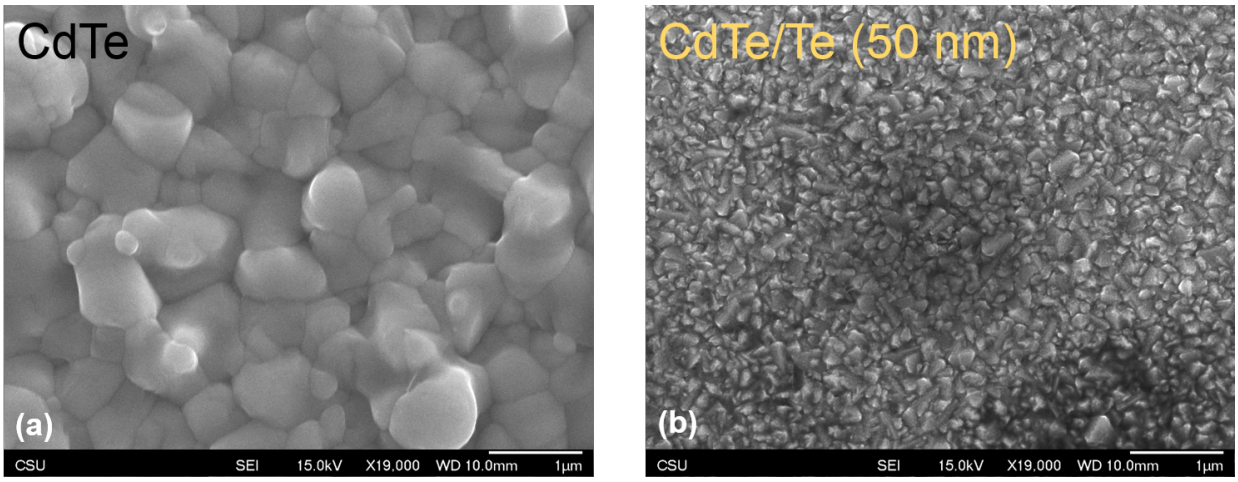

Figure 2.2: SEM images of the back surface of a CdTe thin film (a) and the same film with a 50-nm layer of Te (b) deposited on top.

Figure 2.2 shows the scanning electron microscope (SEM) images of the free surface of a typical CdTe film (a) as compared to the same surface with a 50-nm layer of Te (b) evaporated on top. The Te layer has a much-smaller grain size on the order of 100 nm and appears continuous across the CdTe surface. Overall, evaporated Te on CdTe forms a continuous, polycrystalline thin-film layer.

2.2 Discussion of Back Contact Strategies

The following sections present an extensive picture of various back contacts used in CdTe solar cells fabricated at CSU both before and after the Te-layer research began. CSU's traditional back contact, which includes a carbon buffer layer, is characterized in detail to provide context for the incorporation of the Te buffer layer. Next, the performance and characteristics of various combinations of the Te buffer and the commonly-used Cu contacting treatment are compared with the C-buffer contact, followed by a study of the effect of the Te layer thickness on device performance. Lastly, the results of varying the amount of Cu treatment are discussed.

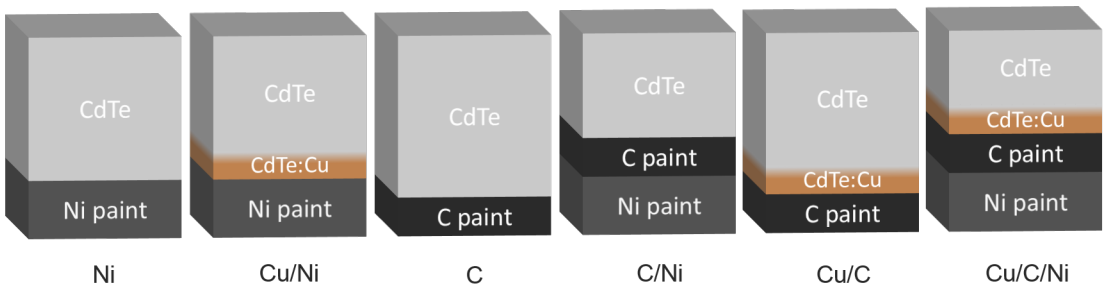

Figure 2.3: Six paint back contact strategies: only Ni paint (Ni); Cu treatment/Ni paint (Cu/Ni); only C paint (C); C paint/Ni paint (C/Ni); Cu treatment/C paint (Cu/C); and (traditional CSU contact strategies) Cu treatment/C paint/Ni paint (Cu/C/Ni).

2.2.1 Carbon Buffer Contact

This section discusses the traditional back contact strategy used at CSU before the Te-layer research began, which consists of the standard Cu treatment (Sec. 1.3.2), followed by a layer of C paint and Ni paint (right-most diagram in Fig. 2.3). The Te layer is not incorporated for the devices discussed in this section. The C-paint layer is ∼5-μm-thick with a sheet resistance of ∼90 Ω/□, and the Ni-paint layer is ∼50-μm-thick with a sheet resistance of ∼0.25 Ω/□. The effect of each layer and/or the Cu treatment on the solar cell performance was explored both separately and in combination.

Six different combinations of the paint contacts and Cu treatment were fabricated on nominally identical CdTe (2.7 μm) devices fabricated with the MZO emitter layer. Fig. 2.3 compares the six back contacts that were studied: only Ni paint (Ni), Cu treatment/Ni paint (Cu/Ni), only C paint (C), C paint/Ni paint (C/Ni), and Cu treatment/C paint (Cu/C), and (traditional CSU contact) Cu treatment/C paint/Ni paint (Cu/C/Ni).

Figure 2.4 compares the J-V and QE curves from devices with these six contacts and Fig. 2.5 shows the box plots of the V_{OC} and FF data for 10 devices fabricated for each back contact. Box plots are a standardized method to display data distributions and are useful for visually comparing data between several groups [58]. The devices with the Ni paint directly on the CdTe (red and black curves) have a very high series resistance. This is postulated to

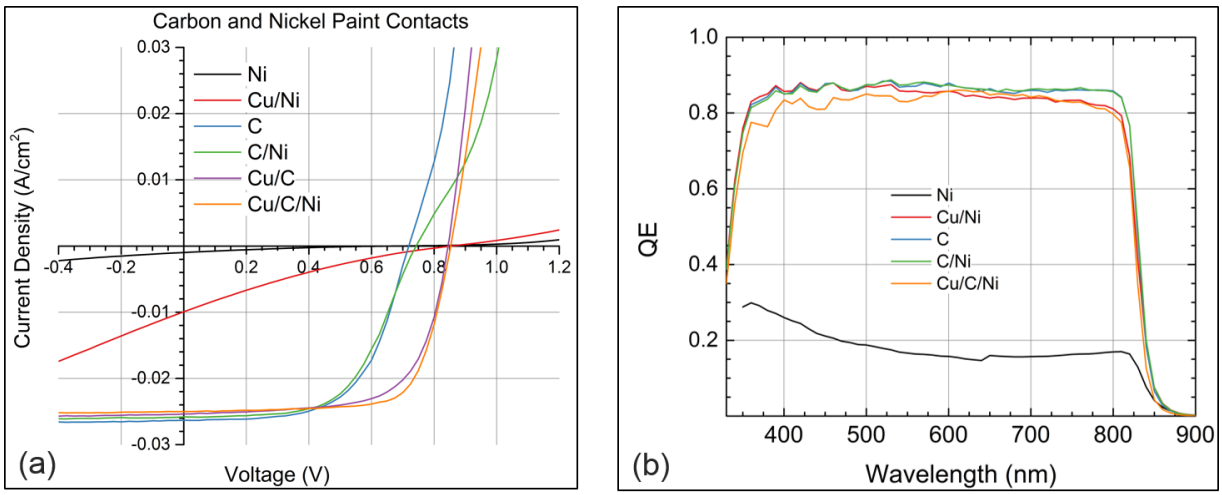

Figure 2.4: J-V (a) and QE (b) curves for the C and Ni paint back contacts.

be caused by incomplete physical contact of the Ni paint to the CdTe back surface. In the Ni contact without Cu treatment, there appears to be a barrier that is large enough to nearly completely impede the photocurrent as seen in the the QE data (Fig. 2.4b, black curve). The barrier is reduced in Cu-treated CdTe with the the Ni-paint contact, indicated by the increased QE (Fig. 2.4b, red curve) and average V_{OC} (Fig. 2.5a); however, the J-V curve is still greatly distorted by the large series resistance.

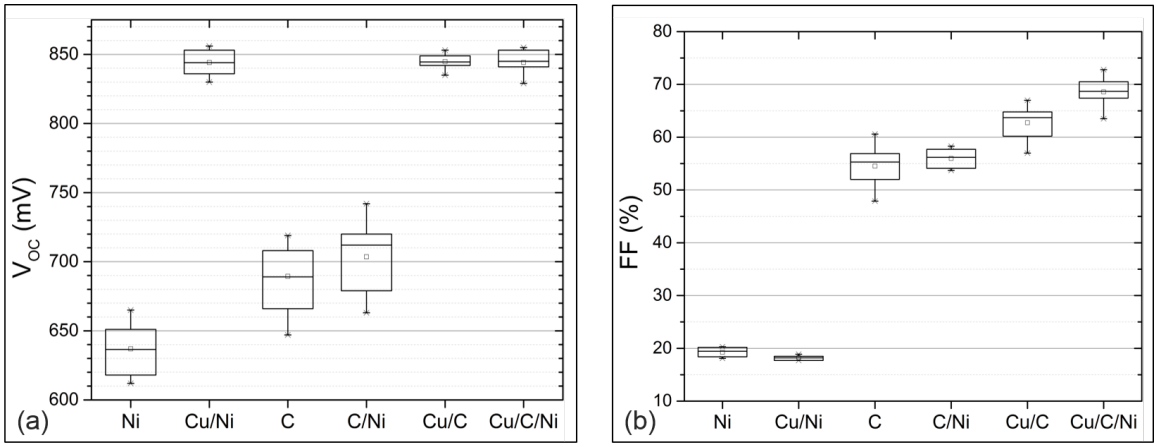

Figure 2.5: Box plots of V_{OC} (a) and FF (b) for the C and Ni paint back contacts. Each box represents nine cells.

The C-paint-only contact (blue curve in Fig. 2.4a) has much less series resistance and exhibits diode behavior, although the J-V curve does demonstrate a slight "kink" behavior [59]. The average V_{OC} is also slightly higher than the Ni-paint-only contact (Fig. 2.5a), suggesting the C-paint forms a lower barrier at the back than the Ni-paint. Adding a layer of Ni-paint on top of the C-paint (green curve in Fig. 2.4a) increases the "kink" behavior, however the average V_{OC} is slightly increased and FF is relatively unchanged. Thus, the C/Ni contact results in similar average performance compared to without the Ni-paint, even though the J-V curve is more distorted. Cu-treatment of the CdTe before applying the C-paint greatly improves V_{OC} and FF (Fig. 2.5a and b), from both increasing the bulk doping and creating a lower-resistance back-contact, which effectively reduces the forward electron current. Ultimately, combining Cu treatment with a C-paint layer and Ni-paint layer produces the best-performing contact. The J-V parameters from the Cu/C and Cu/C/Ni contact devices shown in Fig. 2.4a are compared in Table 2.1. The Cu/C/Ni contact is superior in essentially every category except series resistance. The lower FF of the Cu/C device relates to a large and likely artificial ideality factor (A) of 2.9.

Table 2.1: Comparison of J-V parameters of Cu/C and Cu/C/Ni back contact strategies.

Back Contact	V_{OC} [V]	J_{SC} [mA/cm^2]	FF [%]	η [%]	J_0 [mA/cm^2]	r_{sh} [Ωcm^2]	R_s [Ωcm^2]	A
Cu/C	845	25.4	67.1	14.4	3E-04	1500	0.6	2.9
Cu/C/Ni	853	25.0	72.8	15.5	6E-07	2600	1.9	1.9

The QE of the Cu/C/Ni device is slightly lower than the C/Ni device without Cu treatment (Fig. 2.4b). It is common for the QE in the longer wavelengths to be reduced after Cu treatment due to an increase in recombination centers related to Cu defects. The reduction in the low wavelengths is typically not observed and is likely unrelated to the back contact.

Analyzing the C-V response of these devices gives further insight into the physical mechanisms of the back contacts. Figure 2.6a is a plot of $(A/C)^2$ versus the applied voltage (see Sec. 1.4.3 for C-V analysis details). The problematic devices with Ni paint directly on the CdTe have a higher values of $(A/C)^2$ compared to the devices with the C buffer. An increased resistance, which is seen in the J-V curves, in the circuit can cause a decrease in the measured capacitance. Capacitance may also be decreased due to a smaller area (Eq. 1.12). If so, the $(A/C)^2$ values will be inflated if a larger area than the true contact area is assumed. This appears to be the case for the Ni-paint contacts as the ranges of the depletion width calculated using the apparent measured areas are larger than the physical thickness of the CdTe layer. Figure 2.6b shows the depletion width of the Cu/Ni contact extending to ~3.3 μm, however the physical CdTe thickness is only 2.7 μm. The plot of the Ni-paint-only contact is beyond the plotted range of Fig. 2.6b, but its calculated depletion width at zero bias is 5.3 μm. Using an area of approximately half of the apparent contact area shifts the $(A/C)^2$ plots for these two devices to nearly overlap with the other devices.

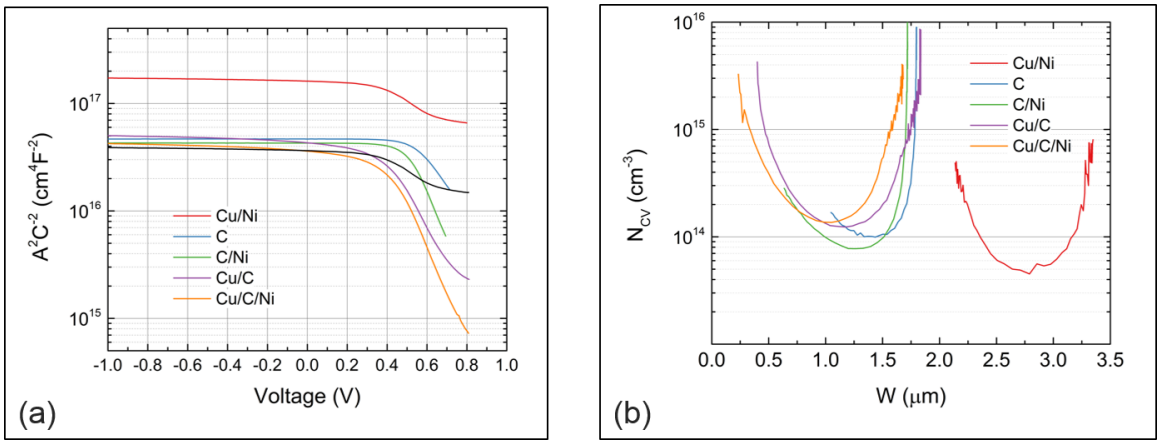

Figure 2.6: Plots of the inverse capacitance squared versus voltage (a) and the carrier density versus depletion width (b) for the C and Ni paint back contacts.

For the devices with the C paint, the C-V analysis yields realistic values for carrier density and depletion width. There is a reduction in $(A/C)^2$ for respective C contacts with Ni. This shift can result from a reduction in potential drop in the device [7].

A notable difference results from the Cu treatment. In voltage bias regions where non-Cu treated devices had little change in $(A/C)^2$, the Cu treated devices have visible curvature, and in the linear portion of the plot, they have a lower slope; both observations indicate an increase in carrier density [7, 52].

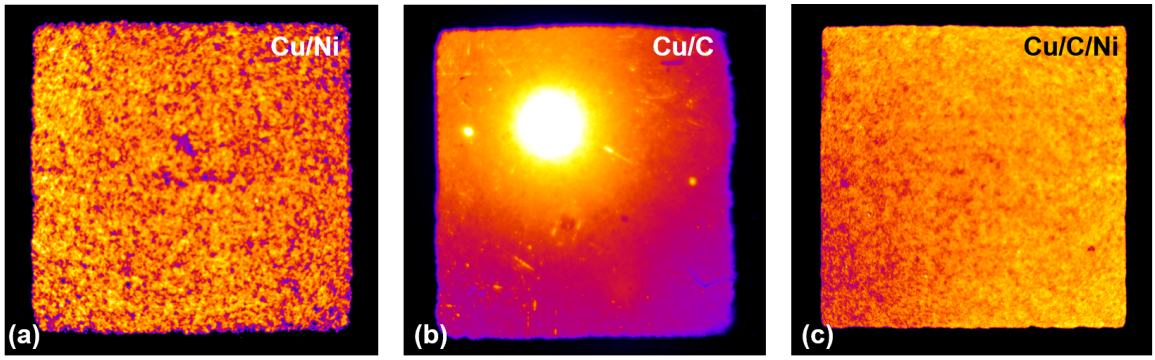

Figure 2.7: EL images of devices with the Cu/Ni-paint (a), Cu/C-paint (b), and Cu/C-paint/Ni-paint (c) back contacts.

The electroluminescence (EL) images of these devices provide a visual look at differences in the back contacts. Figure 2.7 compares the EL images of the Cu/Ni (a), Cu/C (b), and Cu/C/Ni (c) contacts. It appears that the Cu/Ni contact is much more nonuniform and is riddled with small areas of low signal adjacent to small areas with large signal, which could correspond to incomplete contact of the Ni paint to the back surface of the CdTe. The Cu/C contact (the high intensity spot will be discussed separately) does not show the grainy appearance in contrast to the Cu/Ni contact. This suggests that the C-paint makes uniform contact with the CdTe surface. The Cu/C/Ni contact does show some granular nonuniformities, however they are on a smaller scale, and the C layer seems to clearly mitigate their presence. The large, high-intensity circle on the Cu/C contact corresponds with the position of the contact probe used to apply the voltage bias. Due to the high sheet resistance of the C-paint layer, there is a lateral voltage drop across the back contact. The current is exponentially dependent on the locally applied voltage bias and will manifest in the EL image [57]. Adding Ni paint on top of the C-paint eliminates the lateral voltage drop and is possibly the reason for the shift in the $(A/C)^2$ data.

To summarize, the Ni-paint contact directly on the CdTe greatly reduces device performance due to high series resistance, which is suggested to be caused by incomplete physical contact of the Ni to the CdTe surface and is supported by evidence from C-V and EL data. The C-paint contact makes much greater physical contact with CdTe, which creates a lower resistance contact, despite having a higher resistivity than the Ni paint. However, the high sheet resistance of the C paint without a second layer causes a lateral voltage drop over the back contact. The Ni-paint on top of the C paint essentially serves as an large-area electrode. The Cu treatment increases both the V_{OC} and FF by increasing the doping and reducing the back barrier. The combination of the Cu treatment, C and Ni paint layers results in the best performing device for this set of materials. Next, the inclusion of the Te buffer layer in the back contact will be discussed.

2.2.2 Te Buffer Contact

The Te buffer layer was incorporated in the back-contact of a CdS/CdTe (2.7 μm) based device in three different configurations. Note that the use of CdS emitter layer will result in lower device performance compared to an MZO emitter (discussed in Sec. 1.3.1); however, all devices are referenced to the Cu/C/Ni baseline device. The Te-buffer contact methods were compared to the C/Ni contact with and without Cu treatment. All Cu-treated devices received the standard Cu treatment discussed in Section 1.3.2. This study also compared the effect of Cu treatment before and after deposition of the Te layer to that of no Cu treatment with the Te layer. It is unlikely that any Cu_xTe phases formed from the Cu treatment after the Te deposition. The highest temperature the substrate was exposed was 200°C for under 4 minutes. It has been shown that no Cu_xTe formation will occur for temperatures below 260° [60, 61, 62]. Figure 2.8 shows the five back contacts that were studied: C-paint/Ni-paint (C/Ni), Cu treatment/C-paint/Ni-paint (Cu/C/Ni), 50-nm Te/Ni-paint (Te/Ni), 50-nm Te/Cu treatment/Ni-paint (Te/Cu/Ni), and Cu treatment/50-nm Te/Ni-paint (Cu/Te/Ni).

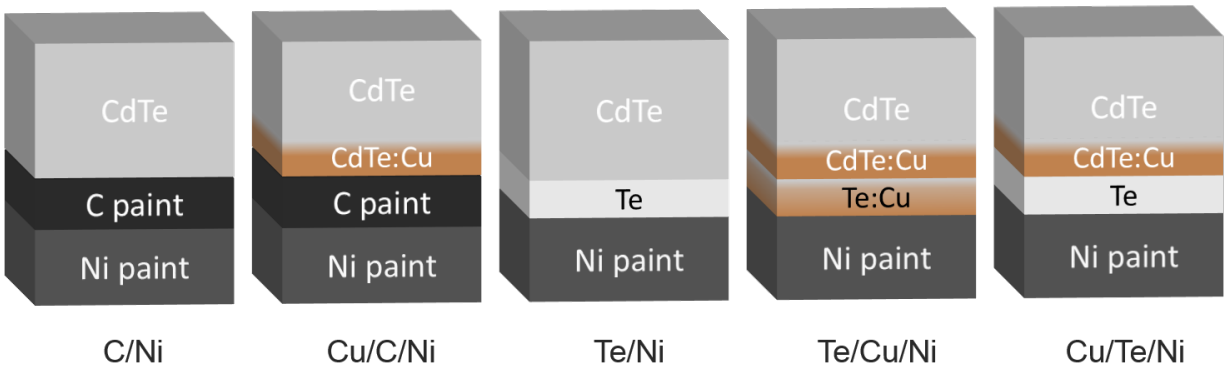

Figure 2.8: Five back contact strategies: C-paint/Ni-paint (C/Ni); Cu treatment/C-paint/Ni-paint (Cu/C/Ni); 50-nm Te/Ni-paint (Te/Ni); 50-nm Te/Cu treatment/Ni-paint (Te/Cu/Ni); and Cu treatment/50-nm Te/Ni-paint (Cu/Te/Ni).

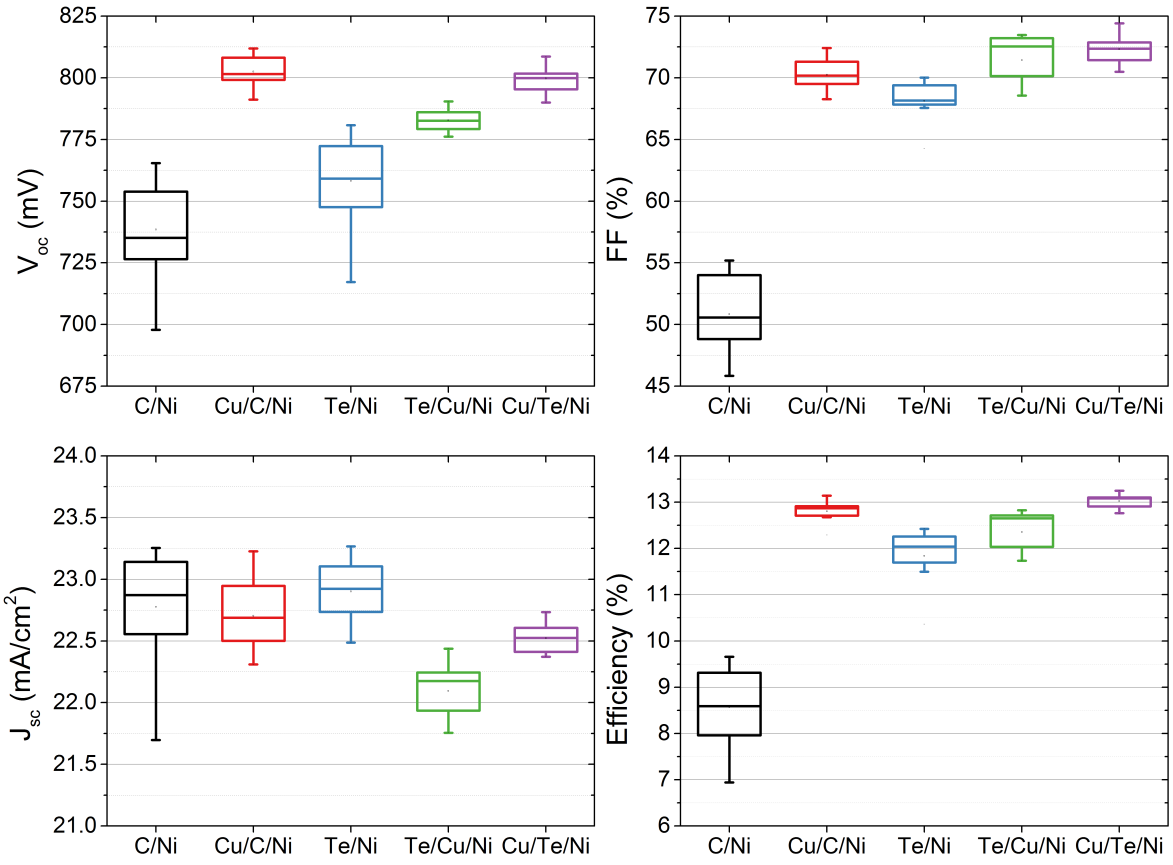

Figure 2.9: Box plots of J-V parameters for CdS/CdTe devices with five different back contact strategies. Each box represents 9 devices on a common substrate.

Figure 2.9 shows the box plots of V_{OC}, J_{SC}, FF, and efficiency of the devices fabricated with the five different back contacts, including the variation in the nine small-area devices from one substrate. The devices without Cu treatment have lower V_{OC} and much higher variation over the substrate than those with added Cu. In comparing the FF of the non-Cu-treated devices, the sample with Te has a much larger FF, leading to a higher efficiency. The devices that received the Cu treatment have similar values of V_{OC} and FF; however there are some differences. The devices that were Cu-treated directly on the CdTe back surface have nearly the same median V_{OC}. The devices that were Cu-treated after the Te layer was deposited had an approximately 18 mV lower median V_{OC}. In regards to the FF of the Cu-treated devices, the Te devices had nearly the same median value while the C devices were approximately 2% lower. The J_{SC} of all devices were nearly the same, except the Te/Cu/Ni device showed slightly lower current than the others. This trend is also consistent with QE measurements (Fig. 2.10b), and it is unclear whether it is an effect of the back contact or due to other processing steps.

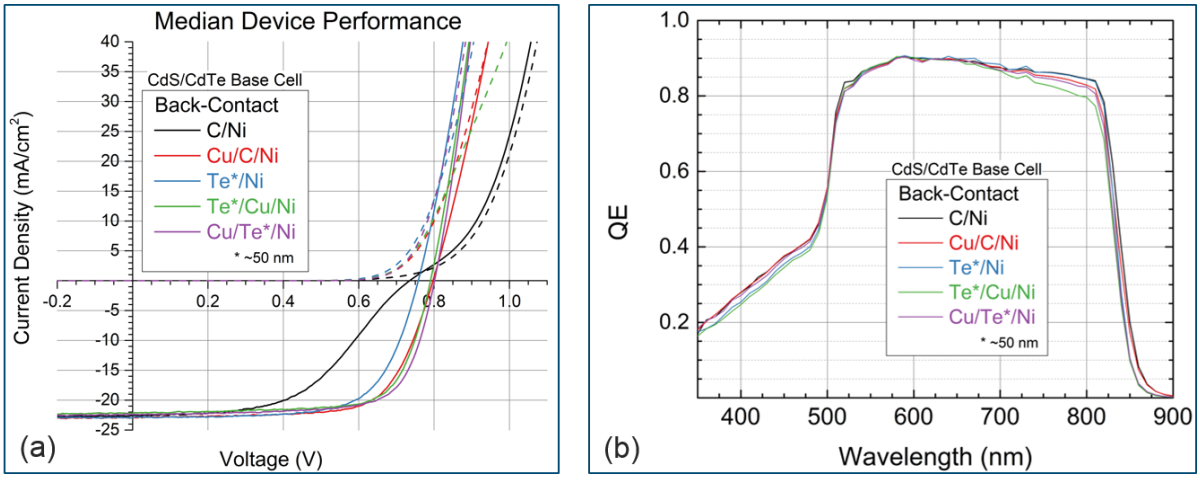

Figure 2.10: J-V (a) and QE (b) curves of CdS/CdTe devices with five different back contact strategies.

Figure 2.10a shows a comparison of the light and dark J-V curves representative of the median device on each substrate. The weakest device is the C/Ni-only back contact which has very poor FF compared to the other devices and has the J-V "kink" shape consistent

Table 2.2: Median J-V parameters of CdS/CdTe devices with five different back contact strategies.

Back Contact	V_{OC} [V]	J_{SC} [mA/cm^2]	FF [%]	η [%]	J_0 [mA/cm^2]	r_{sh} [Ωcm^2]	R_s [Ωcm^2]	A
C/Ni	735	22.6	50.6	8.4	N/A	1400	N/A	N/A
Cu/C/Ni	797	22.9	69.5	12.7	3E-6	1600	2.4	1.9
Te/Ni	758	22.9	68.2	11.9	1E-4	3400	1.4	2.4
Te/Cu/Ni	783	22.0	70.2	12.1	3E-6	900	1.4	1.9
Cu/Te/Ni	801	22.4	72.4	13.0	2E-6	1700	1.1	1.9

with the MZO/CdTe/C/Ni device from Sec. 2.2.1 (J_{SC} and V_{OC} are higher due to the MZO). The "kink" make it impractical to extract detailed cell parameters, which are given for the other cells in Table 2.2. Applying Te instead of C without Cu treatment, greatly increases the FF, however J_0, the A factor, and r_{sh} are all higher than any device with Cu. The devices that received Cu all have the same A factor (1.9) and similar J_0. The Cu/C/Ni device has more slightly series resistance than the Te buffer devices. Overall, the Cu/Te/Ni device has the best value for almost all J-V parameter categories.

The QE curves of the five devices are plotted in Fig. 2.10b. The current collection in all of the devices below ∼650 nm is approximately the same. There are small differences in the CdS absorption region (below ∼520 nm), but that is likely caused by slight variations in CdS thickness. Above ∼650 nm, devices without Cu treatment have the highest QE. The devices that received Cu also have similar collection in this region implying that Cu is causing recombination at the back of the device. The device that was Cu-treated after the Te layer had the most recombination at the back, possibly due to additional or different Cu-related defects at the CdTe/Te interface or in the Te layer itself.

Another notable, but slightly subtle, feature is the sharper cut-off in QE near the CdTe band edge for devices with Te compared to the C contact. This reduction in QE only accounts

for less than 0.15 mA/cm^2, but it is a genuine and reproducible feature. The loss is likely optical and due to reduced photon reflection at the back with the Te layer. For wavelengths near the CdTe band gap, the index of refraction for CdTe is ∼3 [63], for Ni it is ∼2.2 [64], and, for C it is ∼2.1, assuming the C paint behaves like carbon-black materials [65]. Thus, assuming shallow angles of incidence are present, light incident on the interface of CdTe/C or CdTe/Ni have a probability of being totally internally reflected and reabsorbed in the CdTe. The index of refraction for Te is ∼5 [66], and thus a portion of all light incident on the CdTe/Te interface will be transmitted into the Te, regardless of the angle of incidence. Thus, fewer photons that reach the CdTe/Te interface will be reflected and reabsorbed in the CdTe. This phenomenon has been observed in QE near the band edge of amorphous and multicrystalline Si solar cells with different back contact strategies [67, 68].

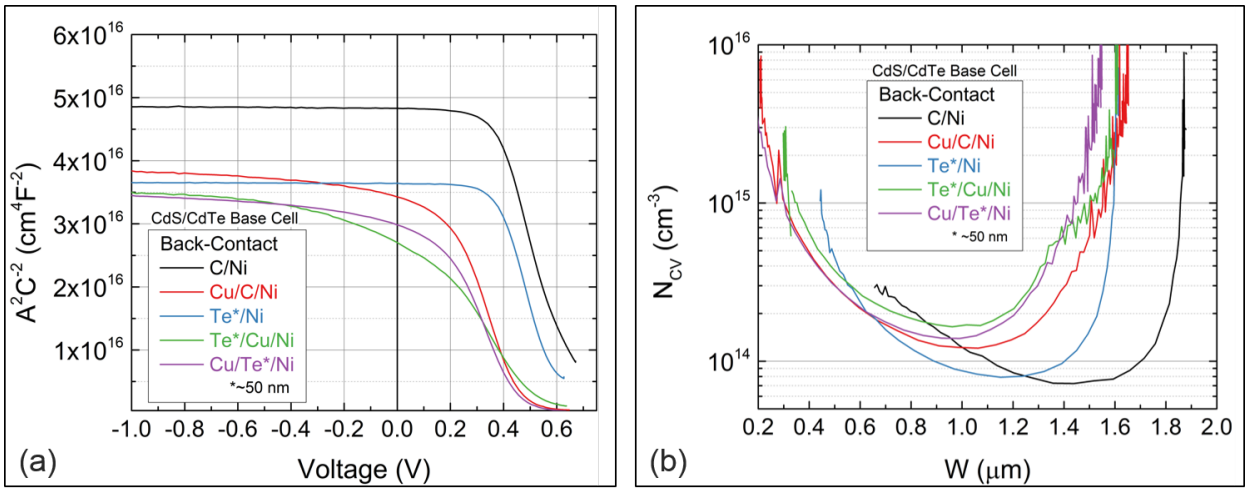

Figure 2.11: Plots of the inverse capacitance squared versus voltage (a) and the carrier density versus depletion width (b) for devices with five different back contact strategies.

The C-V analysis of cells with these contacts gives further insight to their physical mechanisms. These devices with the Cu/Ni and Cu/C/Ni contacts do not converge to the same value of $(A/C)^2$ in reverse bias (Fig. 2.11), however the change in curvature and slope of the Cu treated devices are present, indicating an increase in doping [7]. The Cu treatment also appears to have reduced a potential drop in the device, signified by the shift in $(A/C)^2$, which could be from the effect of the increased Cu doping lowering the back barrier. Use of

the Te layer in place of the C-paint shows a similar shift in $(A/C)^2$, however there is not a change in curvature or slope of the Te/Ni $(A/C)^2$ data. This suggests that the back barrier was lowered and/or the Te layer introduced a negative interface charge, but the decrease in $(A/C)^2$ was not caused by a change in doping.

The C/Ni and Te/Ni contacts with Cu treatment appear to parallel each other with the Cu/Te/Ni shifted down in the $(A/C)^2$ as also observed in the no-Cu treatment case. The device that received Cu treatment after the Te layer appears to have characteristics in between the no Cu treatment and Cu treatment directly on the CdTe. The Te/Cu/Ni devices has slightly higher bulk carrier density than the others; but this does not correlate with V_{OC}. Thus, the apparent increase may be from mid-gap states created by the interaction of the Cu treatment with the Te layer [52].

Overall, the Te layer has proven to be a good buffer layer for the back contact for CdTe solar cells. This is especially true for non-Cu treated samples, as compared to the C buffer. Using the standard Cu treatment, the Cu/Te/Ni has better overall performance than the Cu/C/Ni contact. Next, the effect the Te layer thickness on the device performance will be explored.

2.2.3 Cu/Te/Ni with Variations in Te Thicknesses

Nominally identical MZO/CdTe (2.5 μm) devices with the standard Cu treatment were fabricated with varying thicknesses of the Te buffer layer before the Ni-paint contact. Seven Te thicknesses used were: 0, 4, 8, 15, 35, 54, and 165 nm. The J-V curves representative of the median device from each substrate are shown in Fig. 2.12a. With no Te present, the devices behave as seen in Section 2.2.1. However, incorporation of a thin, 4-nm layer of Te shows a reduction in resistance from the Ni-paint contact, and a Te thickness of 15 nm appears to be the threshold of good device performance.

The box plots of V_{OC} and FF from the nine small-area devices from each substrate are presented in Fig. 2.13. While the V_{OC} does not greatly change, there appears to be an increasing trend with increasing Te thickness, which plateaus above 35 nm. Regarding the

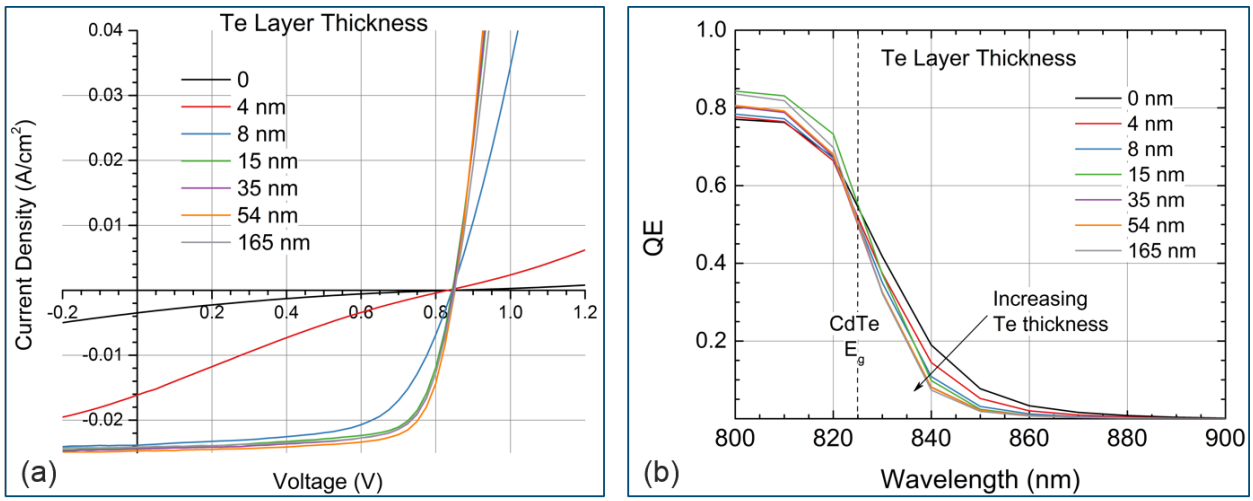

Figure 2.12: J-V (a) and (b) curves of MZO/CdTe/Cu/Te/Ni devices with varied thickness of the back contact Te buffer layer.

FF, approximately 15 nm of Te is required to achieve a respectable FF and the thickness of 54 nm resulted in the best performance.

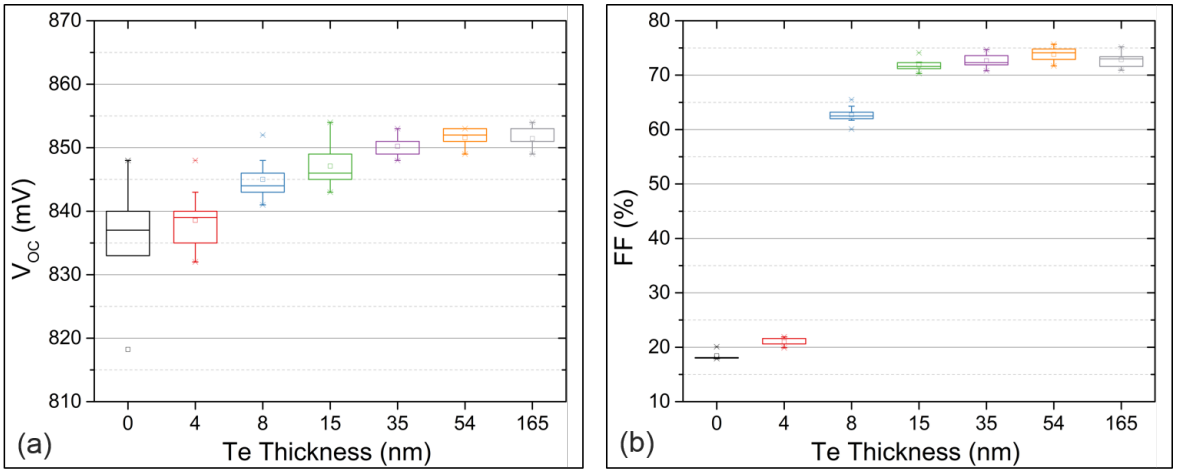

Figure 2.13: Box plots of V_{OC} (a) and FF (b) of MZO/CdTe/Cu/Te/Ni devices with varied thickness of Te buffer layer in the back contact.

The change in QE near the band edge, as seen in Section 2.2.2 devices, is also present. Figure 2.12b shows the QE response of the different Te-thickness devices in the wavelength region of 800-900 nm. There is a trend of reduced QE in wavelengths above the band gap as Te thickness is increased. With thinner Te, more of the light that is transmitted into the Te

layer is able to be reflected at the Te/Ni interface and possibly transmitted back across the CdTe/Te interface before it is absorbed in the Te. As the Te layer thickens, the path length light must travel in the Te, before it is potentially reflected and transmitted back into the CdTe, is longer and the photons are more likely to be absorbed in the Te layer.

The EL images provide an enlightening visual of the transition from no Te to a layer of sufficient thickness for performance improvement (Fig. 2.14). The images show the effect of the incomplete coverage of the Ni-paint being gradually reduced as the Te thickness is increased. At 35 nm of Te, the graininess in the EL imagine caused by the Ni-paint is nonexistent.

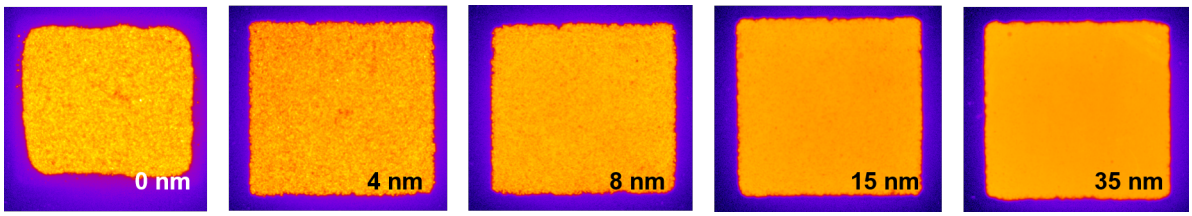

Figure 2.14: EL imagines of MZO/CdTe/Cu/Te/Ni devices with varied thickness of Te buffer layer in the back contact.

The thinner Te layers likely cause performance issues due to both incomplete coverage of the CdTe surface and lack of material to realize the bulk properties of the Te. Incomplete Te coverage adjacent to the Ni-paint, will cause the high resistance issues. Niles et al. also reported that Te layers below 7.6 nm exhibit n-type behavior [69], which would be detrimental to performance and is consistent with our observations. More on the material properties of a sufficiently-thick Te layer will be discussed in Sec. 2.5. Next, the effect of varying the Cu treatment with the Cu/Te/Ni back contact on device performance will be explored.

2.2.4 Cu/Te/Ni with Variations in Cu Treatment

It was demonstrated that the Te buffer layer could produce devices with good FF without Cu treatment as compared to the C/Ni devices without Cu. Thus, the optimal Cu treatment was likely different for devices with the Te contact. A series of nominally identical MZO/CdTe (2.5 μm) devices where fabricated with the duration of the time spent in the CuCl source varied. The Cu treatment was done directly on the CdTe surface. All devices received ~50 nm of Te followed by the Ni-paint.

To review and expand the discussion of the Cu treatment from Sec. 1.3.2, Fig. 2.15 illustrates the Cu treatment process. The substrate enters the vacuum chamber at room temperature and moves into a pre-heating station, where the top and bottom heaters are at 330°C, for 75 seconds. Next, it traverses into the CuCl source station, where the top heater is at 170°C and the bottom crucible, containing the CuCl material, is at 190°C. The standard time for the CuCl station is 110 seconds for devices fabricated at CSU. In this study, this time was varied from 0 to 165 seconds over 10 different substrates. After CuCl, the sample is annealed in the next station, where the top and bottom heaters are at 200°C, for 220 seconds.

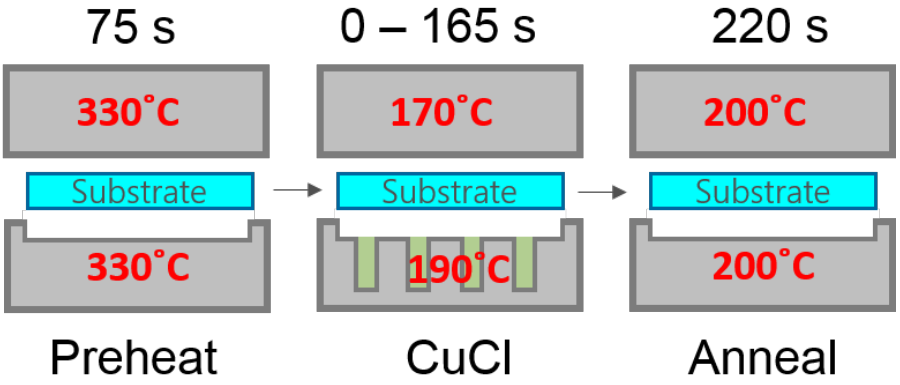

Figure 2.15: Illustration of Cu treatment process.

Figure 2.15 shows box plots of V_{OC} (a) and FF (b) for the devices with different Cu treatment times. Each box plot again represents nine cells from each substrate. Any amount

of Cu treatment greatly increases the V_{OC} (Fig. 2.15). For the groups of cells represented, V_{OC} appears to saturate at ~850 mV. The highest and most uniform FF, however occurs in the range of 15-30 seconds, which is ~20% of the standard time without Te of 110 seconds. Above 30 seconds, there is an abrupt drop in both the average FF and the cell uniformity. By reducing the Cu treatment from 110 s to 15 s, the average FF increased from 72.6 ± 1.3% to 75.4 ± 0.5%.

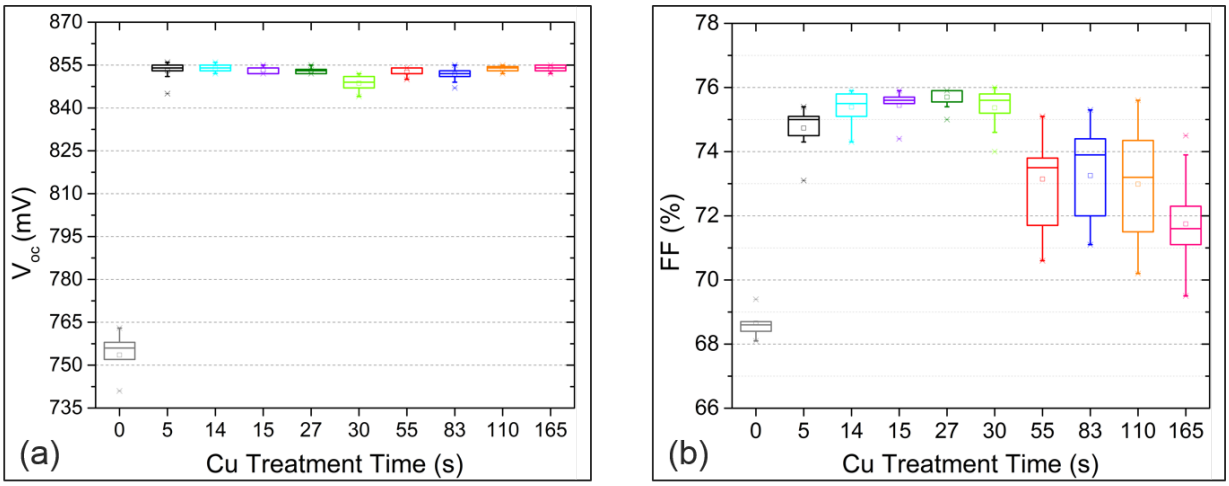

Figure 2.16: Box plots of V_{OC} and FF of MZO/CdTe/Cu/Te/Ni devices with varied time of Cu treatment. All have a 50-nm Te layer.

The J-V parameters of the median device from six different Cu treatment times were analyzed in more detail and are presented in Table 2.3. The device that was not Cu treated was the lowest performing, and it had the highest saturation current (J_0) and A factor. Any amount of Cu significantly lowered J_0 and the A factor. The higher Cu treatment devices, however, tended to have higher J_0 and A values which suggests that there are additional defect states that act as recombination centers and/or carrier traps, likely created due to excess Cu.

The series resistance (R_s) in all of the devices was relatively similar, but, there appears to be a very modest trend of reduced R_s as Cu treatment time is increased, possibly suggesting that Cu aids in creating a lower-resistance back contact. The shunt resistance for all devices

was relatively similar and does not seem to correlate with Cu treatment time for the range studied.

Table 2.3: J-V parameters of the median device from each MZO/CdTe/Cu/Te/Ni substrate with varied time of Cu treatment.

CuCl Time [s]	V_{OC} [V]	J_{SC} [mA/cm^2]	FF [%]	η [%]	J_0 [mA/cm^2]	r_{sh} [Ωcm^2]	R_s [Ωcm^2]	A
0	753	25.0	68.6	12.9	2E-4	1600	1.2	2.5
14	855	25.5	75.3	16.4	6E-7	2200	0.9	1.9
27	852	25.5	75.7	16.5	3E-7	1700	0.9	1.8
83	851	25.0	74.0	15.8	6E-7	1500	0.8	1.9
110	853	25.2	73.1	15.7	1E-6	1500	0.8	1.9
165	854	24.8	71.7	15.2	1E-6	1100	0.8	2.0

The C-V analysis from the devices listed in Table 2.3 are presented in Fig. 2.17. There does not appear to be a trend with Cu treatment time in reverse bias, but a progression is obvious as the device is put into forward bias. All devices with Cu treatment show an increase in carrier density at zero bias, but as the Cu treatment time is lowered so is the slope of $(A/C)^2$ (Fig. 2.17a). This translates into higher apparent carrier density with the lower Cu treatment.

To confirm the amount of Cu in the devices, SIMS depth profiles were measured on devices similar to those discussed in this section. The SIMS characterization was performed at First Solar, Inc. Figure 2.18b shows the carrier density profiles of three MZO/CdTe devices with different Cu treatment times: no treatment, 15 s, and 110 s. Figure 2.18a shows the SIMS depth profiles of Cu concentration for these same devices. The carrier densities are approximately 3-4 orders of magnitude lower than the actual bulk atomic concentrations of Cu. As previously noted, favorable p-type doping from Cu is highly compensated by the

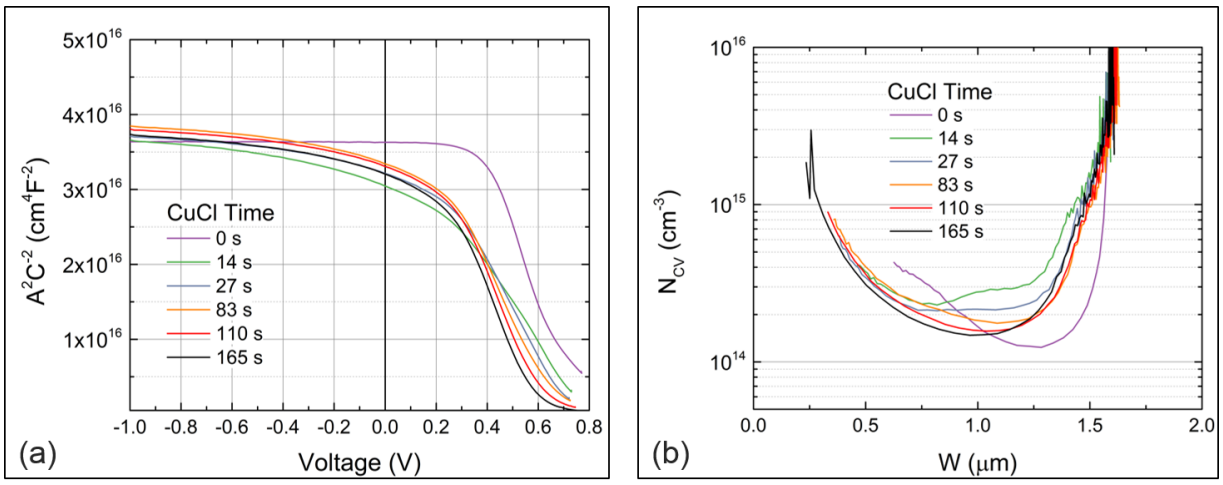

Figure 2.17: Plots of the inverse capacitance squared versus voltage (a) and the carrier density versus depletion width (b) for MZO/CdTe/Cu/Te/Ni devices with varied time of Cu treatment.

formation of other defects and complexes [22], and thus the vast majority of the Cu inside the CdTe does not contribute to the net acceptor doping. The SIMS data shows that Cu treatment time does correlate to the amount of Cu in the bulk of the CdTe. However, the carrier density does not scale with the amount of Cu (Fig. 2.18). The 15-s Cu treatment resulted in approximately half the bulk Cu concentration as the 110-s Cu treatment. The lower atomic Cu concentration in the CdTe (after Cu treatment) resulted in an increased carrier density, likely due to reduced compensation.

Reducing the Cu treatment with the C/Ni back contact is much less effective than using the Te/Ni contact. Figure 2.19 shows the J-V curves of MZO/CdTe devices made on three substrates with the different Cu treatment times (Fig. 2.18): 0 s (a), 15 s (b), 110 s (c). Half of each substrate received the C/Ni (dashed curves) contact and the other half got the Te/C/Ni contact (solid curves). Comparing the two contacts with the lower Cu treatment (Fig. 2.19b), the C/Ni contact has poor FF while the Te/Ni contact has respectable curve squareness, resulting in 14.4% versus 17% average device efficiency, respectively. The C/Ni requires the "standard" 110-second Cu treatment to eliminate "kink" behavior and achieve

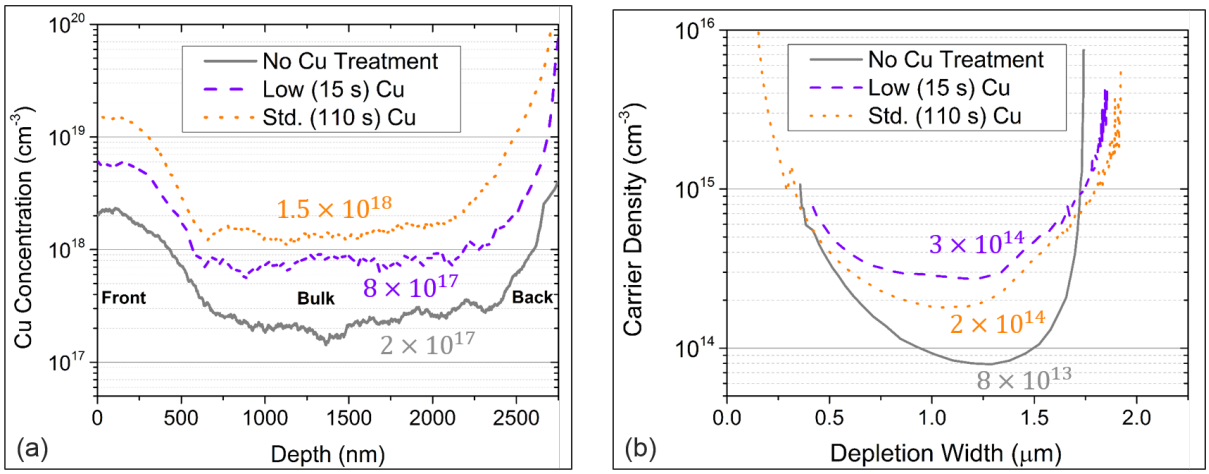

Figure 2.18: Cu concentration depth profiles from SIMS (a) and carrier density versus depletion width (b) for three devices with different Cu treatment times: 0 s (solid), 15 s (dashed), 110 s (dotted). (SIMS characterization performed at First Solar, Inc.)

good FF, which floods the devices with excess Cu and may cause greater metastability issues (discussed in Chap. 3).

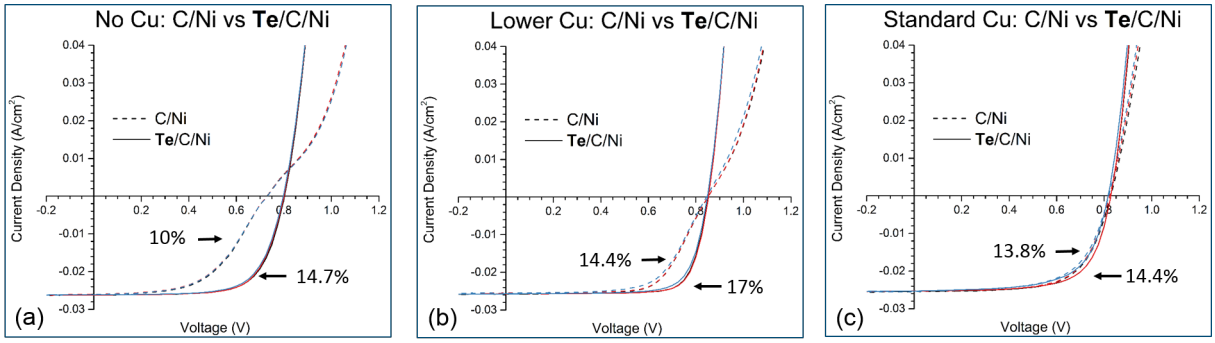

Figure 2.19: J-V curves of MZO/CdTe devices made on three substrates with the different Cu treatments: 0 s (a), 15 s (b), 110 s (c). Half of each substrate received the C/Ni contact (dashed curves) and the other half got the Te/C/Ni contact (solid curves). The average efficiencies of the curves are labeled.

In summary, it was found that amount of Cu could be substantially reduced in CdTe solar cells with the Te buffer layer, which resulted in improved device performance. Some Cu treatment is necessary for the best performing devices, however a lower treatment results in better FF, lower J_0 and A factor. It was also discovered that the amount of Cu in the

device does not scale with acceptor doping. Overall, the Te layer is an effective buffer for the back contact of CdTe. Next, the J-V curves of various devices at different temperatures will be analyzed.

2.3 J-V-T Analysis of Devices with Te Buffer Contact

This section discusses the J-V-T analysis of CdTe devices with the Te buffer back contact (Sec. 1.4.1) and are also compared with the C-buffer devices. To begin, two CdS/CdTe devices with standard Cu treatment are analyzed. One has the C/Ni contact and the other has the Te (50 nm)/Ni contact. The devices were measured at several temperatures from approximately 315 K to 190 K. The room temperature (300 K) J-V parameters for the two devices are listed in Table 2.4. These two devices were nominally processed the same up to the application of the C or Te buffer. The Te-buffer device performed better every category. The performance differences will become more evident as the device temperature is lowered.

Table 2.4: J-V parameters for CdS/CdTe devices with the Cu/C/Ni and Cu/Te/Ni back contacts measured at 300 K.

Back Contact	V_{OC} [V]	J_{SC} [mA/cm^2]	FF [%]	η [%]	J_0 [mA/cm^2]	r_{sh} [Ωcm^2]	R_s [Ωcm^2]	A
Cu/C/Ni	785	21.0	68.0	11.2	7E-5	2300	1.8	2.4
Cu/Te/Ni	797	20.9	72.7	12.1	5E-6	1700	1.0	2.0

Figure 2.20 shows the J-V curves of two devices from Table 2.4, Fig. 2.20a is the Cu/C/Ni contact and Fig. 2.20b is Cu/Te/Ni contact. The multiple J-V curves on each plot are for the same cell at different temperatures. In comparing the devices at room temperature (Table 2.4), the short-circuit current densities (J_{SC}) are the same but the open-circuit voltage (V_{OC}) and fill factor (FF) differ between the devices, 785 mV and 68.0% versus 797 mV and 72.7% for the C/Ni and Te/Ni, respectively. There is a much larger difference between the curves for

the two cells as the temperature is decreased. Figure 2.21a shows the FF versus temperature for the devices, the Te/Ni device shows a relativity small change in FF to temperatures below 200 K (the FF slightly increases until ∼240 K). In contrast, the C/Ni device suffers large FF losses, which decreases approximately linearly with temperature below ∼280 K. The behavior as the temperature decreases resembles the J-V curve "kink" that is seen in the C/Ni-contact devices without Cu treatment. Any roll-over the Cu/C/Ni device may exhibit is convoluted by the complexity of the J-V curve. The Cu/Te/Ni device does not show signs of roll-over until temperatures below ∼220 K, at which point the presence of a barrier to photocurrent in forward bias becomes evident.

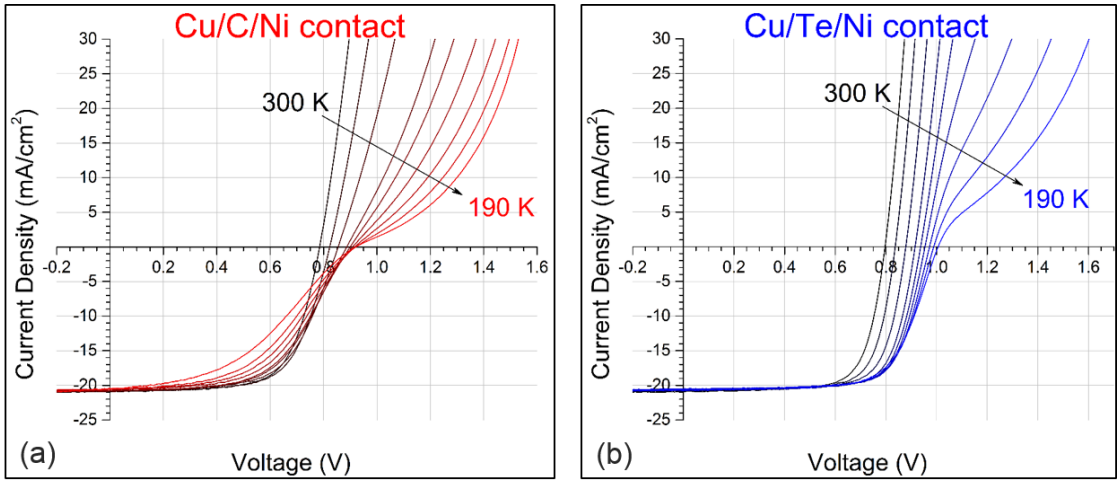

Figure 2.20: J-V curves measured at different temperatures for CdS/CdTe devices with the Cu/C/Ni (a) and Cu/Te/Ni (b) back contacts.

Figure 2.21b shows the V_{OC} versus temperature (T) of these devices. The extrapolated intercept at 0 K provides the activation energy (E_a) of the device [7]. For a well-behaved device, E_a should equal the band gap of the absorber layer (1.5 eV for CdTe). We see that for the Te-buffer device the data is linear over the entire temperature range and its E_a is 1.41 ± 0.01 eV. This agrees well with the CdTe interface band gap assuming a conduction band offset with CdS of -0.1 eV [7]. Extrapolating the linear portion of the data from the C/Ni device, the E_a is 1.32 ± 0.09 eV. An activation energy less than the interfacial band gap is typically attributed to interface recombination [7, 70]. The deviation of V_{OC} vs T from

linearity has been associated with a temperature dependent diode ideality factor caused by tunneling assisted recombination at low temperatures [70, 71].

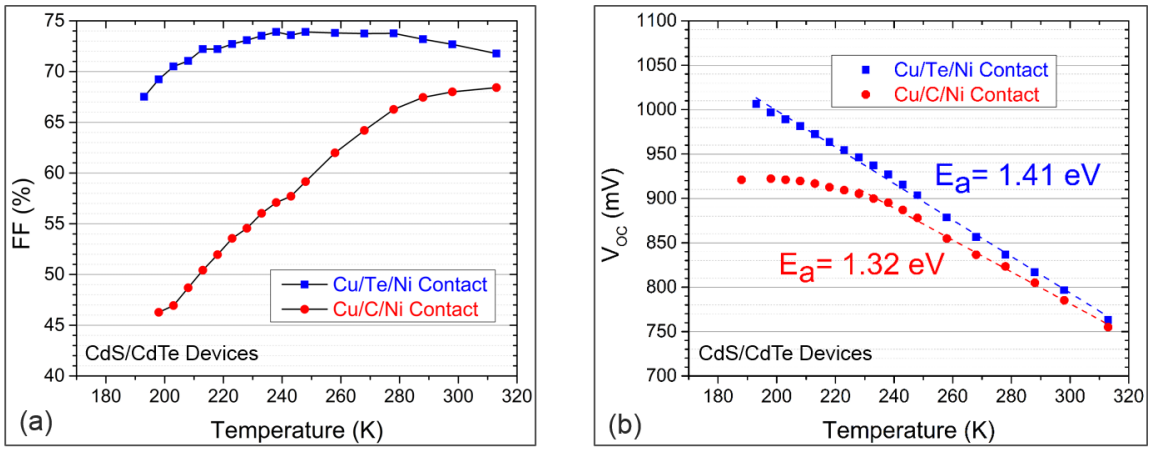

Figure 2.21: FF (a) and V_{OC} (b) versus temperature of CdS/CdTe devices with the Cu/C/Ni and Cu/Te/Ni back contacts. The activation energy (E_a) of each of the devices is labeled.

Similar trends are seen in the V_{OC} vs T from MZO/CdTe devices with the Cu/Ni and Te/Ni back contacts with and without Cu (Fig. 2.22). For the MZO/CdTe devices the ideal activation energy should be the full CdTe band gap, because the CdTe bands fall in between the bands of the MZO. On the no-Cu devices (violet and orange squares), replacing the C-buffer with Te greatly increased the activation energy. The effect of the just the Cu treatment (blue and green circles), regardless of the contact, also substantially increased the activation energy. Just as with the CdS/CdTe devices, the Cu/Te/Ni device extrapolated to an E_a that is nearly the interfacial band gap and the Cu/C/Ni contact extrapolated to a value that was ∼0.1 eV less.

This consistent trend between the Te contacts and C contacts from devices fabricated with different front junctions (CdS/CdTe versus MZO/CdTe) suggests that interfacial recombination at the front junction is not the primary mechanism causing the deviation of E_a from the ideal value. Since the only difference in these devices (for their respective emitter layers) is the back contact, it can be inferred that recombination near the back of the device is reduced as a result of incorporating the Te buffer. The Te layer appears to have the effect of modifying the back surface field and/or passivating defects near the CdTe back surface.

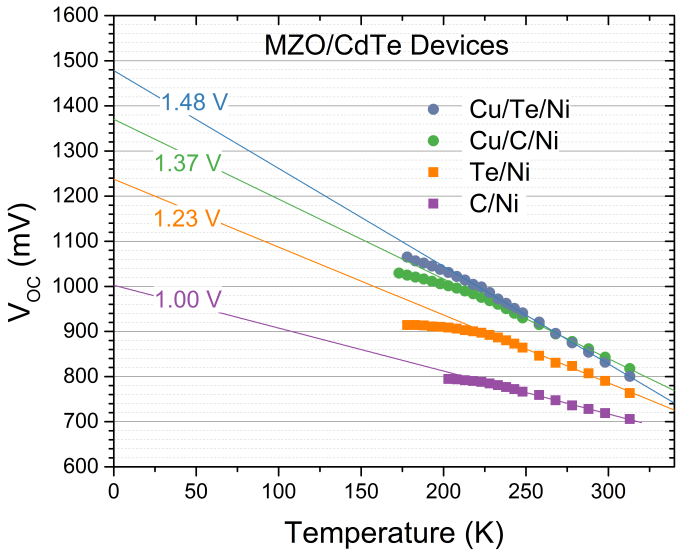

Figure 2.22: V_{OC} versus temperature of MZO/CdTe devices with the C/Ni and Te/Ni back contacts with and without Cu treatment. The activation energy (E_a) of each of the devices is labeled.

2.4 Spectral Photoluminescence of Devices with Te Buffer Contact

Spectral PL was measured on MZO/CdTe devices made on three substrates with the different Cu treatment times in which half of each substrate received the C/Ni contact and the other half got the Te/C/Ni contact (similar to those in Fig. 2.19). The measurements, using a 660-nm wavelength excitation, were performed at First Solar, Inc. and at CSU using a probing wavelength of 520 nm. All measurements were performed on the front side (glass) of completed devices at room temperature (∼300 K).

Figure 2.23 shows the data from the 660-nm wavelength excitation. Regardless of Cu treatment or back contact, there is a primary peak, that is centered around ∼825 nm, which is close to the 1.5-eV band gap of CdTe. As the Cu treatment is increased, the relative intensity of this feature decreases, but the shape does not appear to change. This suggests that the Cu treatment is lowering the lifetime. The better FF seen from lower-Cu devices is likely due to higher lifetime as compared to the standard-Cu treatment.

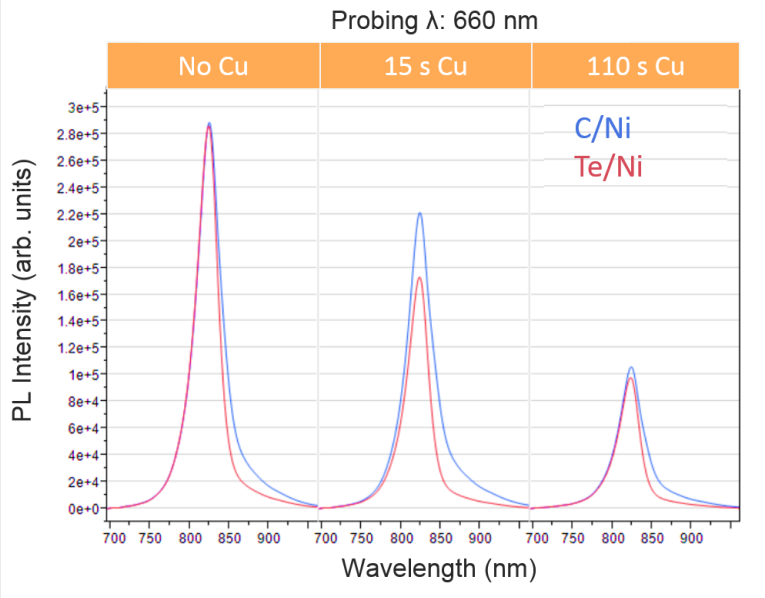

Figure 2.23: PL spectrum from MZO/CdTe devices made on three substrates with the different Cu treatment times (0s, 15 s, 110 s), comparing the C/Ni (blue curve) and Te/Ni (red curve) back contact. Probing wavelength was 660 nm. (Thanks to First Solar, Inc. for providing measurements)

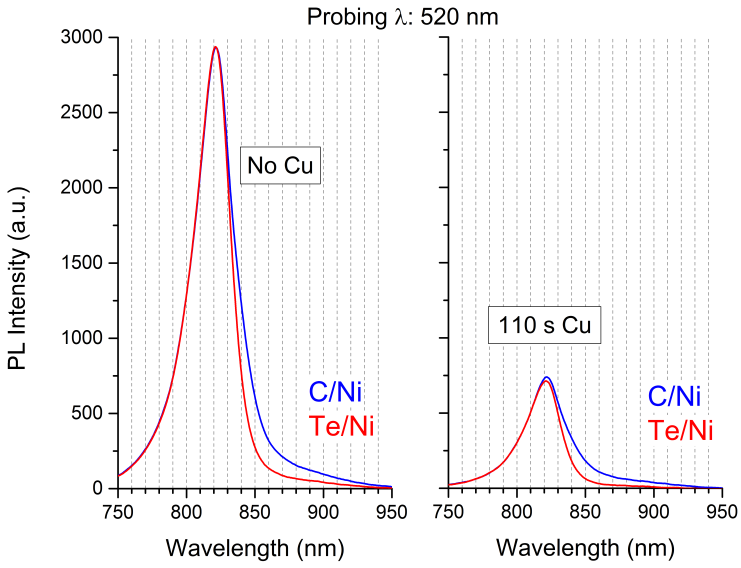

Figure 2.24: PL spectrum from MZO/CdTe devices made on three substrates with the different Cu treatment times and comparing the C/Ni (blue curve) and Te/Ni (red curve) back contact. Probing wavelength was 520 nm.

Comparing the C/Ni contact to the Te/Ni, the shape of the feature does change. The difference is also seen in the PL signal from the same devices using a probe wavelength of 520 nm (Fig. 2.24). The device with the C/Ni contact appears to have an additional lower-energy PL emission. It is not possible to determine the source of this change without performing further PL measurements at lower temperatures and/or using different probing energies. However, the Te is causing a change in the recombination mechanisms in the CdTe, presumably by altering the back surface field and/or passivating/creating defects. Next, the material properties of thin-film Te will be discussed.

2.5 Te Material Properties

This section discusses the material properties of thin-film layers of Te, specifically a 50-nm layer of Te deposited on CdTe by evaporation. Hall measurements were used to extract the carrier density, resistivity, and mobility, which enabled simple band diagram to be constructed using realistic values of the electron affinity and Fermi energy that are representative of Te films fabricated at CSU. The band diagram will be incorporated into device simulation in Section 2.6.

2.5.1 Hall Measurement Results

Various studies, using Hall measurement techniques, have shown that evaporated, polycrystalline Te thin-films (∼100-200 nm) on plain glass exhibit p-type semiconductor behavior [72, 73, 74]. For this study, Hall measurements were performed on Te films (∼40 nm) evaporated at room temperature on three different substrates prepared at CSU: CdTe/MZO/plain glass, Cu-treated CdTe/MZO/plain glass, and plain glass only. The underlying MZO and CdTe layers should not have affected this measurement, since these layers were too resistive to conduct the available probe currents. The values of carrier density, resistivity, and mobility for the Te film on each substrate are listed in Table 2.5.

Table 2.5: Carrier density, resistivity, and mobility of Te thin-films on 3 different substrates.

Substrate	**Carrier Density** ($\mathbf{cm^{-3}}$)	**Resistivity** ($\mathbf{\Omega cm}$)	**Mobility** ($\mathbf{cm^2/Vs}$)
Glass	1.5×10^{18}	1.2	3.3
CdTe/MZO/Glass	5×10^{18}	0.2	5.5
CdTe:Cu/MZO/Glass	3×10^{18}	0.2	9.0

Regardless of the substrate, the Te films were all found to be highly p-type with a bulk carrier density above 10^{18} cm^{-3}, which is in agreement with Capers et al. that reported $\sim 3.8 \times 10^{18}$ cm^{-3} from $\sim 100-150$-nm-thick Te films at room temperature [72]. Transitioning from plain glass to a CdTe underlayer, there is not a significant change in carrier density, however the resistivity drops by an order of magnitude, which may be an effect of the increased roughness of the CdTe surface. The measured mobilities agree well with work by Goswami that reported $\sim$ 3.5 cm^2/Vs for 200-nm-thick Te films [73]. The underlying Cu-treated CdTe surface appears to have little effect on the properties of the Te layer.

2.5.2 Valence Band Maximum of Te (VBM_{Te})

The position the energy bands with respect to the vacuum level is important for constructing accurate energy band diagrams of the device. The valence band maximum (VBM_{Te}) is a convenient energy level to reference. It is the energy difference between the valence band and the vacuum level, i.e. the electron affinity plus the band gap of the material. It can be calculated from the valence band offset (VBO) between CdTe and Te with the knowledge that $VBM_{CdTe} = 5.8$ eV [45]. There have been two published studies by separate research groups to determine the VBO between CdTe and Te using photoemission spectroscopy. Both groups used CSS-deposited CdTe and an evaporated Te layer to create the CdTe/Te interface. In 1995, Niles et al. reported, for a Te film thicknesses above 7.6 nm, a VBO with CdTe of

0.26 ± 0.1 eV and the Fermi level in the Te layer at 0.03 ± 0.05 eV above the VBM, making the Te layer highly p-type [69]. Between 2001 and 2003, Kraft and Fritsche reported, for a film thickness greater than 5 nm, a VBO between 0.4 and 0.5 ± 0.1 eV and the Fermi level in the Te layer at 0.15 ± 0.05 eV above the VBM [75, 76, 77]. Given this range of reported VBOs, the VBM_{Te} should be between ~5.30-5.54 eV. The effect of the VBO on simulated devices as compared to experiment will be explored in Section 2.6.

2.5.3 Simple Te Band Diagram

Thin-films of Te behave like a p-type semiconductor with a low band gap of 0.33 eV at room temperature [78]. The location of the Fermi level with respect to the valence band ($E_F - E_V$) can also be determined by rearranging Eq. 1.2. The density of states for the Te valence band (N_V) has a value of $\sim 7.6 \times 10^{18}$ cm^{-3}, which is calculated using the effective mass of holes, reported to be $0.45m_e$ [66], where m_e is the mass of an electron. This will place E_F approximately ~10-50 meV from E_V for carrier densities in the range for films measured at CSU (~1-5×10^{18} cm^{-3}), which agrees well with the value from Niles et al. [69].

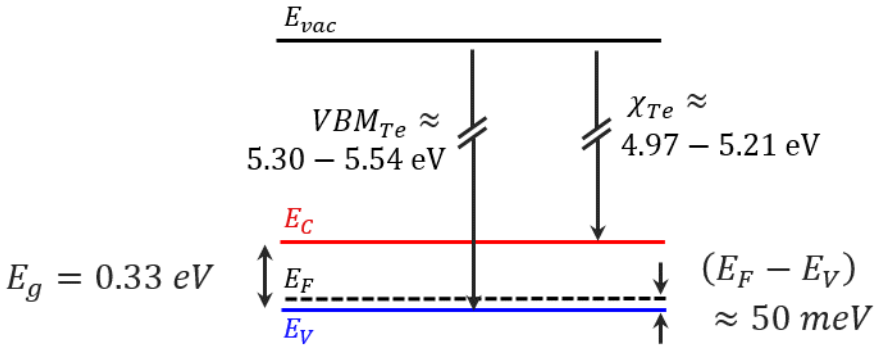

Figure 2.25: Band diagram of Te with band gap (E_g), approximate position of the Fermi level (E_F), and the electron affinity (χ_{Te}) labeled.

The energy band diagram is illustrated in Fig. 2.25. The Te band gap (E_g), the difference between the Fermi level and valence band maximum (E_F- E_V), and the approximate ranges

of the valence band maximum (VBM_{Te}) and electron affinity range (χ_{Te}) are labeled. These properties will be integrated in a device simulation model in the next section.

2.6 Device Simulation with Te Buffer Layer

This section discusses incorporating the Te buffer into device simulation models. The material properties of the previous section were used as input parameters. Simulated device parameters were compared with experiment to reaffirm and narrow the range of unconfirmed material properties. Lastly, a comparison between the J-V results of fabricated and simulated devices is discussed.

2.6.1 Full Device Band Diagrams

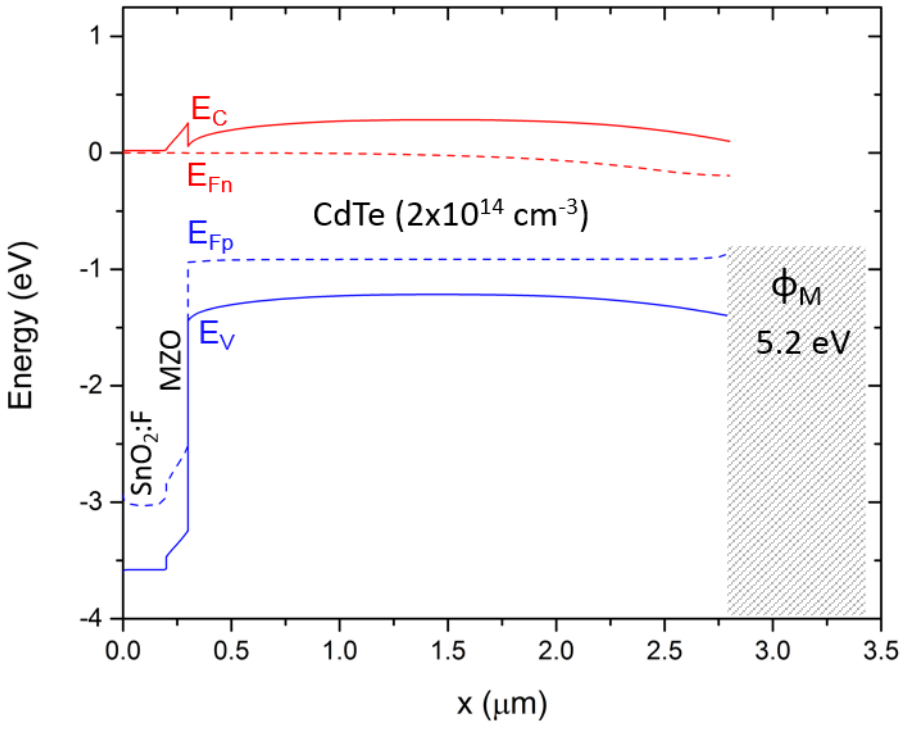

Figure 2.26: Full MZO/CdTe device energy band diagram with Ni-metal back contact.

Simulations were accomplished using SCAPS-1D software, which numerically solves the Poisson equation and continuity equations for electrons and holes for a stack of semiconductor

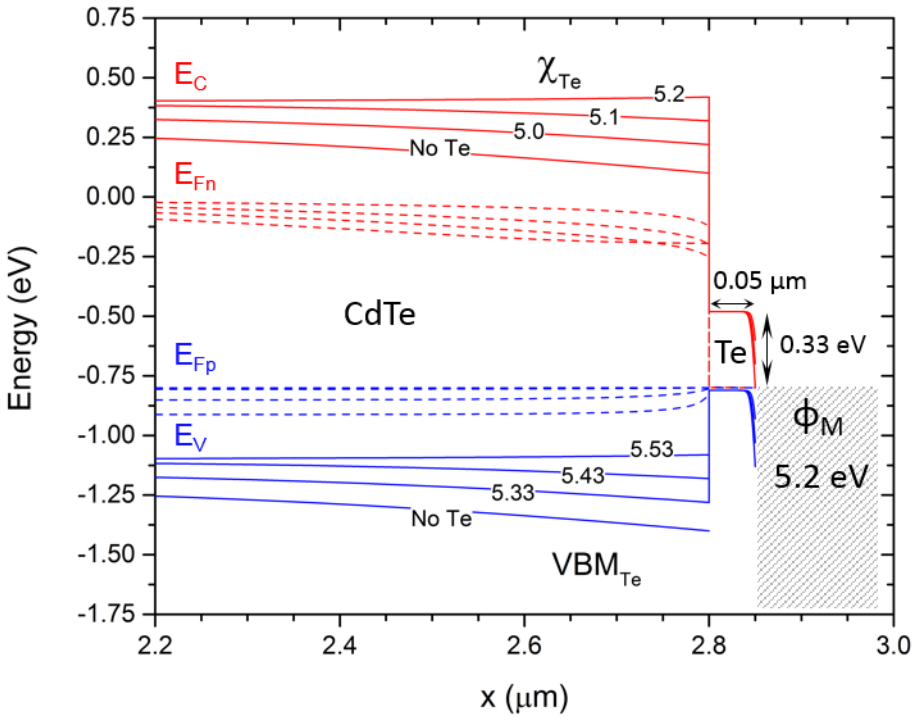

Figure 2.27: Band diagram of CdTe/Te interface with different values of Te valence band maximum and electron affinity of Te (χ_{Te}) along with the Ni back contact. The thickness and band gap of the Te layer are also labeled.

layers [79].The baseline device was modeled on previous work from Song [17]. Figure 2.26 shows the band digram of the base structure (without Te), which consisted of 200-nm of SnO_2:F, 100-nm of MZO, 2.5-μm CdTe, and a Ni (Φ_M = 5.2 eV) back contact. The band picture is shown under forward bias of 0.8 V to illustrate the appearance of near operating conditions. In this diagram, the CdTe is Cu treated, represented by the carrier density of 2×10^{14} cm^{-3} (which may be changed to reflect doping). The 50-nm Te buffer is incorporated into the structure between the CdTe and Ni (Fig. 2.27). For this model, the focus was to study the band alignment of CdTe and Te based on measured values of carrier density. The lifetime of the CdTe was 1 ns for all simulations. No additional defects or interface charges were included.

Figure 2.27 shows the band diagram at the CdTe/Te/Ni interfaces, all at V = +0.8 V, with different values of the valence band maximum of Te: 5.33, 5.43, and 5.53 eV for a Te carrier density of 1×10^{18} cm^{-3}. These values are representative of the measured range from Niles, Kraft and Fritsche [69, 75, 76, 77]. The no-Te-layer bands are shown for comparison. It is evident that as the VBO between CdTe and Te is decreased, the downward band bending at the back of the CdTe is reduced. It should also be noted that while reduced downward band bending may responsible for the performance increase, it may not fully explain the changes in recombination as seen in the JVT and PL measurements. However, for this simulation model, only the band alignment and carrier densities of the CdTe/Te interface were considered.

Furthermore, it should be emphasized that this back contact configuration is distinctly different than a typical semiconductor/metal Schottky diode, which is essentially a p-n junction except the Fermi level of the n-type material fixed at the conduction band. The CdTe/Te/Ni heterostructure is of the p/p+/metal structure. Thus, the Schottky barrier occurs at the Te/Ni interface, but magnitude of the barrier is lower than CdTe/metal due to the lower VBM of Te. The reduced downward band bending between the CdTe and Te is primarily from the band alignment and doping of these two semiconductor layers. The effect of varying the Te carrier density and VBM_{Te} on device performance will be explored next.

2.6.2 Device Simulation versus Experiment

In order to reaffirm and narrow the range of the material properties of Te, simulations were done for a range of VBM_{Te} and carrier densities. The results were compared to average experimental values of devices with similar parameters. The range of Te carrier densities was 1 to 5×10^{18} cm^{-3}, which is the range from Hall measurements on CSU films. The range of VBM_{Te} is the same as that shown in Fig. 2.27.

Two devices were compared: the baseline device with a Te/Ni contact, and the baseline device with Cu/Te/Ni. Over the course of four separate experiments, device structures of MZO/CdTe/Te/Ni without and with Cu treatment (standard—110 s) were fabricated (∼130 devices total). The effect of Cu treatment in the simulation is a change in carrier density of the CdTe. The average carrier density (extracted from C-V) for the Te/Ni and Cu/Te/Ni contacts were $\sim8\times10^{13}$ and $\sim2\times10^{14}$ cm^{-3}, respectively, which were input in the simulation.

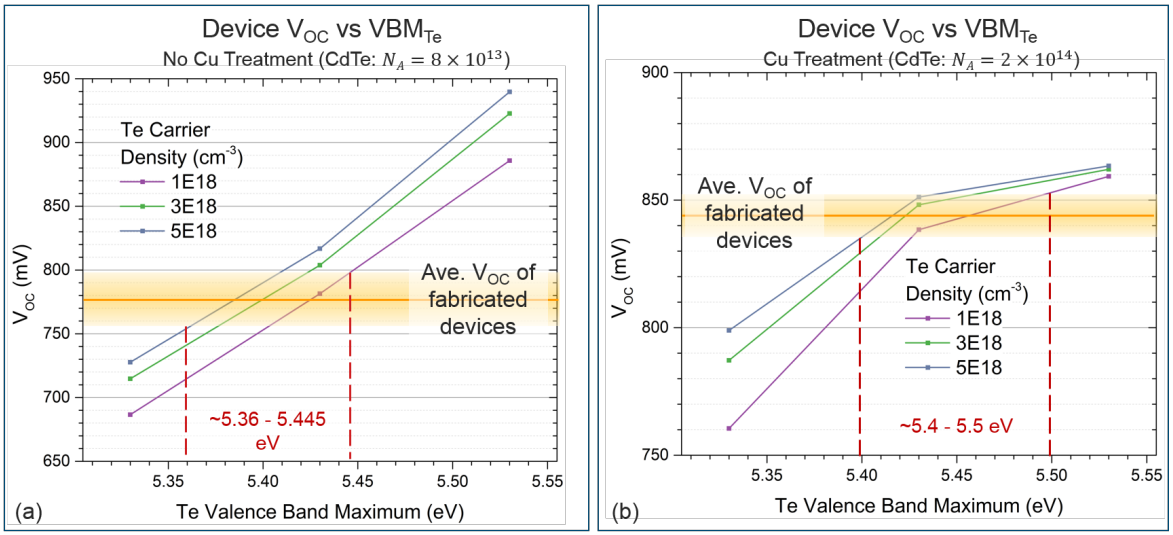

Figure 2.28: Plots of simulated V_{OC} versus Te valence band maximum with different Te carrier densities for no-Cu-treated CdTe (a) and Cu-treated CdTe (b). The average V_{OC} with standard deviation from experimentally measured values is overlaid in order to extract a realistic range of VBM_{Te}.

The V_{OC} of simulated devices for different values of VBM_{Te} are plotted in Fig. 2.28. Each curve represents the carrier density of the Te layer. The no-Cu-treatment devices are shown

in Fig. 2.28a and the Cu-treated devices are shown in Fig. 2.28b. The average experimental V_{OC} of fabricated devices is also shown on the plots, 773 ± 22 mV and 843 ± 9 mV, for Te/Ni and Cu/Te/Ni devices, respectively. Overlaying the average experimental values on the plots of the simulated values allows for the true range of the VBM_{Te} to be narrowed. For the Te/Ni devices, it is between 5.36 and 5.45 eV and for the Cu/Te/Ni devices it is between 5.40 and 5.50 eV. The value of the VBM_{Te} should be the same regardless of the CdTe carrier density. Thus, the value of VBM_{Te} must be in range where the sets overlap, which is between 5.40 and 5.45 eV. This range more closely agrees with the results of Kraft and Fritsche than the work of Niles.

Experimentally, the carrier density of the Te may vary slightly among different substrates. Fig. 2.28 shows that this will cause more variation in the simulated-V_{OC} for the non-Cu-treated devices and may also be the cause for the larger variation in V_{OC} from the experimental values.

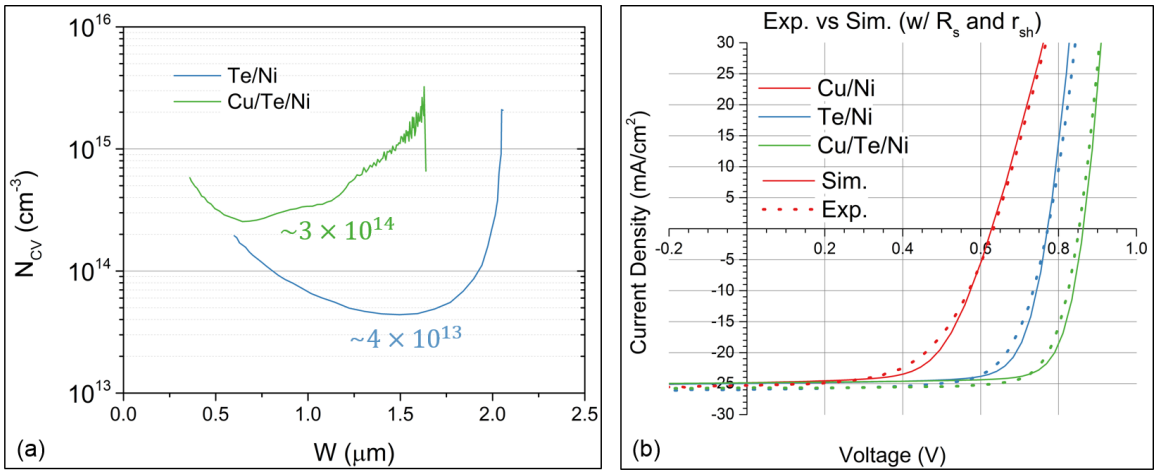

Figure 2.29: (a) The carrier density versus depletion width of the Te/Ni (blue) and Cu/Te/Ni (green) devices used to for comparison with simulation. (b) The experimentally-measured (dotted) and simulated (solid) J-V curves with three different contact methods: Cu/Ni-metal (red), Te/Ni (blue), and Cu/Te/Ni (green).

The full J-V curves from experiment were also compared with simulated results. Three back contact structures were used: Cu/Ni-metal, Te/Ni, and Cu/Te/Ni. The Cu/Ni-metal

device received a sputtered Ni-metal contact after the Cu treatment (device fabricated by Jason Kephart). The simulated Te layer has a carrier density of 3×10^{18} cm^{-3} and a VBM$_{Te}$ of 5.43 eV. The CdTe carrier densities were extracted from C-V measurement for the Te/Ni and Cu/Ni devices (see Fig. 2.29a). The C-V profile was not available for the Cu/Ni devices, and therefore the CdTe carrier density value was chosen based on the agreement of the resulting simulated-V_{OC} to the experimental value. A carrier density value of 1×10^{14} cm^{-3} results in a simulated-V_{OC} of 628 mV, which is nearly the same as experiment, while 3×10^{14} cm^{-3} results in 711 mV, which is much higher than the experimental value. It is to be emphasized that the carrier density of 3×10^{14} cm^{-3} for the Cu/Te/Ni device is a result of the optimized Cu treatment (15 s) and not the Te layer. The Cu/Ni-metal received a 120-s Cu treatment. The series and shunt resistances were extracted from the experimental J-V data and input in the simulation for the respective back contacts. All other parameters in the simulations were identical.

Table 2.6: J-V parameters for MZO/CdTe devices with the Cu/Ni-metal, Te/Ni and Cu/Te/Ni back contacts extracted from the experimental (Exp.) and simulated (Sim.) data.

Back Contact	V_{OC} [V]	J_{SC} [mA/cm^2]	FF [%]	η [%]	r$_{sh}$ [Ωcm^2]	R$_s$ [Ωcm^2]	A
Exp. CuNi	633	25.3	57.4	9.2	1000	3.3	2.6
Exp. TeNi	773	25.9	71.1	14.3	2500	0.8	2.4
Exp. CuTeNi	853	25.7	77.9	17.1	4400	0.6	1.8
Sim. CuNi	628	24.9	64.1	10	900	3.1	1.9
Sim. TeNi	772	25	76.6	14.8	1700	0.8	1.6
Sim. CuTeNi	863	24.9	79.7	17.1	2000	0.5	1.5

Figure 2.29b shows the comparison of the experimental (dotted) and simulated (solid). Table 2.6 shows a comparison of the extracted J-V parameters from the experimental and

simulated results. The Cu/Ni device (red) has a lower V_{OC} than the others, which the simulation suggests is the result of downward band bending caused by the Schottky barrier formed between CdTe and Ni. The addition of Te buffer layer without Cu treatment (blue curve) reduces the band bending and greatly improves the V_{OC}. The simulation calculates that even increasing carrier density to 3×10^{14} cm^{-3} for the Cu/Ni-contact device, which is comparable to the Cu-treated Te/Ni device, the performance will be considerably lower than the Te/Ni-contact device without Cu-treatment (blue). Incorporating a Cu treatment with the Te/Ni-contact (green), will further boost V_{OC} and FF, which is corroborated by the simulation result. In all cases, the FF of the simulation is higher than the experiment, which is likely due to voltage-dependent current collection that is not considered by the simulation. Nonetheless, there is good agreement between experiment and simulation, which suggests that the quantities input for the carrier densities and band offsets are an accurate representation of the true values.

To summarize, MZO/CdTe devices were simulated with the Te buffer-layer contact using experimentally extracted parameters. Comparing the results of experiment and simulation, the realistic range of Te valence band maximum was narrowed, from the values extracted from literature (∼5.30-5.54 eV), to ∼5.40-5.45 eV. A VBM$_{Te}$ value of 5.43 eV was used for input in simulations with the experimentally measured values of carrier densities for CdTe and Te. The experimental and simulated results showed good agreement. The simulation suggests that the reduced downward band bending at the back of the CdTe, from favorable band alignment and high p-type doping of Te, is the physical mechanism by which the Te buffer layer aids in forming a good-performance back contact.

Chapter 3

METASTABLITY OF CdTe SOLAR CELLS

The stability of a solar-cell device is defined as the quantitative changes in the electrical and material properties from their initial values. A stable device will have minimum (or ideally zero) change from its initial state. A device that is metastable has many quasi-stable states, which are a essentially a series of an unstable, local energy-minimums. A metastable device may spontaneously change from a state of higher energy to lower energy. If energy is added to the metastable system, it may also transition to a different local, energy-minimum state.

This chapter focuses on the changes, both positive and negative, in CdTe solar cell device characteristics over time with emphasis of the role of the Te layer. There are numerous factors that may cause a device to behave differently from its original characterization after fabrication. This work will primarily focus on changes caused by diffusion and drift of atoms and charges in the CdTe lattice. As atoms move and/or become ionized their defect states will change, which results in changes in doping and recombination. CdTe devices utilizing the CdS emitter and a Cu treatment, with and without the Te buffer layer, were primarily studied. The changes in storage (equilibrium) and under various applied stress conditions will be analyzed in detail.

3.1 Causes of Changes

Even CdTe solar cells in equilibrium (no illumination at constant temperature) experience changes from diffusion due to nonuniform impurity concentrations and drift from the build-in field from the p-n junction. The drift and diffusion of atoms can be enhanced by elevated temperature, illumination, and voltage bias. This section outlines how these changes occur in general.

3.1.1 Defect Diffusion

Diffusion of atoms in crystal solids primarily depends on the concentrations of atoms in the lattice. The flux (J_X) of particles flows from areas of high concentration to areas of low concentration, as stated by Fick's law:

$$J_{X,diff} = -D_X \frac{d[X]}{dx}, \tag{3.1}$$

where $[X]$ is the concentration of an atomic species X, and D_X is the diffusion coefficient of X [80]. Typically, the diffusion coefficient has temperature dependence and is given by the Arrhenius expression:

$$D_X = D_0 \exp\Big(\frac{-E_X}{kT}\Big), \tag{3.2}$$

where E_X is the activation energy of defect X and D_0 is the maximum diffusion, which depends on the diffusion mechanism, lattice geometry and composition [80]. E_X can be thought of as the energy barrier the defect must over come to move to the next position. D_X is also temperature dependent and the diffusion flux will increase with increased temperature.

There are three basic mechanisms of diffusion: vacancy site jumping, migration through interstitial sites, and interchanging of atoms (interchange movement). Vacancy site jumping is when an atom moves to an unoccupied lattice site that is adjacent to it. Interstitial migration is the movement through interstitial sites. It is generally faster than vacancy jumping due to the larger availability of interstitial sites and weaker interstitial bonding (lower E_X). In CdTe, interstitial defects are the most mobile. Lastly, interchange movement can happen when a defect knocks-off an atom on a lattice site and replaces it [81].

3.1.2 Defect Drift

The flux of charged defects will also be influenced by the presence of an electric field F, such as the built-in potential of the junction. The drift flux of atomic concentration $[X]$ is given by,

$$J_{X,drift} = \theta \frac{D_X}{kT} F[X], \tag{3.3}$$

where θ is the charge carried by the defect [80]. The charge of the defect and the direction of the electric field will determine the direction of the flux, both of which can be affected by external light and/or voltage bias.

3.1.3 Defect and Charge Reaction

As a defect moves in the CdTe, it can react with lattice sites and other defects to form new defects. The interchange diffusion process is technically a type of exchange reaction. Equation 3.4 shows an example of an exchange reaction between interstitial Cu and a Cd atom on a lattice site.

$$\mathrm{Cu_i^+} + \mathrm{Cd_{Cd}} \rightleftharpoons \mathrm{Cu_{Cd}^-} + \mathrm{Cd_i^{++}}, \tag{3.4}$$

If this occurs in the proximity of another $\mathrm{Cu_{Cd}}$, then it can move to the interstitial position and the previously knocked-out $\mathrm{Cd_i}$ can move on the open lattice site [40]. This is essentially the diffusion of the $(\mathrm{Cu_i} - \mathrm{Cu_{Cd}})$ complex.

A complex is formed when two point defects pair together, this is called a combination reaction. The complex will generally have a different energy state and ionization than the separate defects. In p-CdTe, complexes are mostly formed by the pairing of an interstitial defect with a lattice site. Majority of these complexes behave as donors or neutral defects [22], which are detrimental to achieving high acceptor doping in CdTe.

Defects may also react with electrons and holes, resulting in a change of ionization. The rate of this reaction will increase with temperature and the number of excess charge carriers.

3.1.4 Grain Boundary Diffusion

At the grain boundary (GB), the meeting of two grain surfaces, the diffusion of impurities will be much faster than in the bulk material. This is due to the lower bonding energy of the

surface atoms to those in the lattice [82]. The same drift and diffusion mechanisms apply for atoms in the grain boundary, but the diffusion coefficient is likely higher.

As discussed in Sec. 1.3.1, Cl prefers to segregate in the GBs. Mao et al. found that greater than 90% of the Cl in CdTe is found in the GB, thus majority of the movement of Cl will likely be in the GBs. However, the Cl segregation will create a large concentration gradient and diffusion from the GB to the bulk is probable.

Evidence of Cu segregation at the GBs is lacking in comparison to Cl segregation [26, 38]. However Cu present in the GBs, whether it is concentrated in higher quantities than the bulk or not, will diffuse quicker than though the lattice [83, 82, 84, 85].

3.2 Stress Induced Change

The effects of various stress conditions on the CdS/CdTe solar cell device will be discussed in this section. Three primary factors are considered: voltage bias, light bias, and elevated temperature. Figure 3.1 shows an illustrated diagram of a CdS/CdTe junction with (a) a high internal field and (b) a low internal field. The possible atomic flux processes are labeled for the respective internal fields. Fig. 3.1 will be discussed in detail with accompanying energy band diagrams in the following subsections.

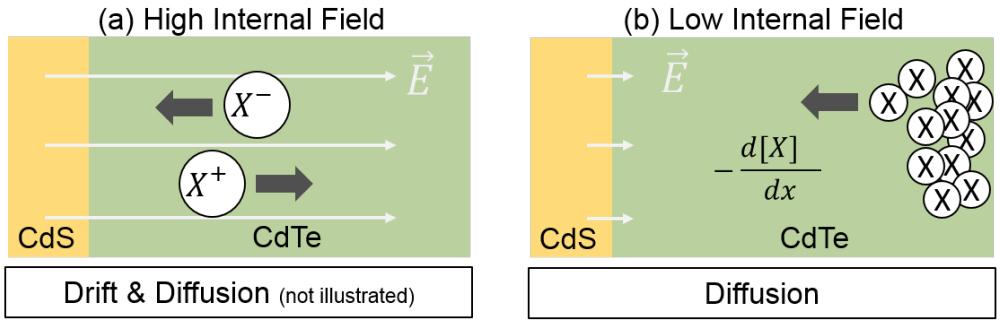

Figure 3.1: Illustrated diagram of a CdS/CdTe junction with (a) a high internal field and (b) a low internal field. The possible atomic flux processes for species X are labeled for the respective internal fields.

3.2.1 Voltage Bias

As discussed in Sec. 1.2.2, voltage bias changes the built-in potential of a diode. With no bias, the internal field points toward the back of the device (Fig. 3.1a and 3.2a). In 2.5-μm CdTe with doping of 10^{14} cm^{-3}, the space-charge region extends through the entire absorber material at zero or negative bias, which is also known as being fully depleted. Mobile positively charged defects will tend to get forced to the back of the device and vice versa for negative defects. In addition to the movement of ions in the field, diffusion can occur due atomic concentration gradients, which may facilitate or compete with the drift of a species. Placing a forward bias on the device will decrease the internal field (Fig. 3.1b and 3.2b), and drift will be reduced. In this work, all forward bias stress is performed at a bias near to the V_{OC} of the device at the respective temperature. This results in a small internal field (less than ~100 mV), and thus atomic diffusion is the primary flux mechanism (Fig. 3.1b).

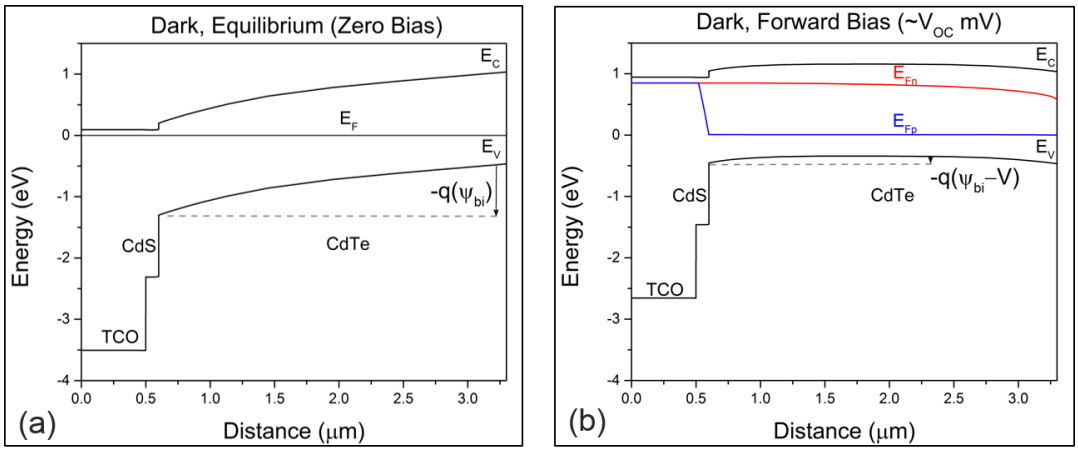

Figure 3.2: Plots of the energy bands of a CdS/CdTe solar cell at different voltage biases in the dark. (a) Zero bias (equilibrium) and (b) forward bias of 850 mV.

3.2.2 Light Bias

Under illumination, the internal field is also affected (Fig. 3.3). If the circuit between the front and back contacts is left open (open-circuit or OC), the photogenerated current must

recombine entirely internally, which results in the lowering of the built-in field (Fig. 3.3b). The open-circuit voltage is the difference between the electron and hole quasi-Fermi levels and its magnitude will be nearly equal to the built-in potential at equilibrium in the dark. When the back and front contacts are shorted (short-circuit or SC), the photogenerated current is able to freely flow and the internal field is equivalent to the equilibrium field (Fig. 3.3a). However, there is much more perturbation occurring inside the bulk of the device due to the spatially dependent photocarrier generation based on the absorption of photons. In contrast to only voltage bias, which injects charges at the front or back of the device, electrons and holes are generated throughout the material under illumination. Thus, the charge-defect reactions will be different for light bias.

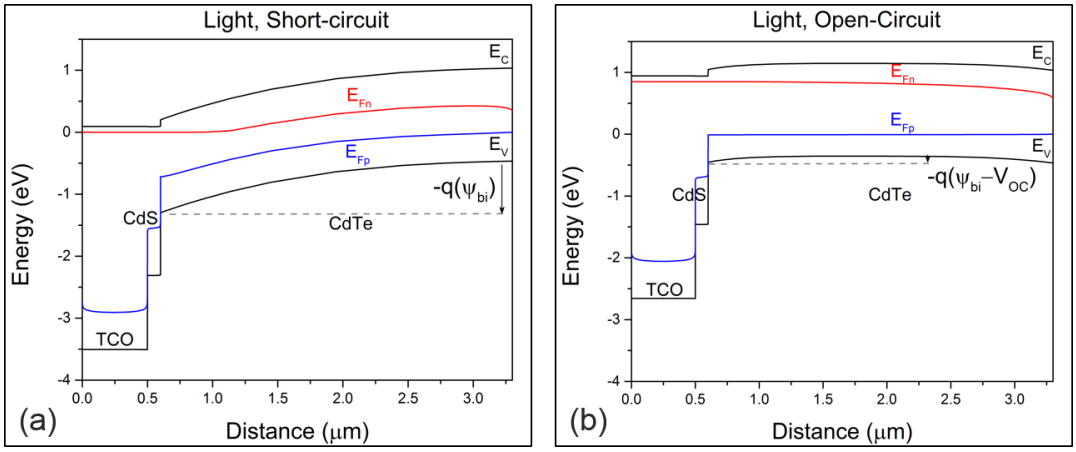

Figure 3.3: Plots of the energy bands of a CdS/CdTe solar cell under illumination for (a) short-circuit and (b) open-circuit conditions.

3.2.3 Temperature

The diffusivity of a defect depends exponentially on temperature. Thus, relatively small changes in temperature can have large effects on changes in a device. The temperature range used in stress experiments in this work is between 60 and 80°C. The elevated temperatures were accomplished by either heating the cells in an oven or contacting to a temperature

stage, which utilized a peltier device with a PID controller. Temperature will also affect changes to devices in storage, which is discussed in the next section.

3.3 Device Changes in Storage

In this work, the initial J-V measurement on each device is typically performed within 24 hours of fabrication. If devices are not being characterized, it is protocol to store the devices in a container (polyethylene box with a tight-fitting, silicone-sealed lid) with desiccant in the dark at room temperature (∼22°C). This section examines changes over time in devices that have been in storage. All measurements were normalized to the initial measured value. All devices examined had a CdS/CdTe primary junction with either a Cu/C/Ni, Cu/Te/Ni, or Te/Cu/Ni back contact with the standard Cu treatment (110 s).

Table 3.1: Mean normalized V_{OC} and FF from devices in storage greater than 5 days for three back contacts: Cu/C/Ni, Cu/Te/Ni, or Te/Cu/Ni.

Back Contact	Mean Normalized V_{OC}	Mean Normalized FF
Cu/C/Ni	0.99 ± 0.01	0.94 ± 0.03
Cu/Te/Ni	0.99 ± 0.01	0.97 ± 0.02
Te/Cu/Ni	1.00 ± 0.01	0.98 ± 0.02

Devices were surveyed from several different fabrication runs in order to account for the possibility of process variations affecting the device metastability. Figure 3.4 shows the normalized V_{OC} (a) and FF (b) versus time after the initial measurement for the three back contacts. The color of each symbol represents the fabrication run number. For both parameters, the amount of change is generally greater as the time increases. Table 3.1 shows the mean normalized V_{OC} and FF for measurement times greater than 5 days for each back contact. For times less than 5 days there is minimal change in the devices.

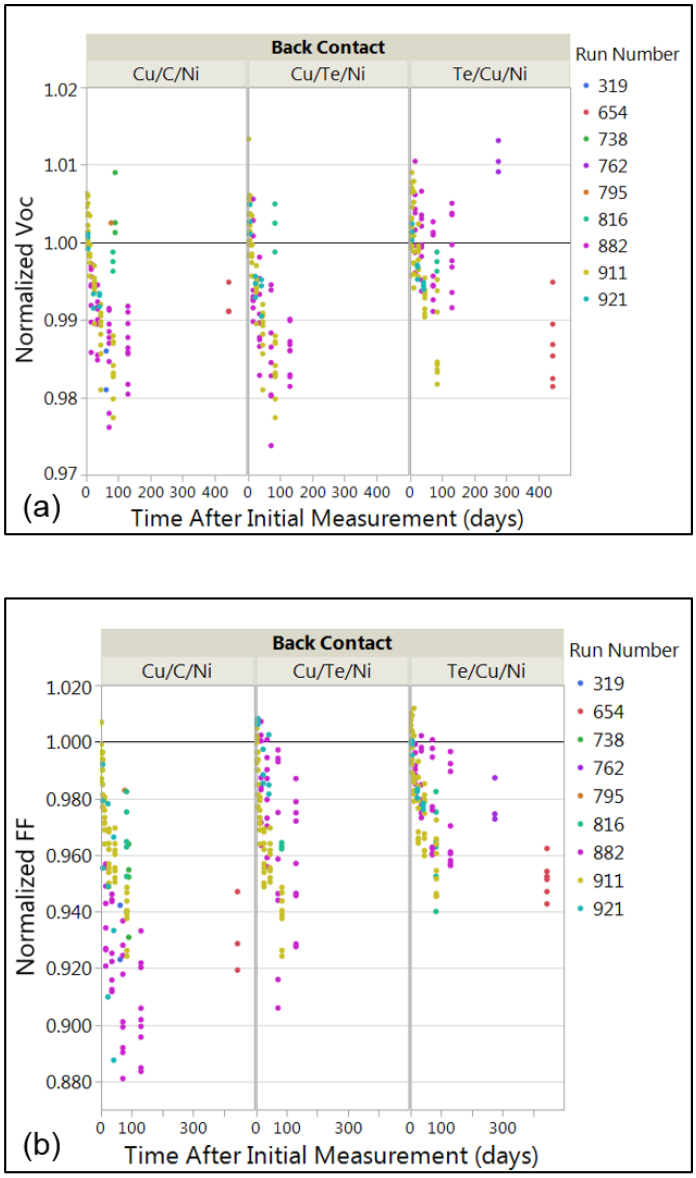

Figure 3.4: Normalized V_{OC} (a) and FF (b) versus time after the initial measurement for devices in storage. Three back contacts were compared: Cu/C/Ni, Cu/Te/Ni, and Te/Cu/Ni. The color of each symbol represents the fabrication run number.

The devices that received Cu treatment directly on the CdTe (Cu/C/Ni and Cu/Te/Ni) showed slightly more change in V_{OC} overall. However, for majority of the devices, regardless of the back contact, the change in V_{OC} is minimal—less than ∼1% loss. In regards to FF, the change is more significant and appears to relate to the device's back contact. The Cu/C/Ni contact showed the most change on average—∼6% loss (Table 3.1). The devices with the Te back contacts showed less loss in FF, with the Cu/Te/Ni showing -3% and the Te/Cu/Ni showing -2%. Overall, the Te/Cu/Ni contact shows the least change in performance.

The source of the primary mechanism for the changes observed in storage was explored. Since the devices are in the dark at a constant temperature, changes due to charge carrier reactions was ruled out. The remaining and most likely mechanisms included: diffusion of impurity atoms, drift of ions in the internal field, and/or moisture/oxygen intrusion.

In order isolate the effects of moisture and oxygen instruction, devices were stored in an Ar environment, with an oxygen level of ∼0.3 ppm and a water level of ∼1 ppm, in dark at room temperature. These devices showed changes on par with those stored in the standard fashion. Thus moisture and oxygen intrusion were not the primary mechanisms causing degradation for devices stored according to standard protocol.

A typical CdS/CdTe device in equilibrium will have a built-in potential between 0.7 and 0.8 V and the electric field will likely extend throughout the entire absorber material for 2.5 μm-thick CdTe. This will put a force on any ionized impurity. There are also concentration gradients of impurities such as Cu and Cl. In order to show that the migration of impurities was the primary mechanism for change, devices were vacuum sealed in polyethylene bags with desiccant and stored in the dark at two temperatures: 8°C and 22°C (standard).

Figure 3.5 shows the average normalized FF for three different back contacts measured at 15 and 130 days after the initial measurement. The black squares represent devices stored at 8°C and the red circles are devices stored at 22°C. The devices stored at the lower temperature showed less degradation in every case. This suggests that the diffusion coefficients of the mobile impurities were reduced with a lower temperature.

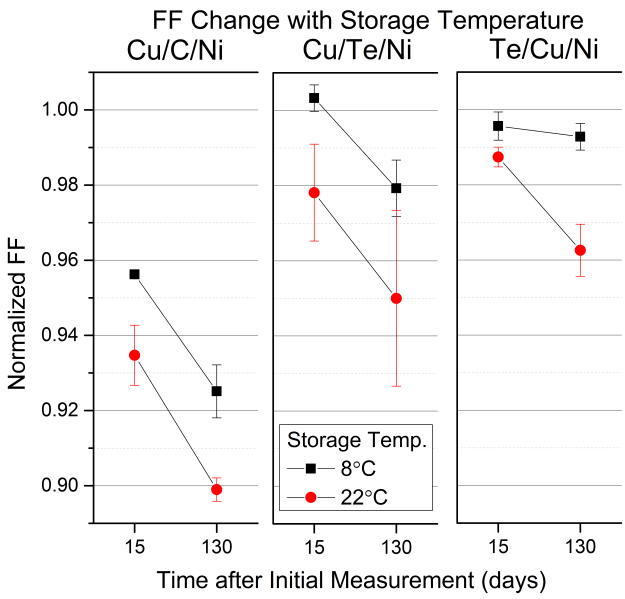

Figure 3.5: Normalized V_{OC} (a) and FF (b) versus time after the initial measurement for devices in storage. Three back contacts are compared: Cu/C/Ni, Cu/Te/Ni, or Te/Cu/Ni. The color of each symbol represents the fabrication run number.

Without performing materials analysis on the samples, it is difficult to know for certain which impurity atoms drifted and diffused in the device. However, hypotheses can be made based on the ionizations of known impurities, their likely concentrations, and the direction of the electric field. Interstitial point defects, such as Cu_i, Cl_i, Te_i and Cd_i, will be the most mobile and readily from complexes with lattice sites.

Cu_i typically is ionized and exist as Cu_i^+, which will tend to get forced towards the back of the device in the presence of a field. Alone Cu_i^+ is a donor which will compensate any net doping due to Cu_{Cd}^-. Cu_i^+ (as long as Cl is present) only favors forming a complex with Cu_{Cd}^- over any other filled lattice site, which won't change the net doping but may passivate Cu_{Cd}^- as a recombination center. Mobile Cl will exist as both Cl_i^+ and Cl_i^- which will form neutral complexes with each other. Cl_i^- will also form a complex with Cl_{Te}^+, which effectively neutralizes its donor behavior. Either ionization of Cl_i will readily pair with any ionization of Te_{Cd}, forming a neutral complex and likely passivating the Te antisite recombination center. Lastly, Cl_i will also form the most detrimental complex with Cu_{Cd}^-, which is a double donor

[22]. The defects of Te_i and Cd_i will be present in lesser quantities and will not be considered for this work.

Regarding Cu, numerous studies have been published on the high mobility of Cu_i in CdTe and stability issues associated with it [40, 86, 87, 82, 88, 89, 90]. However, few studies have considered the possible compensation and migration of Cl_i One possible explanation of the changes observed in devices at equilibrium is Cu_i pushed out of junction area, leaving Cu_{Cd} which increases p-type doping. But Cu_{Cd} is a known recombination center [44], which allows more recombination in the junction region—the area where most charge generation occurs. Cu_{Cd} may also be compensated by Cl_i, resulting in a net loss in doping. Thus, any increased doping near the junction should improve V_{OC} but it is countered by compensation in the bulk and additional recombination centers, which appear to have a larger effect on the FF. The next section further explores these phenomenon by introducing external biases on the devices.

3.4 Short-Term Stress (STS) Experiments

This section discusses changes in devices under various stress conditions over a period of ∼30 hours. This stress duration was labeled as short-term stress (STS) in contrast to the longer-duration stress experiments (∼1000 hrs) which are discussed in Sec. 3.5. The STS experiments were designed to study the changes that occur over time periods of hours as opposed to days. It is to be emphasized that these STS experiments do not represent the conditions that a solar panel would likely experience in the field, nor was that the intention. These studies were carried out with the purpose of providing experimental feedback for a simulation modeled being developed by collaborators at Arizona State University [91, 92]. These experiments also provided validation and further insight into the causes of changes in devices in storage, in addition to comparisons of stability for different Cu treatments.

The short-term stress experimental set-up utilized a temperature-controlled stage and a standard solar simulator lamp for illumination. The device was in direct contact with stage, which allowed for precise temperature monitoring and control of each sample. The light

source for the light bias stress was the same used for J-V measurement and closely resembled the AM1.5 spectrum. Utilizing this arrangement, it allowed the in-situ measurement of the stressed device. By measuring the performance at elevated stress temperatures, the effects of cyclic heating and cooling the sample for measurement were removed. For STS experiments, only J-V data under illumination at 60°C was measured periodically for ∼30 hours of the stress condition. All STS data is presented in the form of normalized J-V parameters, which are normalized to the measured values at the initialization of the stress condition.

Before measurement, all devices are pre-stress conditioned in the dark for ∼15 hours at either 0 V or +0.7 V bias. The purpose of the precondition was to put all devices in the same state before stress measurement and also compare changes during stress for different pre-stress states. Once the measurement period began, the light shutter was opened and a J-V curve was measured. The individual measurements took ∼40 seconds each. If the device was to be stressed in the dark, the light shutter was immediately closed after measurement and light was only exposed to the sample while the J-V measurement was in progress. If light stress was also incorporated, the shutter remained open for the entire stress duration. For the devices stressed in the light at short-circuit, the device was shorted immediately after each J-V measurement. For the devices stressed in the dark at forward bias, the bias was immediately reapplied after J-V each measurement. The temperature for all pre-stress and stress conditions was 60°C, which had the effect of increasing the diffusion coefficient of the impurity atoms.

The STS discussion is organized into two subsections. The first compares the changes in J-V parameters for one precondition and one stress condition for two CdS/CdTe/Cu/Te/Ni devices with different Cu treatment times: standard (110 s) and low (15 s). The second section compares two different preconditions and four different stress conditions for one device structure (CdS/CdTe/low-Cu/Te/Ni).

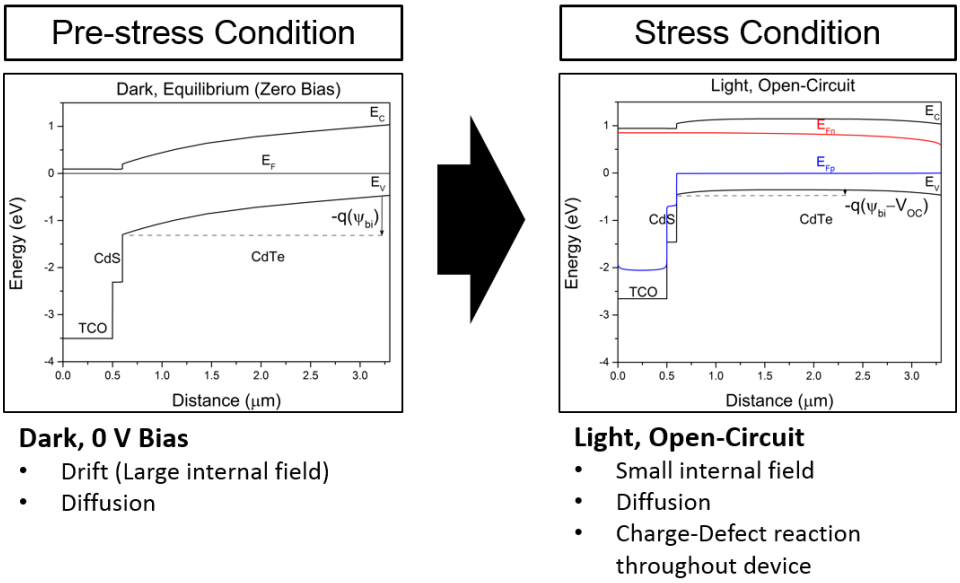

Figure 3.6: Diagram showing the energy bands and descriptions of the possible mechanisms of change for the pre-stress condition and the stress condition for the two CdS/CdTe devices with standard (110 s) and low (15 s) Cu treatments and the Te/Ni back contact.

3.4.1 Low versus Standard Cu Treatment Devices

This section explores the performance differences from STS in typical CdS/CdTe solar cells with a standard Cu-treated device (110 s) versus one with a shorter (15 s) Cu treatment and the Te/Ni back contact. Figure 3.6 shows the pre-stress and stress conditions. The precondition was 60°C in the dark at equilibrium for ∼15 hours. The stress settings were: 60°C, 1 sun illumination, and at open-circuit. Also listed in Fig. 3.6 are the possible mechanisms of change for each bias condition.

Figure 3.7 shows the normalized changes in V_{OC} (black squares), J_{SC} (red circles), and FF (blue triangles) over the duration of the elevated temperature and light stress for the standard (Fig. 3.7a) and low (Fig. 3.7b) Cu treatment devices. In both samples, the first measurement after the initial exposure to light showed an abrupt change in V_{OC}. This is possibly evidence of a relatively fast change in the device due to charge-defect reactions from photogenerated carriers. The low Cu device showed less of a loss in V_{OC}, which correlates to the amount of Cu in the device, followed by a greater relative increase over time. In regards

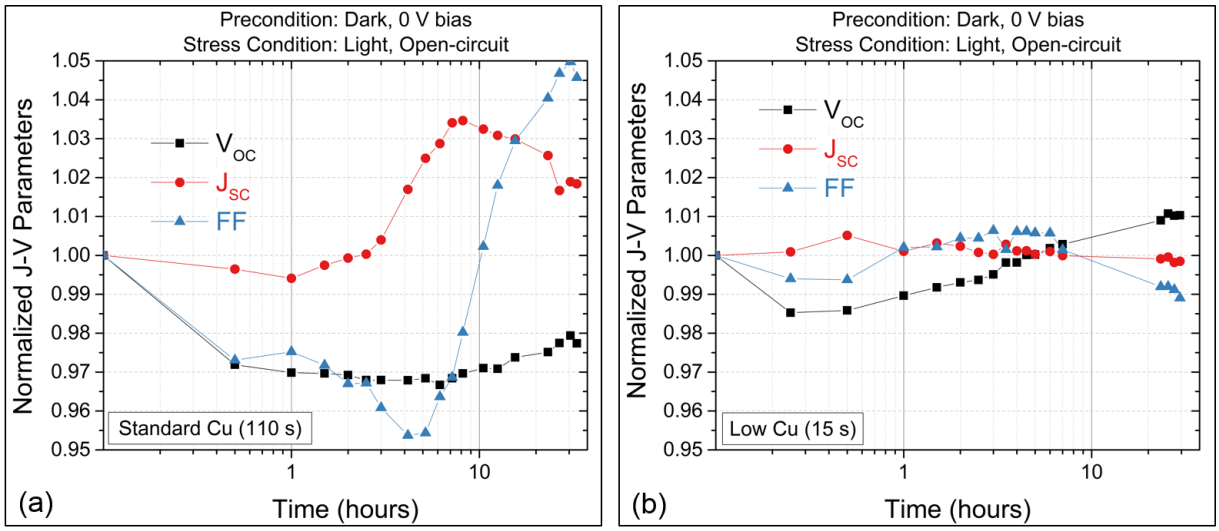

Figure 3.7: V_{OC} (black squares), J_{SC}(red circles), and FF (blue triangles) versus the stress duration for CdS/CdTe/Cu/Te/Ni devices with (a) standard (110 s) and (b) low (15 s) Cu treatment.

to FF, the standard-Cu device showed a steady decrease of ∼5% followed by a sharp increase to ∼5% greater than the initial measurement. After ∼3 hours of stress for the standard-Cu device, the J_{SC} increases by ∼3% before slightly decreasing around 10 hours. The low-Cu device had much less change in all parameters, typically ∼1% absolute.

The standard-Cu device appears to have been shifting to a metastable state for the first 5-6 hours of stress, after which an unstable tipping point was reached, signified by the changes in J_{SC} and FF. This caused a consistent change in the device over the next ∼15 hours, where the device appears to have reached another metastable state at ∼27 hours. Note that, from Sec. 2.2.4, the standard-Cu device has about twice the amount of Cu as the low-Cu device. Thus, the standard-Cu device likely has many more mobile Cu atoms to cause shifts in the spatial doping and recombination profiles. This comparison of the changes in J-V parameters of the two nominally identical devices with different Cu treatments clearly shows that the amount of Cu in the device relates to its stability. The next section explores the affect of various stress conditions on the low-Cu device only.

3.4.2 Low Cu Treatment Devices versus Stress Condition

This section examines various stress conditions on typical CdS/CdTe solar cells with low Cu treatment (15 s) and the Te/Ni back contact. All of the devices were delineated on the same substrate, and thus had the same processing conditions. They had relatively similar current-voltage curves at room temperature with a J_{SC} of 22.0 mA/cm^2, V_{OC} of 761 mV, fill-factor of 70.7%, and efficiency of 11.8%.

Before the measurement cycle began, all the devices were preconditioned under the same settings so that the initial conditions of the devices would be similar. Two preconditions were compared (Fig. 3.8, Col. I): dark at 0 V and +0.7 V (forward) bias for ∼15 hours. Four stress conditions, after the respective preconditions, were also compared (Fig. 3.8, Col. II): light at open-circuit (OC), light at short-circuit (SC), dark at 0 V bias, and dark at +0.7 V bias. The temperature for both the preconditioning and stress was 60°C.

The possible mechanisms responsible for change at each condition are listed in Fig. 3.8, Col. III. The internal field for the light at open-circuit and dark at +0.7 V bias will be approximately the same (small). Similarly, the internal field for cells in the light at short-circuit and for those in the dark at 0 V bias will be approximately the same (near the built-in voltage). Even when the internal fields are the same, there can be differences in the changes caused by light stress compared to dark. This is due to reactions from photogenerated carriers being created throughout the devices under light bias versus carriers only injected carriers at the back and front (or none at all for 0-V bias) for devices in the dark.

Zero-Bias Precondition

Figure 3.9 shows the normalized changes in V_{OC} and FF over the duration of the four different stress conditions for the devices that were preconditioned with zero voltage bias in the dark for ∼15 hours. The plots with the same symbol shape have approximately the same internal field (squares have a small field and triangles have a large field). For the dark at 0 V bias, there is little or no change in V_{OC} or FF, which is likely because the device reached a

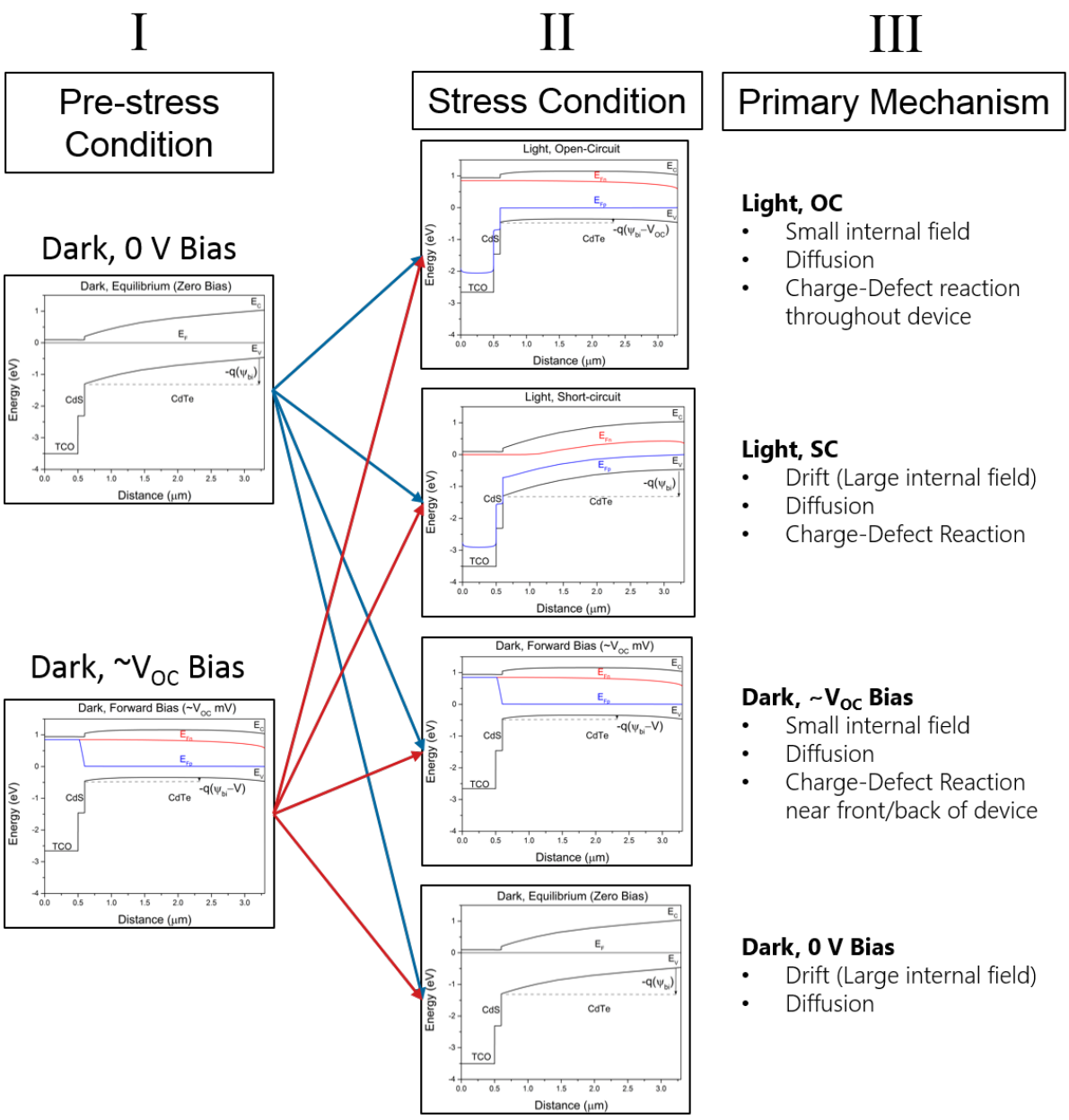

Figure 3.8: Diagram showing the energy bands and descriptions of the possible mechanisms of change for the pre-stress conditions (0 V and +0.7 V bias in the dark) and the stress conditions (OC and SC in the light, and 0 V and +0.7 V bias in the dark) for the CdS/CdTe/low-Cu/Te/Ni devices discussed in this section.

metastable state during the identical preconditioning. However, we see an increase in both V_{OC} and FF for the device that was stressed under forward bias in the dark. The trend of increase is similar to the light OC after the initial decrease observed in the light-stressed device. This may suggest a fast change in the devices caused by the photogenerated carrier interactions, followed by diffusion-related changes that remain dominant over the remaining duration of the stress.

Under a small internal field (dark-forward-bias stress), the interstitial Cu(+), that was pushed out of the junction region from the larger internal field during storage and preconditioning, was able to move back into that area. Doping by Cu_{Cd} near the junction may become compensated, but overall this will create a more uniform carrier density profile throughout the CdTe and possibly less recombination near the junction area from Cu_{Cd}. The simulation suggests that this will increase FF as seen in Fig. 3.9 [91]. Recent evidence from Krasikov suggests that Cl plays a large role in doping compensation due the formation of the Cl_i-Cu_{Cd} complex (a double donor) [22]. Interstitial Cl may exist as either a positive and negative ion. It is postulated that during precondition, Cl_i^+ may migrate to the rear of the device and reduce doping, causing loss in both V_{OC} and FF. This process is reversed once the field in reduced.

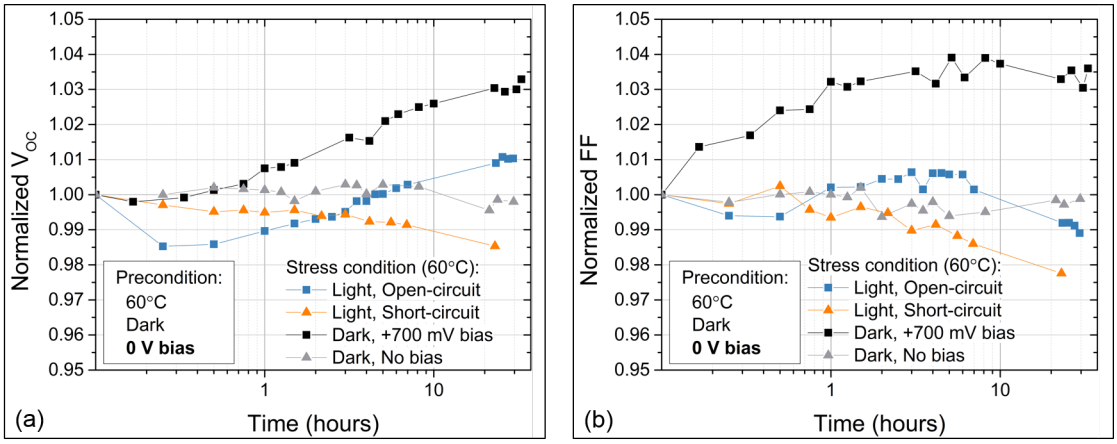

Figure 3.9: V_{OC} (a) and FF (b) versus the stress duration for CdS/CdTe/Cu/Te/Ni devices with 0 V bias precondition and four different stress conditions: OC and SC in the light, and 0 V and +0.7 V bias in the dark.

Forward-Bias Precondition

Figure 3.10 shows the normalized changes to V_{OC} and FF over the duration of the four different stress conditions for the devices that were preconditioned with +0.7 V voltage bias in the dark for ∼15 hours. The devices and the stress conditions are essentially identical to those discussed the previous section, the only experimental difference is the precondition, i.e. a small internal field versus a large internal field.

Beginning with the devices with low internal field during stress (squares in Fig. 3.10), the forward-biased dark-stressed device shows little change in V_{OC} and FF (as expected due to the identical precondition). The light-OC-stressed device (with similar internal field) also shows little change in V_{OC} and FF after a small initial drop in V_{OC}, which may be induced by photogenerated carriers. For the devices that had a large internal field during stress (triangles in Fig. 3.10), both showed loss in V_{OC} and FF. For the FF, both showed relatively similar degradation trends in FF, which hints that this was due to the migration of ions in the internal field. The light-stressed SC device showed an initial drop in V_{OC}, similar to the light-stressed OC device, followed by a consistent decrease in V_{OC}. For the 0-V biased device in the dark, it takes approximately a day for significant changes in V_{OC} to occur, but then the degradation parallels the light-SC-stressed device, suggesting it is caused by the internal field pushing Cu_i and Cl_i ions towards the back.

Overall, the data shows that a small internal field (forward bias in the dark or OC in the light) stress condition after a large internal field (zero bias in dark) precondition tends to improve both voltage and FF, especially for dark stress. It is also found that a large internal field (zero bias in the dark and SC in the light) stress condition after small internal field (forward bias in the dark) precondition tends to reduce both voltage and FF by similar amount. These findings also suggest a method to recover device performance losses induced from long-term storage.

The internal field appears to be dominant mechanism for change for diffusion and drift of atomic species. Additionally, light stress after dark preconditions tends to show greater

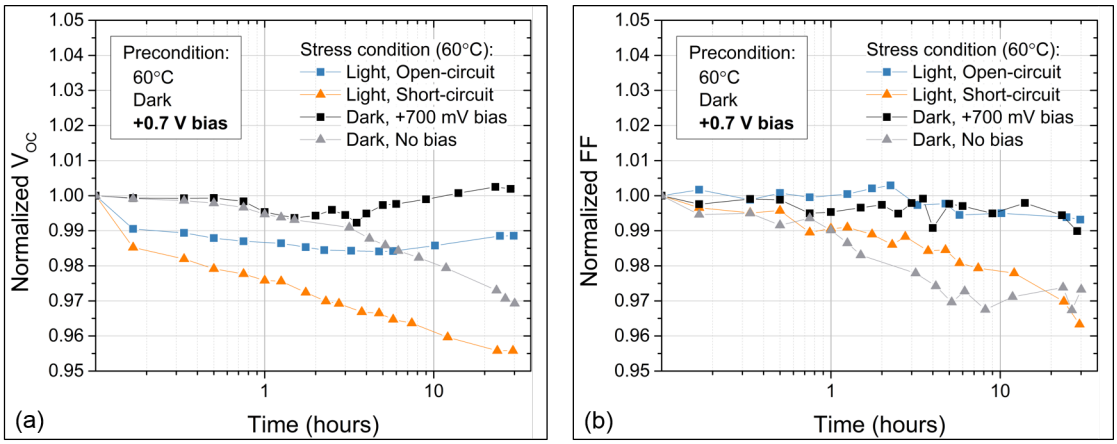

Figure 3.10: V_{OC} (a) and FF (b) versus the stress duration for CdS/CdTe/Cu/Te/Ni devices with +0.7 V bias precondition and four different stress conditions: OC and SC in the light, and 0 V and +0.7 V bias in the dark.

initial change, which is likely due to charge-defect reactions from the photogenerated carriers. The next section will explore the changes in devices over a much longer period of stress.

3.5 Long-Term Stress Experiments

Long-term stress (LTS) refers to solar cells that were stressed for approximately 1000 hours. It is to also be emphasized that these LTS experiments only roughly represent the conditions that a solar panel would likely experience in the field. LTS was meant to push devices towards end-of-life states that panels might experience after decades in the field.

For LTS experiments, devices were stressed in an accelerated life tester (ALT). The ALT consists of an oven, which serves as the heat source and enclosure, that is fitted with broad-spectrum LEDs, which provide the light bias and are calibrated for 1 sun illumination [93]. A LabVIEW program maintains the temperature in addition to an electronic record of the temperature and humidity of the system. Once the ALT reaches stress temperatures (65°C - 80°C), the relative humidity measures ∼0%. An air circulation system is incorporated in the enclosure to promote temperature uniformity. The cells may also be short-circuited or left open-circuit. During LTS, all data was collected at room temperature (∼25°C), which

requires removing the cells from the ALT and cooling before measurement. This allows for QE and C-V measurement to be performed in addition to J-V.

All cells where typical CdS/CdTe devices with the standard Cu treatment. Only light-stress data will be presented. The first subsection examines OC versus SC stress at 65°C and compares the Cu/C/Ni and Te/Cu/Ni back contacts. The next subsection discusses only OC stress at 80°C and compares Cu/C/Ni, Te/Cu/C/Ni and Cu/Te/C/Ni back contacts.

3.5.1 65°C, Illuminated - Open-circuit versus Short-circuit

For this stress experiment, nominally identical cells of the CdS/CdTe structure were exposed to elevated temperature (65°C) and 1 sun illumination for a period of ∼1000 hours. For this stress condition, two different back contacts were studied: Cu/C/Ni and Te/Cu/Ni. Both devices received the same Cu treatment, however the Te layer was deposited before Cu treatment in this experiment. For each respective back-contact, a device was left open-circuit and another was put in short-circuit. The comparison of OC versus SC-stress will be discussed for the individual contacts followed by a comparison of the changes related to the back contacts. No precondition was used, but all devices were in standard storage (described in Sec. 3.3) for the same amount of time before stress was applied.

Cu/C/Ni Contact

Figure 3.11 shows the J-V curves of the Cu/C/Ni back contact device measured periodically during the duration of the OC (a) and SC (b) stress. The initial J-V curves for the stressed devices were essentially identical. Figure 3.11c shows a comparison of the pre-stress and post-stress J-V curves after nearly 1000 hours under their respective stress conditions. While the J-V curves at the conclusion of the stress are similar, the OC-stressed device shows better V_{OC}, but reduced J_{SC} as compared to the SC-stressed device. Looking at V_{OC} and FF versus stress time (Fig. 3.12), the OC-stressed device has an initial period of degradation, followed by a recovery, which is similar to the results from STS in Sec. 3.4. After ∼30

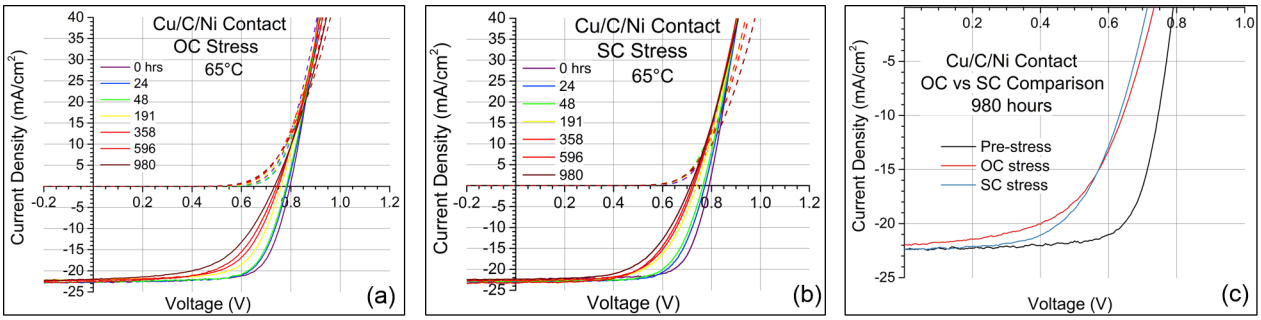

Figure 3.11: Plots of the J-V curves of CdS/CdTe cell with Cu/C/Ni back contact stressed at 65°C under illumination at (a) open-circuit and (b) short-circuit, along with a pre/post-stress comparison of both stress conditions (c).

hours the OC-stressed device shows a gradual degradation in FF. The SC-stressed device only shows a gradual decrease from the inital value in both parameters.

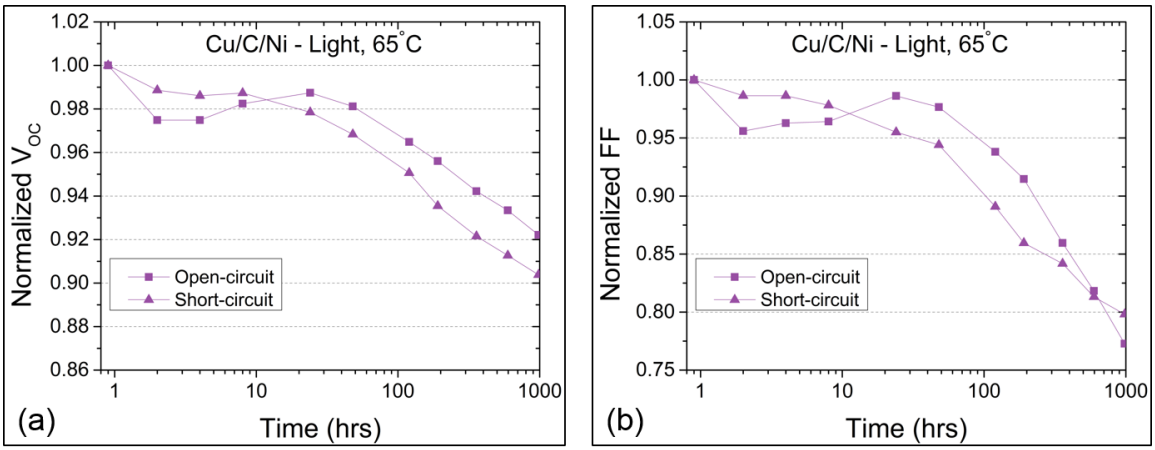

Figure 3.12: Plots of the V_{OC} (a) and FF (b) versus amount of time stressed of a CdS/CdTe cell with Cu/C/Ni back contact at 65°C under illumination at open-circuit and short-circuit.

Examining the QE curves (Fig. 3.13), the OC-stressed device does show a slightly reduced QE in the shorter wave length regions, which typically implies reduced collection near the junction. The SC-stressed device has practically the same QE response pre and post-stress. The QE response for both stress conditions agrees with the J_{SC} observed in the J-V measurements.

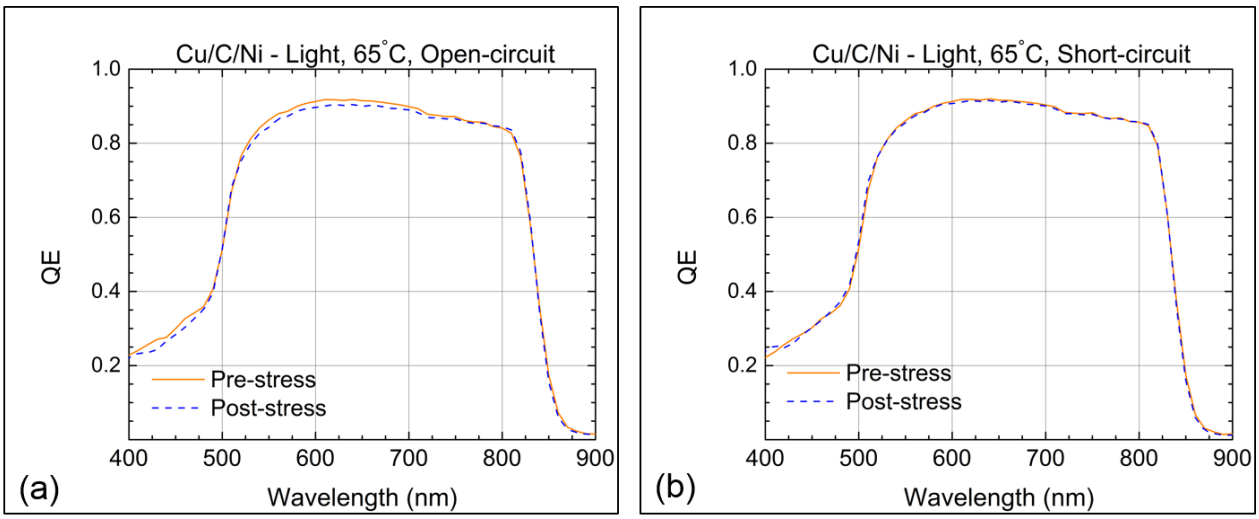

Figure 3.13: Plots of the V_{OC} (a) and FF (b) versus amount of time stressed of a CdS/CdTe cell with Cu/C/Ni back contact at 65°C under illumination at open-circuit and short-circuit.

Figure 3.14 shows the carrier density (N_{CV}) versus depletion width (W) of the devices (extracted from C-V measurements). These plots are the first obvious clue that the respective stress conditions degraded the devices differently. The carriers in the OC-stressed device appear to marginally increase while the SC-stressed device slightly decreased. The significant features between the devices were the differences in the size and location of the SCR over time. The depletion region of the OC-stressed device became narrower, while the depletion width of the SC-stressed device stayed approximately the same size but the region is shifted towards the back of the device.

The SIMS depth profiles for Cu and Cl give insight to changes in concentrations of the two primary impurities in the CdTe (Fig 3.15). Note that the concentration value for each element is only valid in the CdTe region. In the region marked as CdS, the magnitudes of the curves can be compared but the actual concentration values are not legitimate. Also, note that these SIMS measurements were performed to measure bulk concentrations, thus 100-300 nm of the back surface of the CdTe was removed with mechanical polishing. This back layer contained a larger amount of Cu, which would have skewed bulk measurement.

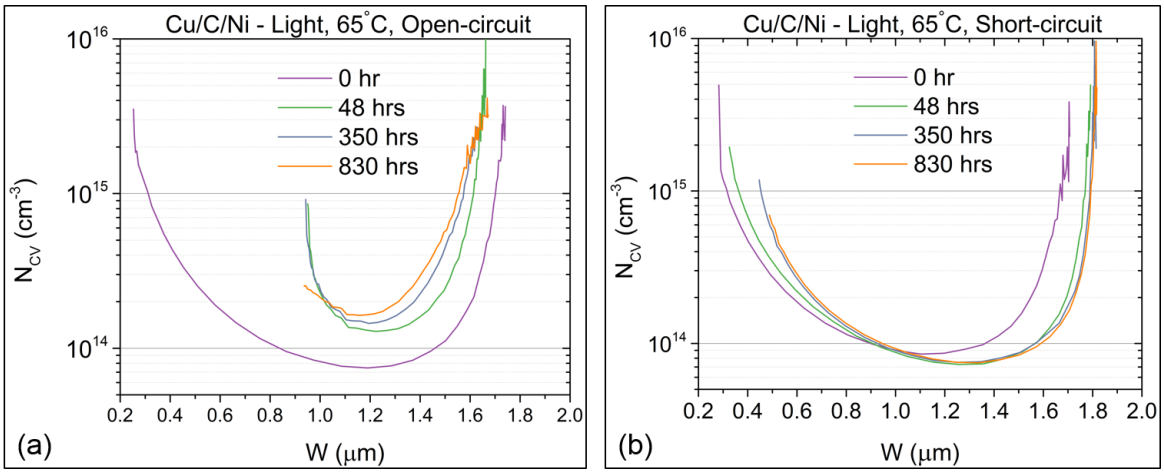

Figure 3.14: Plots of the carrier density (N_{CV}) versus depletion width (W) of a CdS/CdTe cell with Cu/C/Ni back contact at 65°C under illumination at open-circuit (a) and short-circuit (b).

For the OC-stressed device the bulk concentration of Cu is mostly unchanged, but the concentration near the junction is increased along with the magnitude of ion counts in the CdS layer. The field in the device is close to zero at open-circuit and Cu_i^+ would be free to diffusion into these areas. Cu_{Cd} is a p-type dopant in CdS and has also been associated with making the CdS photoconductive [94, 82, 95, 96], which will increase the device resistivity in the dark. Increased series resistance in the circuit can cause the apparent depletion width to shrink in forward bias. The additional Cu in the junction area is likely also causing the increased recombination [44], which may account for the QE loss. In Fig. 3.15(b), Cl from the junction is diffusing towards the back of the OC-stressed device. Majority of the Cl that migrated is likely the more mobile interstitial state, which will highly compensate doping at the back of the device by creating the $(Cl_i - Cu_{Cd})^{2+}$ double donor complex [22]. Thus, reducing doping in both the back and front of the device, while the middle remains relatively the same or slightly increased, will also cause the depletion width to shrink.

With the SC-stressed device, there is a decrease in bulk Cu concentration from approximately 1×10^{18} cm^{-3} (pre-stres) to 3×10^{17} cm^{-3} (post-stress), and the apparent carrier

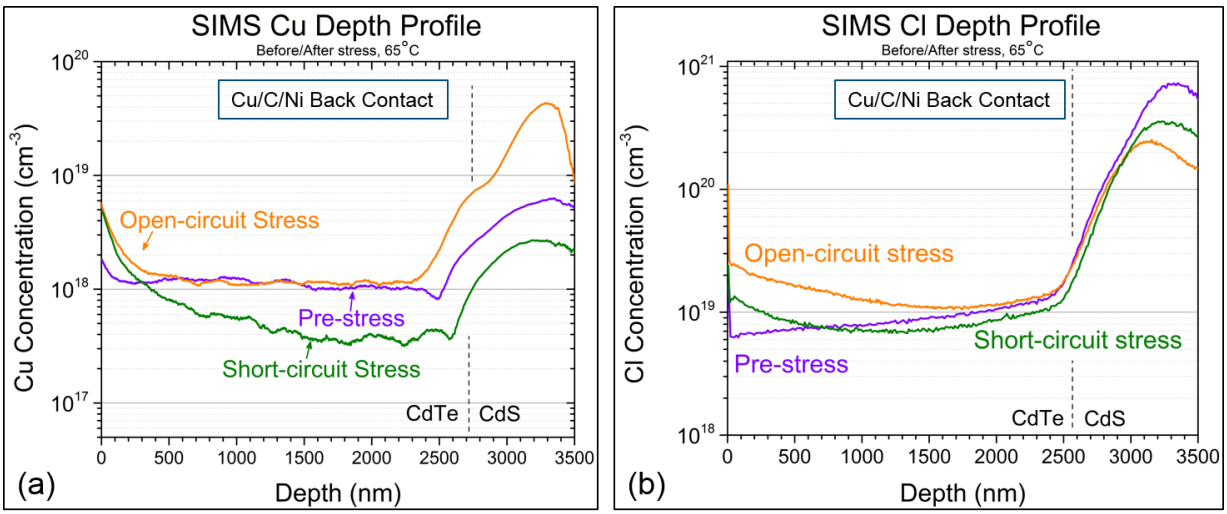

Figure 3.15: Plots of the SIMS depth profiles of the Cu (a) and Cl (b) concentrations pre and post-stress of a CdS/CdTe cell with Cu/C/Ni back contact at 65°C under illumination at open-circuit and short-circuit. (Performed at First Solar, Inc.)

density only changes from 9×10^{13} cm^{-3} to 7×10^{13} cm^{-3} For this to occur without a significant change in carrier density, both Cu_i and Cu_{Cd} would need to migrate out of the area. The internal field from the device being at short circuit will tend to push Cu_i^+ towards the back, which likley reduced the p-type doping in that area. Cu_{Cd} may also move through the exchange reaction proposed by Krasikov et al. [40]. The amount of Cu in the CdS layer is also reduced which possibly improved its n-type doping. The combination of these could have the effect of shifting the depletion area towards the back of the device with little change in carrier density. There was also Cl loss in the CdS and near the junction. The field likely impeded Cl_i^- from leaving and assisted Cl_i^+ migration from the junction area towards the back, in contrast of the ability for diffusion of both ionization states of Cl in the OC-stressed device.

Overall, it is very interesting that these two devices experienced very different stress mechanisms and both yielded similar performance. However, the duration of the test period was arbitrary and it is likely that if the stress was continued their states would have been more distinctly different. For the OC-stressed device the main detrimental mechanisms were the accumulation of Cu in the front junction and CdS and Cl at the back of the device.

With the SC-stressed device, the migration of Cu in the bulk to the back appeared to be the leading cause of degradation. Next, we'll explore these same stress conditions on the Te/Cu/Ni back contact.

Te/Cu/Ni Contact

For the following discussion, the stress conditions and base devices the were identical to the previous subsection, but the back contact was the Te buffer layer followed by the standard Cu treatment and Ni paint (Te/Cu/Ni). Figure 3.16 shows the J-V curves of the Te/Cu/Ni back contact device measured periodically during the duration of the OC (a) and SC (b) stress. The initial J-V curves for the stressed devices were essentially identical. Figure 3.16(c) shows a comparison of the pre-stress and post-stress J-V curves after nearly 1000 hours under their respective stress conditions. Over the duration of the stress, the V_{OC} under both conditions degraded by similar amounts (Fig. 3.17). Similar to the Cu/C/Ni contacts in the previous section, the OC-stressed device shows reduced J_{SC} as compared to the SC-stressed device. In regards to the FF, the OC-stressed device shows a much more stable FF over time compared to the SC-stressed device.

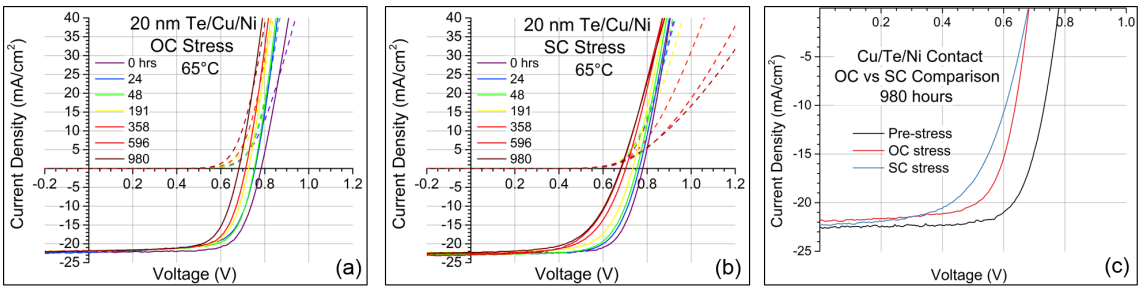

Figure 3.16: Plots of the J-V curves of CdS/CdTe cell with Te/Cu/Ni back contact stressed at 65°C under illumination at (a) open-circuit and (b) short-circuit, along with a pre/post-stress comparison of both stress conditions (c).

The SIMS depth profiles for Cu concentration are shown in Fig. 3.18. The amount of Cu in the bulk of the CdTe is lower for the pre-stress Te/Cu/Ni device than for the Cu/C/Ni device (Fig. 3.15). This suggests that the Te layer acts as a diffusion barrier for Cu. The

SIMS data also shows much less Cu accumulation near the front junction and in the CdS layer, which is likely part of the reason the device performance is better than the OC-stressed Cu/C/Ni contact. The SC-stressed device showed Cu migration out of the bulk, similar to the SC-stressed Cu/C/Ni device.

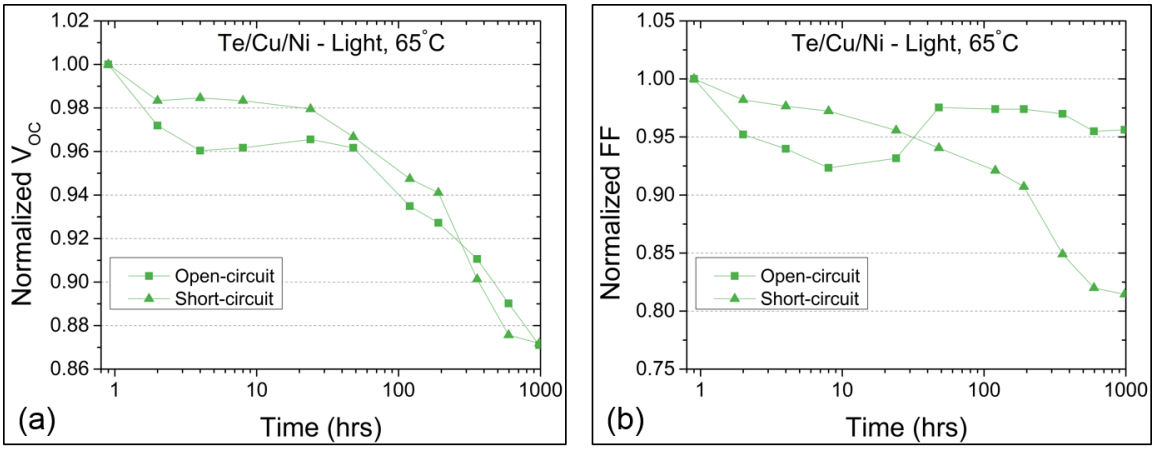

Figure 3.17: Plots of the V_{OC} (a) and FF (b) versus amount of time stressed of a CdS/CdTe cell with Te/Cu/Ni back contact at 65°C under illumination at open-circuit and short-circuit.

The fact that devices with the Te layer in their back contact can produce respectable FF with less Cu treatment coupled with the apparent lack of Cu diffusion towards the front is likely the source of the stable FF in the OC-stressed device. The explanation for the loss in V_{OC} is possibly related to compensation by Cl defects; however, Cl depth profiles were not available for the Te/Cu/Ni contact devices. Perrenound and Gretener have also suggested that Cu_{Cd} can decay and will migrate to the GBs, causing a reduction in doping, which may be an additional source for the loss of V_{OC} [41, 97].

Comparing the two SC-stressed devices with the different contacts, their trends in degradation are relatively similar. This suggests that for SC-stress the back of the device was not the primary source for the changes in performance, but rather the changes were dominated by Cu and Cl migration out of the front junction. Next, long-term stress at a higher temperature (80°C) will be discussed.

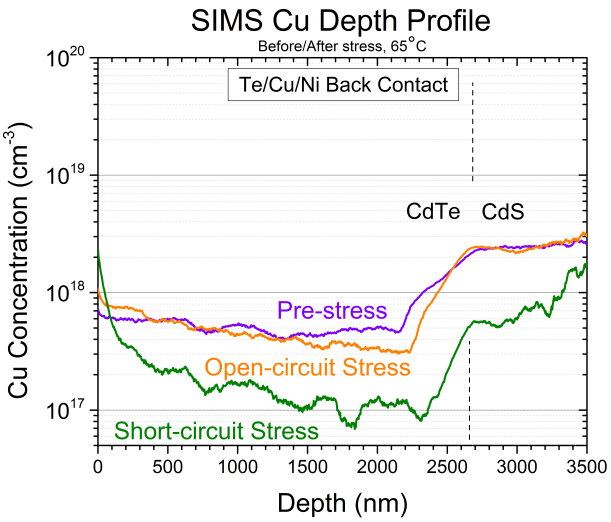

Figure 3.18: SIMS depth profiles of the Cu concentration of a CdS/CdTe cell with Te/Cu/Ni back contact for pre and post-stress at 65°C under illumination at open-circuit and short-circuit.

3.5.2 80°C, Illuminated, OC - Back Contact Comparison

This section explores LTS at a temperature of 80°C under 1 sun illumination at open-circuit. CdS/CdTe devices with three different back contacts (Cu/C/Ni, Te/Cu/C/Ni and Cu/Te/C/Ni) with the standard Cu treatment were compared. The duration of this stress was also ∼1000 hours, but this experiment focused more on the longer-term changes, and therefore the first measurement was not taken until 24 hours after the pre-stress measurement.

All devices were kept in typical storage conditions for 166 days between the initial and pre-stress J-V measurements. Table 3.2 lists the initial, pre-stress, and post-stress J-V parameters for the devices with the three different back contacts. The devices showed mostly regular changes at storage conditions for their respective back contacts as discussed in Sec. 3.3.

The changes in the V_{OC} and FF over the stress duration, normalized the pre-stress values, are shown in Fig. 3.19. For this set of devices, the V_{OC} loss is relatively minimal. However, the FF degradation is accelerated with the increased temperature. Both of the devices with the Te layer show an increase in FF during the first ∼24 hours, especially the devices that

Table 3.2: J-V parameters for CdS/CdTe devices with the Cu/C/Ni, Te/Cu/C/Ni and Cu/Te/C/Ni back contacts for their initial, pre-stress, and post-stress measurements. The devices were storage in the dark and room temperature for 166 days between the initial and pre-stress measurements. The stress condition was 80°C, 1 sun illumination, at OC for ∼1000 hours.

Measurement	Back Contact	V_{OC} [V]	FF [%]	J_{SC} [mA/cm^2]	η [%]
Initial	Cu/C/Ni	805	69.4	22.6	12.6
Pre-stress	Cu/C/Ni	800	65.7	22.1	11.6
Post-stress	Cu/C/Ni	755	37.7	21.8	6.2
Initial	Te/Cu/C/Ni	794	72.3	22.7	13.0
Pre-stress	Te/Cu/C/Ni	796	71.7	22.4	12.8
Post-stress	Te/Cu/C/Ni	761	65.3	22.7	11.3
Initial	Cu/Te/C/Ni	806	73.0	22.9	13.5
Pre-stress	Cu/Te/C/Ni	794	69.0	22.4	12.3
Post-stress	Cu/Te/C/Ni	776	47.0	22.4	8.2

received Cu treatment before Te. The Cu/Te/C/Ni device actually showed almost a 10% increase in FF from the pre-stress and even a 3% increase over the initial measurement. However, after achieving the performance improvement, the Cu/Te/C/Ni device steadily declined over the remainder of the stress duration. The device without Te also showed a steady decline in FF over the stress duration, but without any initial increase. This suggests that both devices likely had similar amounts of Cu in the bulk of the CdTe, which was the primary mechanism for their long-term degradation. The device that was Cu treated after Te showed much less FF degradation as compared to the other back contacts.

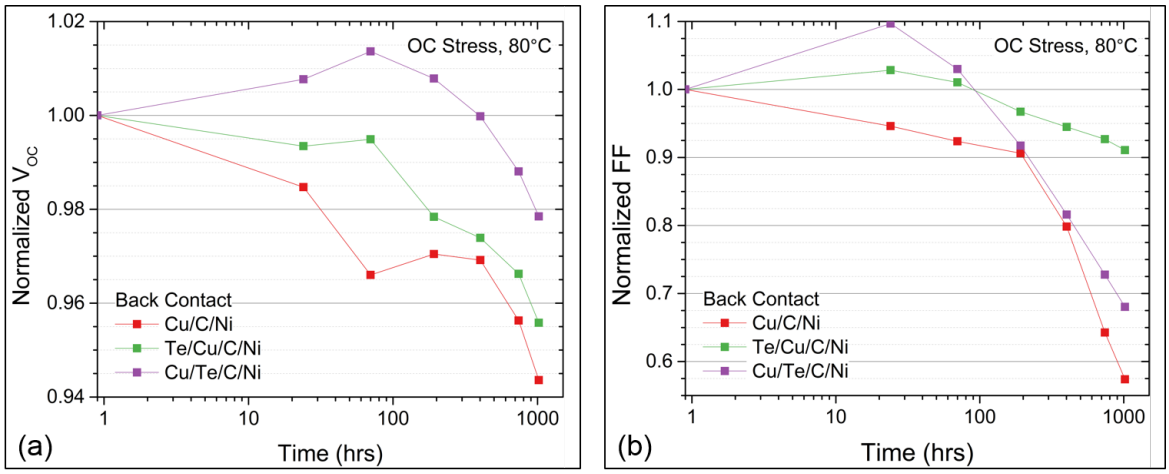

Figure 3.19: Plots of the V_{OC} (a) and FF (b) versus amount of time stressed of CdS/CdTe cells with Cu/C/Ni (red), Te/Cu/C/Ni (green) and Cu/Te/C/Ni (purple) back contacts stressed at 80°C under illumination at open-circuit.

Figure 3.20 shows the J-V curves for the different back contacts over time, which provides context for the changes in the J-V parameters. On striking difference is the appearance of J-V "kink" behavior in the contacts with Te, after ∼1 week of stress. This may be related to the inclusion of C, but the "kink" is much less pronounced in the Cu/C/Ni device without Te. Figure 3.20d shows a comparison of the pre-stress and post-stress J-V curves for each of the contacts. The Cu/Te/C/Ni device shows a very amplified "kink" as compared to the Te/Cu/C/Ni device, which is likely the results of less mobile Cu in the bulk of the Te/Cu/C/Ni device. Pan el al. showed that the "kink" can be formed from the combination of an increased back barrier and low carrier lifetime. The effective back barrier was likely increased due to decreased doping near the back from Cl diffusion. The lifetime likely was decreased from deep states created by Cu in the front.

The QE for Te/Cu/C/Ni and Cu/Te/C/Ni back contacts for pre-stress and post-stress is shown in Fig. 3.21. In the CdS absorption region (below 520 nm), both devices show decreased in QE. As previously mentioned, this may be caused by the creation of deep acceptor states by Cu in the CdS, which can trap holes generated by blue light [94, 82, 95, 96]. Both devices, also show an increase in QE in the longer wavelengths, which is likely due to

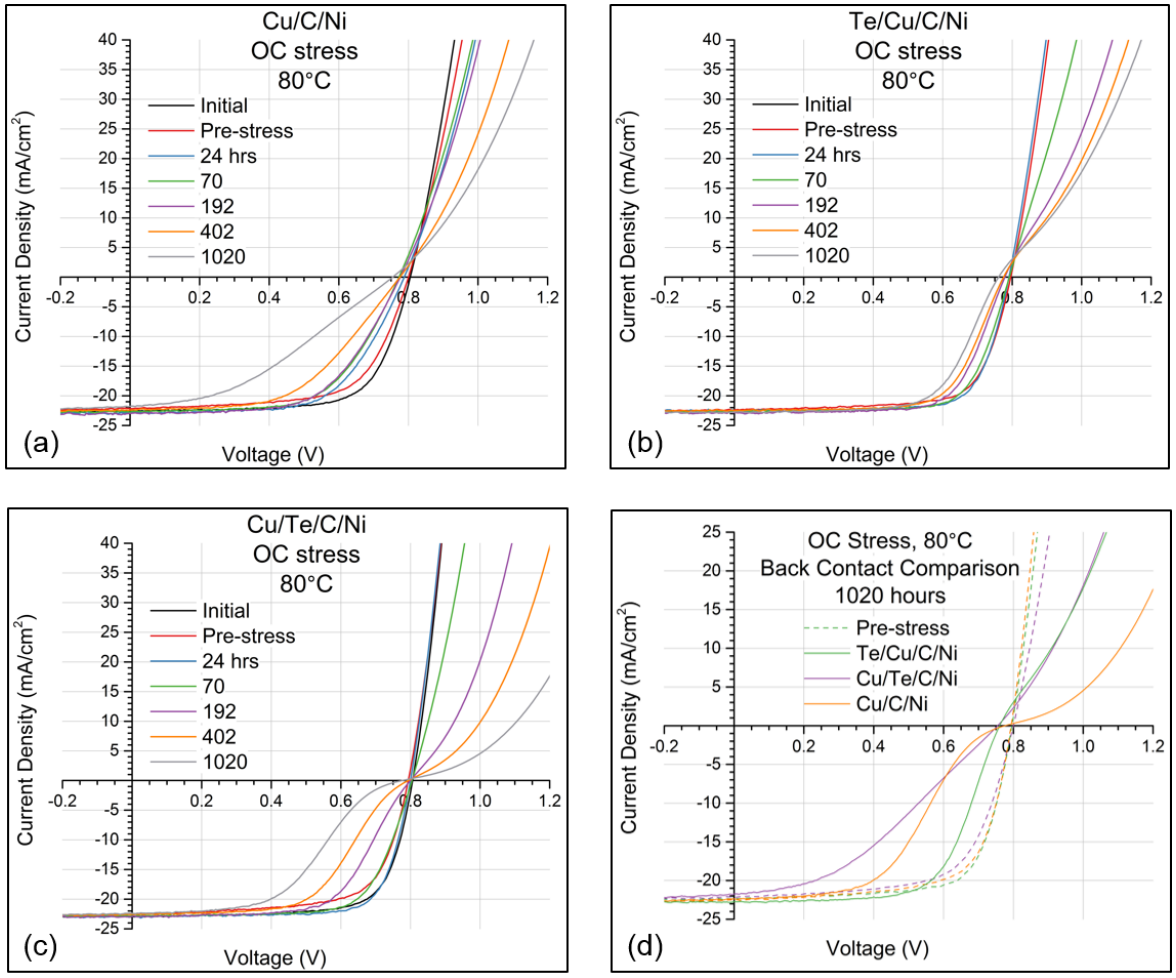

Figure 3.20: J-V curves of CdS/CdTe cells with (a) Cu/C/Ni, (b) Te/Cu/C/Ni and (c) Cu/Te/C/Ni back contacts stressed at 80°C under 1 sun illumination at open-circuit. (d) Pre-stress (dashed curves) and post-stress (solid curves) comparison of the Cu/C/Ni, Te/Cu/C/Ni and Cu/Te/C/Ni back contacts.

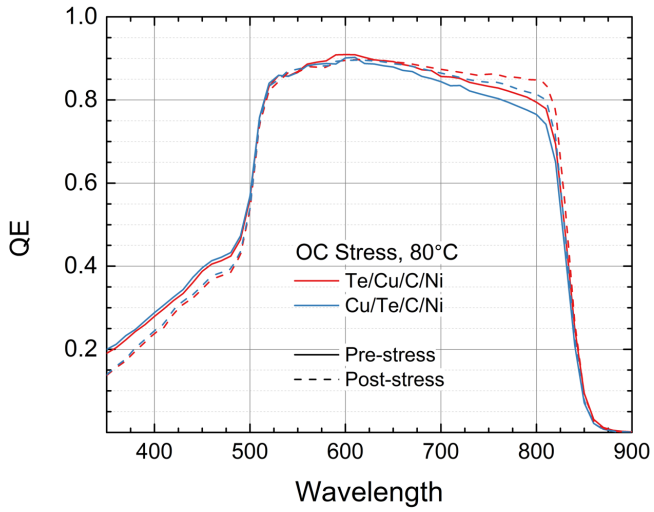

Figure 3.21: QE of CdS/CdTe cells with Te/Cu/C/Ni (red) and Cu/Te/C/Ni (blue) back contacts stressed at 80°C under illumination at open-circuit for pre-stress (solid curve) and post-stress (dashed curve).

the diffusion of recombination-causing defects toward the front of the device. Overall, the Cu/Te/C/Ni shows more recombination than the Te/Cu/C/Ni in the longer wavelengths, which likely relates to its performance issues.

Figure 3.22a shows the $(A/C)^2$ versus the applied voltage for the cells with Te for pre-stress and post-stress. Both devices, show reduced curvature near 0 V bias at the conclusion of the stress, which suggests a more fully depleted absorber post-stress. This is likely the result of lower net doping towards the back of the device, because the bulk doping pre-stress versus post-stress is not largely different. Another notable feature (Fig. 3.22b), is the reduced depletion width, which was also seen for the devices stressed at OC at 65°C. The increase in Cu and decrease in Cl in the junction and CdS areas are likely the causes of this behavior, due to the compensation of defects and creation of midgap states in both the CdTe and CdS. Additionally, increased series resistance in the circuit will show the appearance of a decreased depletion width, which was likely caused by the increased resistivity of the highly-photoconductive CdS layer in the dark. Lastly, the Cu/Te/C/Ni device shows an aburpt change in $(A/C)^2$ for forward biases above $\sim$0.6 V, which typically signifies voltage

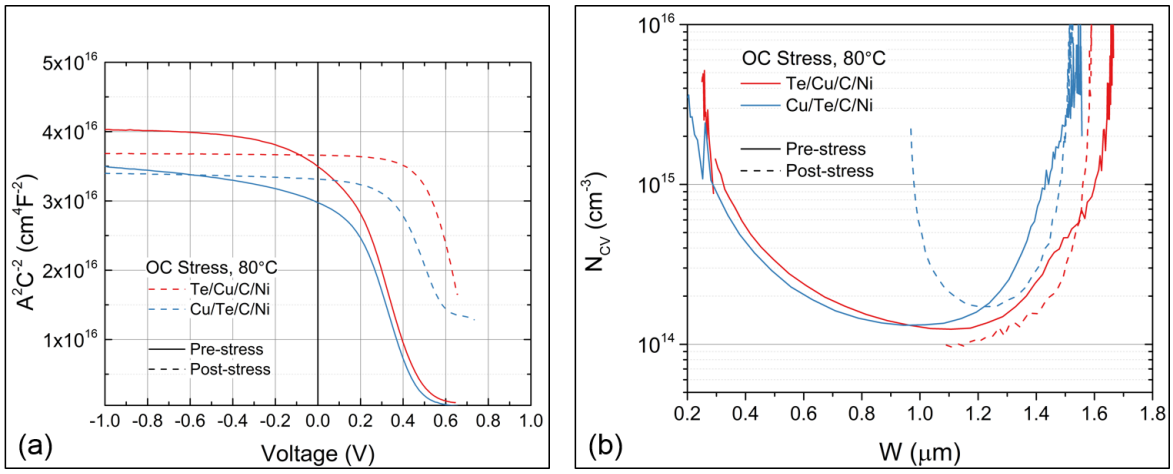

Figure 3.22: Plots of the inverse capacitance squared (a) versus voltage and the carrier density versus the depletion width (b) of CdS/CdTe cells with Te/Cu/C/Ni (red) and Cu/Te/C/Ni (blue) back contacts stressed at 80°C under illumination at open-circuit for pre-stress (solid curve) and post-stress (dashed curve).

sharing with another part of the device. This is also the voltage region where the strong "kink" behavior is present in the J-V data. Both of which are evidence of a barrier in the Cu/Te/C/Ni device (post-stress).

Overall, LTS showed that stress of devices with a small internal field (OC) is only beneficial for short stress durations. For LTS at OC conditions, the device will experience degradation in both V_{OC} and FF, likely caused by the migration of Cu into the front junction and CdS, and Cl towards the back of the device, which are supported by evidence from SIMS. The SC-stressed devices show significant Cu migration out of the front junction and bulk CdTe towards the back of the device. Both the Cu/C/Ni and Te/Cu/Ni back contact devices at SC showed similar degradation in trends in performance, which suggests the changes due to Cu migration overshadow any differences in performance due to the back contact.

In both temperature cases, the devices that received the Te layer before Cu treatment were the most stable. SIMS data suggests this is due to less Cu initially in the bulk (pre-stress) and less Cu diffusion towards the front junction and CdS (post-stress).

3.6 Suggestions for Improving Metastability

The root cause for metastability appears to the migration of Cu and Cl in the device. The base levels of Cu in the CdTe bulk without the Cu treatment are $\sim 1 \times 10^{17}$ cm^{-3}, which should be an adequate amount of Cu to achieve doping at typical levels $\sim 2-3 \times 10^{14}$ cm^{-3}. However, it appears that the additional Cu treatment is needed to shift enough Cu onto Cd lattice sites, albeit at the expense of introducing even more Cu_i. It is possible that if the initial base level of Cu was lower, a similar doping could be achieved, but with less Cu overall.

With the tools available at CSU, the CuCl source is in the same deposition chamber as the CdTe, which very likely causes cross contamination. In order to achieve a lower base level of Cu in the CdTe, the CdTe deposition should ideally be in a Cu-free chamber, which would require the removal of the CuCl source and a thorough cleaning or possibly the replacement of all hardware that may have been exposed to Cu. Granted, this is not a simple task, but it is likely necessary for CdTe device efficiency to be pushed toward the maximum. To further facilitate lower base levels of Cu, higher purity source materials of CdTe and $CdCl_2$ could also be implemented in a Cu-free system.

Furthermore, optimizing the Cl treatment to include the smallest amount of Cl_i would greatly benefit doping achieved by Cu_{Cd}, because the formation of the (Cu_{Cd}-Cl_i) complex is likely the most detrimental defect limiting p-type doping by Cu in CdTe. However, this is likely very difficult to achieve in practice. Since Cl passivation is essential for producing the best-performing CdTe devices, its presence will always have the effect of compensating the Cu doping to some degree. Therefore, it would be wise to investigate options for other p-type impurity dopants in CdTe, such as group V atoms (P, As, or Sb), which have been relatively unexplored until recently. This opens the possibility of increasing both device performance and stability. Results have shown hole densities up to 10^{16} cm^{-3} by incorporating P with Cl treatment but without Cu [98, 99]. However, a device with performance on par with Cu-treated CdTe has yet to be fabricated.

Lastly, evidence from this work shows that applying the Te layer before the Cu treatment results in a more stable device, both in storage and under long term stress, as compared to devices contacted after the Cu treatment. The initial measurement of a Te/Cu/Ni device typically shows lower V_{OC} and FF as compared to the Cu/Te/Ni contact. However, optimization of the Te thickness and Cu treatment for the Te/Cu/Ni device may yield better initial performance along with enhanced stability.

3.7 Summary of Conclusions

It was found that all devices show changes in storage. The majority of the performance change results from a reduction in FF with the most change in devices with the Cu/C/Ni contact, followed by the Cu/Te/Ni contact, and lastly the Te/Cu/Ni contact. It was inferred that defect drift and diffusion were the primary mechanisms causing the changes.

Short-term stress showed that devices with less Cu treatment were more stable under OC-light-stress at 60°C, which was attributed to less mobile Cu present in the device. Additional short-term stress on the low-Cu device at different precondition and stress condition combinations further suggested that the internal field appears to be the dominate mechanism for change. Transitioning from the high internal field to a low internal field shows improvement in the device and the converse shows device degradation. The high internal field is pulling positive Cu_i and Cl_i out of the junction area and thus reducing doping in the bulk due the compensation of Cu_{Cd}. The exposed Cu_{Cd} may improve doping near the from junction but it also decreases lifetime, resulting in lower FF. Additionally, going from dark stress to light stress, a drop in V_{OC} is observed. This is likely due to (de)ionization of midgap states in the CdTe.

Long-term stress showed that biasing devices with a small internal field (OC in the light) is only beneficial for short stress durations. In the long-term, the device will experience degradation in both V_{OC} and FF, caused by the migration of Cu into the front junction and CdS, and Cl towards the back of the device, which are supported atomic depth profiles before and after stress. Cu_{Cd} in CdS is an acceptor and will lower its doping and increase its

resistivity, supported by evidence in J-V, QE, and C-V. It is also possible Cu_{Cd} may decay and migrate to the GBs, thus lowering doping. Regardless of back contact, the SC-stressed devices showed similar changes in performance. The harmful effects due to the Cu migration, both Cu_{Cd} and Cu_i, out of the front junction and bulk CdTe towards the back of the device outweighed any performance differences from the back contact.

In all OC-light-stress, the devices that received the Te layer before Cu treatment were the most stable. Atomic concentration profiles of Cu show that the Te/Cu/Ni contacts have less Cu in the bulk as compared to Cu/Te/Ni contacts that received the same Cu treatment. Additionally, post-stress profiles of the Cu/Te/Ni device do not show any extra Cu in the front junction or CdS. This suggests that Te is likely a diffusion barrier to Cu, and thus less mobile Cu in the bulk of CdTe results in greater stability.

Lastly, should be mentioned that the performance changes observed in these devices was greater than what is typically seen from industry-leading CdTe technology from First Solar, Inc. First Solar has reported only a $\sim$3% power reduction in over similar $\sim$1000-hour stress tests. Their fabrication process is likely much more refined, especially the Cu treatment, and their stability success is also partially attributed to the use of a ZnTe buffer layer in their back contact [100]. Additionally, under real-world conditions, solar cells will transition from a light to dark conditions each day, i.e. small internal field to large internal field. Stress data from this research suggests that this would be beneficial for the performance of the device over these daily time-scales. However, long-term stress incorporating alternating light and dark stress conditions was not performed and would be an obvious next step for future work.

Chapter 4

CONCLUSIONS AND FUTURE WORK

Devices fabricated with the Te buffer layer showed good performance with generally larger FF than the traditional C buffer contact used at CSU, which was especially true if the Cu treatment was reduced. This is postulated to be due to higher lifetime and carrier density from less excess Cu in the bulk, which is supported by evidence from PL, C-V, and SIMS. However, without the Te layer, reduction in Cu treatment does not show performance improvement, indicating that the Te layer is the primary reason for the increased performance. Electron microscopy showed that evaporated Te on the CdTe surface creates a continuous, polycrystalline layer with limited (if any) interdiffusion. This suggests that the bulk Te layer properties, rather than changing the CdTe atomic states by diffusion of Te, was the cause of device performance changes.

From Hall measurements on Te films, the carrier density was found to in the range of 1 to 5×10^{18} cm^{-3}. Using a range of Te valence band maximums found in literature, simulated results of performance were compared to experimental measurements in order to narrow the probable range of the VBM$_{Te}$ to 5.40-5.45 eV. Thus, using these values for the Te carrier density and the VBM$_{Te}$, the simulation suggested that the reduced downward band bending at the back of the CdTe was the primary physical mechanism by which the Te buffer layer aided in forming a good-performance back contact. However, it should be noted that there may be additional mechanisms responsible for the changes in recombination due to the inclusion of the Te layer, as seen in the JVT and PL measurements.

Comparison of the standard Cu treatment on devices before and after the Te layer revealed better initial performance for devices that were first Cu treated before the Te layer. Typically for the Te/Cu/Ni contact devices the V_{OC} was 10-20 mV lower and the FF was reduced $\sim$2% as compared to the Cu/Te/Ni contact devices. SIMS data shows that there is less Cu in the bulk CdTe of the Te/Cu/Ni device as compared to a device that had the

same Cu treatment directly on the CdTe back surface. This suggests that there were different mechanisms present in the Te/Cu/Ni contact device, because a lower-Cu/Te/Ni device results in better FF and V_{OC} that was on par with the standard-Cu/Te/Ni devices.

In regards to the metastability, the Te/Cu/Ni device showed less change in storage and especially under elevated temperature and light stress, typically resulting in better long-term performance as compared to the other contact configurations even though its initial performance was lower. These two results suggest that there is less migration of Cu in the device, but it is also possible that there are additional mechanisms due to applying Cu treatment through the Te layer. From an initial device performance perspective the low-Cu/Te/Ni devices are the clear champions. However, from a reliability point of view, the Te/Cu/Ni is the most stable. Less research has been done on the Te/Cu/Ni configuration, and thus it may be a fruitful avenue for additional exploration.

Future Work

Future work could include an in-depth study of the Te thickness and Cu treatment for the Te/Cu/Ni contact configuration, which might also include variations in the Cu anneal time and temperature. The full suite of measurements discussed in Sec. 1.4 would be useful for characterization along with x-ray diffraction to confirm the phase composition of the Te layer after the various Cu treatments and anneals. Since this contact configuration initially shows superior stability, it is possible that with proper optimization the overall performance could be improved while retaining (or even improving) the reliability.

Since JVT and PL suggest that there are changes in recombination due to the addition of the Te layer. An expanded PL study over a range of low temperatures and various excitation energies on devices with the Te contact versus without would be particularly helpful. These additional studies could reveal additional physical mechanisms of Te the layer based on the energies of the transitions that are increased/decreased by inclusion of the Te layer. Additionally, admittance spectroscopy of devices with Te may help identify the presence of a surface charge that could be present at the CdTe/Te interface.

Long-term stress of the low-Cu/Te/Ni devices would be beneficial for confirming that lower-Cu does improve long-term metastability. Comparing the optimized low-Cu/Te/Ni and Te/Cu/Ni contact devices would give insight to the behavior of Cu-treated CdTe/Te versus just Cu-treated CdTe. Additionally, stress experiments with biases that more closely resemble real-world conditions would also be beneficial.

As mentioned in Sec. 3.6, fabrication of devices with lower baseline Cu should be explored, as well as research on incorporating other p-type dopants. This may open the possibility of fabricating devices with high doping, high lifetime, and less mobile impurity atoms.

Finally, since majority of the research on CdTe solar cells at CSU is transitioning towards only incorporating the MZO emitter rather than the CdS emitter, stability studies focused on MZO/CdTe devices would be an obvious next step.

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