DISSERTATION

DESIGN STRATEGIES FOR HIGH-EFFICIENCY CdTe SOLAR CELLS

Submitted by

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ABSTRACT

DESIGN STRATEGIES FOR HIGH-EFFICIENCY CdTe SOLAR CELLS

With continuous technology advances over the past years, CdTe solar cells have surged to be a leading contributor in thin-film photovoltaic (PV) field. While empirical material and device optimization has led to considerable progress, further device optimization requires accurate device models that are able to provide an in-depth understanding of CdTe device physics. Consequently, this thesis is intended to develop a comprehensive model system for high-efficiency CdTe devices through applying basic design principles of solar cells with numerical modeling and comparing results with experimental CdTe devices.

Four key topics about high-efficiency CdTe cells are covered in this dissertation: (a) material optimization of CdTe absorber, (b) roles of emitter/absorber interface on carrier transport, (c) substrate choices for monocrystalline CdTe cells, and (d) back contact configurations for thin-film polycrystalline CdTe cells. Finally, comparisons between simulation and experiment are carried out to identify both beneficial and detrimental mechanisms for CdTe cell performance and to guide future cell optimization.

The CdTe absorber is central to cell performance. Numerical simulation has shown the feasibility of high energy-conversion efficiency (open-circuit voltage V_{OC} >1000 mV, efficiency $\eta > 25\%$), which requires both high carrier density ($p > 10^{16}\ cm^{-3}$) and long minority carrier lifetime ($\tau_n > 100$ ns). As the minority carrier lifetime increases ($\tau_n > 10$ ns), the carrier recombination at the back surface becomes a limitation for cell performance with absorber thickness $< 3\ \mu m$. Hence, either a thicker absorber or an appropriate back-surface-field layer is a requisite for reducing the back-surface recombination.

When integrating layers into devices, more careful design of interfaces are needed. One consideration is the emitter/absorber interface. It is shown that a positive conduction-band offset ΔE_C ("spike") at the interface is beneficial to cell performance, since it can induce a large valence-band bending which suppresses the hole injection near the interface for the

electron-hole recombination, but too large a spike is detrimental to photocurrent transport. In a heterojunction device with many defects at the emitter/absorber interface (high S_{IF}), a thin and highly-doped emitter can induce strong absorber inversion and hence help maintain good cell performance. Performance losses from acceptor-type interface defects can be significant when interface defect states are located near mid-gap energies. In terms of specific emitter materials, the calculations suggest that the (Mg,Zn)O alloy with $\sim$ 20% Mg, or a similar type-I heterojunction partner with moderate ΔE_C (e.g., Cd(S,O) or (Cd,Mg)Te with appropriate oxygen or magnesium ratios) should yield higher voltages and would therefore be better candidates for the CdTe-cell emitter.

The CdTe/substrate interface is also of great importance, particularly in the growth of epitaxial monocrystalline CdTe cells. Several substrate materials (CdTe, Si, GaAs, and InSb) have been discussed and all have challenges. These have generally been addressed through the addition of intermediate layers between the substrate and CdTe absorber. InSb is an attractive substrate choice for CdTe devices, because it has a close lattice match with CdTe, it has low resistivity, and it is easy to contact. However, the valence-band alignment between InSb and p-type CdTe, which can both impede hole current and enhance forward electron current, is not favorable. Three strategies to address the band-offset problem are investigated by numerical simulation: (a) heavy doping of the back part of the CdTe layer, (b) incorporation of an intermediate CdMgTe or CdZnTe layer, and (c) formation of an InSb tunnel junction. Each of these strategies is predicted to be helpful for higher cell performance, but a combination of them should be most effective.

In addition, the CdTe/back contact interface plays a significant role in carrier transport for conventional polycrystalline thin-film CdTe devices. A significant back-contact barrier ϕ_b caused by metallic contact with low work function can block hole transport and enhance the forward current and thus result in a reduced V_{OC}, particularly with fully-depleted CdTe devices. A buffer contact layer between CdTe absorber and metallic contact is strongly needed to mitigate this detrimental impact. The simulation has shown that a thin tellurium (Te) buffer as well as a highly doped p-type CdTe layer can assume such a role by reducing

the downward valence-band bending caused by large ϕ_b and hence enhancing the extraction of the charge carriers.

Finally, experimental CdTe cells are discussed in parallel with the simulation results to identify limiting mechanisms and give guidance for future efficiency improvement. For the monocrystalline CdTe cells made at NREL, it is found that the sputter damage causing large numbers of defect states near the Cd(S,O)/CdTe interface plays an important role in limiting cell performance, particularly for cells with low oxygen Cd(S,O) (with a "cliff" band offset). Other effects, such as the large series resistance and reflection, also reduce the cell performance. A lattice-matched material with less deposition damage and with a type-I interface is suggested to introduce less interfacial recombination in future emitter growth on epitaxial CdTe absorbers. For polycrystalline CdTe solar cells made at CSU, it is demonstrated that an MZO emitter forms a spike at the MZO/CdTe interface and a Te buffer layer mitigates large back-contact barrier ϕ_b. Both play very important roles in achieving good cell performance ($V_{OC} \sim 860$ mV, $\eta \sim 18.3\%$). The simulation has also shown that the electron reflector would be an effective approach to further increase V_{OC} even with a relative low CdTe carrier concentration ($\sim 10^{14}\ cm^{-3}$).

ACKNOWLEDGMENTS

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Chapter 1

MOTIVATION

My interest in photovoltaics (PV) can be traced back to my junior undergraduate year in 2010. At that time, the air pollution became more and more serious in Beijing (the city where I completed my undergraduate study). I was attracted by PV's low-carbon consumption and sustainability to our environment and believed that it is definitely meaningful to choose solar PV as my upcoming graduate research field. I started with a small research project relevant to spin-coated organic PV (OPV) devices, but then realized that its stability issue and low-performance weakness could restrict its development. Therefore, I decided to switch to a more mature and more promising PV field - thin-film PV, and enrolled for the PhD at Colorado State University (CSU), which has a world-leading CdTe thin-film PV research program.

Now after several years of deep immersion into PV, some rational and critical questions have been emerging in my mind: (1) Is solar PV really an effective solution to reduce the global carbon consumption and reverse the worsening climate situation, such as arising sea level and more frequent extreme weather? (2) Nowadays, is PV viable without subsidies in other than a few places [1]? Can it be more widely adapted worldwide with economical competitiveness over other traditional electricity sources such as natural gas or coal plants? (3) Since PV is an intermittent electricity source, can it be durable to our current electric grid as PV installation continues to increase? A brief overview relevant to these questions is given below.

1.1 Status of Solar Photovoltaics

The increasingly serious environmental problems all over the world have become a core driving force to promote renewable energy. The accelerated global warming and climate

change is one of them, primarily due to the large carbon consumption from the burning of the fossil fuels since the Industrial Revolution. In 2016, the world just passed the symbolic 400 parts per million (PPM) threshold of CO_2 concentration and the average temperature is also set to be the hottest year on record [2]. As a result, the retreat of glaciers continues to raise the sea level and extreme weather like droughts and floods have been reported more frequently. Fresh water scarcity is another big challenge to the humanity as the global population continues to increase. Currently, about 40% of the global population - approximately 2.8 billion people are affected by water scarcity, particularly in the Middle East and North Africa [3]. The people in these regions highly rely on desalinated water. This process is very energy-intensive and has been producing significant amount of carbon emission. Traditional thermoelectric (i.e., gas or coal) power plants with a large water consumption do not seem to be effective power source for water desalination in a long term, particularly with increasing population. Also, lots of cities and countries are struggling with the air pollution due to increased electricity demand from coal plants.

As discussed before, these serious environmental problems are primarily caused by incremental increases in consumption of fossil fuels. Therefore, renewable energy sources with low carbon emission and water consumption are strongly desirable to mitigate these problems. In many peoples' minds, solar PV is a very attractive renewable energy. But one may ask: is it able to provide enough energy for our humanity with limited land? Can it effectively solve the current and the upcoming environmental problems? According to one relevant study [4], PV installation on about 0.6% of the land in the well-developed US could be enough to meet the entire country's electricity need. So the land usage would not be a limitation for PV installation, particularly in the developing countries with less electricity demand per capita. Since the fabrication of PV modules consumes energy, some people have questioned PV's effectiveness on the reduction of carbon emission. But this argument is not valid even for current PV technology. The average energy payback time (i.e., the module power output time needed to compensate the energy consumed for module production) of PV modules is ~ 1 years and decreasing with technology advances, but PV industry has widely guaranteed

a 25-year product lifetime (i.e., producing 80% of its power over 25 years). In addition, PV has much lower water consumption footprint in the energy generation process especially compared to other traditional thermoelectric power plants [3]. Thus, it would be a suitable source to solve the water scarcity crisis. Overall, more and more countries including US and China - the world's two largest carbon emission countries, are encouraging the development of solar PV energy through government incentives. With over a decade of high-speed PV growth, the accumulated installation of PV modules has reached over 230 GW globally in 2015 while the solar installation cost continues decreasing, see Fig. 1.1 [5, 6].

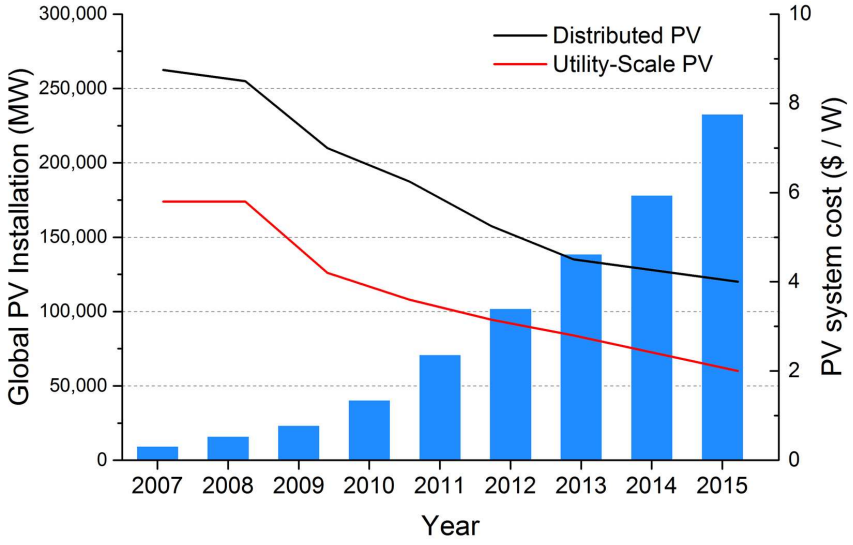

Figure 1.1: Accumulated global PV installations and average PV system costs in recent years. Data reproduced from [5, 6]

However, it must be admitted that the stimulation of government incentives and subsidies has been playing an important role in the PV market. To maintain a long-term and sustainable growth, and to have a more influential impact on climate change, the solar industry needs to rely less on the subsidies and develop economically competitive PV electricity. Many countries such as Spain, Italy, Germany, UK, and Japan, have encountered or are encountering a boom-bust cycle (i.e., with government subsidies, PV installation grows very fast in the first few years; but the installation sharply decreases once governments reduce or cut down the subsidies) due to a strong dependence of the subsidies [1]. To break the strong

dependence of subsidies, which is not sustainable in the long term, the cost of PV energy needs to be further reduced. One way is to keep scaling up the global PV capacity, which can reduce the levelized installation for PV systems. There appears competitive PV tenders in some countries and regions with abundant sunshine, such as India and Brazil with an average power-purchase agreement below \$0.08/kWh at the end of 2015 (The average electricity price for traditional generation sources globally is ∼\$0.10/kWh [1], [7]). With continuous scaling up of PV installation, cheap PV electricity should be feasible in more regions.

The advancement of PV technology can also contribute to reduce the PV system cost. That is to enable more efficient and durable PV products. For instance, First Solar, the world largest thin-film CdTe PV manufacturer, has reduced the CdTe module manufacturing cost from \$1.02/W in 2010 to \$0.51/W in 2015 [8] with its large investment on R&D. Within only 5 years, Its cell and module efficiencies have been boosted from 16.5% to 22.1% and from 14.4% to 18.2% respectively[9]. The cost of PV systems can be further reduced by improving the reliability and decreasing the degradation rate of PV modules. The US National Renewable Energy Laboratory (NREL) has pointed out that extending the PV system lifetime from a more standard expectation of 30 years to 50 years over long term yields less PV system cost [8].

Another challenge about PV is the intermittency. PV electricity is produced during daytime. The electricity demand at night must be offset by other stable power output such as electricity storage or traditional power plants. Otherwise, it would put the electricity grid in danger. Recent study shows that reaching 25% of electricity from PV without major changes to the grid and 50% with storage and other grid improvements is feasible [10, 11]. Currently, the electricity generated by PV plants consists of only about 1% global electricity demand. Therefore, it is viable for solar PV to become one of the major components in the global energy portfolio.

Overall, by taking its environment-friendly advantage, solar PV can play an important role in mitigating or even reversing the worsening climate change. With more efforts being

made on technology improvements, it will possess more growth potential both economically and environmentally.

1.2 Status of CdTe PV

Since the thesis has a focus on CdTe solar cells, this section will give a brief summary of the current status and historic development of CdTe PV, and its advantages and disadvantages compared to the traditional Si PV technology (broadly including monocrystalline and polycrystalline Si). The research of CdTe-based PV devices began in the early 1960s, studied with a variety of device structures including homojunctions, heterojunctions, and Schottky barrier cells, and with efficiencies around 10% at that time [12] [13]. By the middle of the 1990s, the cell efficiency increased to 15% for CdS/CdTe heterojunction configuration [14]. Recently, the cell efficiency has broken the 20% threshold by enhancing optical absorption and electrical properties [9], [15]. As a result, the CdTe-based PV technology has become a mainstream PV technology in part due to a wealth of research advances. Today, First Solar has installed over 13.5 GW CdTe modules worldwide and continues to grow with $\sim$3 GW of annual pipeline production [16].

Though the conventional Si PV technology occupies most of the PV market share, CdTe technology still possesses compelling advantages compared to Si and has the potential to increase the installation capacity. (1) The most obvious advantage of CdTe over Si is a much lower material consumption due to its direct bandgap and thus high absorption coefficient. The typical CdTe absorber layers are usually 1-4 μm thick, while the crystalline Si wafers are over 100 μm thick. As a result, CdTe has a shorter energy payback time than Si cells ($\sim$2 years for silicon, but $<$ 1 year for CdTe thin films) [17]. (2) CdTe has less strict material purity requirement (i.e., 100 times less than Si) and simpler manufacturing process than Si (i.e., the full process time: $<$ 3.5 hours for CdTe but $\sim$ 3 days for Si) [9]. (3) Since CdTe has a superior temperature coefficient, better spectral response, and better shading response, CdTe PV devices yield up to 12% higher energy density than Si in abundant sunshine region [9].

Because of these advantages, the current cost of CdTe module manufacturing is estimated to be \$0.51/W, cheaper than Si with \$0.66-0.74/W [8].

However fairly speaking, we must mention that CdTe PV also exists some disadvantages in current stage. For instance, with respect to increasing large-scale CdTe manufacturing, the perceptions of the Cadmium (Cd) toxicity may become challenging issues for CdTe PV community [18]. The toxicity issue about Cd appears to be one of the public concerns. While scientific research has concluded that the toxicity of Cd is minimal once incorporated into PV modules, governmental policy in individual countries may dictate whether such toxicity concern impacts the development of CdTe solar cells.

1.3 Purpose of This Work

Despite the advantages of CdTe above, further improvement on cell performance is crucial in order to promote the market share of CdTe PV. A recent NREL study has shown that by increasing the current average CdTe module efficiency from 16% to 22%, its manufacturing cost can decrease from \$0.51/W to \$0.34/W, the lowest over other PV technologies [8].

In the past, the performance improvements of CdTe devices could be generally divided into three categories from the perspective of device structure: (1) the optimization of window and buffer emitter layers to reduce the front optical losses and avoid detrimental shunts, (2) the material quality enhancement of CdTe absorber to mitigate the bulk carrier recombination, and (3) the application of novel contact materials to form ohmic contact. Progress has been driven in large part by empirical material optimization, however, efforts to understand the mechanisms causing cell performance losses have been limited. In particular, the design of high-efficiency CdTe cells ($\eta > 25\%$) is directly correlated to an in-depth understanding of CdTe device physics. Therefore, this thesis is intended to develop a systematic device model for high-efficiency CdTe solar cells. By applying basic design principles of solar cells with numerical simulation, both beneficial and detrimental mechanisms for CdTe cell performance are identified to guide future device optimization.

In the following sections of the thesis, Chapter 2 reviews the solar cell basics with a focus on CdTe technology. Chapter 3 summarizes several fundamental design principles of CdTe solar cells from the perspective of carrier dynamics in the junction and also have a short introduction on the design approach - numerical simulation. By applying the design principles discussed in previous chapter, Chapter 4 addresses crucial challenges limiting cell performance and correspondingly proposes specific strategies to solve these limitations with numerical simulations. In Chapter 5, several CdTe solar cells fabricated both in our lab at Colorado State University and by our collaborators (NREL and First Solar) are discussed in parallel with simulated results in order to verify the developed model system and shed light on continuous device optimization. Chapter 6 includes a summary of this dissertation and future work.

Chapter 2

BACKGROUND

In this chapter, the basic device-physics concepts and background for solar cells are reviewed for a better understanding of the following work. It also summarizes two representative device configurations of current CdTe solar cells and compares their process differences and device properties.

2.1 Solar Cell Basics

2.1.1 Fundamental concepts of semiconductors

Semiconductor materials act as the fundamental bricks to build solar cell devices. It is thus helpful to review some basic concepts of semiconductors. Semiconductors are crystalline or amorphous solids with a moderate energy gap (E_g) in which allowed energy states do not exist. The upper bands are called the conduction bands; the lower bands, the valence bands. The conduction band minimum is designated E_C, and the valence band maximum E_V, as shown in Fig. 2.1a.

At $T > 0$ K, a fraction of the energy states at both E_C and E_V are filled with electrons (labeled "n") and holes (labeled "p"), respectively. The occupation of the energy states at E_C and E_V are governed by the Fermi-Dirac distribution [19]:

$$F(E) = \frac{1}{1 + \exp(\frac{E - E_F}{kT})} \tag{2.1}$$

where k is the Bolzmann constant, T the absolute temperature, and E_F the Fermi level. E_F is a hypothetical energy level and represents that if there is a state at E_F, this state will have a 50% chance of being occupied.

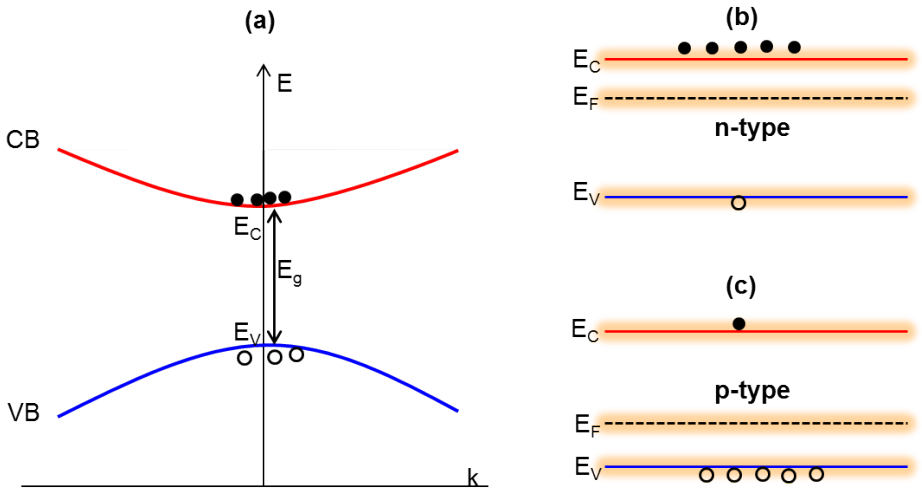

Figure 2.1: (a) Energy band structure of a direct bandgap semiconductor. CB: conduction band; VB: valence band.(b) n-type semiconductor where electrons are the majority carriers. (c) p-type semiconductor where holes are the majority carriers. solid circles represent electrons, and open circles holes.

An intrinsic semiconductor is very pure and contains negligible impurities. Its number of charge carriers (electron and hole) are equal, that is $n = p$. The carrier concentrations can be modified by introducing extrinsic dopants and the intrinsic defect levels. Depending on whether electrons or holes are the majority carriers, the doped semiconductors are classified as either n-type or p-type, as shown in Fig. 2.1b and c. The carrier concentration is given by the total number of states $N_{C,V}(E)$ multiplied by the occupancy of the energy states $F(E)$, integrated over the appropriate band:

$$n, p = \int_{E_{C,V}}^{\infty} N_{C,V}(E)F(E)dE \tag{2.2}$$

At equilibrium, the carrier concentrations of nondegenerate semiconductors can be written as:

$$n = N_C \exp(-\frac{E_C - E_F}{kT}) \tag{2.3}$$

and

$$p = N_V \exp(-\frac{E_F - E_V}{kT}) \tag{2.4}$$

where

$$N_C = 2(\frac{2\pi m_e^* kT}{h^2})^{3/2}, \tag{2.5}$$

and

$$N_V = 2(\frac{2\pi m_h^* kT}{h^2})^{3/2}, \tag{2.6}$$

$m_e^*$and m_h^* are the effective masses of electrons and holes, and h the Planck's constant. The product of the majority and minority carrier concentrations follows the mass-action law:

$$pn = N_C N_V \exp(-\frac{E_g}{kT}) = n_i^2 \tag{2.7}$$

Under non-equilibrium conditions, such as photoexcitation with illumination and carrier injection due to external electric bias, the carrier concentrations are varied and each carrier has its own quasi-Fermi level (E_{Fn} for electrons, E_{Fp} for holes). Now, the carrier concentrations are still determined by Eq. 2.5 and 2.6 but with replacing E_F with E_{Fn} or E_{Fp}, and the mass-action law no longer holds. More detailed descriptions can be found in textbooks such as [12] and [19].

2.1.2 Carrier dynamics in a p-n junction

In practice, nearly all solar cells are configured with a p-n junction, which assists the separation of photo-generated carriers (electron-hole pairs) and extracts the electric power. Therefore, it is of great importance to have a solid understanding on the carrier dynamics in a p-n junction.

A p-n junction is formed by joining n-type and p-type semiconductor materials, where the excess electrons from n-type material diffuse to the p-type side and the excess holes from the p-type material diffuse into the n-side. At equilibrium with the depletion of the free carriers near the junction interface, the left-behind charged states form an electric field (positive charges at n-side and negative charges at p-side, shown in Fig. 2.2(a-b) preventing the diffusion current and such depleted layer is called the space charge region (SCR). The remaining region is called quasi-neutral region (QNR) where negligible electric field exists.

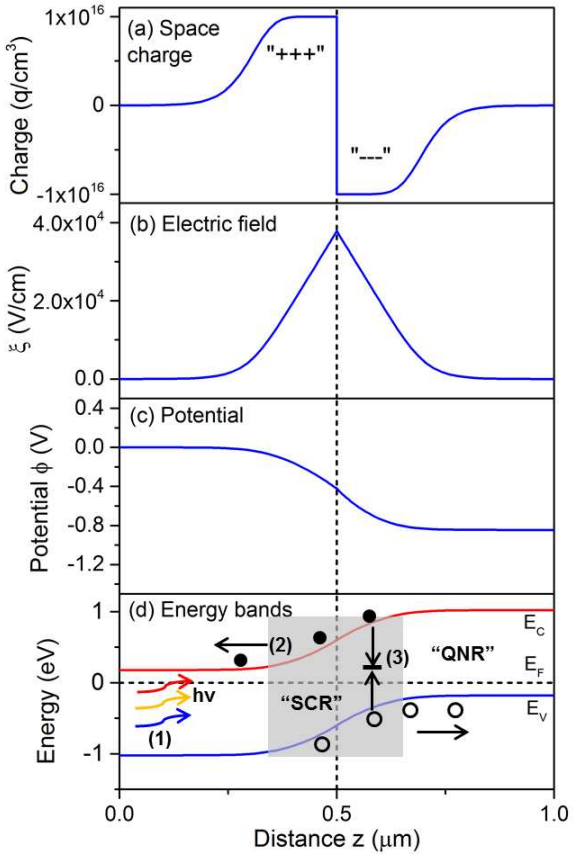

Figure 2.2: A p-n junction at equilibrium. (a) Space charge distribution; (b) Electric field distribution; (c) Potential distribution; (d) Energy band diagram.

Fig. 2.2c-d show the electrostatic potential and the energy band diagram of the p-n junction. When light is incident into a solar cell, the carrier dynamics inside the junction can be described in three main processes as shown in Fig 2.2d: (1) the charge carrier generation due to light absorption, (2) the carrier transport primarily driven by drift and diffusion, and (3) the carrier recombination (will be discussed later).

Three sets of equations govern these processes of the carrier dynamics: the Poisson equation, the continuity equations for electrons and holes, and the current-density equations [12, 19]:

$$\nabla \cdot (-\varepsilon)\nabla\varphi = q(p - n + N_d^+ - N_a^-) \tag{2.8}$$

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q}\nabla \cdot J_n \tag{2.9}$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q}\nabla \cdot J_p \tag{2.10}$$

$$J_n = \mu_n n \nabla E_{Fn} \tag{2.11}$$

$$J_p = \mu_p p \nabla E_{Fp} \tag{2.12}$$

where ε is the dielectric constant, φ is the electrostatic potential, n and p are the free carrier concentrations, N_D^+ and N_A^- are the density of ionized donor and acceptor levels, J_n and J_p are the electron and hole current density, and μ_n and μ_p are the electron and hole mobilities. $R_{n,p}$ is the recombination rate, and $G_{n,p}$ is the generation rate. Note that the generation and recombination of electrons and holes take place simultaneously and we can write $G = G_n = G_p$ and $R = R_n = R_p$. In this work, only steady state solutions are investigated ($\partial n, p/\partial t = 0$) and hence Eq. 2.9 and 2.10 become:

$$\nabla \cdot J_n = -q(G - R) \tag{2.13}$$

$$\nabla \cdot J_p = q(G - R) \tag{2.14}$$

Since these are coupled non-linear differential equations with three variables (φ, E_{Fn}, and E_{Fp}), numerical methods with appropriate boundary conditions at the interfaces and contacts are needed to solve them. Before going into details on numerical simulations (Section 3.3), a brief overview of the physical mechanisms of carrier dynamics is given in the following section.

Carrier Generation

When incident light reaches a solar cell, photons with energy greater than that of the band gap can generate electron-hole pairs inside the solar cell, as shown in Fig 2.2(d). Ideally, all the incident photons are absorbed in the absorber. In practice, however, part of the light can be reflected at the front surface (R labeled as the front reflection) and the light needs to go through several layers before entering the absorber, all of which can lead to optical losses. The photon flux density Φ ($\#\ of\ photons/cm^2 \cdot s$) with a single-wavelength (λ)

decays exponentially with the depth z,

$$\Phi(z,\lambda) = \Phi(z_0) \cdot (1-R) \cdot \exp[-\alpha_X(\lambda) \cdot (z - z_0)] \tag{2.15}$$

where $\Phi(z_0)$ the photon flux density at the depth of z_0, and $\alpha_X(\lambda)$ is the absorption coefficient for Layer X.

Hence, the generation rate is given as [20]:

$$G(z,\lambda) = -\frac{d\Phi}{dz} = \Phi(z_0) \cdot (1-R) \cdot \alpha_X \cdot \exp[\alpha_X(\lambda) \cdot (z - z_0)] \tag{2.16}$$

Equation 2.16 describes photo-excited carrier generation rate due to monochromatic light source. In practice, a spectrum of light shines into PV devices and the simulation in this work assumes a standard one-sun spectrum (also referred to AM 1.5G [21]). The total generation profile is the sum of the single-wavelength generations. For a typical CdTe solar cell, assume a 0.2-μm-thick ITO window layer and 0.1-μm-thick CdS buffer emitter layer before the CdTe absorber (detailed CdTe device introduction will be given in Section 2.2).

Fig. 2.3 shows the calculated total generation profile with the standard one-sun spectrum against the CdTe thickness. Part of the short-λ photons are absorbed in the ITO and emitter region, causing the optical absorption losses. The majority of the electron-hole pairs are generated in the first micrometer of CdTe absorber. These charge carriers can be extracted by the built-in electric field and then be collected at opposite contacts which contribute to the photo current J_{ph}. Note that not all the photo-excited carriers in the absorber contribute to J_{ph} since recombination in the absorber and interfaces can lead to collection loss. These losses can be numerically quantified through a straightforward analysis of quantum efficiency (QE) and optical measurements. Detailed calculations of the J_{ph} loss of CdTe solar cells can be found in Geisthardt's dissertation[22].

Overall, after charge carriers are generated by photons, they need to transport to the contact terminals for electricity conversion while encountering recombination process. The following sections describe how the carriers transport and recombine.

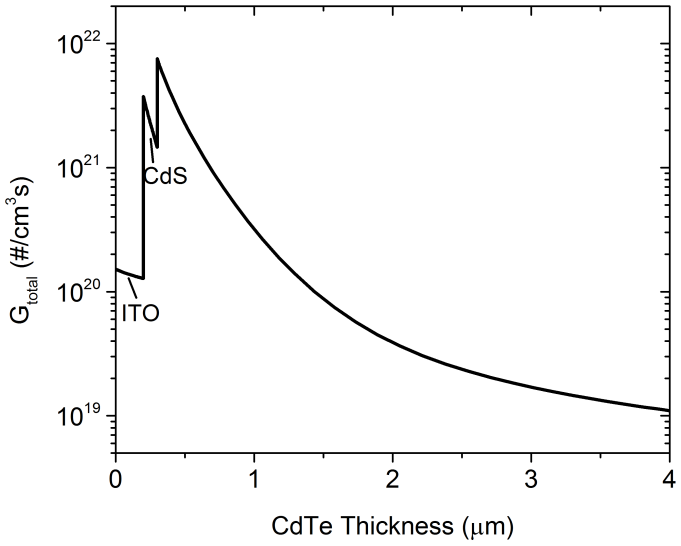

Figure 2.3: The electron-hole generation rates vs. the depth of a CdTe solar cell with 1-sun spectrum.

Carrier Transport

In a p-n junction, the main carrier transport mechanism is the drift-diffusion process. Eq. 2.11 and 2.12 can be expanded as [19]:

$$J_n = \mu_n n \nabla E_{Fn} = q\mu_n n\xi + qD_n \nabla n \tag{2.17}$$

$$J_p = \mu_p p \nabla E_{Fp} = q\mu_p p\xi - qD_p \nabla p \tag{2.18}$$

where the first term at the right represents the the drift current driven by electric field ξ, and the second term the diffusion current determined by the gradient of the carrier density and relevant to the diffusion coefficient $D_{n,p}$.

At thermal equilibrium, the net diode current ($J = J_n + J_p$) is zero. At voltage bias and/or under illumination, extra carriers can be injected with bias or excited by photons and cause a net current flow across the junction. The mechanism of the carrier transport varies inside the junction. Within the space charge region (SCR, see Fig 2.2) where the electric field forms, there are present both the highest electric field strengths and the density

gradient. Therefore, the net current flow is the sum of both the drift and diffusion currents. In the quasi-neutral region (QNR) where the electric field is negligible, the net current flow is dominated by diffusion. The diffusion length, which is the average length a carrier moves between generation and recombination, can be given as

$$L_D = \sqrt{D\tau} \tag{2.19}$$

where $D = \mu \cdot (kT/q)$ is the diffusion constant, and τ the carrier lifetime (both have electron and hole values and will be discussed later).

When there exists a band offset at heterojunction interface, thermionic emission and tunneling will play roles in current flow. In terms of current direction, the photocurrent J_{ph} flows from n to p side since photo-generated electrons moving from p to n side and photo-generated holes from n to p side; under forward bias, since electrons are injected from n-type emitter into p-type CdTe absorber, the direction of forward diode current J_d is opposite to that of J_{ph}. With convention, therefore, the diode current J_d is positive under forward bias and the photocurrent J_{ph} is negative.

Carrier Recombination

Ideally, one expects that all the photo-generated carriers can pass across the junction and be collected by the electron and hole contacts respectively before their loss by recombination. However, under non-equilibrium conditions, the recombination process is unavoidable since the excited electrons in the conduction band find them energetically favorable to return their equilibrium states.

In a bulk semiconductor material, there exist three types of recombination processes (see Fig. 2.4) [19]: (1) the radiative process with the energy dissipated by emission of photons; (2) the non-radiative Auger recombination by transferring the energy to another free electron or hole; and (3) the non-radiative defect related recombination with the energy dissipated by the emission of phonons. The Auger recombination is negligible in CdTe material [23], and hence only radiative and defect-related recombination is included in this work.

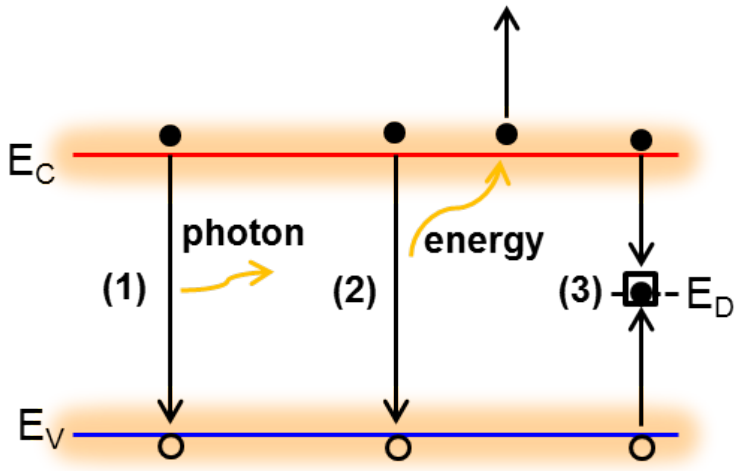

Figure 2.4: Recombination processes in a bulk semiconductor material. E_D represents the defect energy state.

If one assumes a p-type CdTe material, the radiative recombination rate R_{rad} is given by [12]

$$R_{rad} = B \cdot N_A \cdot \Delta n \tag{2.20}$$

and the corresponding radiative lifetime τ_{rad} is

$$\tau_{rad} = \frac{\Delta n}{R_{rad}} = \frac{1}{B \cdot N_A} \tag{2.21}$$

where B is the radiative recombination coefficient ($B = 1 \times 10^{-10}\ cm^3 \cdot s^{-1}$ for CdTe [24]), N_A the doping concentration, Δn the excess minority carrier concentration. Currently, the doping range of p-type CdTe is between $10^{14}\ cm^{-3}$ and $10^{16}\ cm^{-3}$ and thus the corresponding radiative lifetime τ_{rad} is 100 μs - 1 μs.

The defect-related recombination in CdTe often refers to the Schockey-Read-Hall (SRH) recombination and can be derived [19]:

$$R_{SRH} = \frac{np - n_i^2}{\tau_p(n + n^*) + \tau_n(p + p^*)} \tag{2.22}$$

where

$$\tau_n = \frac{1}{\sigma_n N_d \upsilon_{th}} \tag{2.23}$$

$$\tau_p = \frac{1}{\sigma_p N_d \upsilon_{th}} \tag{2.24}$$

$$n^* = n_i \exp[(E_d - E_i)/kT] \tag{2.25}$$

$$p^* = n_i \exp[-(E_d - E_i)/kT] \tag{2.26}$$

The quantities τ_n and τ_p are the electron and hole lifetimes, where σ_n and σ_p are the capture cross sections and υ_{th} is the thermal velocity, n^* and p^* related to the emission rates from the defect state N_d. In the quasi-neutral region where $p \gg n, n^*, p^*$, the SRH recombination rate R_{SRH} becomes

$$R_{SRH} = \frac{\Delta n}{\tau_n} \tag{2.27}$$

By combining Eq. 2.20 and Eq. 2.26, the bulk lifetime for CdTe can be expressed as

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{n,SRH}} = B \cdot N_A + \frac{1}{\tau_{n,SRH}} \tag{2.28}$$

when $\tau_{rad} \gg \tau_{SRH}$, the bulk recombination is dominated by the SRH recombination. This usually takes place in polycrystalline (poly) CdTe material with $\tau_{SRH} < 100\ ns$ ($\ll \tau_{rad}$). For high-quality CdTe material such as large-grain poly or monocrystalline CdTe, Eq. 2.27 still holds. In this work, both recombination mechanisms are taken into account.

Apart from the bulk recombination, the extrinsic defects are likely to be present at or very close to the interfaces between layers of a full CdTe solar cell stack, and these defects can act as recombination centers for electron-hole pairs. Similar to the defect-related bulk recombination, the interfacial recombination rate R_{IF} can be described by

$$R_{IF} = \frac{n_{IF} p_{IF} - n_i^2}{S_p^{-1}(n_{IF} + n^*) + S_n^{-1}(p_{IF} + p^*)} \tag{2.29}$$

but with units of $cm^{-2} \cdot s^{-1}$, where n_{IF} and p_{IF} are the electron and hole concentrations at the interface, which are determined by the band offsets and band bending (they in turn determine the carrier availability for recombination). $S_n = N_{d,IF}\sigma_n\upsilon_{th}$ and $S_p = N_{d,IF}\sigma_p\upsilon_{th}$, are the interfacial recombination velocities for electrons and holes in units of cm/s. Here, $N_{d,IF}$ has the unit of $\# \cdot cm^{-2}$ to represent the area density of the defect states at the interface. Electron and hole capture cross-sections $\sigma_{n,p}$ of $10^{-12}\ cm^2$ were chosen to represent

the attractively charged non-radiative recombination centers for both electrons and holes (smaller $\sigma_{n,p}$ with neutral cross-section will have less impact on interfacial recombination) and hence $S_{IF} = S_n = S_p$. Detailed discussion on how the interfacial recombination affects the cell performance will be given in Section 4.2.

2.1.3 Diode Characteristic

Diode Current

The diode current J_d of the p-n junction is a sum of the electron and hole currents, which are determined by the carrier generation and recombination and boundary conditions as well,

$$J_d = J_n(z) + J_p(z) \tag{2.30}$$

where $J_n(z)$ and $J_p(z)$ are given by Eq. 2.17 and 2.18. Fig. 2.5 shows the energy band diagram and carrier profiles across the heterojunction of a typical CdTe solar cell in the dark and 0.6-V bias. With forward bias, the minority electrons are injected into the p-CdTe absorber, particularly in the quasi-neutral region (QNR, see Fig. 2.5b). Consequently, the electron current J_n dominates the diode current in the QNR. Note that J_n and J_p are dependent on z since the mechanism of the carrier transport varies inside the junction, but J_d is independent of z, as shown in Fig. 2.5c.

In the dark, the solar cell is a pure p-n diode. The general mathematical form of the diode current J_d as a function of voltage bias is [23, 25]:

$$J_d(V) = J_0\big[\exp\big(\frac{qV}{AkT}\big) - 1\big] \tag{2.31}$$

where

$$J_0 = J_{00}\exp\big(\frac{E_a}{AkT}\big) \tag{2.32}$$

J_0 is the saturation current density which is determined by the activation energy E_a. J_{00} is the reference current density for the saturation current density. The two recombination terms, E_a and diode quality factor A, can be used to reflect the recombination region. For

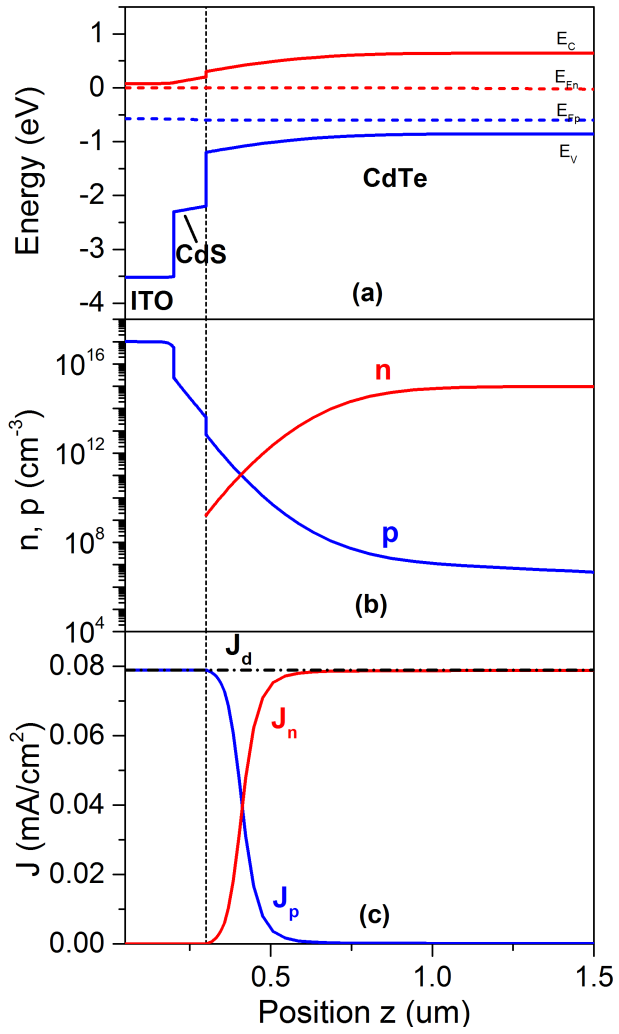

Figure 2.5: Profiles of a heterojunction CdTe solar cell at 0.6-V bias and dark: (a) energy band diagram, (b) electron and hole densities, and (c) current components.

instance, when E_a is close to E_g, bulk recombination (both SCR and QNR) dominates; when $E_a < E_g$, interfacial recombination becomes the dominant factor. For $A = 1$, recombination in the QNR of the absorber dominates; for $A \sim 2$, recombination in the SCR usually prevails. Generally, these recombination paths are actively in parallel and can be adjusted with band alignment and electrical bias. Further discussion will be given in Chapter 4 and 5.

Under illumination, the total current can be written as a sum of the diode and photo currents:

$$J(V) = J_d(V) + J_{ph}(V) \tag{2.33}$$

For good-performance cells, the superposition principle holds, that is, $J(V) = J_d(V) + J_{SC}$. In this case, the photo current J_{ph} is independent of voltage and equal to the short-circuit current J_{SC} at 0-V bias, and the diode current varies little from dark to illumination condition. There may exist non-ideal cases, such as voltage-dependent carrier collection with inferior lifetimes and large energy barriers at the interfaces between layers, where the diode current under illumination is different with that at dark and the photo current may be voltage dependent [26, 27, 28, 29]. In these cases, the superposition principle does not hold.

Light J-V Characteristics

The characteristic current density vs. voltage (J-V) curve under illumination is the most common tool for solar-cell performance evaluation. The basic cell parameters - the open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), fill-factor (FF), and cell efficiency (η), can be obtained from the J-V curves.

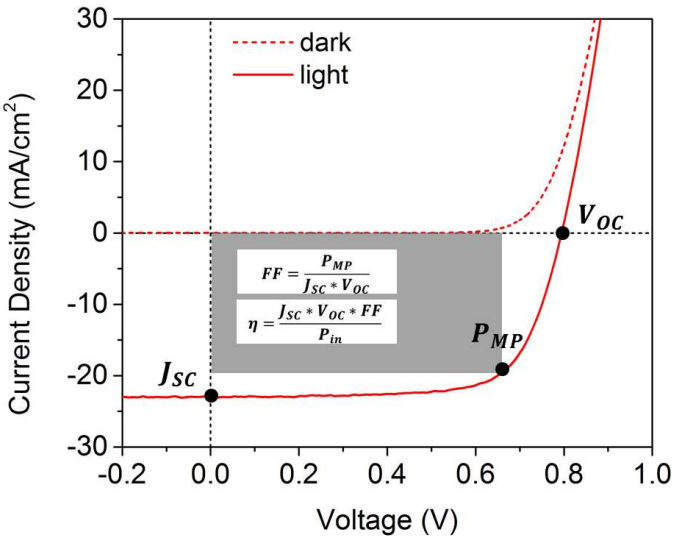

Figure 2.6: J-V curves of a typical CdTe solar cell

Fig. 2.6 shows the dark and light J-V curves of a typical CdTe thin-film solar cell made at CSU. The dark J-V shows the diode behavior with voltage bias. Usually, the superposition principle can be applied to the light J-V, which is a shift-down of dark J-V by the photo-generated current J_{ph}. Thus, J_{SC}, the current density at zero bias, is often assumed to be

the same as the J_{ph}. When a cell encounters a voltage-dependent photo current, $J_L(V)$, for instance, if the carrier diffusion length is very small (usually indicative of a very short carrier lifetime), then the charge carrier collection is strongly dependent on the applied voltage since the SCR varies with voltage bias. Other mechanisms, such as large interfacial recombination and high conduction-band energy barrier, can also reduce J_L in forward bias. Detailed discussion will be given in Chapter 4.

V_{OC}, the voltage at which the current is zero, corresponds to the maximum voltage available from a solar cell. V_{OC} will depend on the absorber E_g. At open-circuit, an ideal solar cell would radiate a photon for every photon that was absorbed in solar cell. In other words, all the generated electron-hole pairs must recombine within the cell (here all of the recombination is radiative). This is the so-called detailed-balance limit [30, 31]. Any additional non-radiative recombination, such as SRH recombination, or photon loss, would lead to V_{OC} loss. For CdTe solar cells where non-radiative recombination dominates in most cases, the diode current increases with the carrier recombination. As a result, the cell has a smaller turn-on voltage and thus a decreased V_{OC}. Specific recombination processes and their effects on cell performance will be discussed in Chapter 3 and 4.

The maximum-power point P_{MP}, the point at which the output power density is maximized, is represented by the dark gray rectangle in Fig. 2.6. FF can be defined by the ratio of P_{MP} to the product of J_{SC} and V_{OC} and is a measure of the shape of the J-V curve behaves. The final parameter is the energy conversion efficiency η, the most commonly used parameter to compare the performance among cells. It is defined as the ratio of the maximum energy output P_{MP} to the incident energy P_{in} from sunlight. In this thesis, these cell parameters will be used frequently to estimate the design strategies.

2.2 Typical CdTe Device Structures

Today, CdTe solar cells are commonly designed with a heterojunction structure. They can be divided into two categories with respect to the degree of CdTe crystallinity: the

conventional polycrystalline (poly) CdTe thin-film solar cells and the potentially higher-efficiency monocrystalline (or single crystal) CdTe solar cells. Commercial applications have generally utilized poly thin-film CdTe solar cells with the main junction grown on a glass, metal- and polymer-foil substrates. In order to explore the S-Q efficiency limit with better-quality CdTe films, however, a few research groups in recent years have been studying the monocrystalline (mono) CdTe solar cells. In this case, the cell junction is formed either with the treatment of mono CdTe wafer [32] or by epitaxial growth of the junction layers on one of several mono substrate materials [33], [34], [35].

To date, the record-efficiency ($\eta = 22.1\%$) [9] CdTe devices has been made with polycrystalline material while the highest open-circuit voltage ($V_{OC} > 1$ V) [35] has been achieved with epitaxial monocrystalline material. Note that except for the grain boundary issue, there should be no fundamental difference between these two materials. Therefore, the two device categories should share very similar design principles. Due to the absence of the defects associated with grain boundaries, mono CdTe has better material quality, which can reflect to smaller amount of SRH recombination defects and thus longer bulk lifetime. The following gives a brief description of the two device configurations, and a straightforward comparison including the primary differences of the device properties, device process and deposition techniques, is summarized in Table 2.1. Detailed design strategies for these cells will be given in Chapter 3 and 4.

2.2.1 Polycrystalline CdTe Thin-Film Solar cells

All the high-efficiency poly-CdTe thin-film solar cells to date have been made with superstrate configuration. In this structure, the transparent conductive oxide (TCO) window and emitter layers are first deposited onto a suitably transparent substrate material such as glass, and then the CdTe absorber and back contact are deposited. The light enters through the absorber from the glass side. The alternative substrate configuration in which the main junction is deposited on opaque substrate such as a metal foil, has been studied but have not

yet attained high efficiency primarily due to lower junction quality and difficulty in forming good back contact during cell processing [13].

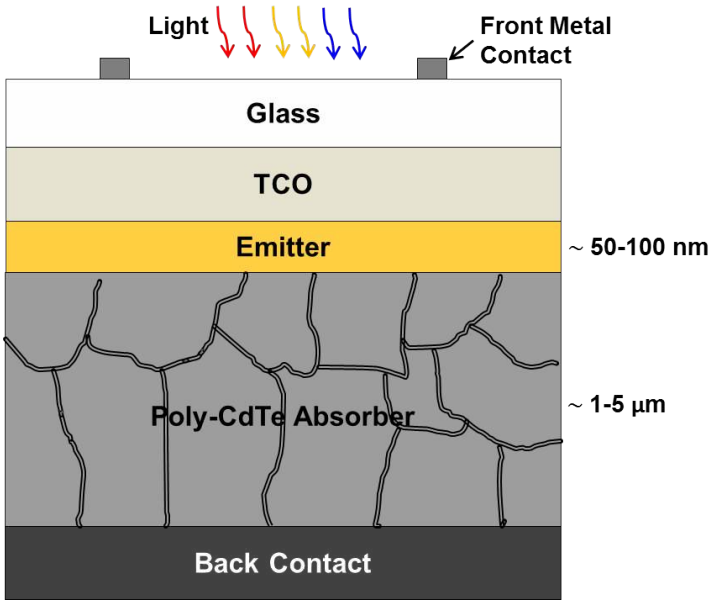

Figure 2.7: Schematic of a typical poly-CdTe thin-film CdTe solar cells with superstrate configuration (not to scale).

Fig. 2.7 depicts the device structure of a typical polycrystalline CdTe thin-film solar cell with the superstrate configuration. It starts with a transparent-conductive-oxide (TCO) coated glass, serving as the front contact to collect the lateral current. There are several commonly used TCO, SnO_2:F, In_2O_3:Sn (ITO), and ZnO:Al (AZO). Most of the incident photons are not absorbed in the TCO layer. Then, an n-type emitter layer such as CdS and (Mg,Zn)O is deposited with a variety of methods such as chemical bath deposition, sputter deposition, and close-space sublimation (CSS). The highly-doped emitter adjacent with the p-type CdTe absorber forms a strong electric field to assist charge carrier collection. Like the emitter, the CdTe absorber can be deposited with a number of techniques, but currently the two most successful methods appear to be CSS and vapor-transport deposition (VTD). The poly-CdTe absorber layers have been lightly p-type doped and limited to $\sim 10^{14} cm^{-3}$ with typical thickness of 1 - 6 μm. Criteria on how to choose appropriate emitter and absorber layers are given in Section 3.2. The typical $CdCl_2$ treatment necessary to making

high-efficiency poly-CdTe devices, is thought to be beneficial in a variety of ways, such as promoting recrystallization and passivating the grain boundaries [13]. In order to achieve a low-resistance ohmic contact, the back-contact (BC) layer typically consists of a buffer layer adjacent to CdTe to mitigate the hole barrier, and a metallic contact layer for lateral current collection.

2.2.2 Monocrystalline CdTe Solar Cells

Though the commercialized thin-film poly-CdTe solar cells have reached 22.1% efficiency, the recent advances were primarily achieved by increasing photocurrent. To further improve the cell efficiency, an increase in V_{OC} is needed since the photocurrent collection for CdTe absorbers has now exceeded 95% of its theoretical limit [15, 36, 37]. However, compared to the V_{OC} of high-quality GaAs (> 1000 mV) with a similar band gap near 1.45 eV, the V_{OC} of polycrystalline (poly) CdTe (in the 850 mV range) has lagged by a considerable amount because of its low carrier concentration, high bulk defect density, and recombination at grain boundaries [15, 38, 39]. Mono-CdTe with greater potential for high carrier concentration, low defect density, and long lifetime can illuminate a path to overcome the V_{OC} limitation, which recently has been demonstrated with V_{OC} over 1000 mV [32, 35].

Fig. 2.8 depicts the device structure of a typical monocrystalline CdTe solar cell. To date, all the high-V_{OC} mono-CdTe devices have been fabricated with substrate configuration though there are differences in the types of layers used. The mono-CdTe solar cells with $V_{OC} \sim 1$ V from NREL [32] were made with p-type mono-CdTe wafers by implementing phosphorous dopant, followed by a thin nanocrystal CdS emitters, bilayer TCO films (i-ZnO + ZnO:Al) at front and a Cu/Mo back contact (BC) at back. The mono-CdTe solar cells with $V_{OC} \sim 1.1$ V from Arizona State [35] were grown on InSb substrate with molecular beam epitaxy (MBE) tool. The mono-CdTe absorbers are n-type with doping $\sim 10^{16} cm^{-3}$ and thickness of 1.4 μm. Before depositing the ITO front contact, a very thin emitter consisting of wider-E_g intrinsic CdMgTe (∼10 nm) and p^+ a-Si:H layers (∼10 nm) was deposited to help collect the photo-generated holes and confine the recombination of photo-generated electrons

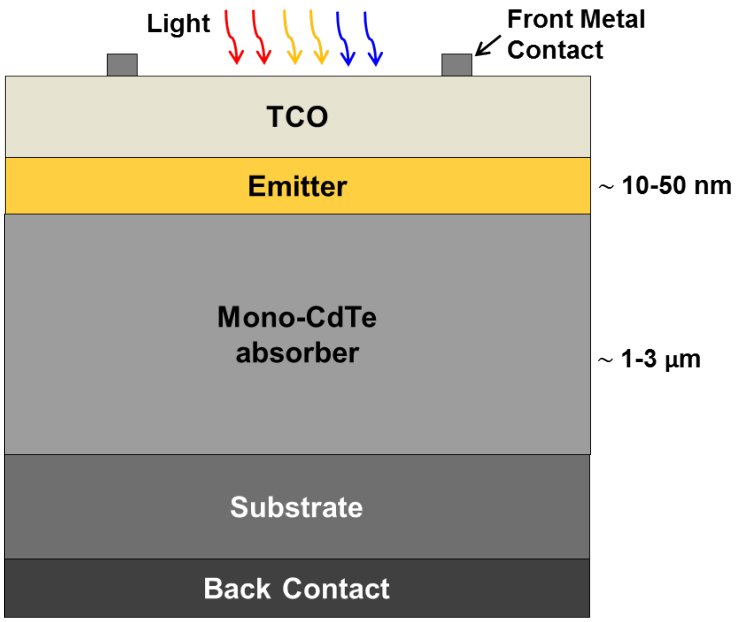

Figure 2.8: Schematic of a typical mono-CdTe thin-film CdTe solar cells with substrate configuration (not to scale).

at front surface. In addition, another wider-E_g n-type CdMgTe layer was deposited between the InSb substrate and n-CdTe absorber to reduce the back surface recombination. A 100-nm-thick layer of silver was sputtered as the back contact. Besides the InSb substrate, other materials such as CdTe, Si, and GaAs [33, 34, 35], have been investigated as substrate candidates but have not yet attained as high V_{OC} as NREL and ASU's devices (A detailed study on the choice of substrate for monocrystalline CdTe cells is given in Section 4.3).

Below is a table comparison on the two CdTe technologies discussed above: poly-CdTe thin-film and mono-CdTe solar cells including representative differences in device properties, device process and deposition techniques.

Table 2.1: Comparison of poly-CdTe thin-film and mono-CdTe solar cells [13, 32, 33, 34, 35, 40]

	Poly-CdTe	Mono-CdTe
Material Properties	1. p: $\sim 10^{14}\ cm^{-3}$	1. both n & p: $\sim 10^{16}\ cm^{-3}$
	2. τ_{bulk}: $\sim$ 1-10 ns	2. τ_{bulk}: $>$ 100 ns
Device Configuration	mostly superstrate	substrate
(substrate material)	(glass, metal foil)	(CdTe, InSb, Si, GaAs)
CdTe Deposition	CSS, VTD, Sputter, et al.	MBE or mono-CdTe wafer
techniques	(low-cost, commercialized)	(very expensive)
Other Layers		
TCO	FTO, ITO, AZO, et al	ITO, AZO
Emitter	CdS, Cd(S,O), (Mg,Zn)O	CdS, CdMgTe, a-SiC_y:H
BC -Buffer	Te, CdMgTe, MoO_x, Cu_xTe, CdTe:Cu, ZnTe:Cu	NP-etched CdTe, CdMgTe
BC -Metal	Ni, Ag, Au, Mo, et al	Ni, Ag, Cu/Mo, Cu/Au, et al.

Chapter 3

DESIGN PRINCIPLES OF CDTE SOLAR CELLS

In order to obtain high-efficiency CdTe solar cells, their optical and electrical losses need to be minimized. These losses depend on both the material qualities of the functional layers and the recombinations in the full device stack. First, the roles of the functional layers and the recombination paths in the CdTe devices are reviewed. Then, some basic design principles of CdTe solar cells are summarized from the perspective of carrier dynamics along the junction, including the impact of each layer's material properties, the energy band alignment associated with carrier transport and recombination. These principles lay out a framework of the comprehensive model system for high-performance CdTe solar cells in the following chapters. This chapter ends with a brief review of the numerical simulation and the simulation packages used in this dissertation.

3.1 Overview

3.1.1 Functionalities of Individual Layers

For typical CdTe cells, a variety of layers with different material choices and process techniques are compared in Section 2.2. Based on the functionalities in PV devices (see Fig. 2.7 and Fig. 2.8), these layers can be classified into four categories: front contact, emitter, absorber, back contact, and substrate (or superstrate).

Table 3.1 summarizes the primary roles, and the preferred features of these functional layers. The front contact is employed to provide the electrical contact of the solar cell to the outside circuit. Ideally, it must possess good conductivity to the main junction. Additionally, it must have little to no impact on the incident photon absorption and charge carrier collection (e.g., an ohmic contact is preferred so as not to impede the carrier transport). The role of emitter is to provide built-in field for extraction of charge carriers and to prevent

Table 3.1: Primary roles and preferred features of layers in a typical CdTe solar cell

Layers	Functionality	Preferred features
Front contact	electrical contact	1. excellent conductivity and ohmic contact
		2. least impact on incident photons
Emitter	charge extraction	1. suppress front surface recombination
		2. large-E_g to minimize J_{ph} loss
		3. low resistivity
Absorber	photon absorption	1. strong photon absorption
	& charge extraction	2. large carrier mobility
		3. low carrier recombination
		4. relatively high doping for charge extraction
Back contact	electrical contact	1. excellent conductivity
		2. ohmic contact assisting carrier transport
Substrate	mechanical stability	1. suitable for the growth of functional layers
		2. thermally stable during deposition

front surface recombination. Thus, it should have high carrier density (i.e., leading to low resistivity and strong electric field) and appropriate band alignment with absorber to reduce front surface recombination. An emitter with larger-E_g is preferred to achieve minimum optical absorption loss. Since most photons are absorbed in the absorber, it is fundamental to the energy conversion process. A good absorber must have strong absorption coefficient, large carrier mobility, and low carrier recombination. A relatively high doping inside the absorber is also needed to achieve a large built-in field and thus an effective charge extraction. Similar to the front contact, a good back contact must have good conductivity and form ohmic contact with the CdTe absorber assisting carrier transport. The final layer is the substrate material, providing mechanical stability. It must be thermally stable for deposition

and suitable for the growth of other functional layers. Here starting with a simple model structure, fundamental rules for CdTe device design will be given in Section 3.2.

3.1.2 Recombination Paths in Solar Cells

In addition to the functionality of the layers, it is helpful to summarize the electron-hole recombination taking place inside the devices. In reality, the recombination processes are not only detrimental to the photocurrent collection, but also determine the diode recombination current and thus affect the cell's V_{OC} and FF [23]. In Section 2.1.2, specific recombination mechanisms inside the CdTe bulk material have been discussed. When the CdTe layer is integrated into a full device stack with emitter and contacts layers, additional interfaces (e.g.., emitter/absorber interface, absorber/back contact surface) and functional regions such as the space-charge region (SCR) are introduced, which can impact the recombination of charge carriers as well.

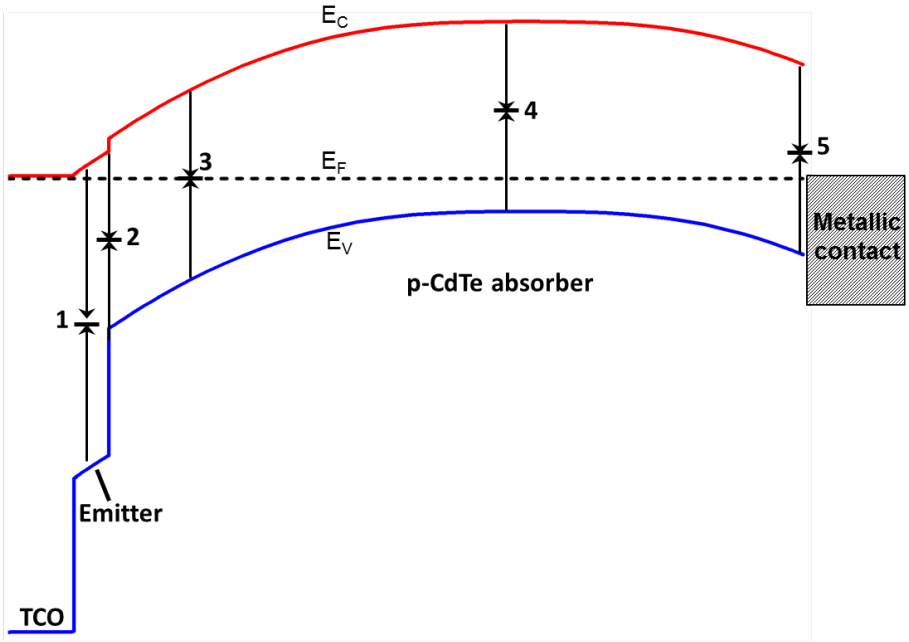

Figure 3.1: Energy band diagram of a typical CdTe solar cell at equilibrium with primary recombination paths labeled.

Fig. 3.1 shows the energy band diagram of a typical CdTe solar cell with a description of specific recombination paths taking place inside the device stack. Recombination path (1) in the emitter layer can reduce the photocurrent and even lead to voltage loss if a large density of defect states exists while the number of photo-generated carriers becomes distinct (e.g., due to thick and/or unoptimized-E_g emitter materials). The recombination path in the CdTe absorber can be divided into two categories: (3) in the SCR and (4) in the Quasi-Neutral Region (QNR) according to the electric field distribution. Usually, both recombination paths are active in parallel. For a short carrier lifetime (with diffusion length less than the depletion width), path (3) in the SCR will dominate, while for a long carrier lifetime, the carriers can be injected into QNR and thus path (4) dominates the recombination in the bulk. More details can be found in [23]. Path (2) and (5) take place at the interfaces. When there exists a large number of extrinsic interfacial defect states, they act as recombination centers deteriorating the charge carrier collection. Principles on how to suppress these recombination paths will be discussed in Section 3.2.

Note that the recombination paths discussed above are defect-related recombination (either bulk defects or surface defects). The radiative recombination is generally not a significant process for CdTe cell performance since most measured τ_{bulk} of CdTe films are well below 1 μs but the value of τ_{rad} is in the range of μs (see Section 2.1.2). In this work, the radiative recombination is included only for $\tau_{bulk} > 100$ ns.

3.2 Key Design Principles

Theoretically, the maximum energy-conversion efficiency of a single-junction CdTe ($E_g \sim 1.5$ eV) solar cell is approximately 33% under AM 1.5G solar spectrum [37]. In reality, the efficiencies of CdTe cells are downgraded by the optical losses and electrical recombination inside the devices. In order to reduce the performance loss as much as possible and shed light on device optimization, it is of great importance to lay out key design principles relevant to the material properties of individual layers and the full device stack. Later, a comprehensive

study on how to design a high-efficiency CdTe cell with adapting these principles will be given in Chapter 4.

3.2.1 Material Properties of Individual Layers

After electron-hole pairs are generated by light, they must be extracted from the absorber and be collected at the opposite contacts to generate electricity while minimizing the photo-generated carrier loss in the emitter. To obtain a sufficient carrier collection, a built-in asymmetry is required to sweep the charge carriers with electric field. In addition, a long diffusion length and smaller amount of recombination centers are desired. Crucial material parameters (i.e., carrier densities n and p, bulk lifetime τ_{bulk}, and layer thickness) of these layers relevant to the carrier collection are briefly discussed below. The impact of the parameters for each layer must be integrated into the overall device operation.

Front and Back Contacts

The primary role of the front and back contacts is to provide the solar cell with the electrical contact to an external load. An ideal front/back contact layer should form an ohmic contact and have a negligible junction resistance relative to the total resistance of the device. Otherwise, it could lead to performance loss due to the blockage of charge carrier extraction and thus a voltage drop in the contact region. Note that the front and back contacts can also impact the photon collection (i.e., a large optical reflection at the front can lead to photocurrent loss, and a lack of back surface reflector can cause insufficient radiative photon reabsorption if the radiative recombination dominates). Note that the relevant optical modeling such as photon trapping and recycling is not included here, and the emphasis is on the electronic model.

For a p-type CdTe solar cell, the front contact has little impact on the cell performance apart from series resistance, which is usually designed to be low. Between the metal front contact and the emitter layer, a highly-doped n-type TCO window layer (e.g., ITO or FTO), is utilized to provide excellent electrical conductivity for lateral current transport and to act

as a "window" to allow the maximum of photons to pass into the absorber. Note that such window layer is heavily-doped, which induces little voltage drop and hence has little impact on the cell performance unless it has an unfavorable band alignment with the emitter layer and/or there exists non-uniformity issue causing local shunts. Relevant modeling studies can be found in [23, 40, 41].

However, since CdTe has an electron affinity (χ) of 4.3 eV and an energy gap of 1.5 eV, it is challenging to find an appropriate back metal contact for p-type CdTe absorber with a sufficiently large work function ($\phi_M = \chi + E_g = 5.8$ eV) to form an ohmic contact. Section 3.2.2 will describe this issue from the perspective of energy-band alignment and Section 4.3 will give detailed discussion and alternative solutions.

Emitter Layer

For CdTe solar cells, the emitter layer in contact with the absorber establishes the electric field and the interface properties and thus is of great importance for charge carrier collection and extraction. For instance, the CdS emitter with a bandgap $E_g \sim$ 2.4 eV will allow absorption loss of short-wavelength photons. In order to minimize the absorption loss, a relatively thin and less-defective buffer emitter is preferable. Additionally, its doping density plays a significant role in the carrier extraction. Generally, a highly-doped emitter ($n \gg p$) is desired to generate a one-sided junction and thus effectively sweep the photo-generated carriers through the emitter. Otherwise, insufficient band bending can enhance carrier recombination at the emitter/absorber interface, especially when there are a large number of interfacial defects. Detailed discussion will be given in Section 4.2.

Absorber Layer

The CdTe absorber is essential for the energy conversion. In principle, all the photons are absorbed in this layer, and the photo-generated carriers are extracted with the built-in field and converted to electric power. Practically, the transport of the charge carriers can be affected by the absorber's material properties, such as, carrier density, bulk lifetime,

and thickness. For instance, a relatively highly-doped absorber is needed to form an effective charge extraction; if there exist a large number of defects states inside the absorber, it causes an inferior bulk carrier lifetime which is detrimental to the carrier transport. A detailed study on the CdTe absorber material optimization is given in Section 4.1.

Substrate Materials

The primary role of the substrate materials is to mechanically support the primary solar-cell junction. Glass is the mostly common-used substrate material for polycrystalline CdTe thin-film solar cells since it has a low cost and can endure the high deposition temperature during the deposition process. Additionally, the substrate assumes an important role in growing high-quality epitaxial mono CdTe devices. A suitable substrate for epitaxy must have good lattice match with CdTe, as well as good electrical properties. Detailed study on the choices of substrate materials for epi-grown CdTe cells is given in Section 4.3.

3.2.2 Energy Band Alignment

As discussed above, the material properties of individual layers have a significant impact on the carrier transport and recombination in CdTe solar cells. When integrating these layers for a full device stack, the corresponding energy-band diagram can determine the carrier dynamics of a solar cell as well, particularly if a large density of interfacial defects is present between layers (see recombination path (2) and (5) in Fig. 3.1). Here, two primary interfacial recombination regions are discussed with the respect of their band alignments: the emitter/absorber interface and the absorber/back contact interface.

Emitter/Absorber Band Alignment

The interface between the emitter and the CdTe absorber is a very critical factor for cell performance, due to both lattice mismatch and other defects created during fabrication of either poly- or sx-CdTe cells. Interfacial defects can act as recombination centers for electron-hole pairs and can be reached by electrons and holes from either the emitter or

the absorber. With such induced interfacial recombination, a solar cell may have reduced photocurrent, but more importantly, a significantly increased diode current and a consequent reduction in V_{OC}, especially as the bulk material properties continue to improve.

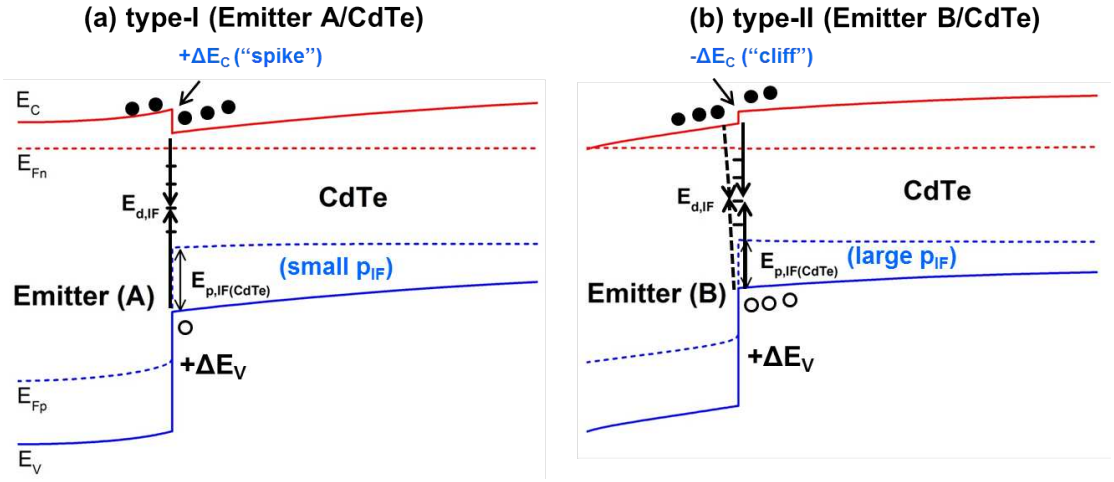

Figure 3.2: Band diagrams of two types of CdTe heterojunction with interface defects at 0.8-V bias under illumination, same ΔE_V in both cases.

Fig. 3.2 shows two types of CdTe heterojunctions with defect states at the emitter/absorber interface: one with a positive conduction-band offset ΔE_C (often referred to as a "spike"), and the other with negative ΔE_C (or "cliff"). Both cases are shown for a forward bias of 0.8 V, which would be in the vicinity of the V_{OC}. Note that the number of electrons near the interface is much greater than the number of holes. In other words, it is the availability of holes determines the interfacial recombination, which is governed by the valence-band bending near the interface. The amount of band bending is clearly different in the two cases.

With the spike, the low point of the conduction band in the CdTe is closer to the quasi-Fermi level for electrons E_{Fn}, which requires greater band bending in the CdTe and hence a larger barrier for holes approaching the interface. A cliff induces less band bending and thus allows larger density of holes on the CdTe absorber side than a spike. This larger hole density may enhance both the cross-interfacial recombination (labeled with dashed arrows in Fig. 3.2(b)), where electrons from the emitter recombine with holes from the absorber, and the recombination where electrons and holes on absorber side recombine (solid arrows).

As a result, the enhanced recombination leads to an increased diode current, which can diminish V_{OC} (detailed explanation in Section 2.1.3). The interfacial recombination rate is proportional to the density of effective recombination centers, which is dependent on the density and energetic locations of the defect states and on the interface charge types affecting the band bending. Detailed analysis is presented in Section 4.2.

Absorber/Back Contact Band Alignment

The interface at the CdTe absorber and back contact is also a significant factor for cell performance, since it can form an unfavorable band alignment to enhance back surface recombination and even impede the photo-generated carrier collection with large contact barrier. Fig. 3.3 shows the energy band diagrams with three values of back metal work

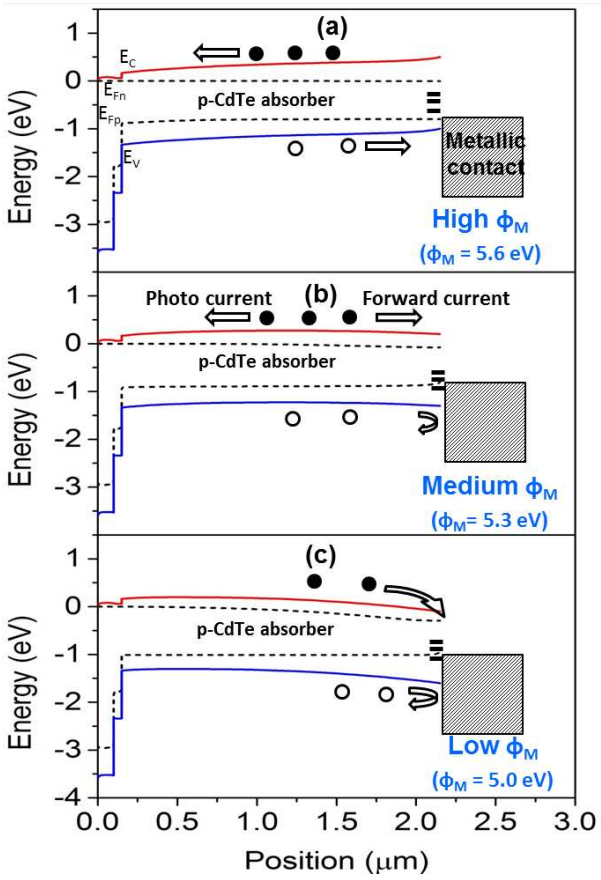

Figure 3.3: Band diagrams of CdTe solar cells with three values of back metal work function ϕ_M again at 0.8-V bias under illumination.

function ϕ_M at 0.8-V bias and under illumination. Ideally, an ohmic contact is required to achieve a smooth carrier transport, as shown in Fig. 3.3(a). However, it is nearly impossible to find such an appropriate metal with a large ϕ_M (> 5.5 eV) to form an ohmic contact with CdTe absorber. The situations such as Fig. 3.3(b) and (c) are more common. In those cases, a portion of the photo-generated electrons can diffuse to the back and recombine with holes at the back surface. The amount of the diffused electrons at the back depends on a variety of material parameters, such as, the carrier mobility and lifetime (determining the diffusion length), the absorber thickness, and the built-in electric field. Detailed analysis can be found in Chapter 4, but qualitatively, Fig. 3.3c shows that the large downward E_V band bending due to low ϕ_M forms a hole barrier, which will impede the photo-generated hole transport. As a result, the forward diode current is enhanced and thus the cell performance is reduced.

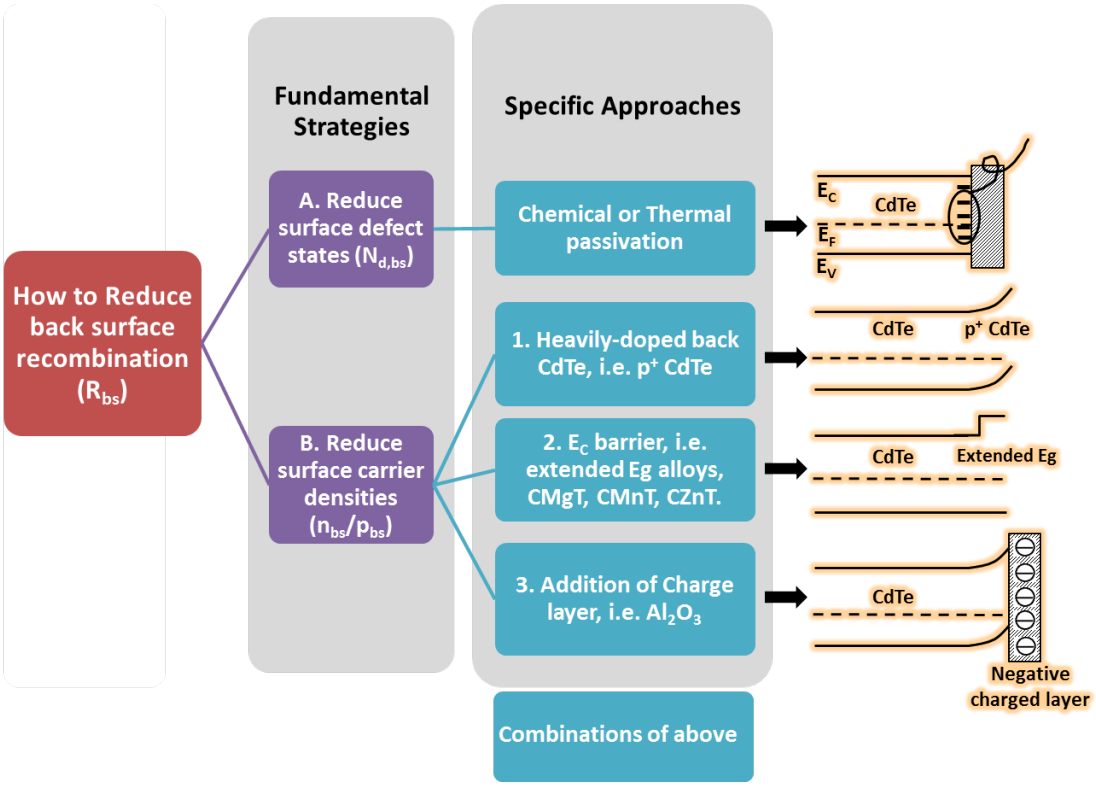

Figure 3.4: Strategies to reduce back surface recombination for CdTe solar cells.

According to Eq. 2.28 in Section 2.1.2, the back surface recombination rate R_{bs} can be described as

$$R_{bs} \approx \frac{n_{bs}p_{bs}}{n_{bs}+p_{bs}}S_{bs} \tag{3.1}$$

where n_{bs} and p_{bs} are the carrier densities at the back surface, and $S_{bs} = N_d\sigma_{n,p}\upsilon_{th}$ is the back surface recombination velocity. Therefore, it is seen that R_{bs} follows from the carrier densities and the density of the defects at the back surface. One way to reduce R_{bs} is with fewer surface defect states N_d, which is often referred to chemical or thermal passivation. It is noted that the highest R_{bs} is achieved at $n_{bs} = p_{bs}$. Consequently, another way to lessen the recombination is by the significant reduction of either type of carrier at the surface, achieved by an electric field. Specific approaches to introduce the electric field include heavy doping of the back absorber, employing extended-E_g material to form a conduction-band E_C barrier, and/or the addition of negative charge layer to repel the surface electrons and lead to a upward E_C barrier (e.g., the dieletric Al_2O_3 layer with negative charge has been successfully used in Si and CIGS PV technologies [42, 43]). Fig. 3.4 summarizes the physical mechanisms of how to reduce the back surface recombination and the corresponding strategies. Note that some practical approaches such as the thermal annealing and/or introducing additional buffer layer may reduce both the surface defects and the surface charge carriers simultaneously. Detailed analysis relevant to these strategies is given in Section 4.3 and 4.4.

3.3 Design Approach - Numerical Simulation

3.3.1 Roles of Simulation

As discussed in Section 2.1.2, the carrier dynamics of a solar cell are governed by three sets of equations (Eq.2.8 - 2.12): the Poisson equation, the continuity equations for electrons and holes, and the current-density equations. Since these equations are coupled and are non-linear, it is very difficult to solve them analytically without major approximations. Instead, the numerical simulation with the aid of appropriate computer software is much more efficient to execute the calculations. Such simulations typically consist of (1) discretization

of the device structure and the governing differential equations, usually called "meshing", (2) application of boundary conditions, and (3) solution of the equation matrix (details can be found in [44, 45]).

Numerical simulation has been widely used in PV community to help understand the device physics of solar cells. It has been a valuable tool to predict cell performance and identify general design principles for cell optimization. Chapter 4 will carry out the design of high-efficiency CdTe cells with the numerical simulation. By combining the characterization results, it can verify the physical mechanisms of the performance losses and other abnormal diode behaviors. The validation of the secondary-barrier-induced J-V distortions in CIGS solar cells with numerical simulation is a good example [46, 26, 27]. Chapter 5 will correlate the experimental results with the simulated results, testing the viability of our model system. In addition, the numerical simulation has become an important technique to interpret characterization results, such as the cathodoluminescence (CL) [47] and the time-resolved photoluminescence (TRPL) [48], though CL and TRPL analysis is not a focus of this dissertation. Note that input parameters in many cases are not well established, so the simulation must be done with only partial knowledge of input parameters. Section 3.3.2 will give general guidances for the selection of these parameters, based on both characterization results and empirical estimates.

3.3.2 Baseline Parameters

Front and Back Contacts

Except for the study of back contact in Section 4.4, the contacts will be assumed to be ohmic, which indicate a flat band alignment at metal/layer interface, as shown in Fig. 3.3(a). A typical 5% of the incident light is assumed to be reflected at the front contact. The surface recombination velocities for electrons and holes at both contacts are chosen to be equal to their thermal velocity ($\sim 10^7 cm/s$) at room temperature.

Layer Properties: TCO, Emitter, and Absorber

As illustrated in Fig. 2.7 and Fig. 2.8 of Section 2.2, the TCO window layer is usually highly doped with large E_g to allow photon transmission. In the model, a highly-doped ZnO layer with E_g of 3.3 eV and n-type doping of 10^{18} cm^{-3} is chosen as the TCO window layer in contact with the emitter.

As summarized in Table 2.2, a variety of deposition techniques have been utilized for growing the emitters and CdTe absorbers. Their material properties may vary with each other depending on the deposition method. The primary material differences for emitters are their band gaps E_g and the induced band alignments (specific emitter parameters will be listed in the corresponding sections).

For polycrystalline (poly)-CdTe material, the carrier concentrations are typically the order of 10^{14} cm^{-3}, but the bulk lifetime may vary from below a nanosecond to tens of nanoseconds depending on the growth ambient and post-treatment [15]. For monocrystalline (mono)-CdTe material, the carrier concentrations and bulk lifetimes have exceeded 10^{16} cm^{-3} and 1 μs, respectively [32, 35]. Note that since it is assumed that there is no fundamental material difference other than the grain boundaries for poly-CdTe, the two categories of CdTe devices - poly and mono CdTe solar cells, are integrated into one model system for much of this work (Section 4.1 and 4.2). Specific problems corresponding to each category will be investigated separately. For instance, the choice of substrate for epitaxial-grown mono CdTe solar cells in Section 4.3 and the possible solutions for avoiding a back contact barrier for poly-CdTe thin-film solar cells in Section 4.4.

Substrate

The substrate assumes an important role in the growth of high-quality epitaxial mono CdTe devices. A suitable substrate for epitaxy must have good lattice match with CdTe, as well as good electrical properties. Four potential candidates, CdTe, Si, GaAs, and InSb, have been considered as the substrate choices for epitaxially grown mono-CdTe absorbers

[33, 34, 35]. In Section 4.3, a numerical study of these substrates on the cell performance is conducted, and specific material parameters of the four substrates are adapted in numerical simulation later.

Table 3.2 lists common input parameters used through modeling work, taken from Refs [20, 49]. Other material parameters which are not included here (labeled with "V" for variable in Table 3.2) will be specified case by case later.

Table 3.2: Baseline input material parameters for CdTe solar cells. "V": the parameter varies case by case; "N.I." for "not included".

Layer parameters	ZnO	Emitter	Interfacial layer	Absorber
Thickness (nm)	200	V	2	V
E_g (eV)	3.3	V	1.5	1.5
ϵ/ϵ_0	9	10	9.4	9.4
N_C (cm^{-3})	2.2×10^{18}	2.2×10^{18}	8×10^{17}	8×10^{17}
N_V (cm^{-3})	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
μ_n (cm^2/Vs)	100	100	320	320
μ_p (cm^2/Vs)	25	25	50	50
n, p (cm^{-2})	$n : 10^{18}$	n: V	N.I.	p: V
ΔE_C (eV)	0		V	
Defect states (determine τ_{SRH}, see Eq. 2.22): Gaussian-distribution, Mid-gap				
Defect type	Donor	Acceptor	Acceptor	Donor
σ_n (cm^2)	10^{-12}	10^{-12}	10^{-12}	10^{-11}
σ_p (cm^2)	10^{-15}	10^{-17}	10^{-12}	10^{-14}
N_d (cm^{-3})	10^{15}	10^{17}	V	V

3.3.3 Comparison of Software Packages

A variety of software packages have been developed for numerical simulations. Most have been written by researchers from universities and research institutes and can be used without charge. These include the commonly-used programs: AFORS-HET, AMPS-1D, wxAMPS (revised version of AMPS-1D), SCAPS-1D, ADEPT, and PC1-D, all of which are one-dimensional and can be applied to understand the physical operation of a solar cell. However, they do not have the capability to model multi-dimensional structures and other sophisticated characteristics like tunnel diode, photon management, and point contact features. Currently, the modeling of these advanced features can be achieved with commercial software packages, such as Atlas by Silvaco and Sentaurus by Synopsys. SCAPS-1D and AFORS-HET also include a few useful advanced settings, such as layer parameters grading (i.e., E_g, carrier densities, etc.) and choices of multiple recombination processes.

Table 3.3 briefly compares four software packages the author has used in his PhD work (wxAMPS [50], AFORS-HET [51], SCAPS-1D [52], and Sentaurus [53]). In Chapter 4, the software packages will be specified for the corresponding modeling task. From the author's modeling experience, the straightforward and user-friendly simulation software wxAMPS is suggested as a starting tool. As the modelers become familiar with the simulation parameters and are able to define their own tasks for modeling, they may turn to more powerful tools, such as AFORS-HET and SCAPS-1D. The TCAD-Sentaurus tool is more powerful, but may be difficult to fully utilize without considerable knowledge of device physics and computer programing.

Table 3.3: Comparison of the simulation packages used in this work.

	wxAMPS	AFORS-HET	SCAPS-1D	Sentaurus
User friendliness	++	+	+	–
Batch processing	No	No	Yes	Yes
Simulation mode	DC	DC, AC, transient	DC, AC	DC, AC, transient
Simulation Dimension	1-D	1-D	1-D	Multi-D
Advanced settings (e.g., layer grading)	No	Yes	Yes	Yes (coding-based)
Customer support	No	No	No	Yes
Cost	Free	Free	Free	Expensive
Power	Fair	Good	Good	Excellent

Chapter 4

SIMULATION RESULTS FOR HIGH-EFFICIENCY CDTE SOLAR CELLS

By applying the design principles discussed in the previous chapter, crucial issues limiting CdTe cell performance can be addressed and specific strategies to evaluate high-efficiency CdTe solar cells proposed. Since the CdTe absorber is central to cell performance, several important CdTe material parameters relevant to high-efficiency devices are investigated. An equally important consideration is the interfaces between different layers of CdTe cells. One of these is the emitter/absorber interface, discussed with various band alignments and interface defect types affecting interfacial recombination. The CdTe/substrate interface is also important, particularly in the growth of epitaxial monocrystalline CdTe cells. It has emphasis on the choices of substrate materials. Finally, the CdTe/back contact interface for conventional polycrystalline CdTe devices is studied to identify the roles of a potential buffer layer and the metallic back contacts itself.

4.1 Material Optimization of CdTe Absorber

4.1.1 Review

Although existing device models [38, 54] provide general support for the need to increase values of the carrier density p and bulk minority carrier lifetime τ, they have not provided specific parameter requirements for efficiencies $> 20\%$ in CdTe. In this section, an expanded range of both p and τ is included in numerical simulation to estimate the maximum device performance achievable with a high-quality CdTe structure. The effect of absorber thickness is also taken into account. The primary goal of the device modeling here is to provide guidance for optimizing the device design for future high-quality CdTe solar cells and to help interpret experimental data from non-ideal materials.

Since the goal of this section is to explore the performance potential of the CdTe absorber, the baseline structure adopted here assumes a CdTe homojunction with ohmic front and back contacts and no interface traps, as shown in Fig. 4.1a. In this model, the only variations take place in the absorber layer (the carrier density p, the bulk minority carrier lifetime τ, and the CdTe thickness). Other material parameters can be found in Table 3.2. Fig.4.1b shows its calculated energy band diagram at equilibrium with absorber carrier density, $p = 5 \times 10^{16}$ cm^{-3}. The numerical simulations were performed with the software package AFORS-HET v2.4.1.

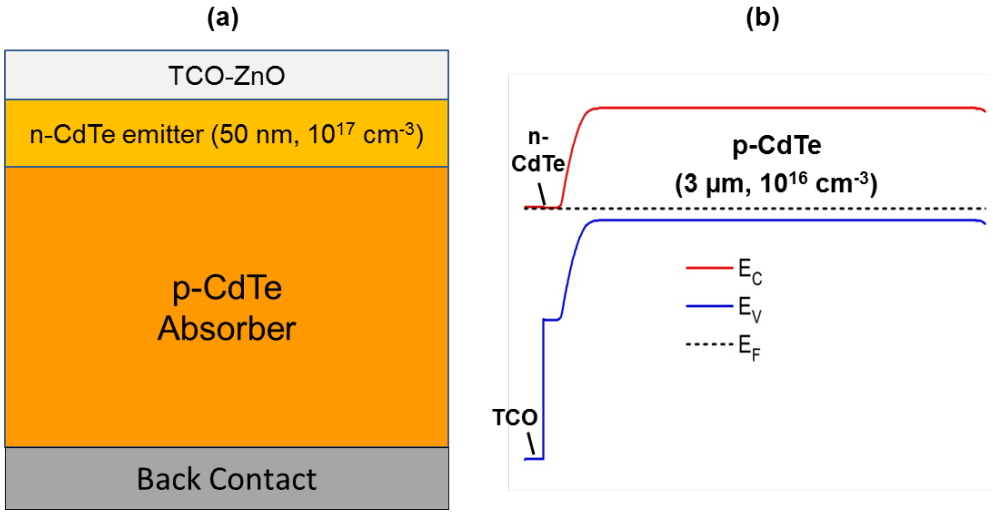

Figure 4.1: (a) Baseline device structure used in Section 4.1. (b) Simulated energy-band diagram at equilibrium with this structure, $p = 5 \times 10^{16}$ cm^{-3}.

4.1.2 Combined Effects of CdTe Doping and Lifetime

The carrier density p and minority carrier lifetime τ for a poly-crystalline CdTe device span a relatively low range, but epitaxial cells have the potential for a much greater range. Hence, here we assume a 3-μm-thick CdTe absorber and expand its range to include parameters reasonable for epitaxial mono-CdTe absorbers to investigate the combined effect of p and τ. Fig. 4.2 shows the contour plots for the primary performance parameters as a function of p and τ.

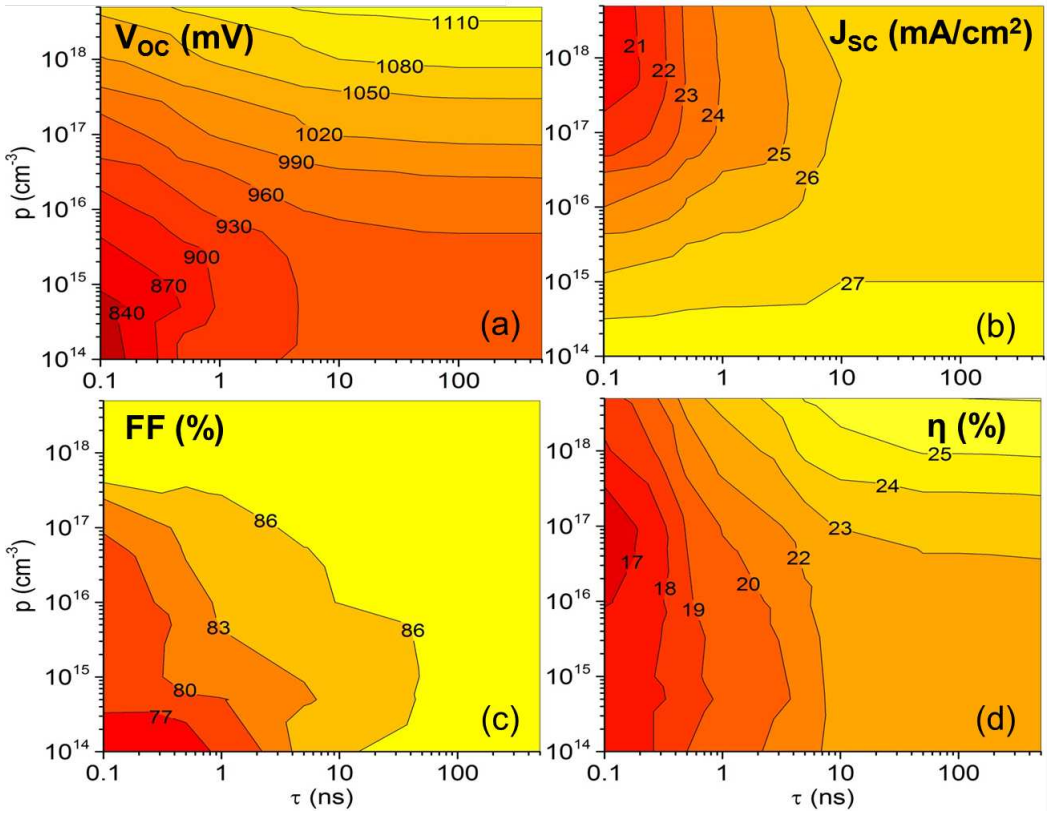

Figure 4.2: Contour plots of V_{OC}, J_{SC}, FF, and η for simulated device parameters as a function of carrier density p and lifetime τ in the CdTe absorber.

In Fig. 4.2(a), the open-circuit voltage V_{OC} is predicted to increase with higher carrier density and longer minority carrier lifetime. In the region where a low carrier density and minority carrier lifetime exist (the lower left in the contour plots), efficient carrier recombination takes place in the bulk, inducing large recombination current and thus low V_{OC}. For reasonably large carrier density ($> 10^{15}\ cm^{-3}$), a simple relationship between absorber carrier density p and V_{OC} increase can be approximated as [23]

$$\Delta V_{OC} \approx kT \ln(p/p_0) \tag{4.1}$$

where p_0 is a reference carrier density. Accordingly, V_{OC} increases by approximately 60 mV per decade (or kT/q per factor of e) in the absorber carrier density, as seen in Fig. 4.3. V_{OC} consistently increases with p since the bulk SRH recombination decreases with increased p (because the dark minority carrier density n in p-CdTe absorber is given by n_i^2/p, an increased

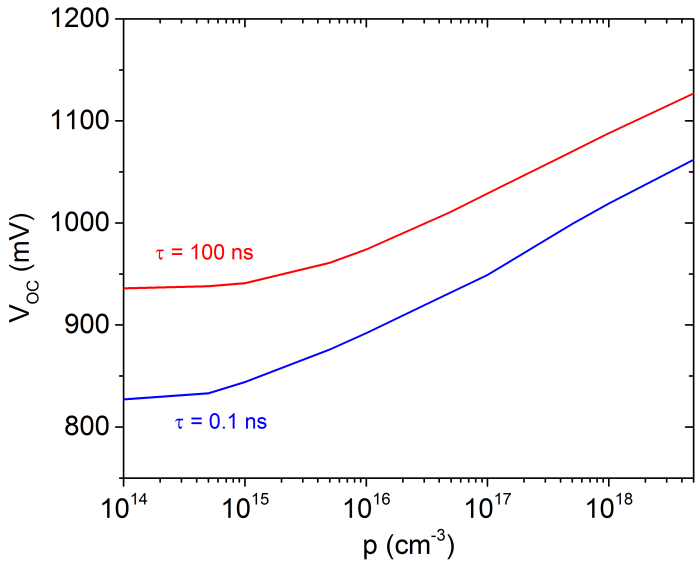

Figure 4.3: V_{OC} vs. p for two values of τ in CdTe absorber: 1 ns and 100 ns.

p leads to a decreased n and hence smaller bulk SRH recombination, $R_{SRH} = \Delta n/\tau_n$, see Section 2.1.2). More physical explanation can be found in [23]. For small p and τ, τ dominates the carrier recombination and thus p has much less impact on V_{OC}, since the minority electron carriers have very short diffusion length (e.g., $L_{D,n} \approx 0.3\ \mu m$ for $\tau = 0.1$ ns) and hence has little chance to be collected. For small p but high τ (e.g., $\tau = 100$ ns, $L_D \approx 10\ \mu m$), V_{OC} is also independent of p. This is because of limited absorber thickness, and greater impact from the back surface recombination (detailed explanation can be found in the next section and Fig. 4.6).

The short-circuit current J_{SC} in Fig. 4.2(b) shows a different trend: J_{SC} suffers a loss at high carrier density when lifetime is in the low region (0.1-10 ns). From the simulated QE (Fig. 4.4) with varying p at two fixed low lifetimes ($\tau = 1$ and 10 ns), it is observed that J_{SC} loss for high p is primarily from the loss of long-wavelength photo-generated carriers. Because of a longer path length, there is more long-wavelength QE loss with increasing p at $\tau = 1$ ns. Since the space-charge region (SCR) narrows while the carrier density p in the absorber is comparable to the n-type buffer ($p = 1 \times 10^{17} cm^{-3}$), a greater number of photo-generated carriers with short lifetime will recombine in the quasi-neutral region and even at

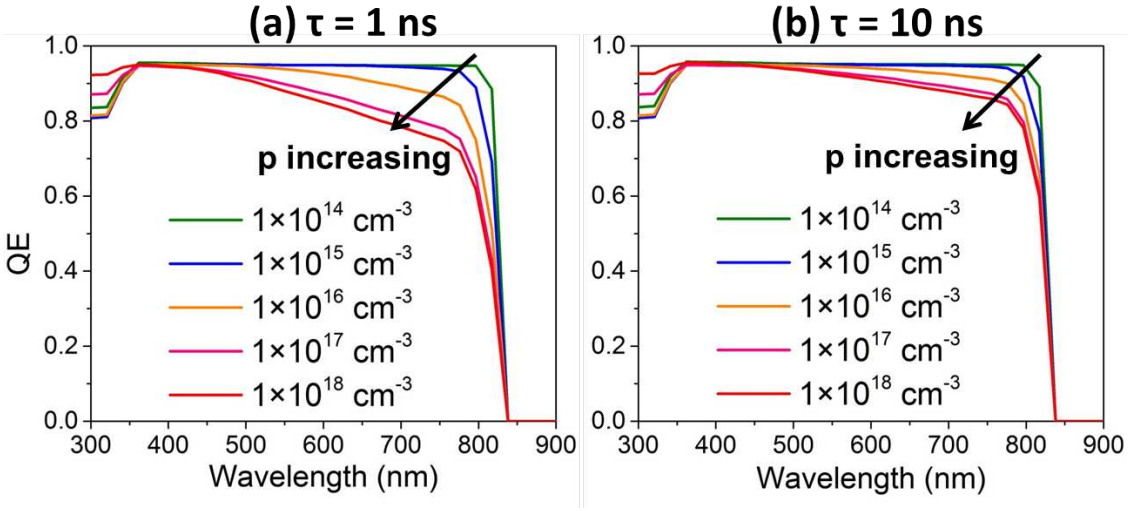

Figure 4.4: Calculated QE for two fixed lifetimes $\tau = 1$ ns and 10 ns, and varying absorber carrier density p.

the back surface where there is not an electric field to assist carriers collection. This J_{SC} loss is true at high carrier density range, but for $p < 5 \times 10^{15}\ cm^{-3}$, J_{SC} is almost independent of lifetime due to a stronger built-in electric field assisting the extraction of charge carriers. Fig. 4.2(c) shows that FF is relatively poor at low τ and p due to significant recombination, and becomes higher in the region with high p and τ. Therefore, the overall device efficiency will also be highest for high carrier density and long lifetime.

4.1.3 CdTe Thickness

CdTe has a large absorption coefficient, and most of the light generation occurs in the first micron of the CdTe absorber. In practice, thin polycrystalline CdTe devices ($\sim$1 μm) have been made without a large compromise in efficiency at Colorado State University. However, the question is whether a high-quality thin monocrystalline CdTe device could achieve higher performance with only modest V_{OC} and J_{SC} loss. In this section, Fig. 4.5 shows simulated device performance of varying the absorber thickness (0.5 - 20 μm) at three different minority carrier lifetimes (1, 10, 100 ns) while setting p fixed at $5 \times 10^{16}\ cm^{-3}$ for high carrier concentration, which is reasonable for mono-CdTe absorbers.

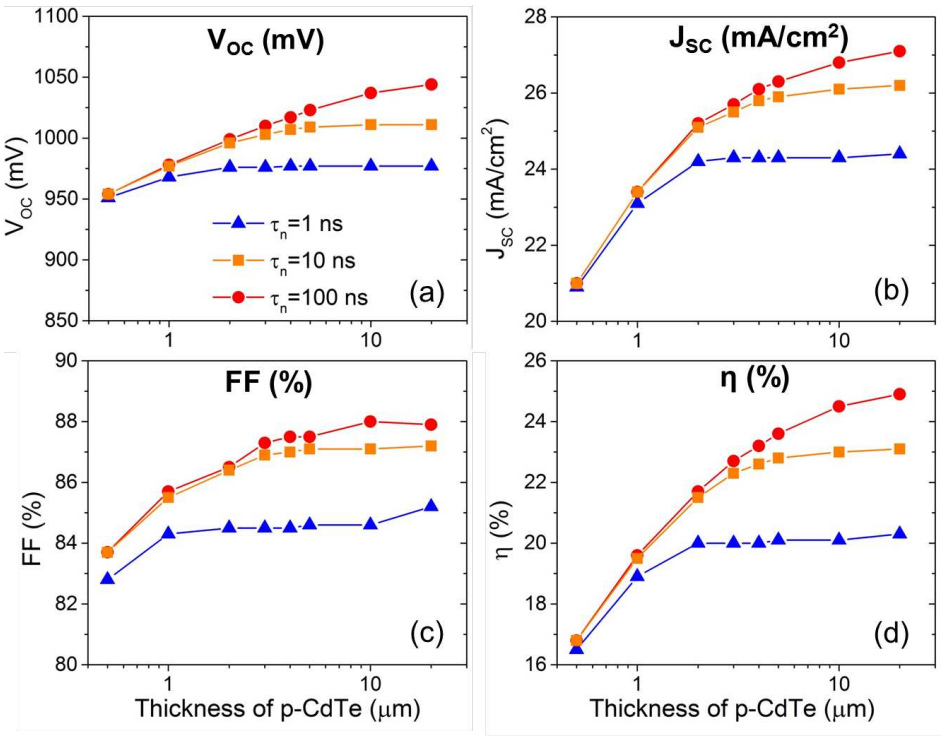

Figure 4.5: Simulated device performance of varying the absorber thickness from 0.5 to 20 μm with τ = 1, 10, 100 ns and $p = 5 \times 10^{16}\ cm^{-3}$.

For short lifetimes and low diffusion lengths, V_{OC} improves only slightly with increasing absorber thickness. For instance, with τ = 1 ns, V_{OC} improves slightly as the thickness increases over a few microns and then saturates. For longer lifetimes, there is a greater increase in V_{OC} up to 3 μm. This increase is due to a lower Shockley-Read-Hall (SRH) recombination rate in the quasi-neutral region (QNR) rather than in the space-charge region (SCR). The SCR width for $p = 5 \times 10^{16}\ cm^{-3}$ is narrow, ~0.2 μm, and thus has less effect on the V_{OC} loss compared to the much thicker QNR (more explanation in next paragraph). Fig. 4.5(b) shows that for short lifetimes, J_{SC} increases significantly for the first 2 μm where most photon collection takes place, and then becomes saturated. For longer lifetime cases (10 and 100 ns), however, J_{SC} shows greater improvement with thicker CdTe absorbers, primarily due to a longer diffusion length and lower defect recombination in the bulk regions. In Fig. 4.5(c), FF for all lifetime cases shows a modest increase with absorber thickness. The efficiency η in Fig. 4.5(d) increases as the absorber thickness increases to 3 μm, then shows

little change except for the very high lifetime case. The analysis here indicates that there is in general little benefit from increasing the absorber thickness above 3 μm unless the lifetime is significantly greater than 10 ns.

These simulations assumed a very high recombination velocity $S_b = 10^7$ cm/s at the back contact. Note that at $\tau = 100$ ns, both V_{OC} and J_{SC} still increase slightly even with 20-μm-thick CdTe absorber. However, if the back surface recombination is lower, V_{OC} and J_{SC} will vary less with thickness, especially for thinner devices. Fig. 4.6 shows how V_{OC} and J_{SC} should change when S_b is varied from 10 to 10^7 cm/s for $\tau = 100$ ns. In Fig. 4.6(a), the impact of the first few microns ($< 3\mu m$) on V_{OC} is much greater with lower S_b (= 10 cm/s) than with high S_b. This is due to fewer photo-generated carriers diffusing to the back surface and to recombine when S_b is lower. At $S_b = 10$ cm/s, V_{OC} decreases with increasing absorber thickness, because carriers recombine to a greater extent in the thicker bulk region. At high S_b, however, V_{OC} increases with the absorber thickness, as the back contact becomes less of a factor. For thick CdTe, V_{OC} converges to the same value for all values of S_b.

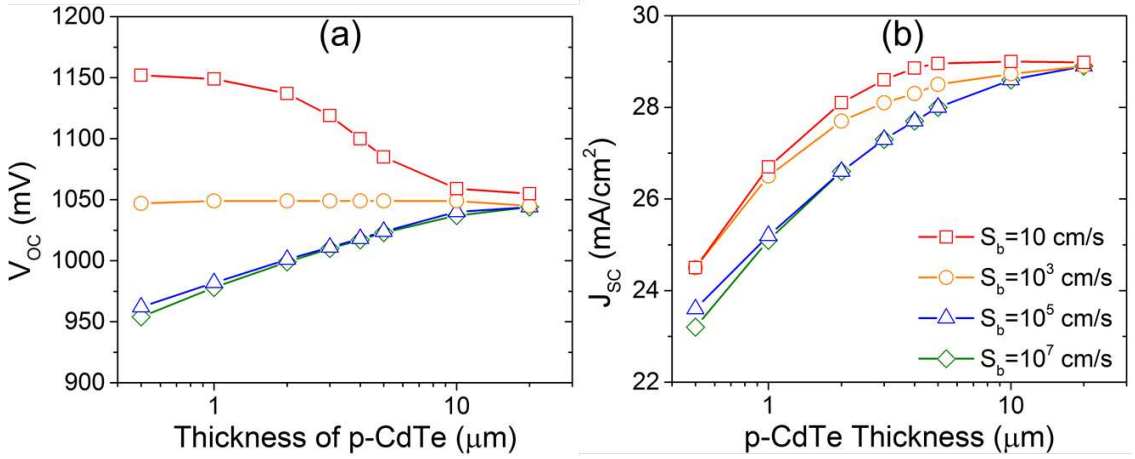

Figure 4.6: Simulated V_{OC} and J_{SC} for varying p-CdTe thickness with the back surface recombination velocity $S_b = 10, 10^3, 10^5, 10^7 cm/s$ at $\tau = 100$ ns.

Fig. 4.6(b), which assumes no optical reflection from the back contact, shows that J_{SC} increases over the first few microns ($< 3\mu m$) due to greater photon absorption. At high S_b (= 10^7 cm/s) and thin CdTe, a significant fraction of the electrons reach the back surface

and recombine. There is less electron recombination loss for thicker CdTe ($> 10\mu m$) at the back surface and high S_b, thus an increase in J_{SC}. J_{SC} with low S_b has slightly greater variation over the first few microns compared to the J_{SC} with high S_b, but also saturates for thicker cells as the effect of back surface recombination diminishes.

In other words, as the bulk lifetime increases, an appropriate buffer layer or other strategy is strongly desired to reduce the back surface recombination while utilizing a relatively thin absorber. The passivation of the back surface recombination has been widely accepted in other PV technologies such as GaAs and Si [55]. Fig. 3.4 in Section 3.2.2 has summarized a strategy roadmap to reduce the back surface recombination for CdTe solar cells. A comprehensive study on these approaches will be given in Section 4.3 and 4.4.

4.1.4 Summary

In this section, the device performance for high-quality CdTe absorbers has been investigated over a wide range of both carrier density p and minority carrier lifetime τ. High V_{OC} above 1000 mV should be achievable when the absorber has a high carrier density ($> 10^{16}$ cm^{-3}). However, superior device performance with $\eta > 25\%$ requires both high carrier density and lifetime. Simulated variations in the thickness of CdTe absorber show that the efficiency improvement for thicker absorbers with high back surface recombination S_b is due to enhancement of both J_{SC} and V_{OC}. However, the variations above 3 μm are modest when the back-contact recombination is relatively small, indicating that the passivation of the back surface is strongly needed. Overall, CdTe material has shown the feasibility of high-efficiency (V_{OC} >1100 mV, $\eta > 25\%$), though much more careful designs are needed in terms of device integration (see Section 4.2-4.4).

4.2 Role of Emitter/Absorber Interface

The performance of CdTe solar cells can be very sensitive to the emitter/absorber interface, especially for high-efficiency cells with high bulk lifetime. One straightforward way to

minimize the interface defects is to employ lattice-matched materials. The III-V PV community therefore pays considerable attention to lattice matching. If the interface defects are unavoidable for CdTe solar cells, then there are other possibilities to reduce losses due to the interfacial recombination.

One effective approach to mitigate the interfacial recombination in CdTe solar cells is to engineer the band alignment at the emitter/absorber interface by forming a moderate conduction-band spike to induce large absorber inversion [23, 56, 57]. Similar studies were conducted in the CIGS solar cell community [27, 58]. However, most studies describe the impact of interfacial recombination only in terms of the interfacial recombination velocity S_{IF}, which is directly related to the density of interface states. In this section, we discuss the other properties that also affect the interfacial recombination rate. For instance, the doping density and thickness of the emitter, and the type and energetic location of interface defects, can play a role in the band bending at the emitter/absorber interface and determine the interfacial recombination rate.

Using numerical simulation, this section will give an in-depth study of these aspects of emitter/absorber interface physics and provide insights on how to suppress the detrimental interfacial recombination if the interface defects are unavoidable. In addition, four practical emitter candidates, CdS, Cd(S,O), (Mg,Zn)O, and CdMgTe, are compared to give more specific guidance for CdTe cell fabrication. While this work concentrates on the CdTe devices, the principles and analyses presented should be relevant and applicable to other PV technologies.

4.2.1 Review

As with many other simulation studies [23, 56, 57], we use the interfacial recombination velocity S_{IF} to describe the interface defects. However, the interfacial recombination, which directly impacts the diode current and hence V_{OC}, is also affected by: (1) the band alignment at the emitter/absorber interface; (2) the emitter properties, such as doping and thickness; and (3) the energetic location and defect type of the interface defects, $E_{d,IF}$.

Mathematically, these factors affecting the interfacial recombination rate R_{IF} can be described by Eq. 2.28, shown here again for the convenience of discussion:

$$R_{IF} = \frac{n_{IF}p_{IF} - n_i^2}{S_p^{-1}(n_{IF} + n^*) + S_n^{-1}(p_{IF} + p^*)} \tag{4.2}$$

where n_{IF} and p_{IF} are the electron and hole concentrations at the interface, which are determined by the band offsets and band bending (they in turn determine the carrier availability for recombination). $S_n = N_{d,IF}\sigma_n\upsilon_{th}$ and $S_p = N_{d,IF}\sigma_p\upsilon_{th}$, are the interfacial recombination velocities for electrons and holes in units of cm/s. Here, $N_{d,IF}$ is the surface defect density and has units of cm^{-2}. Electron and hole capture cross-sections $\sigma_{n,p}$ of $10^{-12}cm^2$ were chosen to represent the attractive charge non-radiative recombination centers for both electrons and holes (smaller $\sigma_{n,p}$ with neutral cross-sections will have less impact on interfacial recombination) and hence $S_{IF} = S_n = S_p$.

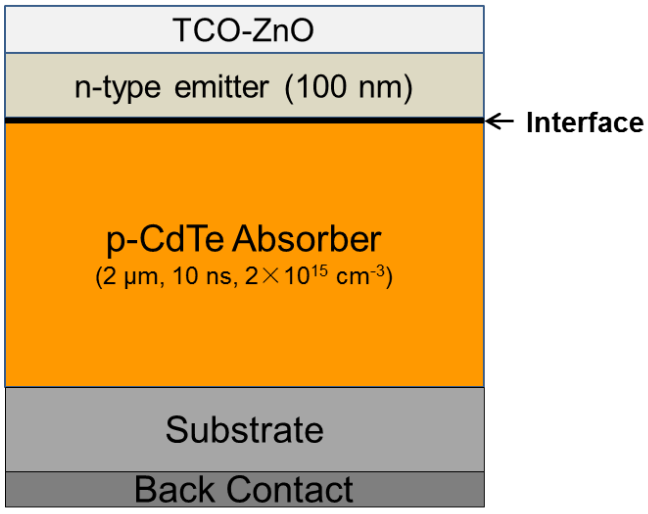

Figure 4.7: Baseline device structure used in the numerical simulations of Section 4.2.

Additionally, both the emitter properties (i.e. emitter doping and thickness) and the charge types of the interface states can change the potential near the interface and thus the carrier concentrations. n_i is the intrinsic carrier concentration, which can be neglected in forward bias. The quantities $n^* = N_C \exp\left[-(E_{C,IF} - E_{d,IF})/kT\right]$ and $p^* = N_V \exp\left[-(E_{d,IF} - E_{V,IF})/kT\right]$ are related to the emission rates from the interface defect states $E_{d,IF}$ to the

corresponding band-edge E_C or E_V, respectively. According to Eq. 4.2 and the expressions of the n^* and p^*, the effectiveness of the interfacial recombination depends on the energetic location of the defects.

The effect of emitter/absorber interfacial recombination on cell performance was evaluated with SCAPS-1D Software. In this section, the CdTe cell is assumed to have a substrate structure (see Fig. 4.7), though the simulations would be similar for a superstrate configuration. The basic structure consists of a highly-doped (10^{18} cm^{-3}) ZnO layer as a TCO window for lateral current collection adjacent to front contact, an emitter layer with adjustable material properties, and a 2-μm-thick CdTe absorber. Other material parameters are taken from Table 3.2. The hole density p of poly-CdTe absorbers has typically been the order of 10^{14} cm^{-3}. However, to also reflect the larger hole concentration in substrate-grown epitaxial CdTe devices of 10^{16} cm^{-3} and above [32], an intermediate hole concentration of 2×10^{15} cm^{-3} was chosen for the baseline model. Unless otherwise stated, the bulk minority-carrier lifetime is set to 10 ns for a typical CdTe absorber. Note that the role of interface properties will become more critical with improved bulk lifetime, since the bulk recombination will be less of a limitation on cell performance as discussed in Section 4.1.

4.2.2 Conduction-Band Offset ΔE_C

The emitter/absorber conduction-band offset ΔE_C has a major influence on band bending and hence on interfacial recombination. A positive ΔE_C at the emitter/absorber interface induces stronger band bending. Conversely, a larger hole barrier $E_{p,IF(CdTe)}$, and a negative ΔE_C results in less band bending and a smaller hole barrier, as shown in Fig. 3.2. In this section, a one-sided heterojunction ($n_e = 10^{17}$ $cm^{-3} \gg p_a = 2 \times 10^{15}$ cm^{-3}) with a 100-nm emitter layer and mid-gap interface acceptor-type defect states are assumed. Hence, p_{IF} is smaller than n_{IF}, n^* and p^* are negligible, and the recombination rate R_{IF} in Eq. 4.2 is nearly proportional to S_{IF}

$$R_{IF} \approx S_{IF} p_{IF,a} \tag{4.3}$$

where $p_{IF,a} = N_{V,a} \exp\left(-E_{p,IF(CdTe)}/kT\right)$ is the hole concentration on the absorber side (the hole concentration at the emitter side is omitted since it is much smaller than $p_{IF,a}$. R_{IF} is therefore governed by the interfacial recombination velocity S_{IF} and the hole concentration at the absorber side $p_{IF,a}$. Note that the high-conductivity ZnO window layer has little effect on the band bending in the one-sided emitter/absorber junction. This is because the doping of ZnO is much larger than the emitter and absorber, and the potential drop in ZnO layer is negligible (i.e., nearly all potential drops in the emitter/absorber junction).

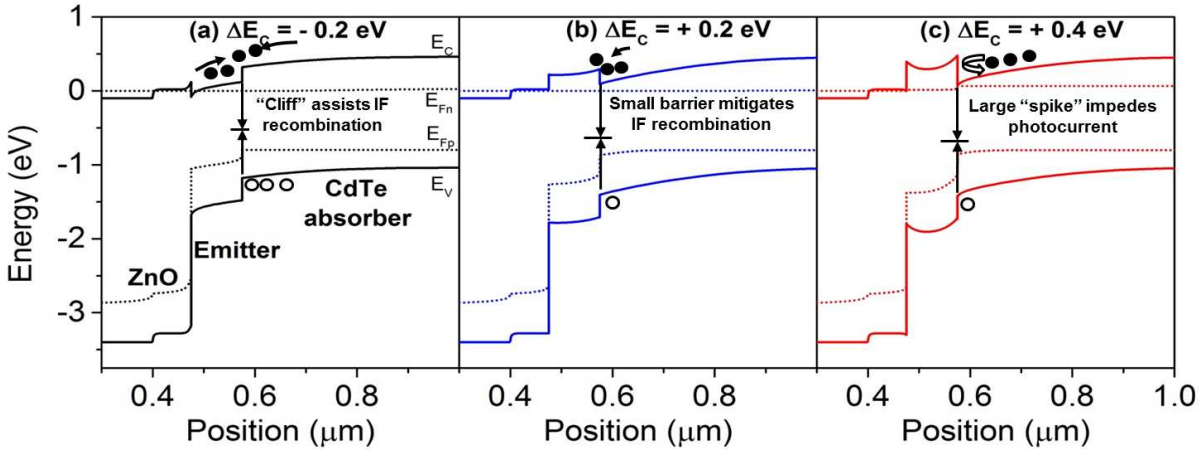

Figure 4.8: Three representative ΔE_C cases of CdTe energy-band diagrams under illumination at 0.8-V bias, $\Delta E_V = +0.3$ eV in each case.

Fig. 4.8 shows the band diagrams for three representative ΔE_C cases for CdTe solar cells with the same valence-band offset ΔE_V. A bias of +0.8 V is used to accentuate the amount of band flattening in the operational range of the cell. In Fig. 4.8a, with a cliff in the conduction band (ΔE_C = -0.2 eV), there is a relatively small hole barrier $E_{p,IF(CdTe)}$, indicating only weak inversion at the CdTe surface. The corresponding small band bending at the interface allows a significant number of holes to recombine with the electrons from either side. As a result, the enhanced recombination current will lead to a reduction of V_{OC}. This is illustrated in the J-V curves of Fig. 4.9a, for $S_{IF} = 10^5$ cm/s and bulk lifetime τ of 10 ns. The J-V curves with a smaller value of τ (0.5 ns) and a lower hole density (10^{14} cm^{-3}) are calculated to reflect the bulk properties of lower-performance CdTe cells. The

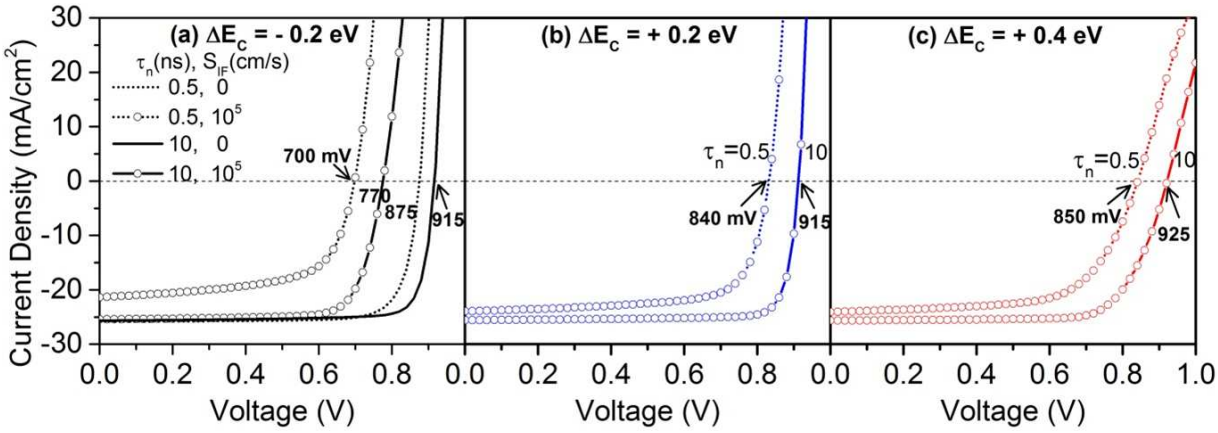

Figure 4.9: Calculated J-V curves for the three ΔE_C cases in Fig. 4.8. In (a), lower voltage results from either low τ or large S_{IF}. (b) and (c) are nearly independent of S_{IF}. A hole density of 2×10^{15} cm^{-3} was used for the 10-ns curves and 1×10^{14} cm^{-3} for the 0.5-ns ones.

calculations show that poorer bulk properties increase the voltage drop at large S_{IF}, and with the enhanced bulk recombination the J-V curves are distorted to varying degrees by the voltage-dependent collection. As the bulk properties continue to improve, the interfacial recombination becomes a significant limitation on cell efficiency.

In contrast, a small positive barrier ($\Delta E_C = +0.2$ eV in Fig. 4.8b) gives rise to a larger built-in potential. The holes on the CdTe side become minority carriers since the absorber is inverted in the vicinity of the interface. As a result, the interfacial recombination is suppressed due to insufficient holes to recombine with the interface electrons. The interfacial recombination no longer dominates, and the voltage is much less dependent of S_{IF}, though V_{OC} is still reduced and the knee of the curve is weaker when larger bulk recombination exists ($\tau = 0.5$ ns).

However, if the spike is too large (i.e., $\Delta E_C = +0.4$ eV in Fig. 4.8c), V_{OC} remains high, actually slightly higher, since the large spike will be a larger barrier for forward diode current. But the photo-generated electrons are partially blocked in forward bias [26, 27]. The reduced photocurrent at forward bias will appear as a fill-factor (FF) loss and eventually a reduction of J_{SC} for ΔE_C above 0.4 eV. The corresponding J-V curves are shown in Fig. 4.9c.

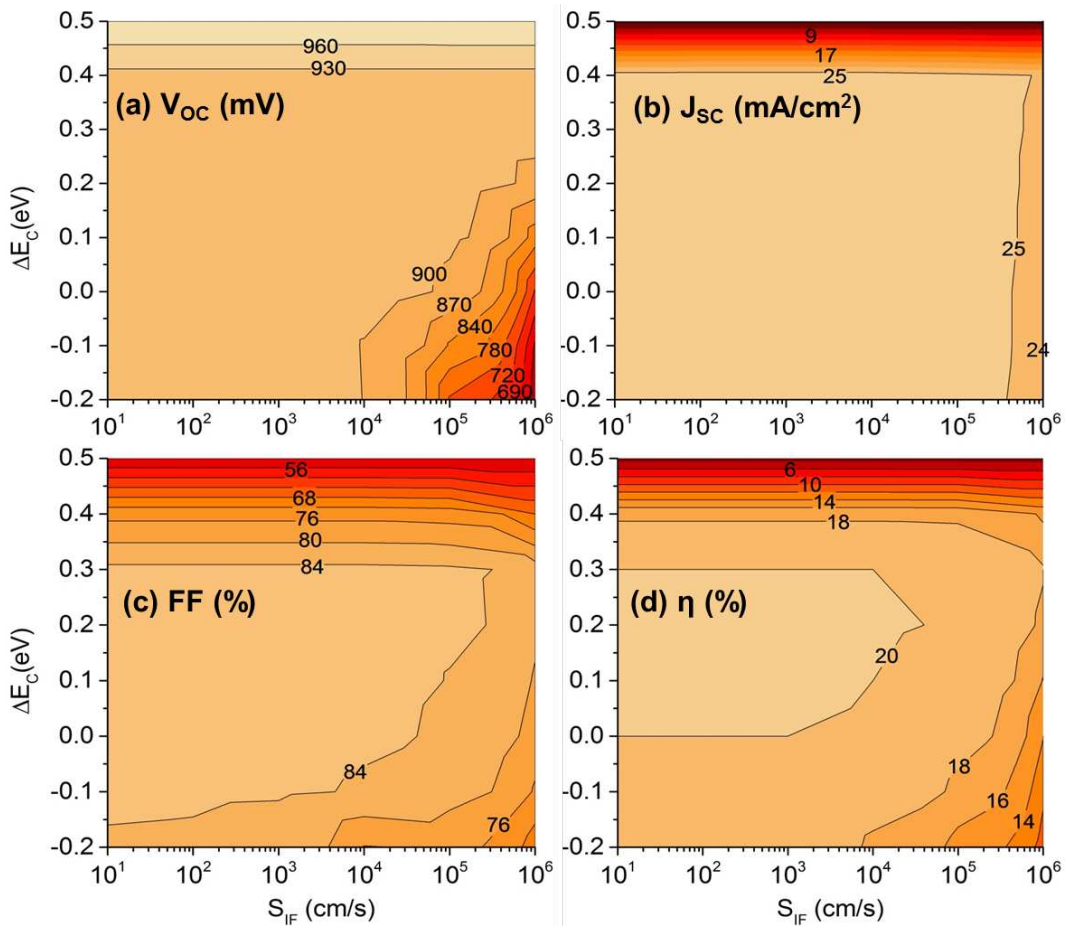

Figure 4.10: Calculated contour plots for the key parameters with varying S_{IF} and ΔE_C.

Contour plots of the calculated J-V parameters for a range of conduction-band offsets ΔE_C and interfacial recombination velocities S_{IF} are shown in Fig. 4.10. The emitter/absorber band alignment determines how forgiving the device performance is toward interface defect density: with a spike between 0.1 and 0.3 eV, S_{IF} the order of 10^5 cm/s can be tolerated; but for zero offset, it should be kept near or below 10^4 cm/s; and for any significant cliff, it needs to be kept quite small. One region of reduced efficiency is the lower right with the cliff and large interfacial recombination. Here the lower efficiency is primarily due to reduced voltage (caused by enhanced interfacial recombination) and secondarily to FF (caused by insufficient carrier collection with weak band bending and hence lower electric field). The other problematic area is the large conduction-band spike that limits the photocurrent collection and thus a loss of J_{SC} and FF independent of S_{IF}. Note that

the large spike ($\Delta E_C \geq 0.4$ eV) induces a slightly larger V_{OC} due to the barrier for forward diode current, but the voltage increase is overshadowed by the photocurrent blockage and consequent reduction in J_{SC} and FF.

4.2.3 Emitter Doping and Thickness

The emitter doping and thickness can also have an impact on the interfacial recombination [25, 59]. Assuming a fixed absorber doping ($p = 2 \times 10^{15}\ cm^{-3}$) and acceptor-type mid-gap interface states as before, variations of emitter doping change the potential distribution across the junction, which causes different degrees of absorber band bending, as shown in Fig. 4.11. In this case, an emitter thickness of 100 nm was assumed. Since n^* and p^* are

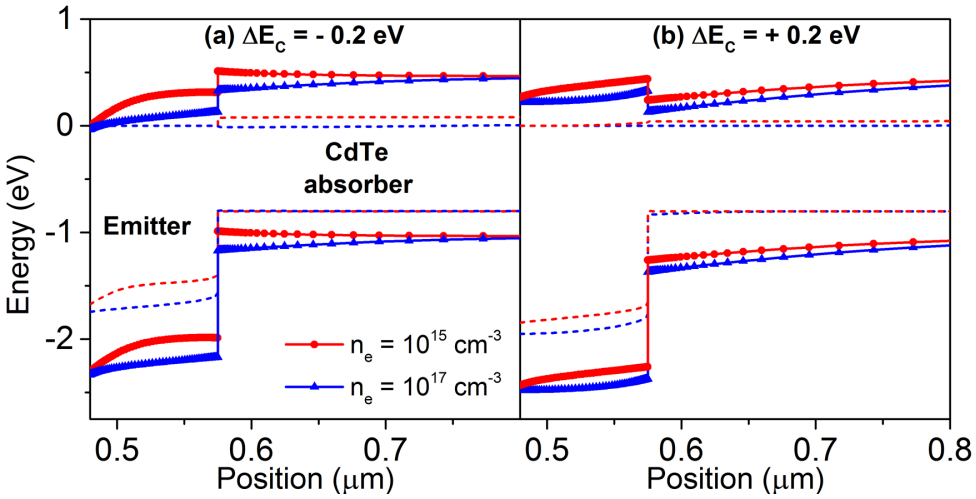

Figure 4.11: Energy band diagrams under illumination at 0.8-V bias with two ΔE_C and two emitter doping cases (10^{15} and $10^{17}\ cm^{-3}$).

negligible at the mid-gap state, Eq. 4.2 can be approximated by:

$$R_{IF} \approx \frac{n_{IF} p_{IF}}{n_{IF} + p_{IF}} S_{IF} \tag{4.4}$$

the recombination rate here is determined by both S_{IF} and the electron and hole densities at the interface. Fig. 4.12a shows the electron and hole densities (n_{IF} and p_{IF}) with varying emitter doping n_e for two values of ΔE_C.

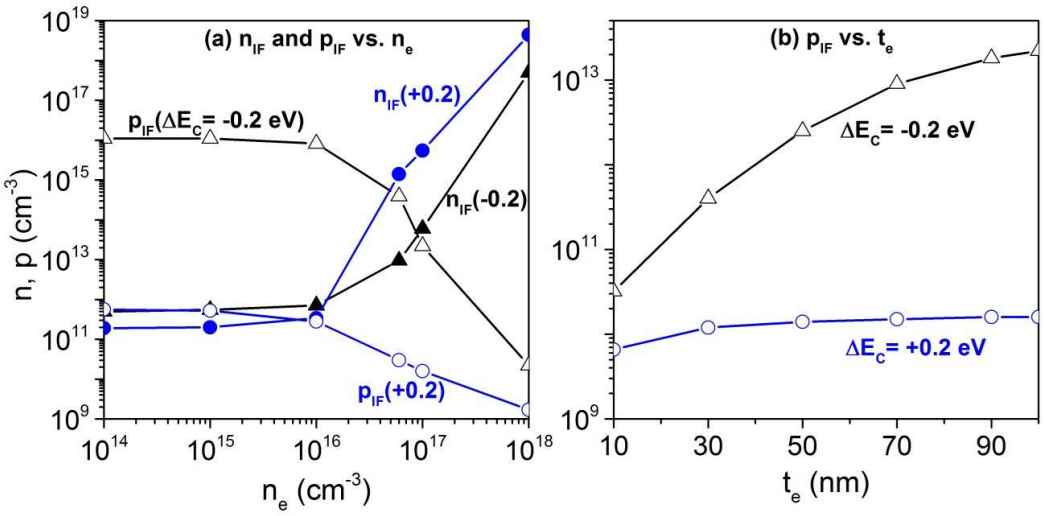

Figure 4.12: (a) Electron and hole densities (n_{IF} and p_{IF}) at the emitter/absorber interface with two ΔE_C under illumination, at 0.8-V bias and emitter thickness of 100 nm. (b) Interfacial hole density as a function of emitter thickness at a fixed emitter doping of 10^{17} cm^{-3}.

For a cliff offset (ΔE_C = -0.2 eV, Fig. 4.11a) and emitter doping smaller than absorber doping (e.g., $n_e = 10^{15}$ $cm^{-3} < p = 2 \times 10^{15}$ cm^{-3}), the electrical potential primarily drops in the emitter (note that the potential drop can be limited by the emitter thickness, which will be discussed later), and there is little absorber band bending in forward bias, indicating limited electrons but sufficient holes at the interface, as shown in Fig. 4.12a. R_{IF} is governed by the availability of electrons at the interface and will be enhanced with large S_{IF}. The impact of these features on cell parameters is shown in Fig. 4.13a. In particular, a significant V_{OC} loss occurs at $S_{IF} = 10^6$ cm/s. Though such significant S_{IF} is possible, this is a very high value. The experimental TRPL data has estimated a large $S_{IF}, \sim$ 1-5 $\times 10^5$ cm/s at either CdS/CdTe or (Mg,Zn)O/CdTe interfaces [60, 61, 62, 63].

When the emitter doping is much higher than the absorber doping (e.g., $n_e = 10^{18}$ cm^{-3} $>> p = 2 \times 10^{15}$ cm^{-3}), the potential mostly drops in the absorber and thus induces absorber band bending even at 0.8-V bias. The much smaller density of interfacial holes (Fig. 4.12a) limits forward current, and large V_{OC} is restored. There is a midpoint near 5×10^{16} cm^{-3} where the electron and hole concentrations at the interface are approximately equal and the

interfacial recombination is maximized. Hence, there is a minimum in V_{OC}, as shown in Fig. 4.13a.

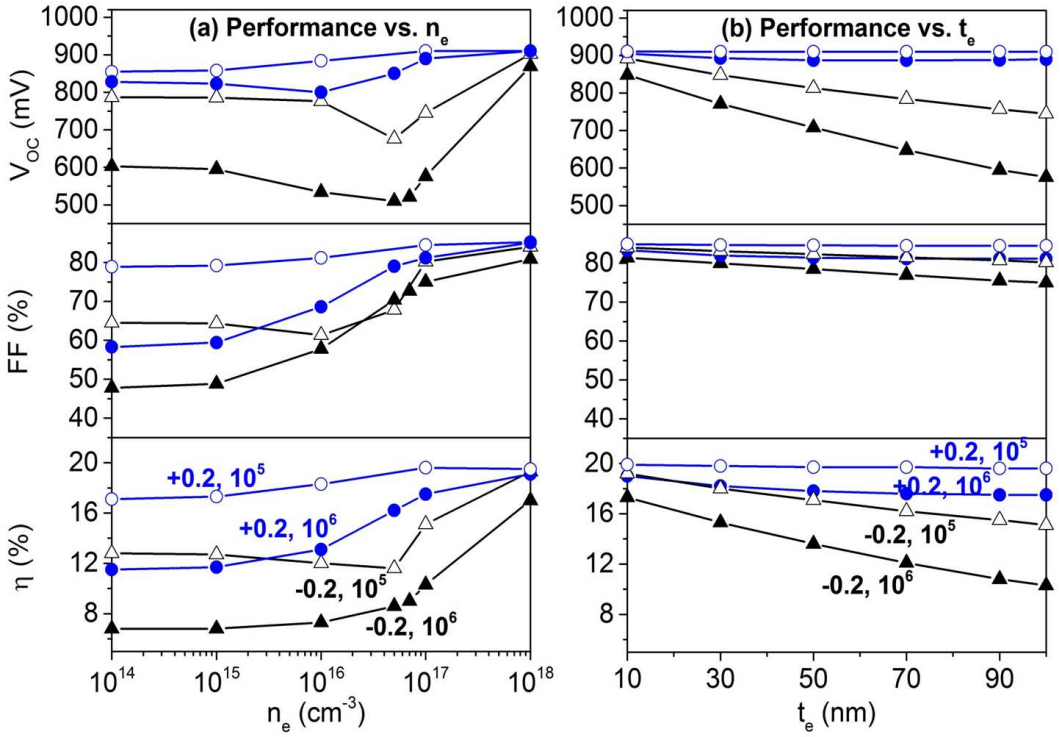

Figure 4.13: Calculated performance parameters for two values of ΔE_C and two of S_{IF} (curves labeled by ΔE_C first and S_{IF} second). (a) Variation in emitter doping (n_e), fixed 100-nm thickness. (b) Variation in emitter thickness (t_e), fixed emitter doping of 10^{17} cm^{-3}.

For a spike feature ($\Delta E_C = +0.2$ eV, Fig. 4.11b), the low emitter doping has a smaller impact on the absorber band bending, leading to a smaller R_{IF}. As a result, the V_{OC} is less affected at low emitter doping. However, for both ΔE_C cases, Fig. 4.13a shows a reduction of FF at low emitter doping since insufficient carrier collection will take place in the absorber layer with weak absorber band bending and hence low electric field. Therefore, a highly resistive emitter layer with low doping is a poor choice even though a conduction-band spike at the emitter/absorber interface can help maintain the cell voltage.

The emitter thickness is also important for the interfacial recombination process since it can limit the potential drop and affect the absorber band bending, particularly with a cliff offset [25]. Assuming an emitter doping of 10^{17} cm^{-3} and mid-gap interface defect states,

according to Eq.4.2, the interfacial recombination rate R_{IF} is now governed by the hole density at the interface. Fig. 4.12b shows the hole densities at the interface with varying the emitter thickness for the two ΔE_C cases. For ΔE_C = -0.2 eV, the band bending of the absorber surface is increasingly reduced with increasing the emitter thickness, corresponding to the increase in hole density in Fig. 4.12b. As a result, there will be a reduction of V_{OC} as shown in Fig. 4.13b. For a positive ΔE_C, however, the impact of emitter thickness on the absorber band bending is negligible. The combined message is that cells with a thin emitter, a high emitter doping, and a spike offset, can have high conversion efficiency even when S_{IF} is large; for thick or lightly-doped emitters, S_{IF} will degrade cell performance.

4.2.4 Defect Energy and Defect Type

The energy of the interfacial recombination states in the previous sections was implicitly assumed to take place at mid-gap with acceptor-type interface defect states, similar to other simulation studies [23, 25, 56, 57]. However, according to Eq.4.2, if $E_{d,IF}$ is located closer to one of the band edges, and hence n^* or p^* is large (see Section 4.2.1 for details), the recombination rate will be reduced, as shown in Fig. 4.14a. Furthermore, if interface defect states are donor-type rather than acceptor-type, they provide positive charges which enhance the absorber surface inversion (see Fig. 4.14b) and can partially mitigate the interfacial recombination. For a general picture of parameter dependence on defect energy, a cliff offset was chosen, since the cell performance is more sensitive to interface defects than with spike offset.

Fig. 4.14c shows the performance parameters as a function of $E_{d,IF}$ location for ΔE_C = -0.2 eV. This region labeled "efficient recombination" is centered near mid-gap and spans roughly half the bandgap. When $E_{d,IF}$ is close to either E_C or E_V, the cell performance is much less affected, and at all energies, acceptor-type interface defects produce a greater V_{OC} loss than donor-type defects as shown in Fig. 4.14c. J_{SC} and FF also decrease somewhat in the efficient recombination region on either side of mid-gap for both types of interface defects, but have a much smaller impact on efficiency than the voltage decreases. This is

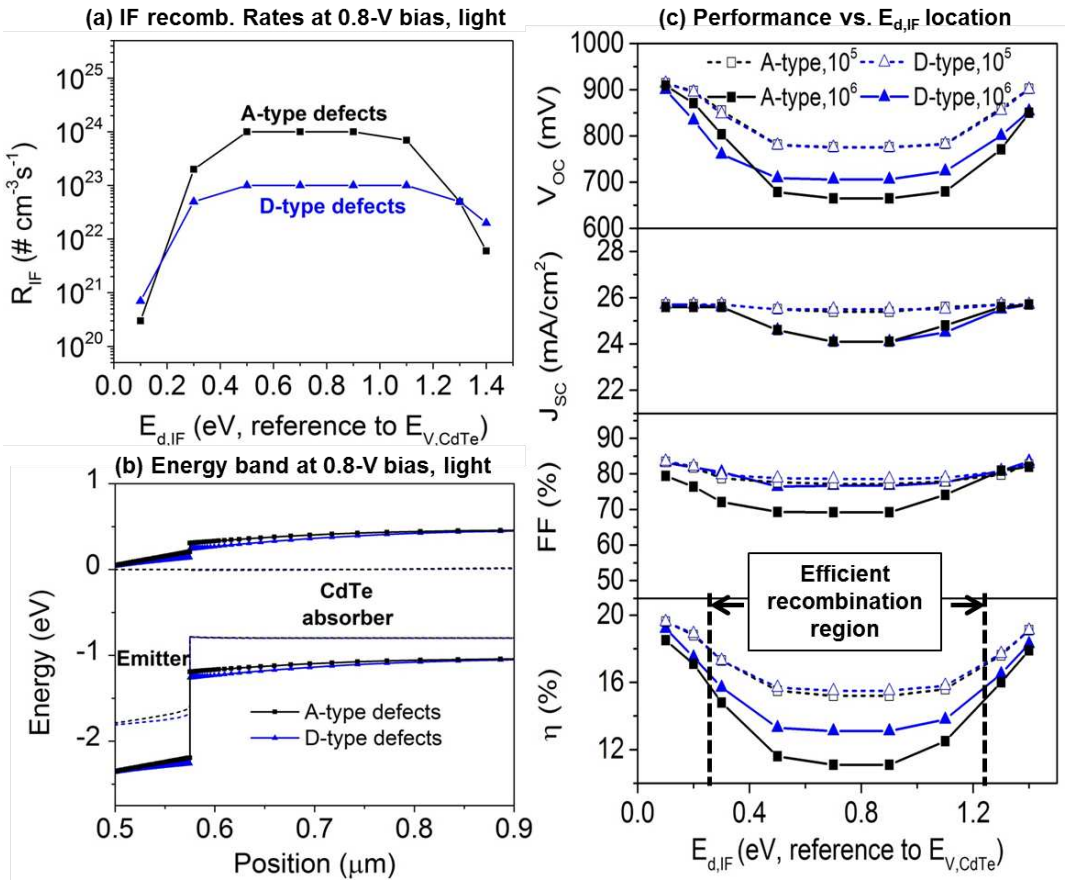

Figure 4.14: (a) The interfacial recombination rates R_{IF} at $S_{IF} = 10^6$ cm/s and (b) Energy band diagrams under illumination at 0.8-V bias for acceptor (A)- and donor (D)-type interface defects with ΔE_C = -0.2 eV; (c) Calculated performance with varying $E_{d,IF}$ locations for two values of S_{IF}.

because V_{OC} is more dependent on the diode current driven by voltage bias (See Section 2.1.3). The differences between the acceptor-type and donor-type defects in Fig. 4.14a-b are reflected in the calculated parameters in Fig. 4.14c.

4.2.5 Specific Emitters

This section will focus on specific emitter materials. Several n-type alloys with wide band gaps, such as CdS, (Cd,Mg)Te, Cd(S,O), and (Mg,Zn)O, should be suitable for high-efficiency CdTe solar cells due to their low optical absorption, especially for the latter two,

which have bandgaps above 3 eV [64, 65, 40]. The other considerations such as the band alignment and interfacial recombination, however, can also lead to large differences in cell performance.

Here, two representative emitters (CdS and (Mg,Zn)O) are compared to illustrate the roles of their emitter-absorber band alignment and interface defects on cell performance. CdS has a band gap of 2.4 eV and commonly forms a small cliff with CdTe (ΔE_C = -0.1 eV) [40, 66]. The band gap of (Mg,Zn)O (MZO) can be tuned by adjusting the Mg composition ratio. It varies with Mg fraction, $E_g(x) = 3.3+2.0x$ ($0 < x < 0.4$), where x = Mg/(Mg+Zn), with the expansion divided between the conduction and valence bands [67, 68, 69]. A band gap of 3.7 eV and ΔE_C of +0.2 eV with CdTe were chosen for simulation, corresponding to a 20% Mg fraction in MZO. Experimentally, CdTe cells with ~20% Mg in MZO emitter have shown very good performance [40]. Note that Cd(S,O) and CdMgTe also have a positive ΔE_C with CdTe and the band-offset is dependent on the oxygen and magnesium ratios, respectively [40, 70]. In terms of an electronic model, therefore, a similar analysis to that for MZO should be applicable for them as well.

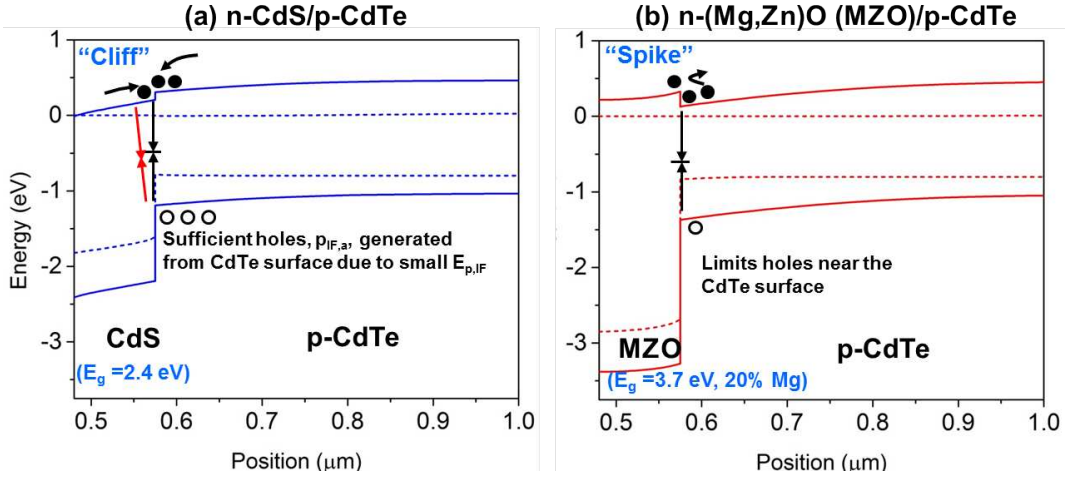

Figure 4.15: Energy band diagrams with two practical emitters: CdS ($E_g = 2.4$ eV, $\Delta E_C = -0.1$ eV) and MZO ($E_g = 3.7$ eV, $\Delta E_C = +0.2$ eV), at 0.8-V bias under illumination.

The negative cliff for CdS allows both the recombination at the CdTe surface and the cross-interfacial recombination between CdS and CdTe, as shown in Fig. 4.15(a). With such

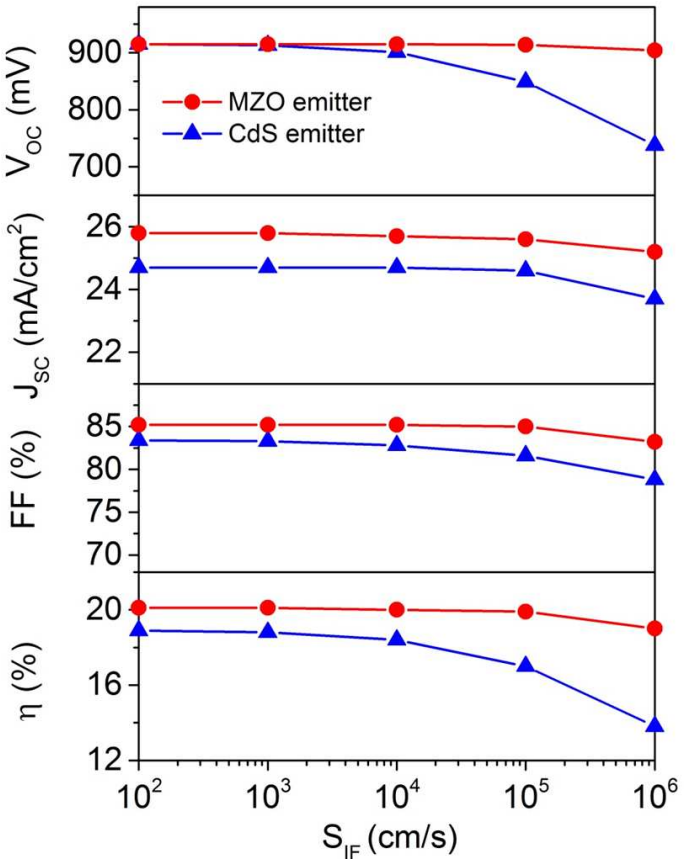

Figure 4.16: Calculated performance parameters as a function of S_{IF} with two practical emitters: CdS ($E_g = 2.4$ eV, $\Delta E_C = -0.1$ eV) and MZO ($E_g = 3.7$ eV, $\Delta E_C = +0.2$ eV).

a type-II band alignment, a small hole barrier $E_{p,IF}$ is formed, which generates sufficient free holes at the CdTe surface (similar to the band alignment in Fig. 4.8(a)). As a result, the electron-hole recombination increases significantly at large S_{IF} ($> 10^4$ cm/s). This increase leads to an increased forward diode current and thus decreased V_{OC} and FF as shown in Fig. 4.16

In contrast, the spike for the MZO/CdTe heterojunction impedes the cross-interfacial recombination. In Fig. 4.15(b), the positive ΔE_C forms a large hole barrier $E_{p,IF}$, which allows only limited holes for recombination (Fig. 4.8(b)). So even with a high density of interface defects ($S_{IF} > 10^4$ cm/s), large V_{OC} is maintained due to a suppressed interfacial recombination current. The FF is also slightly larger than the cell with CdS emitter because even in the absence of interfacial recombination, the bands will not flatten as quickly with

voltage for the spike. In addition, a larger J_{SC} is obtained with the MZO emitter because of its larger optical band gap and lower optical absorption.

A similar approach with the spike configuration at the emitter/absorber interface has been successfully applied in CIGS technology [56, 57], and the advantage with CdTe should be similar. Experimentally, the CdTe cells with 20% Mg in MZO emitters have demonstrated improvement of performance parameters. In our lab, the voltage is typically 860 mV with MZO compared to 800 mV with non-oxygenated CdS, and the current density for MZO is typically 26 mA/cm^2 compared to 22 mA/cm^2 for CdS [40]. These differences are similar to those seen in the calculations of Fig. 4.16. The current advantage comes from the larger band gap itself, but the voltage advantage arises from the band offset. More comparisons of a variety of emitters between experiment and simulation will be given in Chapter 5.

4.2.6 Summary

The impact of the emitter/absorber interface on CdTe cell performance results from (1) the conduction-band offset ΔE_C, (2) the emitter doping and thickness, and (3) the density and energy distribution of interface defects. A positive ΔE_C ("spike") is beneficial to the cell performance, since it can induce a large hole barrier that suppresses the interfacial recombination, but too large a spike is detrimental due to the impedance of the photocurrent transport. In a heterojunction device with many defects at the emitter/absorber interface (high S_{IF}), a thin and highly-doped emitter can induce strong absorber inversion and hence help maintain good cell performance. The charge types and energetic locations of interface defects will also influence the interfacial recombination. When acceptor-type interface defects are located near mid-gap, the performance loss is significantly larger than with defect energies nearer a band edge or with donor-type defects. In terms of specific emitter materials, the calculations suggest that the (Mg,Zn)O alloy with 20% Mg, or a similar type-I heterojunction partner with moderate ΔE_C (e.g., Cd(S,O) and (Cd,Mg)Te with appropriate oxygen or magnesium ratios) should be advantageous for the emitter choice.

4.3 Substrate Choices for Monocrystalline CdTe Devices

Epitaxial monocrystalline CdTe has been shown by others to have a radiative recombination rate approaching unity, high carrier concentration, and low defect density [35]. It has therefore become an attractive candidate for high-efficiency solar cells, with a potential to be competitive with GaAs. The choice of substrate is a key design feature for epitaxial CdTe solar cells, and several possibilities (CdTe, Si, GaAs, and InSb) have been investigated by others [33, 34, 35] and considerable experimental information has been accrued. For polycrystalline CdTe cells, the growth surface is less critical, but will have some impact on the quality of the CdTe absorber. This section is intended to provide additional insights on the epitaxial substrate through numerical simulation.

4.3.1 Review

To understand the material limitations of CdTe cells, mono-CdTe structures with high-purity and well-controlled parameters have been grown by molecular-beam epitaxy (MBE). High minority carrier lifetimes ($>$ 200 ns) and radiative efficiency approaching unity (indicates radiative recombination dominates in the CdTe material rather than non-radiative SRH recombination), were recently reported by researchers from Arizona State and Texas State Universities [24, 35] on CdTe/CdMgTe double heterostructures grown by MBE on InSb substrates. Nevertheless, a major challenge for successful fabrication of epitaxial CdTe solar cells is having a suitable substrate for the deposition of the cells. Four crystalline substrates, Si [34], InSb [35], CdTe [32], and GaAs [33], have been employed to grow the epitaxial CdTe solar cells by different research groups. However, efforts to understand the mechanisms involved with each substrate have been limited. A comprehensive mono-CdTe model system with specific consideration of substrate choices is, therefore, instructional to provide guidance for the future fabrication of high-efficiency CdTe solar cells. This section explores practical problems of the four substrate candidates (Si, GaAs, InSb, and CdTe) using detailed numerical simulations, and then focuses more specifically on InSb since it was

proved effective with impressive V_{OC} ($\sim 1.1V$) [35]. In particular, it proposes three strategies to overcome the valence-band offset between InSb and CdTe.

4.3.2 Baseline Model

The superstrate configuration usually used for poly-CdTe devices cannot be easily translated into epitaxial-grown mono CdTe cells, so a substrate device structure is assumed for epitaxial CdTe, as shown in Fig 4.17. Numerical simulations in this section were performed with the TCAD device simulator Sentaurus Device by Synopsys [53] since finer device "meshing" techniques and advanced features such as the incorporation of tunnel diodes are needed later. The simulated cell features an Al-doped ZnO layer for its front contact, a CdTe homojunction for the collection of photons, and an 800-μm substrate for the growth of epitaxial

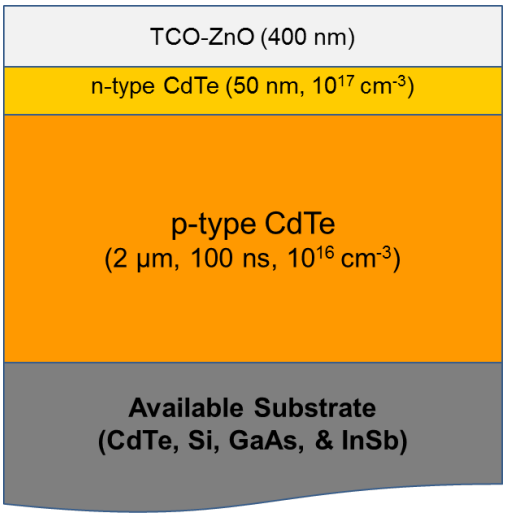

Figure 4.17: Baseline device structure used in the numerical simulations of Section 4.3.

CdTe. The CdTe carrier density is 10^{17} cm^{-3} for the n-type emitter, and 10^{16} cm^{-3} for the p-type absorber, respectively. Radiative and Shockley-Read-Hall recombination are included in the model, while Auger recombination is assumed to be negligible and therefore not included. The baseline minority carrier lifetime is 100 ns and the CdTe radiative recombination coefficient, $B_{rad} = 1 \times 10^{-10}$ $cm^3 s^{-1}$ [24]. Other material parameters in the simulations were taken from Table 3.2.

The baseline epitaxial-CdTe PV-device design assumes an ideal substrate without band-alignment, interfacial-trap, or series-resistance issues. A comprehensive comparison of the available substrates will be examined in detail later. Fig. 4.18a shows the calculated energy-band diagram with an ideal substrate (baseline), at 0.8-V bias and under illumination (close to V_{OC}); Fig. 4.18b shows the corresponding dark and light current-voltage (J-V) curves. With higher carrier density ($p = 10^{16}\ cm^{-3}$) and minority carrier lifetime ($\tau = 100$ ns), the calculated V_{OC} for epitaxial CdTe device should be approximately 100 mV greater than traditional poly-CdTe ($p \sim 10^{14}\ cm^{-3}$, $\tau \sim 10$ ns) [15, 38]. The calculated band diagram and J-V curves shown in Fig. 4.18 assume a device architecture without advanced features, such as a back-surface field (BSF) to mitigate back surface recombination. In addition, material limitations of the substrate were not considered.

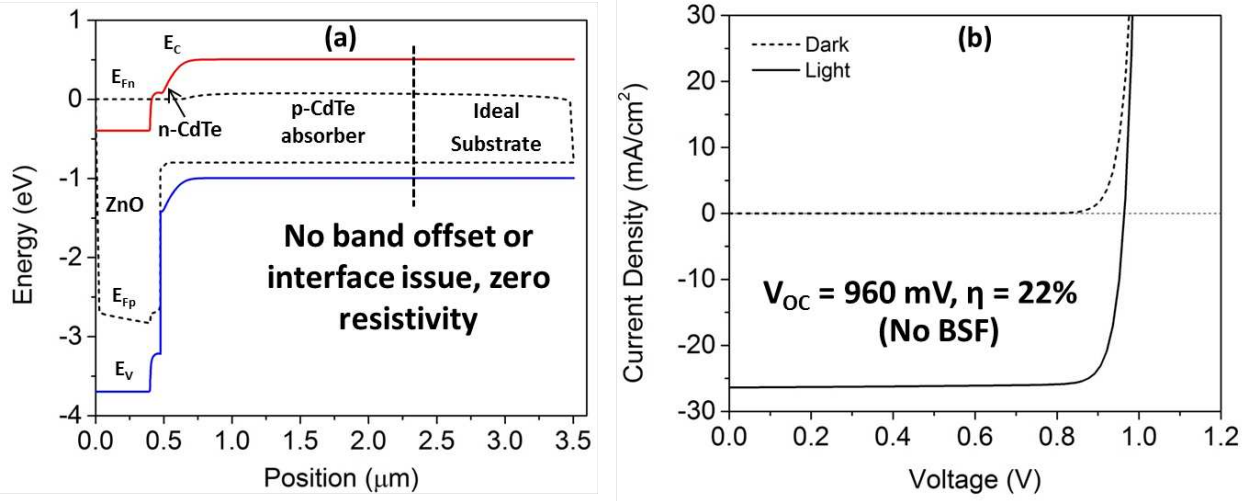

Figure 4.18: (a) Energy-band diagrams with ideal substrate (baseline) at 0.8 V under illumination; (b) calculated J-V curves with an ideal substrate and no BSF included.

4.3.3 Comparison of Substrate Materials

In reality, the growth of epitaxial layers on a substrate creates a non-ideal interface caused by lattice mismatch and/or non-ideal band alignment between absorber and substrate. In

addition, the substrate itself may introduce parasitic effects such as series resistance and non-ohmic contact. Therefore, an appropriate substrate choice is crucial for epitaxial CdTe solar cells to achieve high efficiency. It is known that the GaAs technology achieves high conversion efficiency partially due to the high material quality of a GaAs (or Ge) substrate and the well-controlled interfacial recombination between the main junction and the substrate [71, 72, 73].

Table 4.1: Materials comparison for commercially-available CdTe[74], Si[75], GaAs[76], and InSb[76, 77] substrates.

Substrate	a (Å)	E_g (eV)	χ (eV)	carrier density (cm^{-3})	μ_h (cm^2/Vs)	Resistivity ρ ($\Omega \cdot cm$)
CdTe	6.48	1.50	4.30	$\sim 2 \times 10^{15}$	50	62.5
Si	5.43	1.12	4.05	$\sim 10^{16}$	400	1.5
GaAs	5.65	1.42	4.07	$\sim 10^{17}$	400	0.1
InSb	6.48	0.17	4.60	$\sim 10^{16-20}$	850	10^{-3}

Table 4.1 compares the material properties of four substrates (Si, GaAs, InSb, and CdTe). Choosing CdTe for the substrate avoids the lattice mismatch problem, and InSb very nearly avoid it since CdTe and InSb have nearly identical lattice constants (∼6.48Å), and thus CdTe should grow on an InSb or CdTe substrate without creating significant interfacial traps. A large lattice mismatch of 19% between CdTe and Si (or 14% lattice mismatch between CdTe and GaAs), however, is likely to cause dislocations at the interface and generate a substantial number of electronic defects. Compared with the negligible resistivity of the other three substrates, the available CdTe substrates have an excessive resistivity due to low doping concentration and low hole mobility. Thus their large series resistance will significantly reduce the cells fill factor. Furthermore, it is challenging to find an appropriate back metal

contact for p-CdTe substrate with a large work function to match the valence band of CdTe.

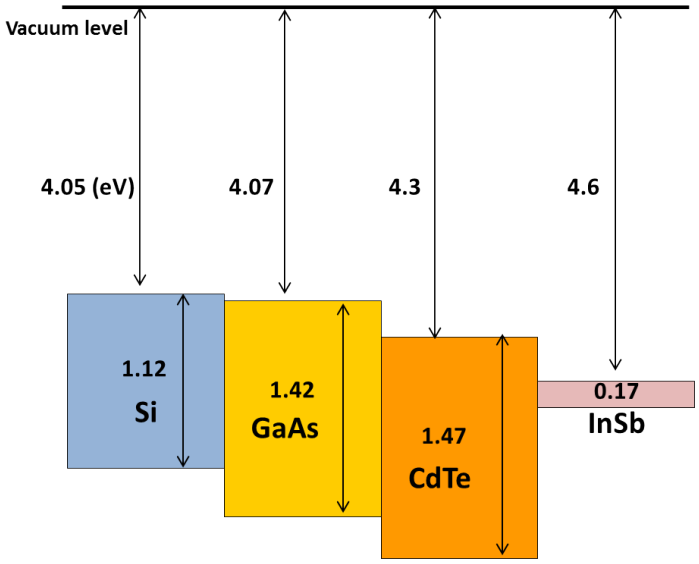

Figure 4.19: Band alignment for Si, GaAs, CdTe, and InSb. The valence-band offset $\Delta E_V =$ 0.3 eV between GaAs and CdTe; $\Delta E_V = 0.6$ eV between Si and CdTe; $\Delta E_V = 1.0$ eV between InSb and CdTe

In terms of electronic properties, InSb should serve as the preferred substrate material. However, there exists a band alignment problem between CdTe absorber and InSb substrate. Fig. 4.19 shows the natural band alignment of Si, GaAs, CdTe, and InSb [74, 75, 76, 77]. As opposed to a CdTe substrate where band alignment is non-issue, a heterointerface between an InSb (or Si, GaAs) substrate and a p-type CdTe absorber creates a large valence-band offset due to band gap plus electron affinity (χ) difference. The resulting valence-band barrier will impede hole transport and cause severe carrier recombination (note that if InSb substrate connects to an n-type CdTe absorber, the valence-band barrier would be much less of an obstacle). Next, we use numerical simulations to investigate how the material limitations for each substrate affect the cell performance. We present only simulation results for Si, but they should be applicable for GaAs since they have similar lattice-mismatch and valence-band offset issues.

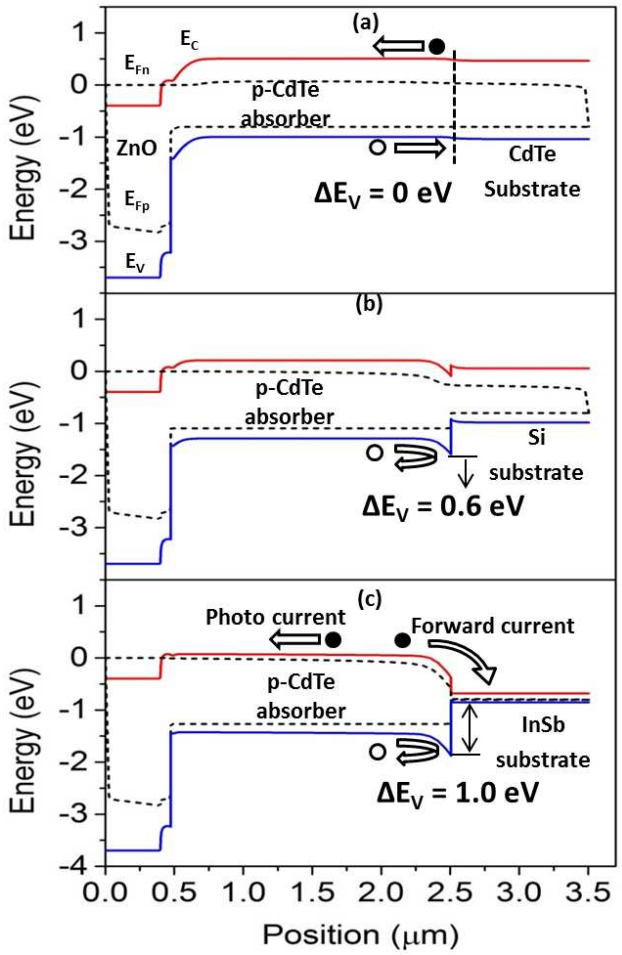

Figure 4.20: Energy-band diagrams at 0.8-V bias under illumination for a PV device with CdTe, Si, and InSb substrates. The solid and open circles represent the electrons and holes, respectively, and the arrows represent the direction of carrier flow.

Fig. 4.20 shows the energy-band diagrams of the three substrates (CdTe, Si, and InSb) under 1-sun illumination and at 0.8-V forward bias. The CdTe substrate has a continuous band alignment with the CdTe absorber and hence should generate the largest V_{OC} (∼960 mV, see Table 4.2). However, the high resistivity of CdTe (see Table 4.1) produces a large series resistance with a 800-μm thick wafer ($R_S \approx 5\Omega \cdot cm^2$) compared to the negligible resistance of Si and InSb. As a result, the large R_S compromises the fill factor for the CdTe substrate choice. To date, it has proven difficult to either reduce the wafer thickness or increase the wafer doping density to lower the series resistance of CdTe substrate [78]. Thus,

even though CdTe substrate has no band alignment or lattice mismatch problem, it does not appear to be a straightforward substrate for growing epitaxial CdTe cells.

For both Si and InSb substrates, there is a large valence-band offset ($\Delta E_V = 0.6$ eV for Si and $\Delta E_V = 1.0$ eV for InSb) which can seriously impede the transport of photo-generated holes and thus enhance the hole recombination. In addition, as shown in the band diagram with the InSb substrate in Fig. 4.20c, the severe conduction-band bending caused by the electron-affinity differences between the two materials allows a large forward current to flow to the back surface. The distance between the conduction-band energy E_C and electron quasi-Fermi level E_{Fn} is much narrower than with a Si or CdTe substrate, and it enhances the forward electron current [79]. Overall, without an enhancement layer, the calculated V_{OC} for InSb (380 mV) are much lower compared with the V_{OC} with CdTe substrate (∼960 mV), as shown in Table 4.2.

Table 4.2: Calculated cell performance with CdTe, Si, and InSb substrates.

Substrate	$p_{sub}(cm^{-3})$	$R_S(\Omega \cdot cm^2)$	$V_{OC}(mV)$	$J_{SC}(mA/cm^2)$	$FF(\%)$	$\eta(\%)$
Baseline	1×10^{16}	0	960	26.4	86.2	21.9
CdTe	2×10^{15}	5	960	26.3	74.0	18.8
Si	1×10^{16}	0.1	700	25.9	83.2	15.1
InSb	1×10^{18}	0	380	28.7	75.2	7.3

4.3.4 Enhancement Layers to Improve V_{OC} with InSb Substrate

InSb remains a favorable substrate choice because of its excellent lattice match and negligible resistivity, but has the unfavorable energy-band alignment with the CdTe absorber. In addition, the conduction-band bending may enhance severe back surface recombination (Fig. 4.20c). It should be helpful to raise the conduction band or add a BSF at the CdTe/InSb interface to effectively reflect electrons away from the back contact. A BSF layer can be

created either by heavy doping or by alloying with elements that would expand the band gap. On the other hand, the large valence-band barrier caused by chemical potential difference blocks the photo-generated holes. To assist hole transport, a highly-doped thin buffer layer at the CdTe/InSb interface could narrow the valence-band barrier and thus allow holes to tunnel across the interface. In this section, three enhancement features are proposed to overcome the V_{OC} limitations imposed by usage of InSb substrate and thus create an opportunity for the epitaxial CdTe device to achieve better performance. The strategies described should be applicable for other substrates as well.

Highly-doped CdTe Buffer Layer

Insertion of a highly-doped (p^{++}) CdTe buffer layer between the CdTe absorber and InSb substrate can reduce the recombination of the diffused electrons caused by severe conduction-band bending at this interface and thus mitigate the large forward electron current. Here it will be referred to as a CdTe buffer layer. This kind of buffer layer is often referred to as a back-surface field (BSF) for Si-based solar cells [55] or an electron reflector for polycrystalline CdTe solar cells [80].

Fig. 4.21a shows the simulated band diagram with a 20-nm thick CdTe buffer at 0.8-V bias under illumination. The conduction-band energy (E_C) near the interface is gradually raised as the carrier density of the buffer layer (p_{buffer}) is increased, as shown in Fig. 4.21a. An effective electron reflector forms with p_{buffer} above 10^{18} cm^{-3}, which can reflect electrons away from the back surface and mitigate the back surface recombination. Meanwhile, with increasing p_{buffer}, the valence-band energy (E_V) of CdTe buffer is lifted near the interface to approach the E_V of InSb. Thus, a thinner valence-band barrier is formed to allow the holes to tunnel across the interface.

As a result, in Fig. 4.21b, V_{OC} is enhanced significantly with increased p_{buffer} due to electron reflection and better hole transport near the interface. In addition, the highly-doped CdTe buffer improves the collection of long-wavelength photons, so a small J_{SC} enhancement is also observed in the short-dash (10^{19} cm^{-3}) and dotted (10^{20} cm^{-3}) J-V curves in

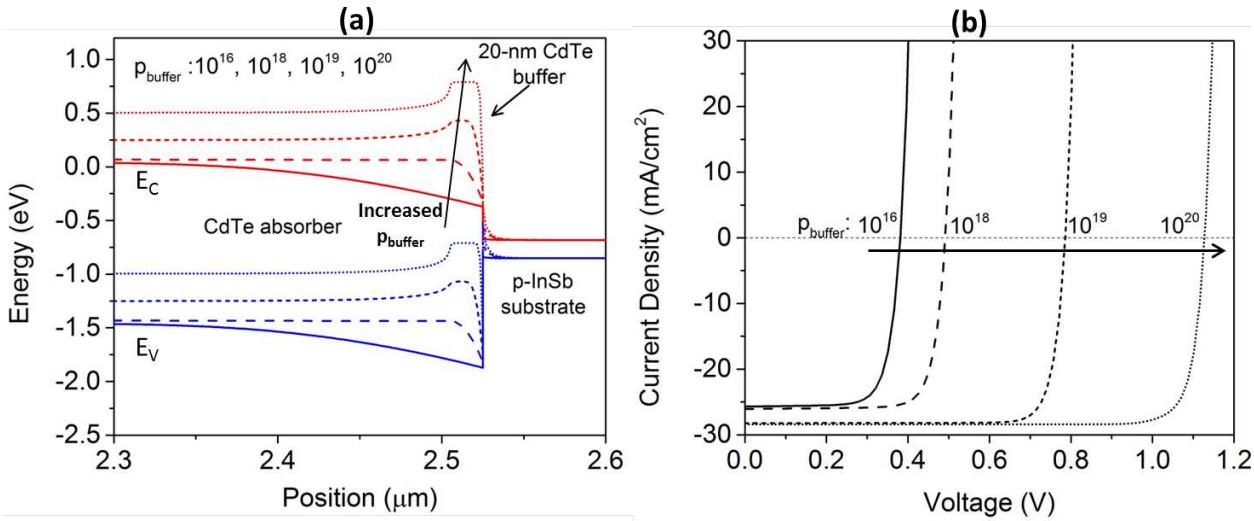

Figure 4.21: (a) Conduction and valence bands of an epitaxial CdTe cell with a 20-nm CdTe buffer layer at 0.8-V bias under illumination, zoomed at the back to emphasize the impact of the CdTe buffer. p_{buffer} varied from 10^{16} to 10^{20} cm^{-3}; (b) Corresponding J-V curves.

Fig. 4.21b. Note that, it is extremely difficult to obtain a heavily-doped CdTe buffer with $p_{buffer} = 10^{20}$ cm^{-3}, which means the effectiveness of a highly-doped CdTe buffer by itself is likely to be limited. Both thermodynamic simulations [81] and experimental characterizations [82] have suggested that the highest doping for p-type CdTe material is pinned to $\sim$ 1-5$\times 10^{18}$ cm^{-3}. While highly doped CdTe buffers ($10^{19} - 10^{20}$) promise significant Voc increases, the maximum achievable p-type doping is in a 10^{18} range. A CdTe buffer layer doped on the order of 10^{18} can improve the Voc for $\sim$ 120 mV (see Fig. 4.21b).

Expanded-Band-gap Buffer Layer

Adding a higher band gap buffer layer to act as an electron reflector can be more effective than a highly-doped CdTe buffer, since the expanded band gap can create an abrupt barrier in the conduction band while the barrier height remains constant with external bias. Alloying CdTe with Mg and Zn to form CdZnTe (CZT) or CdMgTe (CMT) could serve this purpose. The CZT and CMT band gaps can be tuned by adjusting the composition ratios. For CZT, the band gap varies as $E_g(x) = 1.47 + 0.45x + 0.30x^2$ [74], where x is the Zn/(Cd+Zn) ratio.

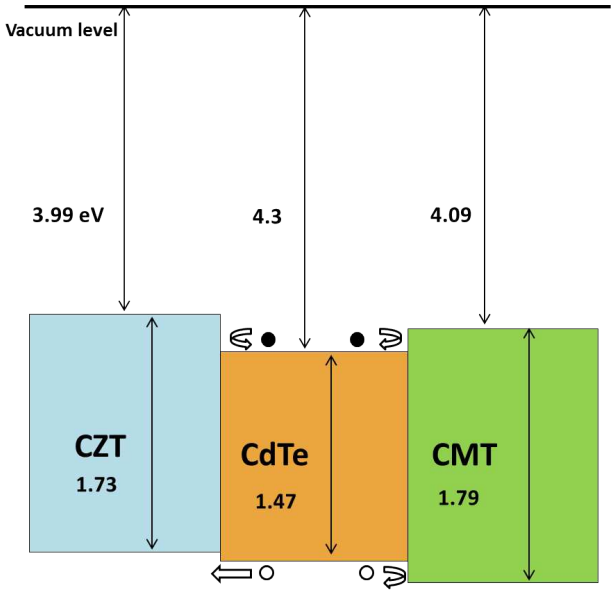

Figure 4.22: Band alignment of CdTe, CZT (40%Zn), and CMT (20%Mg).

The band gap range is from 1.47 to 2.25 eV, and most of the expansion is in the conduction band. For CMT, the band gap variation with Mg fraction is $E_g(x) = 1.47+1.35x+0.55x^2$ [74], where the band gap range is from 1.47 eV to 3.4 eV, and the expansion happens in both the conduction and valence bands. The electron affinities χ of CdTe, ZnTe, and MgTe have been reported as 4.3eV, 3.53 eV, and 3.25 eV, respectively [83, 84, 85], and for current purposes we assume a linear dependence of electron affinity on Zn or Mg fraction. Fig. 4.22 shows the natural band alignment of CdTe, $Cd_{0.6}Zn_{0.4}Te$, and $Cd_{0.8}Mg_{0.2}Te$. CdTe/CZT forms a type II heterojunction, creating a positive conduction-band barrier to reflect photo-generated electrons and a negative valence-band offset to assist hole transport; however, CdTe/CMT forms a type I heterojunction, where there is electron reflection, but the positive valence-band barrier can at least partially impede the hole current from the p-type CdTe absorber (Note that the impedance of hole transport would not be a problem for n-type CdTe absorber and could be less of an issue for a much thinner CMT buffer due to the tunneling-assisted transport). However, the CZT alloy should be a better choice for p-type CdTe from the band-alignment considerations.

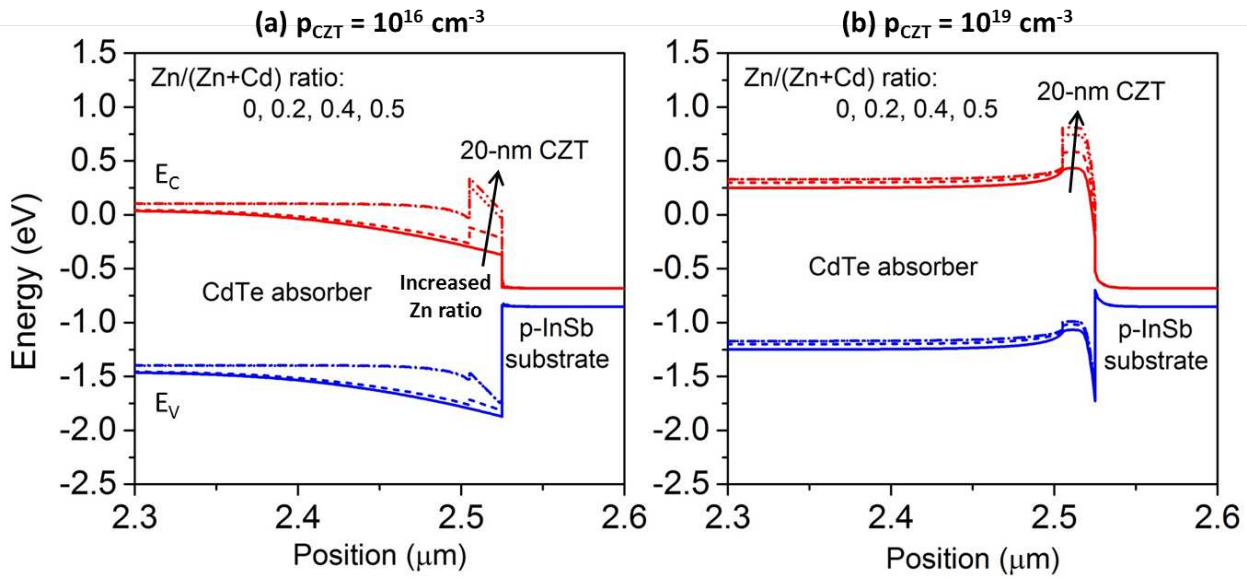

Figure 4.23: Energy-band diagram under illumination, 0.8-V bias, with a 20-nm expanded-band-gap CdZnTe layer, at (a) $p_{CZT} = 10^{16}$ and (b) 10^{19} cm^{-3}.

Next, the combined impact of alloying and high carrier density in the CZT buffer is examined in Fig. 4.23, which shows the conduction and valence bands with varying Zn/(Zn+Cd) ratio (0, 0.2, 0.4, and 0.5) in a 20-nm-thick CZT buffer with carrier densities of 10^{16} and 10^{19} cm^{-3} and under illumination and 0.8-V bias. In Fig. 4.23a, with $p_{buffer} = 10^{16}$ cm^{-3} and a 20% Zn/(Zn+Cd) ratio, the electron reflector due to the expanded gap is marginal because of the severe conduction-band bending, and the curved region near the interface forms a potential well that can trap electrons.

Additionally, there is only a small valence-band modification with increasing Zn ratio. Hence with lower carrier-density CZT, there is only a slight V_{OC} improvement with increased Zn ratio, as shown in Fig. 4.24a. In comparison, higher carrier density, $p_{buffer} = 10^{19}$ cm^{-3} (Fig. 4.23b), forms a more effective electron reflector in the conduction band, and the valence-band barrier narrows to assist hole tunneling across the interface. Therefore, as shown in Fig. 4.24b, V_{OC} should increase significantly with the addition of a thin CZT buffer layer. Note that the rollover of J-V curves at the highest voltage is due to the suppression of forward current if there is an excessive conduction-band offset at CZT/InSb interface.

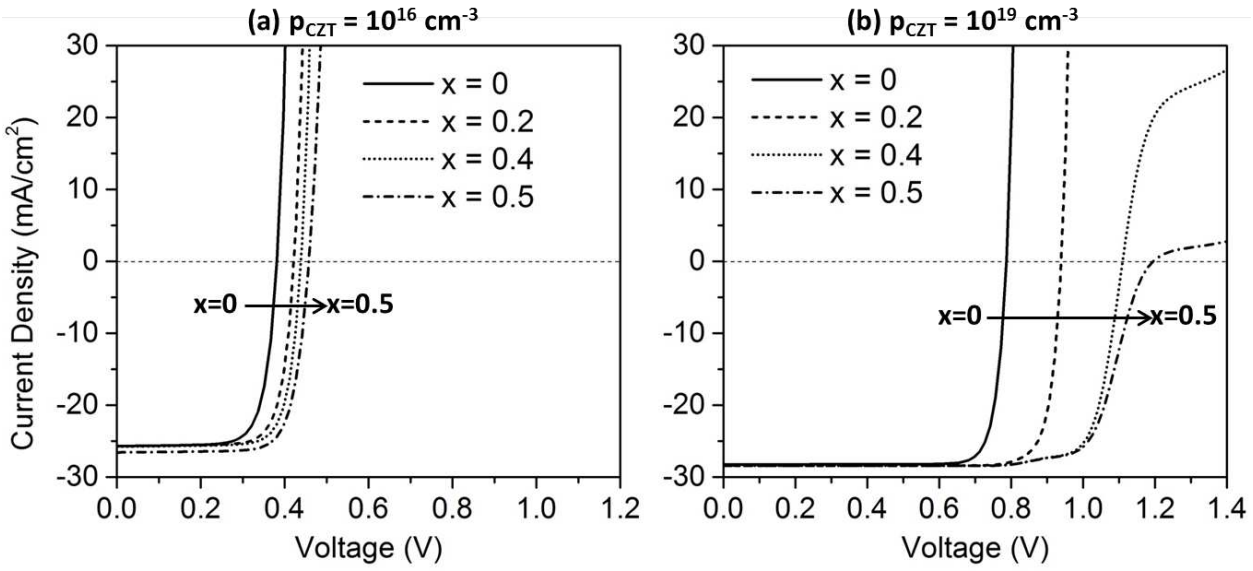

Figure 4.24: Calculated light J-V curves with a 20-nm CdZnTe buffer layer, varying Zn ratio, at (a) $p_{CZT} = 10^{16}$ and (b) 10^{19} cm^{-3}.

Additionally, there is some lattice mismatch between CdTe and CZT, which may cause interfacial recombination. The simulations, however, show that the cell performance has little variation when the interfacial recombination velocity S_{IF} is below 10^3 cm/s though large S_{IF} values can compromise the cell performance.

Incorporation of an InSb Tunnel Diode

The third modification considered here is the incorporation of an InSb tunnel diode (TD) to possibly mitigate the unfavorable band alignment issue. The InSb TD [86, 87], considered consists of a simple p-n junction in which both n and p sides are degenerate and there is a sharp transition between them, as shown in Fig. 4.25. For the InSb tunnel-diode simulation, a nonlocal direct band-to-band tunneling model was employed to better simulate the true carrier transport through the barrier [88]. With small forward bias, the electrons in conduction band on the n-side of the diode can tunnel through the band gap to the valence band on the p-side and recombine with the holes to produce the tunneling current. Fig. 4.25b shows the corresponding J-V curves of the InSb TD with effective masses $m_c = 0.014\ m_0$

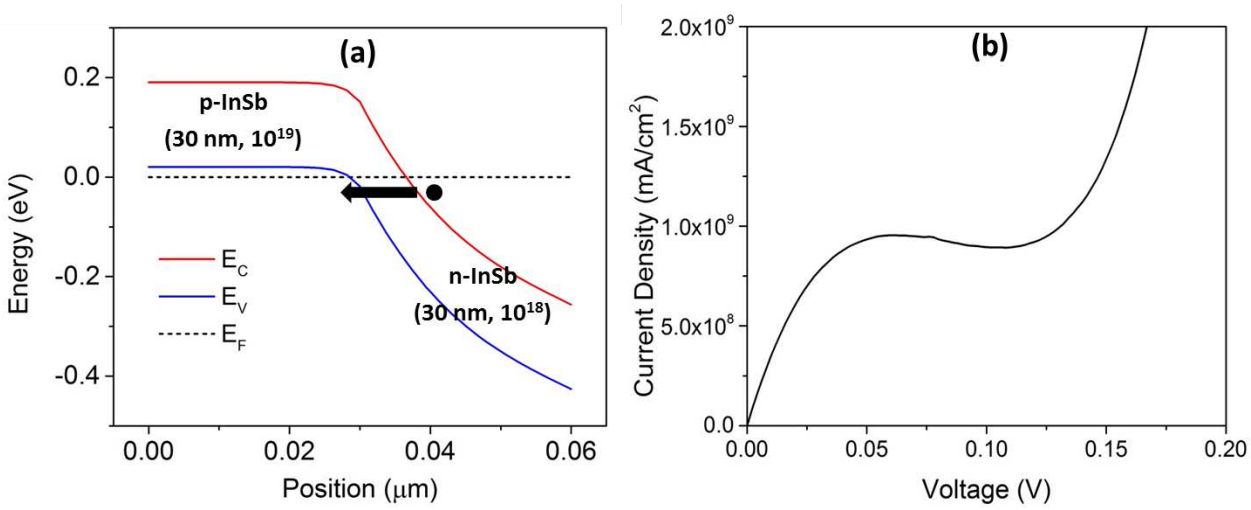

Figure 4.25: (a) Energy-band diagram of an InSb tunnel diode at equilibrium, consisting of 30-nm, 10^{19} cm^{-3} p-InSb and 30-nm, 10^{18} cm^{-3} n-InSb layers; (b) calculated J-V curves of the InSb tunnel diode.

and $m_v = 0.4\ m_0$ [77]. Because of its very narrow band gap, an InSb TD will have a very large current response even at small bias. This indicates there should be little voltage drop for photocurrent transport in solar cells.

When an InSb TD is inserted before a p-CdTe absorber, the n-side of the InSb TD contacts the n-InSb substrate to smooth the carrier flow, in contrast with the p-substrate in previous two approaches. Fig. 4.26a shows the energy-band diagram of a baseline cell with and without the InSb TD (Solid lines represent the bands with TD and dashed lines without TD). It is seen that both the conduction and valence bands shift slightly upwards with TD, indicating a small mitigation of the band bending. Therefore, in Fig. 4.26b, all the J-V curves with TD (solid lines) show a small degree of V_{OC} improvement. The combination of a thin CZT buffer (40%Zn, 10^{19} cm^{-3}) and an InSb TD yields a calculated conversion efficiency of 27.4%, the highest of any of the cases considered. Therefore, a combination of enhancement layers is likely to improve cell performance more than applying any of the individual layers.

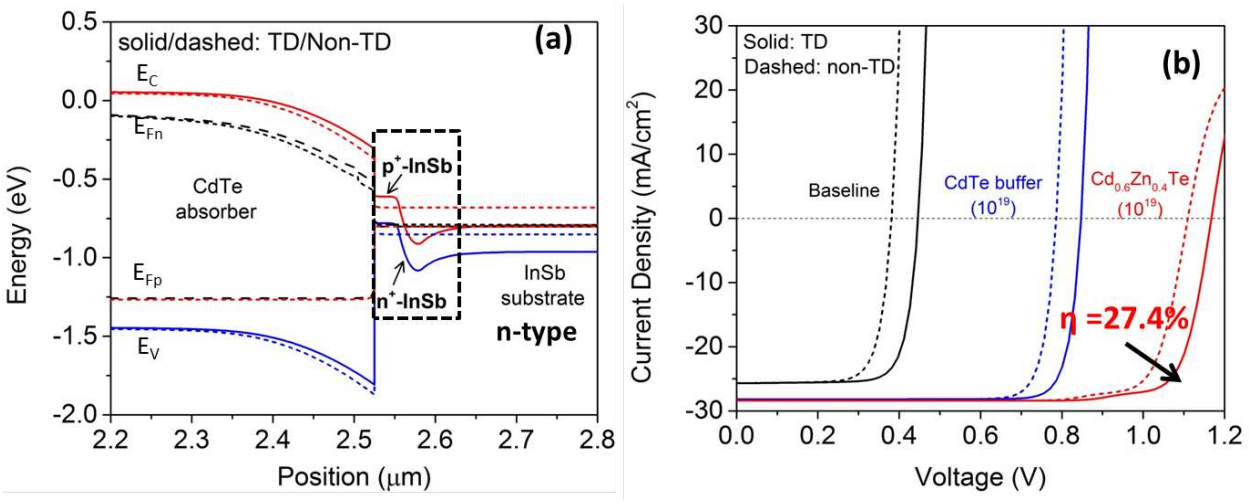

Figure 4.26: (a) Energy-band diagram at 0.8-V bias under illumination, with (solid) and without (dashed) an InSb TD; (b) calculated light J-V curves with and without an InSb TD for the baseline case and adding 20-nm, 10^{19} cm^{-3} CdTe and CdZnTe(40% Zn) buffer.

4.3.5 Summary

Several materials have been considered as the crystalline substrate for epitaxial CdTe solar cells. Each has its advantages and disadvantages. Available CdTe substrates have excessive series resistance; however, Si and GaAs have a large lattice mismatch with a CdTe absorber, and Si, GaAs, and InSb substrates all have issues with band offsets, which impede the flow of holes and allow excessive forward current. To address the unfavorable band alignment for InSb substrate, three enhancement strategies were considered: a highly-doped CdTe buffer, an expanded-band-gap layer, and the application of an InSb TD. Table 4.3 summarizes how these approaches affect CdTe cell performance. A highly-doped CdTe buffer can play a role in both reflecting electrons and assisting holes; however, its effectiveness is likely to be limited due to the difficulty in achieving heavy doping. Since a CZT buffer has an expanded band gap in the conduction band, it can more easily form an electron reflector and thus can improve the cell performance more effectively. The incorporation of an InSb TD adds a small additional mitigation of the band bending and should produce a slightly better V_{OC}. Over all, each approach has different degrees of performance improvement; however, a

Table 4.3: Effectiveness comparison of the three performance strategies.

Approaches	V_{OC} Improvement	
	Degree	Supplement Explanation
Highly doped CdTe buffer	++	Both reflects electrons and assists hole transport
Expanded-E_g Buffer	+++	More effective than highly-doped CdTe
Application of InSb TD	+	Modest help with the mitigation of E_C and E_V barriers

combination of the approaches is advised for the highest efficiencies. In addition, it is noted that CdTe cells with an n-type CdTe absorber might be another solution to the negative effect of the valence-band barrier and is also worthy of investigation.

4.4 Roles of Back Contact for Thin Film Poly-CdTe Devices

Since CdTe is a large-E_g ($\sim$ 1.5 eV) semiconductor with a high electron affinity (χ = 4.3 eV), most metals do not have a sufficiently high work function, and hence there is a tendency to form a carrier-blocking Schottky barrier ϕ_b at the p-CdTe/metal contact interface (see Fig. 3.3(b,c) in Section 3.2.2). To investigate this detrimental effect on the CdTe cells, a detailed study with numerical simulation is performed in this section with a focus on the thin film poly-CdTe cells, though the back contact situation is similar to the epitaxial mono-CdTe cells discussed above.

4.4.1 Review

It has proven to be challenging to achieve an ohmic back contact for either mono- or polycrystalline p-type CdTe solar cells. Therefore, instead of directly employing a metal as

the back contact, an additional buffer layer adjacent to CdTe absorber has been created to mitigate the carrier blockage due to the large back-contact barrier ϕ_b between poly-CdTe and metallic contact. As summarized in Table 2.1, the buffer contact layer is often formed by surface modification (e.g., etching the back CdTe to form a Te-rich surface, and copper doping such as CuCl treatment to highly dope the back CdTe surface), or by deposition of additional layer, such as Te or Cu_xTe (an overview of back contact materials can be found in Ref. [13]). However, most previous modeling work only emphasized on the metallic contact, simplifying the CdTe/metal as a Schottky diode with opposite polarity to the primary junction [28, 29]. This section is intended to give a systematical study to identify the roles of both the buffer and the metallic back contacts through extending the work by J. Pan et al. [79].

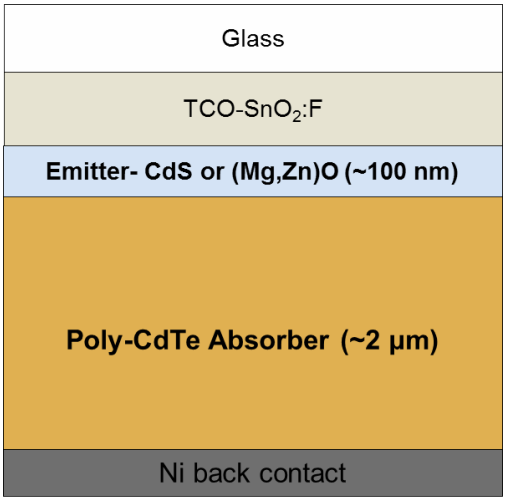

Figure 4.27: Baseline device structure used in the numerical simulations of Section 4.4.

Numerical simulation in this section was performed with SCAPS-1D software. The baseline CdTe device is assumed to have a superstrate configuration for the poly-CdTe solar cells, as shown in Fig. 4.27. The basic structure consist of a 200-nm-thick highly-doped TCO layer, a 100-nm-thick CdS emitter ($n = 10^{17}\ cm^{-3}$), and a 2-μm-thick CdTe absorber with $\tau = 1$ ns to reflect the typical minority carrier lifetime of the poly-CdTe absorber. Two reasonable values of hole densities for poly-CdTe are chosen to represent the fully and non-fully depleted junctions (the zero-voltage depletion width $W_d \approx 3\ \mu m$ for $p = 1 \times 10^{14}\ cm^{-3}$, and $W_d \approx 1$

μm for $p = 1 \times 10^{15}\ cm^{-3}$). The metal work function ϕ_M is varied from 5.0 eV to 5.6 eV. Several buffer contact layers are discussed case by case later.

4.4.2 Role of Metallic Back Contact

For CdTe with a low minority carrier lifetime ($\tau < 0.1$ ns), the presence of a large back barrier ϕ_b can impede hole transport and thus induce the current-limiting effect, "rollover", which is reasonably explained with a two-diode model [28, 29]. However, this phenomenon

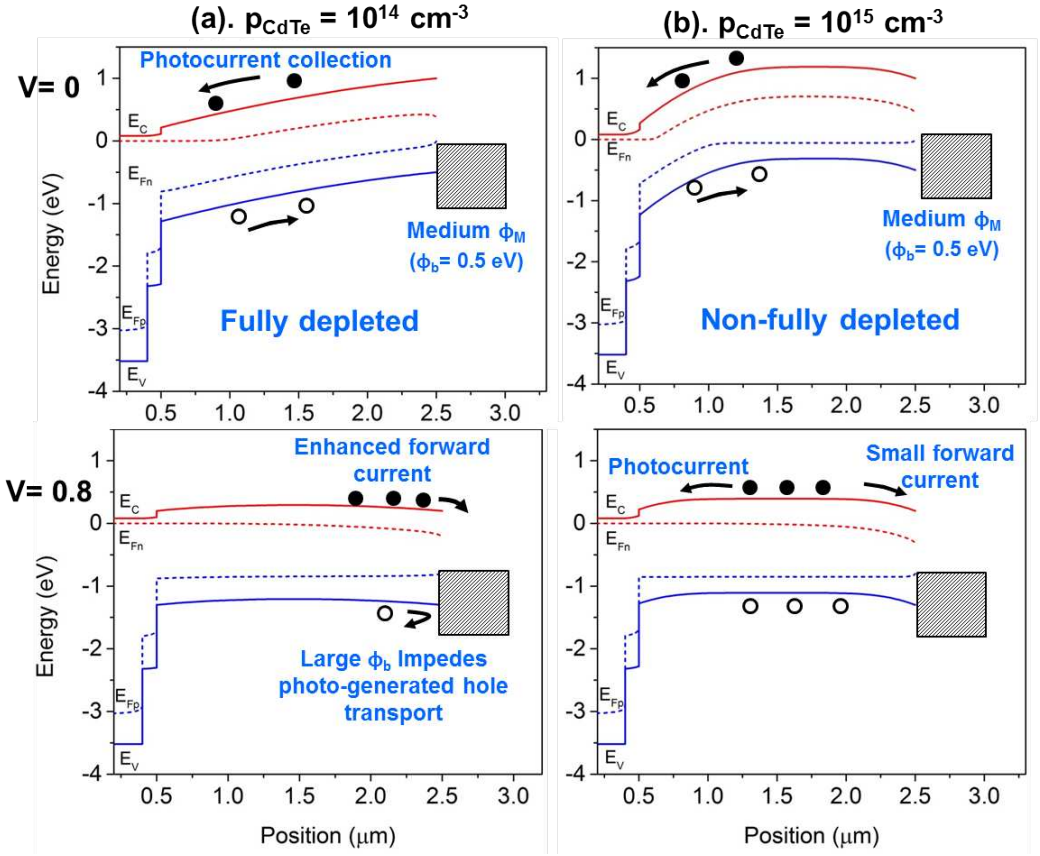

Figure 4.28: Energy-band diagram of CdTe solar cell at both 0-V (top) and 0.8-V (bottom) bias under illumination, with two values of hole densities in CdTe absorber: (a) $10^{14}\ cm^{-3}$ and (b) $10^{15}\ cm^{-3}$.

does not take place in higher-efficiency CdTe cells with larger τ (> 0.5 ns) at room temperature [79]. Since this work is focused on high-efficiency CdTe devices, greater effort was made

to study other impacts of the metallic contact rather than the "rollover" effect. Detailed analysis of "rollover" effect has been carried out by other researchers [28, 29].

The CdTe absorber of high-efficiency poly-CdTe cells can be either fully or non-fully depleted, depending on the the absorber thickness and carrier density. Fig. 4.28 compares the energy band diagrams of a 2-μm-thick CdTe absorber with two hole densities under illumination. Both cases have a high back barrier, $\phi_b = 0.5$ eV ($\phi_M = 5.3$ eV). When $p = 1 \times 10^{14}\ cm^{-3}$, the absorber is fully depleted; when $p = 1 \times 10^{15}\ cm^{-3}$, it has a flat neutral region between the front and back depletion regions. At 0.8-V bias, there is more voltage drop across the back depletion region in the fully-depleted case, which allows greater minority-electron injection at the back (E_{Fn} is closer to E_C) and thus leads to increased forward current.

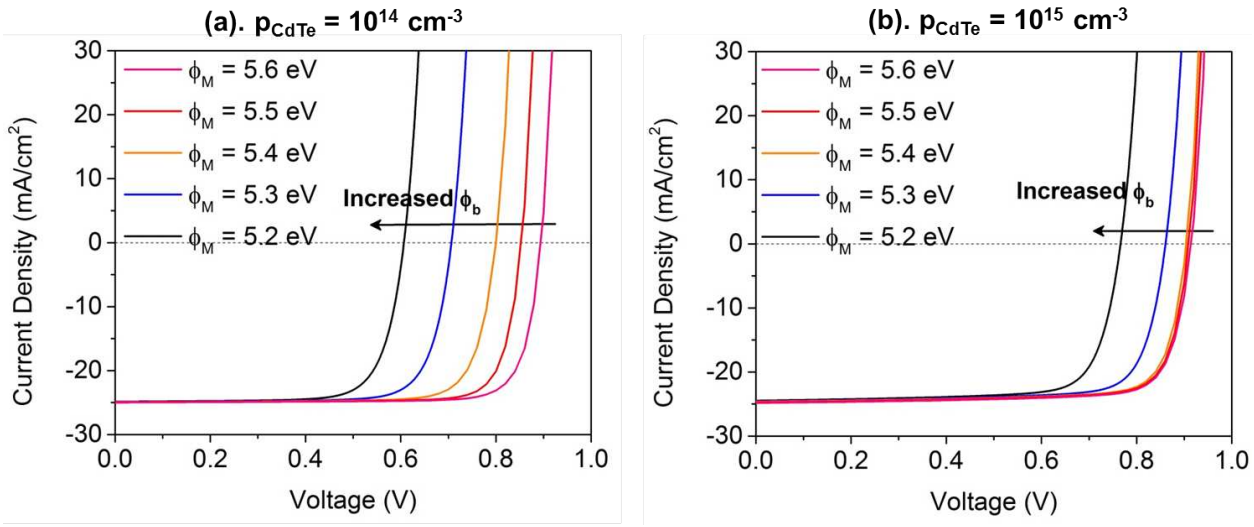

Figure 4.29: The corresponding light J-V curves with a variety of metal work function ϕ_M, for two CdTe hole densities: (a) $10^{14}\ cm^{-3}$ and (b) $10^{15}\ cm^{-3}$. Smaller ϕ_M produces larger back barrier ϕ_b

In contrast, the neutral region in the non-fully depleted case allows the primary front junction to more effectively block the forward current and thus segregates the detrimental impact of high ϕ_b on the J-V curves. Only a small forward electron current takes place due to the back surface recombination. The corresponding J-V curves with a variety of

ϕ_b are shown in Fig. 4.29. As expected, the V_{OC} for the fully depleted CdTe cells is more severely impacted by the back barrier (ϕ_b). When $\phi_b < 0.5$ eV ($\phi_M > 5.3$ eV), V_{OC} is nearly independent on ϕ_b for the non-fully depleted cells. Overall, with low metal work function and no buffer contact layer, V_{OC} decreases with the increased ϕ_b, for both cases but at a lesser rate for non-fully depleted CdTe absorber.

4.4.3 Role of Buffer Back Contact: Tellurium (Te)

A buffer contact adjacent to the CdTe absorber is often created to mitigate the detrimental impact of the large back barrier. Several approaches have been used to form this buffer contact, including etching the CdTe back to form a tellurium-rich p^+ surface, applying copper treatment or copper-containing material to highly dope the back surface, and depositing additional thin layer (e.g., Te [89], Sb_2Te_3 [90], ZnTe:Cu [91]) to adjust the band alignment. Recently, CSU has fabricated record high-efficiency CdTe solar cells for a university with

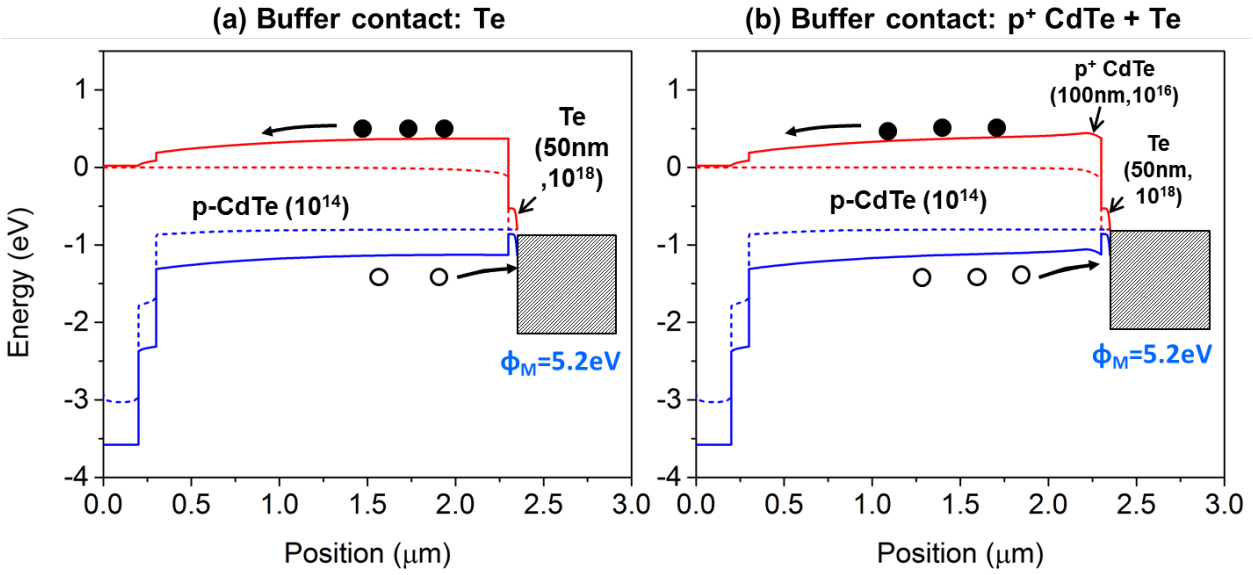

Figure 4.30: Energy-band diagram of CdTe solar cell with two types of buffer back contact at 0.8-V bias under illumination: (a) 50-nm Te (b) 100-nm p^+ CdTe + 50-nm Te.

certified $\eta = 18.3\%$ [92]. The application of the Te buffer contact has played an important role in achieving such high efficiency.

To simulate cells with the Te layer, measured material parameters from films fabricated at CSU were used: the CdTe absorber doping is set as 10^{14} cm^{-3} and a 50-nm-thick Te layer with p-type doping of 10^{18} cm^{-3}. From the UPS measurements by Niles et al. [93], a valence-band offset $\Delta E_V = 0.27$ eV between CdTe and Te is assumed in the baseline model of Fig. 4.30. In Fig. 4.30(b), a 100-nm-thick p^+ (10^{16} cm^{-3}) CdTe at back CdTe is also assumed to reflect the Cu doping with CuCl post treatment [63].

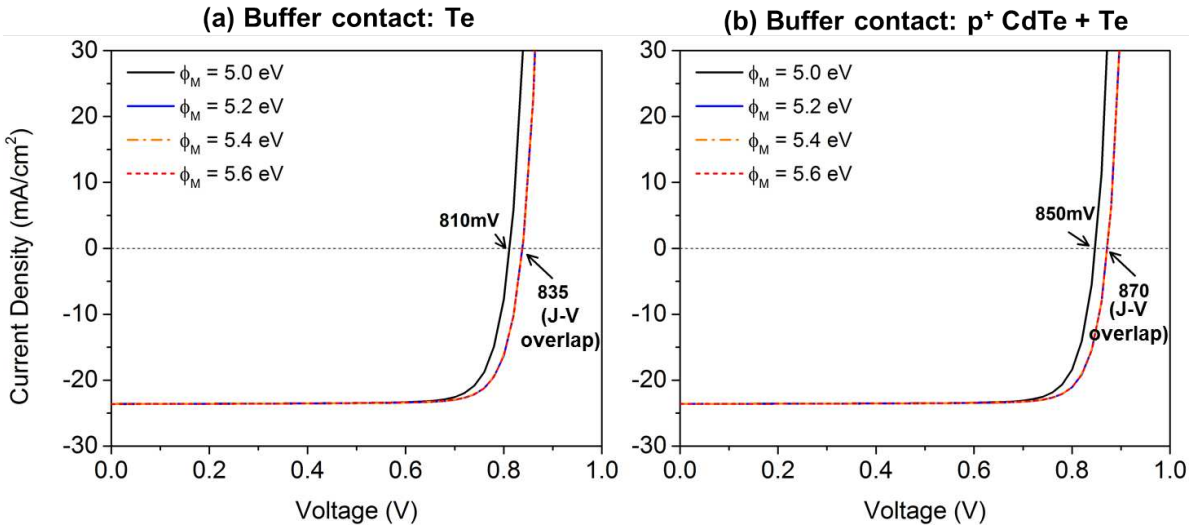

Figure 4.31: The corresponding light J-V curves of CdTe solar cell with two types of buffer back contact and a variety of metal work functions ϕ_M: (a) 50-nm Te (b) 100-nm p^+ CdTe + 50-nm Te.

Fig. 4.30(a) shows the energy band diagram with 50-nm-thick Te buffer contact at 0.8-V bias under illumination. Compared to cells without the buffer contact (see Fig. 4.28(a)), the thin Te buffer causes less voltage drop at the back contact region at the same 0.8-V bias, which suppresses the enhanced forward electron current. Meanwhile, the Te buffer reduces the downward valence-band bending caused by the low metal work function and thus there is less impedance of the light-generated hole current transport. Therefore, the cell V_{OC} is nearly independent of ϕ_M, see Fig. 4.31(a). When a highly-doped p^+ CdTe layer is applied (Fig. 4.30(b)), the electrostatic potential is increased, further enhancing the carrier collection, and hence the J-V curves of Fig. 4.31(b) shows larger V_{OC}.

It is noted that a small valence-band offset ($\Delta E_V = 0.27$ eV) between CdTe and Te has been chosen from Ref. [93], which is favorable for the hole transport. However, the accuracy of this value for ΔE_V remains under discussion [94] and may vary case by case, depending on the Te film processing and post treatments.

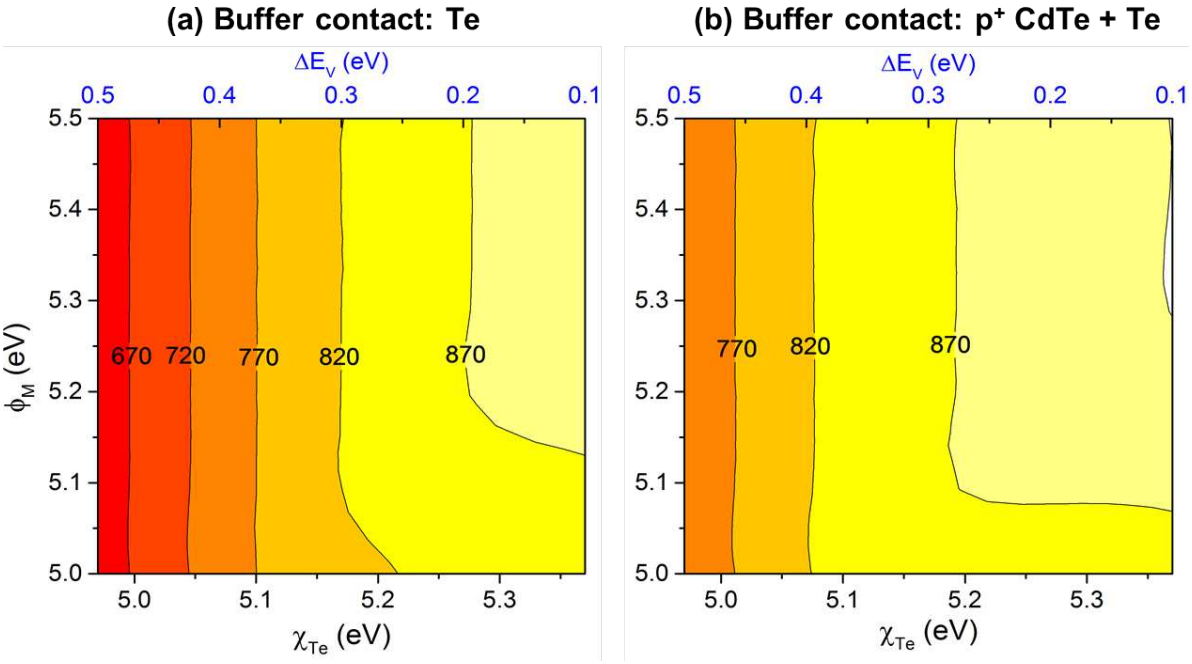

Figure 4.32: The performance contour plots of CdTe solar cell with varying Te electron affinity χ_{Te} and metal work function ϕ_M for two types of buffer back contact: (a) 50-nm Te (b) 100-nm p^+ CdTe + 50-nm Te. The blue axes correspond to the ΔE_V between CdTe and Te due to the variation of the tellurium's electron affinity χ_{Te}.

Fig. 4.32 shows the V_{OC} contour plots with varying the ΔE_V between CdTe and Te (by varying the Te electron affinity χ_{Te}) and the metal work function for the metallic contact ϕ_M for the two types of buffer back contact. The V_{OC} is nearly independent of the metal work function ϕ_M, which is similar to the previous discussion. When $\Delta E_V > 0.3$ eV, V_{OC} is reduced linearly with ΔE_V. This reduction is caused by the downward band bending at the back surface, which enhances forward diode current as shown in Fig. 4.33. Additionally, ΔE_V has very slight impact on other performance parameters (not shown here). From Fig. 4.32(b), it is seen that a p^+ CdTe back surface can partially compensate the detrimental impact of

large ΔE_V with increased electrostatic potential. Overall, a relatively small ΔE_V is desired to achieve the effectiveness of Te buffer back contact.

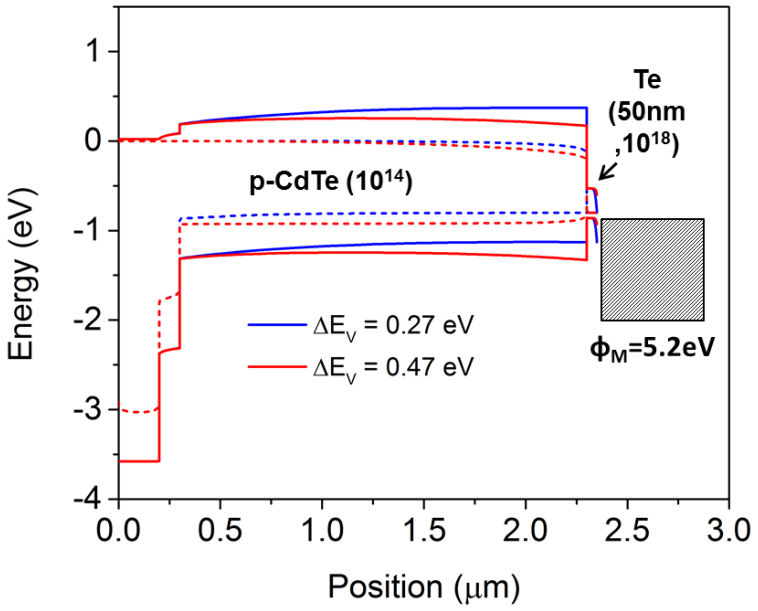

Figure 4.33: Energy-band diagrams for two values of ΔE_V (0.27 ev vs. 0.47 eV) between CdTe and Te at 0.8-V bias under illumination.

4.4.4 Summary

In summary, a significant back-contact barrier ϕ_b caused by the low metal work function can enhance the forward current and thus result in a reduced V_{OC}, particularly with fully depleted CdTe devices. A buffer contact layer between CdTe absorber and metallic contact is highly desirable to mitigate this detrimental impact. The simulation has shown that a thin tellurium (Te) buffer as well as a p^+ CdTe layer can assume such a role by reducing the downward valence-band bending caused by large ϕ_b and hence enhancing the extraction of the charge carriers. The metal work function still plays a role, but a less significant one. A comparison of the Te-buffer contact with the experimental results will be given in Section 5.2 to verify the simulated results.

Chapter 5

COMPARISON WITH EXPERIMENTAL RESULTS

Device simulation is dedicated to explain physics mechanisms and guide the experimental fabrication of solar cells. Good consistency between experiment and simulation should greatly assist device optimization. In this chapter, two types of experimental CdTe devices (monocrystalline cells made at NREL and First Solar, and polycrystalline thin-film cells made at CSU) are discussed in parallel with simulation results. The analysis of their device performance and the corresponding guidance for further efficiency improvement is given.

5.1 Monocrystalline CdTe Solar Cells

5.1.1 Introduction

As discussed in Section 2.2.2, by taking the advantages of high carrier concentration and low defect density of the monocrystalline (mono) CdTe materials, two research groups have broken through the 1-V open-circuit-voltage (V_{OC}) barrier. The cells from NREL [32] were made with p-type mono-CdTe wafers and phosphorous doping, and they reached $V_{OC} \sim 1$ V; the cells from Arizona State [35] were fabricated with n-type CdTe absorbers, which were epitaxially grown on InSb substrates by molecular beam epitaxy (MBE), and these cells obtained $V_{OC} \sim 1.1$ V.

For the current work, a different device structure was adapted for mono-CdTe cells, as shown in Fig. 5.1. The primary solar junction is grown on a p-type mono-CdTe wafer. It consists of an i-ZnO/ZnO:Al bilayer front contact, a 40-nm-thick Cd(S,O) emitter by sputtering deposition, and a 3-μm-thick p-type epitaxial CdTe absorber (carrier density $\sim 10^{16}$ cm^{-3} and bulk lifetime ~ 1 ns, deduced from C-V and TRPL measurements, respectively). The epitaxial CdTe absorbers were grown at Texas State University and First Solar; the emitter, TCO, and back contacts were completed at NREL. To date, the highest V_{OC} achieved with

such device structure is $\sim$ 840 mV, which is below its potential (in principle, $V_{OC} > 900$ mV should be achievable with $p \sim 10^{16}\ cm^{-3}$ and $\tau \sim 1$ ns, see Section 4.1.2). In this section, analytical and numerical calculations will be employed to identify possible mechanisms limiting the cell voltage and to propose enhancement strategies.

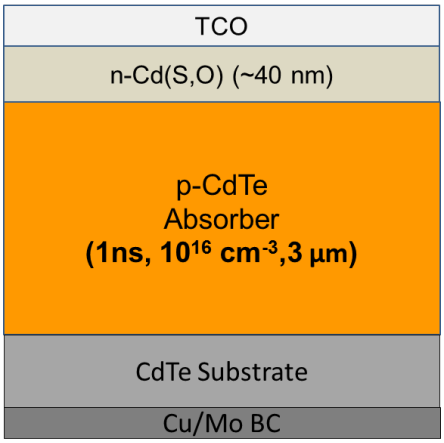

Figure 5.1: Schematic of epitaxial mono-CdTe devices fabricated in our project. Not to scale.

5.1.2 Comparison: Experiment vs. Simulation

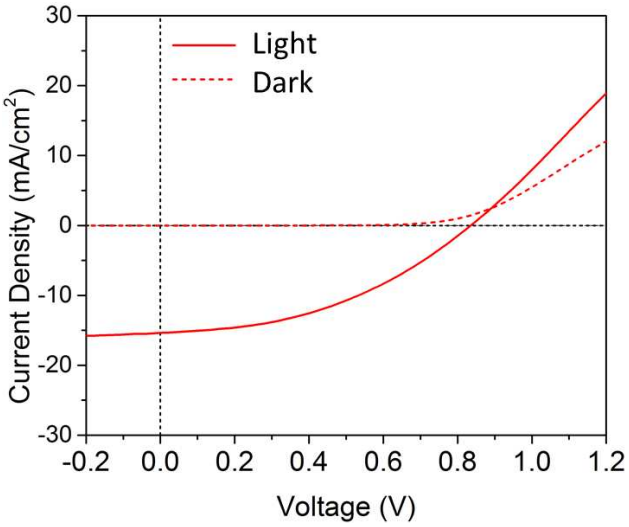

Figure 5.2: The measured dark and light J-V curves of an epitaxial CdTe cell with the configuration of Fig. 5.1. Data from K. Zaunbrecher.

Fig. 5.2 shows the dark and light J-V curves of a typical epitaxial CdTe cell fabricated with the configuration in Fig. 5.1 (experimental results provided by K. Zaunbrecher). The J-V curves show a significant series resistance $R_S \sim 10\ \Omega \cdot cm^2$ (extracted with CurVA software at CSU based on [95]) and hence the FF is significantly reduced. The CdTe wafers available have been highly resistive (see Section 4.3.3) and are the reason for the large R_S. Since the large R_S is due to the wafer and not central to the device operation, it is helpful to back it out of the analysis. Fig. 5.3 shows the device analysis procedure to extract R_S analytically and correct the voltage with $V_{no-R_S} = V_{meas.} - JR_S$ for comparison with the simulated J-V curves.

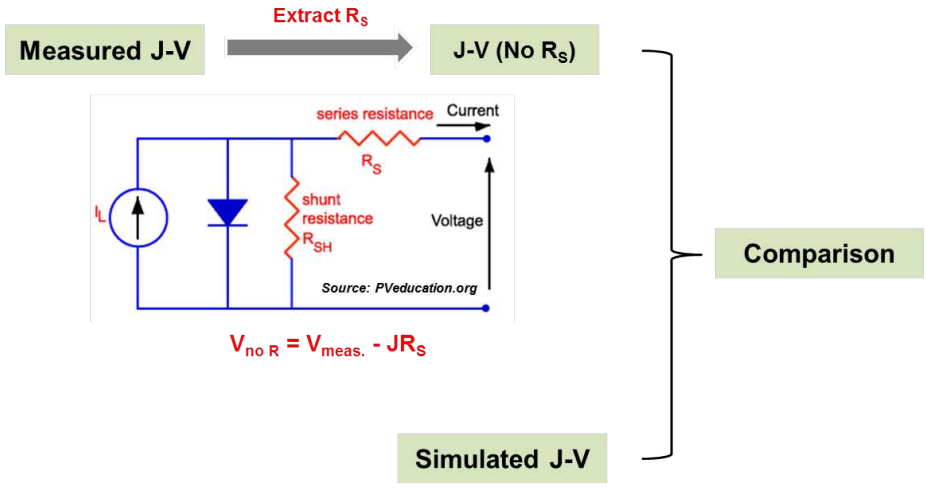

Figure 5.3: The analysis procedure to extract the R_S from measured J-V curves for comparison with simulation.

Fig. 5.4(a) shows the corrected J-V curves (excluding R_S) of the epitaxial CdTe cells with two O_2/Ar ratios in the sputter beam for depositing Cd(S,O) emitters. The energy gap E_g of Cd(S,O) can be adjusted by varying the oxygen fraction in the beam. The low oxygen emitter (0.05% O_2, blue curves) has a measured $E_g \sim 2.38$ eV, close to the E_g of CdS; the high oxygen one (0.55% O_2, red curves) has a measured $E_g \sim 2.63$ eV. The higher O_2 in Cd(S,O) should also shift the conduction-band offset ΔE_C from "cliff" ($\Delta E_C = -0.1$ eV at CdS/CdTe interface [40]) to "spike". In addition, sputtering Cd(S,O) directly onto the

epitaxial CdTe absorber likely creates defects due to the high energy Cd and S ions, which may introduce high carrier recombination near the junction [96].

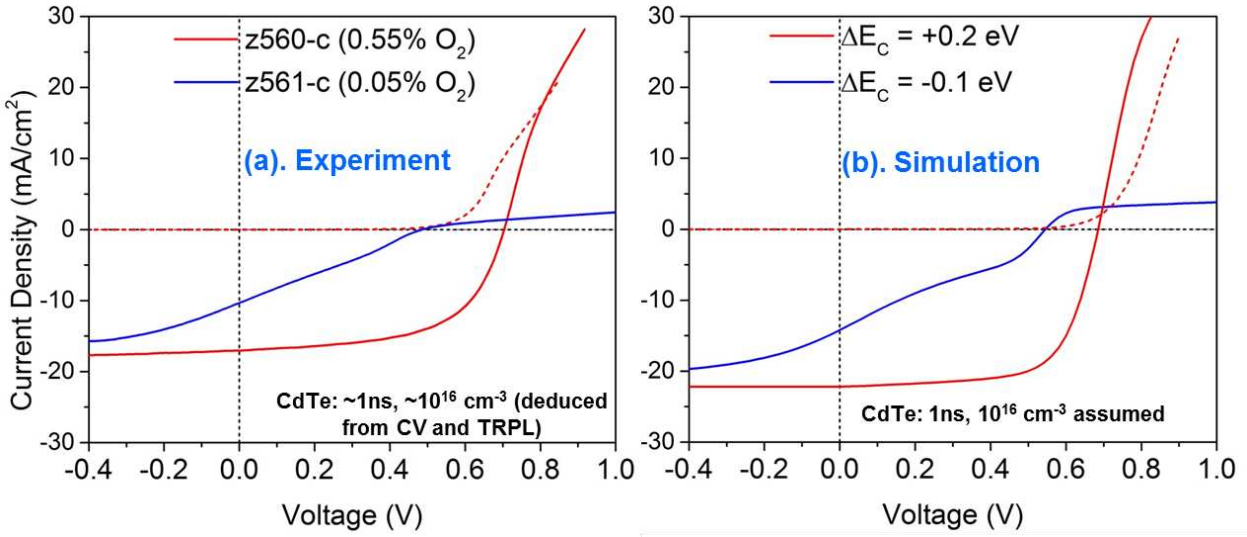

Figure 5.4: J-V Comparison: (a) experimental cells [K. Zaunbrecher] with two O_2/Ar ratios during the deposition of Cd(S,O) emitters; (b) simulated curves with two values of emitter/absorber ΔE_C. Note that it is difficult to extract the R_S of the blue J-V, thus a large $R_S = 10\ \Omega \cdot cm^2$ was included for $\Delta E_C = -0.1eV$ in simulation.

Accordingly, a large S_{IF} ($\sim 10^6$ cm/s) plus a defective CdTe layer (200-nm, with the defect density - the CdTe absorber to interface increased from 10^{13} to 10^{17} cm^{-3}) are chosen for simulation. Two ΔE_C values (i.e., -0.1 eV and +0.2 eV) are assumed to approximate the band alignments between Cd(S,O) and CdTe with the above two O_2/Ar ratios. Fig. 5.4(b) shows the simulated J-V curves with these two ΔE_C values. Similar shapes for the experimental and simulated J-V curves seen in Fig. 5.4 strongly suggest that the conduction-band offset plays a significant role in the impact of interfacial recombination, consistent with the conclusion in Section 4.2.2. With a spike between 0.1 and 0.3 eV, the cell should be able to tolerate a much larger S_{IF} due to the insufficient holes to recombine with the interface electrons; in contrast, with a cliff, the cell has a reduced voltage due to the large interfacial recombination and an inferior FF due to insufficient carrier collection with weak band bending and hence lower electric field.

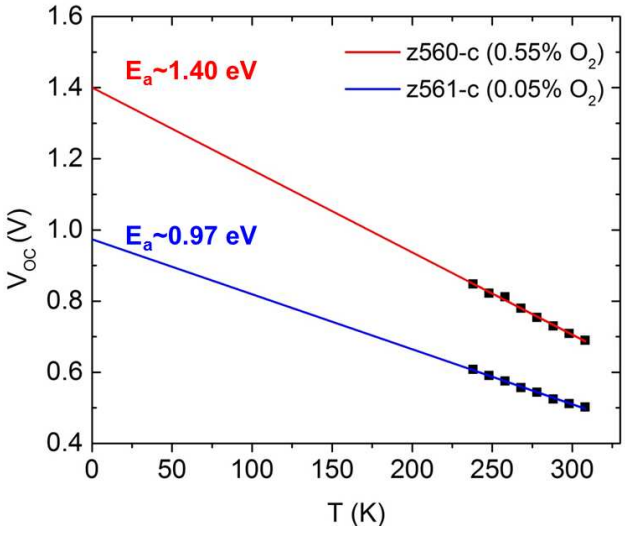

Figure 5.5: V_{OC} vs. temperature for two oxygen ratios in Cd(S,O) emitters: 0.05% O_2 (blue curve) and 0.55% O_2 (red curve).

As discussed in Section 2.1.3, the activation energy E_a in the diode current is a useful parameter to determine the recombination region [23, 25, 59]. E_a can be extracted from the temperature-dependent J-V measurement and the zero-temperature intercept gives E_a. It indicates which region of the junction dominates the recombination and hence limits the cell voltage (i.e., if $E_a \approx E_{g,CdTe}$, the V_{OC} loss is dominated by the recombination in the space-charge region (SCR) of the absorber; if $E_a < E_{g,CdTe}$, the interfacial recombination dominates). Fig. 5.5 shows the open-circuit voltage as a function of temperature for the experimental cells with the two oxygen ratios. By comparing the intercepts between the two cells in Fig. 5.5, it is seen that the E_a for high oxygen $\sim$ 1.40 eV, is close to the CdTe band gap; but the E_a for low oxygen, $\sim$ 0.97 eV, is much smaller than the E_g of CdTe. The difference in intercepts indicates a larger interfacial recombination for the low oxygen ratio, consistent with the previous modeling prediction. In other words, the spike feature with high oxygen ratio can suppress the interfacial recombination and lead to a less voltage-dependent carrier collection and higher V_{OC}. However note that even in the spike case, the cell with high oxygen ratio still shows relatively low V_{OC}, which suggests that the defect states may be spread into the CdTe absorber due to the sputter damage.

5.1.3 Future Work

Based on the previous analysis, it is found that the sputter damage causing large numbers of defect states near the Cd(S,O)/CdTe interface plays an important role in limiting cell performance, particularly for the cell with low oxygen ratio in Cd(S,O) (with a "cliff" band offset). Other effects, such as the large series resistance and reflection, will also reduce the cell performance. A stepwise analysis of the limiting factors to the cell performance is given below.

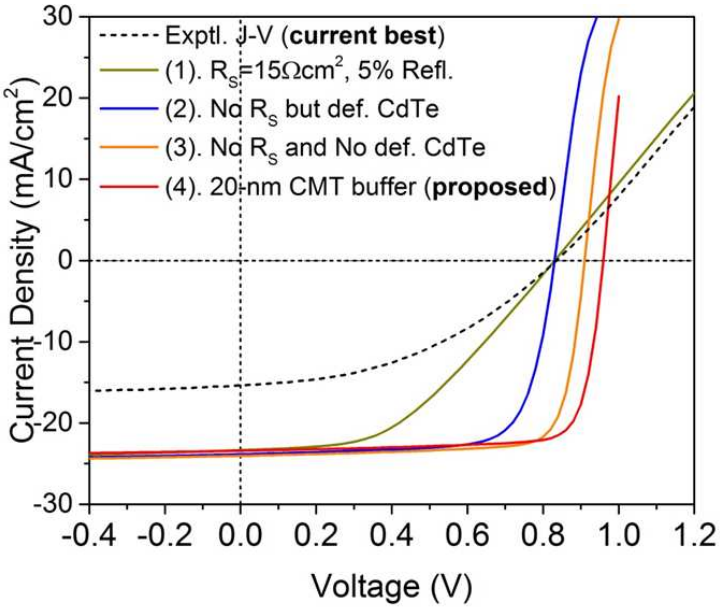

Figure 5.6: Stepwise J-V curves for better cells. "def. CdTe" means that a 200-nm defective CdTe spread from the interface to the absorber is assumed in simulation.

The dashed J-V curve in Fig. 5.6 represents the current best epitaxial cell with $V_{OC} \sim 840$ mV. It was fabricated with high oxygen ratio in the sputtered Cd(S,O) and appropriate post-junction annealing. However, this cell has a relatively low J_{SC} (possibly caused by TCO reflection and high absorption in pre-absorber layers) and poor FF (in part due to resistive CdTe substrate). The V_{OC} near 800 mV is low compared to the simulation of 900 mV for CdTe with 1 ns, 10^{16} cm^{-3}, as shown in Curve (3). Again, one possible reason is that the sputter-damage-induced defective CdTe layer near the interface detracts from the beneficial

effect from the "spike" feature with high oxygen ratio. A thin CdMgTe (CMT) buffer with similar lattice constant and deposition method less prone to damage, such as MBE would likely form a better junction interface. Curve (4) goes a step further and shows the calculated J-V curve with a 20-nm-thick CMT buffer inserted between Cd(S,O) and CdTe. It shows a V_{OC} improvement with favorable positive ΔE_C (=+0.2 eV) and a less-defective CdTe absorber.

Overall, the interface region between the emitter and the absorber is a critical factor for the cell performance of epitaxial CdTe devices, since the bulk recombination has become less of a limitation with increased bulk lifetimes and carrier densities. For future emitter growth on epitaxial CdTe absorbers, a lattice-matched material with less deposition damage is suggested to introduce fewer defect states. However, a type-I interface with the spike should be helpful to suppress the interfacial recombination in any case.

5.2 Polycrystalline CdTe Thin-Film Solar Cells

5.2.1 Introduction

As discussed in Section 2.2.1, most of the high-efficiency polycrystalline (poly) CdTe thin-film solar cells to date have been made with superstrate configuration, as shown in Fig. 2.7. Recently, CSU has fabricated record high-efficiency CdTe solar cells in university level with similar device structure (certified $\eta = 18.3\%$) [92]. The application of an alternative (Mg,Zn)O (MZO) emitter and a Te buffer at the back contact have played important roles in achieving such high efficiency. This section is intended to identify the roles of these layers by comparing them with the simulated results.

5.2.2 Comparison: Experiment vs. Simulation

Fig. 5.7 depicts the device schematic for the poly-CdTe cells made at CSU. Two types of emitters (i.e., CdS and MZO) have been employed for device integration. A CuCl vapor is introduced after depositing the CdTe absorber and is believed to have a reaction with the

CdTe surface. The excess material is subsequentaly removed by evaporation. The result is Cu doping at the CdTe back surface [23, 13, 63]. Then, the cells were deposited with ∼50-nm evaporated-Te buffer contact and painted-Ni metal contact. Detailed fabrication process can be found in Ref. [63].

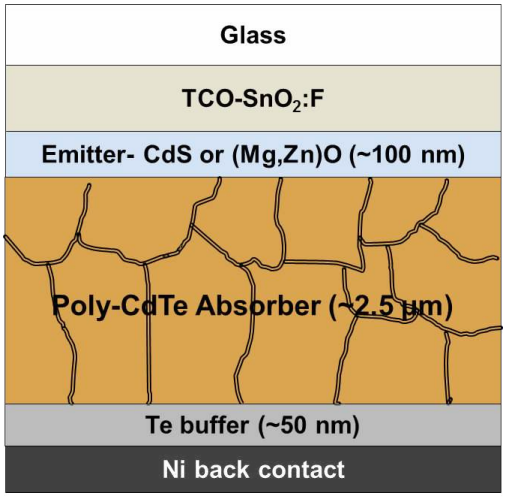

Figure 5.7: Device schematic of poly-CdTe solar cells made at CSU. Not to scale.

Fig. 5.8(a) shows the J-V curves of the experimental cells with CdS and MZO emitters and with and without the introduction of CuCl (experimental J-V data provided by A. Moore). All the cells have ∼ 50-nm-thick Te buffer layers. In Fig. 5.8(a), the cells with MZO emitters have larger J_{SC}, which is a direct result of smaller absorption loss with the larger E_g emitter. In addition, the cells with the CuCl step show less voltage-dependent current collection and better V_{OC}.

Fig. 5.8(b) shows the simulated J-V curves with CdS and MZO emitters. In the simulation, a 50-nm Te buffer layer and a metal with work function $\phi_M = 5.2$ eV were chosen to reflect the back contact system in fabrication, see Section 4.4. The interfacial recombination velocity S_{IF} between the emitter and CdTe absorber was chosen to be 10^5 cm/s based on the TRPL measurements on MZO/CdTe structure by D. Swanson [63]. A 100-nm p^+ (10^{16} cm^{-3}) CdTe layer is assumed at the back surface to reflect the effect of the Cu doping. The comparison of the J-V curves in Fig. 5.8 (a) and (b) shows a reasonable correlation between

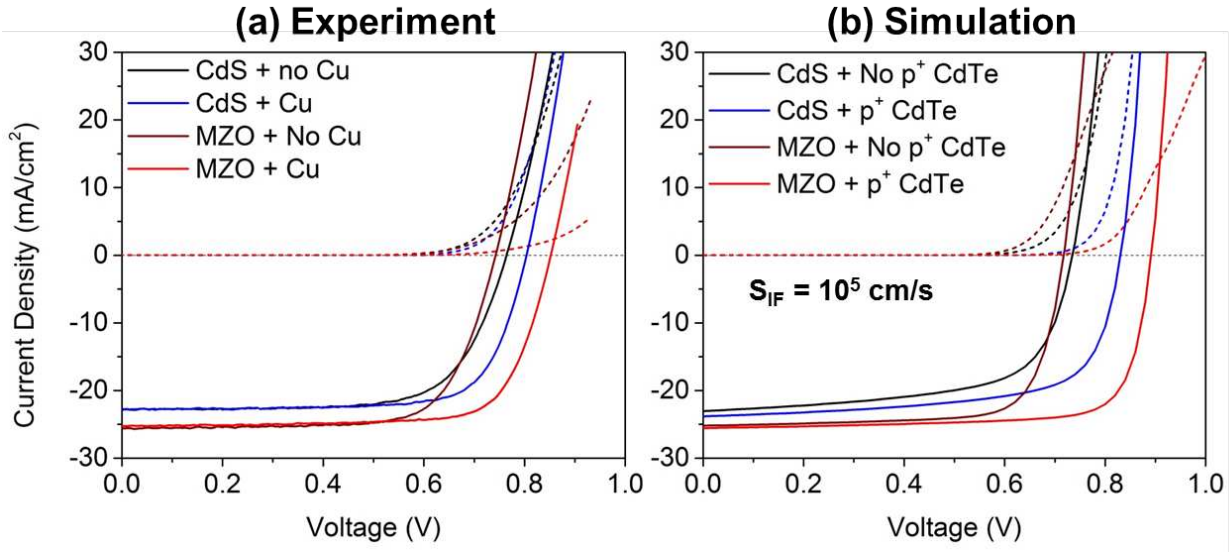

Figure 5.8: Dark and light J-V curves: (a) Experimental cells [A. Moore] with CdS and MZO emitters and with and without CuCl step, but inducing a ∼50-nm Te buffer layer; (b) Simulated cells with CdS and MZO emitters, p^+ CdTe represents an increased-doping back surface due to the CuCl.

experiment and simulation, including the larger J_{SC} with the MZO emitter due to its larger optical band gap and lower optical absorption.

Fig. 5.9 shows the full energy band diagrams of the simulated cells with CdS and MZO emitters. The MZO emitter forms the spike at the MZO/CdTe interface, which suppresses the interfacial recombination as discussed above. In addition, the highly-doped back surface helps reduce the back surface recombination and the Te buffer layer segregates the detrimental impact from the low metal work function (see Section 4.4). As a result, the cell with MZO emitter and a p^+ back surface layer shows the best cell performance, which is consistent with the experimental results.

Note that the above simulations as with the earlier ones were conducted with a combination of experimental parameters and reasonable assumptions. There exists some discrepancy between simulation and experiment in Fig. 5.8, which no doubt means the simulation is neglecting some effects. For instance, an overestimate of the CdS/CdTe interfacial recombination ($S_{IF} = 10^5$ cm/s is assumed in the simulation, the same as the MZO/CdTe interface)

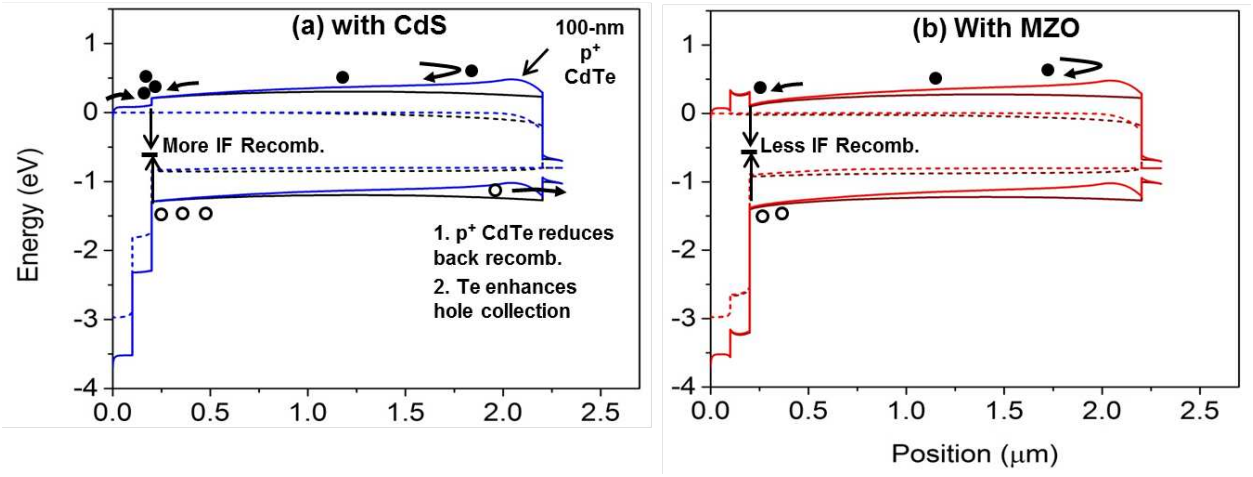

Figure 5.9: Energy-band diagrams of the simulated cells at 0.8-V bias under illumination: (a) with CdS emitter; (b) with MZO emitter. In both cases, a 100-nm $p^+(10^{16})$ CdTe simulates the experimental CuCl step.

may exagarate the V_{OC} loss by the "cliff" and lead to a voltage-dependent current collection in Fig. 5.8(b). Overall, more detailed model system with more accurate experimental parameters is desired in the future.

5.2.3 Future Work

It has been demonstrated that poly-CdTe device can have very good cell performance ($V_{OC} \sim 860$ mV, $\eta \sim 18.3\%$) by utilizing a MZO emitter and a Te buffer contact [92]. There is, however, potential for further V_{OC} improvement. Besides of the optimization of poly-CdTe absorber properties, the application of an electron reflector (ER) can be employed to improve V_{OC} [80]. The principle of ER is to reflect the minority electrons at the back of the CdTe and thus reduce the back surface recombination (see Section 4.3.4 for details). CdMgTe (CMT) is a good candidate for ER, since its conduction-band minimum is increased (reflects electrons away from the back surface) and it has a similar lattice constant to CdTe (introduces less interface defects).

To look at the electron-reflector concept with a specific structure, Fig. 5.10(a) shows the energy band diagram of a proposed device structure with an addition of CMT ER for

poly-CdTe cells. The purpose of CdTe cap layer is to protect the CMT from oxidation (MgO is easily formed when the film exposing into the atmosphere, causing FF loss [63]). Accordingly, the V_{OC} is enhanced with CMT electron reflector as shown in Fig. 5.10(b). It is noted that the FF is slightly compromised at large voltage bias with low bulk lifetime (τ = 1 ns). An increased absorber lifetime would partially recover the FF loss because of longer diffusion length and better carrier collection. Overall, the simulation shows that the electron reflector should be an effective approach to increase the cell efficiency even with a relative low CdTe carrier concentration ($\sim 10^{14}\ cm^{-3}$).

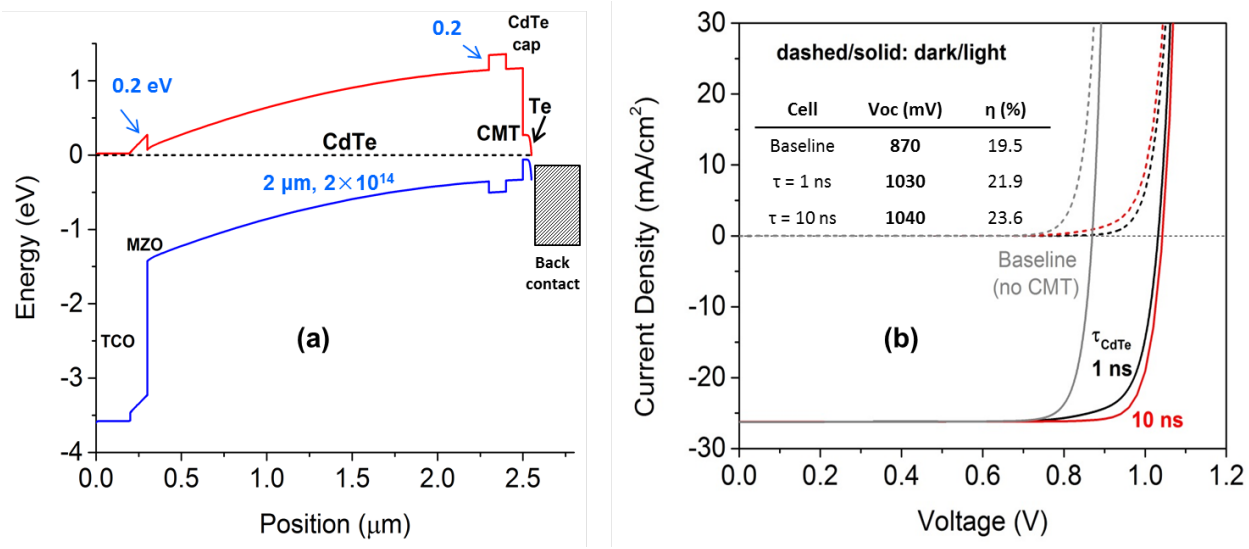

Figure 5.10: (a) Energy-band diagrams of the simulated cells at 0-V bias and dark: (a) simulated J-V curves of the cells without CMT ER and with ER for two bulk lifetimes (τ = 1, 10 ns).

Chapter 6

SUMMARY AND FUTURE WORK

Summary

In this dissertation, a comprehensive model system for high-efficiency CdTe devices was developed to identify both beneficial and detrimental mechanisms for CdTe cell performance and to give guidances for future cell optimization. First, several key design principles for CdTe devices were summarized: (a) the impact of individual layers' material properties, (b) the recombination paths in a full device stack, and (c) the band alignments between layers associated with carrier transport and recombination. By applying these design principles, crucial issues limiting CdTe cell performance were addressed and specific strategies for high-efficiency CdTe solar cells proposed.

Since the CdTe absorber is central to cell performance, several important CdTe material parameters relevant to high-efficiency devices were investigated in Section 4.1. It is found that high V_{OC} above 1000 mV should be achievable when the absorber has a high carrier density ($> 10^{16}\ cm^{-3}$). However, superior device performance with $\eta > 25\%$ requires both high carrier density and lifetime. As the bulk lifetime increases, an appropriate buffer layer is strongly desired to reduce the back-surface recombination while utilizing a relatively thin absorber.

An equally important consideration is the interfaces between different layers of CdTe cells. One of these is the emitter/absorber interface. The discussion in Section 4.2 summarized three primary factors of this interface affecting CdTe cell performance: (a) the conduction-band offset ΔE_C, (b) the emitter doping and thickness, and (c) the density and energy distribution of interface defects. A positive ΔE_C ("spike") is beneficial to the cell performance, since it can induce a large hole barrier that suppresses the interfacial recombination, but too large a spike is detrimental to photocurrent transport. In a heterojunction device

with many defects at the emitter/absorber interface (high S_{IF}), a thin and highly-doped emitter can induce strong absorber inversion and hence help maintain good cell performance. The charge types and energetic locations of interface defects will also influence the interfacial recombination. When acceptor-type interface defects are located near mid-gap, the performance loss is significantly larger than with defect energies nearer a band edge or with donor-type defects. In terms of specific emitter materials, the calculations suggest that the (Mg,Zn)O alloy with 20% Mg, or a similar type-I heterojunction partner with moderate ΔE_C (e.g., Cd(S,O) or (Cd,Mg)Te with appropriate oxygen or magnesium ratios) should be advantageous for the emitter choice.

The CdTe/substrate interface is also important in the growth of epitaxial monocrystalline CdTe cells. Several substrate materials have been discussed and each has its advantages and disadvantages. Available CdTe substrates have excessive series resistance; however, Si and GaAs have a large lattice mismatch with a CdTe absorber, and Si, GaAs, and InSb substrates all have issues with band offsets at the CdTe/substrate interface, which impede the flow of holes and allow excessive forward current. To address the unfavorable band alignment between CdTe absorber and InSb substrate, three enhancement strategies were considered: (a) a highly-doped CdTe buffer, (b) an expanded-band-gap layer, and (c) the application of an InSb TD. A highly-doped CdTe buffer can play a role in both reflecting electrons and assisting holes; however, its effectiveness is likely to be limited due to the difficulty in achieving heavy doping. Since a CZT buffer has an expanded band gap in the conduction band, it can more easily form an electron reflector and thus can improve the cell performance more effectively. The incorporation of an InSb TD adds a small additional mitigation of the band bending and should produce a slightly better V_{OC}. Overall, each approach has different degrees of performance improvement; however, a combination of the approaches is advised for the highest efficiencies.

The CdTe/back contact interface also plays a significant role in forming ohmic contact and thus assist carrier transport for conventional polycrystalline thin-film CdTe devices. In Section 4.4, it was identified that a significant back-contact barrier ϕ_b caused by the low metal

work function can block hole transport and enhance the forward current and thus result in a reduced V_{OC}, particularly with fully depleted CdTe devices. A buffer contact layer between CdTe absorber and metallic contact is strongly needed to mitigate these detrimental effects. The simulation shows that a thin tellurium (Te) buffer as well as a p^+ CdTe layer can assume such a role by reducing the downward valence-band bending caused by large ϕ_b and hence enhancing the extraction of the charge carriers.

Finally, the experimental CdTe cells were discussed in parallel with the simulation results to identify limiting mechanisms for cell performance and give guidance for future efficiency improvement. For the monocrystalline CdTe cells made in our project, it is found that the sputter damage causing large numbers of defect states near the Cd(S,O)/CdTe interface plays an important role in limiting cell performance, particularly for cells with low oxygen Cd(S,O) (with a "cliff" band offset). Other effects, such as the large series resistance and reflection, also reduce the cell performance. In the future emitter growth on epitaxial CdTe absorbers, a lattice-matched material with less deposition damage is suggested to introduce fewer defect states and a type-I interface with the spike should be helpful to suppress the interfacial recombination in any case. For polycrystalline CdTe solar cells made at CSU, it is demonstrated that the MZO emitter forms a spike at the MZO/CdTe interface and the Te buffer layer mitigates the large back-contact barrier caused by low metal work function. Both play very important roles in achieving good cell performance ($V_{OC} \sim 860$ mV, $\eta \sim 18.3\%$). The simulation has also shown that the electron reflector should be an effective approach to further increase V_{OC} even with a relative low CdTe carrier concentration ($\sim 10^{14}\ cm^{-3}$).

Future Work

Although an in-depth model system for high-efficiency CdTe devices has been developed in this work, several other promising aspects relevant to improving cell performance have not yet been fully explored and are worthy investigating in the future. A few of them are listed below.

1. Bandgap gradient of CdTe absorbers. Both First Solar [9] and CSU [63] have demonstrated that a gradually reduced CdTe bandgap with addition of Se element at the front absorber can produce a higher photocurrent while maintaining V_{OC}. However, limited theoretical study has been carried out on this strategy. It would be helpful to quantify the beneficial effect of the bandgap grading and give an optimized CdTe grading structure.

2. Application of n-type absorbers. A conventional p-type CdTe material was chosen in this work. However, it is known that the p-type CdTe has a tendency to form a hole-blocking schottky barrier due to its large E_g and high electron affinity (the fermi-level of p-CdTe is closer to its valence band and thus a metal with high work function is needed to match the E_F). The n-type CdTe absorber gives an alternative approach to solve this challenging task since the E_F of n-type CdTe is closer to the conduction band. ASU has experimentally demonstrated this concept with epitaxial n-type CdTe absorbers and record V_{OC} ($\sim$ 1.1 V) [35], but limited device-physics study has been done to date. Therefore, it would be instructive to develop a parallel model system for n-type CdTe cells as well.

3. Reduction of back surface recombination. Fig. 3.4 summarized several strategies to suppress the back surface recombination. A few of them, such as, the heavily-doped back CdTe and extended-E_g electron reflector (ER), have been investigated in Section 4.3. However, the practical problems limiting the effectiveness of these approaches have not been thoroughly addressed. Our CSU colleagues have identified that when employing a CdMgTe ER, there can be several detrimental mechanisms present, such as, large S_{IF}, hole-blocking valence-band offset ΔE_V at CdTe/CMT, and Mg loss after $CdCl_2$ treatment, all of which can compromise the cell performance [63, 92]. More careful design strategies would be of great importance in the future. For instance, the concept of ER bandgap grading seems to be a promising approach to mitigate the hole-blocking ΔE_V and reduce interface defects due to lattice mismatch. In addition, the application of dielectric charge layer may be applicable to CdTe cells for the reduction of back surface recombination as well. Its basic principle is to reduce the availability of minority carriers at the back surface with the repelling force from charge layers. It has been successful in Si and CIGS technologies [42, 43].

4. Advanced concepts such as photon recycling and tandem cells. Non-radiative SRH recombination for the present is still the dominant limiting mechanism for carrier recombination in majority of the CdTe solar cells, particularly for poly-CdTe devices. However, it has shown that the radiative recombination becomes dominant for some monocrystalline CdTe devices with $V_{OC} \sim 1.1$ V [35]. For these devices, the photon recycling will be a necessity to enhance the absorption of the radiatively emitted photons and hence further improve V_{OC}. In addition, a tandem-junction device structure should be applicable for CdTe when incorporating with other elements such as Zn and Mg and thus having a tunable bandgap. Overall, similar to the III-V technology, advanced optical-electrical coupled design approaches are desired to obtain much higher-efficiency CdTe devices ($\eta \sim 30\%$ for single junction and $\eta > 33\%$ for multi-junction cells)

List of Publications

1. **T. Song**, J. T. McGoffin, J. R. Sites. *Interfacial-Barrier-Induced J-V Distortion of CIGS Solar Cells with Sputtered Zn(O,S) Buffer Layers*, IEEE J. Photovoltaics, vol.4, pp. 942-947, 2014.

2. **T. Song**, A. Kanevce, J. R. Sites, *Exploring the Potential for High-Quality Epitaxial CdTe Solar Cells*, Proc. IEEE Photovoltaics Conf., pp. 2412-2415, 2014.

3. **T. Song**, A. Kanevce, J. R. Sites, *Choice of Substrate Material for Epitaxial CdTe Solar Cells*, Proc. IEEE Photovoltaics Conf., pp. 1-4, 2015. (**finalist for best student paper award**)

4. **T. Song**, A. Kanevce, J. R. Sites, *Design of High-Efficiency Epitaxial CdTe Solar Cells on InSb Substrates*, IEEE J. Photovoltaics, vol.5, no. 6 pp. 1762-1768, 2015.

5. **T. Song**, A. Kanevce, J. R. Sites, *Emitter Choice for Epitaxial CdTe Solar Cells*, Proc. IEEE Photovoltaics Conf., 2016.

6. **T. Song**, A. Kanevce, J. R. Sites, *Emitter/Absorber Interface of CdTe Solar Cells*, J. Appl. Phys., Vol. 119. no. 23, pp. 233104, 2016.

7. A. Moore, **T. Song**, C. Moffett, R. Pandy, J. R. Sites, *Improved CdTe Solar-Cell Performance with an Evaporated Te Layer before the Back Contact*, Submitted to Mat. Res. Soc. Symp. Proc., 2017.

8. **T. Song**, J. R. Sites, *Role of Tellurium Buffer Layer on CdTe Solar Cells' Absorber/Back-Contact Interface*, Proc. IEEE Photovoltaics Conf., 2017.

9. **T. Song**, A. Moore, J. R. Sites, *CdTe Solar Cells' Back Contact System: Effects of Buffer and Metallic Layers*, in preparation.

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