DISSERTATION

INVESTIGATION OF GROUP V DOPING AND PASSIVATING OXIDES TO REDUCE THE VOLTAGE DEFICIT IN CDTE SOLAR CELLS

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ABSTRACT

INVESTIGATION OF GROUP V DOPING AND PASSIVATING OXIDES TO REDUCE THE VOLTAGE DEFICIT IN CDTE SOLAR CELLS

Thin film cadmium telluride is one of the most successful photovoltaic technologies on the market today. Second only to silicon in yearly output and accounting for 40% of U.S. utility-scale photovoltaic installation, CdTe is known for its ease of manufacture, ideal bandgap, and low levelized cost of energy. Despite its commercial success, CdTe underperforms compared to its theoretical potential. The current world record CdTe device is only 21.0% compared to a theoretical maximum of 33.1%. This significant discrepancy in efficiencies can mostly be attributed to the poor open-circuit voltage of CdTe devices. Compared to silicon technologies, CdTe has a large voltage deficiency, exceeding 250 mV.

While copper doping has traditionally been used for CdTe devices, it has proven to be incapable of sufficiently doping CdTe. Copper typically dopes CdTe in the 10^{14} to 10^{15} holes/cm^3 range where most models predict that 10^{16}–10^{17} is needed. Additionally, interstitial copper is a fast diffuser in CdTe, and can lead to numerous stability issues. As an alternative to copper, this work explores arsenic as a dopant for CdTe. Using a novel arsenic doping technique, hole concentrations greater than 10^{15} cm^{-3}, microsecond lifetimes, and increased radiative efficiency are achieved. These are important prerequisites to achieving higher voltages.

Achieving high doping levels alone is not sufficient to achieve higher device performance. A well-passivated and carrier selective contact is needed to ensure that electron-

hole pairs do not recombine and are extracted as useable energy. Aluminum oxide has been shown to passivate CdTe surfaces. This work illustrates the explorations of using Al_2O_3 as a passivation layer, pairing it with highly doped amorphous silicon as a hole contact, resulting in excess-carrier lifetimes up to 8 µs, the highest reported to date for polycrystalline Cd(Se)Te.

Although the inclusion of arsenic doping and an aluminum oxide back contact are each explored separately, the combination of both methods result in massive improvements to the carrier lifetime, interface passivation and radiative efficiency. Through this combination, microsecond lifetime and External Radiative Efficiency of over 4% are achieved. The excellent ERE values measured here are indicative of large quasi-Fermi level splitting, leading to an implied voltage with multiple device structures of nearly 1 V and an implied voltage of 25%.

Finally, while CdSeTe serves as a more promising photovoltaic absorber candidate compared to CdTe, certain difficulties remain which must be addressed. Careful selection of processing conditions is shown to create a dense and large-grained film while eliminating wurtzite-phase crystal growth, which has been shown to degrade device performance. Surprisingly, as-deposited CdSeTe is shown to be n-type or nearly intrinsic rather than the previously supposed p-type. This necessitates additional steps to account for very poor hole conductivity, which can produce zero-current devices if not addressed. Challenges notwithstanding, CdSeTe absorbers are shown to be a key component in devices capable of a photovoltaic conversion efficiency of greater than 25%.

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LIST OF NOMENCLATURE

AM	Air Mass
a-Si:H	Hydrogenated amorphous silicon
BOS	Balance of System
BSF	Back-Surface Field
c-Si	Crystalline Silicon
CdTe	Cadmium Telluride
CdSeTe	Cadmium Selenium Telluride
CIGS	Copper Indium Gallium Selenide
CF	Capacitance vs Frequency
CL	Cathodoluminescence
CV	Capacitance vs Voltage
CO_2	Carbon Dioxide
CSS	Close Space Sublimation
CSU	Colorado State University
EDS	Energy Dispersive X-Ray Spectrometry
E_g	Band Gap
E_C	Conduction Band
E_V	Valence Band
e-h	Electron-Hole Pair
eV	Electron-Volt
ERE	External Radiative Efficiency
FF	Fill-factor
FWHM	Full Width at Half Maximum
GaAs	Gallium Arsenide
GAXRD	Glancing Angle XRD
GDP	Gross Domestic Product
GHG	Greenhouse Gasses
GW	Gigawatt
I_{mp}	Current at max power point
I_{sc}	Short-circuit Current
ICP-MS	Inductively-Coupled Plasma Mass Spectrometry
ITO	Indium-Tin Oxide
iV_{OC}	Implied Open-Circuit Voltage
J_{sc}	Short-circuit Current Density
JV	Current Density vs Voltage
K	Degrees kelvin
kWh	kilowatt-hour
LCOE	Levelized Cost of Energy
MBE	Molecular Beam Epitaxy
MOCVD	Metal-Organic Chemical Vapor Deposition

MTOE	Million Tonnes of Oil Equivalent
MZO	$Mg_xZn_{1-x}O$
NREL	National Renewable Energy Laboratory
PL	Photoluminescence
ppm	Parts Per Million
PTAA	Poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine]
P_T	Theoretical power of a perfect diode
PV	Photovoltaic
QE	Quantum Efficiency
qFL	Quasi-Fermi Level
qFLS	Quasi-Fermi Level Splitting
S	Interface Recombination Velocity (cm/s)
SCP	Scanning Capacitance Microscopy
SEM	Scanning Electron Microscope
Si	Silicon
SIMS	Secondary Ion Mass Spectrometry
SRH	Shockley-Reed-Hall Recombination
TCO	Transparent Conducting Oxide
TOPCon	Tunnel Oxide Passivated Carrier- Selective Contacts
TRPL	Time-Resolved Photoluminescence
TWyr	Terawatt-year
V_{Cd}	Cadmium Vacancy
Voc	Open-circuit Voltage
V_{mp}	Maximum power point/voltage
VTD	Vapor Transport Deposition
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
η	Photovoltaic conversion efficiency
τ_{eff}	Effective Carrier Lifetime
τ_b	Bulk Carrier Lifetime
τ_s	Surface Carrier Lifetime
6N	“6 Nine Pure” indicating 99.9999% purity

CHAPTER 1. INTRODUCTION

1.1 What are Photovoltaics?

Since the discovery of the photovoltaic effect in 1839, photovoltaics (PV) have gone from a scientific curiosity, to a niche technology used only for space and distributed power systems, to a large-scale source of world energy today. Photovoltaics is the conversion of sunlight directly into electricity. The most common method of producing electricity via photovoltaics today is done with solar cells fabricated from semiconducting materials. These special materials produce an electrical voltage and current when exposed to light— a phenomenon which is the result of several subsequent energy conversion processes. Thermal radiation is converted to chemical energy within the absorber when a photon of light interacts with matter, exciting an electron to an elevated energy band and the energy is converted from chemical to electrical by the extraction of a flow of electrons from the material while under illumination. Semiconductors have unique material properties which make them particularly well-suited to the absorption and harnessing of energy from sunlight.

Semiconductor elements are found within a relatively narrow band of the periodic table of elements, in groups two through six (groups twelve through sixteen using the European convention.) Of these semiconductors, silicon (Si) is by far the most commonly used for photovoltaics. This is due to its abundant availability in the Earth's crust, its long history of use in electrical devices, and the fact that it is an elemental semiconductor. Other semiconductor materials consist of two or more elements. Known as compound semiconductors, these materials include pairings of elements that have an average of four valence electrons, such as II–VI or III–V semiconductors. Common semiconductors used in photovoltaic applications are Copper

Indium Gallium Selenide (CIGS), Gallium Arsenide (GaAs), and notably, Cadmium Telluride (CdTe), the material used in this work. These elements and their position in the periodic table of the elements can be seen in Figure 1 below.

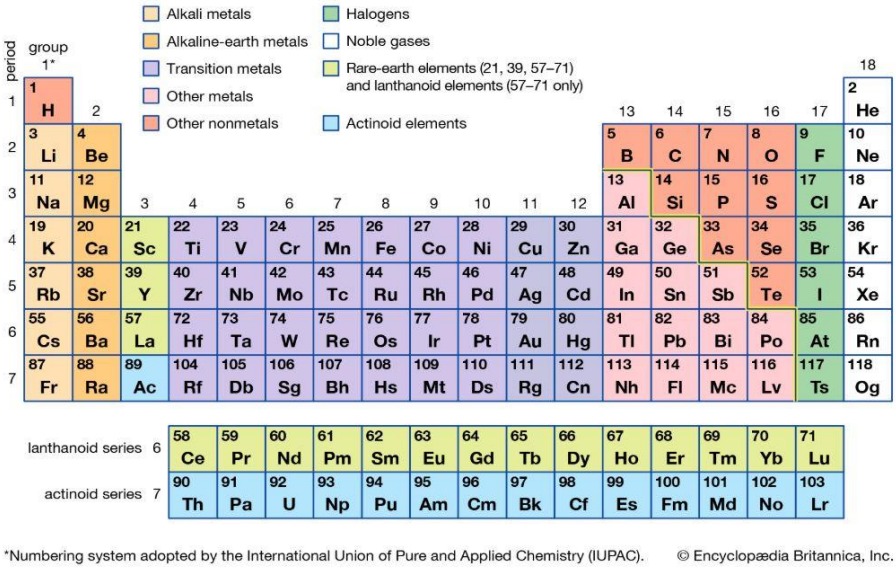

Figure 1. Periodic table of the elements. Adopted from [1]

One of the key material parameters for any semiconductor used for PV applications is that of the bandgap (E_g.) Electrons in a single atom orbit around the nucleus in orbitals that reside at specific, quantized energies. As atoms move closer to one another however, the electrons in the outer shells begin to interact with one another, altering the energy levels of the electrons. The result is that the allowable energy states begin to spread in broad "bands" of allowable energies, as seen in Figure 2. The lower band of allowable energies is known as the valence band (E_v) which corresponds with the energy of electrons that are bound to their host atoms. The upper band is the conduction band (E_c) which corresponds with the energy levels of free electrons that are not bound to a particular atom and are free to move. Between these two

energy bands there is a gap of forbidden energies, known as the bandgap. Without defects in the semiconductor, no electron can reside in a state with energy within this bandgap.

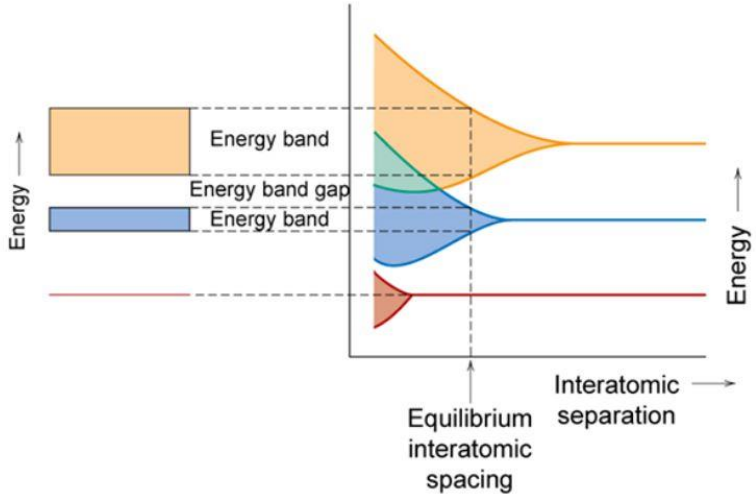

Figure 2: Energy band diagram showing energy states spread into bands as the interatomic distance decreases

Because no state can exist within the bandgap, E_g corresponds with the minimum energy required to excite an electron from the valence band up into the conduction band. If a photon of light has energy equal to or exceeding E_g, it may be absorbed and has sufficient energy to excite the electron into the conduction band, leaving behind a vacancy in the valence band. Rather than visualize a lack of electrons in the valence band, the common convention is to instead designate the absence of an electron as a "hole". This is analogous to visualizing a bubble moving through a liquid, although the liquid is actually moving, it is more convenient to describe the motion of the bubble [4]. This is the generation of an electron-hole pair (e-h.) Photons with energies less than the bandgap do not have enough energy to break the bond and thus do no interact with the electrons and largely pass through the material as if it were transparent. Importantly, the bandgap fundamentally affects how light of different energies interacts with the material. Within the

bandgap of a semiconductor is the Fermi level. At temperatures above 0 K, the Fermi level is a statistical construct that represents the energy at which there is a 50% probability of finding a charge carrier when a Fermi-Dirac distribution is plotted. It does not necessarily mean that a charge carrier will be found at that energy level, considering its location within the bandgap.

The light spectrum that reaches earth from the sun consists of an entire range of photon energies. As seen in Figure 3, this spectrum consists of photons with energies ranging from roughly zero to four electron volts (eV). The distribution of these photons is non-uniform and approximately matches the spectrum of a blackbody radiating at 5800 K. The result is that not all photons of light have enough energy to create an e-h pair and be absorbed into the semiconductor. The lower the bandgap of a material, the larger proportion of the spectrum that will have enough energy to be absorbed. However, if a photon with energy greater than the bandgap is absorbed, the electron is excited far above the conduction band minimum. Within the conduction band there are many allowable states, and thus the electron rapidly loses energy via phonons as it collides with the lattice over a time scale of 10^{-12} s and thermalizes down to the conduction band minimum. Thus light-generated e-h pairs will only have energy equal to the bandgap, so any photons with energies greater than E_g will have the excess energy wasted as heat.

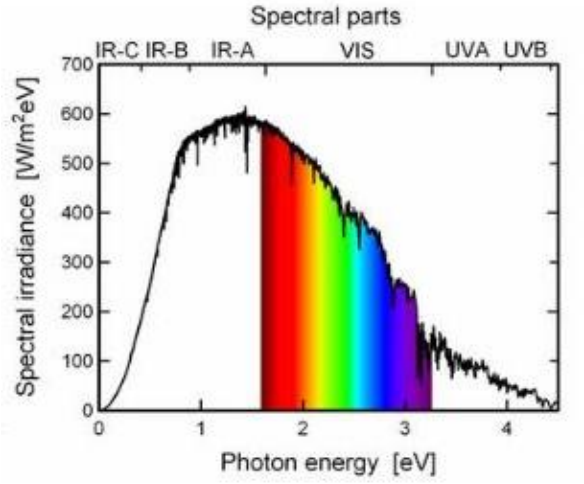

Figure 3. Extraterrestrial (AM0) solar spectrum, Adopted from [3]

Insulators have very large bandgaps, meaning that any e-h pairs that are generated will have a large amount of energy (sufficient to jump the band gap.) However, very few photons in the solar spectrum are energetic enough to create an e-h pair in this material. At the other extreme, metals do not have a defined bandgap of forbidden energies, but instead have many allowable states in their valence and conduction bands that overlap. This allows many photons of many energies to be absorbed, but without a gap between the two bands, an excited electron can easily decay to a lower energy state, transferring or losing its energy. Semiconductors have a moderately sized band gap, which strikes an important balance between there being a large proportion of the solar spectrum with enough energy to excite an electron, and those excited e-h pairs having a large amount of energy and separation so that that energy may be extracted. Figure 4 shows the band diagrams for these different material types.

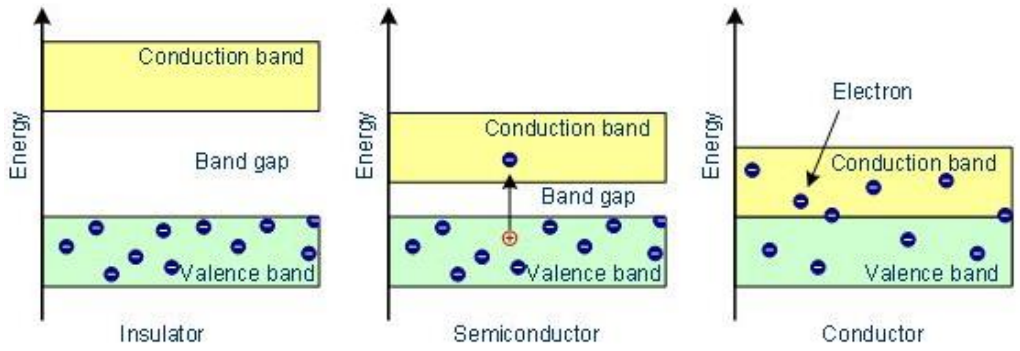

Figure 4. Bandgaps of various materials, adopted from [4]

The band structure of these materials also dictate their electrical conductivities. Due to the large bandgap of insulators, the conduction band is largely empty, and without sufficient electrons free to move, they exhibit poor conductivity. Alternatively, metals typically exhibit high conductivity because their overlapping bands allows for a cloud of unbound electrons free to conduct electrical charge. Semiconductors typically have an electrical conductivity that falls between the ranges of pure conductors and insulators. Semiconductors also have the unique property that their electrical conductivity can be greatly modified by adding trace amounts of impurities in a process known as “doping”. These unique properties are derived from a specific atomic structure where the pure semiconductor bonds to create full valence shells of eight electrons, but the addition of impurities changes the number of valence electrons and thus changes the electrical conductivity of the substance.

Semiconductors can be doped either n-type or p-type, depending on the impurity element that is added. N-type doping increases the number of electrons (negative charge) present in the lattice, and thus increases the electron conductivity of the semiconductor. P-type doping results in fewer electrons than the intrinsic semiconductor (positive charge) and similarly increases hole

conductivity. Figure 5 shows a diagram of doping in silicon where the presence of a phosphorus or boron atom dope silicon n-type or p-type, respectively.

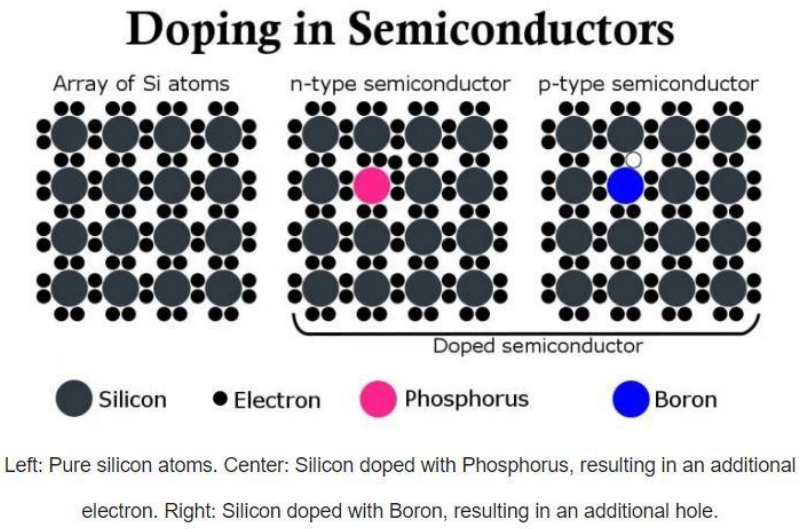

Figure 5. N and P-type doping in semiconductors, adopted from [5]

1.2 Conversion of Thermal Radiation into Chemical Energy

We have established that when a photon of sufficient energy is absorbed in a semiconductor, it generates an energetically separated set of charge carriers. An electron is excited into the conduction band, leaving behind a hole in the valence band. Under constant illumination, many e-h pairs are generated. Once a photon of light has been absorbed, an electron only remains in its excited state for a finite amount of time before it loses its energy and falls back into the valence band. This is known as “recombination” as an electron and a hole recombine and mutually annihilate. This recombination may occur through several, parallel processes. The most preferable method is known as radiative recombination. In this process, the electron spontaneously transitions to an unoccupied state in the valence band, losing its energy in a single step, emitting a photon of light with energy equal to bandgap. This process is

thermodynamically unavoidable, but because the energy transition must occur in a single radiative step, it is the slowest recombination processes and puts an upper bound on how long an excited e-h pair may survive, known as the "lifetime" [6], [7]. Since radiative recombination requires that electrons and holes interact directly with each other, the rate of radiative recombination increases as the concentration of electrons and holes increases. Finally this is the only recombination process which is reversible, with no entropy generation.

In a perfect semiconductor with no defects, the bandgap, by definition, is completely devoid of allowable energy states. In this case, radiative recombination is the only mechanism by which electrons may lose their energy. However, real materials have impurities and defects in the lattice which create states within the bandgap that facilitate the loss of energy over several steps. Known as Shockley-Read-Hall (SRH) or defect-assisted recombination, this occurs when both electrons and holes lose energy in small steps. The small energy steps may be lost to the lattice via individual phonons where it is dissipated as heat, thus no photon is emitted and this recombination is non-radiative. Additionally, because the non-radiative transition of an electron from the conduction band to the valence band via many intermediate steps requires small energy transitions — phonons typically disperse 30–50 meV — it may occur much more easily and over much shorter timescales than radiative recombination [8]. In most real materials, non-radiative recombination is the dominant mechanism and severely limits the charge carrier lifetime. One of the key objectives of solar cell design is to minimize non-radiative recombination. Non-radiative recombination may occur within the bulk of the material and at interfaces between adjoining layers, and multiple strategies may be employed to minimize it, as will be discussed later in this text. Figure 6 shows band diagrams for several prominent recombination methods. In this figure "trap-assisted recombination" is synonymous with SRH recombination. Auger recombination,

which is a non-radiative process which can become important in highly-doped direct bandgap materials [9] is a process where that includes the combination of an electron and a hole accompanied by energy transfer to another free carrier.

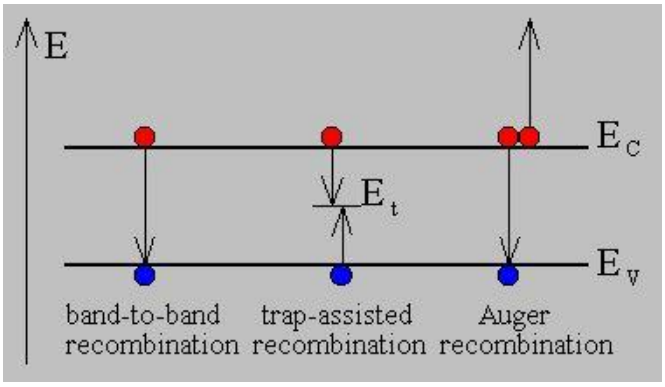

Figure 6. Band diagrams for various recombination methods, adopted from [10]

As previously discussed, the Fermi-level is a probabilistic construct which describes the energy at which there is a 50% chance of locating an electron. In semiconductors, the Fermi-level typically resides within the bandgap and an electron is therefore unlikely to actually reside at this energy. Under equilibrium conditions only one Fermi-level is allowed since only one of the bands will have any appreciable population of carriers. However, when under illumination, many e-h pairs are generated and two Fermi distributions exist— one for each band in which only one of the types of charge carrier (electron or hole) is considered. These are known as quasi-Fermi-levels (qFL.) These qFLs represent the electro-chemical potentials of electrons and holes respectively. The separation of these quasi-Fermi levels is known as quasi-Fermi-level-splitting (qFLS) and signifies the electrochemical potential available which could be extracted — known as the internal or implied voltage (iV_{OC}). Increasing the population of electrons and/or holes moves their qFL closer to their respective bands. Therefore, increasing generation,

increasing equilibrium carrier concentrations through effective doping, minimizing non-radiative recombination in the bulk and at the interfaces, and maximizing charge carrier lifetimes all result in increased qFLS. Because the iV_{OC} indicates the upper limit to the voltage that a particular absorber can produce, maximizing the qFLS within the absorber is a vital first step to producing highly efficient solar cells. A visualization of the quasi-Fermi levels may be seen in Figure 7.

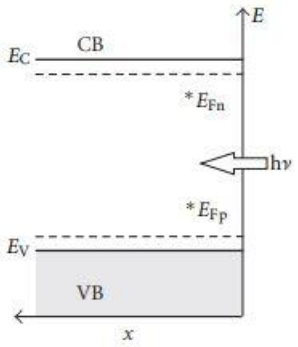

Figure 7. Quasi-Fermi levels in an absorber under illumination, adopted from [11]

1.3 Conversion of Chemical Energy into Electrical Energy

Up to this point, we have discussed how energy from thermal radiation has been converted into chemical energy inside the semiconductor through the absorption of photons to excite electrons to higher energy states. However, in order to utilize this energy, it must be extracted as an electrical current flowing through an external circuit with a voltage difference between the electron and hole terminals. This is accomplished by driving electrons and holes out of the absorber through opposite contacts to create a net flow of charge. Electrons have numerous forces which may act on them, but the most pertinent for this discussion are an electric field (gradient in the electric potential) acting on its charge, and a diffusional force (gradient in the chemical potential) acting on its quantity. These “field” and “diffusion” currents are often

discussed as if they were separate entities, as if certain electrons only "felt" the field effect and contributed only to the field current while others only "felt" the diffusional force and contributed to the diffusion current. It is important to understand that while mathematically these currents can be calculated separately and then combined, in reality the movement of charge carriers within the absorber is influenced by the combination of these forces. It is at this point the concept of a quasi-Fermi level becomes extremely helpful, as the qFL is a representation of the electro-chemical potential. Therefore, *the charge current is driven by a gradient in the quasi-Fermi level* according to Equation 1 where j_Q is the charge current density, σ_e and σ_h are the conductivity of electrons and holes respectively, e is the elementary charge, and ε_{FC} and ε_{FV} are the quasi-Fermi level energies for electrons and holes respectively.

$$j_Q = \frac{\sigma_e}{e} grad\varepsilon_{FC} + \frac{\sigma_h}{e} grad\varepsilon_{FV} \qquad (1)$$

An important implication of equation 1 is that it is true whether an electric field, or a concentration gradient, or both exist. This means that a charge current can flow in the absence of one of these forces, as long as the other is present, or it can flow as the result of the combination of them. Alternatively, there is no charge current when there is no gradient in the quasi-Fermi level. This can best be illustrated by the band diagrams shown in Figure 8 and Figure 9. Figure 8 shows the band diagram of a CdSeTe device operating in the short circuit condition. The dashed lines represent the quasi-Fermi levels for electrons (blue) and for holes (red). The gradients which can be seen in these quasi-Fermi levels indicate that a net force will drive electrons "downhill" for electrons and "uphill" for holes. This drives electrons towards the left of the diagram, the electron contact, and holes towards the right, the hole contact, creating a net flow of carriers out of the device. Under short circuit conditions, with no external resistance to the flow

of electrons and holes, the charge carrier densities within the film are reduced by the extraction of current and the qFLs is minimized. At J_{SC}, there is no difference between the electrochemical potential of electrons at the electron contact and the holes at the hole contact (note the horizontal black line) thus there is no voltage across the device and no work may be performed, despite the flow of current.

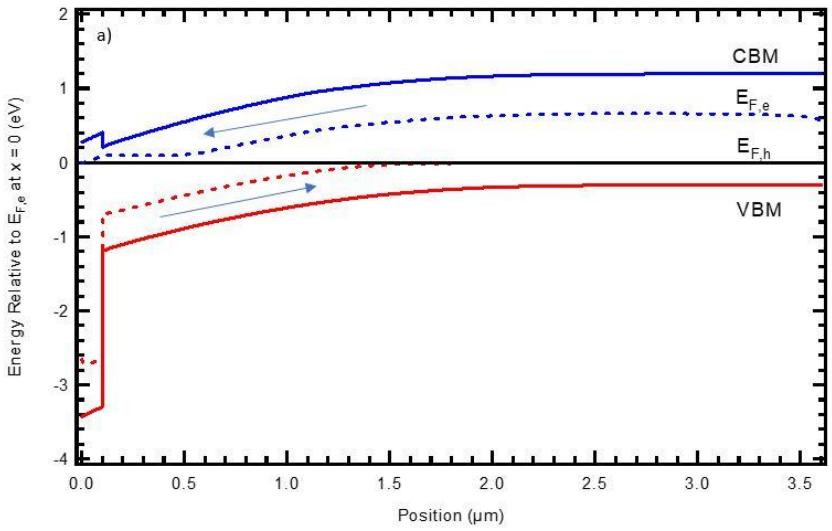

Figure 8. Band diagram of CdSeTe at J_{sc}, modelling and figure by Carey Reich

Figure 9 illustrates the same CdSeTe device under open-circuit conditions. At open-circuit the quasi-Fermi levels are flat, an indication that there is no net flow of current. Without current extraction, the populations of electrons and holes, and thus the qFLS is maximized. In this configuration, the electrochemical potentials of the electrons and holes at their respective contacts are not equal, in fact the difference is maximized, this is the V_{OC}. Note that in Figure 9, the black line is no longer horizontal, but connects two points of differing electrochemical potential. This is useful for visualizing the voltage across the device. Maximum power is extracted from a photovoltaic device at a point between the short and open circuit conditions

where the voltage is maximized without sacrificing current flow. This max power point will be discussed in more depth shortly.

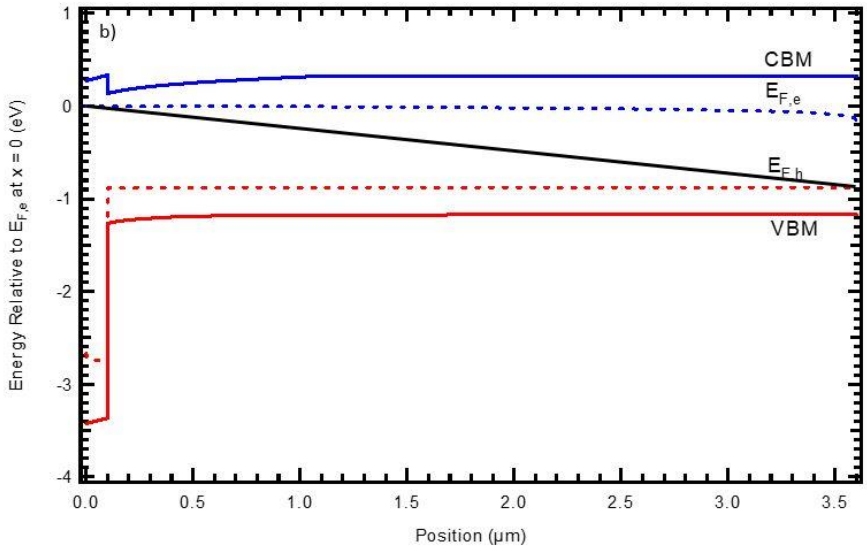

Figure 9. Band diagram of CdSeTe at V_{OC}, modelling and figure by Carey Reich

1.3.1 Charge carrier selectivity and selecting appropriate electron and hole contacts

It has now been established that the gradient of the qFL is the driving force for the motion of charge carriers. However, the magnitude of the flow down a given gradient is still determined by the material's conductivity/resistivity to either electrons or holes. An excellent contact therefore will exhibit extremely high conductivity to one charge carrier while exhibiting extremely low conductivity to the other. The ratio of partial resistances to electrons and holes is known as the selectivity of the contact. Figure 10 illustrates this. The left (hole) contact exhibits poor selectivity, as seen by the size of red rectangles being only slightly unequal. As a result, the quasi-Fermi levels of electrons and holes both converge toward the center of the bandgap at the left of the diagram. Alternatively, the right (electron) contact exhibits excellent electron selectivity. The resistivity to electrons (inverse of conductivity) is extremely small compared to

that of holes. As a result, there is only a small drop in the electron qFL at the right, while the hole qFL drastically falls due to the fact that only a very few holes are able to traverse the contact. The voltage that this device would produce is annotated in Figure 10 as "q x V" and is the difference between the electro-chemical potentials of the carriers at the contacts. This voltage is less than maximum qFLs seen in the absorber (the implied voltage) and is a direct result of voltage drop across the contact, known as selectivity losses [12]. A theoretically perfect contact would exhibit infinite resistance to one carrier, completely blocking it, and the quasi-Fermi level would show no drop across the contact. Because perfect contacts don't exist in reality, choosing/engineering materials with the proper energetic alignment and high selectivity are the primary criteria when designing a contact. The conductivity of a material to a charge carrier is the product of that carrier density and the charge carrier mobility. While the latter is considered to be a material property and not particularly mutable, the carrier density may be increased by the doping methods discussed previously.

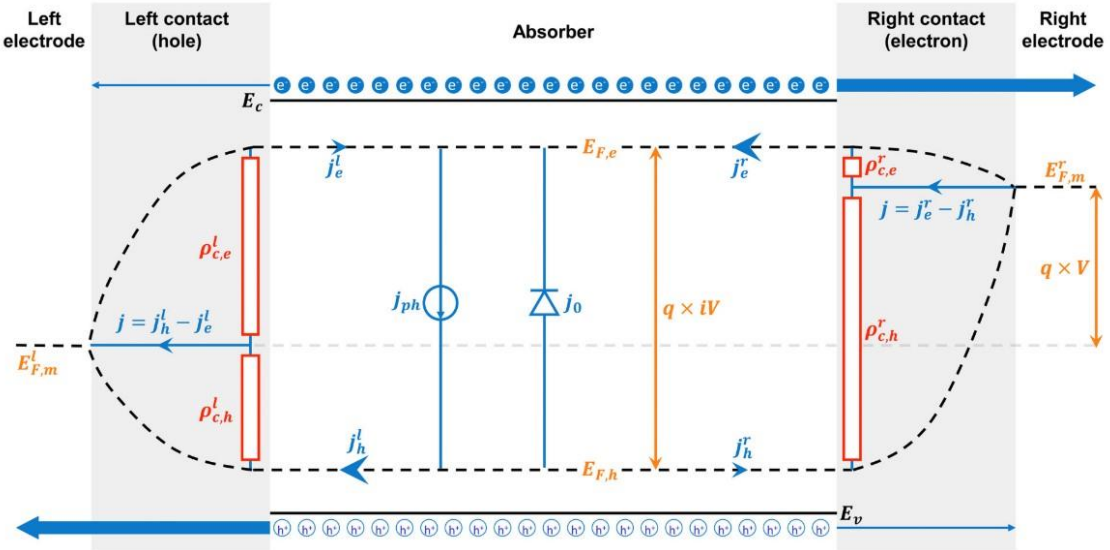

Figure 10. Diagram showing quasi-Fermi levels, the implied voltage, and contact selectivity as the ratio of partial resistivities, adopted from [12]

1.3.2 P-N Junctions

Traditional PV device structures achieved asymmetrical carrier conductivities and selectivity through the use of a p-n junction. A p-n junction is formed when two semiconductors, one doped n-type and one doped p-type are fused together. The n-type material has a large number of free electrons, and the p-type has a large number of holes. When these materials are joined, a large density gradient is formed between the two sides of the junction. The result is that some of the electrons will begin to diffuse towards the P side of the junction. When the electrons diffuse, they leave behind positively charged ion cores which are fixed in the crystal lattice right at the junction. Similarly, holes will diffuse towards the N side, leaving behind negatively charged ion cores. Figure 11 illustrates the resulting configuration. The ion cores that are left behind create an electric field between them which opposes the diffusion of electrons and holes. The electrons and holes continue to diffuse until this electric field is strong enough to repel any additional charge carriers. This electric field is known as the built-in potential. The region formed within this electric field is known as the depletion region or depletion width because any charge carrier that diffuses into it is quickly repelled, and thus the region is virtually depleted of free carriers, compared to the material far from the junction.

P-N junctions were foundational to the first functioning solar cells, and are still the basis of many solar technologies today. However, we know that the electric field is not the only force which must be considered for carrier motion. Indeed, a functioning photovoltaic device may be constructed without a p-n junction or an electric field present [13]. Therefore viewing photovoltaics solely through the p-n framework forms an incomplete picture. P-N junctions are effective because they facilitate the separation of e-h pairs. Furthermore, the high concentration of only one carrier on each side of the junction inherently creates carrier-selectivity by creating a

high ratio of conductivities. State of the art solar cells incorporate well-engineered doping profiles and carefully selected contact materials to ensure that both diffusional and electrical forces work to maximize qFLs and carrier selectivity.

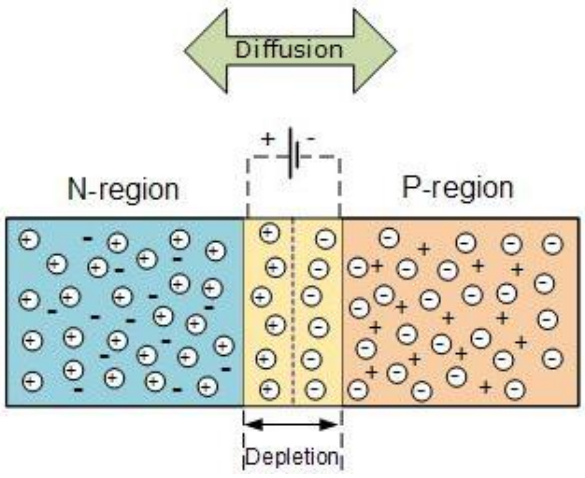

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Figure 11. Diagram of a p-n junction, adopted from [14]

1.4 Photovoltaics as Diodes

It has already been established that when a p-n junction is formed, electrons and holes diffuse, creating a depletion region at the junction with an electric field that opposes the flow of additional carriers. If the entire structure is subjected to a negative bias (where the n-side is biased positively and the p-side is biased negatively), electrons are attracted toward the positive electrode and away from the junction, at the same time, holes are attracted to the negative electrode and away from the junction. The lack of electrons and holes widens the depletion width, and because the depletion width is highly insulative due to the lack of free carriers, it acts similar to the dielectric layer within a parallel plate capacitor. When this dielectric layer widens, the barrier is increased, as is the amount of energy a carrier would need to move across the

depletion width. Alternatively, if the structure is subjected to a positive bias, the depletion width shrinks as the electrons and holes are pushed towards the junction. The external bias pushes the carriers, giving them energy to cross the depletion width. At a certain point, the barrier is sufficiently reduced and no longer prevents the flow of carriers. This creates what is known as a p-n junction diode, where an external bias can be used to either block or allow the flow of current. This diode only allows current to flow in one direction, and unlike with a resistor, the current does not vary linearly with voltage. Instead, the current-voltage curve exhibits exponential behavior according to Equation 2:

$$I = I_o \left[e^{\frac{qV}{nkT}} - 1 \right] \qquad (2)$$

Where I is the current, I_o is the dark saturation current, q is the elementary charge, V is the applied voltage, n is an ideality factor, k is the Boltzmann constant, and T is the absolute temperature. Figure 12 displays a typical diode IV curve that behaves according to the diode law expressed in Equation 2.

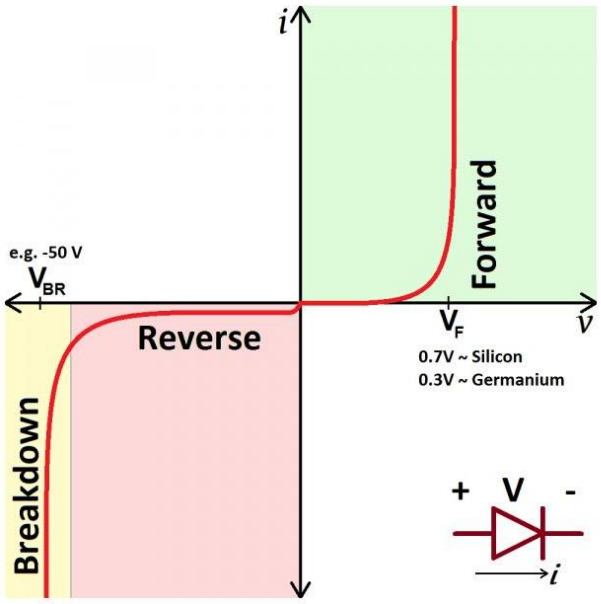


Figure 12. Typical diode IV curve, adopted from [15]

In order to appreciate a photovoltaic device operating as a diode, and the efficiency of photovoltaic energy conversion, it is first necessary to understand several parameters of the diode curve. When combined, these parameters are used to calculate the electrical power that is produced by a photovoltaic device. When the electrical power produced and the incident power of sunlight are both known, the photovoltaic conversion efficiency can be calculated. An e-h pair is generated when light with energy greater than or equal to the bandgap is incident upon the semiconductor. These carriers are known as light-generated carriers. Due to the electric field present at the junction, the electrons are swept to the N side while the holes are swept to the P side of the semiconductor. Under short-circuit conditions, there is no build-up of charge, as the carriers are allowed to leave the device without resistance and exit as light-generated current. This current is commonly known as I_{sc}, the short-circuit current. When this current is divided by the device's physical area, the current density (J_{sc}) is the result. If the current is prevented from leaving the device, light-generated electrons and holes that are generated in the depletion width

are swept to the N and P sides of the junction, respectively, and the total number of electrons on the n-side and holes on the p-side increases. This separation of charges creates an electric field that is in opposition to the one existing inside the depletion width and has the effect of reducing the net field. As previously discussed, the depletion region electric field was acting as a barrier to carrier diffusion and when it decreases, carrier diffusion increases. At some point, the diffusion current is equal to the light-generated current, so that the net current is zero, known as open-circuit condition. The forward bias required to reach open-circuit conditions is known as the open-circuit voltage (V_{OC}). Figure 13 shows a standard current density vs voltage (JV) curve with the I_{sc} and V_{OC} annotated.

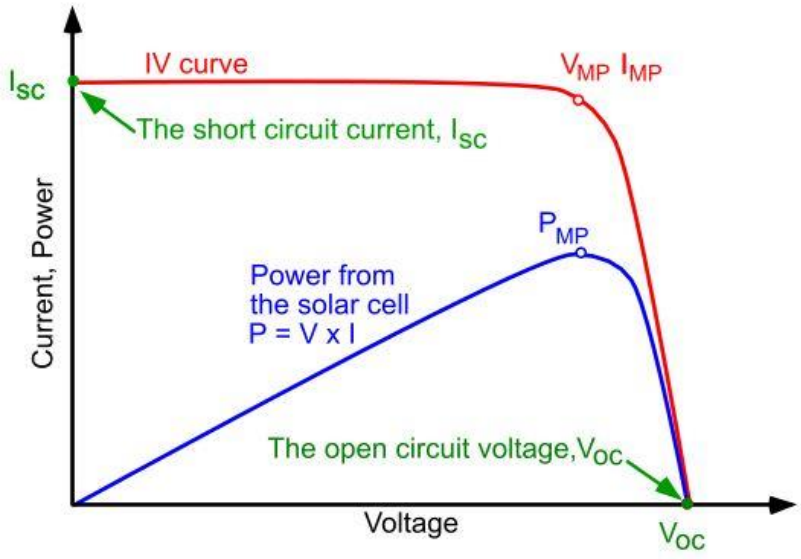


Figure 13. JV curve showing key PV parameters, adopted from [16]

The electrical power produced by the solar device is simply the product of the current and the voltage. Looking at Figure 13, it can be seen that for most of the voltage range, the current is nearly constant. The very slight negative slope is due to the increase in diffusion current which is

counteracting the light-generated current. Near V_{OC}, the current drops drastically, down to zero at the open circuit point. When the power is plotted, it becomes obvious that the maximum power produced from a solar cell is produced at a point just prior to open circuit voltage. While sweeping upward in voltage, this is the last point where the gains in voltage outweigh the loss in current in the power calculation. This is known as the maximum power point or voltage (V_{mp}). A solar cell under illumination is operating under a forward light bias, and is ideally operating near the max power point. The final parameter is known as the fill factor (FF) and is related to the V_{mp}. In a perfect diode, the current would remain perfectly horizontal all the way up to the open-circuit voltage. At V_{OC}, the curve would make a sharp ninety-degree turn and point straight down. The area under the curve would be a perfect rectangle and the V_{mp} would equal the V_{OC}. Real diodes do not behave perfectly, and the JV curve has slope to it, and the "knee" of the curve is rounded. The fill-factor measures the "squareness" of the JV curve, and is a measure of the quality of the diode. FF can be calculated with:

$$FF = \frac{P_{max}}{P_T} = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \qquad (3)$$

Where I_{mp} is the current at maximum power and P_T is the theoretical power of a perfect diode. With these three parameters, it is now possible to calculate the efficiency of photovoltaic conversion denoted with the Greek symbol eta (η). Like most efficiencies, η is defined as power out divided by power in. In this instance, the input power is from the incident light. The efficiency can be calculated using the following equation:

$$\eta = \frac{V_{mp}I_{mp}}{P_{in}} = \frac{V_{oc}I_{sc}FF}{P_{in}} \qquad (4)$$

1.5 Common Characterization Techniques

Although the photovoltaic conversion efficiency is an extremely important feature of a solar cell, as a single number, it does not explain why the value is what it is, or how it could be improved. Fortunately there are multiple optical and electrical characterization methods that provide useful insight into the performance of a PV device. Several common techniques are listed here because the results from these tests will be referred to extensively, but note that this is by no means an exhaustive list, and dozens of additional characterization methods exist in addition to those presented here.

1.5.1 Current Density vs Voltage

The current density vs voltage (JV) measurement is a simple test that reconstructs the diode curve of the solar cell in operation. A device of known area is mounted onto a testing apparatus with electrodes connected to the front and back contacts as shown in Figure 14. The device is then illuminated using a standardized light source at 1000W/m^2 with an AM1.5 spectrum at 25°C [17]. While illuminated, the short-circuit current for the device is measured. The bias across the contacts is slowly swept across the range from short-circuit to open circuit, with current measurements taken at set intervals. Once complete, The V_{OC}, J_{sc}, and FF, are all known, and since the input power is also known, the conversion efficiency can be calculated using Equation 4. In addition to these values, the series and shunt resistances of the device can be calculated using the slopes of the curve, as shown in Figure 15.

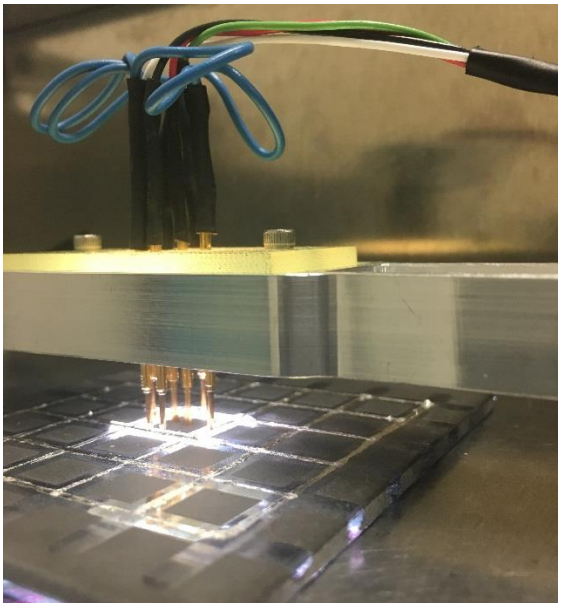


Figure 14. CdTe substrate in CSU's JV tester

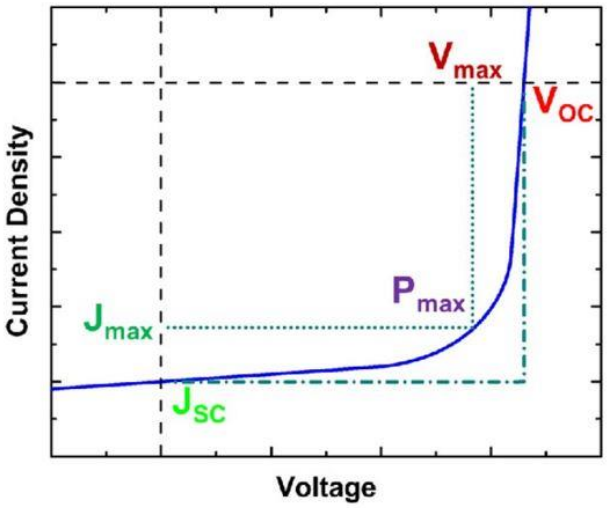


Figure 15. Diagram illustrating the effects of changing series & shunt resistance, adopted from [18]

1.5.2 Steady-State Photoluminescence and Cathodoluminescence

Steady-state photoluminescence is a method designed to indirectly gauge the presence of defects by measuring the amount the radiative vs. non-radiative recombination. To perform the

measurement, the sample to be tested is loaded onto a stage where it can be illuminated. A light source, commonly a laser with photon energy greater than the bandgap of the sample is steadily shone on the sample. Photons emitted from the sample are detected by a spectrometer and the spectrum is recorded. A series of short and long-pass filters are used to ensure that the excitation laser light is not included in the measurement. A sample setup is shown in Figure 16 and a diagram showing several radiative transitions as well as non-radiative recombination is shown in Figure 17 below. The resulting spectrum is a nearly Gaussian distribution centered on the bandgap energy of the sample, similar to those shown in Figure 18. Additional peaks may be present, usually associated with a shallow defect that cause longer wavelength photon emission. A common interpretation of this characterization method is that for a steady-state light input, as the number of defects and non-radiative recombination sites decrease, the proportion of radiative recombination will increase, and the PL peak height will increase. The total photoluminescence of a sample, determined by the integrated PL spectra, is closely related to the External Radiative Efficiency (ERE), a concept that will be discussed momentarily. Cathodoluminescence (CL) is performed similarly to PL, with the exception that electrons are used to excite the emission of photons, rather than light.

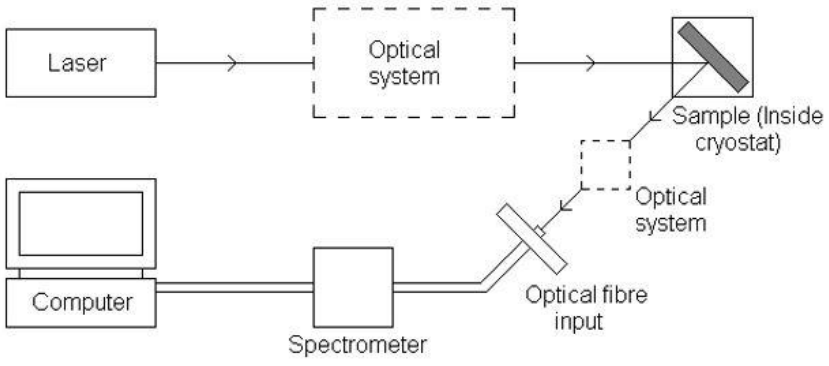


Figure 16. Experimental setup for measuring steady-state photoluminescence, adapted from [19]

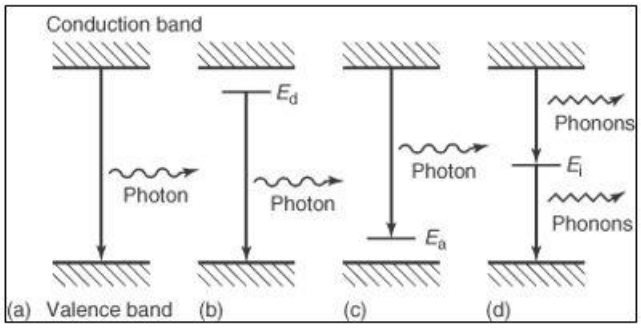


Figure 17. Diagram of radiative and non-radiative recombination, adapted from [20]

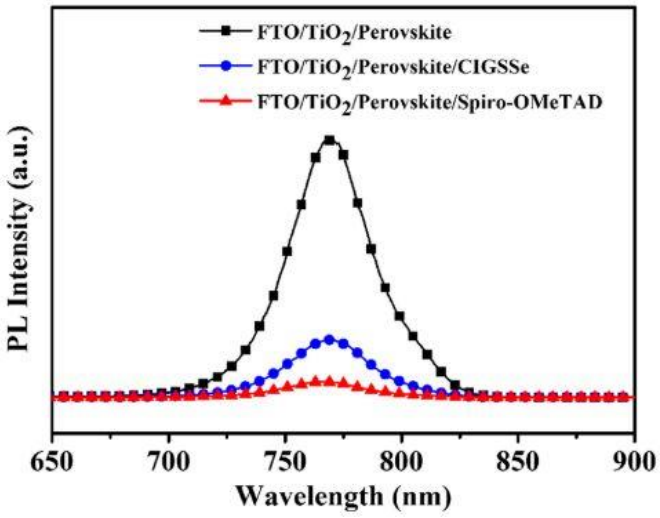


Figure 18. Steady-state PL spectra, adopted from [21]

1.5.3 External Radiative Efficiency

External Radiative Efficiency (ERE) measurements have only recently been adopted and reported by the CdTe community as a method of evaluating the potential of device structures to produce increased voltage [22], [23]. The ERE is the ratio of photons that are emitted through the illuminated surface to the number of incident photons when a photovoltaic sample is illuminated. It is a measure of the number of recombination events which are radiative, and because non-radiative recombination reduces the quasi-Fermi level splitting, ERE is crucial for determining the true maximum voltage possible from an absorber. The quasi-Fermi level splitting may be

described by the implied voltage (iV_{OC}=qFLS/q with q the elementary charge); the voltage which a photovoltaic absorber is capable of producing with perfectly selective contacts [24]. A photovoltaic device can never extract a voltage greater than that represented by the potential difference between the electron and hole quasi-fermi levels. Because quasi-fermi level splitting is improved by increasing bulk minority-carrier lifetime, increasing doping, and decreasing grain boundary and interface recombination, it is a powerful tool for not only indirect measurement of these other parameters, but can also quantify the impact that changing these parameters has on the device's potential to produce a greater open-circuit voltage. Figure 19 illustrates the experimental setup for ERE measurements presented in this work.

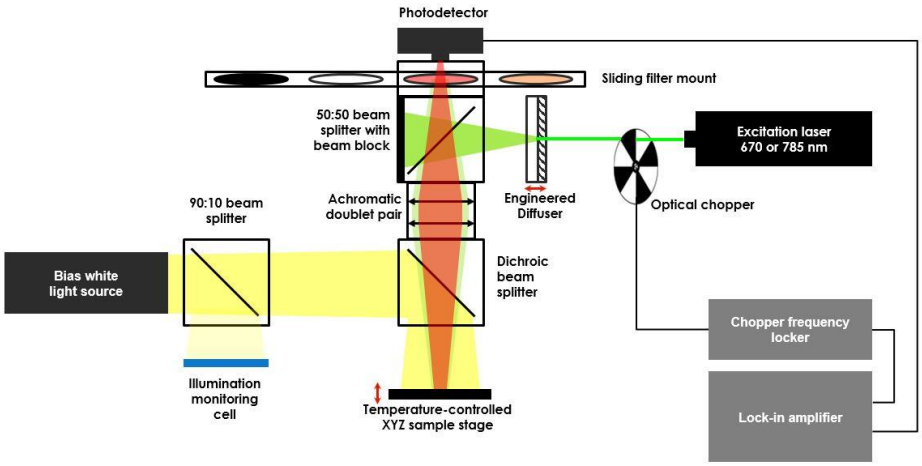


Figure 19. Experimental setup for measuring external radiative efficiency (ERE), figure by Arthur Onno

The ERE contributes to the implied voltage according to Equation 5, where $V_{OC,rad}$ is the radiative recombination limited voltage, about 1150 mV in CdTe [25], k_b is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. Most PV technologies currently exhibit very low ERE values, far below 1%. CdTe, for example, had previously been reported with an ERE of 0.0001% [26].

$$iV_{OC} = V_{OC,rad} - \frac{k_b T}{q} |\ln(ERE)| \qquad (5)$$

Finally, a general trend has been observed, that as ERE and iV_{OC} increase, regardless of technology, the voltage deficit generally decreases. Figure 20 shows the ERE and voltage deficit values for many technologies, and the resulting trend line that shows the beneficial effect of improving the ERE. Two definitions for voltage deficit exist: either the difference between the radiative recombination limited voltage and the open circuit voltage, or difference between the bandgap divided the elementary charge and the open circuit voltage, as in Figure 20.

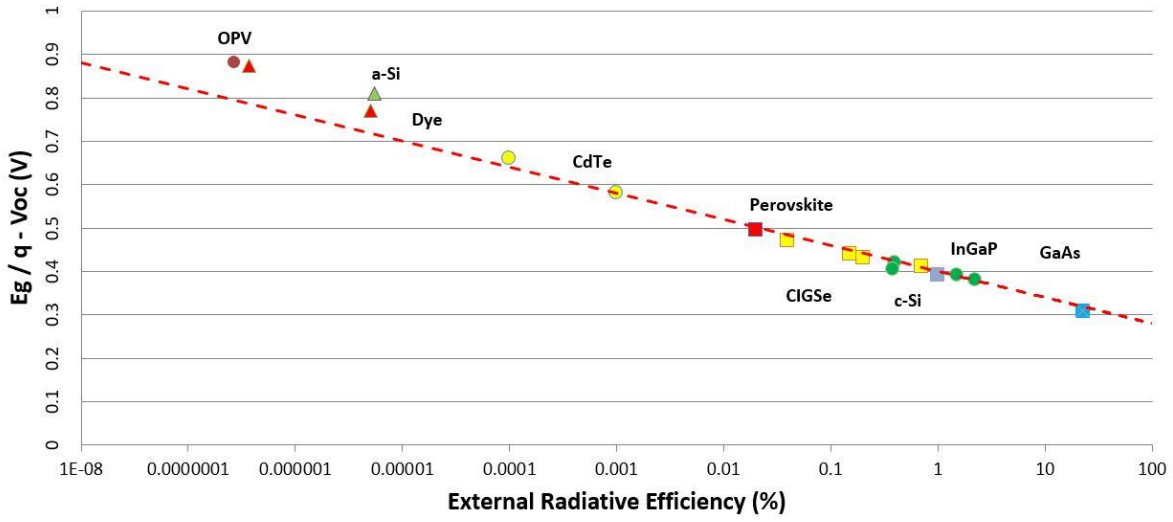


Figure 20. Voltage deficit vs external radiative efficiencies for various photovoltaic technologies, adapted from [27]

1.5.4 Time-Resolved Photoluminescence

Although the information gleaned from steady-state photoluminescence is extremely valuable for understanding defects and sources of recombination, there is some information that is not available from spectral data alone. The minority-carrier lifetime of photovoltaic devices can be measured through the use of Time-Resolved Photoluminescence (TRPL.) During a TRPL

measurement, a sample is mounted inside a sample holder that has optics to deliver laser light to the sample, and to capture emitted light and transfer it to a detector. A femtosecond laser generates pulses of light that strike the sample. For single-photon TRPL, an optical parametric amplifier is used to ensure that the wavelength of laser light is adjusted so the photon energy is greater than the bandgap of the material in the sample. The laser light strikes the sample, where e-h pairs are generated. A fraction of these carriers radiatively recombine and photoluminescence occurs.

Utilizing a setup such as shown in Figure 21, the goal is to measure the amount of photoluminescent light as a function of time. Unfortunately, this decay occurs incredibly quickly, ranging from a few hundred picoseconds to several hundred nanoseconds [28]. Most electronics are unable to resolve time steps of such small magnitude. Additionally, the signal being measured is phenomenally small, sometimes just a single photon. Therefore, a single photon counting system is used to measure the individual photons that luminesce over many excitation cycles as the laser pulses. A histogram is built which aggregates this data and an exponential decay curve such as those shown in Figure 22 can be fit. This fitted decay provides the minority-carrier lifetime for the material. This is the average lifetime of a charge carrier before recombination occurs. Defects which mediate recombination tend to lower the carrier lifetime, and thus lowers the likelihood that the charge carrier will survive long enough to be extracted as usable energy. High lifetimes therefore are an excellent indication of material quality and both bulk and interface passivation.

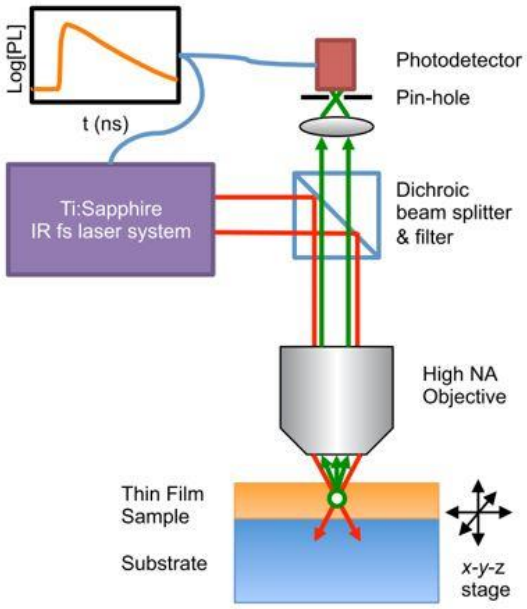


Figure 21. Experimental setup for measuring time-resolved photoluminescence, adopted from [29]

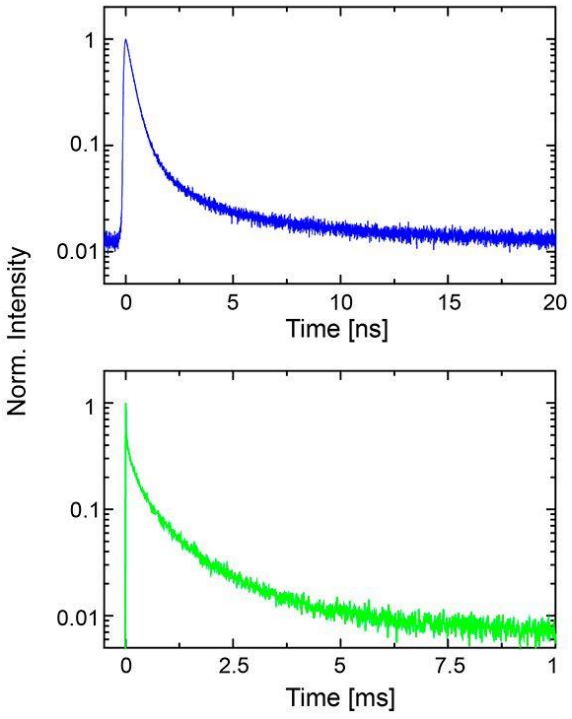


Figure 22. TRPL decay curves for GaAs (Top) and Si nanodots (Bottom), adopted from [30]

Because the laser light energy is greater than or equal to the bandgap, it can be expected that the material will have a high absorption coefficient and most of the laser light will be absorbed (and most of the TRPL data generated) near the surface of the sample. To probe deeper into the sample, two-photon TRPL is used. The process is similar to the single-photon case, with the exception that two lasers, or a single converging beam, with sub-bandgap light is used. The two lasers may be angled towards each other so that their beams converge at a desired depth within the sample. Because the photon energy is below the bandgap, carriers can only be excited if they absorb multiple photons simultaneously. This process is highly dependent upon the photon flux [29], and so excitation can be generated primarily inside the focal volume.

1.5.5 Capacitance vs Voltage and Capacitance vs Frequency

When a p-n junction is formed, the diffusion on electrons and holes creates a depletion region where there are essential no free carriers. With no free carriers, the depletion width is far less conductive than either the n or p-type material on either side. This configuration is analogous to a parallel plate capacitor [6] where the capacitance is governed by

$$C = \frac{\varepsilon A}{W} \qquad (6)$$

Where C is the capacitance, ε is the dielectric constant of the material between the parallel plates, A is the area, and W is the width of the capacitor. When a Capacitance vs Voltage (CV) measurement is performed, an impedance analyzer sweeps the bias exerted on the device which changes the depletion width and in turn changes the capacitance of the junction according to Equation 6. This change in capacitance as a function of bias can be used to calculate the carrier concentrations and built-in field strength for a device. The carrier concentration has historically been reported as the value at either the "belly" of the curve in the case of a U shaped-profile, or

at the zero-bias point. Ideally, these points would overlap, but this is not always the case for CSU-fabricated devices or CdTe in general.

Capacitance-Frequency (CF) measurements take advantage of the fact that different trap states within a lattice have the ability to fill and empty at different speeds. A DC bias is pulsed at frequencies typically ranging from 1kHz to 10MHz [31]. Because different trap states become active at different frequencies, the number of free carriers will change as the frequency is swept. This will in turn change the capacitance. For this reason, a flat CF profile is usually indicative of a defect-free material or electrically inactive defects. Figure 23 shows the CF, Mott-Schottky Plot (From which a CV plot is derived), and doping density vs distance (CV) curves for a typical CdTe device fabricated at CSU.

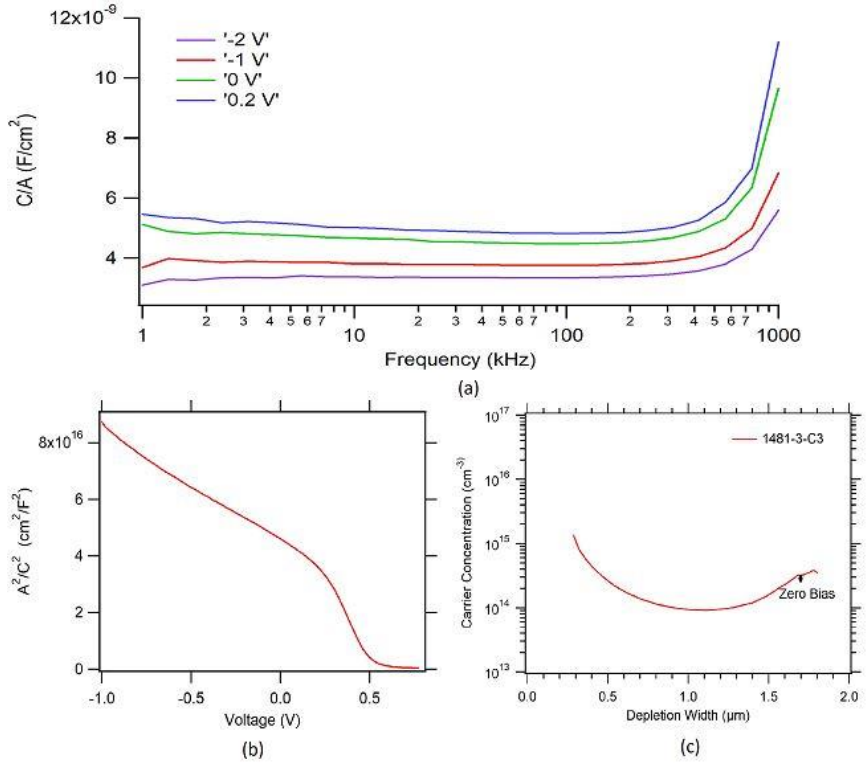


Figure 23. (a) CF Plot, (b) Mott-Schottky Plot, and (c) CV profiles for a CdTe device at CSU

1.5.6 External Quantum Efficiency

The quantum yield, or quantum efficiency (QE) of a device is a measure of how many electron-hole pairs are produced and extracted per incident photon. It provides a useful method of measuring the photocurrent from a device and can often be used to identify losses which are reducing the J_{sc} [32]. These losses can be optical, such a reflection from the front glass, or absorption in the Transparent Conducting Oxide (TCO), or they can result from recombination losses. QE can be further divided into EQE, the External Quantum Efficiency, or the IQE, the Internal Quantum Efficiency. EQE is defined as the ratio of electrons collected by the solar device to the number of incident photons. The IQE, by contrast, only counts the photons that are absorbed by the solar cell, not accounting for things like reflection losses.

The quantum efficiency of a device is measured as a function of incident light wavelength. This is because not only is the absorption of light in a material non-constant with wavelength, but different loss mechanisms can become prevalent at different points in the spectrum. The device to be measured is isolated from outside light sources and illuminated with chopped monochromatic light, usually generated via monochrometers or interferometers. The photocurrent is converted to an AC voltage and measured with a lock-in amplifier [33]. The wavelength of light is swept over the appropriate range for the absorber material but is typically between the range of 300 and 1300 nm. By integrating the area under the curve, the J_{sc} can be calculated. In well-behaved devices, there should be good agreement between the J_{sc} calculated via this integration method and the J_{sc} that is measured in a JV measurement. Additionally, an electrical bias may be applied to the device during the QE measurement, because the electrical losses may be affected by the changing bias, but the optical losses will not, the two loss sources may be deconvoluted in this way. Finally, because the QE of a device will be zero for all photons

with energy less than the bandgap, the QE curve often displays a sharp drop off, or band edge. This can be useful for verifying the bandgap of the material, especially with graded films like the CdSeTe/CdTe absorbers discussed in this work. Figure 24 and Table 1 below show a QE curve for a Cu(InGa)Se_2 solar cell along with the current losses and their associated loss mechanism.

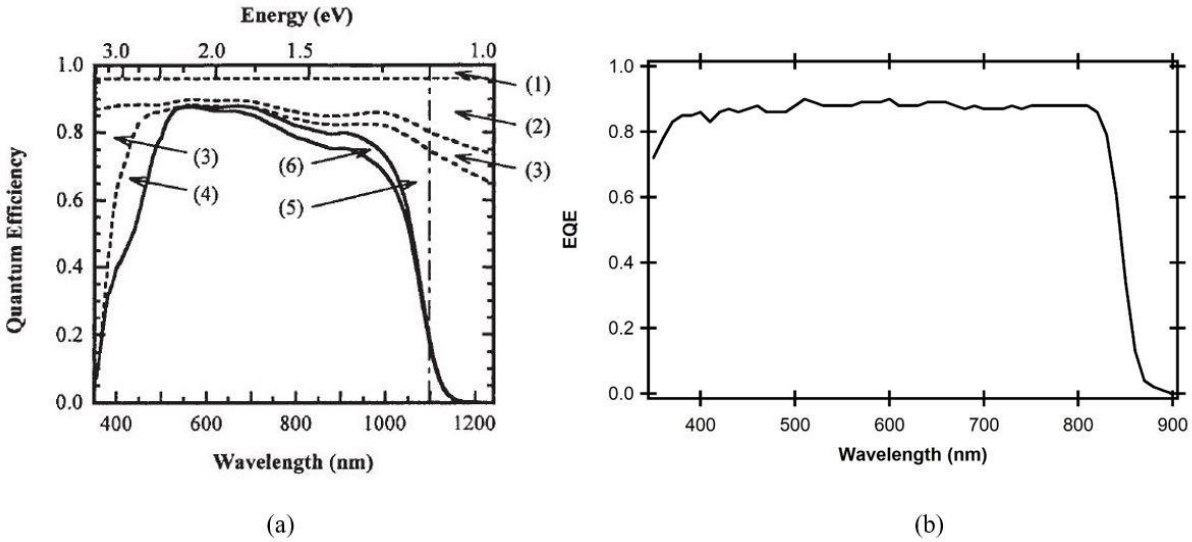


Figure 24. (a) EQE curve for a Cu(InGa)Se_2 Solar Cell, adopted from [18]. (b) EQE of a baseline CdSeTe/CdTe device fabricated at CSU

Table 1. Current losses in a Cu(InGa)Se_2 device as measured by QE, adopted from [18]

Region in Figure 3	Optical loss mechanism	ΔJ (mA/cm^2)	$\Delta J/J_{tot}$ (%)
1	Shading from grid with 4% area coverage	1·7	4·0
2	Reflection from Cu(InGa)Se_2/CdS/ZnO	3·8	8·9
3	Absorption in ZnO	1·9	4·5
4	Absorption in CdS	1·1	2·5
5	Incomplete generation in Cu(InGa)Se_2	1·9	4·4
6	Incomplete collection in Cu(InGa)Se_2	1·0	2·3

CHAPTER 2. THE NEED FOR SOLAR ENERGY

2.1 World Energy Needs

Throughout our history, humans have exhibited a virtually uninterrupted trend of extracting and harnessing ever increasing amounts of energy from our environment. In 2018, the world consumed 18.6 TW-yr of energy [34]. Energy use is increasing in every region of the planet, as seen in Figure 25, with the greatest increases occurring in Asia. The United States Energy Information Agency predicts that this trend will continue until at least the year 2040, with total energy demands growing by 28% by that time, as indicated in Figure 26.

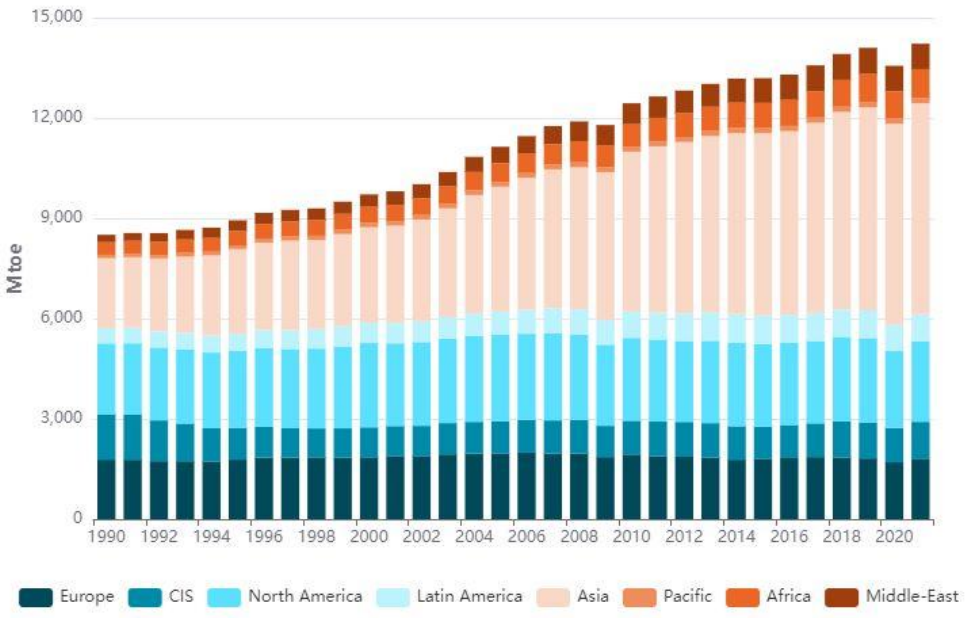


Figure 25. World energy consumption by year in millions of tons of oil equivalent (MTOE) adopted from [34]

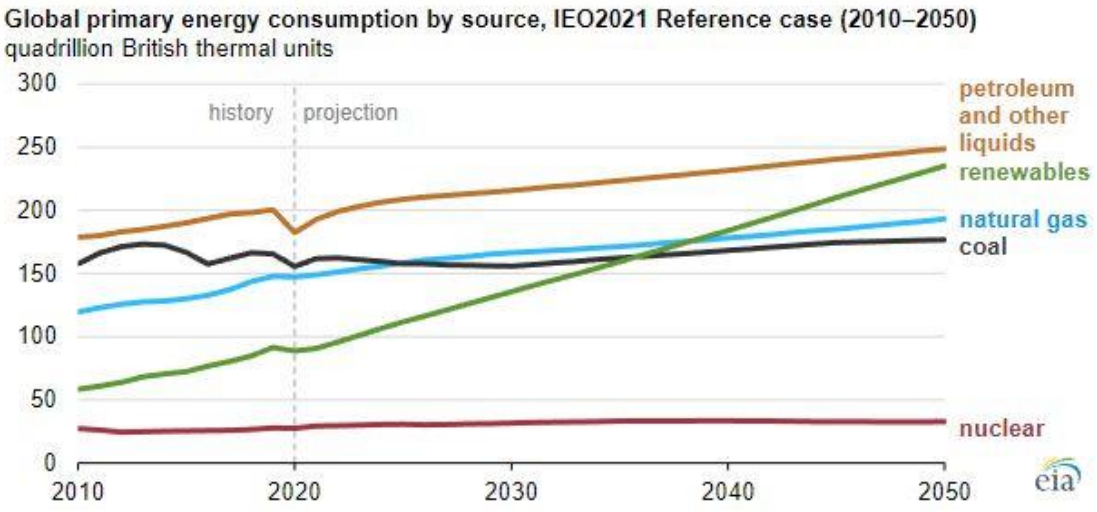


Figure 26. World energy consumption by energy source (2010–2050), adopted from [35]

At first glance, this increasing trend in energy usage may seem discouraging. As the science behind global climate change becomes better understood (as will be discussed shortly), many individuals and organizations have strove to reduce anthropogenic greenhouse gases (GHG), and yet these predictions indicate that humans' yearly contribution to the problem will get worse before it gets better. This is why it is imperative that virtually all of the new demand for energy, as well as the vast majority of existing demand be met by renewable sources. There are however, notable benefits to increasing energy usage. Stern *et al* found a very strong positive correlation between a nation's energy usage and its Gross Domestic Product (GDP) as shown in Figure 27. Additionally, the World Gallup poll consistently notes a strong positive correlation between the per capita GDP of a nation and the reported satisfaction of that nation's citizens with their lives; a sample from the 2006 Gallup Poll is provided as Figure 28 below. Considering these two plots, it is reasonable to conclude that increasing energy use is an important factor in stimulating economic growth, which in turn is a contributor to people's subjective level of

happiness. The goal therefore should not be to stop the expansion of energy use, but rather to ensure that that energy comes from a suitable source.

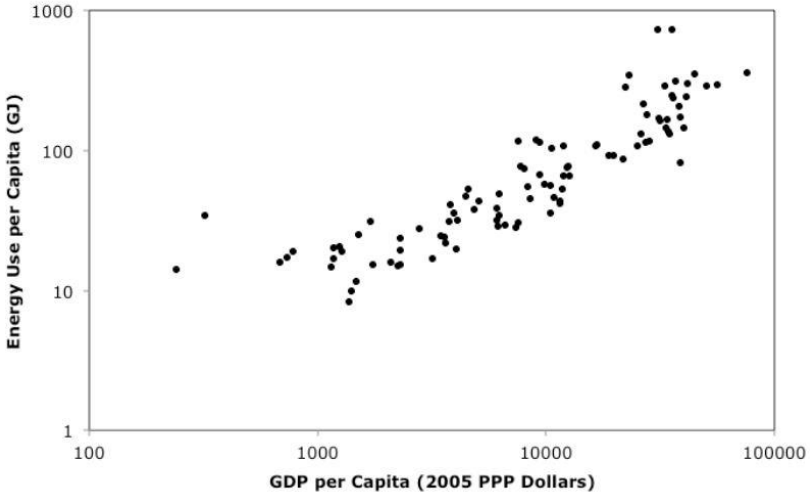


Figure 27. Energy use vs GDP, adopted from [36]

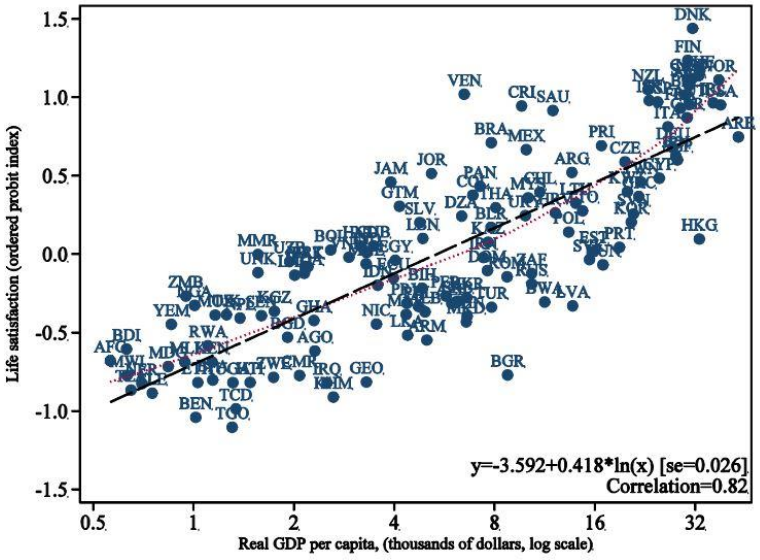


Figure 28. Life satisfaction vs GDP, adopted from [37]

In order to meet this growing demand for energy, it is first necessary to look at the world's energy reserves, to determine which energy sources even have the potential to meet the demand. Using a useful infographic, Figure 29 compares the magnitude of world energy usage to both the reserves of final energy sources such as coal, natural gas, and uranium, and the potential annual energy yield for several renewable sources, including solar.

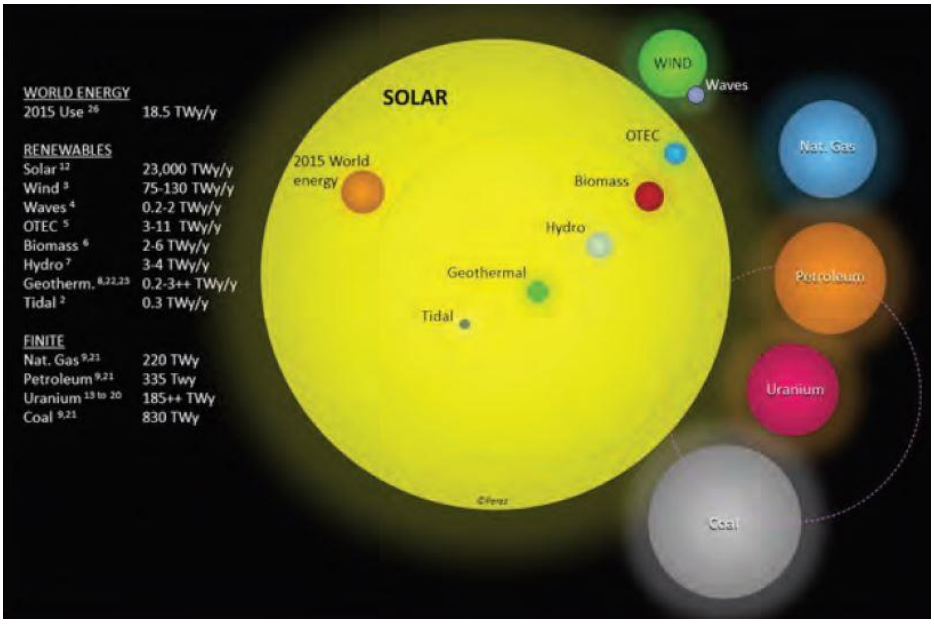


Figure 29. Comparison of energy resources & global energy consumption, adopted from [38]

Upon inspection of Figure 29, a few things become immediately apparent. First, is the astounding amount of solar resources the Earth has in comparison to any other energy source. Harnessing just 0.1% of the incident solar energy is enough to meet all of today's world energy needs. Many of the other renewable resources, while excellent for contributing to energy generation, are simply too limited in supply to serve as realistic sources for 100% renewable energy. Secondly, is that the world energy usage is now a sizable proportion of the world's non-renewable resources. Even when combining all known reserves of non-renewable energy

sources, the world will deplete these sources in about a century at current rates. While the exact amount of time is debatable, and estimates may increase or decrease based on many factors, the amount of time which the world has to use these resources is finite.

But what if fossil fuel sources were not limited? Indeed, new reserves are continually being discovered, and new technologies such as horizontal drilling and fracking enable the extraction of resources that were previously uneconomical to harvest. Even if unlimited fossil fuels were a reality, the world needs to shift from the burning of hydrocarbons to renewable sources because of another factor that far outweighs the fuel availability: Global climate change caused by anthropogenic greenhouse gasses.

2.2 Global Climate Change

In regard to global climate change, there are two primary questions that need to be addressed: Is the climate changing, and is human activity contributing to the change? Many climate change deniers claim that Earth's climate is always changing, and that we can therefore discount any evidence that human activity is worsening the problem. It is, however, true that Earth's climate naturally changes. Small, but predictable changes in Earth's orbit around the sun change the amount of energy the planet receives, resulting in a cyclical climate pattern, as shown in Figure 30 for the past 800,000 years. In this figure, one can see the pattern of "ice ages" where the global temperature drops, interspersed by warmer interglacial periods. As the Earth enters an ice age, ice builds up, primarily in the Northern Hemisphere, covering large areas of both ocean and land. This "locks" huge amounts of carbon dioxide (CO_2) into the permafrost, preventing it from releasing into the atmosphere. Because of this phenomenon, ice core samples show that the concentration of atmospheric CO_2 is also cyclical, and correlates very strongly with global

temperature changes.

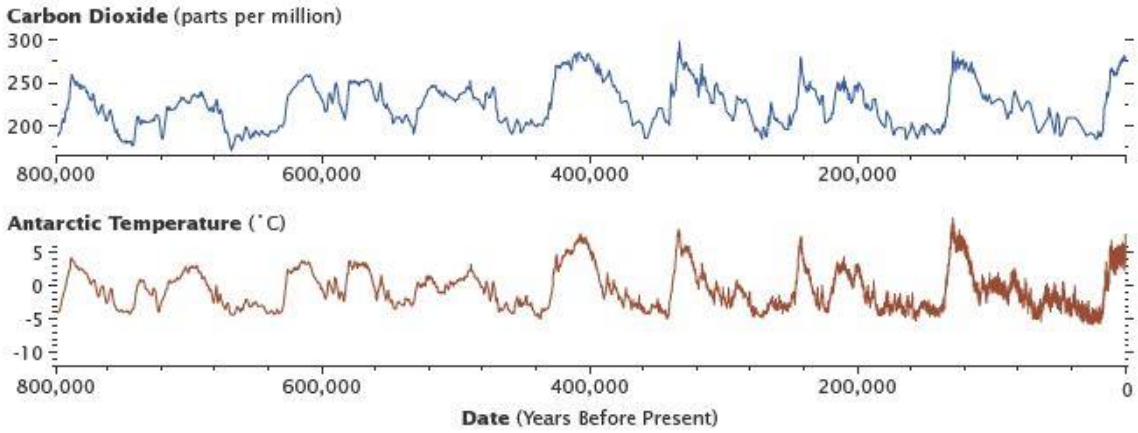


Figure 30. Atmospheric CO_2 and temperatures, adopted from [39]

The release of CO_2 into the atmosphere not only correlates with the increase in global temperature, it also causes it. This is because CO_2, along with methane, ozone, and several other gasses, known as "greenhouse" gasses, reduce the amount of energy that is transmitted back into space. Figure 31 shows the infrared emission of the earth overlaid with the emission spectra of a blackbody at 280K.

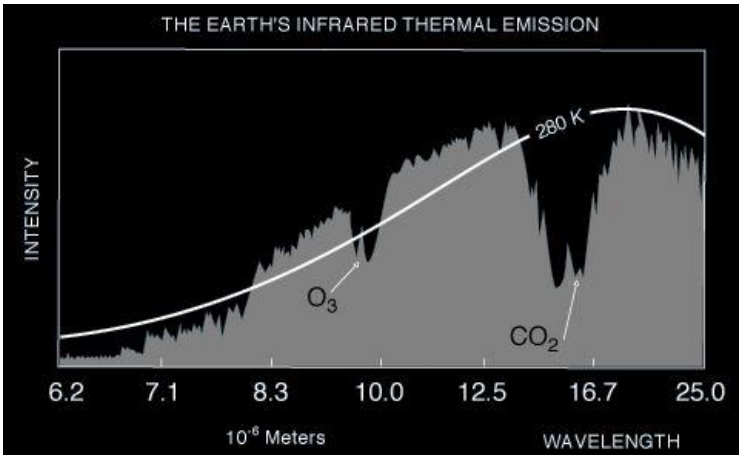


Figure 31. Earth's infrared emission spectrum compared to a 280 K blackbody, adopted from [40]

The areas identified as CO_2 and O_3 show a drastic reduction in emission as compared to the blackbody. These are the emission bands where the respective molecules are highly absorptive, and they prevent the energy within the bands from being transmitted into space. As the concentration of these greenhouse gasses increase, less energy is released into space, causing the Earth to warm. At this point, it is simply a heat transfer problem (albeit a complicated one.) The earth will continue to warm, and as it does its thermal radiation will increase until its emission matches the incoming solar power and a new equilibrium temperature is reached.

While it has been shown that the Earth's CO_2 concentrations and temperatures do fluctuate naturally, the measurements for these metrics from the last few decades exceed what can be explained by natural variation. For much of Earth's recent history (800,000 years) shown in Figure 32, the CO_2 concentration varied between 150 and 300 parts per million (ppm). Figure 33 again shows the CO_2 concentration, but includes zoomed in data for the last few decades, where we see a nearly asymptotical rise in CO_2. This rise continues, and as of June 2022, the atmospheric CO_2 concentration is 419 ppm [41].

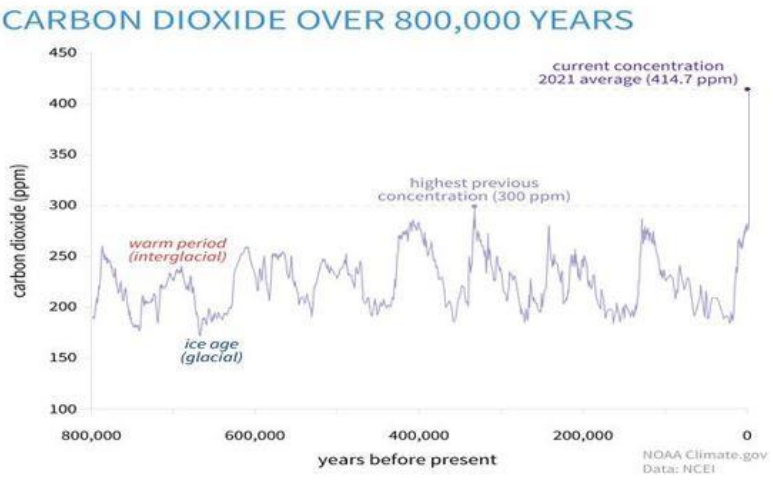


Figure 32. Historic and current atmospheric CO_2 concentration, adopted from [42]

Along with the rise in CO_2 concentrations, the recent global temperature measurements shown in Figure 33 exhibit a similar and alarming rise. Here, the temperature and CO_2 are overlaid, to better illustrate the connection between the two.

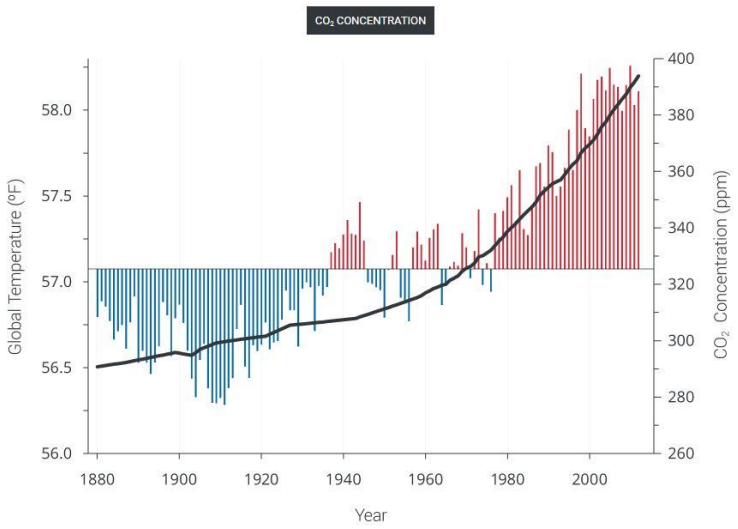


Figure 33. Global temperatures and CO_2 by year, adopted from [43]

A final, poignant indicator of global climate change can be seen in the increase in weather events that cause at least a billion dollars in damage in the United States. While this data is specific to the United States, the trend is found everywhere in the world to varying degrees based on the weather events each region is prone to. Figure 34 shows that these events have steadily risen since 1980. It should be noted that these values are CPI-adjusted, and thus cost inflation has been accounted for. In this plot, the bar graphs represent the number of individual climate events which have occurred while the line graphs show the associated costs. As the Earth continues to warm, draughts, floods, hurricanes, blizzards, and tornadoes are becoming and will continue to become more prevalent and more destructive.

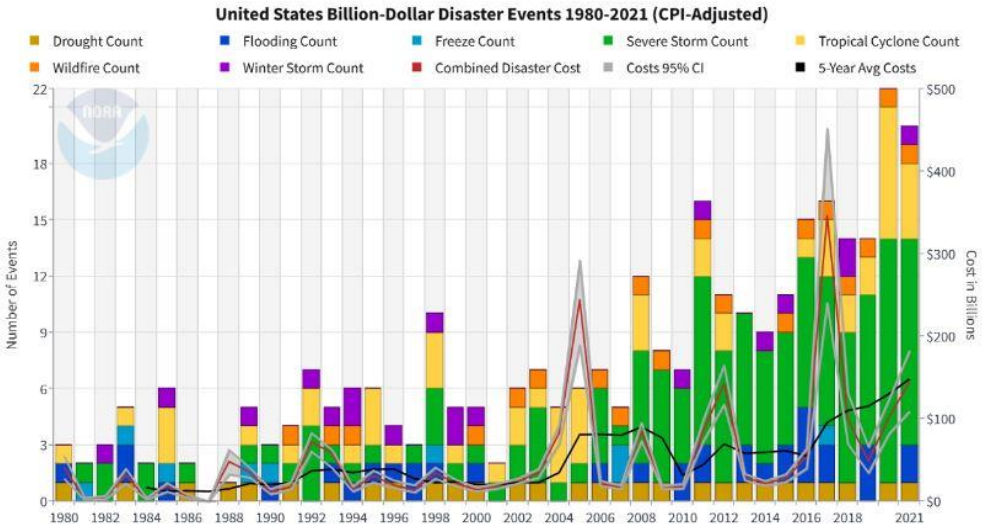


Figure 34. Billion dollar disasters and costs per year, adopted from [44]. The bar graphs represent the number of individual climate events which have occurred while the line graphs show the associated costs.

The question as to whether the climate is changing has been answered: a definitive yes. The amount of atmospheric carbon dioxide is increasing at rates that exceed the historical norms. The increased concentrations of CO_2 and other greenhouse gasses are "closing the window" on the Earth's thermal spectrum, blocking radiation from leaving the atmosphere and insulating the Earth. The next step is determining where the greenhouse gasses are coming from. Figure 35 shows the global CO_2 emissions over the last several centuries. A substantial rise in emissions began with the industrial revolution, accelerated during the post WWII global population boom and continues today. Table 2 shows the current atmospheric concentrations of several greenhouse gasses, along with the annual change.

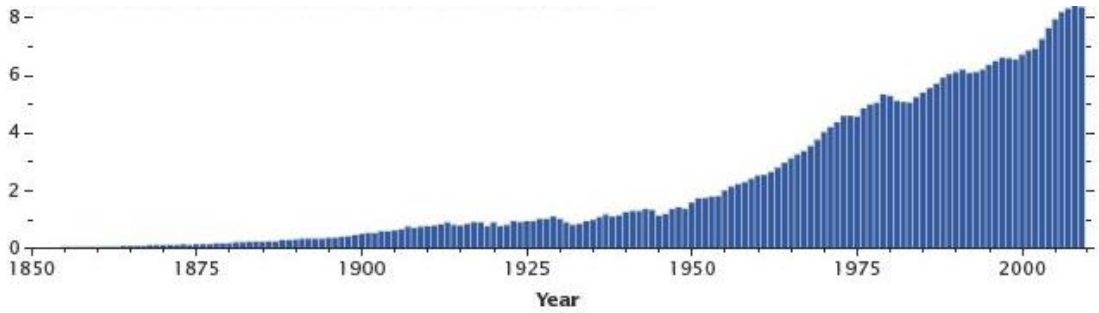


Figure 35. Global carbon dioxide emissions (gigatons of carbon per year, adopted from [45]

Table 2. Atmospheric concentrations of greenhouse gasses, adopted from [46]

Atmospheric Variable	CO_2	CH_4	N_2O	SF_6	CF_4
Pre-industrial atmospheric concentration	280 ppm	0.730 ppm	0.270 ppm	0 ppt	40 ppt
Atmospheric concentration	414 ppm[a]	1.879 ppm[b]	0.333 ppm[c]	10.27 ppt[d]	85.5 ppt[e]
Rate of concentration change	2.32 ppm/yr[f]	7.91 ppb/yr[f,g]	0.97 ppb/yr[f]	0.32 ppt/yr[f]	0.81 ppt/yr[f]
Atmospheric lifetime (years)	See footnote[h]	11.8	109[i]	About 1,000[j]	50,000

[a] The atmospheric CO_2 concentration is the 2020 annual average at the Mauna Loa, HI station (NOAA/ESRL 2021a). The global atmospheric CO_2 concentration, computed using an average of sampling sites across the world, was 412 ppm in 2019.
[b] The values presented are global 2020 annual average mole fractions (NOAA/ESRL 2021b).
[c] The values presented are global 2020 annual average mole fractions (NOAA/ESRL 2021c).
[d] The values presented are global 2020 annual average mole fractions (NOAA/ESRL 2021d).
[e] The 2019 CF_4 global mean atmospheric concentration is from the Advanced Global Atmospheric Gases Experiment (IPCC 2021).
[f] The rate of concentration change for CO_2 is an average of the rates from 2007 through 2020 and has fluctuated between 1.5 to 3.0 ppm per year over this period (NOAA/ESRL 2021a). The rate of concentration change for CH_4, N_2O, and SF_6, is the average rate of change between 2007 and 2020 (NOAA/ESRL 2021b; NOAA/ESRL 2021c; NOAA/ESRL 2021d). The rate of concentration change for CF_4 is the average rate of change between 2011 and 2019 (IPCC 2021).
[g] The growth rate for atmospheric CH_4 decreased from over 10 ppb/year in the 1980s to nearly zero in the early 2000s; recently, the growth rate has been about 7.91 ppb/year (NOAA/ESRL 2021b).
[h] For a given amount of CO_2 emitted, some fraction of the atmospheric increase in concentration is quickly absorbed by the oceans and terrestrial vegetation, some fraction of the atmospheric increase will only slowly decrease over a number of years, and a small portion of the increase will remain for many centuries or more.
[i] This lifetime has been defined as an "adjustment time" that takes into account the indirect effect of the gas on its own residence time.
[j] The lifetime for SF_6 was revised from 3,200 years to about 1,000 years based on recent studies (IPCC 2021).
Source: Pre-industrial atmospheric concentrations and atmospheric lifetimes for CH_4, N_2O, SF_6, and CF_4 are from IPCC (2021).

To better understand the CO_2 sources, this emission can be further broken down by industrial sector and fuel type, as shown in Figure 36. This data comes from the United States, but the proportions will be similar for most modernized nations. This figure makes several things immediately clear: First, the two primary sources of CO_2 emissions are from burning fossil fuels for electrical generation and transportation. Secondly, we can see that petroleum products make up virtually all of the transportation emissions, while coal and natural gas constitute almost all of

the electrical power emissions. These two sectors account for nearly 72% of the U.S.'s greenhouse gas emissions. Replacing the fossil fuels in these sectors with non-emitting renewable sources like photovoltaics will slow the accumulation of carbon in the atmosphere and has the potential to stop global climate change.

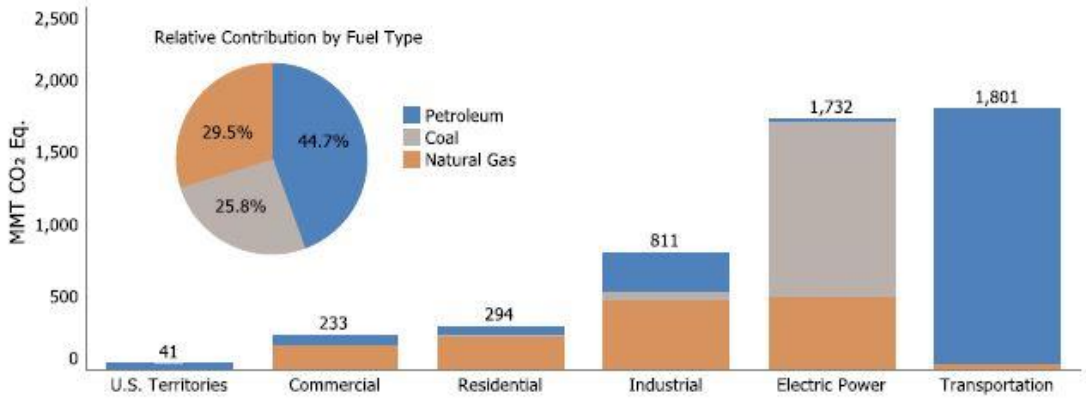


Figure 36. Relative contribution of CO_2 emission by industrial sector and fuel type, adopted from [46]

The first sector to be significantly influenced by massive installations of renewable energy is the electric power generation sector. As will be discussed shortly, global solar installations are rapidly rising all over the world, with a large proportion of that capacity being in utility-scale PV fields providing electricity directly to the grid. Figure 37 and Figure 38 reveal the first signs of large scale renewable energy penetration into the electrical grid. They show a steady decline in GHG emissions from electric power production beginning around 2007 and continuing to present. Because the other sectors are relatively stable, this results in an overall decrease in GHG emissions. This reduction can largely be attributed to the installation of PV and wind powered generation, and the replacement of coal by natural gas power plants.

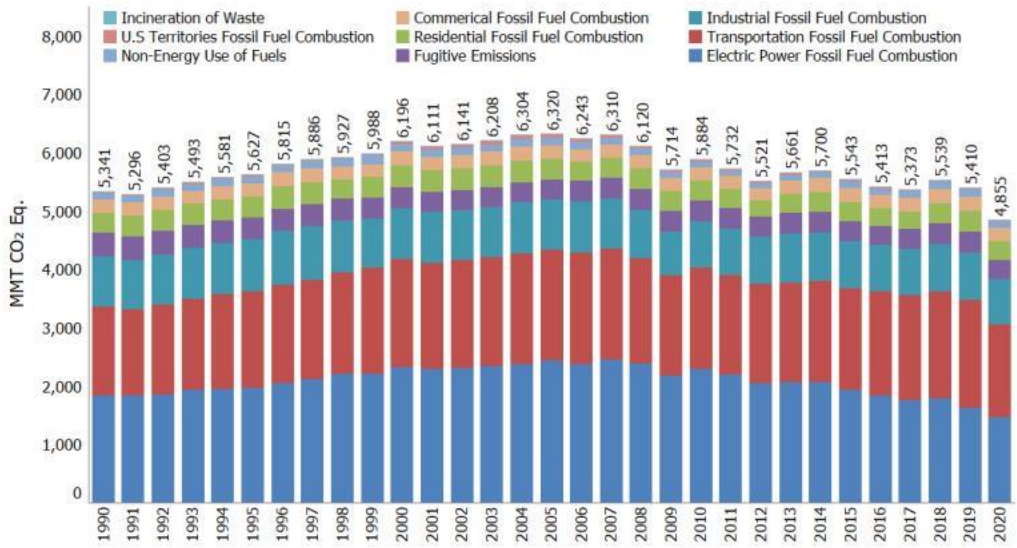


Figure 37. U.S. greenhouse emissions by sector, by year, adopted from [46]

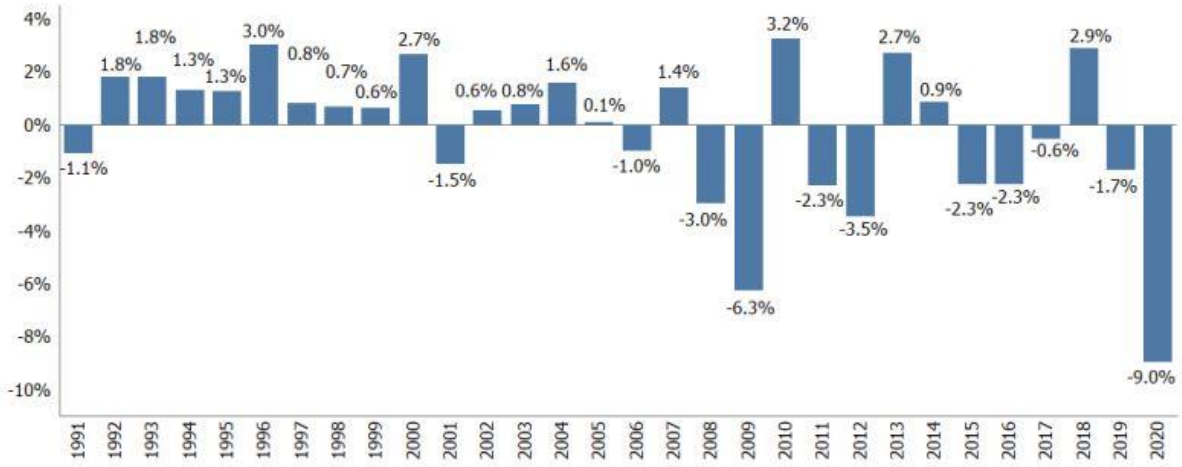


Figure 38. Percent change per year, U.S gross greenhouse gas emissions, adopted from [46]

Since 2005, when U.S GHG emissions peaked, the current trend has been towards decreasing emissions, particularly from electric power production, which has brought U.S emissions back down to 1990 levels. While this is encouraging, stopping climate change will require further reductions. It should be noted that the significant -9.0% reduction in GHG emissions seen in 2020 was overwhelmingly due to the COVID-19 pandemic and the resulting

economic slowdown. Since 2020, emissions have largely returned to pre-2020 levels[47]. The size of the required reductions make it necessary to reduce emissions not only in the electrical power production sector, but the other sectors as well. The transportation sector is responsible for approximately as much GHG emission as the power production sector. Fortunately, with advancing technology, the electrification of the transportation fleet seems likely in the near future. At least 10 nations currently have electric car sales targets and of these, at least 4 have committed to 100% zero-emission vehicles by mid-21st century [48], [49]. Using an electric vehicle offers only a moderate environmental benefit if the electricity that powers it is generated using fossil fuels. As, however, the electrical generation moves towards zero-emission sources, the benefit of electric vehicles will only increase.

2.3 The Growth of Photovoltaics

By 2020, global PV installations exceeded 700 GW [50]. This accounts for more than 3% of the global energy demand. While this seems like a relatively small proportion, it is necessary to put this number into historical context to understand the explosive growth of PV. In 2000, there was less than 1 GW of global installed PV capacity [51]. Beginning in the early 21st century, PV began an exponential growth rate as seen in Figure 39. This growth has been fueled by year after year increases in annual installations, illustrated in Figure 40, amounting to an astounding 24% compound annual growth rate from 2010 to 2017 [52].

The Chinese market accounts for just under half of all global PV installations, with India, The United States, The European Union, and Japan collectively accounting for another 37%. However, numerous countries are rapidly expanding their PV portfolio, and 32 countries currently have at least 1GW installed PV [53].

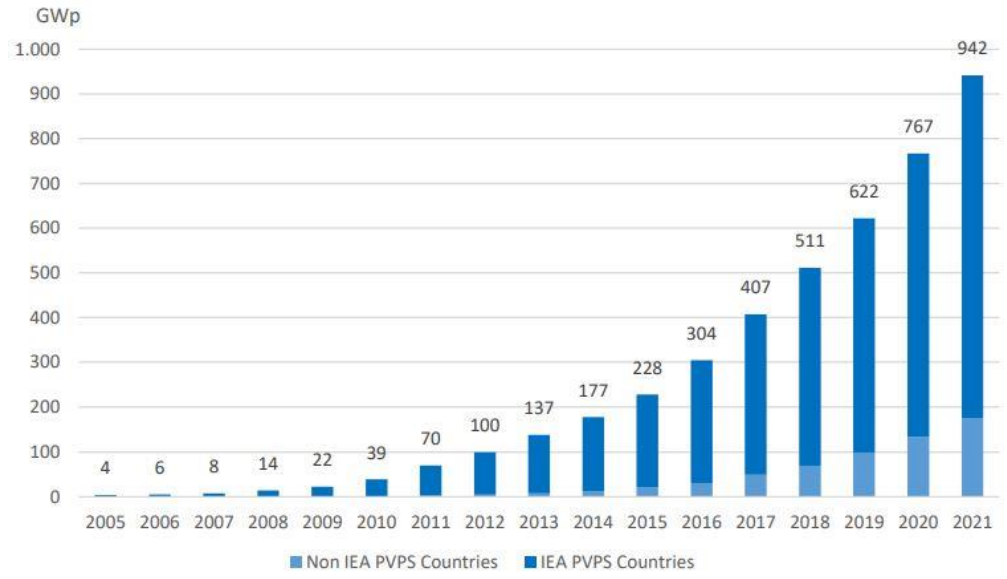


Figure 39. Global PV capacity, adopted from [54]

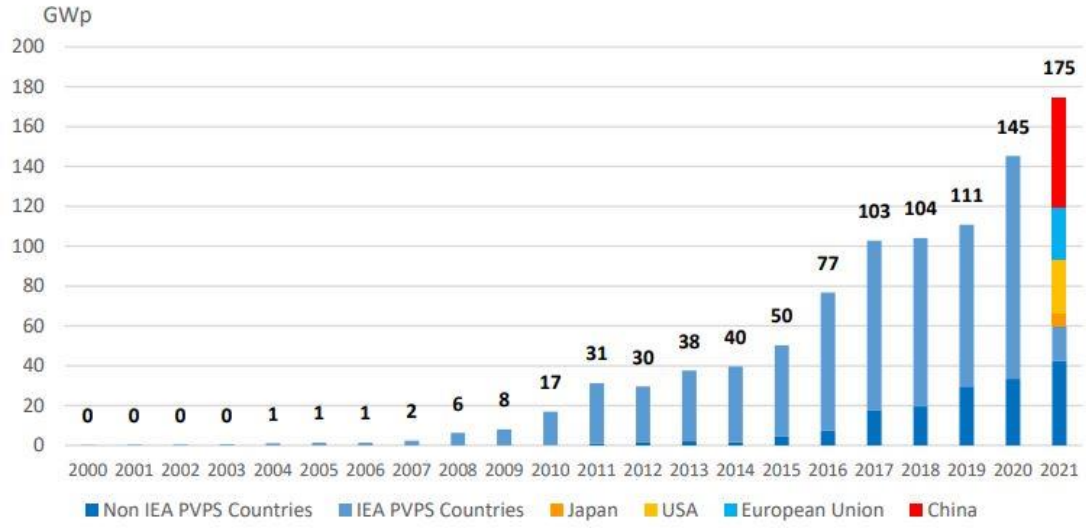


Figure 40. Annual PV installations worldwide, adopted from [54]. The country-specific breakdown is only applicable for the 2021 data, all other years are broken up between IEA and non-IEA countries

The PV market is largely dominated by the crystalline silicon PV technology, which holds approximately 95% of the total market share. Silicon has the benefits of having been

studied for several decades more than most other PV technologies due to it being the original PV technology. Additionally, silicon has been extensively studied for its uses in computing and personal electronics, and much of the learning developed there is transferable to a PV application. Most of the remaining 5% of the market is supplied by thin-film PV, primarily Cadmium Telluride (CdTe), Copper-Indium-Gallium-Selenium (CIGS), and amorphous Silicon (a-Si), of which CdTe has the largest annual production capacity at approximately 9 GW/yr, and is expected to grow to 15 GW/yr within 2 years [55]. CdTe currently accounts for approximately 40% of U.S. utility-scale photovoltaic installation [56].

Several factors have driven the phenomenal growth of photovoltaics over the past decade. Firstly, as more people are exposed to the evidence of global climate change presented in this chapter, and become convinced of its seriousness, the political pressure for local, state and national governments to act has increased. Figure 41 and Figure 42 show examples of this from the United States, where both cities and states with official renewable energy commitments are shown. Additionally, concerns about the long-term availability of non-renewable sources and unrest in geopolitically sensitive areas where much of the fossil fuel is located has encouraged the search for other alternatives. However, the single most impactful factor in stimulating the growth of PV worldwide has been economic.

Powered by 100% Renewable Energy: These communities have currently achieved their 100% clean, renewable electricity targets.

Committed to 100% Renewable Energy: These communities have made community-wide commitments to transition to 100% clean, renewable electricity by no later than 2050.

Figure 41. American cities with a 100% renewable energy commitment, adopted from [57]

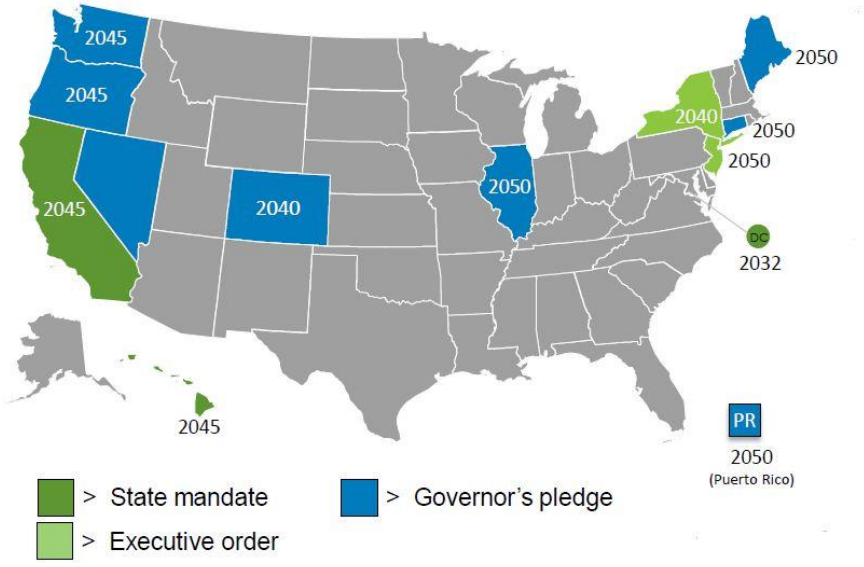


Figure 42. American states with 100% renewable energy commitments, adopted from [57]

2.4 The Falling Cost of Solar

As the solar market has experienced its rapid expansion, the cost of manufacturing, installing, and operating PV has undergone an equally astounding decrease. The average American household currently pays $0.13 per kilowatt-hour (kWh) [58], while worldwide, citizens of most nations pay between $0.08 and $0.33/ kWh [59]. By comparison, Power Purchase Agreements (PPA) for electricity produced via PV are routinely signed by utility companies around the world for less than $0.03/kWh and recently the Las Angeles Department of Water and Power approved a 400MW PPA at a world-record $0.013/kWh [60]. Figure 43 shows the falling cost of PV electrical production compared to growing global installations.

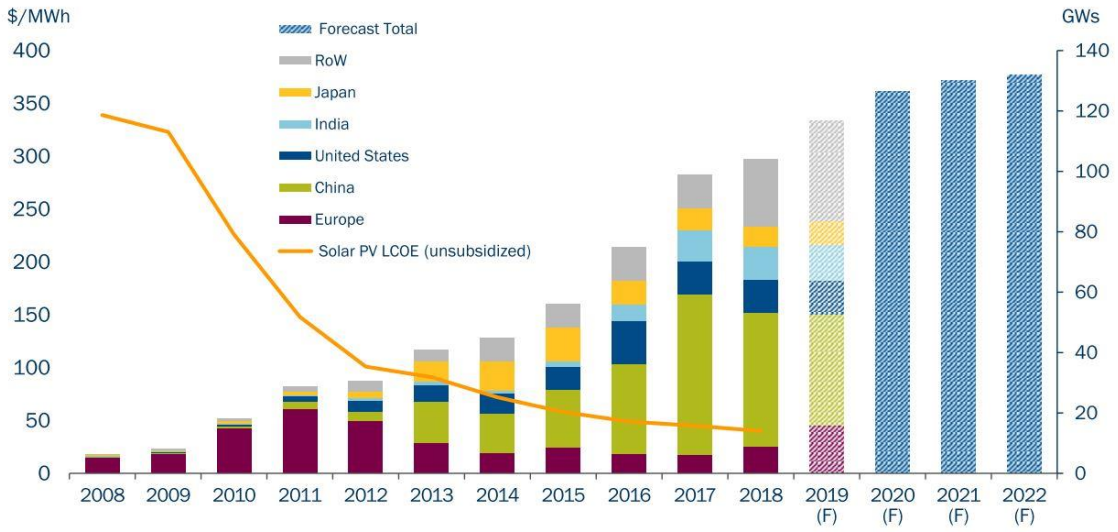


Figure 43. PV cost vs global installation, adopted from [61]

While this is the price paid by the power distribution utility company, and not the price paid by the end consumer, it is drastically cheaper than conventional fossil fuels, where the production costs from natural gas are between $0.07 and $0.10/kWh and from coal are between

$0.07 and $0.14/kWh in the United States [62]. Figure 44 compares the costs of numerous electricity sources, both conventional and renewable.

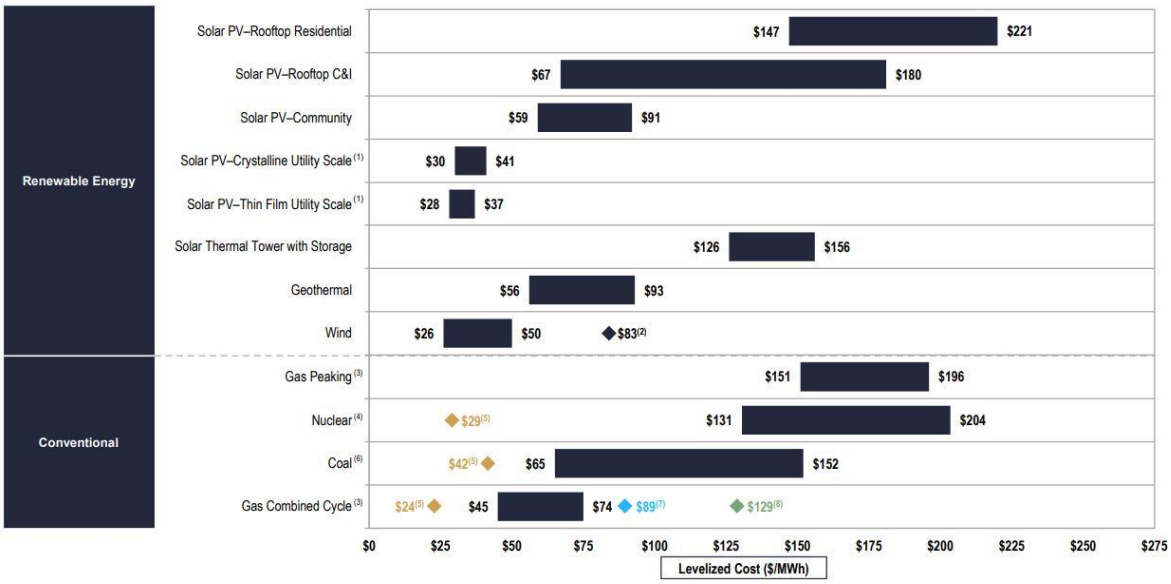


Figure 44. U.S. levelized cost of energy (LCOE), adopted from [63]

This figure uses a metric known as the Levelized Cost of Energy (LCOE). The LCOE accounts for the initial capital costs of installing an energy source, the costs for fuel, maintenance and financing throughout the life of the installation, and finally the decommission and demolition costs at end of life. It is a technology-agnostic method for comparing very different methods of electricity generation by cost. Figure 44 shows that even without subsidies, installing new solar PV installations is cheaper than installing new conventional sources. Finally, in just the past few years, the costs of PV have dropped to such levels that it is now becoming cheaper to install new solar than it is to continue to run an existing conventional plant, as shown in Figure 45, where the cost of a new solar build is comparable to the marginal cost of running coal and nuclear powered plants.

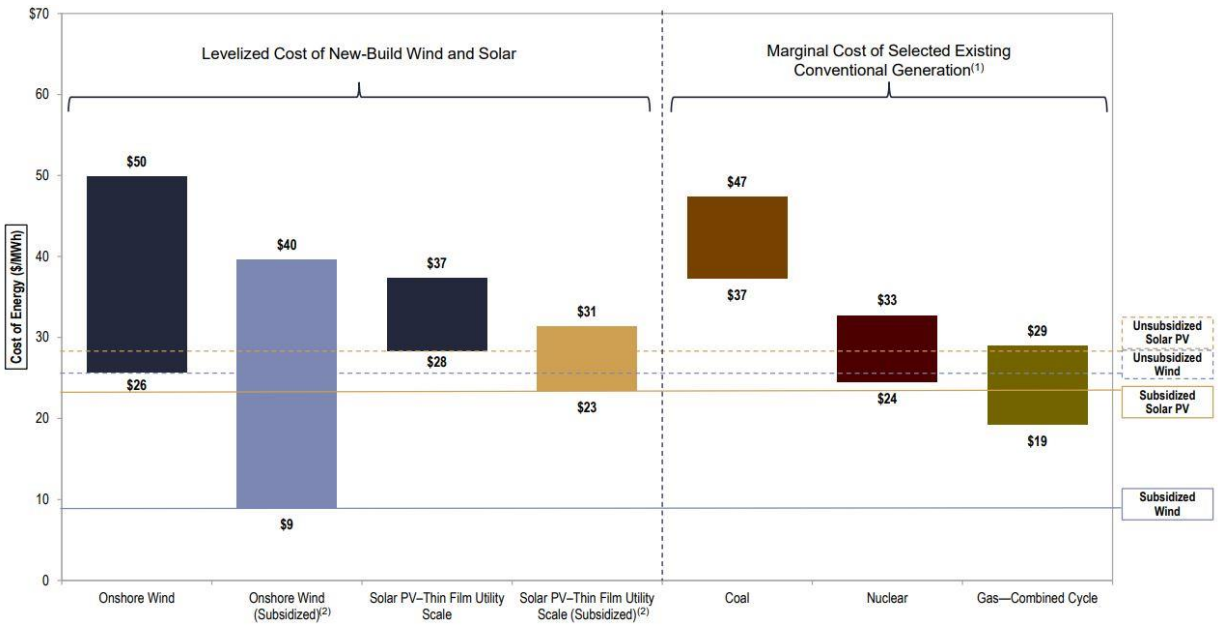


Figure 45. Cost of new solar vs marginal cost of existing conventional generation, adopted from [63]

Multiple factors have contributed to the decrease in PV costs. Most industries experience a "learning curve" as they expand. As the production of an industry increases, economies of scale, improved technology, and production efficiency gains manifest as a cost reduction, an example of which is shown in Figure 46 for crystalline silicon. Specifically, for the PV industry, the photovoltaic conversion efficiency has a large impact on the cost. First, and most obviously, as the conversion efficiency increases, you need fewer PV modules to meet the energy demand. But less obvious is the fact that as the number of modules decreases, the costs of things other than the module, known as the Balance of System (BOS) also decrease. BOS costs include the land where the PV installation will be built, the racking and wiring to connect the modules into an array, and the installation labor required, all of which decrease as conversion efficiency increases. Figure 47 shows the famous NREL PV efficiency chart, which tracks the world record

efficiencies of many PV technologies over time. Although this chart show research devices, the learning that facilitates these efficiencies is quickly translated into industrial processes.

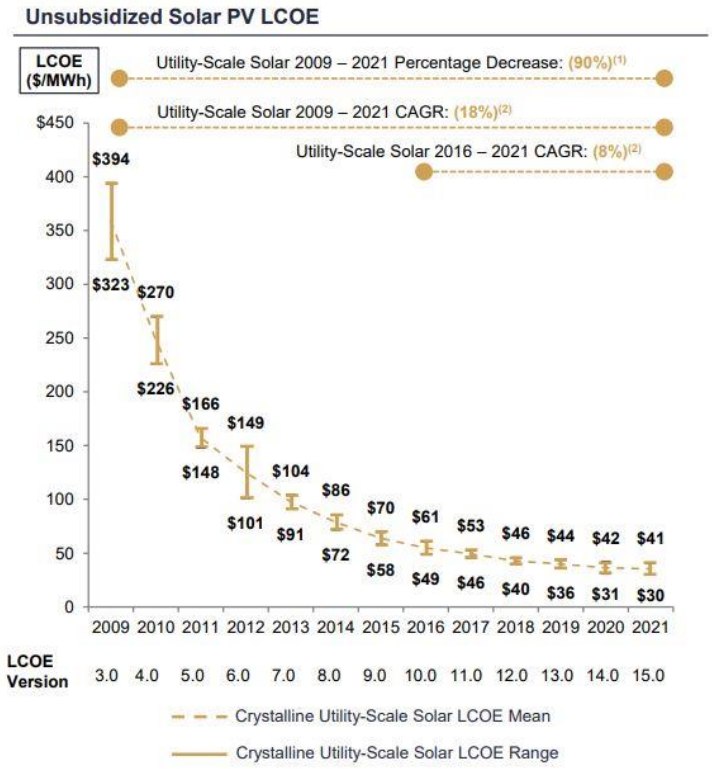


Figure 46. Solar PV learning curve, adopted from [63]

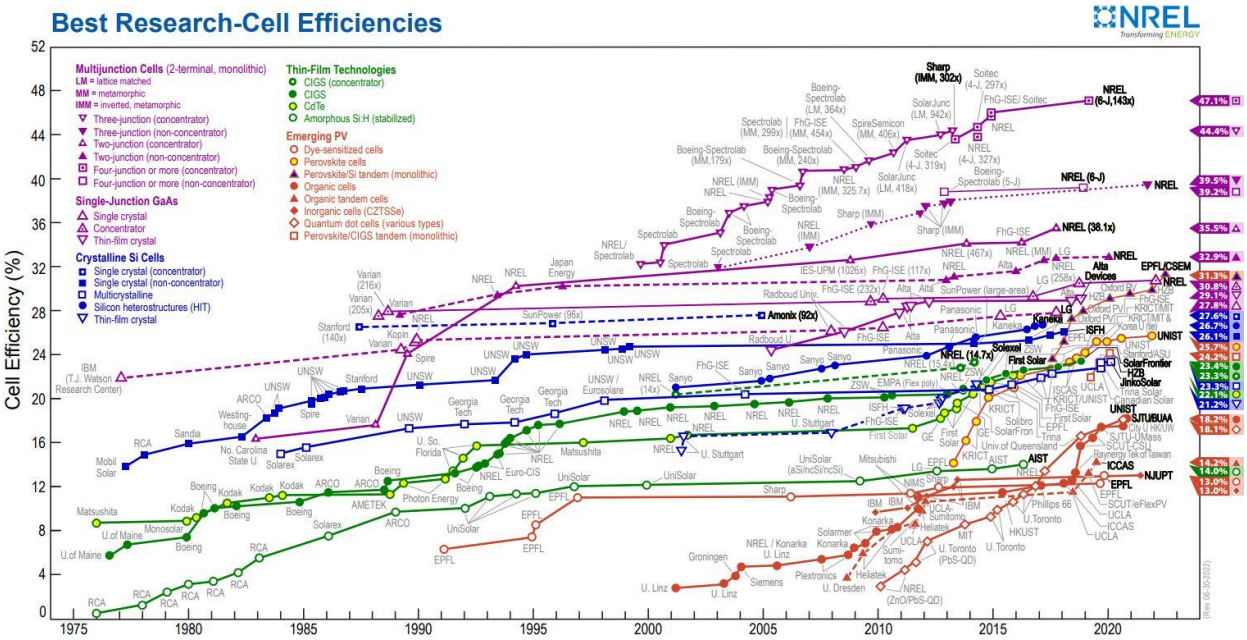


Figure 47. NREL research cell efficiency chart, adopted from [64]

Because crystalline silicon currently makes up the majority of the PV market, it is understandable that its development has thus far had the greatest influence on the massive growth and declining cost of PV. However, there are numerous reasons why CdTe, the leading thin film technology, may be a better solution for multiple future applications and may play a critical role in integrating solar generation as the majority energy source. While silicon and CdTe may be considered to be competing technologies, a PV-powered future requires so much installation that the two industries can still grow by orders of magnitude before meeting the full need.

CHAPTER 3. THE ADVANTAGES OF CdTe OVER Si

3.1 Maximum Theoretical Efficiency

Figure 3, shown in Chapter 1, displays the spectrum of light emitted from the sun. This spectrum consists of light of many wavelengths, each with different amounts of energy according to Equation 7:

$$E = h\nu \qquad (7)$$

Where E is the photon's energy, h is Planck's constant and ν is the frequency. Additionally, light's frequency and wavelength are related via:

$$c = \lambda\nu \qquad (8)$$

Where c is the speed of light in vacuum and λ is the wavelength. These equations demonstrate how the energy, wavelength, and frequency of light are related. Any photon that has energy below the bandgap of a photovoltaic material is incapable of exciting an electron into the conduction band. Therefore, these photons have little interaction with the material and pass through it. Conversely, any photon with energy greater than the bandgap will likely be absorbed. However, if an electron absorbs this energy, it will be excited to an unstable position above the conduction band. The electron quickly decays to a relatively stable position at the conduction band minimum, releasing the excess energy as heat. Only those photons with energy exactly equal to E_g will be absorbed with 100% efficiency. Resultantly, the theoretical maximum efficiency was calculated by William Shockley and Hans Queiser, and that theoretical limit is a function of the bandgap of the material [65]. Low bandgap materials may absorb a large proportion of the spectrum, but much of the energy from highly energetic photons is wasted as

heat. On the contrary, high bandgap materials only absorb from a smaller portion of the total light, but with less waste from those absorbed photons. Figure 48 shows the theoretical maximum efficiency of a single-junction photovoltaic device, calculated for both a 6000K blackbody spectrum and the AM1.5 spectrum.

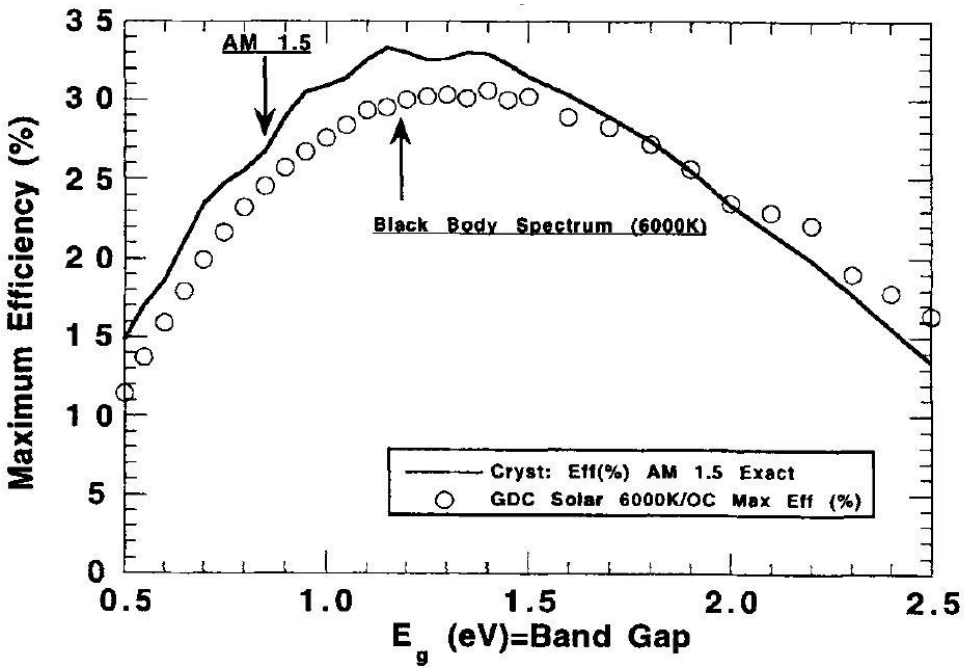


Figure 48. Theoretical maximum efficiency of a single-junction PV Device, adopted from [66]

Silicon has a bandgap of 1.11 eV while CdTe has a bandgap of 1.49 eV [67], both of which reside in the ideal range of E_g where the theoretical maximum efficiency is approximately 33%. Photovoltaic materials outside of this range suffer from an inescapable disadvantage due to the light that our sun produces. Although both Si and CdTe hold an advantageous position within the ideal E_g range, Auger recombination, a process during which an electron and hole recombine and transfer the energy to a third carrier, reduces the lifetime and efficiency of Silicon from this

theoretical maximum. Auger recombination decreases as the bandgap increases, and thus CdTe is far less susceptible to this recombination mechanism [68].

3.2 Manufacturability

The widespread availability of silicon-based photovoltaics belies the intricate and complicated process that is necessary to fabricate solar devices. Although silicon is the third most prevalent element on Earth [69], most of it is unsuitable for processing into high-purity Si. The primary source of the SiO_2 needed to start the process is quartzite. The SiO_2 is reacted with carbon to create elemental silicon and CO_2. At this point, the silicon contains approximately 2–3% impurities and is designated as metallurgical grade Si. The Si is then reacted with hydrochloric acid to produce trichlorosilane and hydrogen. Trichlorosilane is repeatedly distilled to increase the purity to at least 99.99999% known as "7N" pure. The trichlorosilane is next decomposed into pure silicon. This silicon is cast into large ingots, which is then sliced into wafers of approximately 150µm thickness. The wafers are etched to remove the surface layers which were damaged by the cutting wires. The wafers are then heated in a furnace with a boron-rich atmosphere and Boron is introduced into the wafer as a p-type dopant through diffusion. The emitter layer is doped n-type through a similar process using phosphorus. Front and rear contacts are adhered to the surface, commonly using screen printing or evaporation techniques. At this point, a single silicon cell has been fabricated. Many cells are then wired in series to create a "string." Multiples strings can be wired either in series or in parallel depending on the voltage and current requirements into a module [70]. It should be noted that the above describes a fairly basic silicon solar module. More advanced modules contain numerous additional steps, including the addition of passivating oxide layers, advanced anti-reflection coatings, and bypass diodes.

Even with modern manufacturing techniques and processes designed for mass production, this process takes approximately three days [71].

Comparatively, the manufacture of CdTe PV modules is a much faster, simpler process. The industrial practices developed by First Solar, the leading manufacturer of CdTe photovoltaics, allow for the complete fabrication of a photovoltaic module in less than 3.5 hours. Cadmium and Tellurium are byproducts of existing mining operations for Zinc and Copper, respectively [72]. These elements are combined to create the source material, CdTe, at relatively low purities when compared to silicon (devices with greater than 20% efficiency are fabricated with source materials that are only 5N or 6N pure.) The CdTe is deposited on TCO-coated glass via either sublimation or Vapor Transport Deposition (VTD), a process that takes only a matter of minutes. The CdTe is then subjected to a heat treatment in the presence of $CdCl_2$, which is known to cause recrystallization, remove stacking faults, promote grain growth, and facilitate the diffusion of Selenium in CdSeTe/CdTe hybrid absorbers [73]. The film is then doped, most commonly with copper, and a back contact, either tellurium or ZnTe is deposited at the back.

CdTe is a direct bandgap material, unlike silicon, which is an indirect bandgap material. In direct bandgap materials, the energy states within the conduction and valence bands have the same crystal momentum vector, while indirect bandgap materials have different crystal momentums. Indirect bandgap materials require a transfer of energy and momentum within the crystal lattice for photon absorption while direct bandgap materials do not. The practical result is that indirect bandgap materials have a much lower absorption coefficient, even for photons with energies near and above the bandgap. Therefore, thicker absorbers are required to absorb all of the light. Whereas a silicon wafer typically exceeds 100 μm thickness, CdTe films are virtually always less than 5 μm thick. This difference in absorber thickness, and the fact that CdTe does

not experience material loss from the ingot cutting and etching processes, mean that to produce the same number of photovoltaic modules, 100x less CdTe material is needed, compared to silicon. Figure 49 is an infographic which illustrates the thickness difference between the typical silicon absorber and First Solar CdTe.

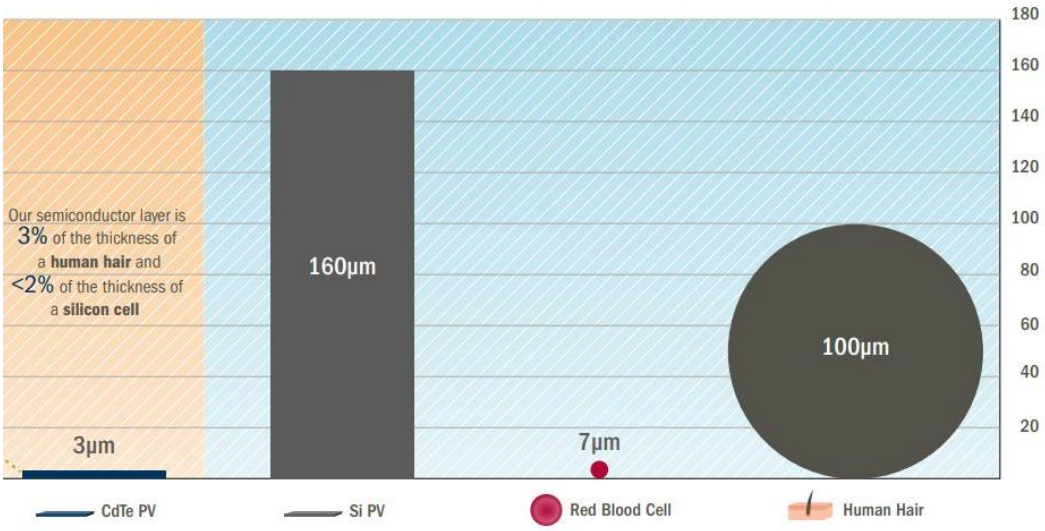


Figure 49. Silicon vs CdTe absorber thickness, adopted from [74]

The combination of a relatively simple manufacturing process and the small amount of semiconductor material has lead utility-scale CdTe to become the cheapest photovoltaic technology as demonstrated earlier in Figure 44. This effect can be further seen in Figure 50, which shows the cash to debt ratios for First Solar and five competitors. While corporate strategies and national policies have a large influence on the financial health of a company, manufacturing costs also play a large role.

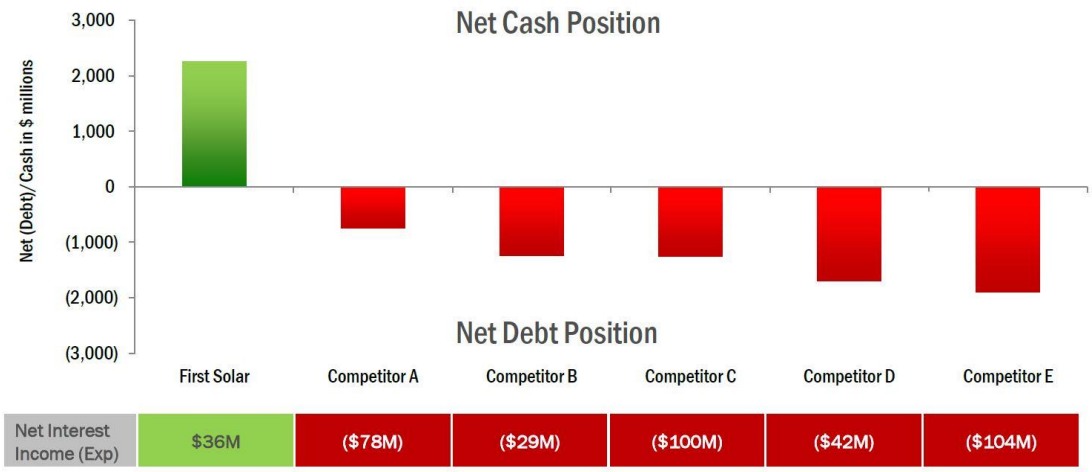


Figure 50. Net cash to debt for six PV manufacturers as of 2019 , adopted from [71]

3.2.1 Device Fabrication at Colorado State University

Excepting industrial manufacturers of CdTe-based photovoltaics, Colorado State University has one of the largest CdTe production capabilities in the world. Beginning with a glass substrate, the electron contact deposition, absorber layer deposition, $CdCl_2$ heat treatment, doping treatment, hole contact deposition, back electrode deposition, and device delineation and testing are all performed in-house. A brief review of the manufacturing steps for a copper-doped baseline device is provided here.

Samples are deposited on TEC10 substrates, a commercially available glass with a ~400 nm layer of fluorine-doped tin oxide (FTO) and a sheet resistance of approximately 10 Ω/square. 100 nm of MgZnO is then magnetron sputter deposited on the FTO to serve as a buffer layer/electron contact. The MgZnO is deposited at 140 W RF power across a 4 inch diameter target in an environment maintained at 5 mTorr by relative flow rates of 3% O_2/balance Ar process gas. The singular oxide target is composed of 11 wt% MgO and 89 wt% ZnO at

99.99% purity. Figure 51 shows a picture of the magnetron sputter tool in operation where the plasma is suspended above the MgZnO target.

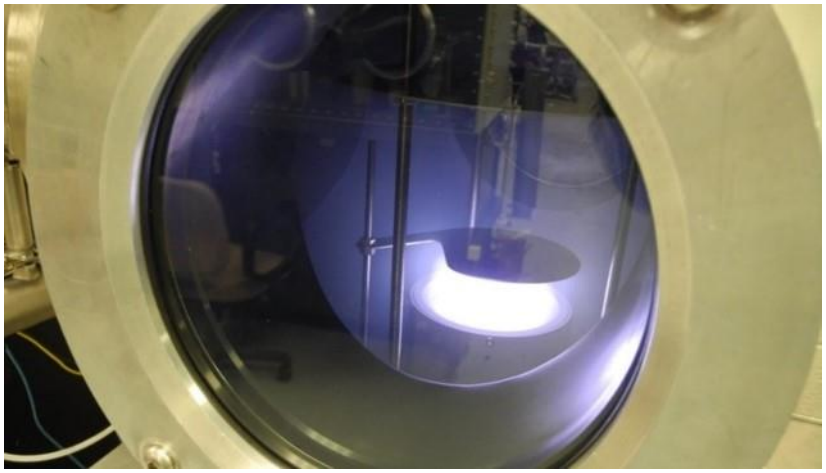


Figure 51. MgZnO deposited via magnetron sputtering

After a vacuum break, the substrates are transferred to the absorber-deposition chamber, where they are preheated to 500°C and immediately transferred to one of several deposition stations within the chamber, containing either CdSeTe or CdTe, as described in [75]. The CdSeTe is a mix of 40% CdSe and 60% CdTe making its composition $CdSe_{0.4}Te_{0.6}$. Absorber films are deposited in a 40 mTorr environment of either nitrogen or 2% oxygen, with the balance nitrogen. After the films are deposited, they receive a $CdCl_2$ treatment followed by a 400°C anneal. Once cooled, and following a vacuum break, the samples are doped using a CuCl treatment, described in [73], and receive 30 nm of evaporated 5N-pure Te to serve as a hole contact. Finally, spray-coated carbon then nickel paints suspended in a polymer binder serve as the back electrode. A mask is overlaid on the films and glass bead blasting is used to delineate the film into 25 small-area devices of approximately 0.6 cm^2. Indium is soldered to the exposed front electrode to ensure good contact during electrical characterization.

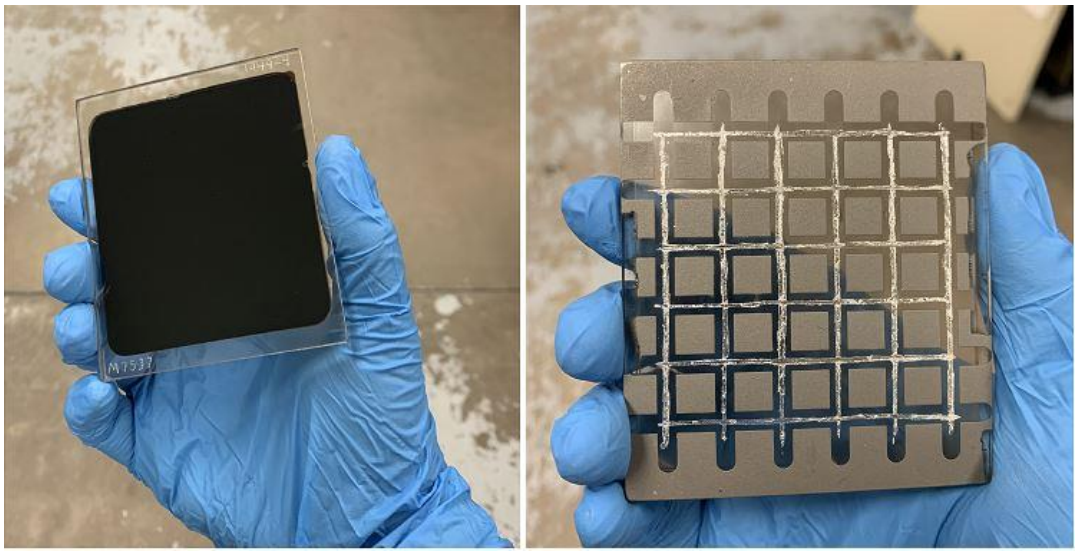


Figure 52. Cd(Se)Te film seen from the front (left), and finished devices seen from the back (right)

Note that many of the results presented in this work are the result of modifying this base structure, and the steps required to replace copper-doping with arsenic-doping, or incorporate passivating oxides and novel hole contact materials into the structure, will be discussed in their respective chapters.

3.3 Energy Payback and Harmful Emissions

A related benefit of the rapid manufacturing of CdTe photovoltaics is that it minimizes both the energy payback period for a solar module and the harmful emissions released during fabrication. The energy payback period is defined as the amount of time during which a photovoltaic module would need to operate in order to produce just the amount of usable electrical energy to offset the energy that was expended during its manufacture. At a point in photovoltaics' history, it was claimed that a solar panel could not produce enough in its lifetime to payback this energy, but today it is a very different situation. Figure 53 displays the energy payback periods for four different PV technologies with stated efficiencies. CdTe enjoys the

lowest payback period of approximately half a year. Considering most modules are warrantied for at least a 20-year life, this low payback period ensures that the module produces many times the energy that was needed for its production. Similarly, CdTe thin film manufacturing has the lowest carbon footprint of any of photovoltaic technologies and is tied with wind for the lowest footprint of all power generation technologies as seen in Figure 54.

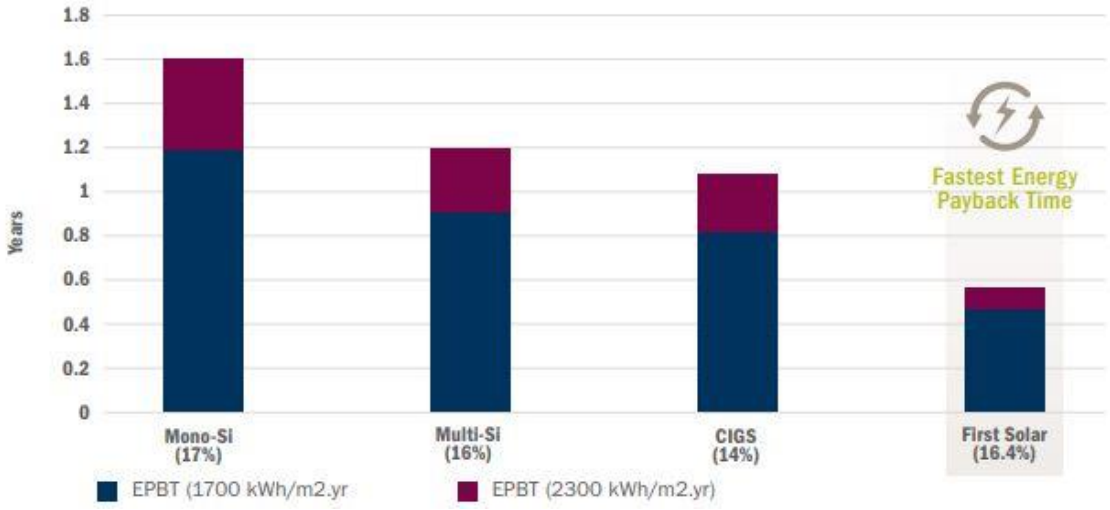


Figure 53. Energy payback period for four PV technologies, adopted from [74]

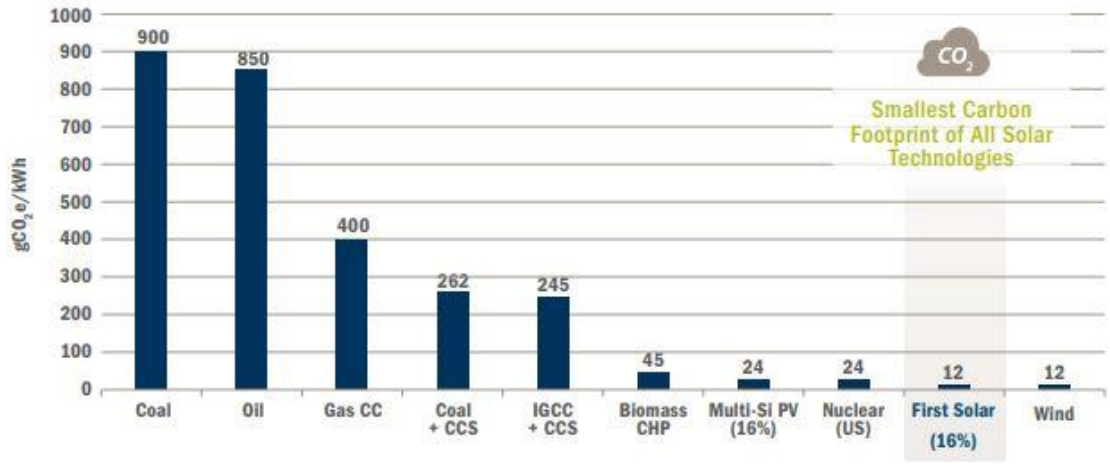


Figure 54. Carbon footprint of electricity-generating technologies, adopted from [74]

Finally, because cadmium is a known carcinogen when inhaled, there is a reasonable concern about the emission of this element during the manufacture and operation of CdTe PV. Fortunately, the compound CdTe exhibits lower reactivity and solubility than its elemental constituent. A 2003 NREL report concluded that the use of CdTe photovoltaics may actually reduce the amount of cadmium in the environment by displacing coal burning plants, which contains on average 0.5 parts per million (ppm) of cadmium [76].

3.4 Performance in Hot/Humid Climates

It comes as no surprise that the benefits of installing photovoltaic systems are maximized when they are installed in geographical areas that receive the most annual sunlight. Commonly, the areas which receive the most sunlight are the tropical and subtropical areas of the globe which also have hot and/or humid climates. Both high temperatures and humidity have a deleterious effect on photovoltaic conversion efficiency. Water, if it infiltrates the module, can react with either the semiconductor or the contacts to create unwanted compounds or accelerate oxidation, harming the device. Additionally, even if the water is kept outside of the encapsulant, high humidity correlates strongly with cloud cover, which drastically changes the proportions of direct and indirect light as compared to the standard testing conditions under which modules are certified. A 2018 study comparing CdTe and silicon arrays installed in Thailand found that CdTe's actual output was much closer to the installed capacity [77].

High temperatures also decrease performance. Chapter 1 explained how during operation, an electric field is established within the semiconductor when illuminated. This electric field separates the charge carriers and an electric current is produced. However, because this electric field separates the types of carriers, and concentrates them on opposing sides of said field, there is always diffusion of carriers trying to move from high concentration to low

concentration. This unavoidable “dark current” directly opposes the light-generated current and reduces the performance of a PV device. Because diffusion is a thermally driven process, higher temperatures allow more carriers to gain the thermal energy necessary to flow against the electric field. Although higher temperatures are universally detrimental to PV performance, various materials are affected by a rising temperature at different rates. These differences manifest as a thermal coefficient, which describes the amount of lost performance per degree. Figure 55 illustrates the relative energy yield advantage for CdTe when compared to silicon. It can be seen that CdTe performs better throughout most of the central latitudes, but the advantage is especially pronounced in the hottest, sunniest areas of the globe that are most likely to have high proportions of installed photovoltaics for economic reasons.

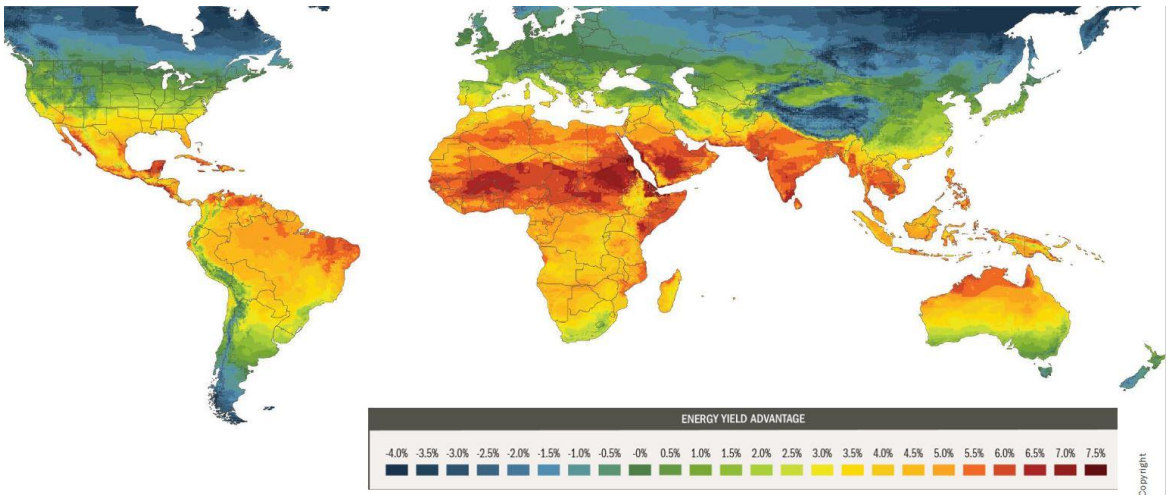


Figure 55. Energy yield advantage for CdTe vs Si, adopted from [71]

CHAPTER 4. MAJOR ISSUES IMPEDING > 22% CdTe DEVICES

4.1 Theoretical Performance of CdTe

Despite its leading position amongst thin-film photovoltaics, cadmium telluride's current performance falls far short of its theoretical potential. Other leading technologies, most notably GaAs and Si, are far nearer their respective theoretical maxima. While this makes CdTe's commercial success all the more remarkable, it also indicates that CdTe has far more room for improvement in the future. Table 3 below compares the current record device parameters for CdTe and silicon to the theoretical maximums.

Table 3. Comparison of current CdTe/c-Si performance to theoretical limits under standard testing conditions, adopted from [65], [78], [79], and [80]

Performance Parameter	Theoretical Maximum	Current Record	Percent of Maximum (%)
Cadmium Telluride			
Open-Circuit Voltage (mV)	1156	875.9	75.8
Short-Circuit Current Density (mA/cm^2)	32.0	30.25	94.5
Fill Factor (%)	89.5	79.4	88.7
Photovoltaic Conversion Efficiency (%)	33.1	21.0±0.4	63.4
Crystalline Silicon			
Open-Circuit Voltage (mV)	825	738.0	89.5
Short-Circuit Current Density (mA/cm^2)	44.0	42.65	96.9
Fill Factor (%)	85.0	84.9	99.9
Photovoltaic Conversion Efficiency (%)	30.85	26.7±0.5	86.5

*Assuming CdTe E_g of 1.45eV and c-Si E_g of 1.1eV

4.1.1 Voltage Deficit in CdTe

The above table makes it clear that CdTe still has a great deal of potential performance that has not yet manifested. The current world record device converts less than two-thirds of the

energy that it possibly could, and standard production cells convert even less. This loss of conversion efficiency can by mostly attributed to the low V_{OC}. Whereas the J_{sc} and FF are relatively close to the theoretical limit, V_{OC} has stubbornly remained at less than 900 mV for many years. Indeed, most of the recent advances in CdTe technology, to include incorporating a transparent front contact/buffer, incorporating CdSeTe into the absorber, or optimizing the back contact has resulted in improved J_{sc} and FF, but has had little effect on the extracted voltage. For comparison, Figure 56 below shows the JV performance of CSU's champion device. At 20.1% efficient, this is the best performing CdTe device manufactured at any research institution in the world, and yet its voltage remains below 900 mV, far from its potential output. Overcoming this substantial voltage deficit remains one of the most impactful goals towards improving device efficiency, and is the primary focus of this work. The remainder of this chapter is dedicated to understanding those factors which impact the voltage produced by a photovoltaic device.

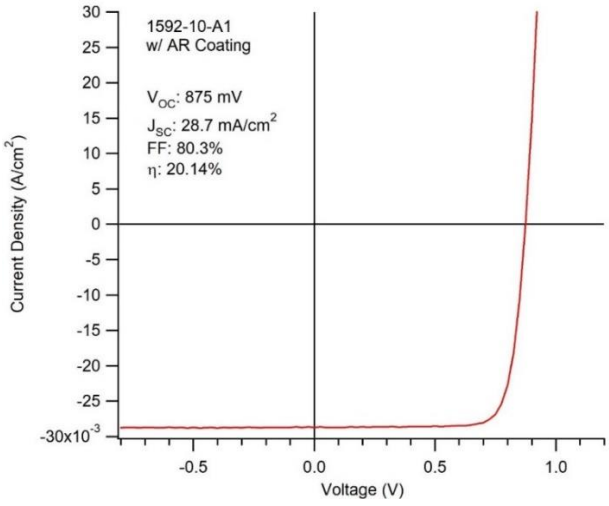


Figure 56. JV plot and conversion efficiency for CSU champion device

4.2 Charge Carrier Concentration

Close-Space Sublimated (CSS) cadmium telluride intrinsically contains approximately 10^{13}–10^{14} carriers per cubic centimeter. This is predominately due to V_{Cd} which is a p-type dopant in CdTe. [81] The charge carrier concentration can be increased from this intrinsic value through the doping process described in Chapter 1. Copper has historically been used to dope CdTe through Cu_{Cd} substitution, and is capable of increasing the doping density to mid-10^{14} carriers per cubic centimeter. For comparison, typical silicon wafers are commonly doped into the 10^{16}–10^{17} range.

Increasing the doping density has several notable effects on a photovoltaic materials. First, as the doping densities increase (assuming that the doping process doesn't drastically decrease carrier lifetimes) the quasi-Fermi level splitting present in the absorber increases, and as previously discussed, the qFLS indicates the maximum voltage that can be extracted from an absorber, assuming perfectly selective contacts and no other losses. Furthermore, increased doping can reduce e-h recombination by reducing the dark current within a device. Dark current, driven by diffusion, directly opposes the light generated current and increases recombination by allowing electrons and holes to meet and recombine. A stronger field imposes a stronger opposing force on these diffusing carriers, impeding its motion. Finally, very localized doping at the interface may be utilized to maximize the contact selectivity. As an example, high levels of p-type doping at the hole contact may be used to simultaneously increase hole conductivity through increased acceptor concentration while simultaneously inducing upward band bending which creates an energetic barrier to electrons, reducing the electron population at the back surface.

4.3 Charge Carrier Lifetime

Once an electron-hole pair is photo-generated, it exists for a finite time before recombining, either radiatively or through Shockley-Reed Hall recombination. The radiative lifetime of an e-h pair is orders of magnitude longer than S-R-H lifetimes because the entire energy transition must be accomplished in a single step, rather than over a series of small transitions. This time interval, designated by the Greek letter τ, is the carrier lifetime. As the carrier lifetime increases, it becomes more likely that the charge carrier will survive long enough to be extracted as usable energy. Additionally, increased lifetime increases the quasi-Fermi level splitting. Long lifetime carriers exist in the conduction or valence band, and thus affect the total charge carrier population and distribution of the Fermi-Dirac function, pushing the quasi-Fermi levels closer to their respective bands. Carrier lifetime is heavily affected by material quality, defect densities and energies, grain boundaries in polycrystalline materials, and interfaces. Because of the influences of these factors, the carrier lifetime can vary greatly depending upon its location within the device. The lifetime of a carrier deep within the material is known as the bulk lifetime, τ_b. The lifetime at a surface or interface is known as τ_s, the surface lifetime. The lifetime which is measured via TRPL systems is commonly referred to as τ_{eff}, the effective lifetime, and is influenced by both τ_b and τ_s as in Equation 9.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \qquad (9)$$

For many years, the minority-carrier lifetime of CdTe was considered to be a major constraint limiting performance. CdTe lifetimes were typically reported at less than 10 ns [82]. In recent years however, the CdTe community has made strong progress towards improving the lifetime of CdTe-based materials. Recently, the introduction of selenium into CdTe to form

CdSeTe has greatly improved the minority-carrier lifetime. Selenium has been observed to have a strong passivating effect on CdTe grain boundaries [83]. Absorbers containing graded CdSeTe/ CdTe layers now often exhibit measured lifetimes in excess of 30 ns [84]. Even more recently, Kephart *et al* deposited a film of CdSeTe between layers of aluminum oxide to form a double heterostructure. This structure was revealed to have an unprecedented excess-carrier lifetime of 430 ns. This phenomenal result heavily motivated this work, and the implementation of passivating oxides into a functioning device will be discussed in chapter seven.

4.4 Surface/Interface Recombination

Even when the bulk of the material is a near perfect crystal, with few or no defects (and correspondingly high carrier lifetime), the surface represents the abrupt end of that perfect repeating order. The surface may contain increased defects due to material processing procedures, impurities due to contact with other substances, or dangling bonds at the ends of the crystal lattice. The surface of a material is therefore often an area of high recombination. Even if a material has a very long bulk lifetime, the effective lifetime of a charge carrier may be dominated by surface recombination if the surface is sufficiently bad. This phenomena may occur either at the interface between two materials, or at a bare surface, and is measured as the surface recombination velocity, S measured in cm/s. When a material is illuminated, the increased recombination at the surface vicinity depletes the region of minority carriers, electrons in the case of p-type CdTe. Minority carriers then diffuse from deeper within the bulk towards this area of low carrier density. Therefore, no matter how terrible the surface, the surface recombination velocity is ultimately limited by the diffusion of carriers into the region in order to recombine. This upper limit is determined by the diffusivity of the carrier within the material and the temperature, but is commonly held to be approximately 10^7 cm/s. Unfortunately, this upper

limit is more than sufficient to greatly degrade the performance of any photovoltaic material with such a surface. A highly defective interface not only acts as a pathway for rapid recombination, but because carriers diffuse from the bulk towards the depleted vicinity, it reduces the excess carrier concentration through the material, reducing the quasi-Fermi energy level and implied voltage.

The surface recombination velocity of CdTe, although historically very high, was often considered to be a secondary problem because when the bulk lifetime was so low, as described previously, it dominated the effective lifetime. The recent achievements in increasing the bulk lifetimes has also renewed interest in improving the surface passivation, as it has now become a limiting factor. As the bulk lifetime improves, the importance of well passivated interfaces increases, as carriers are likely to survive long enough to reach the interface. CdTe surfaces have typically been reported to have surface recombination velocities from 10^5–10^6 cm/s. Several passivation methods, including surface treatments, adjusting the surface stoichiometry, or forming an interface with tellurium have improved this value to the mid 10^4 cm/s [85]. As with the carrier lifetime discussion, the addition of CdSeTe and Al_2O_3 have recently improved the recombination velocities drastically. Recombination velocities using these structures have been reported below 100 cm/s [86]. While these results show the incredibly low recombination velocities that these materials are capable of, further work is required to engineer these layers into working devices.

4.5 Interdependence

Each of the parameters presented in this chapter have been shown to greatly affect the extracted voltage from a photovoltaic device. Moreover, the current status of CdTe parameters has been shown, to illustrate where additional improvements might be made. However,

improving CdTe performance is not as simple as improving these parameters independently. There is an interdependence amongst these parameters, and the relative importance of each may grow or diminish as others are adjusted. Numerous studies have been made to attempt to model CdTe device performance while adjusting these parameters, and predict how best to maximize the voltage and photovoltaic conversion efficiency. Several examples of these interdependencies are here given, not to serve as an exhaustive list, but to illustrate how complicated the problem can become before discussing these modelling results.

4.5.1 Interdependence of Doping and Bulk Lifetime

As doping densities are increased in a semiconductor, the amount of defects, by definition is also increased. The increased defect load makes it so that as doping increases, bulk lifetime often decreases. To compound the difficulty, as doping increases, the depletion width shrinks. This increases the likelihood that an e-h pair will be generated at some point outside of the depletion width and is not immediately subjected to the electric field there present. Therefore the bulk lifetime becomes more important to ensure that the charge carrier survives long enough to reach its appropriate contact. Finally, even the radiative recombination lifetime of e-h pairs decreases as the carrier concentration increases. This results from the fact that in order for radiative recombination to occur, an electron and hole must “find” one another, which increases in likelihood as the charge carrier density increases. A balance must therefore be maintained between doping density and bulk lifetime to maximize the likelihood of charge extraction.

4.5.2 Interdependence of Doping and Interface Recombination

Interface recombination can likewise be affected by the increased defect load that accompanies higher doping levels. Impurities present at the surfaces may have a particularly deleterious effect on device performance. Additionally, maintaining high levels of dopant

activation (typically defined as the carrier concentration, measured by CV divided by the dopant atom incorporation, measured by Secondary Ion Mass Spectrometry (SIMS)) may be difficult at high doping levels, increasing recombination both within the bulk and on surfaces. Finally, a dopant in one material may simply be an impurity in another, so care must be taken to ensure that the dopant is confined within the intended material so as to not contaminate other layers in heterostructures.

4.5.3 Interdependence of Bulk Lifetime and Interface Recombination

When bulk lifetimes are low, as they have historically been in CdTe, the increasing or decreasing the interface recombination velocity has relatively little effect on the device performance. In such a case, a charge carrier exists for such a short time that it is unlikely to ever reach an interface before recombining. As the bulk lifetime improves, the probability of a carrier reaching the interface, regardless of where it was generated, improves greatly. As this happens, the impact of the surface recombination velocity grows. The most dramatic instance of this phenomena occurs when a very high bulk lifetime coincides with a very high recombination velocity. When this occurs, much of the benefit of the high lifetime is lost, because a charge carrier is almost certain to recombine at the surface, thus the effective lifetime, as shown in Equation 9, is utterly dominated by the low surface lifetime, and drives a low effective lifetime.

4.5.4 Quasi Fermi-level

Increasing the bulk lifetime, effectively doping a material, or improving the interface passivation can all contribute to increased excess carrier density with the photovoltaic absorber. The large excess carrier population results in an elevated quasi-Fermi level — located closer to its respective band, and further separated from the quasi-Fermi level of the opposing carrier. Therefore, the qFLS is an effective way to capture and describe the contributions of disparate

improvements to the semiconductor. Guided by the qFLS, researchers can directly measure whether or not experimental materials or processes improve the potential voltage of a device. The first step in developing a photovoltaic material is typically maximizing the qFLS in the bulk material by improving material quality and minimizing non-radiative defects. Once the qFLS in the bulk has been maximized, researchers may next work to incorporate electron and hole contacts. This likely will require steps to ensure proper interface passivation which may include chemical treatments, passivating oxides, or epitaxial growth. Highly selective contacts, with proper band alignment and a very high ratio of e/h or h/e conductivities (depending on the contact) will ensure that the full implied voltage is harvested as an actual voltage across an external circuit. The qFLS should be measured at each stage of production to ensure that it is not compromised by the addition processes.

4.6 Modeling Results

In recent years, multiple scientists at NREL have published models which seek to understand where the current performance of CdTe is most deficient, and what gains in conversion efficiency might be realized by improving one or more aspects of the device. As with all models, it is important to realize that the underlying assumptions of the model may cause some differences compared to real devices, but when numerous models are compared and contrasted, a general understanding of the required performance metrics begins to emerge. The intricacies of semiconductor physics, along with the interdependencies of multiple performance parameters make it difficult to declare single performance values that will achieve a desired conversion efficiency. Rather, the results are often presented as contour maps with many possible combinations of factors that result in performance above a threshold value.

4.6.1 Kanevce Model

The work by Kanevce *et al* modeled a CdS/CdTe device, seeking to understand the effects of doping density, carrier bulk lifetime, and front interface recombination velocity. In this work, the CdS doping level was maintained at 1.1 x10^{18} and the rear interface recombination velocity was kept at 10^5 cm/s. This model showed that with a S_{front} at 10^5 cm/s, it was impossible to achieve a 1 V cell. It did indicate, however, that greater than 1 V V_{OC} and indeed $\eta > 25\%$ was achievable when S_{front} is reduced to 100 cm/s, τ_b exceeded 50 ns, and the doping density reached 10^{16} holes/cm^3. Finally, the model revealed that at low doping levels, similar to what is seen in CdTe today, the interface recombination velocity is relatively un-impactful in terms of conversion efficiency. As the doping increases, however, the interface becomes ever more important, to the point where device performance will begin to decrease with improved doping, unless the interface is improved simultaneously [87].

4.6.2 Ablekim Model

The Ablekim *et al* work modeled an MgZnO/CdTe device, very similar to CSU's device structure. In this work the CdTe bulk lifetime was maintained at 25 ns, while the interface recombination velocity, doping levels of both the CdTe and MgZnO, and the conduction band offset were varied. It was determined that at 10^{14} holes/cm^3 doping levels, it was impossible to achieve 1 V open circuit voltage or an efficiency of 25%. It further indicated that it was possible to reach 25% efficiency, even with an S_{front} of 10^5 cm/s, but it required doping levels in excess of 10^{16} and an appropriate conduction band offset between the MgZnO and the CdTe [88].

4.6.3 Duenow Model

The Duenow model used a SnO_2/CdS/CdTe structure to further study the interplay between doping, lifetime, and interfaces. Through this model, it was determined that this

structure was capable of 28% efficient devices, shown below. To reach this level of performance, the device needed reasonably high doping, at 2 x 10^{16} cm^{-3}, both front and rear interfaces to be well passivated, with recombination velocities of 0 and 1000 cm/s respectively, and a bulk lifetime exceeding 100 ns. This study, similar to Kanevce's found that an S_{front} of 10^5 cm/s limited the device performance to 22%, even with high doping. Finally, this work advocated for the incorporation of a back-surface electron reflector, such as a wide band-gap material or graded doping might provide, to reduce rear surface recombination velocities [89].

Although not specifically identified and discussed in their respective publications, using the same device parameters and properties, it is possible to calculate the implied voltage of each theoretical device. The Kanevce model resulted in an implied voltage of 1081 mV while both the modelled devices in the Ablekim and Duenow models had implied voltages of approximately 1095 mV. This is important because it proves the external voltages and efficiencies which their models predict are feasible. To achieve these high iV_{OC}s, they all require large hole concentrations. Because they all assume relatively short carrier lifetimes, the devices are in low injection under 1-sun illumination, and thus need high levels of p-type doping to set the quasi-Fermi level of holes. A final factor to consider is the inherent assumption in these models of effective contacts, such that the external voltage is approximately equal to the internal voltage. Achieving this, particularly at the hole contact for Cd(Se)Te is not trivial, as will be discussed.

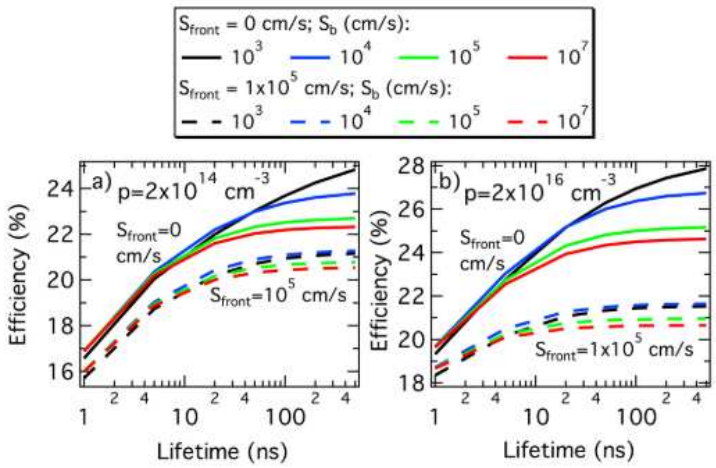


Figure 57. Modelled device efficiencies as a function of doping, lifetime and interface recombination, adopted from [89]

CHAPTER 5. GROUP V DOPING

5.1 Limitations of Copper Doping

As previously noted, copper has historically been used to dope CdTe-based photovoltaics in both research and production settings. Despite this use, copper has numerous liabilities which limit the performance of a Cu-doped device. Undoped CdTe typically has an intrinsic hole density of approximately 1–5 x 10^{14} holes/cm^3[90]. This is primarily attributed to the cadmium vacancies which have a thermodynamic tendency to form at high temperatures. Because the doping levels are primarily driven by V_{Cd}, the "intrinsic" doping level may be tailored during deposition by encouraging vacancies in a Te-rich deposition environment or hindering vacancy formation in a Cd-rich environment. Unfortunately, adding copper as a dopant only has a very mild effect on the bulk hole density of CdTe. Even with copper doping, bulk acceptor concentrations rarely exceed $10^{15}/cm^3$ when measured by CV, often not even a single order of magnitude increase. W Three main mechanisms have been identified which together explain the poor doping performance of copper: self-compensation, low activation, and grain-boundary segregation.

5.1.1 Self Compensation

Yang *et al* have observed that continually increasing the Cu concentration in CdTe does not lead to a corresponding increase in hole concentrations. Instead, they have observed that the increase in Cu_{Cd}, an acceptor, is offset, or compensated, by a near identical increase in Cu_i, a donor, and thus the hole concentration stagnates [91]. Kucys *et al* have proposed several reactions, which may contribute to this self-compensating behavior, which are shown as

Equations 10 and 11 below [92]. Therefore, adding more Cu to the semiconductor will have harmful effects, as will be shown momentarily, but will not increase the carrier concentration.

$$Cu + Cd_{Cd} \rightarrow Cu_{Cd}^{-} + Cd_i^{+} \qquad (10)$$

$$Cu_{Cd}^{-} + Cu \rightarrow Cu_{Cd}^{-} + Cu_i^{+} + e^{-} \qquad (11)$$

5.1.2 Low Activation

Even when copper is properly situated as a dopant in a cadmium vacancy, it still must be ionized before it may act an acceptor. The probability of ionization is dependent on the difference between the defect energy and the energy of (in the case of copper and other acceptors) the valence band. In this way, defects are often described as shallow or deep defects, and the more shallow the p-type defect, the closer it is to the valence band, and the higher its ionization probability will be. Numerous studies have been conducted to identify the Cu_{Cd} defect energy, and its energy level is accepted to be between 160 mV and 310 mV above the valence band [93], [94]. Shallow defects are generally considered to be within a few kT of its band (<100 meV.) Therefore Cu_{Cd} is a relatively deep acceptor, and non-ideal for doping purposes. Between self-compensation and low activation rates, copper doping only marginally increases the acceptor concentration above that found in a film with no intentional impurity dopants. One such comparison illustrates this in Figure 58 below where the CV profiles of Cu-doped and undoped samples fabricated at CSU are compared.

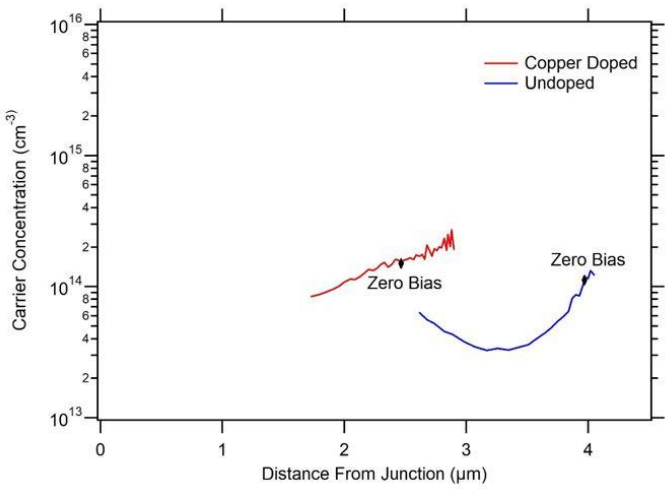


Figure 58. Comparison of CV profiles for a Cu-doped and undoped sample

5.1.3 Copper Mobility and Grain Boundary Segregation

Copper has a propensity to distribute unevenly throughout the polycrystalline bulk of CdTe. First principles studies have indicated that it is energetically favorable for copper to migrate and reside at the grain boundaries, a finding which has been corroborated by TEM studies [95]–[97]. This may in part explain why the carrier concentrations in Cu-doped CdTe is almost always several orders of magnitude below the copper incorporation.

Yet this is not the only issue which copper mobility within CdTe causes. Interstitial copper is a fast diffusor in CdTe, and may create a myriad of issues. Interstitial copper is capable of diffusing even at room temperatures, and thus may migrate during normal operating conditions. This had led to short, mid, and long-term stability issues in CdTe devices. Photovoltaic performance may fluctuate widely as copper congregates at the grain boundaries and interfaces. In addition, the high mobility of copper is such that doping must be performed after the $CdCl_2$ passivation step. While this is not an insurmountable issue, it does constrain

manufacturing processes, as the elevated temperatures and chlorine flux present during the $CdCl_2$ treatment will drive the copper to the front interface, killing the device.

5.1.4 Carrier Lifetime in Cu-doped Devices

Both the self-compensation and the low activation tendencies of copper in CdTe contribute to very low excess-carrier lifetimes. Any defect which does not contribute a hole is simply a defect without benefit. Defects, by their nature, reduce carrier lifetimes by creating imperfections within the crystal lattice, and therefore states within the bandgap that facilitate recombination. Thus far, attempts to increase acceptor concentrations with copper treatments above 10^{15} cm^{-3} have resulted in severely decreased lifetimes, down to fractions of a nanosecond, due to the increased copper load, as seen in Figure 59.

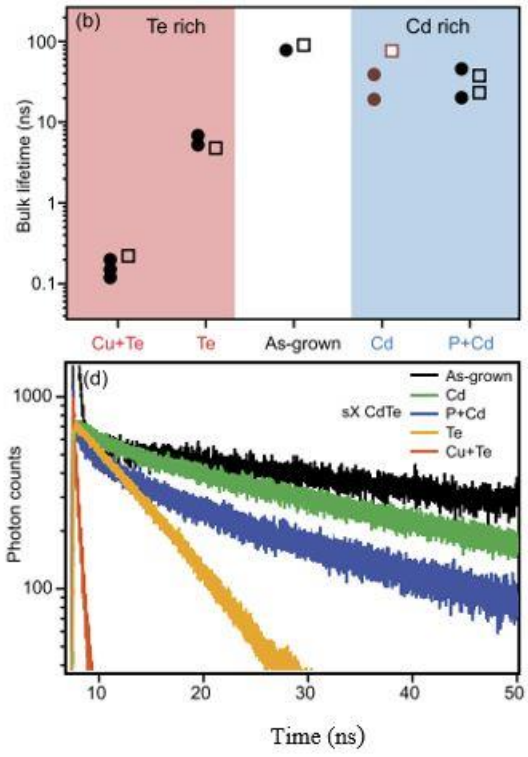


Figure 59. CdTe lifetimes using varying dopants, adopted from [81].

5.2 Group V Doping

The limitations of copper doping in CdTe is the most commonly identified culprit preventing increased voltage extraction. This has prompted the investigation of Group V dopants as a possible alternative that may boost performance. Unlike copper, which resides in the cadmium site, Group V dopants, when activated, replace a tellurium atom. Initial investigations of Group V dopants in CdTe have revealed several promising indicators which suggest that these new dopants, and primarily arsenic, may be used to mitigate or altogether eliminate the problems inherent with copper.

5.2.1 Previous Group V Dopant Work

Burst *et al.*, utilizing phosphorus to dope single crystal CdTe, achieved a hole density of 10^{17} cm^{-3}, 50% dopant activation, and minority-carrier lifetimes of several hundred nanoseconds, culminating in several samples with an open circuit voltage of 1 V [98]. Alternatively, using Vapor Transport Deposition (VTD) techniques, McCandless *et al* were able to successful incorporate phosphorous, arsenic, and antimony into CdTe thin films, with varying success in activating the respective dopants [99]. Figure 60 below shows the incorporation and activation rates for this study.

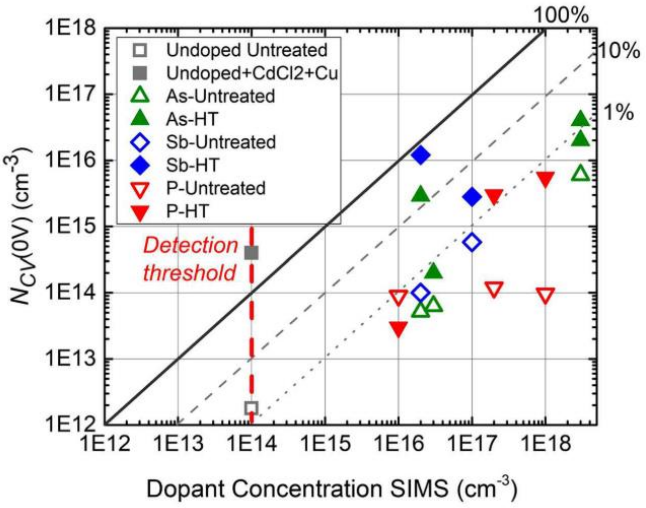


Figure 60. Carrier concentration and dopant concentration, adopted from [99]

It can be seen from the above that Sb and As both were able to achieve activation rates of greater than 10%, followed distantly by P activation. A post-deposition anneal/heat treatment was beneficial towards achieving higher activation rates. These anneals were performed in the presence of Cd vapor, used to encourage the formation of tellurium vacancies into which the dopants might migrate. The Cd vapor source temperature, however, must be controlled, as excessive cadmium overpressure facilitates the formation of interstitial cadmium, a deep trap within CdTe, estimated at 330mV below the conduction band [99].

When evaluating potential dopants, it is important to consider the energy level of the defect within the bandgap. This is particularly important considering that one of the primary shortcoming of copper is its location deep within the bandgap. Table 4 shows the energy levels of the three aforementioned Group V dopants compared to Cu. Of the tabulated dopants, antimony resides considerably deeper than either phosphorus or arsenic.

Table 4. Dopant defect energy levels, adopted from [100]

Dopant	Defect	Energy level above E_V (meV)
Cu	Cu_{Cd}	160–310
P	P_{Te}	50
As	As_{Te}	100
Sb	Sb_{Te}	230
As	As_{Te} (In CdSeTe)	37*
		*Based on measurements performed at NREL

5.2.2 Previous Arsenic Doping Work

Because the arsenic dopant energy level is considerably shallower than either antimony or copper, paired with the promising incorporation results shown earlier, arsenic appears to be the most promising candidate and has received the most attention in early Group V studies Farrell *et al*, using molecular beam epitaxy (MBE), showed that arsenic incorporation as high as 7×10^{17} atoms/cm^3 and acceptor concentrations exceeding 5×10^{16} holes/cm^3 were achievable. Additionally, this study provided clear evidence that the arsenic incorporation in CdTe is greatly improved when done in the presence of a cadmium overpressure of approximately 20%. Throughout this study, an arsenic cracker, operating at 1000°C was used to break the native As_4 molecules, which are not a dopant in CdTe, into As_2. Despite this effort, the as-grown films had very low carrier concentration until a follow-on activation anneal was performed. Using this, a 50% activation rate was reported [101].

Nagaoka *et al*, using a traveling-heater method, we able to grow single-crystal CdTe ingots which were doped with various amount of arsenic from the range of 10^{15}–10^{19} atoms/cm^3. The carrier concentration, measured by CV, increased as the arsenic incorporation increased.

However, the increase in doping did not keep pace with the incorporation, and so although activation rates of approximately 20% were reported when the As incorporation was at 10^{16} atoms/cm^3, it fell to below 1% when As concentrations reached 10^{19} atoms/cm^3. The authors attributed this decreases to either self-compensation of arsenic doping by the formation of AX centers, or the formation of other As point defects which did not activate as a dopant [102].

Kartopu *et al*, have shown that carrier concentrations as high as 3 x 10^{16} holes/cm^3 were obtained using Metal-Organic Chemical Vapor Deposition (MOCVD). Nevertheless, they noted that performance degraded as arsenic incorporation increased, and dopant activation rates were below 2% for all conditions. Perhaps in part due to this low activation, the best device performance had a V_{OC} of only 763 mV and efficiency of 13.3% [103].

Utilizing sputtered CdSe, sublimated CdTe, and low-temperature *ex-situ* $AsCl_3$ treatments, Li *et al* showed improved hole concentrations, carrier lifetimes, and device performance compared to copper-doped baselines. Utilizing these methods, they report hole concentrations of 2 x 10^{15} cm^{-3}, dopant activation of 5.88% and an open-circuit voltage of 863 mV [104].

Finally, using its proprietary VTD deposition methods, First Solar, in collaboration with NREL, have demonstrated polycrystalline CdSeTe/CdTe devices with a J_{sc} of 30 mA/cm^2, FF of 80% and a conversion efficiency of 20.8% using arsenic doping. These devices demonstrated acceptor concentrations exceeding 10^{16} holes/cm^3 and comparable lifetimes to copper-doped devices. Despite the substantial increase in hole density, the V_{OC} of these devices did not improve, remaining in the range of ~850 mV, and activation rates of the arsenic were reported at 1.5% [105].

It is clear from these results that multiple methods are capable of producing high arsenic incorporation and some single crystal growth techniques are capable of producing high carrier concentrations in CdTe using an arsenic dopant. However, the high activation rates seen in these single crystals are difficult to translate to the rapid polycrystalline deposition methods which have made CdTe commercially viable. To date, simultaneously achieving high hole concentrations, high dopant activation, long excess-carrier lifetimes, and efficient photovoltaic conversion using arsenic doping remains a challenge. Colorado State University's Next Generation Photovoltaic Lab has a long history of expertise in CSS as a method of fabricating CdTe solar cells. Therefore, a novel method of arsenic incorporation and activation has been pioneered at Colorado State University with the goal of increasing doping levels above those achievable with copper while maintaining a high level of activation, and thus avoiding the harmful effects of non-activated arsenic defects. The research presented here is organized into four distinct hypotheses which will be presented over the subsequent chapters. Collectively, these hypotheses are focused on answering key questions that must be addressed in order to incorporate arsenic doping and passivating oxides into modern CdTe device architectures in order to reduce the voltage deficit.

5.3 Hypothesis I

Hypothesis IA: ***Close Space Sublimation (CSS) of an arsenic-containing CdTe or CdSeTe source material is an effective method for incorporating at least 10^{18} atoms/cm^{3}arsenic into the growing film.***

Hypothesis IB: ***The incorporated arsenic from a CSS source charge resides as an activated dopant, monoatomic arsenic sitting in tellurium vacancy sites. Therefore, dopant activation will be > 25%***

5.3.1 Device Structure

In order to determine arsenic incorporation and dopant activation using CSS, it was necessary to modify the historic process and device structure. Initially, the device structure was designed to mimic the CSU champion device structure. In this structure, a 100nm layer of MgZnO was deposited on TEC10 glass via magnetron sputtering, followed by a 500 nm layer of undoped CdSeTe. Next, a 3 µm film of CdTe:As was deposited from a source charge that contained 10^{20} atoms/cm^3 of arsenic dissolved into the CdTe material. During the deposition of the arsenic-containing film, cadmium overpressure was provided via the co-sublimation source containing elemental cadmium at temperatures that ranged from 140°C to 230°C. The film stack was then subjected to a $CdCl_2$ treatment with a 450°C source temperature and a 420°C substrate heater temperature. Figure 61 shows this device structure. Full details of all samples presented in this work can be found in the table of samples located at the end of this document.

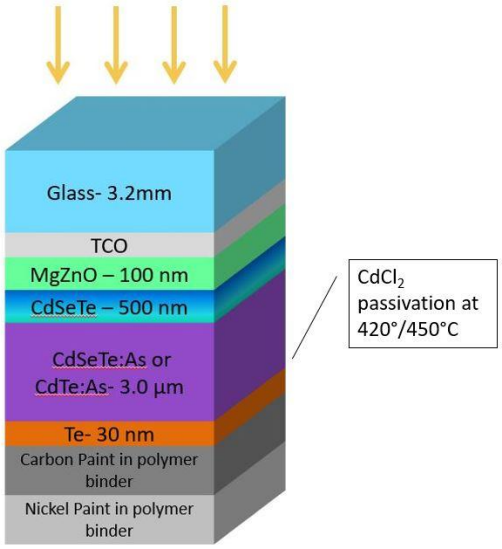


Figure 61. Device structure used in the initial arsenic-doping experiments, referred in the text as the "non-diffused method". Not to scale.

5.3.2 Co-sublimation Hardware and Cadmium Overpressure

Farrell *et al* provided convincing evidence that arsenic incorporation is heavily affected by the presence or absence of cadmium overpressure during film growth. Based on these results, Co-sublimation was utilized to fabricated films under cadmium overpressure. In this configuration, two sublimation sources were installed one on top of the other. The sources were thermally isolated so they could each maintain different temperatures, but the upper source had channels bored into it to allow the vapor from the lower source to reach the substrate. Further details of the co-sublimation source may be found in [106] and Figure 62 shows a diagram and photo of the source hardware. The top source was loaded with the primary absorber material—either CdTe:As or CdSeTe:As. The lower source was loaded with elemental cadmium.

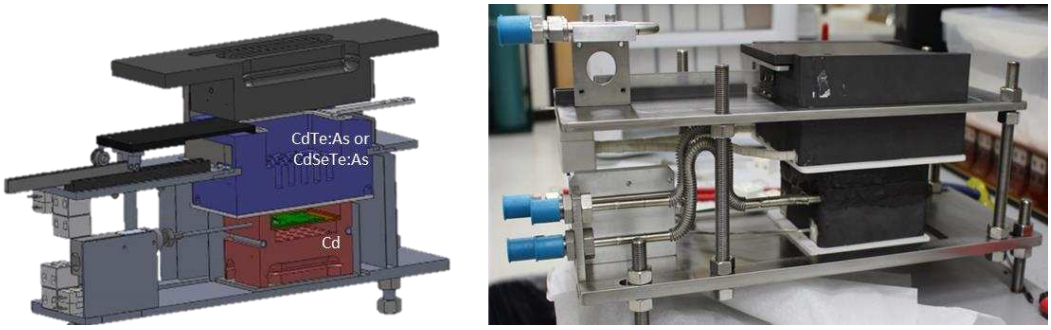


Figure 62. Co-sublimation hardware used in arsenic doping experiments

Using the aforementioned methodology, numerous experiments were conducted. During these experiments, devices were characterized to measure the doping, lifetime, luminescence, and photovoltaic conversion efficiency, seeking indicators of effective arsenic doping. Below are shown the initial results of the arsenic doping experiments, aimed at discerning whether or not

close-space sublimation of an arsenic containing source charge is a viable method or incorporating and activating the arsenic.

5.4 Hypothesis I Results

5.4.1 JV Performance

This method was met with initially encouraging results, as a 16.8% efficient device was fabricated, the JV curve of which is shown in Figure 63, both with and without a tellurium back contact. Several notable features deserve discussion. First, a 16.8% efficient device, particularly one fabricated so early in the experimental cycle, was encouraging. 16.8% conversion efficiency already places this device in the upper tiers of CdTe performance. While a great deal of additional improvement would be required, these samples showed that arsenic-doped CdSeTe/CdTe holds promise. Secondly, while the overall performance is impressive, the open-circuit voltage remains lower than would be expected from a well-optimized copper-doped sample. Finally, the sample without the tellurium back contact shows a substantial kink, which reduces the V_{OC} and FF of the device. The thin layer of evaporated tellurium deposited as the hole contact for CdTe has been thought to reduce the barrier to hole extraction and remove the "kink." If the back few nanometers of CdTe were doped-highly enough, the hole barrier would likely not be present and there would be little to no difference in performance between the two samples shown in Figure 63. The fact that there is a large difference in performance provides possible evidence that the back surface is not highly doped. Nonetheless, these promising results warranted further investigation, to see if the arsenic incorporation and/or high levels of doping might explain the encouraging early results.

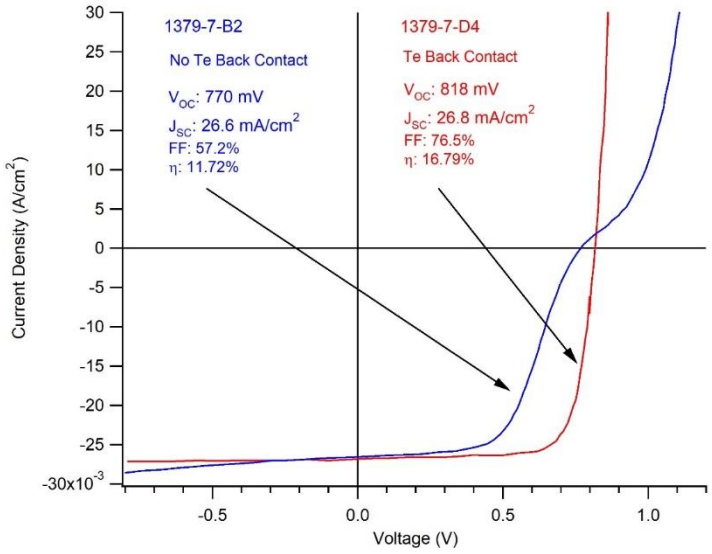


Figure 63. JV curve for a 16.8% CdSeTe/CdTe:As device with and without tellurium

5.4.2 Arsenic Incorporation

To measure the arsenic incorporation in CdTe films deposited from an arsenic-containing source, and to measure the response as a function of cadmium overpressure, a series of films were fabricated while the cadmium source temperature was gradually increased. SIMS measurements were performed on each sample and the arsenic incorporation was compared. This comparison is shown in Figure 64 below. Unlike Farrell's work using MBE, the amount of cadmium overpressure does not appear to significantly alter the amount of arsenic incorporation in polycrystalline films deposited using co-sublimation. Indeed, the insert in Figure 64 shows a zoomed-in view of a section of the curve, where the curves for all four cadmium overpressures tested overlay one another. It should be noted that the difference in sputtering time between the sample without Cd overpressure and the other samples is due to a difference in sample thickness rather than a significant difference in the sputter rate. When compared against a CdTe:As standard of known incorporation produced at NREL, these signals could be correlated to arsenic

incorporation of 10^{18} atoms/cm^3, indicating approximately a 1% incorporation rate from the source charge of 10^{20} atoms/cm^3.

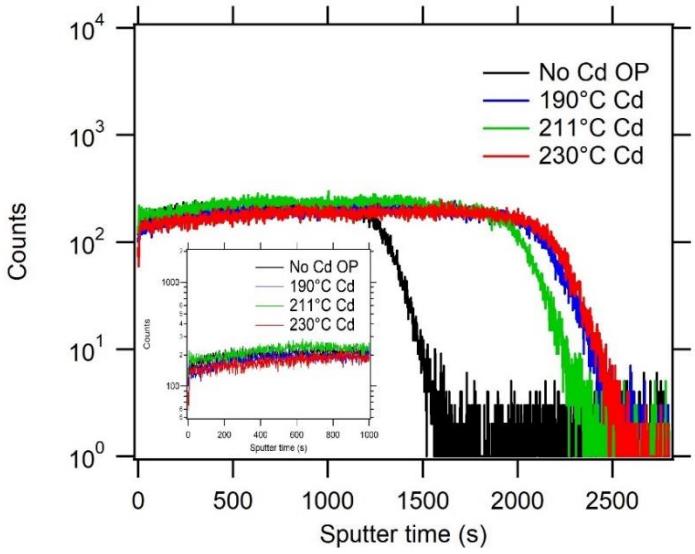


Figure 64. Arsenic profiles of MZO/CdTe:As films deposited under varying cadmium overpressures, obtained using SIMS. SIMS measurements performed at Colorado School of Mines

5.4.3 Acceptor Concentration

Next, utilizing CV, the carrier concentrations of multiple CdTe, CdSeTe, and graded bilayer samples were measured. First, the 16.8% CdSeTe/CdTe:As device shown in Figure 63 was measured using CV. The acceptor concentration was found to be quite low — between $7x10^{13}$ and $2x10^{14}$ cm^{-3} depending on whether the belly of the curve or the zero bias point is used, as seen in Figure 65. In either case, this is comparable to the intrinsic doping found in a sample with no intentional doping. This evidence, along with the kink behavior seen in the JV indicates that the direct deposition of CdTe:As from an arsenic-containing source is not sufficient to achieve high hole concentrations. The moderately high JV performance therefore, is more indicative that depositing CdTe:As behind CdSeTe enabled the high J_{SC} and FF as traditional

bilayer structures, and the unactivated arsenic in the CdTe was only mildly harmful, decreasing the V_{OC} but not by a great deal.

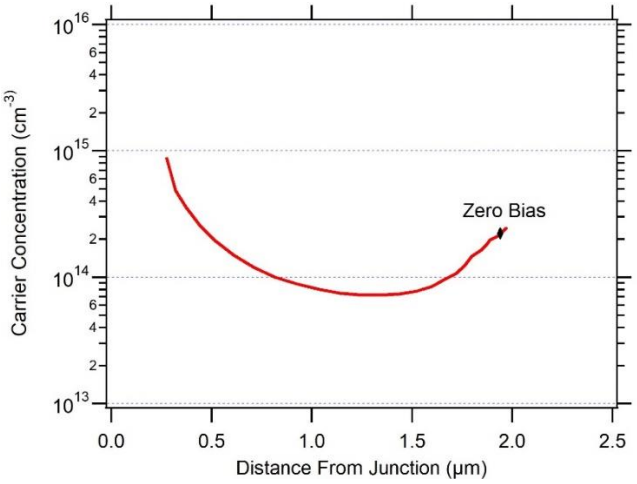


Figure 65. CV profile for the 16.8% MZO/CdSeTe/CdTe:As arsenic-doped device (1379-7) showing acceptor concentration of approximately $10^{14}cm^{-3}$.

Additional CV measurements were taken on multiple other structures to explore the effect of starting with a CdSeTe:As source material as opposed to CdTe:As. The CV curves for a CdSeTe:As/CdTe/CdSeTe (Figure 66) as well as a CdSeTe:As only device (Figure 67) are shown below. The belly of both of these curves remain in the 10^{13}–10^{14} cm^{-3} range, however, the large difference in carrier concentration as determined by the belly and the zero-bias point (which extends up to 10^{16} cm^{-3}) makes it difficult to determine exactly. The possibility that CdSeTe is more readily doped with arsenic will be further explored in Chapter 6.

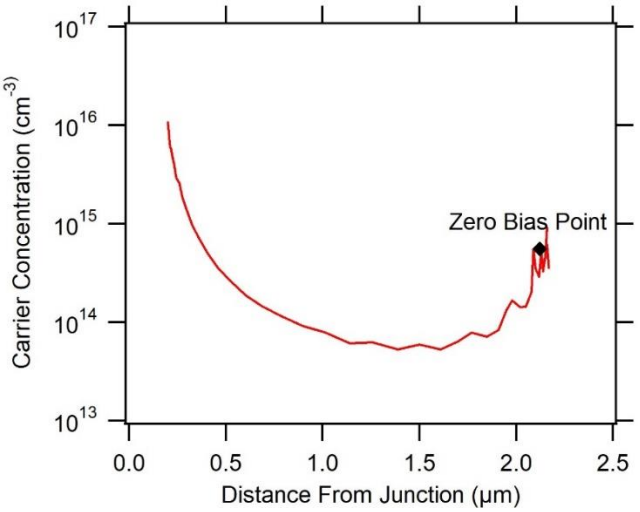


Figure 66. CV Profile of a MZO/CdSeTe:As/CdTe/CdSeTe device (1732-8R)

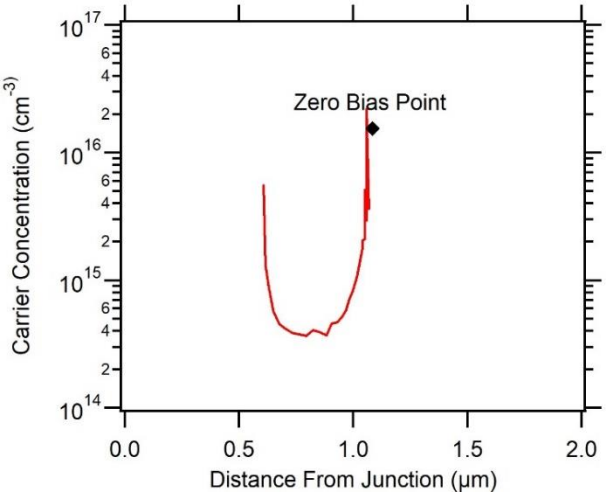


Figure 67. CV Profile of a MZO/CdSeTe:As device (1886-3)

Finally, CV measurements were performed on the same CdTe:As samples which were measured with SIMS. All of the samples displayed similar carrier concentrations as measured by CV. This indicates that not only does the cadmium overpressure not drastically affect arsenic incorporation into the film, but it also does not appear to have a significant effect on the rate of arsenic activation.

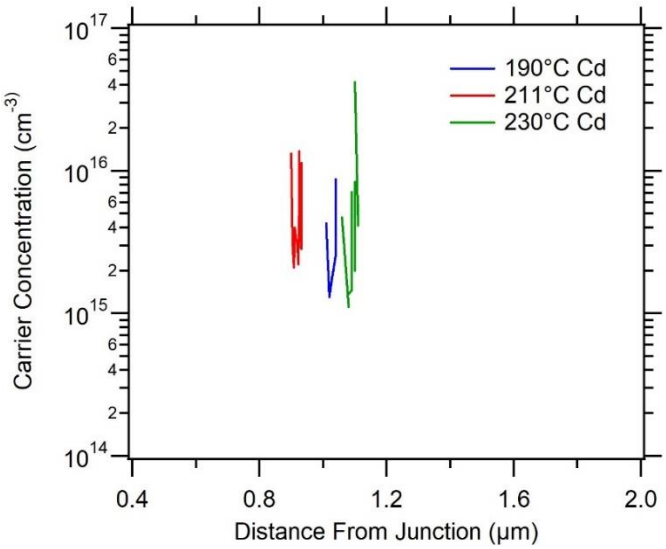


Figure 68. CV Profiles for MZO/CdTe:As samples deposited under various cadmium overpressures (1811-3,4,5)

5.4.3.1 Dopant Activation

Having determined both the carrier concentration (by CV) and the arsenic incorporation (via SIMS) for the same CdTe:As samples, it is now possible to calculate the activation rate of the dopant. Dividing the acceptor concentration (10^{16} cm^{-3}) by the total arsenic density (10^{18} cm^{-3}) gives an activation rate of just 1%, and this value may be much smaller if the belly of the curve is used. In either case, the direct deposition of Cd(Se)Te:As material into a film results in virtually all of the arsenic incorporating not as an activated dopant, but as a defect.

5.4.4 Carrier Lifetimes

To corroborate the findings that as-deposited material was highly defective, TRPL measurements were performed. Figure 69 shows the TRPL decays for a 2 µm CdSeTe:As sample. Because the lifetimes in CdTe are typically on the order of just few nanoseconds, it can be difficult to see the effect of adding arsenic. Therefore, CdSeTe, with its much greater lifetime was chosen to show the effect. Undoped CdSeTe films have been shown to exhibit microsecond

lifetimes [107]. These samples however, exhibited lifetimes of only 9–16 ns, depending on injection. This serves as another indication that the film contains high levels of defects, and that those defects are reducing the effective lifetime by providing non-radiative recombination pathways.

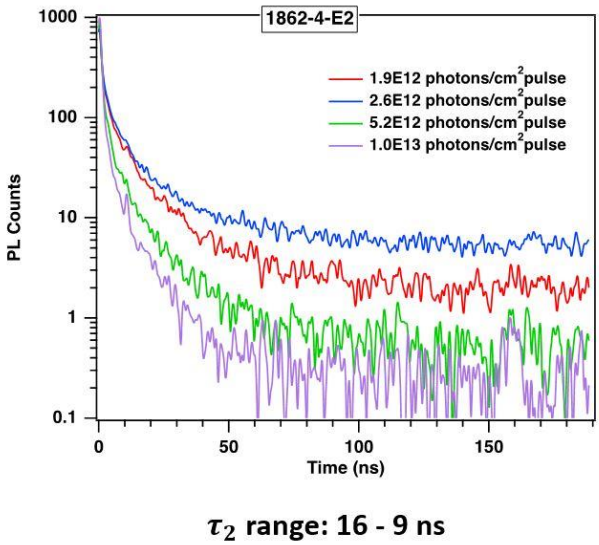


Figure 69. TRPL decays for a 2 µm CdSeTe:As sample (1862-4) under various injection levels showing low excess-carrier lifetime

5.4.5 External Radiative Efficiency

ERE measurements confirmed the TRPL findings indicating high amount of non-radiative recombination. Although numerous samples were measured for ERE, they were all at or below the detection limit for the tool —with an external radiative efficiency of approximately 0.0005%. This corresponds to an implied voltage at or below 900 mV. Therefore, despite the fact that some as-deposited, non-diffused sample demonstrated decent JV behavior, their potential is extremely limited. The high defect density, although not harmful enough to prevent conversion

efficiencies in the upper teens, does prevent this structure from being a viable path forward to achieve voltages greater than 900 mV.

5.4.6 Scanning Electron Microscopy and Energy-Dispersive X-Ray Spectrometry

The CdTe:As and CdSeTe:As source materials were prepared by the High Pressure Bridgman (HPB) growth technique, performed at Washington State University, to melt CdTe, CdSe, and Cd_3As_2 with Cd overpressure as described in [108]. When it was fabricated, it was initially hypothesized that the arsenic would be completed dissolved as monoatomic arsenic. If this were the case, then as the source material sublimated, single arsenic adatoms would impinge upon the growing film to become As_{Te}. To investigate possible sources of the defect-heavy films, these source materials were studied using a Scanning Electron Microscope (SEM) equipped with Energy Dispersive X-Ray Spectrometry (EDS). It was soon discovered that arsenic was not dissolved into the source material as single atoms but rather had a tendency to cluster into areas of high Cd_3As_2 concentration, as the EDS maps in Figure 70 for CdSeTe:As and Figure 71 for CdTe:As display. These findings are corroborated by literature, where Burton *et al* similarly found arsenic clusters in MBE-deposited films [109].

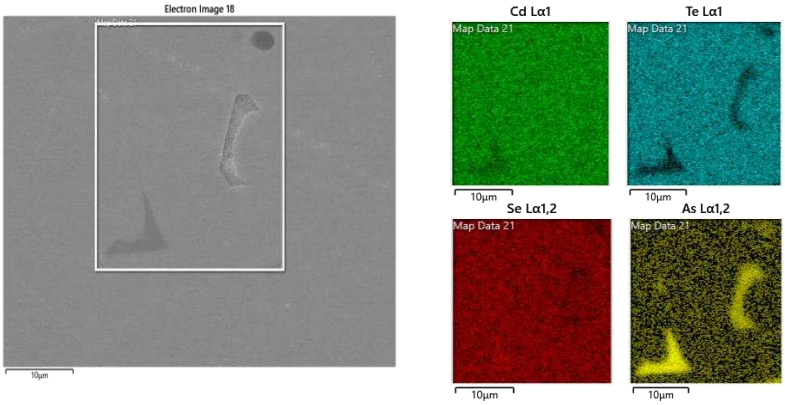


Figure 70. SEM/EDS map for CdSeTe:As source charge showing areas of high arsenic concentration, microscopy images taken by University of Illinois at Chicago

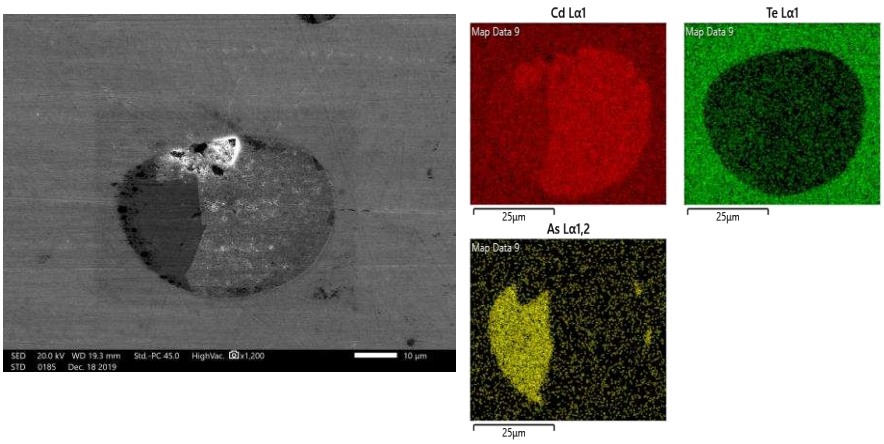


Figure 71. SEM/EDS map for CdTe:As source charge showing areas of high arsenic concentration, microscopy images taken by University of Illinois at Chicago

This provided a possible explanation for the low carrier densities shown in the sublimated films, as it was unlikely that monoatomic arsenic was sublimating into the film, but was instead likely impinging the growing film as either As_2 or As_4. Therefore, a new structure was devised, which is the subject of Chapter six, and will be described there.

5.5 Conclusions

The combined evidence indicates that fabricating films from an arsenic-containing source results in films in moderate arsenic incorporation, but low dopant activation, short excess-carrier lifetimes and the resulting low implied voltage. Although this method is capable of incorporating up to 10^{18} cm^{-3} of arsenic into CdTe films, the vast majority of it is not monoatomic, and therefore cannot serve as a p-type dopant. Resultantly, many samples exhibit carrier concentrations only marginally higher than that of undoped structures. Finally, remaining arsenic, likely in the form of dimers, tetramers, or arsenic complexes, act as defects which mediate non-radiative recombination. This contributes heavily to the short excess-carrier lifetimes and low ERE measured, which in term reveal the limited potential for these structures.

Therefore, while Hypothesis IA is supported by the evidence, Hypothesis IB must be rejected due to very little apparent doping of arsenic when directly deposited from an arsenic-containing CdTe:As or CdSeTe:As source. Based on these findings, it appears unlikely that high arsenic activation can be obtained from direct sublimation of CdSeTe:As and CdTe:As, and further steps are required to trigger activation, which is the subject of Hypothesis II.

CHAPTER 6. DIFFUSED-ARSENIC DOPING

6.1 Hypothesis II

The as-deposited CdTe:As or CdSeTe:As is highly defective with arsenic complexes present in the film. Therefore, diffusing arsenic into the light absorbing portion of the film from the as-deposited layer will result in a higher quality film.

6.1.1 Diffused-Arsenic Methodology

The results shown in Chapter 5 indicate that simply using an arsenic-containing source charge during close space sublimation to fabricate films is not sufficient to achieve high levels of dopant activation and carrier concentrations. Therefore, a new structure was devised which was designed to only allow monoatomic arsenic species into a portion of the absorber. This design, referred to as the "diffused" structure, and shown in Figure 72 , was inspired by the kinetic modelling results from Krasikov and Sankin [110]. They showed that interstitial arsenic, As_i, experiences a significantly smaller diffusion barrier compared to the various other As species, complexes, and AX centers. This suggests that As_i may be the only arsenic species capable of diffusing a significant distance during processing.

6.1.2 Device Structure

In the diffused structure, a 100 nm layer of MgZnO was deposited on TEC10 glass via magnetron sputtering, followed by a 1–4 µm layer of undoped CdSeTe. Next, a 1–1.2 µm film of either CdTe:As or CdSeTe:As was deposited. During the deposition of the arsenic-containing film, cadmium overpressure was once again maintained via the co-sublimation source containing elemental cadmium. The temperature of the cadmium source was maintained at 211°C, chosen because it was the middle temperature in a range where the incorporation appeared to be

insensitive to temperature variation. Finally, a thin 200 – 500 nm "cap" of undoped CdSeTe was deposited at the back, to minimize any potential loss of arsenic during the $CdCl_2$ process. The entire film stack was then subjected to an aggressive $CdCl_2$ treatment with a 480°C source temperature and a 430°C substrate heater temperature, considerably hotter than the previously optimized temperatures used for standard device structures. During the $CdCl_2$ process, interstitial arsenic is intended to diffuse from this back "reservoir" of arsenic-containing material into the front layer, resulting in two distinct regions within the film: a front "diffused" layer where only monoatomic arsenic is present, and the back layer where all of the less mobile complexes and AX centers are retained. A simple diagram of this process can be found in Figure 73 for illustrative purposes. Krasikov and Sankin's work also shows that the reaction of As_i into other arsenic species occurs on the microsecond timescale, ultimately leading to the desired As_{Te} formation over the timescale of seconds [110].

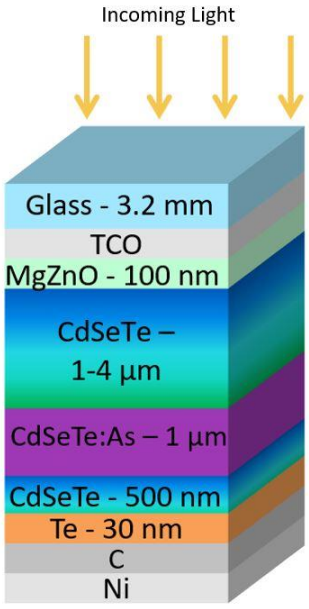


Figure 72. Device structure used in the diffused arsenic-doping experiments, referred to in the text as the "diffused method". Not to scale.

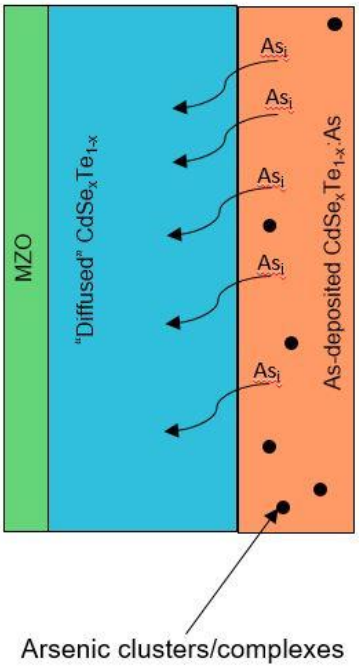


Figure 73. Diagram of the arsenic diffusion process, where interstitial arsenic diffuses towards the front while arsenic complexes are retained in the as-deposited layer. Not to scale.

6.2 Hypothesis II Results

6.2.1 Arsenic Incorporation

To verify arsenic incorporation in the absorber using this diffused method, SIMS measurements were conducted by EAG Laboratories and the results are presented in Figure 74. To gain insight into the As diffusion profile in the front CdSeTe layer without complication from surface roughness and uneven sputter rates, the entire film was peeled from the substrate and measured from the front interface using a proprietary method. This sample had 2.5 µm of undoped CdSeTe at the front followed by 1.2 µm of CdSeTe:As. This profile shows arsenic incorporation as high as 10^{19} atoms/cm^3 at the back in the "as-deposited" reservoir region when using a source material with 10^{20} atoms/cm^3 arsenic concentration. Interestingly, the arsenic

concentration in the “as-deposited” CdTe:As shown in Figure 64 in chapter 5 only reached 10^{18} cm^{-3} when deposited from a source material with the same arsenic concentration. This may indicate that arsenic more readily incorporates into CdSeTe, with an incorporation rate of approximated 10% compared to the 1% in CdTe. The arsenic signal decreases as it approaches the front interface until it reaches the detection limit for arsenic at 5 x 10^{15} atoms/cm^3 at which point the plot becomes erratic and jagged. The unique arsenic profile seen in Figure 74 may result from the combined behaviors of the multiple arsenic species. This includes substantial amounts of immobile arsenic complexes retained in the “reservoir” at 2.5–4 µm from the front, rapid diffusion of interstitial arsenic towards the front interface, and the evolution of As_i into more stable but less mobile species, where they cease to diffuse any appreciable distance and ultimately react to form As_{Te}.

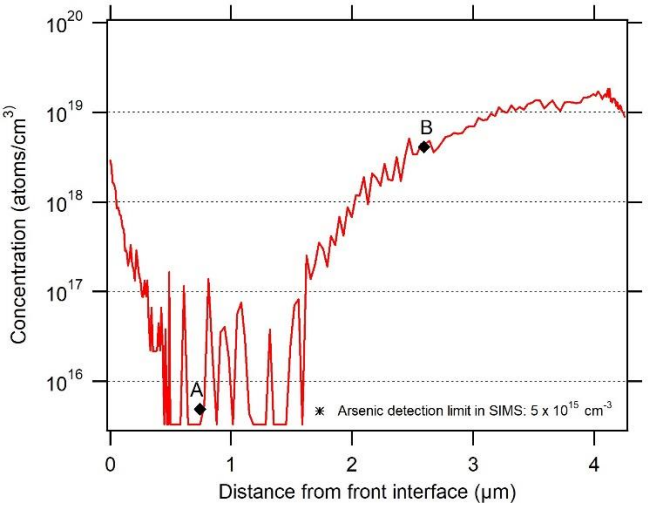


Figure 74. SIMS showing the arsenic profile of a "diffused" sample (1546-7). SIMS were performed at EAG Laboratories. Point “A” and "B" are points of interest and compared to CV and SCM results at the same film depths

A second sample, fabricated several years later and peeled from the front and measured with SIMS in the exact same way shows a similar arsenic profile shown in Figure 75, indicating that this structure can be repeatedly made.

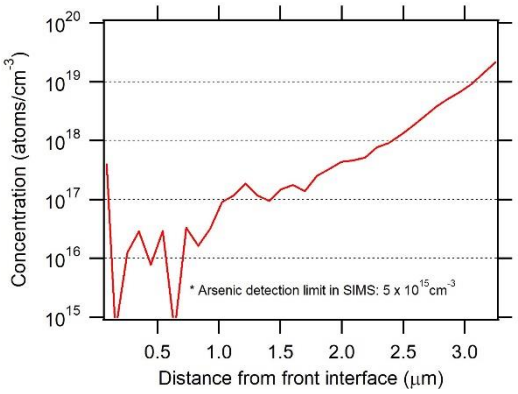


Figure 75. SIMS showing the arsenic profile of a "diffused" sample (1968-2). Sample was peeled at NREL and SIMS were performed at EAG Laboratories.

6.2.2 Acceptor Concentration

As with the non-diffused arsenic doping work, it was necessary to determine the carrier concentration within the fabricated devices to ascertain the effectiveness of the arsenic doping process. Capacitance-Voltage measurements were once again performed. Additionally, Scanning Capacitance Microscopy was used to probe locations that were too deep within the film to be accurately investigated by CV.

6.2.2.1 Capacitance-Voltage

Figure 76 below shows the CV plots of numerous devices which have been fabricated using the diffused doping methodology. It shows that the device structure discussed in section 6.1 has repeatedly produced acceptor concentrations in excess of 10^{15} carriers/cm^3. The blue plot is the CV profile for the sample shown in Figure 74, the first SIMS profile for the diffused method. The black plot was observed when the front layer of undoped CdSeTe was increased from 2.5 µm to 4 µm. The green plot, showing a carrier concentration of greater than 10^{16} holes/cm^3 was achieved by performing two $CdCl_2$ treatments. The first $CdCl_2$ treatment occurred

after the front layer of CdSeTe was deposited (but before the CdSeTe:As). The second treatment occurred after all absorber layers were deposited. This early $CdCl_2$ treatment would have caused recrystallization and grain growth in the front CdSeTe layer, which potentially increased the rate of arsenic diffusion. All three diffused-arsenic-doped curves can be compared to the orange curve, which is a repeat of Figure 65, the 16.8% non-diffused arsenic sample and the red curve, which is the CV profile of a baseline copper-doped device, which exhibits the low-10^{14} doping levels typical of a copper-doped CdSeTe/CdTe device [91]. In these discussions, all reported doping levels are taken as the carrier concentration at zero bias, indicated by a diamond on the plots.

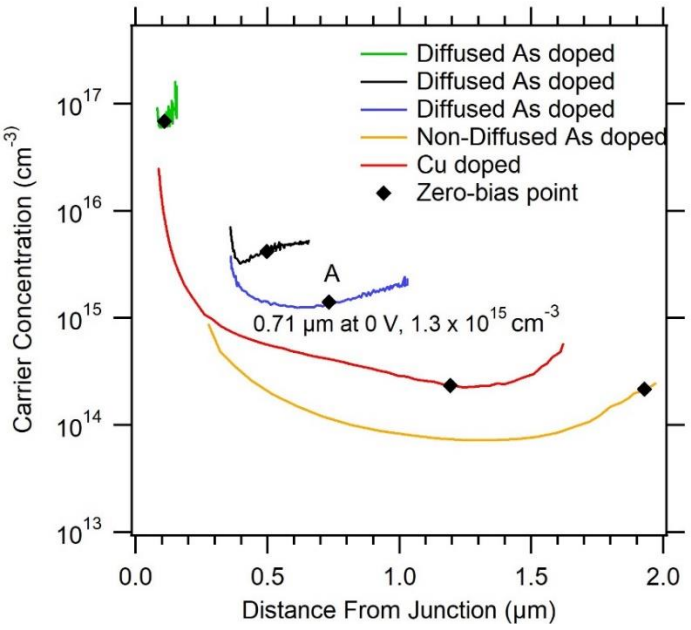


Figure 76. CV profiles for three different diffused-arsenic devices (Blue: 1546-7, Black: 1633-4L, and Green:1894-8) compared to the profile of a non-diffused arsenic-doped sample (1379-7) and a typical baseline copper-doped sample (1634-7).

6.2.2.2 Scanning Capacitance Microscopy

One of the limitations of the CV measurement is that it is incapable of measuring the carrier concentrations towards the back of the device. In order to obtain a measurement toward the back, the depletion width must be extended by applying a reverse bias to the device. Unfortunately, this method cannot extend the depletion width all the way to the back of devices more than a few microns thick. It is however important to measure the carrier concentration towards the back, as the high levels of doping near the back will induce upward band bending, which creates an electron energy barrier, reducing back surface recombination and may aid in hole collection. Therefore, a measurement known as Scanning Capacitance Microscopy (SCM) was performed, and the results may be seen in Figure 77 . In SCM, a low signal, such as seen on the left of the plot near point "B", corresponds with a small change in capacitance as a function of voltage, which implies high doping levels, alternatively, a higher reading implies lower doping, such as at point "A". According to EAG Laboratories, where the measurement was performed, the flat profile towards the left, taken at approximately 2.5 μm from the front interface, corresponds to doping levels of at least 10^{18} carriers/cm^3.

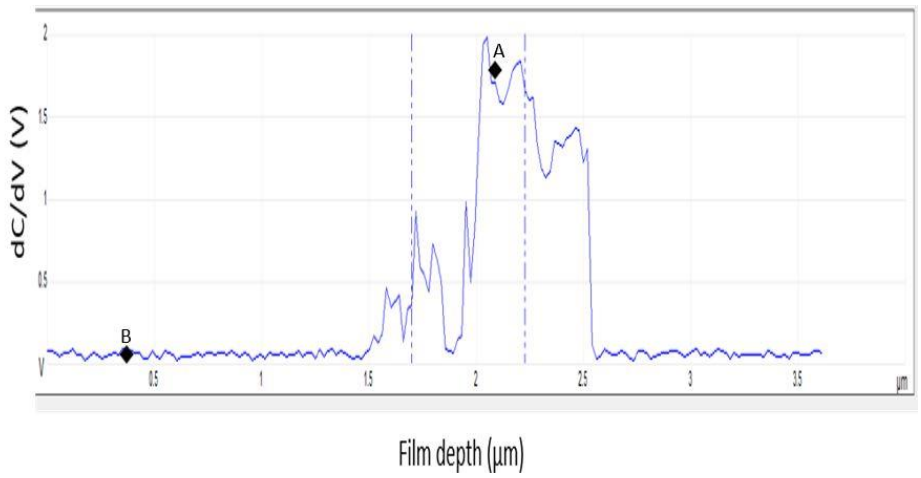


Figure 77. Scanning capacitance microscopy measurements throughout the depth of a diffused-arsenic-doped device (1546-7.) Points "A" and "B" are points of interest for comparison at the same depths using SIMS & CV measurements. SCM performed at EAG Laboratories

6.2.2.3 Dopant Activation

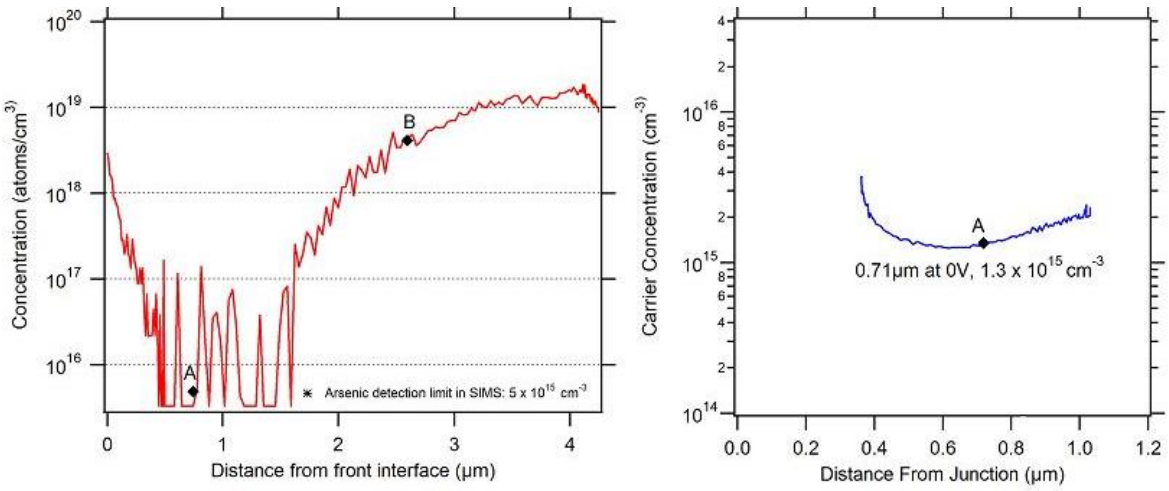


Figure 78. Side-by-side comparison of SIMS and CV results for the same diffused-arsenic-doped sample (1546-7)

Figure 78 displays the previously shown SIMS and CV results for the diffused-arsenic-doped sample 1546-7 for easy side-by side comparison. By dividing the carrier concentration as measured by CV at 0.7 µm from the front (1.3 x 10^{15}) by the total arsenic concentration

(5×10^{15}) at the same depth, an activation ratio of at least 26% is obtained. For ease of comparison, these points on the different plots have been labeled as point "A". Another location, point "B" shows a different location, approximately 2.5 μm from the front interface, which will allow for a similar activation calculation for a point deep within the film using SCM.

Performing the same activation calculation as before, but using the 10^{18} cm^{-3} carrier concentration given by SCM and the arsenic concentration of 3.4×10^{18} from SIMS at point "B" at depth of 2.5 μm, gives a doping activation ratio of 29%. Therefore, it appears that the doping profile within the front "diffused" layer of CdSeTe, which was previously undoped, is graded from approximately 10^{15} at the front to 10^{18} at the back while maintaining consistent activation rates.

6.2.3 Luminescence

The evidence for high arsenic doping is further supported when considering the luminescence of these devices. Using both cathodoluminescence and steady state photoluminescence, energy peaks which correspond to arsenic sitting in a tellurium site have been identified. Figure 79 and Figure 80 respectively show the CL and PL spectra for arsenic-doped films. Figure 80 shows multiple device structures, including samples with Al_2O_3, ITO, and Ag back contact/electrode layers. These additional layers do convolute the data, particularly with the addition of the low-energy peak at 1.27 eV, but the A_{STe} peak is still clearly visible in most of these structures. In this figure, only the black plot (1601-5R) is not doped with arsenic. While the CL measurements were taken at a temperature of 7 K, the PL results were obtained at room temperature. The fact that the dopant energy peak is visible at room temperature is yet another indicator that large amounts of arsenic are acting as activated dopants.

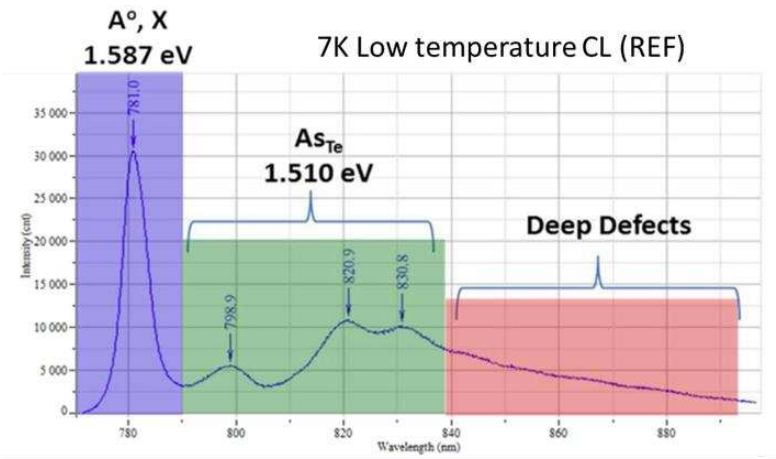


Figure 79. Low temperature CL spectrum of an As-doped device made at NREL, measurement by NREL

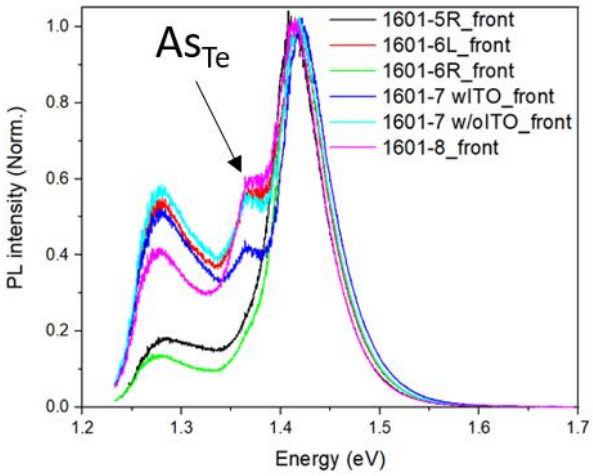


Figure 80. Room temperature PL of various As-doped device structures (1601-5,6,7,8) manufactured at CSU's PV manufacturing lab, measurement by NREL

6.2.4 Carrier Lifetimes

As previously discussed. Kephart *et al* were able to achieve excess-carrier lifetimes in excess of 400 ns using a heterostructure where CdSeTe was deposited between layers of Al_2O_3. This lifetime was orders of magnitude longer than previous findings, and was an early indicator that CdTe lifetimes could be greatly improved. Figure 81 below shows the measured TRPL curve for an arsenic-doped device, with a copper-doped device included for comparison. This

device, which used a CdSeTe:As layer the source of arsenic, did not have an Al_2O_3 layer, and yet had a measured lifetime exceeding 1 µs, nearly four times the lifetime of Kephart's heterostructure. This unprecedented lifetime can be attributed to the passivating effects of selenium at grain boundaries and interfaces as well as remarkable field effect passivation due to the graded doping. This graded doping profile bends the valence and conduction bands upward towards the rear of the device, and thus creates a barrier to the electron dark current towards the back, preventing them from reaching the recombination-prone back surface.

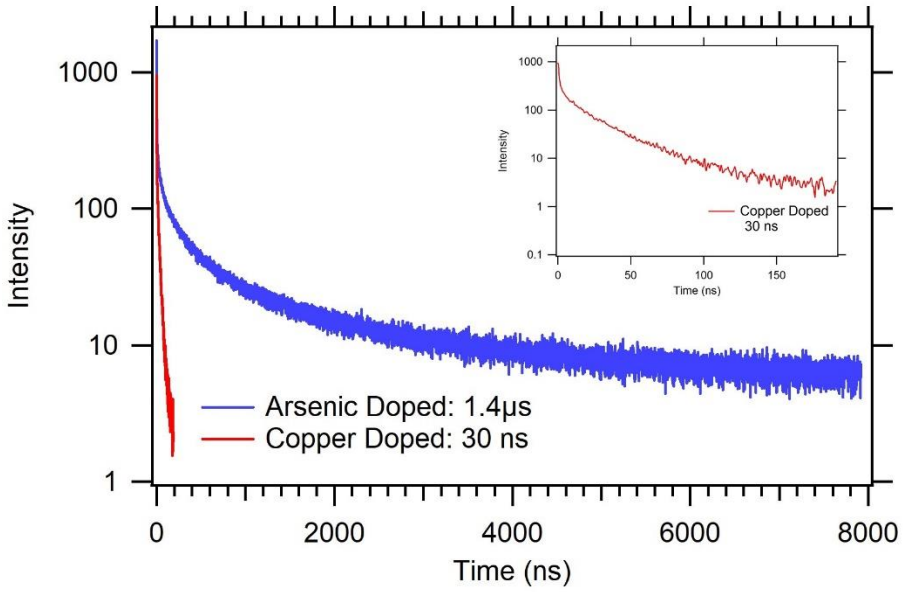


Figure 81. A comparison of TRPL decays and fit lifetimes of copper-doped (red, 1894-7) and arsenic-doped (blue, 1633-4L) devices. The copper-doped decay curve is reproduced (inset) at a shorter timescale for better visualization.

These results illustrate that diffused-arsenic doping produces devices with excess-carrier lifetimes that are orders of magnitude longer than can be obtained using any known copper-doping process. Additionally, the short excess-carrier lifetimes of non-diffused arsenic doped samples, such as were shown in Chapter 5, were evidence of poor doping activation and high

defect loads. To confirm that the diffused doping method resulted in higher quality films with less non-radiative recombination, dozens of substrates split over eight experimental runs were fabricated. In each experiment, both diffused and non-diffused samples were fabricated and measured via TRPL for direct comparison. The average lifetimes of each type of sample can been seen below in Table 5. It can be seen that the average lifetime of a diffused-arsenic doped sample was nearly 20x that of a non-diffused arsenic sample. It should be noted that there was significant variation in the lifetimes of both types of samples. It is believed that this variation is primarily due to changes in the CdSeTe, not the arsenic doping process. This will be a major point of discussion in Chapters 8 and 9. The highest lifetimes measured for diffused-arsenic doping were 2.3 µs (Figure 82) whereas non-diffused lifetimes never exceeded 75 ns, approximately equal to the lowest diffused-sample lifetimes.

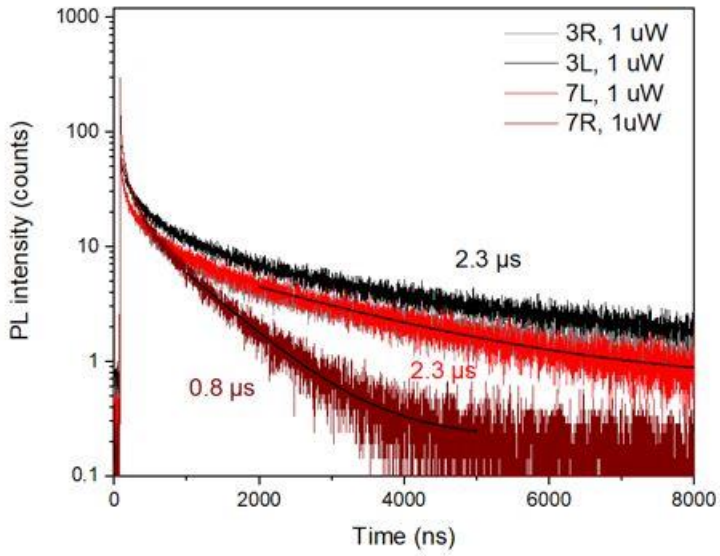


Figure 82. TRPL decay curves showing 2.3 µs lifetime for several diffused-arsenic devices. 1698-3L,R was 4 µm CdSeTe/1 µm CdSeTe:As/500 nm CdSeTe while 1698-7L,R was 1.5 µm CdSeTe/200 nm CdSeTe:As/500 nm

Table 5. Average excess-carrier lifetime for diffused vs non-diffused arsenic-doped samples

Average τ_2 lifetime as measured by TRPL	
Diffused-arsenic doped samples	**Non-Diffused arsenic doped samples**
807 ns	39 ns

6.2.5 Interface Passivation

Lifetimes such as those shown for the diffused-arsenic doped samples in the previous section are simply not possible with very high interface recombination rates. Even if the bulk material lifetime were very good, carriers would only survive long enough to reach an interface, where they would recombine. Using TRPL where the exciting laser illuminates the back interface, it is possible to study the rear surface passivation. TRPL measurements were conducted with 640 nm laser excitation from the back of the device. 640 nm was chosen to ensure the light would be absorbed where back surface recombination dominates the response. Because the lifetimes measured from the back are quite short, and the light is predominately absorbed in the area immediately adjacent to the interface, it is safe to assume that the recombination which causes the τ_1 decay is not limited by carrier diffusion. Therefore, the interface recombination velocity may be determined from the measured lifetime by Equation 12 [111], where S is the recombination velocity, α is the absorption coefficient at 640 nm, and τ_1 is TRPL lifetime.

$$S_{Back} = \frac{1}{(\alpha_{640}\tau_1)} \qquad (12)$$

Table 6 summarizes the results of measuring the back surface recombination velocity for devices containing various dopants. It clearly shows that while copper worsens the interface passivation compared to an undoped device, arsenic doping and the inclusion of CdSeTe at the back interface marginally improves it.

Table 6. Back interface recombination velocities using various dopants

Sample Structure	S_{Back} (cm/s)
MZO/CdSeTe/CdTe:Cu/Te (baseline)	1.2×10^6
MZO/ CdSeTe /CdTe (undoped)/Te	2.7×10^5
MZO/ CdSeTe /CdTe:As/ CdSeTe /Te	1.4×10^5

Yet, while this evidence that the back interface is improved by the presence of arsenic and/or selenium, the recombination velocity remains too high to reasonably allow for microsecond lifetimes. Therefore, even though the interface itself exhibits recombination velocities in the range of 10^5 cm/s, the *effective* recombination velocity is much lower. The band diagram shown below in Figure 83 is the result of DFT modelling showing upward band bending when there is a monolayer of 100% activated As_{Te} at the back of CdTe. The large amount of band bending which is induced by the graded doping towards the back of the device creates an electron reflector, which confines and repels the electrons, preventing them from ever reaching the relatively poorly passivated back interface and recombining. It is estimated, based on the exceedingly long lifetimes that the effective recombination velocity in these arsenic-doped devices are comparable to Al_2O_3 heterostuctures, with $S < 100$ cm/s.

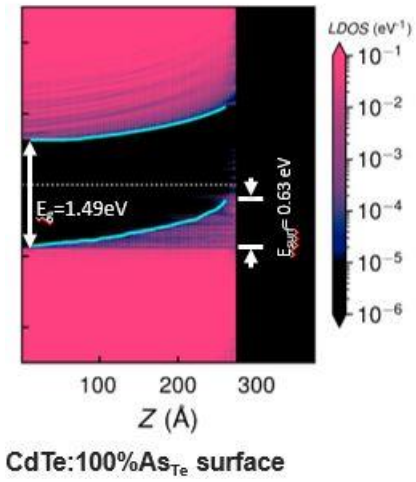


Figure 83. Upward band bending shown in the band diagram of CdTe with a single monolayer of 100% activated As_{Te} at the back. DFT modelling by Anthony Nicholson.

6.2.6 External Radiative Efficiency

Figure 84 shows the EREs for cells with both CdSeTe and CdSeTe/CdTe absorbers for undoped, diffused-arsenic doped, and copper-doped conditions. All cells utilized MgZnO as an electron contact and evaporated Te as a hole contact layer. The CdSeTe-only absorbers were 3–4 µm thick while the CdSeTe/CdTe bilayers were 500nm CdSeTe/3µm CdTe. Inspection of these data reveals several key findings. First, for all doping conditions, CdSeTe-only films consistently exhibit significantly greater radiative efficiencies than absorbers with a CdTe layer. The passivating effect of selenium on CdTe grain boundaries was well-illustrated by Fiducia *et al.* [83] and these effects are apparent here where CdSeTe-only films routinely exhibit EREs an order of magnitude greater than films with a graded bilayer. Second to note is the effect of the dopant on ERE. Undoped CdSeTe in particular exhibits remarkably high EREs, nearly 1%. The addition of diffused-arsenic doping reduces the radiative efficiency for both absorber structures, but not nearly to the extent of copper. The addition of copper drastically reduces the radiative efficiency, often by several orders of magnitude. While increasing carrier concentration is a

viable method for increasing quasi-Fermi level separation, it can be counteracted by a reduction in lifetime. Therefore the reductions in ERE noted in doped samples indicate that the current methods of doping most likely also introduces at least some recombination-active defect states, which is consistent with the finding that the activation rate is approximately 26%.

For copper-doped CdSeTe/CdTe, given the ERE shown in Figure 84 and assuming a $V_{OC,rad}$ value of 1150 mV, the implied voltage calculated by Equation 5 is approximately 880 mV. This means that current generation CdSeTe/CdTe:Cu devices, with a V_{OC} of approximately 860 mV, are nearly passivation or material quality limited, and will not produce a greater voltage until the structure is changed to increase the quasi-Fermi level splitting. Alternatively, arsenic-doped CdSeTe samples, with greatly improved ERE values, translate to implied voltages of 900–950 mV. The exact implied voltage again depends on the $V_{OC,rad}$ term and is affected by sub-bandgap absorption as will be discussed later. For this reason, the band edge, reconstructed by either photoluminescence or external quantum efficiency, must be measured for each sample for which an iV_{OC} calculation is performed [22]. Finally, it must be noted that these values represent a significant improvement compared to historical values for CdTe, which had previously been reported with an ERE of 10^{-4} %. Furthermore, the current CdTe efficiency record device exhibited an ERE of 0.008% and only a few photovoltaic technologies have reported ERE values of greater than one percent [26], [27], [112] Recent studies have shown that CdSeTe, with proper processing and the addition of passivating layers, can demonstrate radiative efficiencies of several percent, resulting in iV_{OC} values that are approaching 1 V [22].

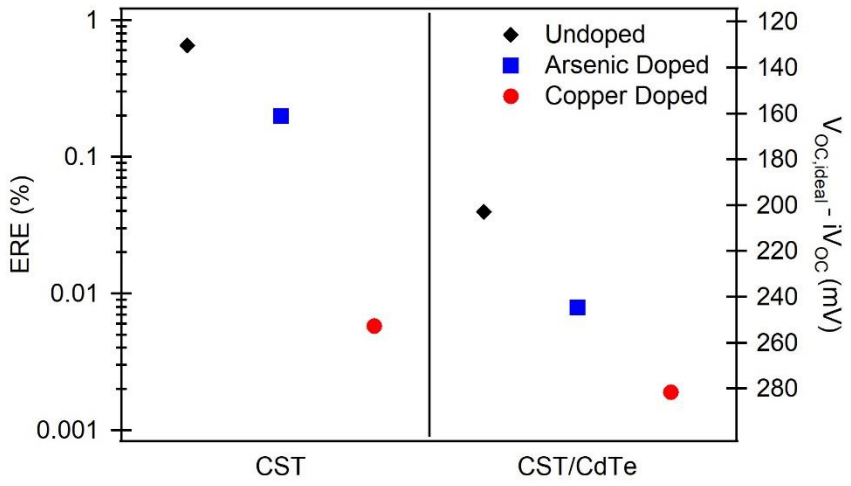


Figure 84. ERE measurements for undoped, arsenic-doped and copper-doped CdSeTe only (left) and CdSeTe/CdTe bilayer (right) absorbers.

Similar to the carrier lifetime results of Section 6.2.4, the EREs of diffused and non-diffused arsenic doped samples were compared. Indeed, the same samples which were measured for TRPL also had ERE measurements taken. The diffused-arsenic samples exhibited ERE values that ranged from 0.01 to 0.1%. The ERE of all non-diffused samples remained at or below the detection limit for the ERE tool, at approximately 0.0005%. An ERE value of 0.1% for a diffused-arsenic sample represents an increase of approximately 135 mV iV_{OC} compared to a non-diffused sample with an ERE of 0.0005%

6.2.6.1 Band Tails and Reduced Theoretical Maximum Voltage

Diffused-arsenic doping shows great potential to eliminate many of the most adverse effects of copper doping. Additionally, diffused-arsenic doped films simultaneously exhibit greater acceptor concentrations, vastly improved carrier lifetimes, and higher radiative efficiencies compared to either non-diffused arsenic or copper-doped counterparts. There remain, however, obstacles to be overcome to maximize the implied voltage of arsenic-doped devices.

PL and EQE measurements, necessary for the calculation of $V_{OC,rad}$ and iV_{OC}, reveal the presence of sub-bandgap features in arsenic-doped samples. These features indicate that sub-bandgap absorption occurs, likely due to defect states and bandgap fluctuations, and this absorption lowers the effective bandgap and thus $V_{OC,rad}$ from Equation 5, ultimately limiting the implied voltage which is possible for any given value of ERE. Determination of $V_{OC,rad}$ is highly sensitive to sub-bandgap absorptance since the blackbody radiation at 300K is quasi-exponential in the near infrared [8], [113], [114]. One such example of these sub-bandgap features can be seen in the PL emission spectra given in Figure 85a between 900 and 1000 nm. In order to determine the $V_{OC,rad}$ for these devices, absorptance was extracted by an appropriate fitting of the measured photoluminescence spectrum using the generalized Planck Law as presented by Wurfel [8] and is shown in Figure 85b. For these samples, the sub bandgap features resulted in an estimated reduction of 25 mV to $V_{OC,rad}$ for the arsenic-doped sample compared to the copper-doped sample. Similar features were reported by Moseley *et al.* in [115] for VTD-grown CdSeTe:As samples. Further investigation is needed to understand the cause of and full extent of these sub-bandgap features, as well as how different device structures or processing steps might mitigate them. This will be discussed in Chapter 9. Identifying, understanding and ultimately mitigating this sub bandgap absorption/emission will be an important step towards optimizing diffused-arsenic doped structures.

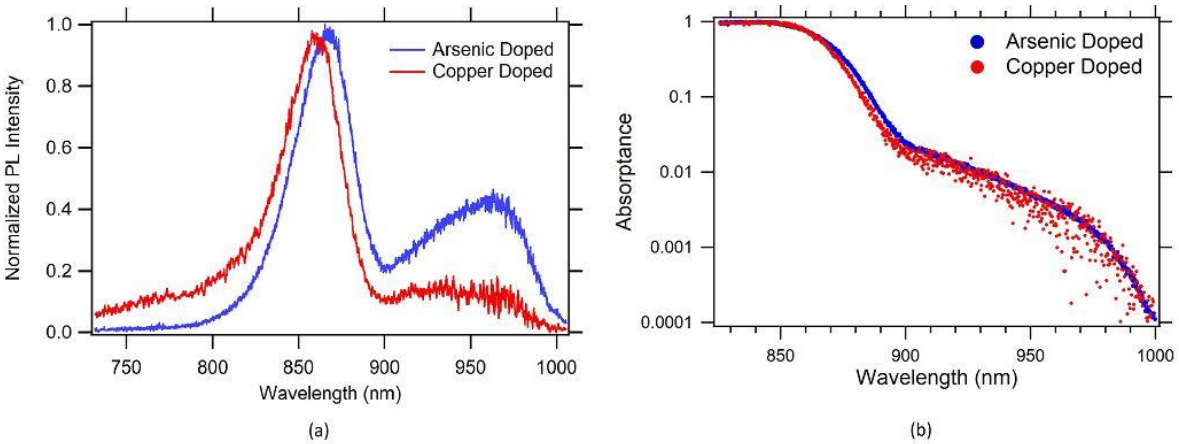


Figure 85. (a) Photoluminescence emission spectra comparing sub bandgap features in copper (red, 1732-6L) and diffused-arsenic (blue, 1732-8L) doped samples. (b) Absorptance extracted by an appropriate fitting of the measured PL spectrum shown in Figure 85a. PL fitting by Arthur Onno

6.2.7 JV Performance

Largely due to the fact that these devices, despite their numerous electro-optical improvements, have not produced a greater open circuit voltage, the 16.8% device seen in Figure 63 remains the champion device for a sample deposited from an arsenic-containing source. Of the devices which exhibit high carrier lifetimes and increased doping and a high ERE, the best device to date had a photovoltaic conversion efficiency of 13%, shown in Figure 86.

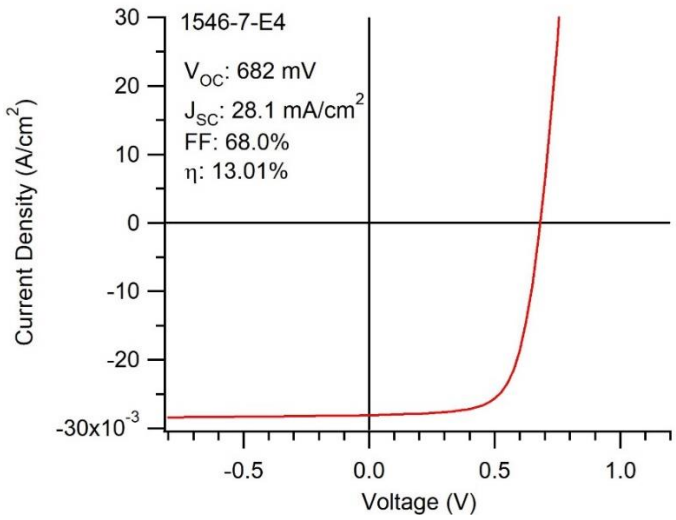


Figure 86. JV curve showing 13.0% diffused-arsenic doped device (1546-7)

At present, it is believed that this relatively poor device performance is due to three main factors. First, the deposited CdSeTe:As layer that serves as an arsenic reservoir retains all of the dimers, tetramers and complexes. It is therefore a defective and recombination-prone region within the film. As such, the device performance is severely hindered, despite the superior front layer because carriers generated within the front layer may still recombine within this defective region. Secondly, the doping profile may be inappropriate for high efficiency devices. It was previously shown that the doping profile appears to be graded within the front layer of CdSeTe from 10^{15} at the MZO interface to 10^{18} at the back. However, no experiment to date has shown high levels of arsenic doping within the CdSeTe:As reservoir layer. Therefore, it is likely that the CdSeTe:As reservoir layer has an acceptor concentration of roughly 10^{14} holes/cm^3. This graded doping profile followed by a precipitous drop in hole density would effectively create a barrier to electrons followed immediately by a barrier to holes, preventing them both from escaping. Attempts to remove the reservoir layer after the diffusion process via both chemical etch and

chemical-mechanical polish have thus far been unsuccessful, resulting only in a poorly passivated interface, low excess-carrier lifetime, and poor JV performance.

Finally, even finding a method for removing the defective material will not necessarily improve the device performance. Recall from Chapter 1 that in order to maximize solar cell performance, a device must simultaneously exhibit large quasi-Fermi level splitting and highly selective electron and hole contacts. Even when a sample has a high implied voltage, such as with many of the diffused-arsenic samples shown here, the large implied voltage is lost across the contacts and the voltage difference from electrode to electrode is far smaller than the implied voltage. In this case, the potential benefit of improved qFLS vanishes again as selectivity losses. An example of this can be seen in Figure 87, which shows the band diagram for a theoretical device with very high quasi-Fermi level splitting but poor selectivity at one of the contacts. Looking closely at the quasi-Fermi levels as they approach the hole contact (towards the right on the diagram) one can see that they begin to converge again and some of the potential voltage is lost. Figure 88 compares the various voltage losses between copper and diffused-arsenic doped samples. It can be seen that the arsenic-doped samples consistently exhibit a higher implied voltage compared to copper-doped samples. Unfortunately, they simultaneously suffer larger selectivity losses, resulting in a lower overall V_{OC}. Tellurium, the back contact used for the experiments shown here, is known to have non-ideal band alignment for hole selectivity. Shown in Figure 89, it is apparent that it would be energetically favorable for both electrons and holes that reach this interface to fall to the tellurium conduction and valence bands, respectively. Furthermore, even if only holes reach this back interface, the large offset between the valence bands of tellurium and CdTe make it such that the QFL of holes must be closer to the center than it otherwise would be, this is a selectivity loss.

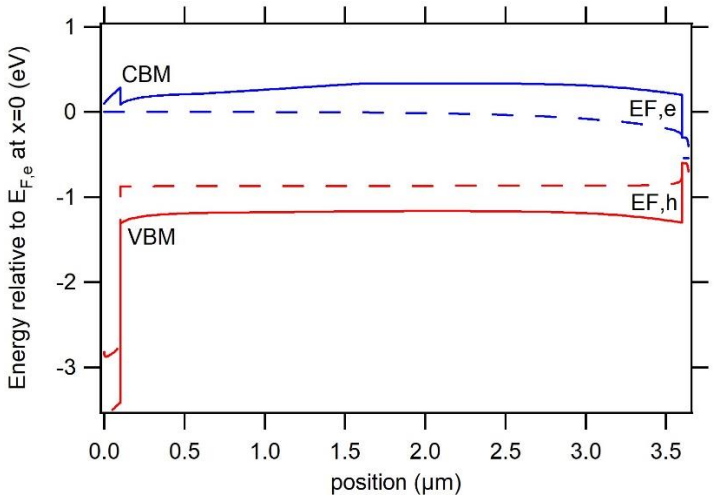


Figure 87. Band diagram of a CdSeTe device with a theoretical hole contact with severe selectivity losses. The convergence of the quasi-Fermi levels indicates voltage loss, SCAPS modelling by Carey Reich

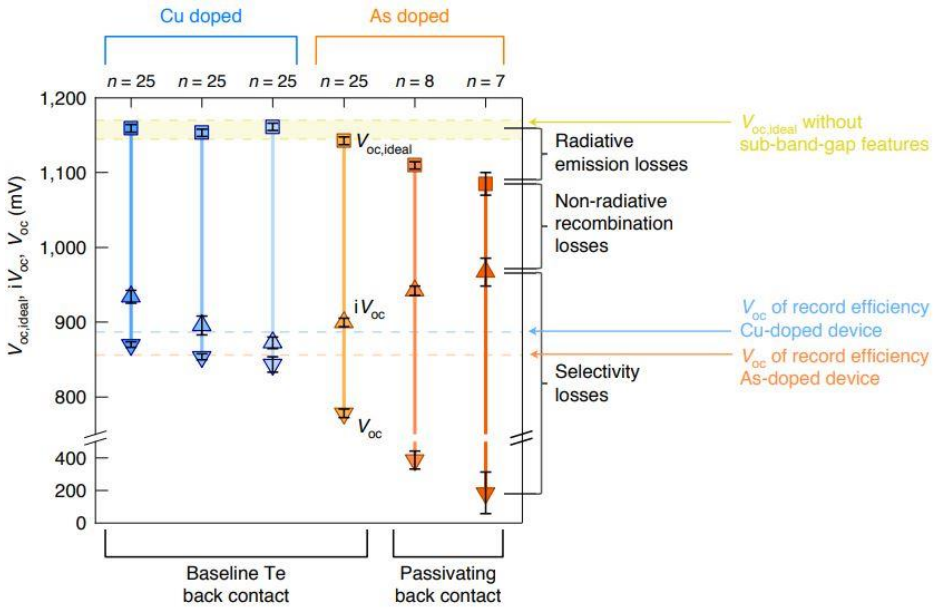


Figure 88. Voltage loss analysis for copper and diffused-arsenic doped samples showing improved implied voltage but greater selectivity losses in arsenic-doped samples, adapted from [22].

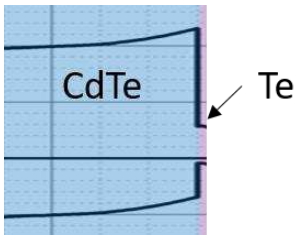


Figure 89. Band alignment of the CdTe/tellurium interface showing non-ideal hole selectivity, modelling from Ramesh Pandey

6.3 Conclusions

This chapter has provided evidence that the diffused-arsenic doping methodology is capable of producing samples with improved carrier concentration, excess-carrier lifetime, and radiative efficiency than can be produced with either copper doping or non-diffused arsenic doping. Indeed, on multiple occasions, individual samples simultaneously demonstrated acceptor concentrations in excess of 10^{15} cm^{-3}, microsecond lifetime, and EREs in the vicinity of 1%. Additionally, although the CdSeTe/Te and CdTe/Te interface has a known high recombination velocity, the graded doping profile that results from arsenic diffusion screens this defective interface. By inducing upward band bending, the graded doping profile repels electrons and minimizes the detrimental effects at the interface. **The evidence overwhelmingly supports the hypothesis that the diffused arsenic doping method produces higher quality films with far greater potential to produce photovoltaic devices with improved voltage and conversion efficiency.** The substantial improvement in ERE indicates that the bulk material is significantly improved with diffused arsenic doping as compared to other doping methods. However, additional steps remain that may further improve the device performance. Further passivation of the interfaces and the search for carrier selective contacts are the subject of Chapter 7.

CHAPTER 7. PASSIVATING OXIDES AND SELECTIVE CONTACTS

The multiple models presented in Chapter 4 all agree that interface passivation and its effect on excess-carrier lifetime strongly influences device performance. In fact, these studies indicate that as the doping levels and bulk lifetime increase, the interface becomes ever more important. Therefore, neither doping nor interfaces can effectively be studied in isolation, but need to be considered on the basis that a change in one may have a large impact on the performance of the other.

Passivation may be defined as the reduction in chemical reactivity of a bulk material, or at the surface or interface. In the context of solar cells, passivation usually refers to decreasing electron-hole recombination. $CdCl_2$, long known to be essential to CdTe's performance as a photovoltaic, passivates the bulk material and grain boundaries. Although bulk passivation is critically important, a great deal of work has already been accomplished, and the focus of this chapter is the rear interface of Cd(Se)Te. Interfaces typically contain much higher defect densities than the bulk material, and these defects create mid-gap energy states which enable extremely high recombination rates. There are two general mechanisms which can be utilized to passivate these interfaces: chemical passivation and field effect passivation.

7.1 Interface Passivation Mechanisms

7.1.1 Chemical Passivation

Any defect present at the interface represents a likely site for e-h recombination. These defects may include vacancies, interstitial atoms, dangling bonds, or large lattice strains. These may be particularly prevalent at an interface where, by definition, two different materials meet.

Therefore, chemical passivation is any process which physically reduces the interface defect density. Hydrogen has been used in numerous PV technologies to passivate surfaces, where its small size facilitates its diffusion into the surface, where it may bind to and remove dangling bonds. It is believed that chlorine fulfills a similar function at CdSeTe and CdTe grain boundaries [116]. Alternatively, native oxides have been widely used in the silicon industry to passivate the surface of silicon wafers. In this technique, thermally grown SiO_2 is grown directly on the surface of the silicon wafer. The SiO_2 has a very small lattice mismatch with the underlying silicon, and creates an interface with very low defect density [117]. This oxide layer has been the foundation of next generation silicon devices, to include the Passivated Emitter, partial Rear Contacted (PERC) and Passivated Emitter, Rear Locally diffused (PERL) structures.

7.1.2 Field Effect Passivation

Chemical passivation works by physically reducing the defect density at the interface. Alternatively, field effect passivation works by preventing either electrons or holes from reaching an area of high defect density and recombining, without materially changing the interface. According to Schottky-Mott theory, the concentrations of either electrons or holes at the interface may be controlled through the careful selection of the work functions of both the semiconductor and metal contact. When a metal is put in contact with a semiconductor, electrons will flow between them due to any work function difference between them. If the metal has a higher work function than the semiconductor, electrons will flow from the semiconductor to the metal until an equilibrium state is reached where the Fermi levels of the two are equal. This alignment of the Fermi levels causes “band bending” in the valence and conduction bands of the semiconductor. The direction of the band bending, either upwards or downwards, depends on whether the work function of the metal is greater or less than that of the semiconductor. Such

band bending is illustrated for both situations in Figure 90 below. Figure 91 shows band bending in a p-type semiconductor when contacted with a lower work function metal, the downward band bending is very similar to current CdTe contact structures. This downward band bending creates an energy barriers which impedes hole extraction, which is problematic because the back contact is the hole contact. Opposingly, a higher work function metal induces upward band bending, which repels electrons and reduces interface recombination. The selection of a material with an appropriate work function is particularly important when creating carrier selective contacts, as will be discussed in a later section of this chapter.

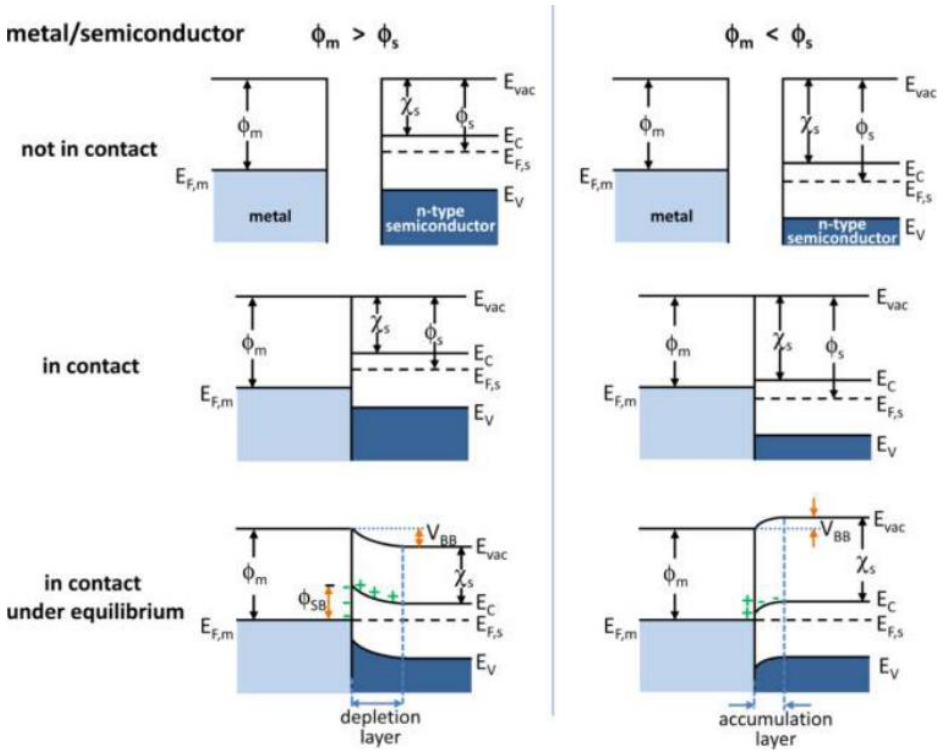


Figure 90. Band bending induced by differing work functions with n-type semiconductors, adopted from [118]

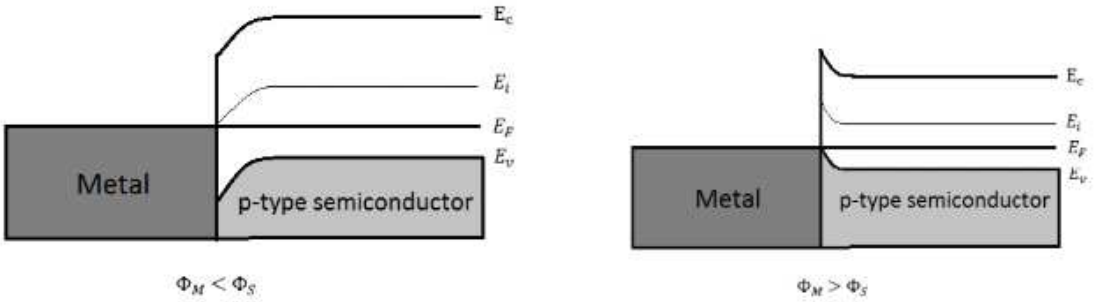


Figure 91. Band bending induced in a p-type semiconductor by a lower work function metal (Left) and higher work function (right), adopted from [119]

High levels of doping, particularly near an interface, may also create field effect passivation. Using CdTe's rear interface as an example, high levels of p-type doping increases the number of holes. This would, in turn, push the Fermi level down nearer the valence band, but because there may only be one Fermi level present at the interface, this may rather be visualized as the valence and conduction bands bending upwards, as in Figure 92 which has been repeated from earlier, this time with an emphasis on the band bending. The upward band bending represents an energy barrier which prevents electrons from reaching the rear interface. Importantly, the amount of band bending (and thus the energetic barrier) that can be achieved only through doping is constrained because the band gap, determined by the valence/conduction band locations, is set. Utilizing a separate material with a large band gap and appropriate band alignment is a much more effective method to reduce the current of the unwanted carrier.

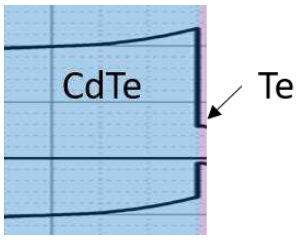


Figure 92. Upward band bending induced by p-type doping, modelling from Ramesh Pandey

Finally, field effect passivation may also be obtained through the use of a fixed-negative charge dielectric, such as Al_2O_3. In aluminum oxide, native defects, including aluminum vacancies and oxygen interstitials exhibit a negative charge. These defects are prevalent in tetrahedrally oriented Al, the dominant orientation when Al_2O_3 is grown on silicon [120]. This fixed negative charge induces band bending which repels electrons, and has been observed to passivate the interface of p-type silicon wafers [121].

7.2 Previous Passivating Oxide Work

The role which passivating oxides has played in the development of silicon devices cannot be understated. Optimizing the oxide layers has been a crucial step in engineering devices with greater than 20% conversion efficiency. The ubiquitous nature of passivating oxides in high performing silicon devices has in turn inspired a great deal of work within the CdTe community. This work has sought to reap the same performance improvements that silicon devices currently enjoy.

7.2.1 Electron Contact Work

It is important to consider that all solar cells must have two contacts, one for each charge carrier. Because of work function-induced band bending, each contact must be individually engineered, and it is not uncommon for one of the contacts to be more problematic than the

other. Therefore, the discussion of previous research has been divided into separate sections for the electron and hole contacts. Note that in this work, electron contact may be used synonymously with front contact, and hole contact with back or rear contact.

Until recently, most CdTe devices included a thin layer of CdS to act as the n-type partner to the p-doped CdTe. CdS could be easily doped and its small lattice mismatch with CdTe aided in forming a reasonably passivated interface. However, Perkins *et al* noted that the as-deposited interface was not as well passivated as after a $CdCl_2$:O treatment. They found that the $CdCl_2$:O treatment formed a layer of sulfur and tellurium oxides. The prevalence of these oxides correlated well with device performance, which the authors attributed to improved front interface passivation [122].

A major advancement in research-scale CdTe technology occurred when CdS was replaced with MgZnO (MZO). MZO served as a high resistance transparent layer, and a 50-100 nm layer with a magnesium content between 10–23% was found to be optimal. MZO devices were found to have improved J_{sc} compared to CdS devices, because they avoided the parasitic absorption of the blue light spectrum found in CdS. Kephart showed that by adjusting the magnesium content in the MZO film, the conduction band alignment could be changed from a “cliff” to a “spike”. Increasing the magnesium corresponded with a conduction band spike, which in turn reduced interface recombination and produced improved open-circuit voltage [123]. It was discovered that increasing the conduction band spike up to 0.3 eV produces an increase in voltage, but any larger offset creates a barrier to electrons which is too great to overcome via thermionic emission, manifesting as a kink in the JV curve. The 3.7 eV band gap of MZO [124], paired with a small conduction band offset, corresponds with the very large valence band offset between the MZO and CdTe as illustrated in Figure 93.

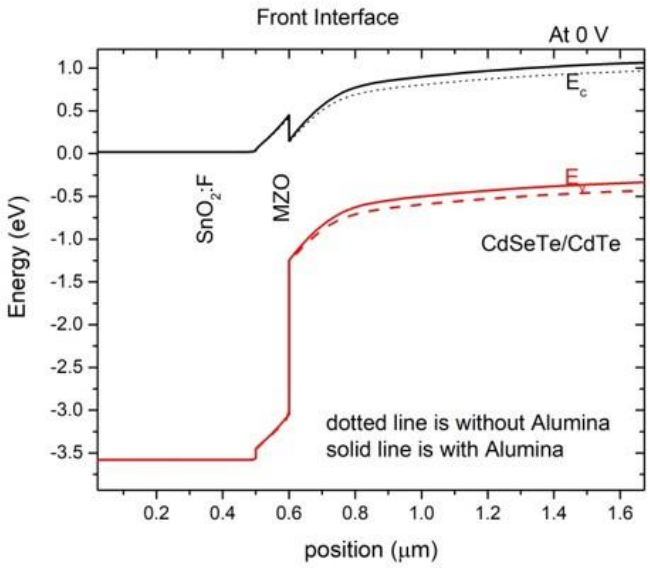


Figure 93. MZO/CdSeTe/CdTe band alignment, showing a large valence band offset and a small conduction band "spike", modelling by Ramesh Pandey

This large offset drastically reduces the hole population at the MZO/Cd(Se)Te interface. The conduction band spike, although much smaller, is hypothesized to serve a similar role for electrons: reducing the number present at the interface while still allowing for electron transfer into the underlying TCO. The recombination rate, being a product of the number of electrons and holes at the interface, is drastically reduced, and recombination velocities of less than 100 cm/s have been observed from the MZO/CdSeTe interface. The thorough passivation and small conduction band spike account for the improved open-circuit voltage.

7.2.2 Hole Contact Work

As discussed earlier, it is beneficial to select contacts with appropriate work functions to ensure proper band alignment and possible band bending. For the hole contact, this requires a large conduction band offset and upward band bending going into the contact. However, due to CdTe's unusually high work function of 5.7 eV, it has proven difficult to find a viable material

with an equal or greater work function. It is unsurprising, therefore that CdTe's back contact has historically been problematic, as most contacts exhibit a smaller work function, inducing downward band bending which inhibits hole extraction rather than aid it.

At Colorado State University, a tellurium back contact has typically been deposited behind the CdTe. This has historically been done based on experimental results which show that an improvement in voltage and fill factor with the inclusion of approximately 30 nm of Te [125]. It has been hypothesized that Te mitigates the downward band bending that would otherwise be present, and recent first-principles work by Nicolson *et al* has shown upward band bending when Te is deposited on [111] oriented CdTe, as seen below in Figure 94 [126]. Despite this band bending, the passivation of the CdTe/Te interface remains poor, with measurements indicating an interface recombination velocity of approximately 10^6 cm/s [127].

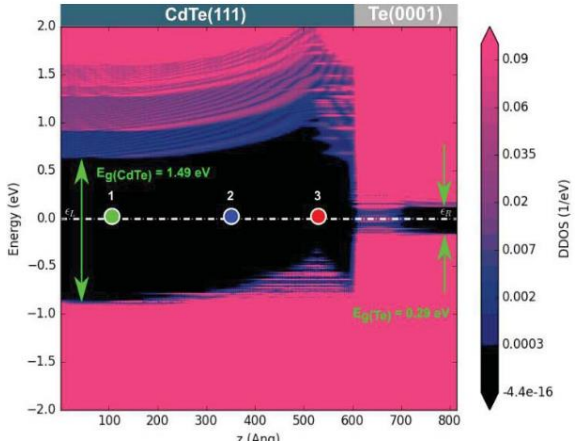


Figure 94. Band alignment at the [111]CdTe/Te Interface, adopted from [126]

NiO has been proposed as an alternative hole contact due to its high work function and good band alignment with CdTe. Xiao *et al*, using X-ray photoelectron spectroscopy (XPS) techniques, found that when deposited by electron beam evaporation, NiO has a large conduction

band offset of 2.68 eV and a relatively small valence band offset of 0.52 eV, is conducive to hole transport. Figure 95 shows the band alignment as measured as a part of that work. Using this alignment, the authors measured an increase in V_{OC} of 65 mV, from 724 to 790 mV, compared to a baseline which had a CdTe/metal back interface.

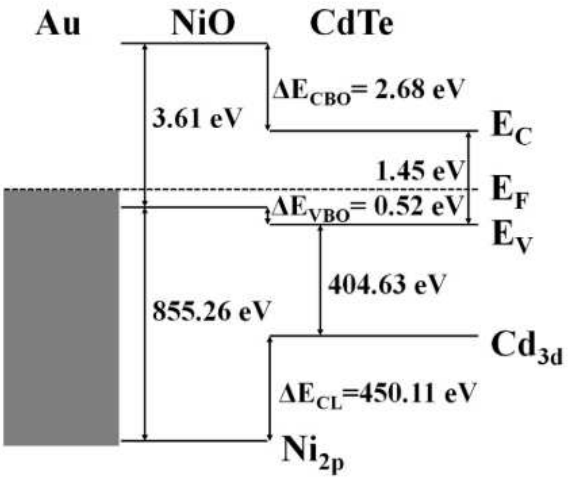


Figure 95. Band alignment of the NiO/CdTe interface, adopted from [128]

Kephart *et al*'s work with aluminum oxide on CdTe has already been cited as foundational to the work present herein. Using an Al_2O_3/CdSeTe/Al_2O_3 heterostructure, they achieved τ_2 lifetimes of 430 ns, as seen below. While this indicates that the CdSeTe/Al_2O_3 interface is well passivated, the underlying mechanism for this passivation is still unknown. It may be that the Al_2O_3 contains a fixed negative charge, as has been observed when it is deposited on silicon. Alternatively, because the aluminum vacancies and oxygen interstitials appear to coincide with tetragonal Al_2O_3, it may not be present when grown on CdTe. Perkins *et al*, have proposed an alternative passivation mechanism. They found that well passivated interfaces of CdTe and Al_2O_3 corresponded with an increase in the Te^{+4} peak during XPS

measurements [129]. They concluded that a tellurium oxide may be forming under the Al_2O_3 during the $CdCl_2$ treatment process, and that is providing chemical passivation at the interface.

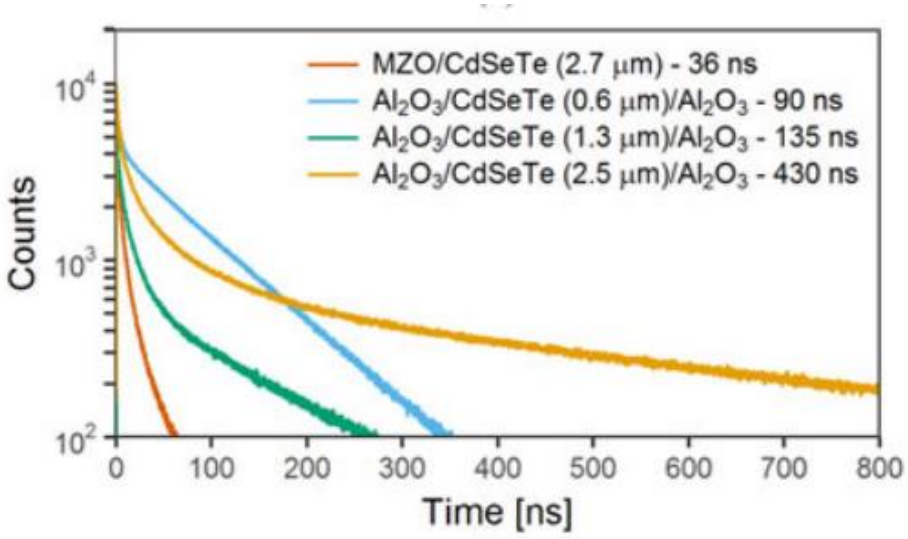


Figure 96. TRPL lifetimes measured for various CdSeTe heterostructures, adopted from [130]

The wide band gap of aluminum oxide (7.6 eV) ensures that very large offsets exist at both the valence and conduction bands when deposited onto CdTe [131]. These large band offsets, shown below in Figure 97, prevent either electron or hole transport when the oxide layers are as thick as in Kephart's work (20–100 nm). However, if the oxide layer is made thin enough, and with sufficient band bending, carriers may pass through this barrier via quantum tunneling. Tunneling transport is the fundamental concept behind the TOPCon (tunnel oxide passivated carrier- selective contacts) structure found with silicon devices. In these structures, the absorber is completely covered in a very thin (0.5–1.8 nm) oxide layer, typically SiO_2 [132]. A highly doped layer, either n or p as appropriate, is deposited onto the oxide layer, which aids in the tunneling transport of one carrier while the other is effectively blocked. Being completely encased in an oxide, this device structure typically exhibits phenomenal passivation compared to partial rear contacted structures. Although SiO_2 is most prominent in the TOPCon structure,

Al_2O_3 has also shown very impressive levels of passivation [121]. While it is generally agreed that the majority of the carrier transport is via quantum tunneling, debate still exists as to whether microscopic pinholes in the oxide are beneficial to device performance [133].

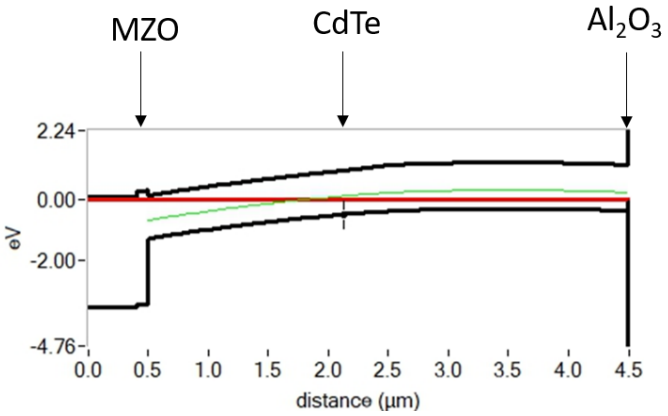


Figure 97. Band structure with large VBO/CBO at CdTe/Al_2O_3 interface, modelling from Ramesh Pandey.

7.3 Hypothesis III

Even with graded doping profiles, passivating the back surface with aluminum oxide will improve the quasi-Fermi level separation, indicated by increasing ERE.

Literature from the silicon industry, where passivating oxides are most prevalent and well understood, indicates that even when the absorber doping is optimized, devices are improved with the addition of a passivated interface and selective back contact. Therefore, although the graded doping shown in Chapter 6 is extremely promising, it is likely that additional back contact layers will further improve the device performance.

7.4 Hypothesis III Results

Based on the previous work, multiple experiments were conducted where thin layers of Al_2O_3 were deposited onto CdSeTe and CdTe structures using either atomic layer deposition (performed at ASU) or magnetron sputtering of an oxide target. Resultant devices were characterized to measure the lifetimes, luminescence, and photovoltaic conversion efficiency to discern the effectiveness of aluminum oxide as a passivating and carrier selective contact for Cd(Se)Te.

7.4.1 Luminescence Results

In order to better understand the mechanics behind the passivation, Al_2O_3 films of various thicknesses were deposited. It was found that when only Al_2O_3 was deposited behind the CdTe, the PL response grew as the Al_2O_3 became thicker, as seen in Figure 98. Additionally, no peak-shift was noted as the aluminum oxide became thicker, which indicates that within this thickness range, the thicker oxide did not significantly affect the amount of selenium diffusion from the CdSeTe into the CdTe during the $CdCl_2$ treatment. Although increasing the aluminum oxide thickness shows a dramatic increase in the photoluminescence when it is very thin, the marginal gain diminishes rapidly at thicknesses greater than 4 nm. This indicates that most of the passivation mechanism occurs at the immediate interface, and is not reliant on the bulk Al_2O_3. Additionally, increasing the Al_2O_3 layer thickness likely improves the total coverage/continuity of the film (in the case of sputtered Al_2O_3) when it is very thin, but becomes less impactful as the thickness increases.

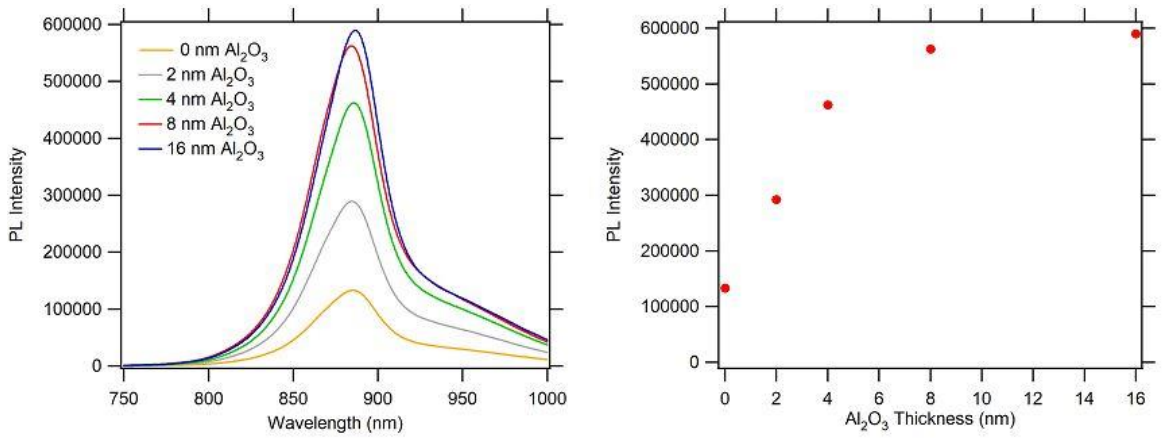


Figure 98 (a) PL spectra of CdSeTe/CdTe devices (1537) with increasingly thick layers of aluminum oxide deposited at the back surface. (b) Plot showing the PL peak intensity for the curves shown in (a) revealing an asymptotic increase in intensity with thickness

In order for aluminum oxide to be successfully incorporated into a device structure, and allow quantum tunneling, it must be kept very thin, likely less than 2 nm. Additionally, while the large conduction and valence band offsets seen in Figure 97 facilitate the passivating nature of Al_2O_3, but they do nothing to aid in hole extraction. For that, additional back contact layers are needed with an appropriate band alignment to encourage hole transport to the external circuit. Figure 99 shows large increases in photoluminescent response as aluminum oxide, highly p-doped amorphous silicon (a-Si:H), Indium Tin oxide (ITO), and silver are sequentially added to CdSeTe/CdTe devices. The back contact layers deposited after the aluminum oxide was chosen based on their proven performance as a hole contact in silicon devices. This shows that back-contact processing steps can further reduce the non-radiative recombination within the device. The addition of the Al_2O_3 results in an increase in PL from approximately 30k counts to more than 100k counts. This is followed by an even greater increase up to 400k counts with the addition of the a-Si:H, ITO and a silver back contact. Several phenomena are likely contributing to the interface passivation. In addition to the passivation provided by the Al_2O_3 itself, further

upward band bending induced by the highly p-doped a-Si, may also repel electrons from the Al_2O_3 interface, further reducing the electron population at the back. Finally, when the device was annealed in air at 200°C for 10 minutes, the PL doubled again to more than 700k counts. It is hypothesized that during this anneal, hydrogen, present in the a-Si, may diffuse towards the interface, chemically passivating dangling bonds. Combined, the addition of Al_2O_3, a-Si:H, ITO, and Ag with an anneal increased the PL response by more than an order of magnitude, from the baseline CdSeTe/CdTe device.

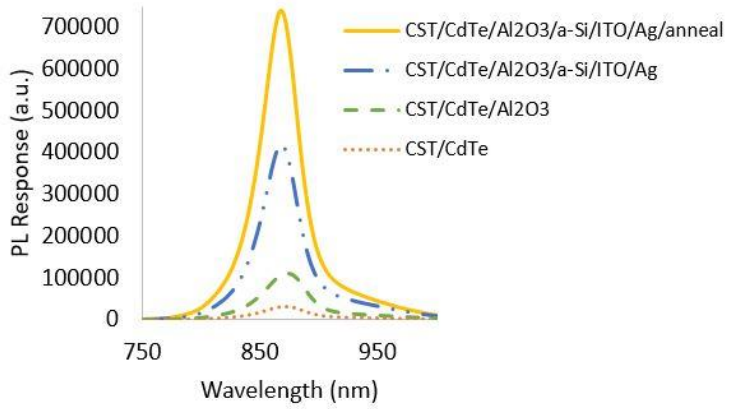


Figure 99. Plot showing the PL response of a CdSeTe/CdTe device structure (1481) where back contact layers are sequentially added. It shows a large and consistent increase in PL with the addition of each layer or process

7.4.2 Carrier Lifetimes

Similar to the substantial increase in steady state photoluminescence, Time-Resolved Photoluminescence (TRPL) measurements show that the addition of the aluminum oxide at the back surface greatly increases the carrier lifetime. Whereas CdSeTe/CdTe devices typically have measured lifetimes from 10–100 ns, CdSeTe-only devices with Al_2O_3 displayed excess-carrier lifetimes of up to 8 µs, as seen in Figure 100. **To the author's knowledge, these are the highest carrier lifetimes ever measured in polycrystalline CdSeTe or CdTe devices.** In this study,

Atomic Layer Deposition (ALD)-deposited alumina was compared against sputter-deposited alumina for both differing layer thicknesses and for both CdSeTe-only and CdSeTe/CdTe absorbers. A couple of key findings in this study merit discussion. First, there is a radical difference between the lifetimes which may be achieved using only CdSeTe compared to a CdSeTe/CdTe bilayer. The CdTe layer exhibits a significantly shorter lifetime, and it therefore limits the overall lifetime. The gains of a well-passivated back interface do not manifest when the charge carriers have to traverse a very low lifetime material. This is strong evidence that a CdSeTe-only device structure will be capable of a far greater conversion efficiency. Secondly, contrary to expectations, the ALD-deposited alumina did not result in longer lifetimes compared to a sputtered oxide. Typically, the sputtering process could be expected to introduce sputter damage that might create non-radiative recombination sites within the lattice as energetic ions bombard the surface. However, no evidence of this is present in the TRPL lifetimes. It seems that either the CdSeTe is resilient to sputter damage at the sputter conditions used, or more likely that the post-deposition $CdCl_2$ treatment repairs and removes most of the damage. This is an important finding as sputtering is highly compatible with the rapid manufacturing processes which CdTe photovoltaics are associated with. Next, there is not a significant difference between the lifetimes for 1 nm and 10 nm layers of sputtered Al_2O_3. This is further evidence that most of the passivation occurs directly at the surface and the total volume of alumina is not as important. Finally, lifetimes approaching 10 µs represent a fundamental paradigm shift compared to traditional CdTe devices with excess-carrier lifetimes of only a few nanoseconds. With extremely short lifetimes, the field is extremely important, as it is needed to quickly separate the carriers and sweep them to their respective contacts before they recombine. This is not nearly important in a microsecond device, where the carriers may survive long enough to traverse the

full film thickness many times before recombining. Such long lifetimes enable the possibility of device structures that do not have a built-in field, relying on well-passivated contacts with appropriate band alignment to dictate the flow of charge carrier currents.

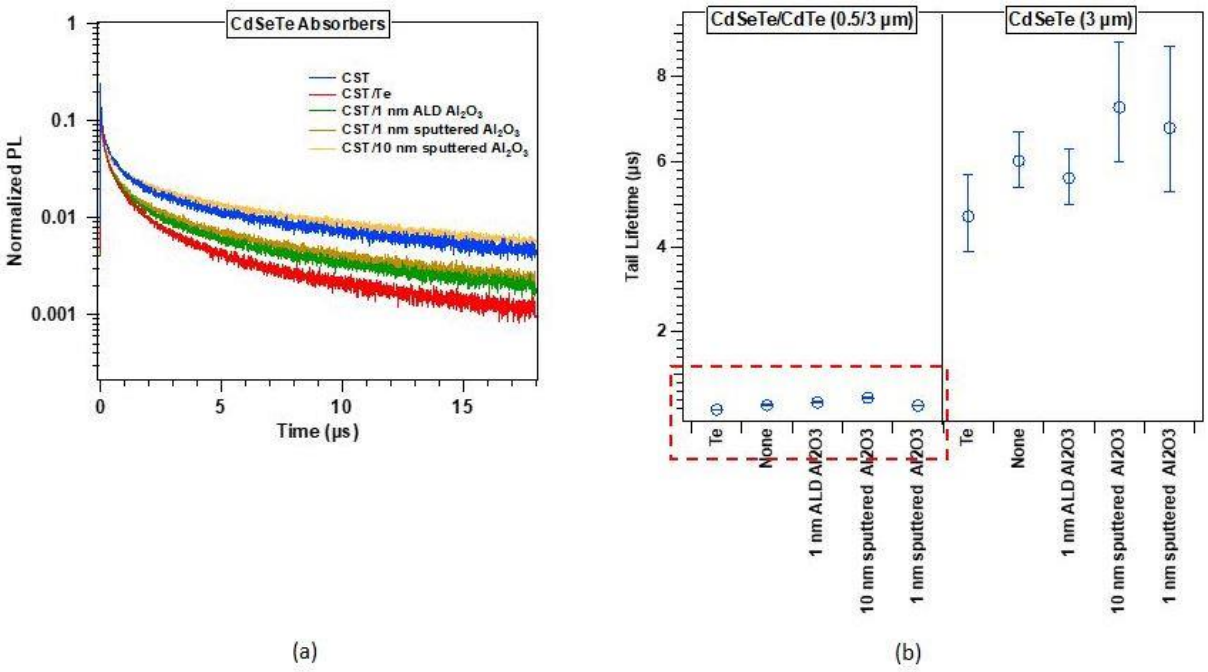


Figure 100. (a) TRPL decays for CdSeTe films with either no back contact, a tellurium back contact, or alumina passivation layer (ALD or sputtered). (b) TRPL tail lifetimes for both CdSeTe/CdTe and CdSeTe-only absorbers with various back contacts

7.4.3 Interface Passivation

The long carrier lifetimes measured in the previous section are due in large part to improved interface passivation at the back surface. Similar to the doping work, TRPL was measured from the back to measure the back surface recombination velocity. As Table 7 shows, there is a mild improvement in the back surface recombination velocity when aluminum oxide is deposited, compared to a baseline device with a tellurium back contact. This improvement is present even on a copper-doped sample. Given that copper is known to drastically increase non-radiative recombination, the fact that the overall recombination velocity has decreased indicates

that aluminum oxide is passivating the interface and possibly mitigating some of the negative effects of copper. That being said, it is still has higher recombination than an undoped device with the tellurium back contact, so it clearly cannot completely remove the deleterious effects of copper.

Table 7. Back interface recombination velocities for CdSeTe/CdTe with various back contacts

Sample Structure	S_{Back} **(cm/s)**
MZO/CdSeTe/CdTe:Cu/Te (baseline)	$1.2x10^6$
MZO/ CdSeTe /CdTe:Cu/Al_2O_3	$8.3x10^5$
MZO/ CdSeTe/CdTe/Te (undoped)	$2.7x10^5$

7.4.4 External Radiative Efficiency

The improvement in interface passivation may also be seen in the ERE measurements of Figure 101. The addition of a 2 nm layer of Al_2O_3 improves the ERE by an order of magnitude. Several higher performing baseline copper-doped CdSeTe/CdTe devices with high conversion efficiencies and V_{OC}s still display ERE's of only approximately 0.01%. The addition of Al_2O_3 by contrast increases the ERE to 0.1%. Later experiments with an optimized CdSeTe absorber boosted the ERE as high as 2.3%

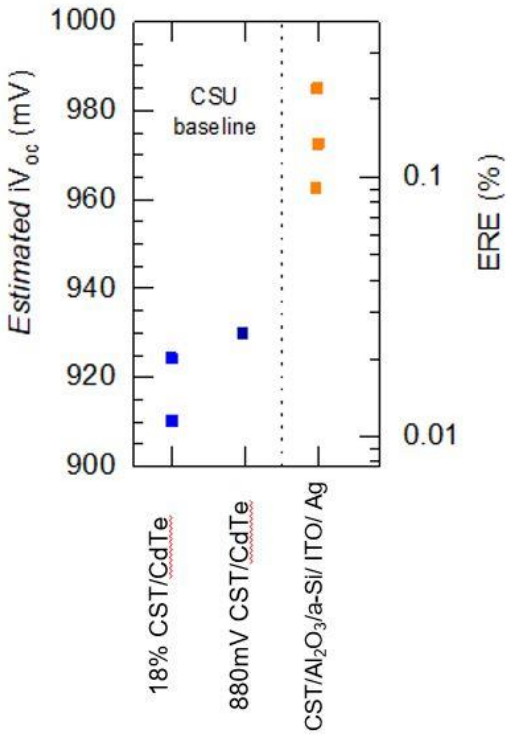


Figure 101. ERE measurements for a passivated back contact sample, compared to the ERE of high-performing baseline structures, ERE measurements performed at ASU

7.4.4.1 Band Tails/sub bandgap features

Similar to with replacing copper doping with arsenic, the inclusion of an alumina passivating layer significantly improves the external radiative efficiency. The greater proportion of radiative recombination, in turn, increases the implied voltage of the device. However, it is necessary to inspect the band edge using EQE or PL for band tails or sub-bandgap features. These features reduce the effective bandgap of the material and therefore reduce the $V_{OC,rad}$ term in equation 5. The reduction of this term means that the implied voltage for any given ERE will be lower than in a sample without such features. Figure 102 shows the sub bandgap features for both copper and arsenic-doped samples with either a tellurium or an Al_2O_3 back contact. For both dopant cases, the passivating oxide increases the prevalence of the sub bandgap features,

reducing the $V_{OC,rad}$ term by up to 75 mV depending on the severity [22]. However, despite this reduction in $V_{OC,rad}$, the increased luminescence still results in an overall increase in the implied voltage compared to a non-passivated and especially a copper-doped sample.

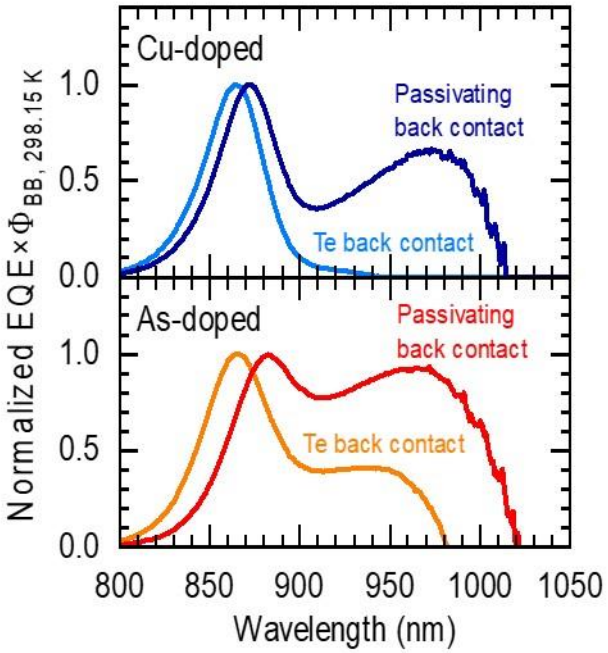


Figure 102. Plot revealing the presence of large band tails and sub bandgap features reconstructed from EQE. The features are larger with aluminum oxide for both copper and arsenic-doped samples, adapted from [22]

7.4.4.2 Implied JV Curves

Utilizing ERE measurements taken as the light injection is modulated (known as the SunsERE method, it is possible to construct an implied JV curve for a sample using only its photoluminescence emission. The same samples for which the TRPL lifetimes were shown were also measured using SunsERE. The resulting implied JV curves can been seen in Figure 103 and the implied efficiencies are shown in Figure 104 . Similar to with carrier lifetimes, we see that CdTe is fundamentally limiting the potential performance of these device. CdSeTe/CdTe bilayers are limited to an implied voltage of approximately 900 mV and an implied efficiency of

approximately 22–23%. By contrast, CdSeTe-only devices exhibit implied voltages of 1000 mV and implied efficiencies of 25–26%

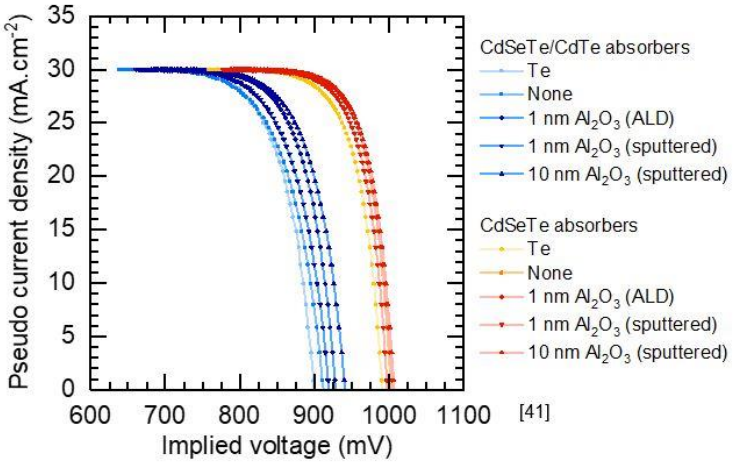


Figure 103. Implied JV curves for CdSeTe/CdTe (Blue) and CdSeTe-only (Red/Orange) samples with various back contact structures

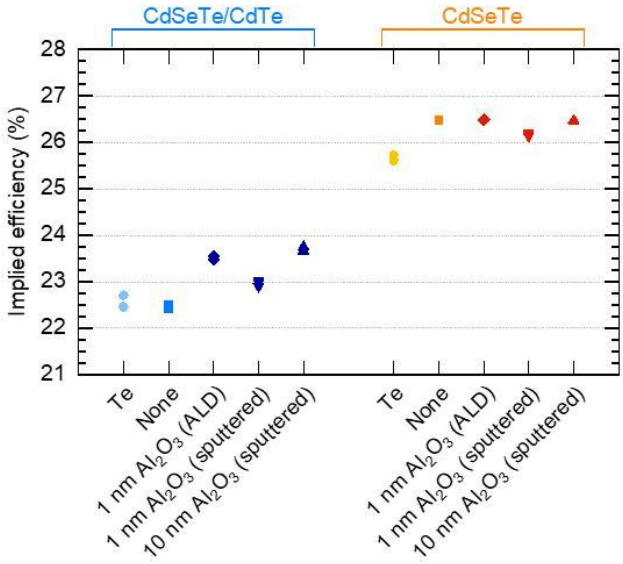


Figure 104. Implied efficiencies for CdSeTe/CdTe (Blue) and CdSeTe-only samples (Red/Orange) with various back contact structures

7.4.5 JV Performance

Figure 105 shows the best (in terms of JV performance) Al_2O_3 back-contacted device made to date. This device contained 2 nm of Al_2O_3, 8 nm of p^+ a-Si, and approximately 70 nm of ITO. Despite the substantial increase in excess-carrier lifetime previously shown, this does not yet translate into improved open-circuit voltage. This device exhibited a V_{OC} below 780 mV, whereas a good baseline device without aluminum oxide may show as high as 860 mV. Additionally, the poor fill factor and the notable rollover seen in the JV indicates that the oxide layer has increased the series resistance and created a hole barrier which has not yet been overcome. As previously mentioned, the Al_2O_3 is excellent at passivating the back interface, but by itself it does not help with hole extraction. The highly p-doped α-Si was intended to serve this purpose by inducing enough upward band bending to make a hole-selective contact. However, functioning devices such as shown here are only obtained when the $CdCl_2$ treatment follows the deposition of the Al_2O_3, a-Si, and ITO. It is currently unknown what effect the high temperatures and $CdCl_2$ treatment may have on the properties of these materials. Particularly, if the doping levels of the a-Si were drastically changed by the $CdCl_2$ treatment, it may no longer function as a hole contact as intended.

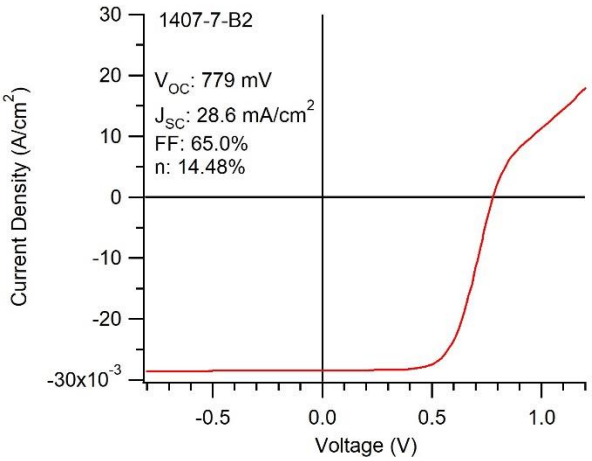


Figure 105. Best JV performance of an Al_2O_3 back-contacted device (1407-7)

7.5 Results of Combining Al_2O_3 and Diffused-Arsenic Doping

While diffused-arsenic doping and Al_2O_3 passivation each individually improve the electro-optical properties of Cd(Se)Te devices, the combination of both results in further improvement in interface passivation and ERE while maintaining excellent lifetimes. This is consistent with the idea that improved doping densities, high bulk lifetimes, and less non-radiative interface recombination both contribute to greater quasi-Fermi level separation.

7.5.1 Carrier Lifetimes

Figure 106 below shows the structures and resulting TRPL lifetimes of devices fabricated during experiments which combined arsenic-doped CdSeTe absorbers with an aluminum oxide back contact layer. All of these devices demonstrated a measured τ_2 lifetime of greater than or equal to1.4 μs, reaching a maximum of 2 μs for a device with the full Al_2O_3/a-Si/ITO/Ag back contact stack. These lifetimes are slightly lower than what has been obtained with undoped CdSeTe films, which is consistent with the diffused-arsenic doping work which showed a slight reduction in carrier lifetime. Nonetheless, at more than a microsecond, these lifetimes remain among the highest ever measured for Cd(Se)Te samples.

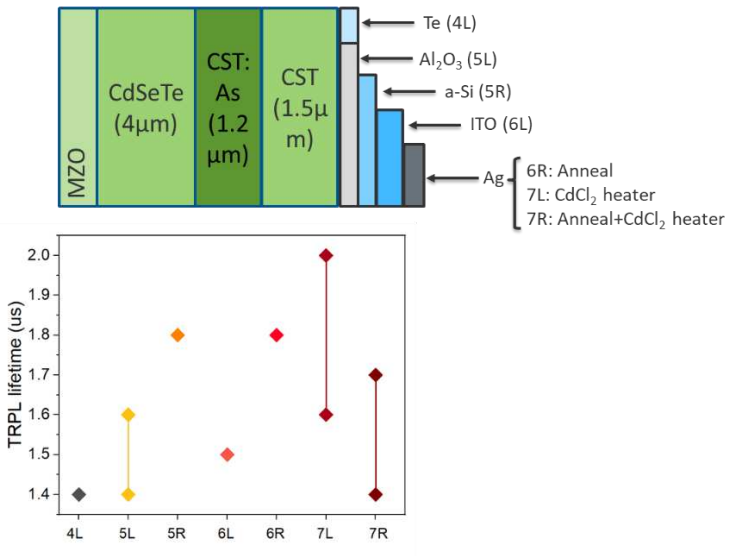


Figure 106. Device structures and TRPL lifetime measurements for devices with diffused-arsenic doping and Al_2O_3 back contacts (1633)

7.5.2 Interface Recombination

The effects of both arsenic doping and aluminum oxide on the back surface recombination velocity have already been shown. Table 8 below offers a full summary of these effects, along with data points for devices that contain both arsenic and aluminum oxide. As previously noted, the inclusion of arsenic and aluminum oxide separately each result in an improved back surface compared to a copper-doped, tellurium-contacted device. When both are utilized, the back surface recombination velocity drops by nearly 2 orders of magnitude compared to the baseline device, from 1.2×10^6 cm/s to 5.0×10^4 cm/s.

Table 8. Back surface recombination velocities for devices with As-doping and Al_2O_3 back contacts (Experimental Run 1601)

Sample Structure	S_{Back} (cm/s)
MZO/CdSeTe/CdTe:Cu/Te (baseline)	$1.2x10^6$
MZO/ CdSeTe /CdTe:Cu/Al_2O_3	$8.3x10^5$
MZO/ CdSeTe /CdTe/Te (undoped)	$2.7x10^5$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Te	$1.4x10^5$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Al_2O_3	$9.0x10^4$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Al_2O_3/a-Si	$8.0x10^4$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Al_2O_3/a-Si/ITO	$5.0x10^4$

7.5.3 External Radiative Efficiency

As both TRPL effective lifetime and interface recombination velocities are measures of e-h recombination rates, it comes as no surprise that improvements in both manifest as improvements to the ERE. Figure 107 and Figure 108 show the ERE measurements from two separate experimental runs utilizing both diffused-arsenic doping and Al_2O_3 passivation. The samples in Figure 107 used CdTe:As as the arsenic source and are compared to copper-doped and undoped samples. These devices all had a base CdSeTe/CdTe:As/CdSeTe structure (1601-6R). Additional devices included subsequent layers of Al_2O_3 (1601-6L), ITO (1601-7) and Ag (1601-8). 1601-4 was undoped while 1601-5 was copper doped, and 1601-10 was copper doped with a layer of Al_2O_3. It can be seen that even the undoped sample is a significant improvement over the previously reported ERE values for CdTe, largely due to the addition of selenium. However, copper-doping does not improve or reduces the radiative efficiency. Alternatively, arsenic is shown to consistently improve ERE by nearly 2 order of magnitude, up to maximum of nearly 2% when combined with Al_2O_3.

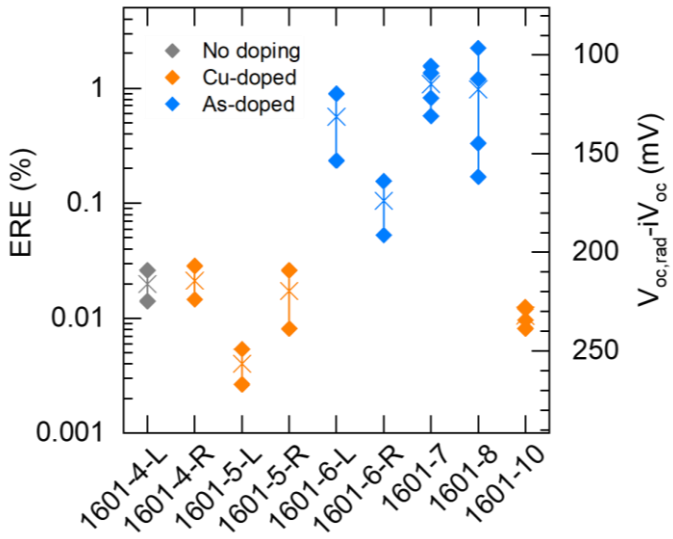


Figure 107. External radiative efficiencies for CdSeTe/CdTe devices with various dopants

Figure 108 shows the radiative efficiencies for devices with the same structure except the CdTe:As is replaced with CdSeTe:As. A systematic increase in the radiative efficiency is noted with the addition of each subsequent layer of Al_2O_3, a-Si, ITO, and Ag. In this plot all devices had a base structure of CdSeTe/CdSeTe:As/CdSeTe (1633-4L and 4R.) Each device after added a subsequent layer to the back contact: Al_2O_3 (1633-5L), p^+ α-Si (1633-5R), ITO (1633-6L), and Ag (1633-6R). 1633-7L and 7R were identical to the 1633-6R structure, but received a $CdCl_2$ treatment with a top heater temperature ten degrees hotter than all other samples. **The best ERE measured during this experiments was over 4%, not only is this higher than any other known measurement for CdTe-based devices, it is among the highest ERE values reported for any photovoltaic technology [26].**

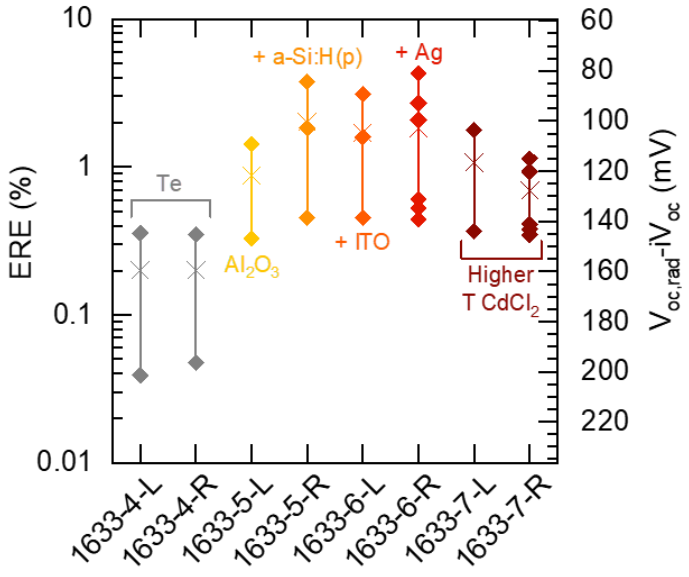


Figure 108. External radiative efficiency for diffused CdSeTe:As devices with varying passivating back contact structures (1633)

7.5.4 Implied Voltage and Voltage Loss Analysis

Together, Table 9 and Figure 109 summarize numerous device structures and their resulting $iV_{OC,}$ calculated from equation 5, as well as a visualization of the various voltage losses. Replacing copper with diffused-arsenic results in several notable effects. First, there is a sizable increase in the iV_{OC} due to the greatly improved radiative efficiency. This is annotated by a green arrow pointing upward in Figure 109. This is somewhat offset by a decrease in $V_{OC,ideal}$ (synonymous with $V_{OC,rad}$ used previously). This is the effect of the increased sub-bandgap features and band tails. Ultimately, replacing copper doping with diffused-arsenic results in an improvement to the implied voltage from approximately 900 mV up to above 940 mV. The addition of Al_2O_3 as a passivating back contact layer further improves the ERE which drives up the implied voltage while also exacerbating the sub-bandgap features and reducing the $V_{OC,rad}$. The subsequent addition of Al_2O_3, a-Si, ITO, and Ag systematically improves the iV_{OC} from approximately 970 to 980 mV. The highest iV_{OC} measured to date for a sample with diffused-

arsenic doping and a passivated back contact has an implied voltage of 982 mV. This result, just shy of the coveted 1 V mark, proves that the absorber structure is capable of producing voltages far greater than those typically seen today. The fact that these massive improvements in iV_{OC} have not been matched by an increase in actual device performance confirms that while Al_2O_3 is an excellent passivating layer, it is not an effective hole selective material. The large difference between the implied and actual voltages shown in orange in Figure 109 illustrates the criticality of finding an appropriate hole selective material.

Table 9. Implied V_{OC} calculations for various device structures

Simplified Sample Structure	$V_{OC, ideal}$ (mV)	ERE (%)	iV_{OC} (mV)
MZO/CST/CdTe/Te	1152.9	0.03	940.7
MZO/CST/CdTe:Cu/Te (baseline)	**1152.3**	**0.01**	**900**
MZO/CST/CdTe:As/Te	1109	0.16	942.9
MZO/CST/CdTe:As/CST/Al_2O_3	1092.4	0.90	971.5
MZO/CST/CdTe:As/CST/Al_2O_3/ a-Si/ITO	1082.9	1.57	976.1
MZO/CST/CdTe:As/CST/Al_2O_3/ a-Si/ITO/Ag	1080.6	2.23	982.9
MZO/CST/CdTe:Cu/CST/Al_2O_3/ a-Si/ITO/Ag	1105.6	0.01	874.8
MZO/CST/Al_2O_3	1092	2.30	1005

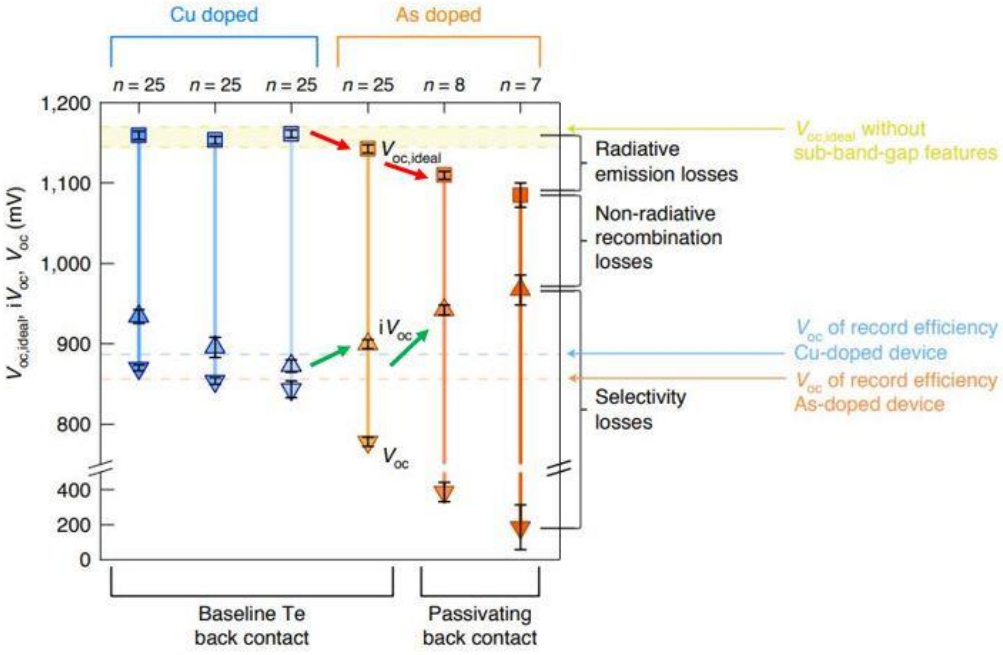


Figure 109. Voltage loss analysis for CdSeTe samples with various dopants and back contacts, adapted from [22].

Figure 110 is a recreation of the ERE vs voltage deficit plot shown earlier in this work. Here, several data points have been added which illustrate the progress made in improving the ERE for CdTe-based devices. It can be seen that these time-stamped data points do not follow the trend line, meaning that despite the improvement in radiative efficiency, the extracted voltage has not improved. This indicates that inclusion of extremely high lifetime CdSeTe, diffused-arsenic doping and a passivating oxide layer have improved the acceptor concentration while also drastically reducing non-radiative recombination. These result in greater quasi-Fermi level separation and an improved implied voltage approaching 1 V. However, this potential voltage gain is lost either in the defective CdSeTe:As layer or at the contact as the quasi-Fermi levels collapse towards one another due to defects and poor selectivity.

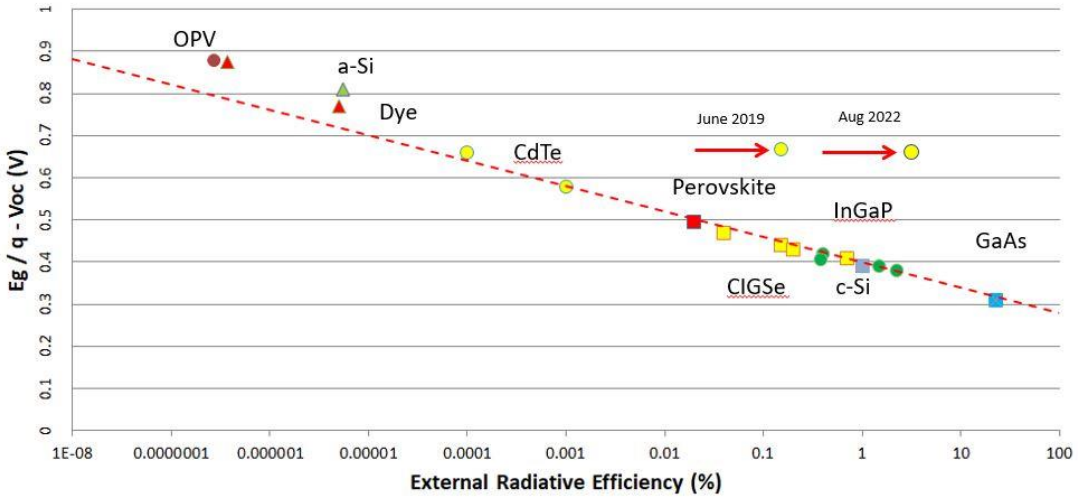


Figure 110. Voltage deficit vs external radiative efficiencies for various photovoltaic technologies with recent CdTe progress, adopted from [27].

7.6 TeO_x Passivation

The carrier lifetime experiment displayed in Figure 100 produced a very surprising result. The control sample, with no Al_2O_3, displayed an excess-carrier lifetime of 6 µs. This was unexpected because the bare CdSeTe/air interface should have had a very high density of dangling bonds and recombination-active defects. During testing, which occurred at three separate universities/national labs, the samples were exposed to atmosphere for approximately two weeks before the TRPL measurements were performed. The fact that this sample exhibited one of the longest lifetimes ever measured meant that some form of unintentional interface passivation must be occurring. XPS was used to inspect the exposed surface of CdSeTe films immediately after fabrication and after prolonged exposure to atmosphere at room temperature. Two weeks was chosen as the exposure duration to mimic the conditions of the natural experiment which occurred with the TRPL samples. The results can be seen in Figure 111 .

Unsurprisingly, the relative intensity of the Te^{4+} peak, which is associated with oxidized tellurium (TeO_x) was greater after exposure to air. The proportion of oxidized tellurium at the surface, as determined by the ratio of peak heights, went from 0.32 to over 0.38 in as-deposited material and from 0.28 to 0.32 in $CdCl_2$-treated material. What was striking was that an increased oxidized tellurium fraction correlated with an increase in ERE, as seen in Figure 112. It appears that when exposed to air for two weeks, CdSeTe forms a thin layer of tellurium oxides which chemically passivate the surface, mitigating the effects of the exposed surface. This has some precedent in photovoltaics, where natively grown silicon dioxide (SiO_2) is commonly used to passivate silicon wafers. This finding suggests the possibility of other oxides being viable candidates for passivating layers for CdTe-based photovoltaics. Natively grown oxides are particularly attractive options, so as to avoid possible surface damage that may accompany a deposited oxide, depending on the deposition method.

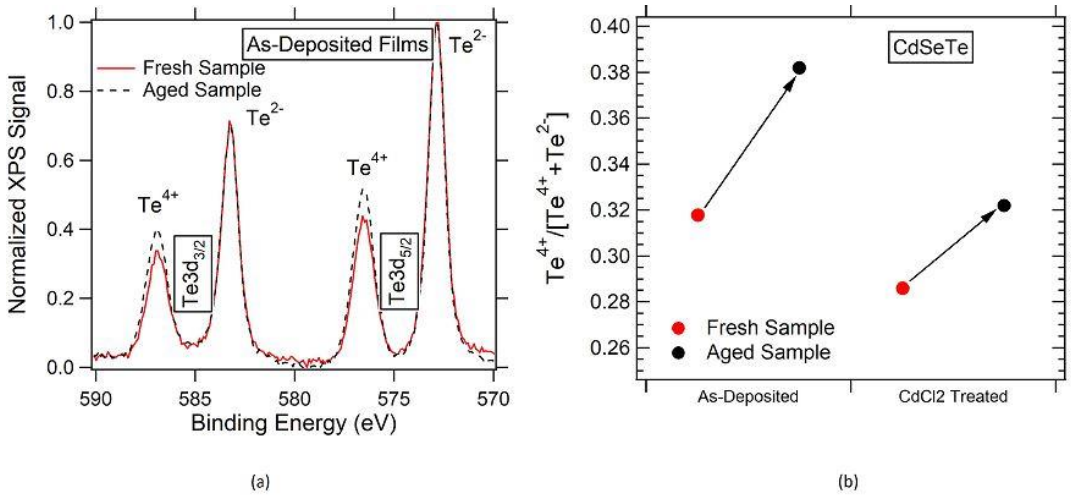


Figure 111. (a) XPS spectra for As-deposited CdSeTe films showing that the relative Te^{4+} peak increases after two weeks exposure to air. (b) Plot showing the increase in oxidized tellurium fraction after aging for both as-deposited and $CdCl_2$-treated CdSeTe

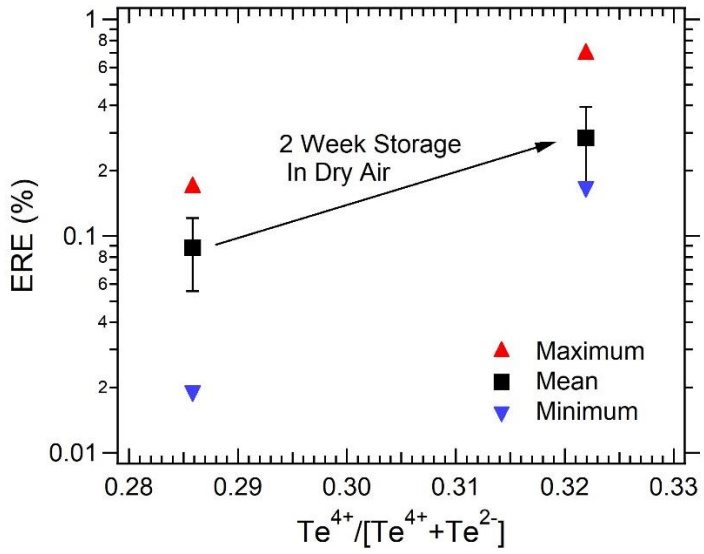


Figure 112. Plot showing the increase in external radiative efficiency as a function of oxidized tellurium fraction

7.7 Conclusions

The inclusion of a thin layer of deposited Al_2O_3 at the back interface of Cd(Se)Te devices has a drastic influence on the interface recombination velocity, TRPL-measured carrier lifetime, and external radiative efficiency. The ERE values which are enabled with alumina passivation indicate that voltages approaching 1 V are possible. Nonetheless, as a wide bandgap oxide, it creates a substantial barrier to both electrons and holes and the layer therefore needs to be kept exceedingly thin to allow for tunneling transport of holes. The increase in series resistance and kinking behavior seen in the JV plots likely is due to this increased barrier to holes. Aluminum oxide alone cannot therefore serve as a hole contact, and requires an additional layer with proper band alignment and possible p-type doping to allow the holes to tunnel through to the proper energy level. The low voltage measured for alumina-passivated samples to day is indicative of poor hole-selectivity. As p^+ α-Si has thus far served as that highly p-doped layer, it seems that

the $CdCl_2$ treatment has changed its properties to sufficiently to prevent it from serving as an effective hole contact in this structure. New material candidates must be explored to fully harness the implied voltage of alumina-passivated Cd(Se)Te.

Including both diffused-arsenic doping and Al_2O_3 passivation further improves the electro-optical properties of Cd(Se)Te devices. The graded-doping profile paired with the passivating oxide both contribute to a drastically lower recombination velocity at the back interface. Additionally, an increased carrier concentration paired with long carrier lifetimes support a greater quasi-Fermi level splitting and high radiative efficiency. **Hypothesis III is overwhelmingly supported by an abundance of evidence from TRPL and ERE measurements.** But these samples are once again limited by selectivity and will not produce their full potential voltage until an appropriate hole contact is found.

Finally, the native growth of tellurium oxide provides an alternative route for interface passivation. It has already been shown to improve the ERE of samples, and with optimization, it may prove to be a viable way of reducing interface recombination and increasing the extracted voltage.

CHAPTER 8. EXTRACTING CURRENT FROM CdSeTe-ONLY DEVICES

Although not the primary focus of this work, one conclusion which can clearly be drawn from the presented evidence is that CdSeTe has a much higher potential performance compared to CdTe or CdSeTe/CdTe bilayer absorbers. The highly luminescent and exceedingly-long lifetime CdSeTe films enable greater quasi-Fermi level splitting and therefore implied voltage than can be supported by a CdTe-containing architecture. Therefore, working towards a CdSeTe-only device structure was performed as a parallel effort to the doping and passivation work presented in the previous chapters. The intention was to incorporate the benefits of highly activated dopants and passivating oxides into absorbers with the greatest potential to maximize the total performance. Therefore, in many of the studies presented in this work, samples were fabricated where one sample contained CdTe or CdTe:As and another had a mirrored structure where the 1-4 μm CdTe was replaced with CdSeTe to maintain the same total thickness.

8.1 Zero Current Device

Recall that the introduction of CdSeTe into previously CdTe-only devices resulting in a large improvement in J_{SC} due to the lower bandgap. The bandgap of CdSeTe varies depending on the selenium composition. From a bandgap of 1.49 eV as CdTe, the bandgap shrinks to a minimum of 1.37 eV at approximately 40% CdSe, then grows with increasing selenium as the bandgap approaches that of pure CdSe at 1.7 eV, described as “band bowing” [134], [135]. Because of this history, CdSeTe has typically been associated with higher currents, up to the maximum of 32 mA/cm^2 under AM1.5 illumination. Surprisingly, these CdSeTe-only devices would often produce zero current. The JV curve of an example zero-current device is provided in Figure 113. Strangely, these devices often displayed a strong diode curve, and show impressive

carrier concentrations, lifetimes, and radiative efficiencies. This indicates that although film is of high quality, something is preventing carrier extraction.

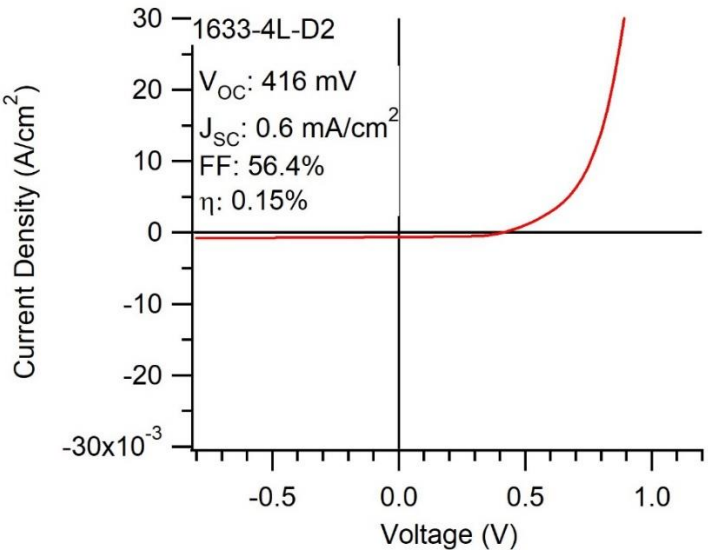


Figure 113. Example of a zero short-circuit current device with a CdSeTe absorber (1633-4L)

Several possible explanations for this phenomenon are here proposed: First, it is possible that the CdSeTe, as deposited, is n-type due to a large number of V_{Te} caused by the high vapor pressure and low sticking coefficient of selenium, rather than the previously supposed p-type. The conductivity of a material to a particular carrier is proportional to the product of the mobility and the carrier concentration [9]. Therefore, an n-type material will inherently have a lower conductivity to holes. N-type CdSeTe is not particularly problematic in the traditional CdSeTe/CdTe device structure. In this structure, the CdSeTe layer is kept thin, typically less than 1 µm, so the holes do not have to travel far before reaching the p-type CdTe. Additionally, the diffusion of selenium between the CdSeTe and CdTe layers likely removes much of the V_{Te}. Finally, even if n-type CdSeTe is located at the front, it would display increased conductivity to

the electrons which are moving toward the front interface. N-type CdSeTe is however highly problematic in a CdSeTe-only structure. If the thickness is kept the same, the holes must now travel through several micrometers of very low conductivity material. In order to produce current, both the electrons and holes must be able to conduct out of the absorber. The very low hole current that would result from this scenario would restrict the total current.

Alternatively, using electron backscatter diffraction, First Solar has noted that prior to $CdCl_2$ treatment, CdSeTe films contained large amounts of large bandgap wurtzite crystalline phase. The higher the selenium concentration in the film, the more wurtzite phase was present. It is only after the $CdCl_2$ treatment blends the CdSeTe into the CdTe and reduces the selenium concentration in the front that the desired zinc blende crystalline phase is predominately found. Even small amounts of wurtzite phase resulted in decreased performance [136]. Therefore, in the CdSeTe-only devices shown in this work, especially those with very thick layers of CdSeTe, large amounts of wurtzite phase likely exist even after the $CdCl_2$ treatment.

The above problems are exacerbated by the fact that the selenium concentration in deposited CdSeTe films is not constant. It is hypothesized that the selenium content changes with processing conditions and with time as the source material is used. Because wurtzite phase preferentially grows at higher selenium concentrations, a changing source charge may result in a different phase structure even when the same processing conditions are used. The changing microstructure may affect how the $CdCl_2$ treatment interacts with the film, making it difficult to optimize the process. Whereas too light a $CdCl_2$ treatment will result in a poorly-passivated bulk, a too aggressive treatment may cause chlorine accumulation at the interfaces which could block current collection. Combined, these potential issues will be explored as a part of Hypothesis IV.

8.2 Hypothesis IV

The intermittent loss of current in arsenic-doped devices is primarily due to three causes. Eliminating the following causes will result in devices with >25mA/cm^2 J_{SC}:

I) A buried junction caused by a layer of n-type CdSeTe.

II) Increasing selenium concentration causing the formation of photo-inactive wurtzite phase.

III) Increasing selenium concentration causing microstructural changes during film growth. These changes affect how $CdCl_2$ interacts with the film. $CdCl_2$ accumulation at the grain boundaries and interfaces confine charge carriers and reduce current.

8.3 Hypothesis IV Results

8.3.1 Determining Carrier Type

Several characterization methods were employed to probe the doped nature of CdSeTe. The hot probe method is a simple method of determining the majority carrier type. Two electrical probes of a multimeter are put in contact with the semiconductor. The positive terminal is heated significantly above the temperature of the negative terminal. The thermal energy of the hot probe causes diffusion of the majority carrier away from the probe, inducing a voltage across the terminals. The sign of the voltage indicates the majority carrier type, a positive voltage indicates an n-type semiconductor while a negative voltage indicates p-type [137].

The Hall Effect measurement relies on the Lorentz force to determine the carrier type in a semiconductor. The Lorentz force describes how when an electron moves perpendicular to a magnetic field, it experiences an additional force that is perpendicular to both the magnetic field and the direction of motion. If an applied magnetic field is directed in the x-direction, and the electrons move in the y-direction, the Lorentz Force exerts a force on the electron in the z-direction. This causes electron drift in the z-direction causing accumulation of charge on one end of the semiconductor. This leads to a potential difference across the different sides of the

semiconductor, the Hall Voltage. Not only can the carrier type be determined by the sign of the voltage, but the magnitude of the voltage can indicate the carrier concentration [138].

Scanning Kelvin Probe Microscopy (SKPM) is a particular variation of atomic force microscopy. In this method, a nanometer-scale tip is used to probe the surface of a semiconductor. An electrostatic force exists between the tip and the sample, which can be negated by a DC voltage applied to the tip. The amount of voltage needed to negate the electrostatic force is used to calculate either the work function or electrical potential depending on the conditions of the measurement. Once again, this can be used to determine the type of carrier within the semiconductor [139].

8.3.1.1 Hall Effect and Hot Probe Measurements

Neither the Hall Effect nor the hot probe measurements gave conclusive results. In the case of Hall measurements, the Hall voltage was below the detection limit which not only made it impossible to determine whether the CdSeTe was n or p-type, but also indicated that regardless of the type, the carrier concentration was likely quite low. This is exacerbated if the material also has a low mobility. Hot probe measurements experienced a similar issue. An extremely low voltage was measured and the sign of the voltage would change between subsequent measurements, which again likely indicates a film which is close to intrinsic.

8.3.1.2 Scanning Kelvin-Probe Microscopy Measurements

Figure 114 shows the results of the SKPM measurements. The top profile shows the topography of the film as determined by normal AFM measurement. The subsequent plots show the potential, potential difference, and ultimately the calculated electric field, respectively. The electric field, being slightly negative and relatively constant through the film depth indicate that

undoped CdSeTe is slightly n-type. It should be noted that when considering hole conductivity, the difference between an intrinsic material and a slightly n-type material is not particularly impactful. Both materials are characterized by a low hole concentration which will be set by excess carriers within the interaction volume during illumination. Particularly if the hole mobility is also low, the semiconductor will have poor hole conductivity.

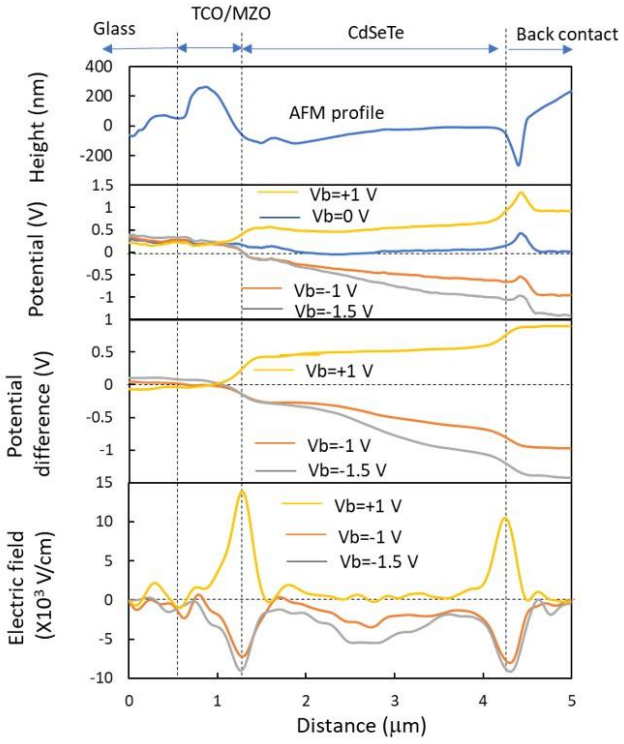


Figure 114. Scanning Kelvin probe microscopy measurement of a CdSeTe-only device (1809-8L) indicating that the CdSeTe is slightly n-type, SKPM measurements performed at NREL.

8.3.2 Wurtzite Phase CdSeTe

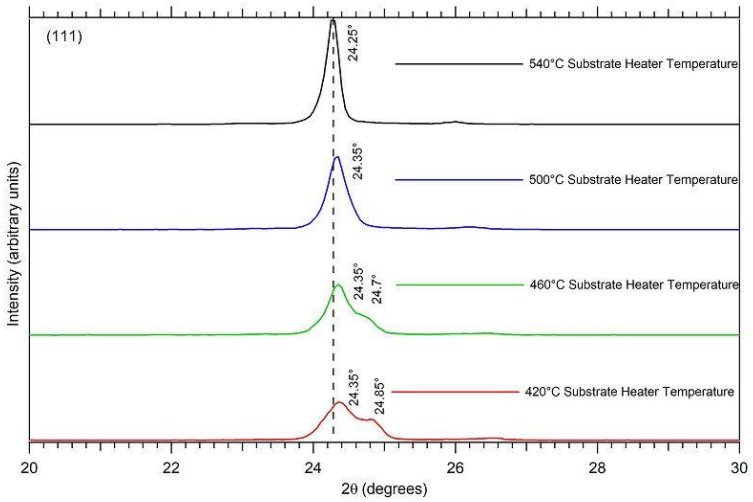
In addition to the low hole conductivity caused by the apparent n-type or intrinsic nature of CdSeTe, the presence of wurtzite phase material may also contribute to current loss. CdSeTe forms cubic crystals until approximately 50% CdSe, at which point the hexagonal-phase wurtzite becomes energetically favorable. As previously mentioned, the bandgap also increases beyond

40% selenium up to a maximum of 1.7 eV for pure CdSe. Even if a film predominantly consists of cubic phase CdSeTe, even small amounts of a high bandgap material interspersed throughout it will likely serve as a barrier to carriers. While both carriers may be affected by this, the hole barrier will be more apparent because e-h generation occurs so much closer to the electron contact in CSU devices.

To study the formation of hexagonal phase CdSeTe, films were deposited where the substrate temperature during deposition was varied. The substrate heater was varied from 420°C, which was the historic temperature used for CSU CdSeTe/CdTe baseline structures up to 540°C. The films were then analyzed using Glancing Angle X-ray Diffraction (GAXRD), the results of which are shown in Figure 115a . In this figure, each fit peak location is annotated above the curve, and a vertical dashed black line is centered on the 540°C peak location to highlight the peak shift between samples.

It is apparent from the XRD spectra that the depositing film forms two sets of peaks at lower substrate temperatures corresponding to the cubic (111) and hexagonal (002) phases, but a single cubic peak at higher substrate temperatures. Using XRD cards of the CdTe-CdSe solid solution the the lattice parameter a_0 for the cubic phase and the lattice parameters a and c for the hexagonal phases were fit.[140]–[143]. Based on these fits and determination of the lattice constants using the cubic (111) and (220) planes and the hexagonal (002) and (110) peaks, composition for the different phases was calculated and compared to the selenium composition as determined by Inductively-Coupled Plasma Mass Spectrometry (ICP-MS). The comparison is shown in Figure 115b. First, it is apparent that the hexagonal phase has a selenium composition between x = 0.5 and x = 0.7, decreasing with the increased substrate heater temperature but always drastically greater than that of the cubic phase material. Additionally, it is clear that the

volume fraction of these hexagonal phases is small, since the ICP-MS data agree with the compositions determined by the cubic phase, approximately x = 0.3 to 0.38. It is likely that the hexagonal phase is the result of poor adatom surface diffusion behavior leading to localized regions of higher selenium concentration during deposition at lower substrate temperatures. As the substrate heater temperature is increased from 420°C to 540°C, the crystallinity markedly improves, as evidenced by the elimination of the hexagonal peak and reduction of the full width of the peak at half of the peak maximum (FWHM) of the main cubic peak. At temperatures of 500°C and greater, only the cubic phase is seen. The increased substrate temperature also resulted in large equiaxed grains and only a small decrease in the deposition rate, indicating that it likely a viable method for removing hexagonal phase material.



(a)

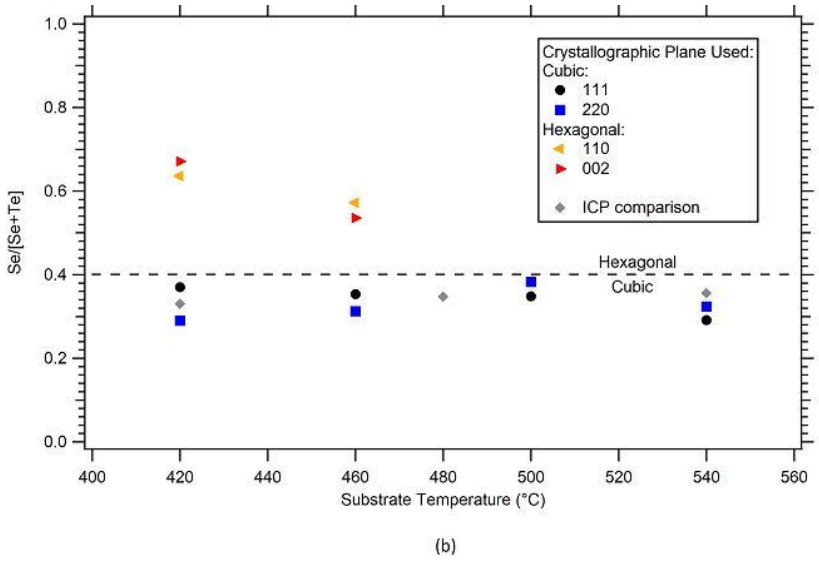


Figure 115. XRD measurements of as-deposited $CdSe_{0.4}Te_{0.6}$ shows the reduction of the hexagonal peak and strengthening cubic peak as substrate temperature increases. The vertical dashed corresponds with the 540°C peak to aid in visualizing the peak shift. (b) A comparison of the selenium composition of the cubic and hexagonal phases within $CdSe_{0.4}Te_{0.6}$, as determined by a fit of the lattice parameters, adapted from [144].

8.3.3 Microstructural Changes and $CdCl_2$ Accumulation

The samples prepared for and presented in this work were fabricated using a CdSeTe source charge that was $CdSe_{0.4}Te_{0.6}$, meaning 40% CdSe mixed with 60% CdTe. This results in a 20 atomic percent selenium mixture. Figure 116 compares two EDS line scans performed on films that were fabricated from CdSeTe source charge that was initially at 20 atomic percent selenium.

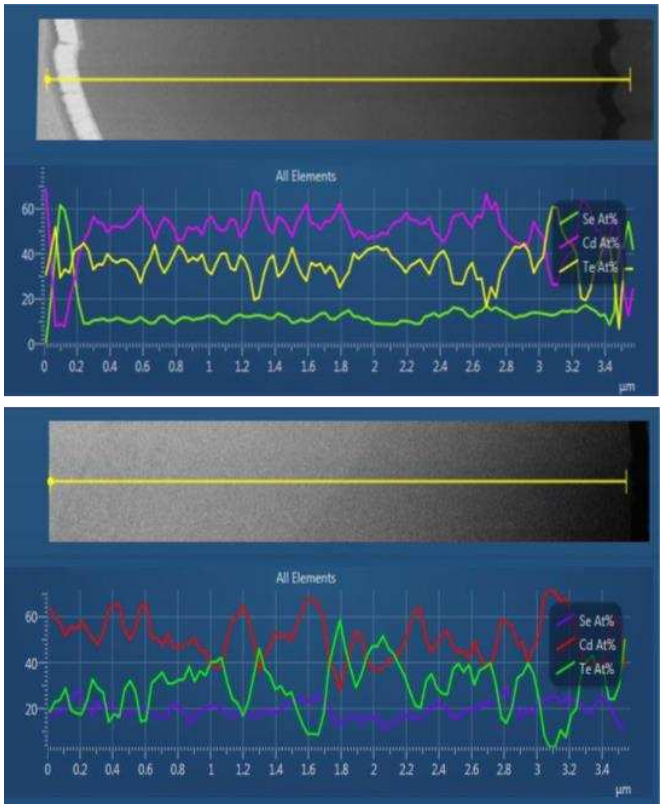


Figure 116. EDS line scans comparing two devices, Sample 1546-7 (Top) and Sample 1633-4 (Bottom) deposited with the same source charge material composition, microscopy images taken by University of Illinois at Chicago

Previous EDS measurements have shown that the selenium concentration in growing films is usually lower than that of the source charge, as not all the sublimated selenium incorporates into the film. Typically for a 20 atomic percent source charge, films show between 10 and 12 at% selenium. This is very similar to the first linescan shown in Figure 116. However, the second line scan shows that the selenium concentration is double the typical value at 20 atomic percent. This finding contributes to the growing body of evidence that the CdSeTe source material changes over time and therefore films fabricated under the same conditions at different times may not necessarily exhibit the same properties [144]. As the source is heated, the constituent materials sublimate at different rates due to their differing partial vapor pressures. Over time, it is

hypothesized that the CdTe disproportionately leaves the source material, leaving it selenium rich. This encourages the growth of wurtzite phase crystals, and drastically affects the deposition rate, as can be seen in Figure 117. In this figure, the number of days which have elapsed is used as a reasonable proxy for total time of use as the average daily time of use is relatively consistent. The thick vertical lines represent when the sublimation source material was replaced. The deposition rate peaks with fresh material, and gradually declines with use. CdSeTe appears to eventually reach a critical threshold of use where the deposition rate drops precipitously, reaching a low of less than 40% of the original rate. Alternatively, if the material is replaced with reasonable frequency, the deposition rate can maintained at approximately 70% or more of the maximum. It is likely that the drop in deposition rate corresponds with preferential sublimation of CdTe and a progressively Se-rich source material. Therefore, the same processing conditions, performed using the same nominal materials, can result in drastically different devices.

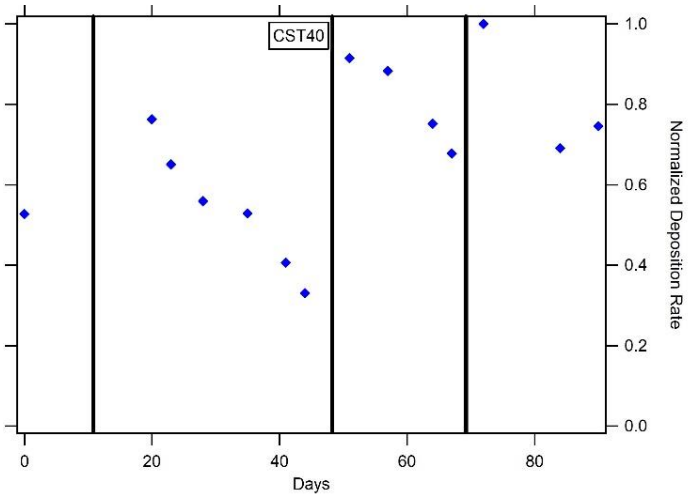


Figure 117. The normalized deposition rate of CdSeTe over several months showing a drastic decrease as the source material is used. The vertical black lines represent when the source material was replaced with fresh material. Adapted from [144]

In addition to, and possibly because of the changes in selenium concentration, it has been noted that the film microstructure can vary greatly, even when the same materials and processing conditions are used. Figure 118 and Figure 119 are TEM images showing the grain structure of the same films for which the earlier EDS data was shown. The first TEM image shows a dense film with large grains. Contrastingly, the second image, which was intended to be a repeat of the first's structure, shows multiple voids and stacking faults. The thicknesses of these films were also considerably different, despite the same deposition time.

These structural differences may be the result of the changing source stoichiometry or the changing deposition rate as the material ages. Additionally, the arsenic diffusion pathways and rate will likely be affected by the microstructure, therefore a consistent microstructure will not only aid in recovering the current but is also a crucial step towards developing a method for dependable and predictable doping profiles.

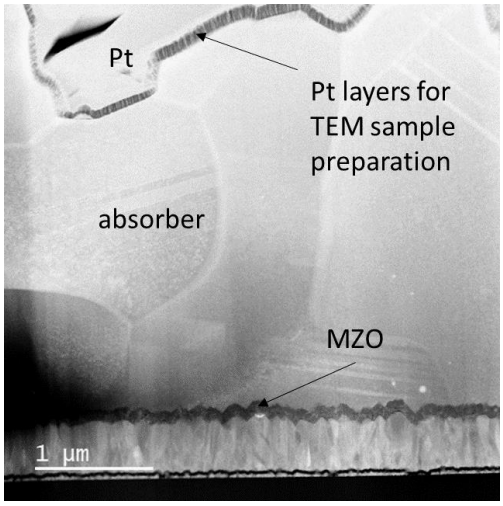


Figure 118. TEM image showing large grained microstructure in an arsenic-doped device, Sample 1546-7, microscopy images taken by University of Illinois at Chicago

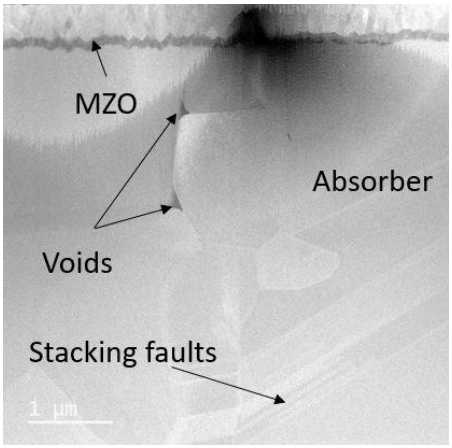


Figure 119. TEM image showing an arsenic-doped film from sample 1633-4 with voids and stacking faults, microscopy images taken by University of Illinois at Chicago

Finally, as the film density and prevalence of voids change within the film, the interaction between the $CdCl_2$ and the film changes too. $CdCl_2$ treatment is a necessary step in the fabrication of CdTe based devices, passivating defects and facilitating grain growth. But too much $CdCl_2$ can harm the device, particularly if large amounts of $CdCl_2$ reside at the interfaces. $CdCl_2$ is a high bandgap material and may block charge transport. Just such a device is shown in Figure 120, where the "light element grains" are $CdCl_2$ accumulation at the front interface.

If the $CdCl_2$ encounters a less dense film, it is likely to migrate towards the front interface more quickly. Similar to the previous discussions, the result is that the same $CdCl_2$ treatment may be optimal for one film, but the same treatment may drive too much $CdCl_2$ to the front interface in another. Therefore, the $CdCl_2$ optimization cannot be performed independently, the robust control of film quality is a prerequisite.

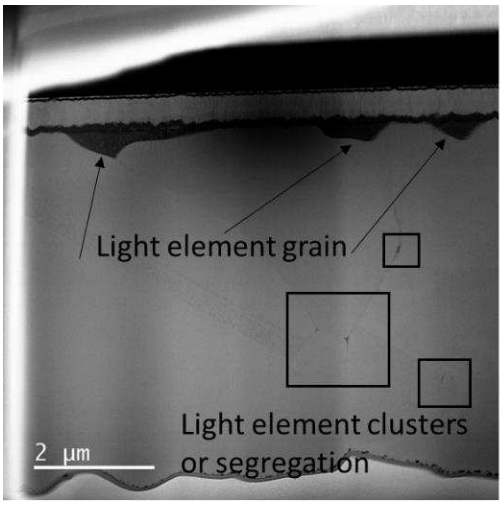


Figure 120. TEM image showing the segregation of chlorine in voids and at the interface in sample 1633-4, microscopy images taken by University of Illinois at Chicago

8.4 Recovering Current in CdSeTe-only devices

Now with a better understanding of the potential causes for current losses, specific device structures could be designed to combat the loss. At present, numerous CdSeTe-only devices have been fabricated, each employing a unique set of strategies, and all producing a current density of at least 25 mA/cm^2.

Figure 121 shows the JV plot for a CdSeTe-only device with a conversion efficiency of 7.8% and J_{SC} of 25 mA/cm^2. This result was obtained by thinning the total CdSeTe layer down to 1 µm and then adding sputtered ZnTe:Cu as a hole contact. Accounting for low hole conductivity, the thin absorber ensures that e-h generation occurs close to the hole contact. The thin absorber has the added benefit of maximizing the excess carrier concentration and thus qFLS (assuming the interfaces are well passivated.) The CdSeTe was deposited at an elevated substrate heater temperature of 480°C to ensure a dense film consisting of large equiaxed grains and no wurtzite phase. The ZnTe:Cu is an experimental hole contact that will be discussed in the

'Future Work' section of Chapter 9. It is a hopeful candidate as a hole contact due to its band alignment and purported ability to be highly p-doped, but has not yet been optimized. The low V_{OC} seen in this device is believed to be due to the poor interface passivation between the CdSeTe and the ZnTe:Cu. Despite this, the copper-doping may also assist in increasing the hole conductivity in the ZnTe and into the CdSeTe.

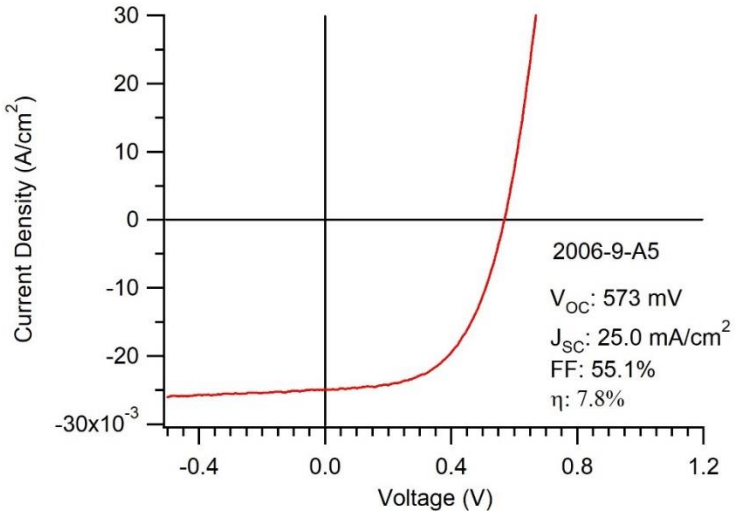


Figure 121. JV plot of a CdSeTe/ZnTe device exhibiting 25 mA/cm^2 current density, device fabricated by Pascal Jundt

In another experiment (samples 1999-1,3), 2.5 µm thick CdSeTe films were fabricated. Some samples received a CuCl-doping treatment while others did not. Additionally, some samples were etched in a solution consisting of 20 g of citric acid dissolved in 100 mL of hydrogen peroxide to see if removing a portion of the absorber thickness affected current collection. Table 10 below summarizes the J_{SC} results. The sample without a copper treatment or etch exhibited low current density at just 7 mA/cm^2. Adding an acid etch reduced the current marginally, likely due to etch damage from the acid, particularly at the grain boundaries. Similarly, for Cu-doped samples, the etch-only results in a marginally higher J_{SC}, going from 26

to 28mA/cm^2. This indicates that while the etch and subsequent thinning of the total absorber may have a marginal effect on current collection, it is predominately driven by the presence or absence of copper doping, and therefore the hole conductivity is likely a more impactful factor.

Table 10. Current collection for CdSeTe samples with Cu-doping and an acid etch, experiment performed by Tushar Shimpi

Acid Etch	CuCl Treatment	J_{SC} (mA/cm^2)
No	No	7
No	Yes	26
Yes	No	5
Yes	Yes	28

The final experiment fabricated a CdSeTe film, reported at 820 nm thick and deposited at 420°C substrate heater temperature. After film deposition, the sample received a CuCl treatment and an 1800-second anneal over a Cd_3As_2 source maintained at 360°C while the substrate heater was set to 500°C. Figure 122 shows the JV plot for this device compared to an identical sample which did not receive the Cd_3As_2 anneal. This plot reveals that while the non-annealed sample had a J_{SC} of approximately 12 mA/cm^2, the Cd_3As_2-annealed sample demonstrated a J_{SC} greater than 28 mA/cm^2. Previous experiments with Cd_3As_2, which are beyond the scope of this work, have shown that Cd_3As_2 may hold some promise as an alternative method for arsenic doping CdTe-based materials. Thus far, Cd_3As_2 has not been able to produce samples with the high dopant activation or radiative efficiency of the diffused-arsenic method. There has however, been some conflicting evidence that suggests that it may improve the acceptor concentration within the absorber. Regardless, the effect of the Cd_3As_2 anneal on the current collection in CdSeTe-only devices was substantial.

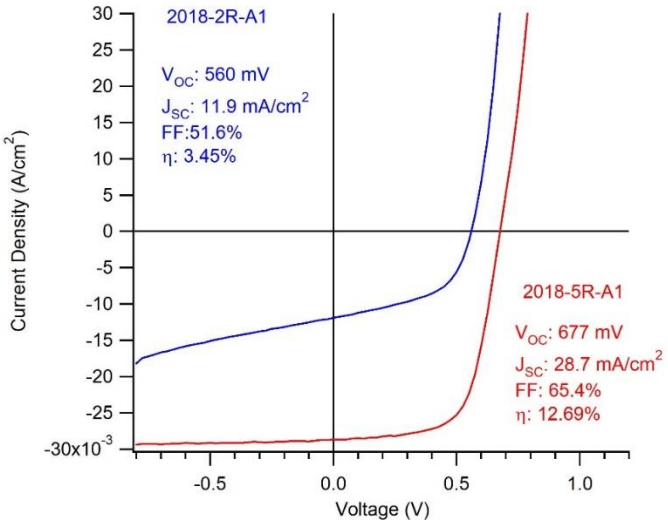


Figure 122. JV plots of CdSeTe-only devices showing the effects of a 1800s Cd_3As_2 anneal (Red) compared to no anneal (Blue). Samples fabricated and tested by Zach Lustig.

8.5 Conclusions

Although the multiple methods for testing the carrier type in CdSeTe have different sensitivities and detection thresholds, they consistently and conclusively report very low acceptor concentrations. It is not certain if this is due to an absorber which is nearly intrinsic or lightly n-type doped, but at these levels, the difference is largely semantic rather than practical. The constant result is that the very low hole concentrations found in these films contribute to low hole conductivity, particularly if the hole mobility is also low, which may be impacted by the presence of wurtzite crystallites in the film.

In addition to the general low hole conductivity throughout the film, the presence of high bandgap wurtzite material may also create localized, sudden, and large energetic barriers which impede or even confine carriers. XRD measurements conclusively show that wurtzite is present in CdSeTe when deposited using the conditions which have historically been used. Based on this evidence, the standard substrate temperatures used for CdSeTe deposition by numerous

researchers have been increased to a minimum of 480°C to prevent hexagonal phase formation. Of the potential issues impeding current collection, this was the most easily remedied, as the increased substrate temperature had only a small impact of the deposition time and resulted in a higher quality film.

The densification of the film that accompanied the increase in substrate temperature has reduced the prevalence of voids which has likely reduced $CdCl_2$ accumulation. Nonetheless, there exists widespread evidence that the CdSeTe source charge changes over time as it is used. The compositions of devices made from this source charge, therefore, are not constant either. These changes do result in differing structures, making it difficult to optimize $CdCl_2$ passivation without overdoing it until they can be made consistently the same.

Bearing in mind these potential sources of current loss, three separate strategies which have successfully recovered a current of at least 25mA/cm2 have been presented. The fact that each was able to recover current while being designed to mitigate one or more differing obstacles indicates that multiple issues contribute to current loss as opposed to a sole cause. There is however, one striking similitude between each of the three strategies to recover current: They each address the problem of low hole conductivity, albeit in different ways. Sample 2006-9 recovered current by thinning the total absorber thickness and by incorporating an increased substrate temperature to eliminate hexagonal phase material. Samples from experimental run 1999 also thinned the absorber thickness via etching, but recovered most of the current by using CuCl to dope the CdSeTe. Finally, sample 2018-5R thinned the absorber and utilized both copper and Cd_3As_2 to dope the film p-type. **At this time, there is sufficient evidence to support Hypothesis IV, and careful control over the device structure recovers full short-circuit current values. Additionally, of all the potential sources of current loss, the low hole**

conductivity, predominately driven by the low hole density in n-type CdSeTe is the primary factor limiting current collection from CdSeTe-only devices.

CHAPTER 9. CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

The work presented in this dissertation has been focused on utilizing arsenic doping and passivating oxides to reduce the voltage deficit in CdTe-based solar cells. Throughout this work, I have endeavored to show that copper, although historically used to dope CdTe, is a major limitation to future development. As a deep acceptor with low activation and self-compensation as well as a tendency to migrate, copper results in devices with low excess-carrier lifetimes, low luminescence, and consequently smaller implied voltages.

By contrast, arsenic doping has been shown to a viable method for drastically improving the electro-optical properties of the absorber. Arsenic has resulting in films with higher measured carrier concentrations, longer lifetimes, lower interface recombination rates, higher radiative efficiencies, better implied voltages…often simultaneously and in the same sample. However, the arsenic doping method substantially alters the efficacy of the process. Fabricating films directly from an arsenic-containing source material without additional processing results in only moderate arsenic incorporation. This method has been shown to be able to incorporate up to 10^{18} cm^{-3} arsenic in CdTe and up to 10^{19} cm^{-3} in CdSeTe. Furthermore, the incorporation rate is insensitive to the cadmium overpressure that is present during deposition. The arsenic that does incorporate into the film does so as dimers, tetramers, and clusters as opposed to the desired monoatomic arsenic. The doping activation rate is therefore low and the devices exhibit low acceptor concentrations at or below 10^{14} cm^{-3} and lifetimes on the order of nanoseconds. In order to obtain the superior properties necessary for improved performance, further processing of the arsenic containing films is needed.

These superior properties are obtained through the diffused-arsenic method. In this method, the arsenic-containing layer is deposited behind a layer of undoped CdSeTe. An aggressive $CdCl_2$ treatment, performed at an elevated temperature, encourages diffusion of arsenic from the initial layer into the previously-undoped CdSeTe. Kinetic simulations suggest that the only species of arsenic which is capable of diffusing any appreciable distance is interstitial arsenic, which quickly moves through a series of reactions culminating in As_{Te}, a shallow p-type dopant in Cd(Se)Te, resulting in activation rates of at least 26% and a graded doping profile. Using this method, microsecond lifetime and carrier concentrations greater than 10^{16} cm^{-3} have been measured using CV. Resultantly, the implied voltages of diffused-arsenic samples are approximately 40 mV greater than have ever been measured for a copper-doped device.

Aluminum oxide has previously been shown to be effective at passivating silicon TOPCon solar cells, as well as CdSeTe in double heterostructures. In this work, Al_2O_3 was incorporated into function devices by adding a thin layer, typically 2 nm, at the back interface to provide interface passivation. Due to its large bandgap, Al_2O_3 has large offsets in both the conduction and valence bands when paired with Cd(Se)Te and therefore creates a large energetic barrier to both electrons and holes. While it is desirable that the electrons be repelled, this necessitates additional layers to ensure that holes can traverse this barrier and be extracted. To that end, p-type amorphous silicon, ITO, and a silver electrode were deposited behind the Al_2O_3 to induce upward band bending and encourage tunneling transport of holes through the Al_2O_3. When alumina was deposited behind CdSeTe, it resulted in a TRPL-measured lifetime of 8 µs, the longest lifetimes ever measured for polycrystalline CdTe-based materials. These lifetimes, along with improved interface recombination, again resulted in improved radiative efficiencies.

Combining the diffused-arsenic method with aluminum oxide passivation further reduced the interface recombination velocity, contributing to ERE values as high as 4% and implied open-circuit voltages approaching 1 V.

Despite these substantial improvements, the devices presented in this work did not demonstrate an improved open-circuit voltage. Both of these structures exhibit extremely poor carrier selectivity at the hole contact. While the absorber is capable of producing a substantial internal voltage, that voltage is lost across the contacts due to the poor alignment of the hole contact conduction band and an inadequate ratio of hole/electron conductivities. Therefore the search from an appropriate hole contact for Cd(Se)Te should be considered a critical step in the future development of this technology.

CdSeTe has shown greater potential than CdTe as a material capable of producing the internal voltages necessary to exceed current voltage records. The benefits of diffused-arsenic doping and aluminum oxide passivation are maximized when paired with CdSeTe. Therefore, it is likely that future devices will consist of an entirely CdSeTe absorber layer. To aid in this endeavor, the cause of CdSeTe-only devices which produced no current needed to be studied and addressed. While several contributing factors were identified, the low hole conductivity, due to low hole density in intrinsic or slightly n-type CdSeTe appears to be limiting current collection.

Employing these methods, this contribution has shown that CdSeTe-only absorbers with well passivated interfaces and carrier selective contacts have the potential to produce devices with a photovoltaic conversion efficiency of at least 25%. Table 11 below summarizes the key findings presented in this work. These advancements will place CdTe in good stead when competing in global energy markets as a cheap, reliable, and highly efficient photovoltaic

technology. More importantly, highly optimized photovoltaics offer humanity additional tools to combat climate change while providing clean and renewable energy.

Table 11. Summary of Key Findings

ARSENIC DOPING	ALUMINA PASSIVATION
Arsenic incorporation of 10^{18} cm^{-3} in CdTe	Increased photoluminescence
Arsenic incorporation of 10^{19} cm^{-3} in CdSeTe	**Carrier lifetime of up to 8 µs observed**
Arsenic clusters observed in source material	Al_2O_3 creates a large barrier to hole extraction
Poor dopant activation and lifetimes in as-deposited films	**Combining As-doping and Al_2O_3 results in ERE of up to 4%**
DIFFUSED-ARSENIC DOPING	**IMPLIED VOLTAGE**
Diffusion of As_i necessary for high dopant activation	CdSeTe/CdTe bilayer reduces ERE/iV_{OC}
Doping density of 10^{15}–10^{16} cm^{-3} achieved	Copper doping drastically reduces ERE/iV_{OC}
Doping Activation > 25%	**iV_{OC} = 1 V achieved**
Graded doping profile	**Implied efficiency = 25%**
Reduced interface recombination velocity	**RECOVERING CURRENT IN CdSeTe**
Carrier lifetime > 1 µs	n-type CdSeTe, Wurtzite phase crystals & $CdCl_2$ accumulation observed
ERE > 2 %	**28 mA/cm^2 may be recovered**
High doping/long lifetime/high ERE in the same devices	Thinner absorber, improved CdSeTe crystallinity, and p-type doping improve hole conductivity

9.2 Future Work

Despite the progress demonstrated in this work, a significant effort remains before the full implied voltage shown here can be extracted as an external voltage. Four main efforts have been identified and are briefly described below.

9.2.1 Optimizing CdSeTe-only devices

As previously discussed, the high lifetime of CdSeTe makes it a much more promising material for use in high efficiency solar cells compared to CdTe. Chapter 8 discussed several of the difficulties that were encountered when transitioning from a CdSeTe/CdTe bilayer absorber to CdSeTe-only, but there are other issues which still need to be addressed. First, the most widespread commercial method for depositing CdSeTe today is to deposit a thin layer of CdSe

followed by CdTe and using the $CdCl_2$ process to create CdSeTe. This is an excellent method for creating an absorber with a graded bandgap due to selenium diffusion. This method, however, may not be appropriate for creating an absorber where the full thickness has a consistent selenium content. Additionally, it was alluded to in Chapter 9, but CdSeTe film growth and the resulting grain structure has been found to be highly sensitive to certain deposition conditions, particularly the substrate temperature during fabrication. Figure 123 reveals the radical change in CdSeTe grain structure as the substrate heater temperature is increased from 420°C to 540°C, as seen using SEM imaging. The grain boundaries in CdTe have been previously identified as recombination-active areas [145], and minimizing grain boundaries by increasing grain size corresponded with an increase in device performance [146]. It remains to be seen whether there is a similar benefit to increasing the CdSeTe grain size, particularly given the highly passivating nature of selenium in CdTe. Particularly if the total absorber thickness is thinned down to between one and two micrometers, grains which run the full depth between the two contacts should be possible. The cross-sectional SEM image shown in Figure 124 gives an example of a CdSeTe film where dense, multi-micrometer-sized grains have been obtained, although they are not full depth in the shown sample.

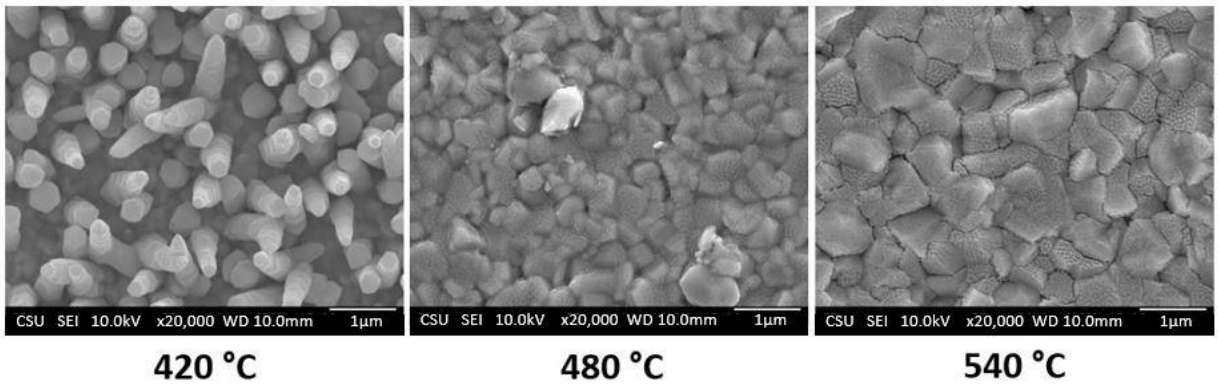


Figure 123. SEM images of as-deposited CdSeTe, showing extreme columnar growth occurring at lower substrate temperatures and larger, equiaxed grains at higher temperatures

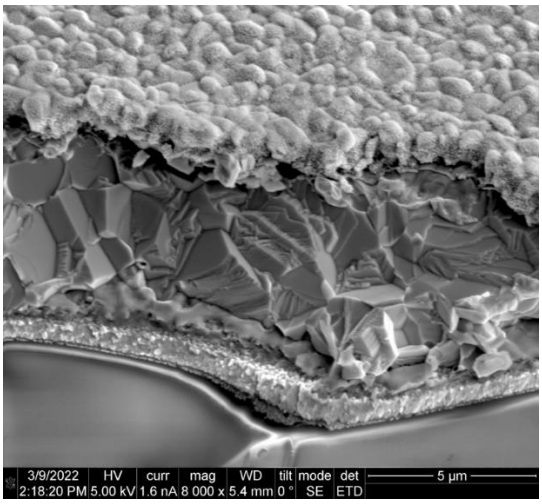


Figure 124. Cross-sectional SEM image showing large dense grains of CdSeTe and a top layer of Al_2O_3. Image taken at Arizona State University

9.2.2 Explore undoped CdSeTe devices to maximize implied voltage

It is clear that the diffused-arsenic-doping method results in carrier lifetimes which are orders of magnitude greater than what has been achieved using copper doping. Nonetheless, there is still a small decrease in TRPL-measured lifetime for arsenic-doped samples compared to undoped CdSeTe. This is to be expected, as anything less than 100% dopant activation means that there is some arsenic within the absorber which is simply acting like a defect, likely creating a site for non-radiative recombination. In fact, even with perfect activation, as the concentration of electrons and holes increase, the radiative-limited lifetime will decrease due to the nature of recombination being dependent upon electrons and holes finding one another [7]. For this reason, an undoped absorber may be capable of supporting greater-quasi Fermi level separation than its doped counterpart. This is the basis of the p-i-n solar cell structure. An undoped CdSeTe absorber, with sufficiently long lifetime would ensure that each charge carrier was capable of reaching its respective contact. Carrier selectivity could then be derived from the band alignment

of the two contacts, without having to modify the absorber layer, which could improve the overall absorber quality and simplify the manufacturing process.

9.2.3 Utilize Arsenic doping to improve hole conductivity

As Chapter 8 illustrated, there may be issues springing from using an entirely undoped, nearly intrinsic layer of CdSeTe as the absorber. A low hole concentration was determined to be a key factor contributing to CdSeTe-only devices which produced zero current. As carrier conductivity is the product of the carrier mobility and carrier density, poorly doped films will naturally exhibit lower conductivity. Worse, if the material naturally has a low carrier mobility, as is suspected of CdSeTe for holes, then these factors combine to create a conductivity that is prohibitively low for charge transport through the absorber and into an external circuit. Therefore, it may be that an entirely undoped CdSeTe absorber is not feasible. If this is the case, arsenic doping may yet be necessary. In this case, the arsenic doping may not be used to achieve a bulk doping level in excess of 10^{16} cm^{-3} as shown in this work, but rather just the minimum doping required to achieve proper levels of hole conductivity while maintaining very high levels of arsenic activation. Possibly the diffused-arsenic method could be used, if an effective method of removing the "reservoir" material is found, or alternatively a new material which can easily be applied to and removed from the back surface of the CdSeTe, similar to how aluminum paste is utilized in Back-Surface Field (BSF) silicon solar cells or spin-on dopants. SCM measurements will be a valuable tool when measuring carrier concentrations, particularly towards the back of devices, where CV measurements cannot probe.

9.2.4 Find an effective hole contact for Cd(Se)Te

The final proposal for future work is hardly a new one. For several decades researchers have struggled with finding an appropriate hole contact. Cd(Se)Te's large work function makes it

difficult to find a partner material which has an appropriately large valence band energy and a large conduction band offset with Cd(Se)Te. Nevertheless, this is perhaps the most critical task needed to enable next generation CdTe-based solar technology. This work has shown that multiple CdSeTe architectures, each utilizing a different combination of diffused-arsenic, aluminum oxide passivation, and large-grained, dense CdSeTe absorbers have already produced implied voltages ranging from 970–1000 mV. This signifies that selectivity losses caused by imperfect contacts is preventing this technology from producing 1 V cells today. Copper-doped samples exhibit low selectivity losses, which indicates that the MgZnO electron contact is not the source of most of the selectivity losses in the current structure. Therefore, improvements to the hole contact are almost certain to produce large gains in external voltage. Possible candidate materials include both intrinsic ZnTe and ZnTe:Cu, platinum, TiO_x, MgO and MXenes, as well as a number of organic-based hole transport layers such as Poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA.) Finally, it may be possible to incorporate perovskite layers which have shown excellent hole selectivity in other technologies, although the sensitive nature of these materials may make it difficult to incorporate into existing processes. Regardless of which material ultimately proves to be the best, a well-passivated back interface between CdSeTe and an optimized hole-selective contact with proper band alignment will minimize voltage loss across the contact, maximize the external voltage, and push the device performance beyond what has thus far been possible.

TABLE OF SAMPLES

Sample Number	Electron Contact	Absorber 1	Absorber 2	Absorber 3	$CdCl_2$ Treatment	CuCl Treatment	Hole Contact Layer 1	Hole Contact Layer 2	Hole Contact Layer 3	Back Electrode	Source Material Arsenic
1379-7	MgZnO	CdSeTe (40%)	CdTe:As	N/A	600 s	N/A	Te	N/A	N/A	C/Ni Paint	Unknown
	100 nm	500nm	3 µm	N/A	425/450°C	N/A	30 nm	N/A	N/A	N/A	N/A
1407-7	MgZnO	CdSeTe (40%)	CdTe	N/A	600 s	120/140/560 s	Al_2O_3	α-Si	N/A	C/Ni Paint	N/A
	100 nm	1 µm	3 µm	N/A	420/450°C	330/190/200	2 nm	6 nm	N/A	N/A	N/A
1546-7	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Te	N/A	N/A	C/Ni Paint	1E+20
	100 nm	2.5 µm	1 µm	500 nm	430/480°C	N/A	30 nm	N/A	N/A	N/A	N/A
1601-4L	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	N/A	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	700 nm	3 µm	N/A	420/450/400°C	N/A	30 nm	N/A	N/A	N/A	N/A
1601-4R	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	120/280/560 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	700 nm	3 µm	N/A	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
1601-5L	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	120/280/560 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	700 nm	3 µm	N/A	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
1601-5R	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	120/280/560 s	Al_2O_3	N/A	N/A	C/Ni Paint	N/A
	100 nm	700 nm	3 µm	N/A	420/450/400°C	330/190/200	2 nm	N/A	N/A	N/A	N/A
1601-6L	MgZnO	CdSeTe (40%)	CdTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	N/A	N/A	C/Ni Paint	Unknown
	100 nm	4 µm	1.2 µm	500 nm	430/480°C	N/A	2 nm	N/A	N/A	N/A	N/A
1601-6R	MgZnO	CdSeTe (40%)	CdTe:As	CdSeTe (40%)	900 s	N/A	Te	N/A	N/A	C/Ni Paint	Unknown
	100 nm	4 µm	1.2 µm	500 nm	430/480°C	N/A	30 nm	N/A	N/A	N/A	N/A
1601-7	MgZnO	CdSeTe (40%)	CdTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	C/Ni Paint	Unknown
	100 nm	4 µm	1.2 µm	500 nm	430/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1601-8	MgZnO	CdSeTe (40%)	CdTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	Ag	Unknown
	100 nm	4 µm	1.2 µm	500 nm	430/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1601-10	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	120/280/560 s	Al_2O_3	α-Si	ITO	Ag	N/A
	100 nm	700 nm	3 µm	N/A	420/450/400°C	330/190/200	2 nm	8 nm	70 nm	N/A	N/A
1633-4L	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Te	N/A	N/A	C/Ni Paint	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	430/480°C	N/A	30 nm	N/A	N/A	N/A	N/A
1633-4R	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Te	N/A	N/A	C/Ni Paint	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	430/480°C	N/A	30 nm	N/A	N/A	N/A	N/A
1633-5L	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	N/A	N/A	C/Ni Paint	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	430/480°C	N/A	2 nm	N/A	N/A	N/A	N/A
1633-5R	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	N/A	C/Ni Paint	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	430/480°C	N/A	2 nm	8 nm	N/A	N/A	N/A
1633-6L	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	C/Ni Paint	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	430/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A

Sample Number	Electron Contact	Absorber 1	Absorber 2	Absorber 3	$CdCl_2$ Treatment	CuCl Treatment	Hole Contact Layer 1	Hole Contact Layer 2	Hole Contact Layer 3	Back Electrode	Source Material Arsenic
1633-6R	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	430/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1633-7L	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	440/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1633-7R	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	1.2 µm	1.2 µm	440/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1634-7	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	120/280/480 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	750 nm	3 µm	N/A	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
1698-3L	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	1 µm	500 nm	430/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1698-3R	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900/600 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	1 µm	500 nm	430/480/400°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1698-7L	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	200 nm	500 nm	430/480°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1698-7R	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	600 s	N/A	Al_2O_3	α-Si	ITO	Ag	1E+20
	100 nm	4 µm	200 nm	500 nm	420/450°C	N/A	2 nm	8 nm	70 nm	N/A	N/A
1732-6L	MgZnO	CdSeTe (40%)	CdTe	CdSeTe (40%)	600/600 s	120/480/580 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	500 nm	3 µm	200 nm	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
1732-8L	MgZnO	CdSeTe:As	CdTe	CdSeTe:As	600/600 s	N/A	Te	N/A	N/A	C/Ni Paint	1E+20
	100 nm	500 nm	2.6 µm	200 nm	430/480/400°C	N/A	30 nm	N/A	N/A	N/A	N/A
1732-8R	MgZnO	CdSeTe:As	CdTe	CdSeTe:As	600/1200 s	N/A	Te	N/A	N/A	C/Ni Paint	1E+20
	100 nm	500 nm	2.6 µm	200 nm	430/480/400°C	N/A	30 nm	N/A	N/A	N/A	N/A
1809-8L	MgZnO	CdSeTe (40%)	N/A	N/A	600/1200 s	N/A	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	3 µm	N/A	N/A	420/450/400°C	N/A	30 nm	N/A	N/A	N/A	N/A
1811-3	MgZnO	CdTe:As	Cd OP-190°C	N/A	600/1200 s	N/A	N/A	N/A	N/A	N/A	1E+20
	100 nm	2 µm	N/A	N/A	420/450/400°C	N/A	N/A	N/A	N/A	N/A	N/A
1811-4	MgZnO	CdTe:As	Cd OP-211°C	N/A	600/1200 s	N/A	N/A	N/A	N/A	N/A	1E+20
	100 nm	2 µm	N/A	N/A	420/450/400°C	N/A	N/A	N/A	N/A	N/A	N/A
1811-5	MgZnO	CdTe:As	Cd OP-230°C	N/A	600/1200 s	N/A	N/A	N/A	N/A	N/A	1E+20
	100 nm	2 µm	N/A	N/A	420/450/400°C	N/A	N/A	N/A	N/A	N/A	N/A
1862-4	MgZnO	CdSeTe:As	N/A	N/A	600/1200 s	N/A	N/A	N/A	N/A	N/A	5E+17
	100 nm	2 µm	N/A	N/A	420/450/400°C	N/A	N/A	N/A	N/A	N/A	N/A
1886-3	MgZnO	CdSeTe:As	N/A	N/A	600/1200 s	N/A	N/A	N/A	N/A	C/Ni Paint	5E+17
	100 nm	2 µm	N/A	N/A	420/450/400°C	N/A	N/A	N/A	N/A	N/A	N/A
1894-7	MgZnO	CdSeTe (40%)	CdTe	N/A	600/1200 s	120/280/560 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	500 nm	3 µm	N/A	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A

Sample Number	Electron Contact	Absorber 1	Absorber 2	Absorber 3	$CdCl_2$ Treatment	CuCl Treatment	Hole Contact Layer 1	Hole Contact Layer 2	Hole Contact Layer 3	Back Electrode	Source Material Arsenic
1894-8	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	(2 $CdCl_2$s) 600/1200/900 s	N/A	Te	N/A	N/A	C/Ni Paint	5E+17
	100 nm	2.5 µm	1 µm	500 nm	420/450/400/430/480°C	N/A	30 nm	N/A	N/A	N/A	N/A
1968-2	MgZnO	CdSeTe (40%)	CdSeTe:As	CdSeTe (40%)	900 s	N/A	Te	N/A	N/A	C/Ni Paint	5E+17*
	100 nm	2.5 µm	1 µm	500 nm	430/480°C	N/A	30 nm	N/A	N/A	N/A	N/A
1999-1	MgZnO	CdSeTe (40%)	N/A	N/A	600/300 s	120/280/560 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	2.5 µm	N/A	N/A	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
1999-3	MgZnO	CdSeTe (40%)	N/A	N/A	600/300 s	120/280/560 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	2.5 µm (acid etch)	N/A	N/A	420/450/400°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
2006-9	MgZnO	CdSeTe (40%)	N/A	N/A	600/300 s	N/A	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	1 µm	N/A	N/A	420/450/400°C	N/A	40 nm	N/A	N/A	N/A	N/A
2018-2R	MgZnO	CdSeTe (40%)	N/A	N/A	900 s	120/280/560 s	Te	N/A	N/A	C/Ni Paint	N/A
	100 nm	800 nm	N/A	N/A	420/450°C	330/190/200	30 nm	N/A	N/A	N/A	N/A
2018-5R	MgZnO	CdSeTe (40%)	N/A	N/A	900 s	120/280/560 s	Te	Cd_3As_2 Anneal	N/A	C/Ni Paint	N/A
	100 nm	820 nm	N/A	N/A	420/450°C	330/190/200	30 nm	1800 s @ 360/500°C	N/A	N/A	N/A

*SIMS measurements indicate an arsenic concentration as high as 10^{19} cm^{-3}

REFERENCES

[1] Encyclopædia Britannica, “Periodic Table of the Elements.” [Online]. Available: https://www.britannica.com/science/periodic-table. [Accessed: 03-Jul-2019].

[2] A. S. Stuart R. Wenham, Martin A. Green, Muriel E. Watt, Richard Corkish, *Applied Photovoltaics*, 3rd ed. New York: Earthscan, 2011.

[3] “The extraterrestrial (AM0) solar spectrum.” [Online]. Available: https://www2.pvlighthouse.com.au/resources/courses/altermatt/The Solar Spectrum/The extraterrestrial (AM0) solar spectrum.aspx. [Accessed: 05-Jul-2019].

[4] “Semiconductor Technology from A to Z.” [Online]. Available: https://www.halbleiter.org/en/fundamentals/conductors-insulators-semiconductors/. [Accessed: 09-Jul-2019].

[5] Akash Peshin, “What are semiconductors? And how do they work?,” 2021. [Online]. Available: https://www.scienceabc.com/innovation/what-are-semiconductors-and-how-do-they-work.html.

[6] M. A. Green, *Solar Cells*. Englewood Cliffs: Prentice-Hall, 1998.

[7] Peter Wurfel and Uli Wurfel, *Physics of Solar Cells*, 3rd Editio. Weinheim, Germany: Wiley-VCH, 2016.

[8] P. Wurfel, “The chemical potential of radiation,” *J. Phys. C Solid State Phys.*, vol. 15, no. 18, pp. 3967–3985, 1982, doi: 10.1088/0022-3719/15/18/012.

[9] D. A. Neamen, *Semiconductor Physics and Devices*, 3rd ed. New York: McGraw-Hill, 2003.

[10] “Simple Recombination Model.” [Online]. Available: http://ecee.colorado.edu/~bart/book/recomb.htm. [Accessed: 12-Jul-2019].

[11] R. Beranek, “(Photo)electrochemical methods for the determination of the band edge positions of TiO2-based nanomaterials,” *Adv. Phys. Chem.*, vol. 2011, no. Iv, pp. 80–83, 2011, doi: 10.1155/2011/786759.

[12] A. Onno, C. Chen, P. Koswatta, M. Boccard, and Z. C. Holman, “Passivation, conductivity, and selectivity in solar cell contacts: Concepts and simulations based on a unified partial-resistances framework,” *J. Appl. Phys.*, vol. 126, no. 18, 2019, doi: 10.1063/1.5117201.

[13] U. Wurfel, A. Cuevas, and P. Wurfel, “Charge carrier separation in solar cells,” *IEEE J. Photovoltaics*, vol. 5, no. 1, pp. 461–469, 2015, doi: 10.1109/JPHOTOV.2014.2363550.

[14] “PN Junction Theory.” [Online]. Available: https://www.electronics-tutorials.ws/diode/diode_2.html. [Accessed: 09-Jul-2019].

[15] “Diodes.” [Online]. Available: https://learn.sparkfun.com/tutorials/diodes/real-diode-characteristics. [Accessed: 09-Jul-2019].

[16] "IV Curve." [Online]. Available: https://www.pveducation.org/pvcdrom/solar-cell-operation/iv-curve. [Accessed: 10-Jul-2019].

[17] ASTM, "Standard Test Method for Electrical Performance of Photovoltaic Cells Using Reference Cells Under Simulated Sunlight -- E 948-05," vol. 15, no. Reapproved, pp. 1–5, 2005, doi: 10.1520/E0948-16.Copyright.

[18] A. D. Printz and D. J. Lipomi, "Competition between deformability and charge transport in semiconducting polymers for flexible and stretchable electronics," *Appl. Phys. Rev.*, vol. 3, no. 2, 2016, doi: 10.1063/1.4947428.

[19] T. Gfroerer, "Photoluminescence in Analysis of Surfaces and Interfaces," *Encyclopaedia of Analytical Chemistry*. John Wiley and Sons Ltd, pp. 9209–9231, 2000.

[20] "Photoluminescence." [Online]. Available: https://warwick.ac.uk/fac/sci/physics/current/postgraduate/regs/mpagswarwick/ex5/techniques/optical/pl/. [Accessed: 27-Apr-2020].

[21] L. Xu, L. L. Deng, J. Cao, X. Wang, W. Y. Chen, and Z. Jiang, "Solution-Processed Cu(In, Ga)(S, Se)2 Nanocrystal as Inorganic Hole-Transporting Material for Efficient and Stable Perovskite Solar Cells," *Nanoscale Res. Lett.*, vol. 12, no. 1, 2017, doi: 10.1186/s11671-017-1933-z.

[22] A. Onno *et al.*, "Understanding what limits the voltage of polycrystalline CdSeTe solar cells," *Nat. Energy*, 2022, doi: 10.1038/s41560-022-00985-z.

[23] D. Kuciauskas *et al.*, "Voltage Loss Comparison in CdSe/CdTe Solar Cells and Polycrystalline CdSeTe Heterostructures," *IEEE J. Photovoltaics*, vol. 12, no. 1, pp. 6–10, 2022, doi: 10.1109/JPHOTOV.2021.3117914.

[24] B. Korevaar, G. Zorn, K. Raghavan, J. Cournoyer, and K. Dovidenko, "Cross-Sectional mapping of hole concentrations as a function of copper treatment in CdTe photo-voltaic," *Prog. Photovoltaics Res. Appl.*, vol. 23, pp. 1466–1474, 2015, doi: 10.1002/pip.2576.

[25] A. Onno *et al.*, "Calculation of the thermodynamic voltage limit of CdSeTe solar cells," *Conf. Rec. IEEE Photovolt. Spec. Conf.*, vol. 2020-June, pp. 0535–0537, 2020, doi: 10.1109/PVSC45281.2020.9300938.

[26] M. GREEN, "Radiative efficiency of state-of-the-art photovoltaic cells," *IEEE*, vol. 20, no. 6, pp. 1114–1129, 2012, doi: 10.1002/pip.

[27] M. Yamaguchi, K. H. Lee, K. Araki, N. Kojima, H. Yamada, and Y. Katsumata, "Analysis for efficiency potential of high-efficiency and next-generation solar cells," *Prog. Photovoltaics Res. Appl.*, vol. 26, no. 8, pp. 543–552, 2018, doi: 10.1002/pip.2955.

[28] Picoquant, "Picoharp 300 User's Manual and Technical Data," 2013.

[29] E. S. Barnard *et al.*, "Probing carrier lifetimes in photovoltaic materials using subsurface two-photon microscopy," *Sci. Rep.*, vol. 3, pp. 1–9, 2013, doi: 10.1038/srep02098.

[30] “Time-Resolved Photoluminescence.” [Online]. Available: https://www.picoquant.com/applications/category/materials-science/time-resolved-photoluminescence#images. [Accessed: 11-Jul-2019].

[31] “Electrical characterization of photovoltaic materials and solar cells with the model 4200-SCS semiconductor characterization system,” 2011.

[32] S. Hegedus and W. N. Shafarman, “Thin-film solar cells: device measurements and analysis,” *Prog. Photovoltaics Res. Appl.*, vol. 12, no. 23, pp. 155–176, 2004, doi: 10.1002/pip.518.

[33] A. Luque and S. Hegedus, *Handbook of Photovoltaic Science and Engineering*. John Wiley & Sons, Inc., 2003.

[34] “Global Energy Statistical Yearbook 2021.” [Online]. Available: https://yearbook.enerdata.net/total-energy/world-consumption-statistics.html. [Accessed: 12-Jul-2022].

[35] “EIA projects accelerating renewable consumption and steady liquid fuels growth to 2050.” [Online]. Available: https://www.eia.gov/todayinenergy/detail.php?id=49856. [Accessed: 12-Jul-2022].

[36] D. I. Stern, Z. Csereklyei, and M. Rubio, “Energy and the Economy: Energy and Economic growh the stylized facts,” *IAEE Energy Forum*, pp. 7–9, 2014.

[37] B. Stevenson *et al.*, “Economic Growth and Subjective Well-Being: Reassessing The Easterlin Paradox,” *Natl. Bereau Econ. Res.*, 2008.

[38] M. Perez, R and Perez, “A Fundamental look at Supply Side Energy Reserves For the Planet,” *Sol. Heat. Cool. Program.*, no. April 2009, 2015, doi: 10.1016/j.eneco.2008.12.011.

[39] NASA, “Earth Observatory.” [Online]. Available: https://earthobservatory.nasa.gov/features/CarbonCycle/page4.php. [Accessed: 31-Jul-2019].

[40] C. Best, “A Simple Model of the CO2 greenhouse effect.” [Online]. Available: http://clivebest.com/blog/?p=4265. [Accessed: 31-Jul-2019].

[41] NASA, “Global Climate Change.” [Online]. Available: https://climate.nasa.gov/vital-signs/carbon-dioxide/. [Accessed: 31-Jul-2019].

[42] R. Lindsey, “Climate Change: Atmospheric Carbon Dioxide.” .

[43] N. C. Assessment, “Observed Change.” [Online]. Available: https://nca2014.globalchange.gov/report/our-changing-climate/observed-change. [Accessed: 12-Jul-2022].

[44] A. Smith, “2018’s Billion Dollar Disasters in context,” *NOAA*, 2019. [Online]. Available: https://www.climate.gov/news-features/blogs/beyond-data/2018s-billion-dollar-disasters-

context. [Accessed: 09-Aug-2019].

[45] NASA, “Changes in the Carbon Cycle,” 2011. [Online]. Available: https://earthobservatory.nasa.gov/features/CarbonCycle/page4.php. [Accessed: 08-Aug-2019].

[46] EPA, “Inventory of U.S. Greenhouse Emissions and Sinks, 1990-2017.”

[47] “Carbon dioxide emissions from energy consumption in the United States from 1975 to 2021,” 2022. [Online]. Available: https://www.statista.com/statistics/183943/us-carbon-dioxide-emissions-from-1999/.

[48] A. Petroff, “These countries want to ditch gas and diesel cars,” 2017. [Online]. Available: https://money.cnn.com/2017/07/26/autos/countries-that-are-banning-gas-cars-for-electric/index.html. [Accessed: 09-Aug-2019].

[49] B. Jones, “By 2040, You Won’t Be Able to Buy a Non-Electric Vehicle in These Nations,” 2017. [Online]. Available: https://futurism.com/by-2040-you-wont-be-able-to-buy-a-non-electric-vehicle-in-these-nations. [Accessed: 09-Aug-2019].

[50] “Renewable Capacity Statistics 2019,” 2019.

[51] “Global Market Outlook for Solar Power 2016-2020,” 2016.

[52] Fraunhofer Institute, “Photovoltaics Report,” *Annu. Energy Outlook*, vol. 2013, no. November, pp. 1–18, 2016, doi: 26.05.2014.

[53] “A Snapshot of Global PV,” 2019. [Online]. Available: http://www.iea-pvps.org/index.php?id=266. [Accessed: 14-Aug-2019].

[54] IEA-PVPS, “Snapshot of Global PV Markets 2022,” *Www.Iea-Pvps.Org*, pp. 1–23, 2022.

[55] “First Solar Investor Overview-2022,” 2022. [Online]. Available: https://s2.q4cdn.com/646275317/files/doc_presentations/2022/First-Solar-Investor-Overview-(April-2022).pdf. [Accessed: 27-Jul-2022].

[56] “Manufacturing of Advanced Cadmium Telluride.” [Online]. Available: https://www.usa-cdte.org/.

[57] R. Margolis, D. Feldman, and D. Boff, “Solar Industry Update,” *Natl. Renew. Energy Lab.*, no. May, pp. 1–83, 2018, doi: NREL/PR-6A20-68425.

[58] U.S Energy Information Administration, “U.S Energy Facts Explained,” 2018. [Online]. Available: https://www.eia.gov/energyexplained/index.php?page=us_energy_state. [Accessed: 15-Aug-2019].

[59] T. Wang, “Global Electricity Prices in 2018, by Select Country,” *2019*. [Online]. Available: https://www.statista.com/statistics/263492/electricity-prices-in-selected-countries/. [Accessed: 15-Aug-2019].

[60] Department of Water and Power of the City of Las Angeles, “Board of Water and Power

Commissioners, LADWP Special Meeting Agenda," 2019.

[61] A. B. Mark Widmar, Paul Kaleta, "FIRST SOLAR ANNUAL STOCKHOLDER MEETING," 2019.

[62] EIA, "Levelized Cost and Levelized Avoided Cost of New Generation Resources," *Annu. Energy Outlook 2019*, no. June, p. 25, 2019.

[63] Lazard, "Lazard's Levelized Cost of Energy Analysis - Version 15.0," no. October, pp. 0–20, 2021.

[64] National Renewable Energy Laboratory, "Best Research-Cell Efficiency Chart," *2019*. [Online]. Available: https://www.nrel.gov/pv/cell-efficiency.html. [Accessed: 15-Aug-2019].

[65] W. Shockley and H. J. Queisser, "Detailed Balance Limit of Efficiency of p-n junction solar cells," *J. Appl. Phys.*, vol. 32, no. 3, pp. 510–519, 1961.

[66] G. D. Cody, "Theoretical maximum efficiencies for thermophotovoltaic devices," vol. 58, no. 1999, pp. 58–67, 2011, doi: 10.1063/1.57845.

[67] C. Kittel, *Introduction to Solid State Physics*, 6th Editio. New York: John Wiley & Sons, Inc., 1986.

[68] J. Hader *et al.*, "On the importance of radiative and Auger losses in GaN-based quantum wells," *Appl. Phys. Lett.*, vol. 92, no. 26, 2008, doi: 10.1063/1.2953543.

[69] J. W. Morgan and E. Anders, "Chemical composition of Earth, Venus, and Mercury," *Proc. Natl. Acad. Sci.*, vol. 77, no. 12, pp. 6973–6977, 1980, doi: 10.1073/pnas.77.12.6973.

[70] PVEducation.org, "Solar Cell Production Line." [Online]. Available: https://www.pveducation.org/ru/node/258. [Accessed: 20-Aug-2019].

[71] First Solar, "First Solar Investor Overview." 2019.

[72] V. Fthenakis, "Sustainability of photovoltaics: The case for thin-film solar cells," *Renewable and Sustainable Energy Reviews*, vol. 13, no. 9. pp. 2746–2750, 2009, doi: 10.1016/j.rser.2009.05.001.

[73] A. H. Munshi *et al.*, "Effect of CdCl2 passivation treatment on microstructure and performance of CdSeTe/CdTe thin-film photovoltaic devices," *Sol. Energy Mater. Sol. Cells*, vol. 186, 2018, doi: 10.1016/j.solmat.2018.06.016.

[74] First Solar, "First Solar Sustainability Report," *First Sol. Sustain. Rep.*, pp. 14–32, 2017.

[75] A. Munshi and W. Sampath, "CdTe Photovoltaics for Sustainable Electricity Generation," *J. Electron. Mater.*, 2016, doi: 10.1007/s11664-016-4484-7.

[76] V. Fthenakis and K. Zweibel, "CdTe PV: Real and Perceived EHS Risks," *Natl. Cent. Photovoltaics Sol. Progr. Rev. Meet.*, no. May, pp. 1–3, 2003.

[77] A. H. Munshi, N. Sasidharan, S. Pinkayan, K. L. Barth, W. S. Sampath, and W. Ongsakul, "Thin-film CdTe photovoltaics – The technology for utility scale sustainable energy generation," *Sol. Energy*, vol. 173, no. August, pp. 511–516, 2018, doi: 10.1016/j.solener.2018.07.090.

[78] F. Meillaud, A. Shah, C. Droz, E. Vallat-Sauvain, and C. Miazza, "Efficiency limits for single-junction and tandem solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 18–19, pp. 2952–2959, 2006, doi: 16/j.solmat.2006.06.002.

[79] R. M. Geisthardt, M. Topiˇ, S. Member, and J. R. Sites, "Status and Potential of CdTe Solar-Cell Efficiency," vol. 5, no. 4, pp. 1217–1221, 2015.

[80] M. A. Green, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, M. Yoshita, and A. W. Y. Ho-Baillie, "Solar cell efficiency tables (version 54)," *Prog. Photovoltaics Res. Appl.*, vol. 27, no. 7, pp. 565–575, 2019, doi: 10.1002/pip.3171.

[81] J. M. Burst *et al.*, "Carrier density and lifetime for different dopants in single-crystal and polycrystalline CdTe," *APL Mater.*, vol. 4, no. 11, 2016, doi: 10.1063/1.4966209.

[82] J. Ma *et al.*, "Dependence of the minority-carrier lifetime on the stoichiometry of CdTe using time-resolved photoluminescence and first-principles calculations," *Phys. Rev. Lett.*, vol. 111, no. 6, pp. 1–5, 2013, doi: 10.1103/PhysRevLett.111.067402.

[83] T. A. M. Fiducia *et al.*, "Understanding the role of selenium in defect passivation for highly efficient selenium-alloyed cadmium telluride solar cells," *Nat. Energy*, vol. 4, no. 6, pp. 504–511, 2019, doi: 10.1038/s41560-019-0389-z.

[84] A. H. Munshi *et al.*, "Polycrystalline CdSeTe/CdTe absorber cells with 28 mA/cm2 short-circuit current," *IEEE J. Photovoltaics*, vol. 8, no. 1, pp. 310–314, 2018, doi: 10.1109/JPHOTOV.2017.2775139.

[85] M. O. Reese *et al.*, "Intrinsic surface passivation of CdTe," *J. Appl. Phys.*, vol. 118, no. 15, 2015, doi: 10.1063/1.4933186.

[86] D. Kuciauskas, J. M. Kephart, J. Moseley, W. K. Metzger, W. S. Sampath, and P. Dippo, "Recombination velocity less than 100 cm/s at polycrystalline Al2O3/CdSeTe interfaces," *Appl. Phys. Lett.*, vol. 112, no. 26, pp. 2–7, 2018, doi: 10.1063/1.5030870.

[87] A. Kanevce, M. O. Reese, T. M. Barnes, S. A. Jensen, and W. K. Metzger, "The roles of carrier concentration and interface, bulk, and grain-boundary recombination for 25% efficient CdTe solar cells," *J. Appl. Phys.*, vol. 121, no. 21, 2017, doi: 10.1063/1.4984320.

[88] T. Ablekim, E. Colegrove, and W. K. Metzger, "Interface Engineering for 25% CdTe Solar Cells," *ACS Appl. Energy Mater.*, vol. 1, pp. 5135–5139, 2018, doi: 10.1021/acsaem.8b01173.

[89] J. N. Duenow and W. K. Metzger, "Back-surface recombination, electron reflectors, and paths to 28% efficiency for thin-film photovoltaics: A CdTe case study," *J. Appl. Phys.*, vol. 125, no. 5, 2019, doi: 10.1063/1.5063799.

[90] F. Molva, J. P. Chamonal, and J. L. Pautrat, “Shallow Acceptors in Cadmium Telluride,” *Phys. Status Solidi*, vol. 109, no. 2, pp. 635–644, 1982, doi: 10.1002/pssb.2221090222.

[91] J. H. Yang, W. K. Metzger, and S. H. Wei, “Carrier providers or killers: The case of Cu defects in CdTe,” *Appl. Phys. Lett.*, vol. 111, no. 4, 2017, doi: 10.1063/1.4986077.

[92] E. Kučys, J. Jerhot, K. Bertulis, and V. Bariss, “Copper impurity behaviour in CdTe films,” *Phys. Status Solidi*, vol. 59, no. 1, pp. 91–99, 1980, doi: 10.1002/pssa.2210590112.

[93] S. Wei and S. B. Zhang, “Chemical trends of defect formation and doping limit in II-VI semiconductors : The case of CdTe,” no. May, pp. 1–10, 2002, doi: 10.1103/PhysRevB.66.155211.

[94] D. Krasikov, A. Knizhnik, B. Potapkin, S. Selezneva, and T. Sommerer, “First-principles-based analysis of the influence of Cu on CdTe electronic properties,” *Thin Solid Films*, vol. 535, no. 1, pp. 322–325, 2013, doi: 10.1016/j.tsf.2012.10.027.

[95] L. Zhang, J. L. F. Da Silva, J. Li, Y. Yan, T. A. Gessert, and S. H. Wei, “Effect of copassivation of Cl and Cu on CdTe grain boundaries,” *Phys. Rev. Lett.*, vol. 101, no. 15, pp. 1–4, 2008, doi: 10.1103/PhysRevLett.101.155501.

[96] J. Perrenoud *et al.*, “A comprehensive picture of Cu doping in CdTe solar cells,” *J. Appl. Phys.*, vol. 114, no. 17, 2013, doi: 10.1063/1.4828484.

[97] Y. Yan, K. Jones, J. Zhou, and M. Al-Jassim, “TEM study of Locations of Cu in CdTe Solar Cells,” *MRS Proc.*, vol. 1012, 2007.

[98] J. M. Burst *et al.*, “CdTe solar cells with open-circuit voltage breaking the 1V barrier,” *Nat. Energy*, vol. 1, no. 4, 2016, doi: 10.1038/NENERGY.2016.15.

[99] B. E. Mccandless *et al.*, “Overcoming Carrier Concentration Limits in Polycrystalline CdTe Thin Films with in situ doping,” *Sci. Rep.*, vol. 8, 2018.

[100] S. H. Wei and S. B. Zhang, “First-principles study of doping limits of CdTe,” *Phys. Status Solidi Basic Res.*, vol. 229, no. 1, pp. 305–310, 2002, doi: 10.1002/1521-3951(200201)229:1<305::AID-PSSB305>3.0.CO;2-3.

[101] S. Farrell, T. M. Barnes, W. K. Metzger, J. Park, R. Kodama, and S. Sivananthan, “In Situ Arsenic Doping of CdTe-Si by molecular beam epitaxy,” *J. Electron. Mater.*, vol. 44, no. 9, 2015.

[102] A. Nagaoka, K. B. Han, S. Misra, T. Wilenski, T. D. Sparks, and M. A. Scarpulla, “Growth and characterization of Arsenic doped CdTe single crystals grown by Cd-solvent traveling-heater method,” *J. Cryst. Growth*, vol. 467, pp. 6–11, 2017, doi: 10.1016/j.jcrysgro.2017.03.002.

[103] G. Kartopu *et al.*, “Study of thin film poly-crystalline CdTe solar cells presenting high acceptor concentrations achieved by in-situ arsenic doping,” *Sol. Energy Mater. Sol. Cells*, vol. 194, no. January, pp. 259–267, 2019, doi: 10.1016/j.solmat.2019.02.025.

[104] D. B. Li *et al.*, "Low-temperature and effective ex situ group V doping for efficient polycrystalline CdSeTe solar cells," *Nat. Energy*, vol. 6, no. 7, pp. 715–722, 2021, doi: 10.1038/s41560-021-00848-z.

[105] W. K. Metzger *et al.*, "Exceeding 20% efficiency with in situ group V doping in polycrystalline CdTe solar cells," *Nat. Energy*, vol. 4, no. 10, pp. 837–845, 2019, doi: 10.1038/s41560-019-0446-7.

[106] A. H. Munshi, A. H. Danielson, K. L. Barth, G. Gelinas, J. N. Beaudry, and W. S. Sampath, "Advanced Co-sublimation of Low Bandgap CdSex Te1-x Alloy to Achieve Higher Short-Circuit Current," *2018 IEEE 7th World Conf. Photovolt. Energy Conversion, WCPEC 2018 - A Jt. Conf. 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC*, pp. 148–152, 2018, doi: 10.1109/PVSC.2018.8548272.

[107] C. Reich, A. Danielson, M. Mahaffey, W. Weigand, Z. C. Holman, and W. S. Sampath, "High efficiency undoped CdSeTe solar cells enabled by long lifetimes," *TBD*.

[108] T. K. Al-Hamdi *et al.*, "CdTe synthesis and crystal growth using the high-pressure Bridgman technique," *J. Cryst. Growth*, vol. 534, no. December 2019, p. 125466, 2020, doi: 10.1016/j.jcrysgro.2019.125466.

[109] G. L. Burton *et al.*, "Understanding arsenic incorporation in CdTe with atom probe tomography," *Sol. Energy Mater. Sol. Cells*, vol. 182, no. February, pp. 68–75, 2018, doi: 10.1016/j.solmat.2018.02.023.

[110] D. Krasikov and I. Sankin, "Beyond thermodynamic defect models: A kinetic simulation of arsenic activation in CdTe," *Phys. Rev. Mater.*, vol. 2, no. 10, pp. 1–10, 2018, doi: 10.1103/PhysRevMaterials.2.103803.

[111] R. K. Ahrenkiel and S. W. Johnston, "An optical technique for measuring surface recombination velocity," *Sol. Energy Mater. Sol. Cells*, vol. 93, no. 5, pp. 645–649, 2009, doi: 10.1016/j.solmat.2008.12.028.

[112] M. A. Green and A. W. Y. Ho-Baillie, "Pushing to the Limit: Radiative Efficiencies of Recent Mainstream and Emerging Solar Cells," *ACS Energy Lett.*, vol. 4, no. 7, pp. 1639–1644, 2019, doi: 10.1021/acsenergylett.9b01128.

[113] J. F. Guillemoles, T. Kirchartz, D. Cahen, and U. Rau, "Guide for the perplexed to the Shockley–Queisser model for solar cells," *Nat. Photonics*, vol. 13, no. 8, pp. 501–505, 2019, doi: 10.1038/s41566-019-0479-2.

[114] U. Rau, B. Blank, T. C. M. Müller, and T. Kirchartz, "Efficiency Potential of Photovoltaic Materials and Devices Unveiled by Detailed-Balance Analysis," *Phys. Rev. Appl.*, vol. 7, no. 4, pp. 1–9, 2017, doi: 10.1103/PhysRevApplied.7.044016.

[115] J. Moseley *et al.*, "Impact of dopant-induced optoelectronic tails on open-circuit voltage in arsenic-doped Cd(Se)Te solar cells," *J. Appl. Phys.*, vol. 128, no. 10, 2020, doi: 10.1063/5.0018955.

[116] A. H. Munshi *et al.*, "Effect of CdCl2 passivation treatment on microstructure and

performance of CdSeTe/CdTe thin-film photovoltaic devices," *Sol. Energy Mater. Sol. Cells*, vol. 186, no. June, pp. 259–265, 2018, doi: 10.1016/j.solmat.2018.06.016.

[117] S. W. Glunz and F. Feldmann, "SiO2 surface passivation layers – a key technology for silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 185, no. February, pp. 260–269, 2018, doi: 10.1016/j.solmat.2018.04.029.

[118] Z. Zhang and J. T. Yates, "Band bending in semiconductors: Chemical and physical consequences at surfaces and interfaces," *Chem. Rev.*, vol. 112, no. 10, pp. 5520–5551, 2012, doi: 10.1021/cr3000626.

[119] S. Cui, "Metal-Semiconductors Contacts," 2019. [Online]. Available: https://eng.libretexts.org/Bookshelves/Materials_Science/Supplemental_Modules_(Materials_Science)/Semiconductors/Metal-Semiconductors_Contacts.

[120] B. Hoex, J. J. H. Gielis, M. C. M. Van De Sanden, and W. M. M. Kessels, "On the c-Si surface passivation mechanism by the negative-charge-dielectric Al2O3," *J. Appl. Phys.*, vol. 104, no. 11, 2008, doi: 10.1063/1.3021091.

[121] G. Agostinelli *et al.*, "Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge," *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 18–19, pp. 3438–3443, 2006, doi: 10.1016/j.solmat.2006.04.014.

[122] C. L. Perkins, D. L. McGott, M. O. Reese, and W. K. Metzger, "SnO2 -Catalyzed Oxidation in High-Efficiency CdTe Solar Cells," *ACS Appl. Mater. Interfaces*, vol. 11, no. 13, pp. 13003–13010, 2019, doi: 10.1021/acsami.9b00835.

[123] J. M. Kephart, "Optimization of the front contact to minimize short-circuit current losses in CdTe thin-film solar cells," Colorado State Univeristy, 2015.

[124] T. Minemoto, T. Negami, S. Nishiwaki, H. Takakura, and Y. Hamakawa, "Preparation of Zn1-xMgxO films by radio frequency magnetron sputtering," *Thin Solid Films*, vol. 372, no. 1, pp. 173–176, 2000, doi: 10.1016/S0040-6090(00)01009-9.

[125] C. Moffett, "Characterization of Tellurium back contact layer for CdTe thin film devices," Colorado State University, 2018.

[126] A. P. Nicholson, A. H. Munshi, U. Pozzoni, and W. S. Sampath, "First Principles Approach to CdTe/Te Interface Band Alignment Using Density Functional Theory and Nonequilibrium Green's Function," *2018 IEEE 7th World Conf. Photovolt. Energy Conversion, WCPEC 2018 - A Jt. Conf. 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC*, pp. 1932–1936, 2018, doi: 10.1109/PVSC.2018.8547599.

[127] A. Danielson, C. Reich, W. Weigand, and Z. Holman, "CdSexTe1-x/CdTe Devices with Reduced Interface Recombination Through Novel Back Contacts and Group-V Doping," *IEEE PVSC Conf. Proceeedings*, 2020.

[128] Di Xiao, X. Li, D. Wang, Q. Li, K. Shen, and D. Wang, "CdTe thin film solar cell with NiO as a back contact buffer layer," *Sol. Energy Mater. Sol. Cells*, vol. 169, no. April, pp. 61–67, 2017, doi: 10.1016/j.solmat.2017.05.006.

[129] C. L. Perkins *et al.*, “Interfaces Between CdTe and ALD Al2O3,” *IEEE J. Photovoltaics*, vol. 8, no. 6, pp. 1858–1861, 2018, doi: 10.1109/jphotov.2018.2870139.

[130] J. M. Kephart *et al.*, “Sputter-Deposited Oxides for Interface Passivation of CdTe Photovoltaics,” *IEEE J. Photovoltaics*, vol. 8, no. 2, pp. 587–593, 2018, doi: 10.1109/JPHOTOV.2017.2787021.

[131] E. O. Filatova and A. S. Konashuk, “Interpretation of the Changing the Band Gap of Al2O3 Depending on Its Crystalline Form: Connection with Different Local Symmetries,” 2015, doi: 10.1021/acs.jpcc.5b06843.

[132] Y. Zeng *et al.*, “Theoretical exploration towards high-efficiency tunnel oxide passivated carrier-selective contacts (TOPCon) solar cells,” *Sol. Energy*, vol. 155, pp. 654–660, 2017, doi: 10.1016/j.solener.2017.07.014.

[133] F. Feldmann, M. Bivour, C. Reichel, H. Steinkemper, M. Hermle, and S. W. Glunz, “Tunnel oxide passivated contacts as an alternative to partial rear contacts,” *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 46–50, 2014, doi: 10.1016/j.solmat.2014.06.015.

[134] N. Muthukumarasamy, S. Jayakumar, M. D. Kannan, and R. Balasundaraprabhu, “Structural phase change and optical band gap bowing in hot wall deposited CdSexTe1-x thin films,” *Sol. Energy*, vol. 83, no. 4, pp. 522–526, 2009, doi: https://doi.org/10.1016/j.solener.2008.10.004.

[135] D. E. Swanson, J. R. Sites, and W. S. Sampath, “Co-sublimation of CdSexTe1−x layers for CdTe solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 159, pp. 389–394, 2017, doi: 10.1016/j.solmat.2016.09.025.

[136] K. J. Hayes, “CdTe Solar Cell Optimization by Planar and Transmission EBSD,” *Microsc. Microanaylsis*, vol. 2, pp. 2–3, 2016.

[137] A. Axelevitch and G. Golan, “Hot-probe method for evaluation of majority charged carriers concentration in semiconductor thin films,” *Facta Univ. - Ser. Electron. Energ.*, vol. 26, no. 3, pp. 187–195, 2013, doi: 10.2298/fuee1303187a.

[138] “Hall Effect Measurements.” [Online]. Available: https://warwick.ac.uk/fac/sci/physics/current/postgraduate/regs/mpagswarwick/ex5/techniques/electronic/hall-effect/. [Accessed: 08-Sep-2022].

[139] M. Al-Jassim, “Scanning Kelvin Probe Microscopy.” [Online]. Available: https://www.nrel.gov/materials-science/scanning-kelvin.html. [Accessed: 08-Sep-2022].

[140] H. Ben-Dor, L. Yellin, N. Shaham, “Low Temperature Synthesis of Pseudobinary Chalcogenides,” *Mater. Res. Bull.*, vol. 19, no. 4, pp. 465–470, 1984, doi: https://doi.org/10.1016/0025-5408(84)90107-7.

[141] G. Vitrikhovskii, N. Mizetskaya, I. Oliinyk, “Properties of Alloys Belonging to the System CdSe-CdTe,” *Inorg. Matterials*, vol. 7, p. 657, 1971.

[142] I. B. Shevchenko, Y. . Nikol’skii, E. M. Stairnova, V. R. Darashkevich, and Y. E. Sutyrin,

"Solid Solutions of the System CdSe-CdTe," *Inorg. Mater.*, vol. 10, no. 184, 1974.

[143] J. Litwin, "X-Ray Examination of the Binary System CdTe-CdSe," *Phys. Status Solidi*, vol. 5, no. 3, pp. 551–553, 1964, doi: 10.1002/pssb.19640050311.

[144] W. Danielson, A., Reich, C., Drayton, J., Bothwell, A., Shimpi, T., Sites, J., Sampath, "A comprehensive material study of CdSeTe films deposited with differing selenium compositions," *Thin Solid Films*, 2022.

[145] J. Moseley *et al.*, "Recombination by grain-boundary type in CdTe," *J. Appl. Phys.*, vol. 118, no. 2, 2015, doi: 10.1063/1.4926726.

[146] J. D. Major, Y. Y. Proskuryakov, K. Durose, G. Zoppi, and I. Forbes, "Control of grain size in sublimation-grown CdTe, and the improvement in performance of devices with systematically increased grain size," *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 6, pp. 1107–1112, 2010, doi: 10.1016/j.solmat.2010.02.034.

PUBLICATIONS

Journal Publications

Danielson, A., Reich, C., Munshi, A., Pandey, R., Sites, J., & W. Sampath "Electroptical characterization of arsenic-doped CdSeTe and CdTe solar cell absorbers doped *in-situ* during close space sublimation". Thin Solid Films. *Under Review*.

Danielson, A., Reich, C., Bothwell, A., Drayton, Shimpi, T., Sites, J., & W. Sampath "A comprehensive material study of CdSeTe films deposited with differing selenium compositions*". Under Review*.

Reich, C., **Danielson, A.,** Onno, A., Mahaffey, M., Weigand, W., Holman, Z., & W. Sampath "High efficiency undoped CdSeTe solar cells enabled by long lifetimes". *In preparation.*

Xiao, C., Jiang, C-S., Nardone, M., Albin, D., **Danielson, A.,** Munshi, A., Shimpi, T., Sampath, W., Jones, S., Al-Jassim, M., Teeter, G., Haegel, N., & H. Moutinho "Microscopy Visualization of Carrier Transport in CdSeTe/CdTe Solar Cells," ACS Applied Materials & Interfaces. Accepted. (2022)

Onno, A., Reich, C., Li, S., **Danielson, A.**, Weigand, W., Bothwell, A., Grover, S., Bailey, J., Xiong, G., Kuciauskas, D., Sampath, W., & Z. C. Holman "Understanding what limits the voltage of polycrystalline CdSeTe solar cells," *Nature Energy*. (2022) https://doi.org/10.1038/s41560-022-00985-z

Jiang, C., Albin, D., Nardone, M., Howard, K.J., **Danielson, A.,** Munshi, A., Shimpi, T., Xiao, C., Moutinho, H.R., Al-Jassim, M.M., Teeter, G., & W. Sampath "Electrical Potential Investigation of Reversible Metastability and Irreversible Degradation of CdTe Solar Cells," *Solar Energy Materials and Solar Cells.* (2021)

Shah, A., Pandey, R., Nicholson, A., Lustig, Z., Abbas, A., **Danielson, A.,** Walls, J., Munshi, A., & W. Sampath "Understanding the Role of CdTe in Polycrystalline $CdSe_0Te_{1-x}$/CdTe Graded Bilayer Photovoltaic Device" Submitted to *Solar Rapid Research Letters*. (2021)

Zhao, G., Reich, C., Onno, A., Bothwell, A., **Danielson, A**., Holman, Z., Sampath, W.S., & C. Walden "Robust passivation of CdSeTe based solar cells using reactively sputtered magnesium zinc oxide." *Solar Energy Materials and Solar Cells.* (2021)

Guo, J., Sharma, A., Munshi, A., Reich, C., **Danielson, A.,** Sampath, W., Swain, S., & R. Klie "Study of Arsenic Doped CdSeTe Solar Cells Using Transmission Electron Microscopy." *Microscopy and Microanalysis*. (2020)

Munshi, A. H., Kephart, J. M., Abbas, **A., Danielson,** A., Gẽlinas, G., Beaudry, J. N., Barth, Walls, J. M., & W. Sampath "Effect of $CdCl_2$ passivation treatment on microstructure and performance of CdSeTe/CdTe thin-film photovoltaic devices." *Solar Energy Materials and Solar Cells.* (2018)

Conference Proceedings

Danielson, A., Reich, C., Maheffey, M., Onno, A., Holman, Z.C., & W. Sampath. (2022, June) Native Oxide Growth on Cd(Se)Te for Improved Back Surface Passivation. In *2022 IEEE 49th Photovoltaic Specialists Conference.*

Danielson, A., Kuciauskas, D., Reich, C., Li, S., Onno, A., Weigand, W., Kindvall, A., Munshi, A., Holman, Z., & Sampath, W. (2020, June) $CdSe_xTe_{1-x}$/CdTe Devices with Reduced Interface Recombination Through Novel Back Contacts and Group-V Doping. In *2020 IEEE 47th Photovoltaic Specialists Conference*.

Kuciauskas, D., Albin, D., Moseley, J., Li, S., Cajev, P., Reich, C., Munshi, A., **Danielson, A.,** & Sampath, W. (2020, June) Microsecond Carrier Lifetimes in Polycrystalline CdSeTe Heterostructures and in CdSeTe Thin Film Solar Cells. In *2020 IEEE 47th Photovoltaic Specialists Conference*.

Munshi, A., Reich, C., **Danielson, A.,** Pandey, R., Kuciauskas, D., Li, S., Shah, A., Swain, S., Shimpi, T., Al-Hamdi, T., Lynn, K., & Sampath, W. (2020, June) Arsenic Doping of Polycrystalline CdSeTe for Microsecond Life-times and High Carrier Concentrations. In *2020 IEEE 47th Photovoltaic Specialists Conference*.

Onno, A., **Danielson, A.,** Reich, C., Kindvall, A., Weigand, W., Kuciauskas, D., Sampath, W., & Holman, Z. (2020, June) What limits the voltage of CdSeTe solar cells? In *2020 IEEE 47th Photovoltaic Specialists Conference*.

Shimpi, T., Reich, C., **Danielson, A.,** Munshi, A., Kindvall, A., Pandey, R., Barth, K., & Sampath, W. (2020, June) Influence of Process Parameters and Absorber Thickness on Efficiency of Polycrystalline CdSeTe/CdTe Thin Film Solar Cells. In *2020 IEEE 47th Photovoltaic Specialists Conference*.

Danielson, A., Munshi, A., Onno, A., Weigand, W., Kindvall, A., Reich, C., Yu, Z,. Shi, J., Holman, Z., Kuciauskas, D., Abbas, A., Walls, J., & Sampath, W. (2019, June) Sputtered Aluminum Oxide and p^+ Amorphous Silicon Back Contact for Improved Hole Extraction in Polycrystalline $CdSe_xTe_{1-x}$ and CdTe Photovoltaics. In *2019 IEEE 46th Photovoltaic Specialists Conference.*

Greenhalgh, R., Tsai, V., Abbas, A., Kornienko, V., Fiducia, T., Togay, M., Li, K., Grovener, C., **Danielson, A.,** Munshi, A., Barth, K., Sampath, W., Bowers, J., & Walls, J. (2019, June) Analysis of an MZO/CdTe photovoltaic device treated with cadmium bromide. In *2019 IEEE 46th Photovoltaic Specialists Conference.*

Kindvall, A., Munshi, A., Shimpi, T., **Danielson, A.,** & Sampath, W. (2019, June) Effect of Process Temperature and Coper Doping on the Performance of ZnTe:Cu Back Contacts in CdTe Photovoltaics. In *2019 IEEE 46th Photovoltaic Specialists Conference.*

Munshi, A., **Danielson, A.,** Swain, S., Reich, C., Shimpi, T., McPherson, S., Lynn, K., Kuciauskas, D., Ferguson, A., Guo, J., Klie, R., & Sampath, W.S. (2019, June) Doping $CdSe_xTe_{1-x}$/CdTe Graded Absorber Films with Arsenic for Thin-Film Photovoltaics. In *2019 IEEE 46th Photovoltaic Specialists Conference.*

Danielson, A., Munshi, A., Kindvall, A., Swain, S., Barth, K., Lynn, K., & Sampath, W. (2018, June) Doping CdTe Absorber Cells using Group V Elements. In *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion.*

Danielson, A., Munshi, A., Swanson, D., Drayton, J., Kartopu, G., Irvine, S., & Sampath, W.*S.* (2018, June) MOCVD Deposition of Group V Doped CdTe in Sublimated CdTe and CdSeTe Devices. In *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion.*

Kindvall, A., Munshi, A., Shimpi, T., **Danielson, A.,** & Sampath, W. (2018, June) Copper-Doped Zinc Telluride as a Back Contact for Cadmium Telluride Photovoltaics. In *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion.*

Munshi, A., **Danielson, A.,** Barth, K, Gḗlinas, G., Beaudry, J. N., & Sampath, W. (2018, June) Advanced Co-sublimation of Low Bandgap $CdSe_xTe_{1-x}$ Alloy to Achieve Higher Short-Circuit Current. In *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion.*

Munshi, A., Kephart, J. M., Hemenway, D., Shimpi, T., Abbas, A., Cameron, K**., Danielson, A.,** Barth, Walls, J. M., & Sampath, W. (2018, June) Advanced co-sublimation hardware for deposition of graded ternary alloys in thin-film applications. In *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion.*

Munshi, A., **Danielson, A.,** Kindvall, A., Barth, K., & Sampath, W. (2018, June) Investigation of Sputtered Oxides and p+ Back-contact for Polycrystalline CdTe and CdSeTe Photovoltaics. . In *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion.*