DISSERTATION

DEVELOPMENT AND ADVANCEMENT OF THIN CdTe-BASED SOLAR CELLS FOR PHOTOVOLTAIC PERFORMANCE IMPROVEMENTS

Submitted by

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ABSTRACT

DEVELOPMENT AND ADVANCEMENT OF THIN CdTe-BASED SOLAR CELLS FOR PHOTOVOLTAIC PERFORMANCE IMPROVEMENTS

Photovoltaic technologies, with an essentially infinite energy source, large total capacity, and demonstrated cost competitiveness, are well-positioned to meet growing global demand for clean energy. Cadmium-telluride (CdTe) thin-film photovoltaics is advantageous primarily for its direct optical band gap (approximately 1.48 eV) which is well-matched to the standard AM 1.5G solar spectrum, and its high absorption coefficient. These advantages, in tandem with innovations in fabrication and photovoltaic design in the past decade, have significantly increased CdTe photovoltaic device performance and reduced cost.

Major advances in CdTe device performance have been achieved through improved current collection and fill factor, however, the open-circuit voltage (V_{OC}) of CdTe devices remains limited compared to the band gap-determined maximum achievable V_{OC}. The voltage deficit could be minimized through various approaches, and this work addresses it through progressive structural changes to a thin CdTe device. Absorbers of less than 2 µm were pursued for ultimate electron-reflector devices which incorporate a wide band-gap material behind the absorber to induce a back-surface field via a back-side conduction-band offset for improved V_{OC}.

An optimized and stable base structure is necessary to quantify characteristics and improvements in progressive devices with additional material layers. Thin, 0.4-1.2 µm CdTe absorber devices were optimized and demonstrated respectable and repeatable performance parameters, and a maximum efficiency of 15.0% was achieved with only 1.2 µm CdTe. Capacitance measurements also showed that thinner devices had fully-depleted absorbers into forward bias.

To improve device performance through increased current collection, a 1.4-eV band gap CdSeTe layer was introduced as an additional absorber material preceding CdTe. Prior understanding of the effects of the additional CdSeTe material was incomplete, and this work deepens and expands this understanding. Performance improvement was achieved for thin, 1.5-µm absorber devices with no intentional interdiffusion of the CdSeTe and CdTe. The importance of the CdSeTe thickness was demonstrated, where performance was consistently reduced for CdSeTe thickness greater than CdTe thickness, independent of CdSe composition in the close-space sublimation (CSS) CdSeTe source material. Longer time-resolved photoluminescence (TRPL) tail lifetimes in CdSeTe/CdTe devices compared to CdTe devices suggested better bulk properties, and current loss analysis showed that CdSeTe is the dominant absorber in 0.5-µm CdSeTe/1.0-µm devices. 1.5-µm CdSeTe/CdTe devices demonstrated increased current collection and 30-mV voltage deficit reduction due to the 100-meV narrower band gap of CdSeTe compared to CdTe and passivating effects of selenium, for an ultimate efficiency improvement to 15.6%.

Lattice-constant matching to CdTe and wide, ∼1.8-eV band-gap requirements directed the selection of CdMgTe as the electron-reflector layer. CdMgTe was incorporated into the CdSeTe/CdTe device structure first through CSS, but sputter deposition was found to be more favorable to address the material complexities of CdMgTe (temperature-induced magnesium diffusion and $CdCl_2$ passivation loss, doping, and MgO formation), and produced higher-performing CdMgTe electron-reflector devices. Low substrate temperature achievable in sputtered CdMgTe deposition proved the greatest advantage over CSS-CdMgTe: $CdCl_2$ passivation and magnesium can be appropriately maintained with a corresponding maintenance of device performance, whereas temperature-induced $CdCl_2$ passivation loss or magnesium loss will occur for CSS-deposited CdMgTe with incumbent performance reduction. Through low-temperature depositions, doping optimization, and small structural adjustments, 16.0% efficiency was achieved with CdMgTe sputtered on 0.5-µm CdSeTe/1.0-µm CdTe absorbers, the highest-known CdMgTe electron-reflector device performance. The CdMgTe and non-CdMgTe-containing device V_{OC}'s suggested that electron reflection was

enacted with partial success for the sputter CdMgTe-incorporated structure, but the significant improvements expected based on simulation have not been realized due to MgO formation and a negative valence-band offset which somewhat impedes hole transport to the back contact. Suggestions to overcome or circumvent these limitations are presented and discussed in the context of progressed understanding of CdMgTe electron-reflector devices.

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Chapter 1

INTRODUCTION

1.1 Status of the World Energy Problem

Global energy demand has accelerated over the last century due to significant population growth, expanded industrial and technological systems, and rising standards of living; world energy consumption increased by an order of magnitude from ∼50 exajoules in 1900 to 583.9 extrajoules in 2019 (corresponding to ∼14,000 to 162,000 terrawatt-hours) [1, 2]. To meet these demands, energy extraction, generation, and distribution have traditionally relied on fossil fuel energy sources such as oil, coal, and natural gas. However, these energy sources have several drawbacks. First is their finite supply, and although reported reserve quantities may vary, the availability of these fuel sources is inherently limited such that additional energy sources will be required. Second are the well-documented negative environmental effects caused by the burning of fossil fuels. Climate change, which encompasses increasing global temperature, rising sea levels, shrinking glaciers, accelerating ice melt at earth's poles, and shifts in flower and plant bloom times, is predominantly human-caused and directly linked to the increased concentration of greenhouse gases in earth's atmosphere (from 280 to 414 ppm in the last 150 years) [3–5]. Carbon dioxide is the most abundant greenhouse gas (comprising about 2/3 of the total), and its emission is predominantly caused by the burning of fossil fuels [3–6]. Continued climate change will lead to rising temperatures, more extreme weather patterns (drought, heat waves, changes in precipitation, and increased hurricane intensity), rising sea levels, accelerated ice melt, and altered grow seasons [5]. The October 2018 IPCC (Intergovernmental Panel on Climate Change) special report on the impacts of global warming found that many of these adverse effects will come at temperatures 1.5 °C above pre-industrial levels [7]. Limiting global warming to 1.5 °C will require rapid and

extensive societal modifications, and given the massive contribution of fossil fuels to this warming, significant changes can be made with a transition to renewable energy sources.

1.2 Advantages of Solar Energy

Renewable energy sources such as wind, solar, geothermal, hydro, and biomass are favorable alternatives to fossil fuels for the significant reduction in greenhouse gas emissions. However, given the large global energy demand, not all of these sources are equally viable. Fig. 1.1 compares the energy reserves for renewables and non-renewables, where the volume of each sphere represents the total recoverable energy from finite reserves (for the cases of coal, petroleum, uranium, and natural gas), and the yearly recoverable energy from renewable sources [8]. These are compared to the total world energy use per year, 16 TW-year per year. This provides a clear visual representation of the primary advantage of solar energy: its total capacity. The solar resource is larger than all other renewables combined by orders of magnitude, and each of these resources with the exception of wind, do not provide nearly enough capacity individually to satisfy world energy demands. Solar energy is also advantageous for its cost-competitiveness: manufacturing costs are below 10 ¢/W, and LCOE (levelized cost of energy) is generally near or below grid parity for utility-scale implementation (this is location-dependent for both the price of electricity and amount of solar radiation received), with reported values decreasing each year [9, 10]. Each energy source has limitations such as intermittency, such that replacing fossil fuels will require the collective development of all renewable energy sources, with solar offering extremely promising contributions.

1.3 Cadmium Telluride Photovoltaic Technology

Solar radiation can be directly converted to electrical power through the use of photovoltaic (PV) devices that operate via the internal photoelectric effect [11]. Solar cells thus require an absorber material, which also defines individual PV technologies. Silicon currently

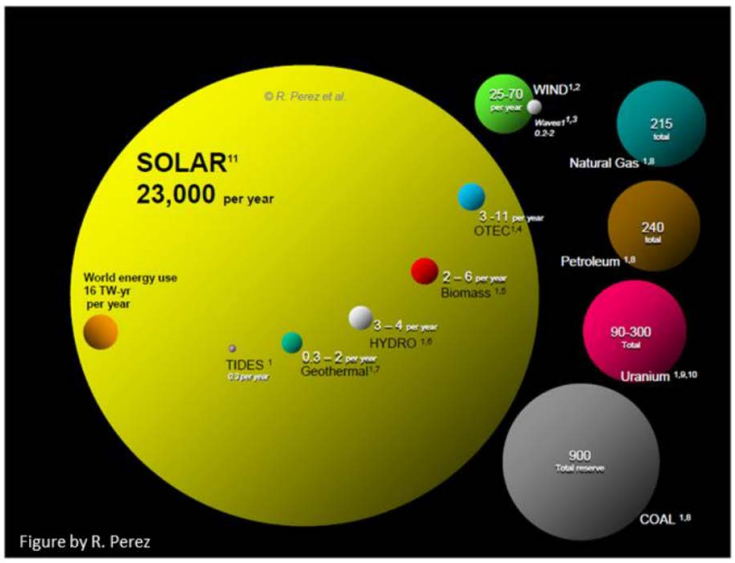

Figure 1.1: Planetary reserves of renewable and finite energy sources compared to the 16 TW-year per year world energy demand. From [8].

makes up ∼90% of the global PV market, although rapid understanding, development, and production of cadmium telluride (CdTe) technology in the past decade has positioned it to be increasingly competitive [12, 13].

CdTe has many advantages which make it favorable for terrestrial photovoltaic solar energy conversion. First, CdTe has a direct optical band gap (E_g) of approximately 1.48 eV which is very closely matched to the standard AM 1.5G solar spectrum such that it is capable of absorbing a large part of that spectrum. It also has a high absorption coefficient (greater than 5 x 10^5/cm) such that 99% of the absorbable incident AM 1.5G photons with E>E_g are absorbed within 2 µm of CdTe material [14]. This translates to a number of associated manufacturing advantages, the first being significantly less required material (compared to crystalline Si which is typically two orders of magnitude thicker [14]), with affiliated reduction in fabrication time and cost. Coupled to this is significantly less energy payback time, which is much less than a year [15]. Thin CdTe absorbers also make semi-transparent and bifacial structures achievable for the realization of new routes to improved photovoltaic efficiencies [16, 17]. The numerous successful fabrication techniques for CdTe deposition,

including close-space sublimation (CSS), vapor transport deposition (VTD), physical vapor deposition (PVD), sputtering, electrodeposition, and screen printing promotes research and industry flexibility and versatile scalability from personal-use mini-modules to grid-integrated solar arrays [14].

Despite the many material and manufacturing advantages of CdTe and documented improvement in efficiencies, production, reliability, and cost-effectiveness, CdTe module performance is still notably lower than the technology-based theoretical maximum [18]. This performance differential is tied to limited improvement in the performance parameter, open circuit voltage (V_{OC}) [19, 20]. Therefore this work focuses on improving CdTe-based photovoltaic device efficiencies through progressive structural changes to a thin CdTe device structure to target the voltage deficit limitation.

Chapter 2

BACKGROUND

2.1 Semiconductor Basics

Photovoltaic device operation relies on the incorporation of semiconductor materials into device structures. Semiconductors are a group of crystalline, polycrystalline, or amorphous solids (which are characterized by the size of their ordered crystal structure) that have electronic energy bands caused by the closely-spaced electron states in the repeating lattice structure [21, 22]. Given the Pauli exclusion principle, these energy bands will be occupied by electrons up to a certain level, the Fermi level (E_F), which is the energy at which a state has a 50% probability of being filled with an electron [21]. For increasing temperature, electrons may gain energy greater than E_F such that the occupation of an electronic state can be described by a probability-of-occupation function, the Fermi-Dirac distribution function, $f(E)$:

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \tag{2.1}$$

where E is the electron state energy, k is Boltzmann's constant, and T is absolute temperature.

The position of the Fermi level energy in relation to allowed energy bands dictates the material classification as a metal, insulator, or semiconductor. In metals, the Fermi level is located within an allowed band such that electrons can contribute to current flow. In insulators, where there is a fully-occupied band and a next-highest band devoid of electrons separated by a large energy gap (as the definition of E_F dictates), the Fermi level lies in the forbidden band between the filled and unfilled allowed bands. Current does not flow because neither completely empty nor filled bands permit electron motion [21, 22]. A semiconductor is similar to an insulator but with a much narrower forbidden energy gap such that at

higher temperatures some levels of the filled band become vacant and some in the next highest band become filled. The almost-full band, the valence band, has unoccupied states devoid of electrons, which are more easily described by states which are *filled* by holes (an electron's positively charged pseudo-particle opposite) and the almost empty band, the conduction band, has some electron-occupied states. Since the states in the valence and conduction bands are mostly empty of holes and electrons respectively, charge carriers in these bands are mobile such that current can flow [21, 22]. Fig. 2.1 shows the valence and conduction bands in momentum space (a) and simplified band blocks (b) and (c) for direct band-gap p-type and n-type semiconductors (defined below). The band gap corresponds to the energy difference between the conduction band minimum and valence band maximum. It is inherently a material property and can be used as an excitation threshold: incident photons with $E \geq E_g$, when absorbed by the crystal, have sufficient energy to excite an electron from the valence to conduction band and create an electron-hole pair [21, 22].

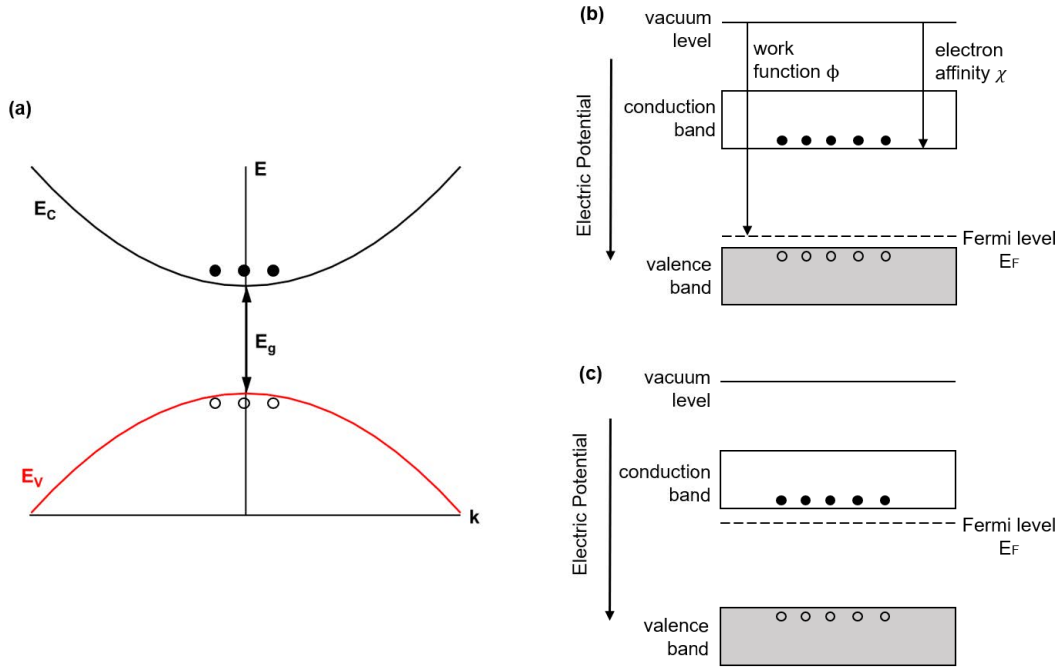

Figure 2.1: Valence and conduction bands in momentum space (a) and simplified band blocks for p-type (b) and n-type semiconductors (c).

Intrinsic semiconductors contain negligible impurities such that the electron and hole concentrations, n and p respectively, are equal. With the presence of interstitial or substitutional impurities in the lattice, which classify the semiconductor as extrinsic, the carrier concentrations are no longer equal and at equilibrium are given by [21, 22]:

$$n = N_C e^{(E_F - E_C)/kT} \tag{2.2}$$

and

$$p = N_V e^{(E_V - E_F)/kT} \tag{2.3}$$

where N_C and N_V are constant at fixed temperature and correspond to the effective density of states in the conduction and valence bands respectively.

$$N_C = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2},\ N_V = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \tag{2.4}$$

where h is Planck's constant and m_n^* and m_p^* are effective masses for electrons and holes respectively.

The purposeful addition of impurities to a semiconductor is called doping, and is typically accomplished by the incorporation of an impurity atom into the crystal. Dependent on the valence properties of the semiconductor and impurity, the impurities can either give up an electron, and are referred to as donors, or accept electrons and referred to as acceptors [21,23]. Because the energy required to release the electrons into the conduction band for donors and holes into the valence band for acceptors is relatively small, this gives rise to allowed energy levels in the band gap just below the conduction band minimum for donors, and just above the valence band maximum for acceptors. This accordingly shifts the Fermi energy up or down respectively, and these impurity-shifted energy states classify semiconductors as p-type or n-type, which have an excess concentration of holes or electrons respectively [21, 23]. The Fermi energy shifts for p-type and n-type semiconductors are pictured in Figs. 2.1 (b) and (c) respectively. For p-type CdTe, Cu is a historically-used dopant, although other group V dopants have been or are currently being explored [24–26].

2.2 P-N Junctions

p-n junctions are formed when a p-type and n-type semiconductor material are brought into contact, and serve as the basis for most photovoltaic device operation. The inherent asymmetry in carrier transport properties of p-type and n-type semiconductors generate electron flow such that electrons ultimately flow from the p-type to n-type region, and vice versa for holes. An initial movement of electrons (and holes) from the n-type (p-type) to p-type (n-type) material occurs due to the concentration gradient between the two materials. This leaves behind positive (and negative) ion cores such that an electric field is created, directed from n-type to p-type, which opposes the inherent diffusion motion [21].

Since a system in thermal equilibrium can only have one Fermi level, and regions which are sufficiently far from the junction are relatively unaffected by junction effects such that their Fermi levels remain unchanged compared to that of the material in isolation, a transition region near the junction exists in which a potential change, also known as built-in potential, V_{bi}, occurs [21]. This is pictured in Fig. 2.2.

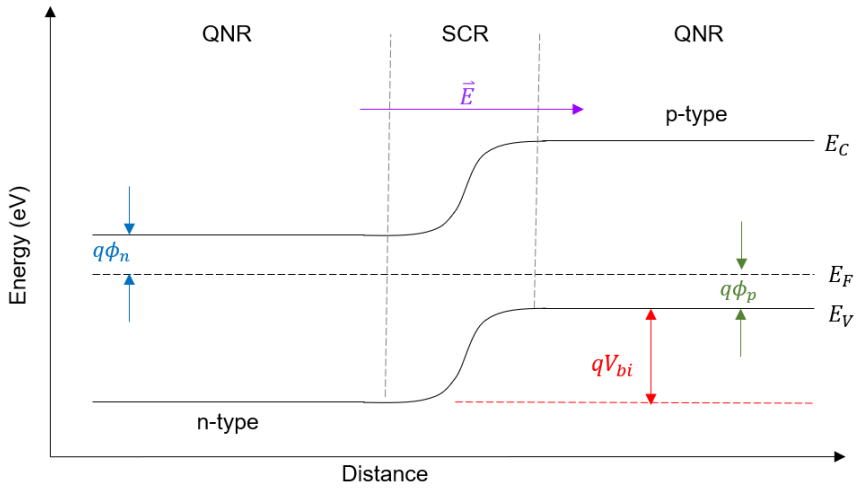

Figure 2.2: n-p junction band diagram in equilibrium which emphasizes the electric field direction, built-in potential, energy differential between the Fermi energy and conduction-band minimum and valence-band maximum, (ϕ_n, ϕ_p), and space-charge region (SCR) and quasi-neutral regions (QNR).

The electric field will sweep carriers away from the junction, ideally with electrons in the conduction band moving toward the n-type side and holes in the valence band moving toward the p-type side. This creates the space-charge region (SCR) or depletion region, where carrier densities are assumed small such that only ionized dopants contribute to space charge density [21]. Further from the junction are the quasi-neutral regions (QNR) where the space-charge density is assumed to be zero. The built-in potential, induced by the necessity for Fermi energy conservation, is given by:

$$V_{bi} = \frac{E_g}{q} - \phi_n - \phi_p \tag{2.5}$$

where q is the elementary charge, and $\phi_n = E_C - E_F$ on the n-type side and $\phi_p = E_F - E_V$ on the p-type side. Given Eqs. 2.2 and 2.3 and the definition of the intrinsic carrier concentration [21],

$$n_i^2 = N_C N_V e^{-E_g/kT} \tag{2.6}$$

the built-in potential can be written in terms of carrier concentrations as:

$$V_{bi} = \frac{kT}{q} ln\left(\frac{np}{n_i^2}\right) \tag{2.7}$$

The carrier concentration behavior presented is applicable for the case of equilibrium, however under non-equilibrium conditions, such as applied voltage or illumination, excess carriers dominate the electrical properties of the solar cell, and these carrier dynamics are fundamental to solar cell operation.

2.3 Carrier Dynamics

Under non-equilibrium conditions such as varied temperature, applied voltage, or incident light, three stages of carrier dynamics occur in a solar cell: generation, carrier transport, and recombination. While described individually for simplicity, these three processes occur simultaneously in the solar cell. Described simply, generation is the creation of electron-hole

pairs often from absorbed photons with energy greater than the absorber band gap energy. Due to reflection and absorption at surfaces preceding the absorber layer, and exponential photon flux density dependence, the generation rate will decrease as a function of depth into the solar cell [21, 22].

Carrier transport, or the movement of electrons and holes, is dominated by two phenomena: drift and diffusion. Provided available states exist in the conduction and valence bands, the electric field within the semiconductor exerts a force on electrons such that there is net electron and hole acceleration and motion. The net movement of charge carriers due to an electric field is called drift. In the presence of an electric field, carrier velocity in a semiconductor material will vary: velocity will increase due to the force from the electric field, but will also decrease when energy is lost due to collisions with ionized impurity atoms and thermally-vibrating lattice atoms [21]. Thus an average drift velocity is defined which is directly proportional to the electric field for electrons and holes:

$$v_{drift,n} = -\mu_n E,\ v_{drift,p} = \mu_p E \tag{2.8}$$

where $\mu_{n,p}$ is the electron and hole mobility, a material-dependent constant proportionality factor that describes how well a charge carrier will move in an electric field. Given the volume charge density of charge carriers,

$$J_{drift,n} = -qnv_{drift,n},\ J_{drift,p} = qpv_{drift,p} \tag{2.9}$$

for electrons and holes respectively, the drift current for electrons and holes is given by:

$$J_{drift} = q\left(\mu_n n + \mu_p p\right) E \tag{2.10}$$

Diffusion occurs when excess particles dissipate into available space through random thermal velocity. In solar cells, given the p-n junction and resultant concentration gradient, carriers will diffuse to regions of lesser concentration until concentration equilibrium is reached. The diffusion current density is given by:

$$J_{Diff,n} = qD_n\nabla n,\ J_{Diff,p} = qD_p\nabla p \tag{2.11}$$

for electrons and holes respectively. $D_{n,p}$ is the diffusion coefficient and $\nabla n, p$ the three-dimensional concentration gradient for electrons and holes. Diffusion and drift processes are related through the diffusion coefficients and carrier mobilities which are coupled by the Einstein relations [21]:

$$D_n = \frac{kT}{q}\mu_n,\ D_p = \frac{kT}{q}\mu_p \tag{2.12}$$

The net diode current, $J = J_n + J_p$, is a combination of drift and diffusion currents, and the relative component contributions are location-dependent. In the SCR the electric field strength is greatest, as is the concentration gradient. Although drift effects tend to be more dominant near the junction in CdTe devices, in the SCR both drift and diffusion contribute to the diode current. In the QNRs, the electric field strength is much smaller such that diffusion dominates the diode current [21, 22].

Thermionic emission and tunneling may also contribute to current flow if a band offset occurs at a heterojunction interface. In the case of thermionic emission, electrons are transported over the energy barrier, and in tunneling, due to quantum effects, electrons can penetrate the barrier. Generally thermionic emission reduces device performance and tunneling can be purposefully pursued in certain device structures [22].

Recombination is the process by which electrons and holes annihilate, or recombine given non-equilibrium conditions. Multiple recombination mechanisms exist: radiative recombination, Auger recombination, recombination through traps, and recombination at surfaces. Radiative recombination, described simply, is the reverse process of absorption. An electron in a higher energy state as compared to its equilibrium state energy transitions to a lower energy state and emits light with energy that corresponds to most or all of the energy-state differential. Radiative recombination will occur more rapidly in direct semiconductors than indirect semiconductors because the latter requires a phonon-involved two-step process. The radiative recombination rate is given by

$$R_R = Bpn \tag{2.13}$$

and is directly proportional to the product of the concentration of hole-occupied valence-band states and concentration of electron-occupied conduction-band states. B is the proportionality constant which is material-dependent, and can be calculated from the semiconductor's absorption coefficient [21, 27].

Characteristic lifetimes are also used to describe recombination processes and are related to recombination rates by

$$\tau_n = \frac{\Delta n}{U},\ \tau_p = \frac{\Delta p}{U} \tag{2.14}$$

for electrons and holes respectively, where U is the net recombination rate and Δn and Δp are the carrier concentration differences from equilibrium for electrons and holes respectively.

Auger recombination is the process by which the excess energy from electron-hole recombination is given to a second electron which relaxes back to its original energy by emitting phonons. It is not particularly effective in CdTe due to its somewhat low doping, and is described in more detail in [21].

Given allowed energy states within the band gap due to defects and impurities, the two-step Schockley-Read-Hall recombination process can occur. There are four basic processes in this recombination classification. First is an electron which relaxes from the conduction band to an initially neutral trap state. Second is its inverse: an electron initially occupying a trap state is emitted to the conduction band. Third, an electron occupying a trap state can relax into the valence band (or a hole from the valence band is captured by a trap state), and fourth, its inverse, an electron from the valence band is captured by a trap state (or a hole occupying a neutral trap state relaxes to the valence band). The dynamics of this recombination mechanism are detailed in [21, 22, 28, 29].

Recombination also occurs efficiently at surfaces due to the crystal-structure defects and the multitude of allowed states in the band gap that they cause. These surface states can

occur at energies throughout the band gap but those lying near midgap are the most effective recombination centers. The net recombination rate per unit area is given by [21]

$$U_S = \frac{S_{n0} S_{p0} \left(np - n_i^2\right)}{S_{n0} \left(n + n_1\right) + S_{p0} \left(p + n_p\right)} \tag{2.15}$$

where S_{n0} and S_{p0} are electron and hole surface recombination velocities. Generally, $S = N\sigma v_{th}$ where N is the area density of the defect states, σ is the charge carrier capture cross section, and v_{th} is thermal velocity. Defect-mediated recombination, through SCR, QNR, or interface recombination is the dominant recombination process in CdTe devices that significantly reduces performance [30, 31].

As previously stated, these recombination processes occur concurrently such that their recombination rates are additive, or represented more typically, the inverse lifetimes are additive:

$$\frac{1}{\tau} = \frac{1}{\tau_R} + \frac{1}{\tau_A} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_S} \tag{2.16}$$

The diffusion length, the average length a charge carrier moves between generation and recombination is related to the lifetime by

$$L_D = \left(D\tau\right)^{1/2} \tag{2.17}$$

By establishing electrical contacts on each side of the p-type and n-type materials and applying a voltage bias, V, current will flow dependent on the applied bias. Without bias no net current flows because the recombination of electrons and holes is equal. In reverse bias there is also no net current flow because the Fermi level in the n-type region is lower than that in the p-type region which increases the potential barrier $(V_{bi} + V)$ as compared to its unbiased level, V_{bi}. Under forward bias, the Fermi level in the p-type region is lower than that in the n-type region which reduces the potential barrier $(V_{bi} - V)$ such that the depletion region narrows, the electric field strength decreases, and charge carriers are able to diffuse and current can flow [22]. This voltage-dependent current density is described by the diode equation:

$$J_d(V) = J_0 \left[exp\left(\frac{qV}{AkT}\right) - 1 \right] \tag{2.18}$$

where A is the diode quality factor which is related to the dominant recombination process. For large forward bias, $A \approx 1$ when diffusion dominates (and recombination takes place in the QNR through defect or surface states) and for low forward bias $A \approx 2$ when recombination dominates and takes place in the SCR. And there is a transition region where $1 < A < 2$ [11, 22]. J_0 is the saturation current density given by [22, 32]

$$J_0 = \left[\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n} \right] = J_{00} exp\left(-\frac{E_a}{AkT}\right) \tag{2.19}$$

where E_a is the activation energy which is associated with interface recombination; if its energy is near that of the absorber band gap, bulk recombination is the primary recombination mechanism, and for energies not close to the band gap, interfacial recombination dominates due to interface defects [33]. J_{00} is a weakly temperature-dependent prefactor of J_0. A quantitative, mathematically derived outline of the p-n junction current-voltage relationship is given in [22].

When the solar cell is illuminated, photons with sufficient energy ($E \geq E_g$) will excite electrons from the valence band to conduction band and create a non-equilibrium state such that the charge carriers have their own respective quasi-Fermi levels. Under ideal operation, the charge carriers will be separated by the internal field and flow to opposite electrical contacts and recombine in the external circuit for current collection. That collection of the photogenerated carriers is in opposition of the diode current such that the total current is $J(V) = J_d(V) - J_L(V)$.

In realistic solar cells, especially thin-film solar cells, the current-voltage (J-V) behavior does not act as an ideal diode in a circuit; the solar cell is subject to parasitic losses such that the total current density of an illuminated device is given by

$$J_d(V) = J_0 exp\left[\frac{q}{AkT}(V - RJ)\right] + GV - J_L \tag{2.20}$$

for the case of constant J_L. R corresponds to series resistance and G shunt conductance, and are lumped circuit-model representations of losses which occur in parallel and series with the diode respectively [32].

2.4 Device Characterization

Since photovoltaic devices can be structurally, materially, optically, and electrically complex, a multitude of measurements are used to characterize specific properties of the solar cell, typically with the goal of advancing understanding to improve efficiency. This section describes device characterization techniques implemented in this work, and is by no means a comprehensive account of all characterization techniques; many additional valuable techniques are described in detail elsewhere [11, 28].

2.4.1 Current Density vs. Voltage

Diode behavior and encompassed parasitic losses are measured by placing a photovoltaic device in an external circuit and measuring current as a function of applied voltage bias in dark and illuminated conditions. This is one of the most fundamental PV measurements, referred to as the current-voltage (J-V) measurement, because the resulting diode data can be analyzed simply, with current normalized to device area, such that four fundamental parameters are extracted: open circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor, and conversion efficiency. An example of measured dark and illuminated J-V data from a CdTe-based solar cell is given in Fig. 2.3 with the parameters indicated.

The measured V_{OC} corresponds to the voltage at which the net current flow is zero. Recombination is the fundamental process which limits the V_{OC} of a photovoltaic device such that measured V_{OC} is less than the band gap-dependent ideal V_{OC}. The measured J_{SC} is the total current density collected from an illuminated device at short circuit and is also less than the band gap-dependent ideal J_{SC} due to photon conversion losses. For a well-behaved device, J_L is voltage-independent and equal to J_{SC}. Fill factor is the ratio of the

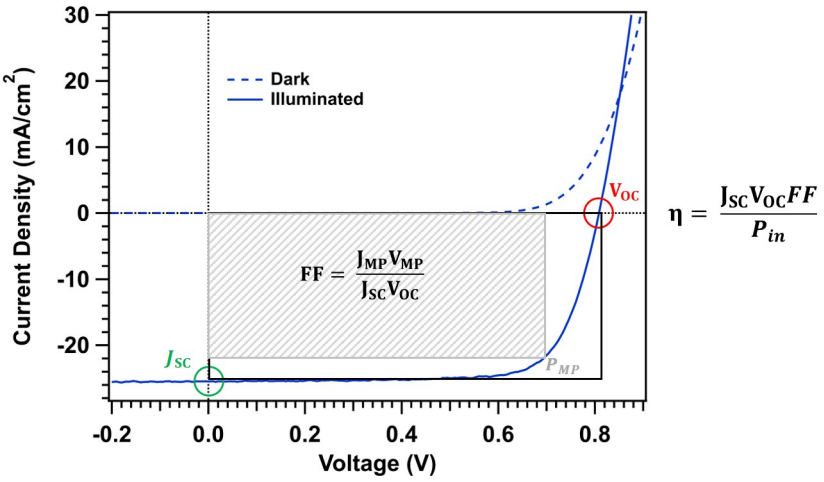

Figure 2.3: Example J-V curves measured under dark and illuminated conditions. The V_{OC}, J_{SC}, and maximum power point (P_{MP}) locations are given, fill factor and efficiency equations are shown, and regions which determine fill factor are indicated.

maximum power point (P_{MP}) to the product of V_{OC} and J_{SC}, and is visually represented as the ratio of the gray shaded rectangle to black outlined rectangle in Fig. 2.3. Given its dependence on V_{OC} and J_{SC}, ideal fill factor is also band-gap dependent. Conversion efficiency is determined by the ratio of output power to input power. The input power is 100 mW/cm^2, a standardized power which corresponds to the AM 1.5G radiation intensity. The output power is given by the product of V_{OC}, J_{SC}, and fill factor. The ideal J-V parameters, their band gap dependence, and their loss contributors in non-ideal devices are discussed in Chapters 3 and 4. J-V measurements are typically performed at standard test conditions (25 °C, AM 1.5G spectrum, 100 mW/cm^2 illumination, and four-point probed), but can also be measured with varied illumination and/or temperature to investigate additional device characteristics [32].

For J-V measurements in this work, devices were measured in a homemade light-tight enclosure at standard test conditions where illumination was provided by a xenon arc lamp solar simulator with intensity adjusted to a certified GaAs solar cell. A Keithly sourcemeter was used for the applied bias voltages in dark and light measurements.

2.4.2 Quantum Efficiency

A spectrally-resolved method to determine a solar cell's J_{SC} and current density loss mechanisms is carried out by the measurement of external quantum efficiency (QE) as a function of wavelength. QE is defined as the ratio of the number of electrons collected per photon incident on the solar cell at each wavelength. And J_{SC} is the integral over wavelength of the product of the measured QE, incident spectral photon flux density, and fundamental charge, explicitly given by

$$J_{SC} = q \int_0^\infty (QE) N_{ph}(\lambda) d\lambda \tag{2.21}$$

$N_{ph}(\lambda) = \lambda P(\lambda)/hc$ is the spectral photon flux density, dependent on the solar spectral irradiance density, $P(\lambda)$, and h is Planck's constant and c the speed of light.

Given the multi-layer structure of solar cells, especially in thin-film technologies, changes in QE as a function of wavelength or energy can be analyzed to understand the role of different layers in current collection or loss. For example, at short wavelengths (high energies), incident photons are absorbed in front layers of the cell such that shifts in QE in those regions are indicative of current-related changes in the front-side layers. At photon energies below the absorber band gap, the energy is not sufficient to excite electrons to the conduction band, therefore QE data demonstrate a fairly sharp decrease at the band-gap wavelength. An example of this is given in Fig. 2.4 where the shift in absorption edge at long wavelengths of two devices indicates a difference in band gap. Band gap is determined as the energy at which $|dQE/d\lambda|$ is maximized.

QE can be paired with additional optical measurements as a function of wavelength such as reflection, transmission, and absorption to determine current loss mechanisms present in the solar cell. The categorization and quantification of current losses and collection are detailed in Chapter 3.

Details of the CSU QE system setup are given in [34].

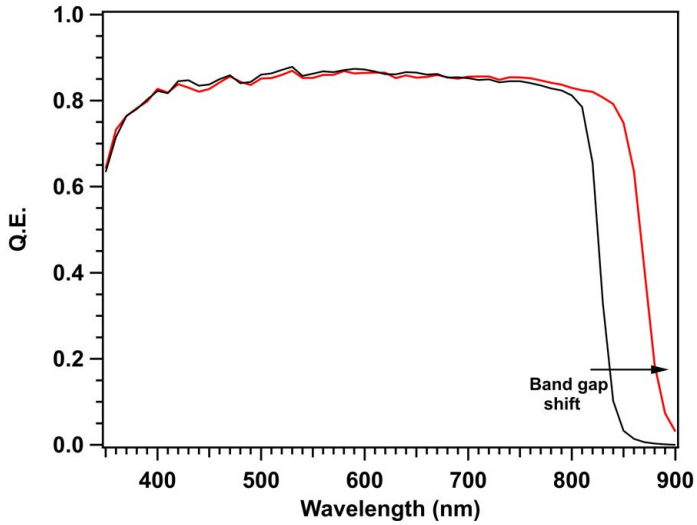

Figure 2.4: Example QE data of two CdTe-based devices with different band gaps. The band gap shift is indicated at the absorption edges.

2.4.3 Capacitance Measurements

Capacitance measurements use an applied AC voltage to induce an AC current response from the solar cell which can provide information on free carrier densities, depletion widths, potential barriers, and deep trap densities [11, 32]. One such measurement, capacitance-voltage (C-V), is the capacitance technique employed in this work. To analyze the capacitance data as a function of applied voltage, the depletion approximation is made where the depletion region is defined with abrupt edges and contains no free carriers. A change in applied voltage will cause a change in stored charge at the depletion edges [11, 21], therefore a parallel plate capacitor model is applied:

$$C = \epsilon A/W \tag{2.22}$$

where W is the width of the depletion region, A is device area, and ϵ is the dielectric constant of the semiconductor material [14]. For a diode with one side of the junction which is heavily doped,

$$W = \left[\frac{2\epsilon\left(V_D - V\right)}{qN(W)}\right]^{1/2} \tag{2.23}$$

such that

$$C^2 = \frac{q\epsilon A^2 N(W)}{2\left(V_D - V\right)} \tag{2.24}$$

where N(W) is the doping concentration on the lightly-doped side of the junction, V_D is the diffusion potential, and V is the applied voltage [11, 21, 32]. V_D is different from the built-in potential (V_{bi}) by the Fermi energy: $qV_{bi} = E_F + qV_D$. In crystalline silicon (c-Si), $V_{bi} \approx V_D$ since $E_F \sim kT$, but in thin-film solar cells the difference between these two values is larger such that V_D is more appropriate [32].

Since V_D is not generally known, the discrete derivative is taken and Eq. 2.24 can be solved for N(W), the position-dependent hole density in the case of a p-type CdTe absorber device:

$$N(W) = \frac{C^3}{q\epsilon A^2}\frac{\Delta V}{\Delta C} \tag{2.25}$$

Interpretation of capacitance-voltage data must be approached conservatively for thin-film solar cells because of their significant densities of deep states. Ideally, a linear fit can be applied to Eq. 2.24, such that the intercept and slope yield V_{bi} and N(W), typically applicable to c-Si solar cells. In thin-film devices like CdTe, C^{-2} vs. V data do not result in a straight line, therefore comparative changes in the shape of these Mott-Schottky plots between different devices rather than absolute fits are used to suggest changes in depletion and carrier density. Similarly, carrier density as a function of depletion width will not provide an absolute value for carrier densities at different positions within the absorber. Instead, estimated values for the carrier density are reported based on the carrier density at the minimum of the U-shaped carrier profile or at zero bias voltage.

Finally, C-V measurements are preceded by capacitance-frequency (C-F) measurements where capacitance is measured as the frequency of the AC bias is varied for different voltage

set points. This is done to select a frequency for C-V measurements such that the free carrier relaxation time is short compared to the applied frequency. This avoids deep-level trap state contributions (low frequencies), and instrument-induced series resistance, stray inductance, and imprecision (high frequencies) [11,32,35]. The frequency is selected based on unchanged capacitance at and surrounding that frequency for each applied voltage and is typically 100 kHz. A low-frequency impedance analyzer is used in the measurement such that phase angle as a function of frequency is also measured, and reliable separation of capacitance and conductance can be verified at the chosen frequency (corresponding to an admittance phase angle of 90°). A detailed description of the capacitance measurement setup at CSU is provided by R. Geisthardt [34].

2.4.4 Electroluminescence

Electroluminescence (EL) is the emission of light from a diode due to an applied forward voltage bias. For EL measurement of solar cells, it is the reciprocal action of the standard solar cell operation. Although most PV devices aren't efficient light-emitters, given an applied voltage and electrically-excited charge carriers, part of the recombination will be radiative such that with proper sensitive detection and background measurement, the radiated photons are detectable [11]. The EL measurement system used in this work was designed, built, and employed for in-depth solar cell and module characterization by J. Raguse, and a comprehensive description of the measurement system can be found in [36]. Measurements are made in a large black-box enclosure to minimize background light, and the solar cell is electrically biased with a DC power supply, and current is measured by a digital multimeter. For the devices measured in this work, bias was applied such that the current density was 20 mA/cm^2, comparable to J_{SC}. EL signal was imaged with an Apogee Alta 8300 camera with 50-mm macro lens, extension tubing, and Si CCD detector, chosen for detection of the radiated photon energies near the CdTe band gap. The CCD is cooled to -25 °C to reduce dark noise. EL images were processed with ImageJ software: background was subtracted and data were normalized to the 20 mA/cm^2 current density and 100-second camera exposure time.

The spatial data are plotted on a logarithmic z-scale since the logarithm of EL intensity was shown to be proportional to PV device voltage deficit, i.e. the voltage differential between ideal and measured V_{OC} [36, 37].

2.4.5 Photoluminescence Emission Spectroscopy

The spectra produced by the emission of photons from photon-induced excitation can be measured on completed PV devices or films to detect and identify energy transitions, commonly from impurities. In the photoluminescence emission spectroscopy (PL) measurement photons of sufficient energy incident on the device or material will excite charge carriers. Recombination through radiative emission is detected and the radiative emission intensity is proportional to the impurity density [28]. Different energy transitions may occur in a PL measurement, and are dependent on measurement conditions such as excitation injection power and energy, device temperature, applied bias, and material properties. PL data presented were measured at room temperature where the probability of band-to-band (conduction band minimum to valence band maximum) transitions is very likely because the bands are sufficiently populated by photoexcited carriers [11, 28]. Additional radiative transitions such as conduction band-to-acceptor-state, donor state-to-valence band, and acceptor state-to-donor state may also occur. Given proper calibration and knowledge of a device's absorption profile, drift, diffusion, recombination, and emitted photon propagation through the sample, the shape of the measured PL spectra can be used to determine PL yield, PL efficiency ($\eta_{PL} = \tau_{tot}/\tau_{rad}$ where τ_{tot} and τ_{rad} correspond to the total and radiative lifetimes respectively), and recombination mechanisms [11].

In this work, all of these parameters are not precisely known, therefore qualitative interpretations of PL data are made based on changes in PL spectra given purposeful variation in film or device structure. Because the measurement probe depth, given by the inverse of the semiconductor absorption coefficient ($\alpha(\lambda)^{-1}$) at the excitation wavelength of 520-nm, is known to be approximately 125 nm or greater given carrier diffusion, the front-side PL measurement is sensitive primarily to recombination in the bulk or near the front interface,

and only in some cases towards the back of the device. Thus PL data are used to estimate absorber band gap and the cumulative role of radiative recombination in the devices. PL measurements in this work were conducted in a light-tight enclosure and utilized a 520-nm excitation diode laser at 15 mW focused to a spot size of $\sim$1 mm^2. Device or material photoluminescence passed through a 570-nm long pass filter to eliminate excitation signal and was focused through a focusing lens into an Ocean Optics spectrometer.

2.4.6 Time-Resolved Photoluminescence

Charge carrier dynamics can be monitored and characterized by time-resolved photoluminescence measurements (TRPL). A short pulse of incident photons with energy greater than the absorber band gap generates excess carriers and the time dependence of light emitted by the recombining electrons and holes is used to monitor excess carrier density [28]. TRPL intensity data demonstrate a decay over time corresponding to the carrier dynamics, and analysis of this decay curve can provide information on the average lifetime of the measured film structure or device. As discussed in section 2.3, contributions to the overall lifetime can come from several recombination mechanisms which, paired with complex film or device structures, can make interpretation and attribution of TRPL trends to specific recombination mechanisms complicated, especially in thin-film devices such as CdTe. Analysis can be somewhat simplified given certain structural constraints, for example, well-passivated samples such as double heterostructures to determine bulk material properties, or polycrystalline films without p-n junctions [38]. Additionally, intelligent experimental and measurement design (such as structure and material-specific changes, wavelength-dependent measurements, voltage bias-dependent measurements, excitation direction, and single or two-photon measurement) paired with modeling can be used to try to determine material properties [39–43]. Relative changes in TRPL decays were considered in this work to understand general changes in recombination rates in devices with intentional structural differences.

Single-photon TRPL was measured at the National Renewable Energy Laboratory (NREL) using a 640-nm excitation laser generated by a femtosecond optical parametric amplifier, focused to a beam diameter of 0.3 mm. The repetition rate was 1.1 MHz and TRPL emission was measured using different band pass filters dependent on the absorber band gap. The minimum lifetime which can be measured is ∼0.3 ns due to inherent equipment delay.

2.5 Material Characterization

2.5.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is an imaging technique performed on surface or cross-section bulk samples to glean information about film layer thicknesses, surface topographies, and grain structure and sizes, with sample-dependent resolution down to or below 1 nm. For secondary electron SEM imaging, a magnified image is produced by scanning a sample with a focused electron beam and detecting the secondary electrons emitted. The system consists of a primary electron gun, a system of lenses, scanning coils, an electron collector, and a cathode ray display tube (CRT). The SEM image is produced by movement of the primary electron beam across the sample, and at each location electrons are emitted, amplified, detected, and displayed on a CRT screen, and that information is mapped from specimen-space to CRT-space [11, 28]. Magnification results from this mapping process according to the ratio of the dimension scanned on the CRT to dimension of the scanned sample. Image contrast is influenced by sample topography, surface conditions, and the local electric field. The electron beam energy is typically 10-30 keV, controlled by the accelerating voltage, and its value determines the penetration depth, or electron range, into the material. Secondary electrons are typically emitted from approximately the top 10 nm of the sample surface, although this may be varied by tilting the sample stage from normal incidence. The electron-beam current changes the electron injection rate into the sample [11, 28].

SEM imaging presented in this work was measured with a JEOL JSM-6500F field emission scanning electron microscope. Samples were cleaved and gold-coated to reduce charging

during measurement. The working distance was 10 mm, and the electron-beam voltage (10-15 kV) and magnification were varied dependent on sample properties and features of interest.

2.5.2 Transmission Electron Microscopy

Transmission electron microscopy (TEM), like SEM, is an electron-beam induced imaging technique. It is different from SEM in that transmitted electrons rather than secondary electrons are mapped and imaged, and greater resolutions (to 0.15 nm) can be achieved given the higher (typically 100-400 kV) accelerating voltage, thin samples (such that the electron beam has reduced spread within the sample), and different instrumentation setup. Given the necessity for electron transmission, samples must be sufficiently thin (a few tens to hundred nanometers) to be imaged. Transmitted and forward scattered electrons form a magnified image in the image plane and a diffraction pattern on the back focal plane, and utilization of different lenses allows for image or diffraction viewing, the latter of which allows for structural information to be obtained. Bright-field images are formed using transmitted electrons and dark-field images are formed using a specific diffracted beam. The image brightness is determined by the intensity of electrons transmitted through the sample that pass through the image forming lenses. This is influenced by atomic number, Z: electrons which interact with larger Z atoms are more strongly scattered and thus not transmitted, whereas the electrons weakly scattered by lower Z atoms are transmitted. This results in atomic-number based imaging contrast such that low Z elements appear bright and higher-Z atomic elements appear bark in bright-field imaging, and vice versa for dark-field imaging [28].

Scanning transmission electron microscopy (STEM) is slightly different from TEM in that the stationary, parallel, coherent electron beam whose sample transmission is projected onto a fluorescent screen in TEM is replaced by a fine beam which is raster-scanned across the sample. In this case the objective lens recombines the location-varied transmitted electrons to a fixed region in the back focal plane where they are detected by an electron detector.

The STEM-imaged samples were prepared by focused-ion-beam milling and in-situ lift-off at Loughborough University and the Colorado School of Mines (CSM) for images in Chapters 3 and 4 respectively [11]. At Loughborough University STEM imaging was performed with an FEI Tecnai F20, and CSM-prepared samples were imaged at CSU with a JEOL JEM-2100F.

2.5.3 Energy-Dispersive X-ray Spectroscopy

In this work, SEM and STEM imaging were often accompanied by energy-dispersive X-ray spectroscopy (EDX) measurements. In EDX, all emitted X-rays from a sample are recorded by an energy-dispersive spectrometer and the chemical composition can be analyzed. Electron impingement on a sample can scatter an inner-shell electron from a sample atom with reoccupation of the inner state by an electron from an elevated state. The potential energy differential between the two states can be transferred to a bound electron which can be emitted as an X-ray quanta, and the energy is characteristic of a specific element. The X-ray quanta generate charge pulses in a field-effect transistor that are processed and binned according to energy such that a final energy (and thus element)-dependent spectra is produced. EDX compositional analysis can be performed at a specific point, within a specified region (EDX mapping), or across a specified line (EDX line scans). The detectable energy range is somewhat limited at low energies: given a system with a Be window, elements with $Z \geq 11$ are detectable, and for a windowless systems, $Z \geq 6$ is detectable [11, 28]. In SEM, EDX map resolution as low as 100 nm can be achieved for reduced accelerating voltages of 5-7 keV, although the resolution is also dependent on the X-ray quanta of interest: those with a shorter mean free path will have greater resolution. In TEM, spatial resolution below 1 nm can be achieved, although counting statistics are reduced due to the thin sample and resultant low count rates.

2.5.4 Time-of-Flight Secondary Ion Mass Spectrometry

Time-of-flight secondary ion mass spectrometry (TOF-SIMS) is a destructive characterization technique which provides elemental depth data through sample depth sputtering

and mass analysis of detected ions. In this measurement, the incident ion beam consists of pulsed ions from an ion gun with pulse widths on the order of nanoseconds such that the ionized species are sputtered from the surface and the time it takes for the ions to travel to the detector is measured. The ionized species travel to the detector under the influence of a secondary-ion accelerating field, and the kinetic energy is determinable from the elapsed time between sample ejection and detection. The ionized species' mass is determined from the kinetic energy (KE=$1/2mv^2$) such that mass/charge ratios of detected ions can be analyzed and elemental data can be collected as a function of sputter depth. In TOF-SIMS the analysis beam must be pulsed very rapidly to precisely determine the time at which an ionized species is emitted from the sample. Therefore a secondary ion beam is applied for sputtering [11, 28].

TOF-SIMS was measured at CSM using a thermal ionization Cesium sputtering source with a 70 µs cycle time operated in positive mode to look at electro-positive and electro-negative species. The primary ion beam was a 30-keV, three-lens BiMn cluster ion gun. In mass identification, most masses were cluster ions, element-bonded to Cs+ masses, but single elements are presented in plots and discussions for clarity. Unless otherwise indicated, the most abundant isotope of elements were analyzed. Due to the absence of implant standards for the system, SIMS profiles are plotted as intensity as a function of sputtering depth.

2.5.5 Glancing-Angle X-Ray Diffraction

When X-rays interact with a crystalline material, coherent elastic scattering, or diffraction may occur. The scattering of X-rays from a group of hkl lattice planes can be considered as the reflection from a series of parallel planes in the crystal separated by a lattice plane distance d_{hkl}. For two parallel rays incident on adjacent planes at an angle, the reflected rays will be in phase (and demonstrate maximum intensity) if the differences in path length between incident and outgoing rays is an integer multiple of the X-ray wavelength. More commonly presented mathematically as Bragg's Law, $n\lambda = 2d_{hkl}sin\theta$, detection of these intensities as a function of angle between an X-ray beam and sample can provide information

about crystalline structure and crystal defects in films. Glancing-angle X-ray diffraction (GAXRD) is an asymmetric scan where the path length of the X-rays in the film is increased by using a fixed angle of incidence, α, for incident X-rays. GAXRD is advantageous for thin-film structures because due to the small α value ($\alpha < 3°$), diffraction data from a top material layer can be measured without interference from deeper layers or the substrate. The measurement is performed at a constant angle of incidence and the detector moves over a 2θ range of interest [11].

GAXRD data discussed in Chapter 4 were measured at CSU using a Bruker D8 Series II Thin Film Diffractometer (D8TF) and Cu K-α X-ray source with K-α2 stripped such that λ = 1.5406 Å. A 0.6-mm exit slit was used to maintain a good balance between resolution and counts, and data were collected for 2θ = 20-80° with 0.02 increment steps and scan speed = 1 second/step. An Al XRD flat plate intensity standard with known 2θ =35.14° peak was also measured to determine if an offset angle application to the data was necessary. GAXRD data discussed in Chapter 5 were measured at CSM using a Empyrean XRD system with a Cu K-α X-ray source. hkl peaks were identified with the XRD PDF database provided by the International Centre for Diffraction Data.

2.5.6 X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface science technique which utilizes X-rays to ionize atoms and analyzes the kinetic energy of ejected photoelectrons. It is based on the photoelectron effect, which relates the energy of an incident excitation photon to the kinetic energy of the emitted photoelectron and the binding energy of the electrons in the atom referenced to the vacuum level. In sample measurement, when the incident X-rays interact with the material and the photoelectrons are ejected, a core-level vacancy is left in the material. The vacancy becomes occupied by a higher energy-level electron, and the corresponding de-excitation occurs by emission of Auger electrons or X-ray fluorescence. XPS spectra are therefore the detected intensity of Auger electrons and X-ray fluorescence

over a range of binding energies. XPS measurements are performed under high or ultra-high vacuum mostly to prevent signal attenuation through emitted photoelectron and gas molecule collisions. Due to the short path length that a photoelectron can travel before it is subjected to inelastic scattering, XPS spectra are generated from the outermost ten nanometers or less of the film surface. The analysis depth can be extended by cycling ion bombardment and analysis such that etch-depth profiles through the sample structures can be measured [11].

In thin-film solar cells, XPS is commonly used to analyze surface chemistry, layer compositions, and compositional gradients in materials or film structures. In this work, core levels and binding energies of specific structures and elements were analyzed to determine valence-band offsets between thin-film materials. Measurements were made with a Physical Electronics 5800 system, and additional measurement and analysis details are described in section 5.5.

2.6 Device Fabrication

The presented CdTe-based thin-film PV devices are fabricated in a superstrate configuration in which devices are made on a transparent substrate and light enters the absorber through the first deposited layers. The substrate which serves as the foundation for thin-film depositions is a commercially-made SnO_2:F transparent conducting oxide (TCO) layer deposited on 3.1" x 3.6" soda lime glass (Tec10 made by Pilkington). The TCO is an n-type semiconductor with a fairly low sheet resistance of 10-12 $\Omega/\square$ such that it is favorable as a transparent front contact in the superstrate configuration. Before film deposition, the Tec10 glass undergoes a thorough cleaning process to clear grease or particulate residue from the commercial process [44].

A thin magnesium-zinc oxide (MgZnO) layer serves as the n-type emitter semiconductor layer in the p-n junction formation. MgZnO was chosen for this layer because its $\sim$3.5-eV band gap is wide enough that incident photon absorption in the MgZnO layer is minimal, leading to increased current collection. The MgZnO also has a positive, spike conduction

band offset with CdTe (∼0.2 eV) which reduces interface recombination and improves device performance [45]. A 100-nm MgZnO layer is RF-sputter deposited onto the Tec10 substrate from a $(MgO)_{11}(ZnO)_{89}$ by percent weight target.

The absorber materials and subsequent passivation treatments are carried out in a single in-line automated vacuum deposition system with multiple CSS sources [46]. Bottom and top source temperature differentials are employed with the substrate located between the sources such that material sublimates upwards from the bottom source onto the substrate. A schematic of the CSS system is given in Fig. 2.5. Before material sublimation, substrate temperatures are elevated in a preheat source immediately preceding absorber deposition for improved thermal uniformity and film growth. Substrate temperatures are monitored in-situ by a pyrometer and controlled by dwell time in the preheat source. In standard CdTe devices, the p-type polycrystalline CdTe layer is CSS-deposited onto the MgZnO, and film thickness is typically controlled by sublimation time. The CdTe is subsequently passivated by a $CdCl_2$ treatment which consists of deposition of $CdCl_2$ material and an anneal. This treatment is necessary for good CdTe device performance: it promotes CdTe grain recrystallization, grain coalescence, passivation of dangling bonds, and improved bulk properties [14, 47–51]. After the substrate is removed from the CSS deposition system $CdCl_2$ residue is rinsed from the film surface with deionized water.

Cu-doping of the passivated CdTe absorber is performed in a separate CSS vacuum system. The Cu treatment consists of a CuCl deposition followed by anneal and is done to improve the doping of bulk CdTe and the back of the device. After Cu-treatment, the atomic concentration in CSU bulk CdTe is 10^{17}-10^{18} cm^{-3} although the CdTe carrier concentration is typically in the 10^{14} cm^{-3} range. This has been attributed to self-compensation with interstitial Cu (Cu_i), a shallow donor [52–54]. Cu has historically been used as the CdTe dopant but due to carrier concentration limitations and stability issues, new group V dopants such as arsenic are being explored [24–26]..

A 40-nm Te buffer layer is deposited by evaporation at room temperature after the Cu doping treatment. Because the work functions of metals are not great enough for ohmic

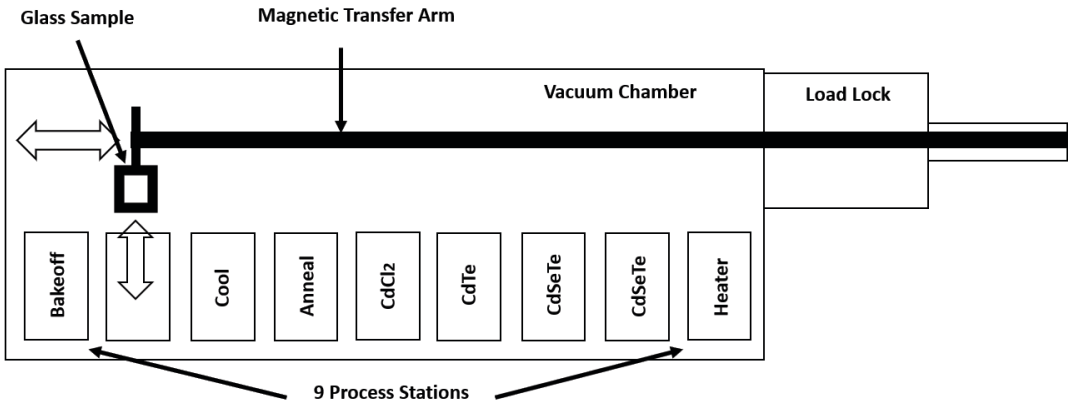

Figure 2.5: Schematic of the main CSS in-line, automated vacuum deposition system. Each source function is indicated, and the glass substrate is moved between sources with an automated magnetic transfer arm.

contact with CdTe given its 4.3-eV electron affinity and 1.5-eV band gap, making a low resistance ohmic contact with CdTe is challenging, and typical contacting metals such as Ni or Au form a Schottky barrier which can reduce performance through increased forward electron current and decreased photogenerated hole current. Incorporation of the thin Te buffer layer at the back acts as a back-valence-band-offset mitigating layer which reduces some of the band-alignment-induced problems and improves device performance [55].

The film structure is completed with spray application of a conductive Ni paint which serves as the back-electrode contact. To convert the film stack into electrically contactable devices the thin-film structure is delineated such that the front-side TCO and Ni back contact are electrically accessible. Twenty-five small area ($\sim$0.65 cm^2) devices are made on each substrate through the application of pressurized glass-bead media through a substrate mask. Indium solder is applied in a grid pattern between devices to improve contact to the front TCO and minimize lateral resistance during electrical measurements.

The structure of a standard CdTe device is shown in Fig. 2.6, and changes to this structure will be presented throughout this work. For a more detailed description of the CdTe-based device fabrication process at CSU, see [44].

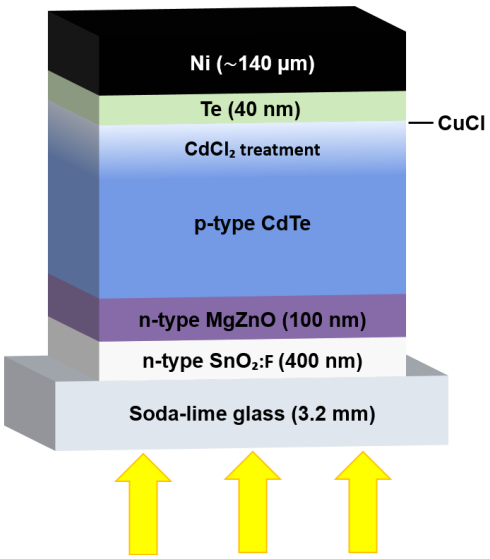

Figure 2.6: Basic CdTe thin-film device structure with incident light direction indicated. Not to scale.

Chapter 3

ANALYSIS OF OPTIMIZED THIN CdTe ABSORBER STRUCTURES

High-performing CdTe devices have historically utilized CdTe absorber layer thicknesses between 3 and 10 µm [19, 56–58], however, there are several potential advantages of maintaining performance with thinner CdTe absorbers. The most obvious benefits from a manufacturing perspective are the material, time, and consequently, cost savings associated with thinner CdTe deposition. Thinner CdTe absorbers also unlock opportunities for bifacial and semi-transparent solar cell development [16, 17, 59]. CdTe devices with 0.2-2 µm absorbers deposited by sputtering, close space sublimation (CSS), vapor transport deposition (VTD), and metalorganic chemical vapor transport (MOCVD), on a CdS emitter layer have demonstrated respectable device efficiencies, proving the fabrication diversity and performance capability of thin-CdTe devices [60–68]. One of the greatest impacts of thinning the CdTe absorber layer is the potential to minimize the voltage deficit in CdTe devices. This requires the incorporation of an electron-reflector layer (discussed in detail in Chapter 5), which relies on a fully-depleted absorber, attainable for CdTe thicknesses below 2 µm [55, 64, 69–71]. To take advantage of the potential benefits of thin CdTe absorbers, the thin CdTe structure must be optimized and analyzed for best performance; this chapter outlines fabrication-based optimization experiments and film and device analyses, used to establish a thin CdTe baseline structure for continued development of next generation CdTe-based devices.

3.1 Fabrication Optimization of Thin CdTe Structures

Thin CdTe absorber layers were fabricated on conductive Tec10 substrates coated with the 100-nm sputtered MgZnO emitter layer described in Chapter 2. CdTe thicknesses of 0.6-1.2 µm were chosen for fabrication optimization experiments to satisfy fully-depleted absorber requirements where the thickness was controlled by varying the CdTe deposition

time, i.e. the exposure time of the substrate to the sublimating CdTe material in the CSS system. The deposition rate of 19 ± 1 nm/sec remained fairly constant for the CdTe thickness range. Post-deposition $CdCl_2$ passivation and Cu doping treatments, described in Chapter 2, are highly dependent on CdTe absorber thickness, therefore optimization of each of these treatments on thin absorbers is necessary. The optimization structure, given in Fig. 3.1, was completed into devices as described in Chapter 2.

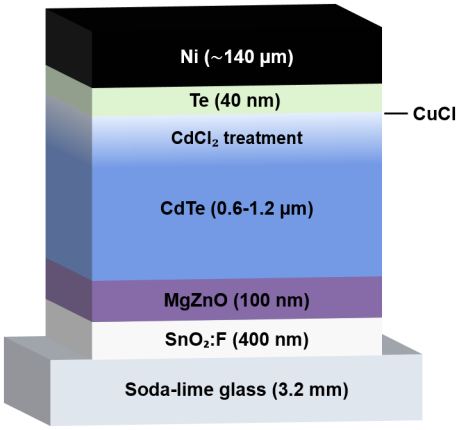

Figure 3.1: Device structure for thin CdTe fabrication optimization.

3.1.1 $CdCl_2$ Passivation

$CdCl_2$ passivation optimization experiments, described fully in [72, 73], focused on the $CdCl_2$ dose and anneal times. The $CdCl_2$ dose time window of 38-180 seconds encompassed times well below and well above a hypothesized optimal dose time of 120 seconds, based on $CdCl_2$ passivation conditions for thicker samples [56]. Fig. 3.2 shows the effects of varied $CdCl_2$ dose time on J-V parameters for the best-performing devices at each of the CdTe absorber thicknesses. All J-V parameters demonstrated under-performance at short $CdCl_2$ dose times, signifying incomplete absorber passivation. The dose time for minimum acceptable passivation was lower for thinner CdTe devices as expected and following the minimum absorber passivation, J_{SC} remained relatively flat over the dose time range, V_{OC} increased slightly, and fill factor peaked, and decreased slightly independent of CdTe thickness. These parameter trends dictate the trend seen in efficiency, where performance was low

at short dose times, stable after minimum passivation, and decreased slightly at the longest dose times. These data suggest that thin CdTe device performance can greatly suffer with under-passivation, as is the case for all CdTe devices, but can also suffer somewhat due to over-passivation. They also indicate that for these CdTe thicknesses, there is a relatively wide range of $CdCl_2$ dose times for which performance is optimal, therefore a 150-second $CdCl_2$ dose time was chosen as the optimized dose condition for thin CdTe absorbers, and was implemented in all forthcoming device fabrication.

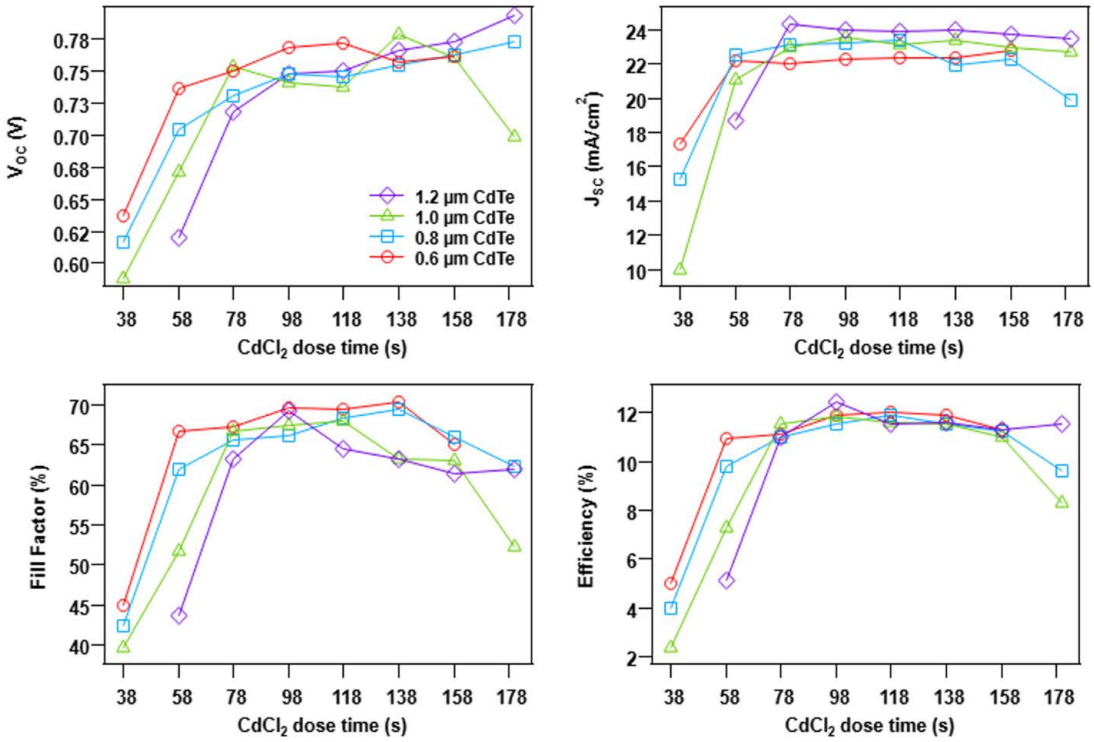

Figure 3.2: J-V parameters as a function of $CdCl_2$ dose time for best-performing 0.6-1.2 µm CdTe devices.

Effects of varied $CdCl_2$ anneal time were also explored through the fabrication of 1.0-µm CdTe devices with $CdCl_2$ dose time held fixed and anneal time varied from 90-300 seconds in 30-second increments. The J-V data, presented by A. Wojtowicz [73], exhibited little dependence on $CdCl_2$ anneal time and good device behavior; efficiencies were ∼13% and variation in best device performance did not exceed 0.6% across the anneal time range. This

demonstrated that thin CdTe device performance is much more sensitive to $CdCl_2$ dose time than the subsequent anneal time.

3.1.2 Cu Doping Treatment

Similar to the $CdCl_2$ passivation treatment, optimization experiments for the Cu doping treatment were two-fold through independent variation of Cu dose and anneal times, described in detail in [73]. Devices for Cu dose-time variation were fabricated with 1.0-µm CdTe absorbers, and passivated with 120 seconds $CdCl_2$ dose, followed by a 180-second anneal. The Cu dose time was varied from 0 to 10 seconds such that the range encompassed devices with no intentional Cu doping to devices with heavy doping (where heavy doping was based on Cu treatment conditions for thicker samples [56]). J-V parameter data of the devices as a function of Cu dose time are given in Figs. 3.3 (a), (b), (c), and (d) for V_{OC}, J_{SC}, fill factor, and efficiency respectively. V_{OC} improved significantly with the incorporation of Cu-doping, and increased in value and reproducibility for 2-6 seconds of Cu doping before decreasing in the same metrics at the longest Cu dose times. J_{SC} exhibited minor improvements with increased Cu dose time, while fill factor improved somewhat with the introduction of Cu doping, but decreased at longer Cu dose times. Consequently the devices demonstrated optimal performance for short Cu dose times, which may also be beneficial for the mitigation of potential stability problems, as over-doping can cause long-term performance instability in Cu-doped CdTe devices [74, 75].

To decouple possible Cu dose and anneal time inter-dependence in Cu anneal experiments, both Cu dose and anneal times were varied; Cu dose times of 2, 6, and 10 seconds were selected, and for each Cu dose time, anneal times of 35, 45, 55, 110, and 220 seconds were studied. The results of J-V characterization, not shown here, but presented in [73] demonstrated a number of trends in J-V parameters which were consistent across all three Cu dose times: improvement in V_{OC} with longer Cu anneal times, a J_{SC} which remained relatively high for short anneal times, but decreased for the 110 and 220 second anneal times, and a fill factor which consistently decreased as anneal time increased. Thus, device

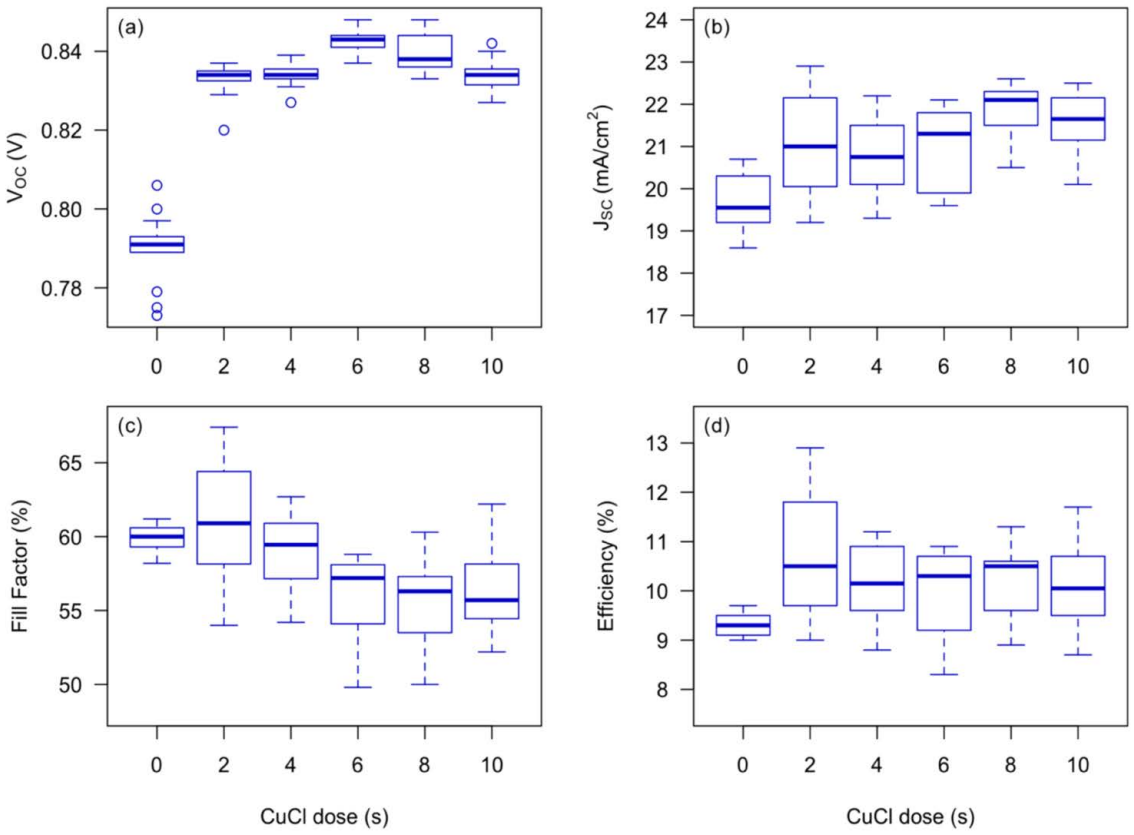

Figure 3.3: J-V parameters as a function of CuCl dose time for 1.0-µm CdTe devices. (The number of devices ranges from 13-19; some extreme outlier were removed). From Ref. [73].

efficiencies were best with the shortest anneal times, and decreased notably for the 110 and 220-second anneal times. Longer Cu doses demonstrated slightly poorer performance overall such that the best-performing devices had a 2-second Cu dose with a 35-second anneal.

3.2 Structure Morphology

Electron microscopy imaging was used to examine film characteristics such as grain size, coalescence, and interface quality for thin CdTe structures. Figs. 3.4 (a), (b), (c), and (d) show planar SEM images of 0.4, 0.5, 0.9, and 1.1 µm CdTe films respectively, deposited on Tec10/100-nm MgZnO substrates. The minimum grain size appeared to increase slightly with increasing CdTe thickness such that the grain size range was somewhat narrowed with thicker CdTe, as detailed in Table 3.1. Grain coalescence also seemed to increase somewhat for thicker CdTe absorbers. The changes in grain size and coalescence, although fairly small, could be due to the slightly longer CdTe sublimation times [56]. The SEM images showed uniform CdTe film coverage with no signs of voids or columnar growth formations, which is typically exhibited by substantial space in between grains [76, 77]. The favorable grain morphology indicates that when completed into devices, CdTe absorbers as thin as 0.4 µm should not suffer from film non-uniformity effects.

Table 3.1: CdTe grain sizes as determined by planar SEM.

CdTe Thickness (µm)	Grain Size Range (µm)
0.4	0.3-1.3
0.5	0.4-1.0
0.9	0.5-0.9
1.1	0.5-1.2

Interfaces were examined through STEM imaging of a FIB-prepared 1.0-µm CdTe film structure with optimized $CdCl_2$ and Cu treatments. The bright field cross-sectional STEM

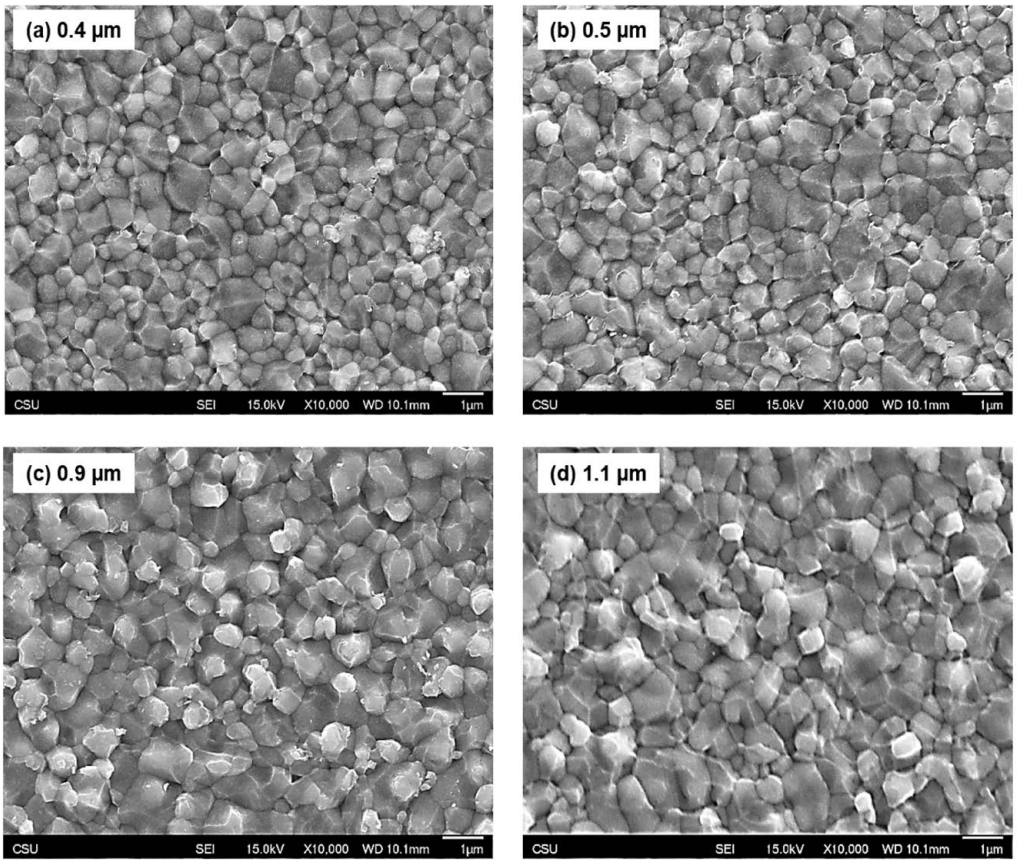

Figure 3.4: Planar SEM images of CdTe films with thicknesses of 0.4 (a), 0.5 (b), 0.9 (c), and 1.1 µm (d). Grain size and coalescence appear to increase slightly with CdTe thickness.

image, given in Fig. 3.5, showed several features which are favorable for solar-cell performance. First, at the front interface, is the continuity of the MgZnO layer; there are no discernible void formations at the CdTe/MgZnO interface or within the MgZnO layer. EDX analysis also showed no significant change in magnesium composition in the MgZnO layer for different CdTe thicknesses. Thus the CdTe deposition and $CdCl_2$ treatment conditions for this structure do not significantly impact the MgZnO layer. Secondly, most of the CdTe grains in the image area extend throughout the entire absorber layer, and there are no visible smaller CdTe crystallite formations near the MgZnO interface. At the back surface, the roughness of the CdTe grains is on the order of 0.1 µm, with the minimum thickness defining the effective electronic thickness of the structure. The final favorable feature, despite the CdTe roughness, is that the Te layer is conformal to the CdTe at the back. This, combined with the apparent robustness of the MgZnO layer, suggests that a completed device with this structure should have uniform lateral performance.

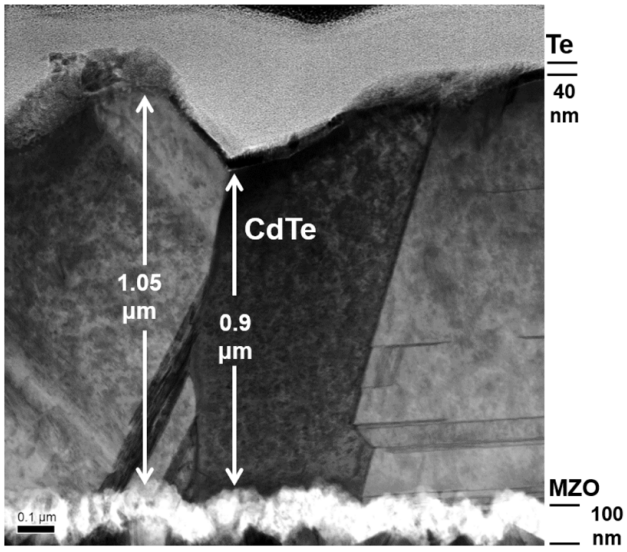

Figure 3.5: Bright field STEM image of a nominal 1.0-µm CdTe structure. The MgZnO/CdTe, and CdTe/Te interfaces are conformal, and the CdTe grains extend throughout the absorber layer. From Ref. [78].

3.3 Performance of 0.4-1.2 µm CdTe Devices

3.3.1 Current Density-Voltage Behavior

Given an understanding of the optimized post-deposition $CdCl_2$ and Cu treatment conditions and morphology in thin CdTe structures, devices were fabricated with CdTe absorber thicknesses of 0.4, 0.6, 0.8, 1.0, and 1.2 µm ± 0.05 µm. J-V dark and light curves of the best-performing devices for each CdTe thickness are given in Fig. 3.6 and corresponding J-V parameters are listed in Table 3.2. 15.0% device efficiency was achieved for a 1.2-µm device, with a V_{OC} of 0.847 V, J_{SC} of 24.0 mA/cm^2, and fill factor of 74.0%. This performance is considerably higher than the 11-13% ∼1.2 µm CdTe device efficiencies reported in literature [60–62,64], due primarily to increased J_{SC} and V_{OC}. The improvements are likely owed to the combined benefits of replacing the CdS emitter layer with MgZnO, incorporation of a Te layer at the back, and fabrication optimization.

Although device performance decreased with CdTe thickness, the diode quality of all of the J-V curves was well-behaved. Fig. 3.6 shows that as the absorber thickness was reduced, the extent of crossover between light and dark J-V curves increased. This may be due to a change in electron current, which is dependent on both absorber thickness and recombination strength in the bulk. As presented by McMahon and Fahrenbruch, as absorbers are made thinner, the electron current component of the total current can become quite large and have a strong voltage dependence. In this case, in the far-forward voltage domain, light can supply additional electron current through the cell and become the dominant component of the total current at the back [79]. Modeling results presented in [79] demonstrated that in this case, where the electron current is dominant in the light and dark, crossover of the light and dark J-V data occurs. Thus the increased extent of crossover exhibited in Fig. 3.6 for thinner absorbers could be attributed to increased dominance of the electron current over the hole current.

The J-V parameters of the five best-performing devices at each CdTe absorber thickness are given in Fig. 3.7. J_{SC} and fill factor demonstrated the most significant dependence

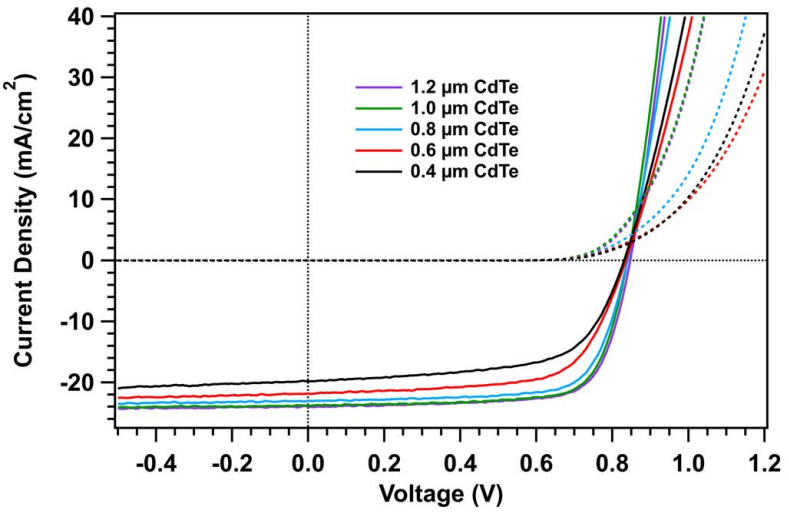

Figure 3.6: Dark and light J-V curves of the best-performing devices with 0.4-1.2-µm CdTe absorbers.

on CdTe thickness, and are discussed in detail in section 3.4. V_{OC} demonstrated a minor dependence on CdTe thickness such that there was an overall voltage gain of approximately 20 mV from 0.4 to 1.2 µm. Although fairly minimal, the voltage loss for thinner absorbers is likely due to the closer proximity of the emitter/absorber junction to the recombination-prone back contact, which increases the probability of recombination at the back, and generates a reduction in V_{OC}.

3.3.2 Capacitance Measurements

Capacitance measurements are particularly useful for thin CdTe devices as they can provide a good measure of the range of voltages over which an absorber is fully depleted. Capacitance was measured on the best-performing devices given in Table 3.2 at fixed voltages of -2.0, -1.0, 0, and 0.2 V as a function of frequency, from 1-1000 kHz. The admittance phase angle was near 90° for the applied voltages such that capacitance and conductance could be reliably separated. For each CdTe thickness, variation in the capacitance was minimal across all applied voltages up to 400 kHz. 100 kHz was selected for capacitance-voltage measurements to avoid erroneous capacitance measurements at low and high frequencies,

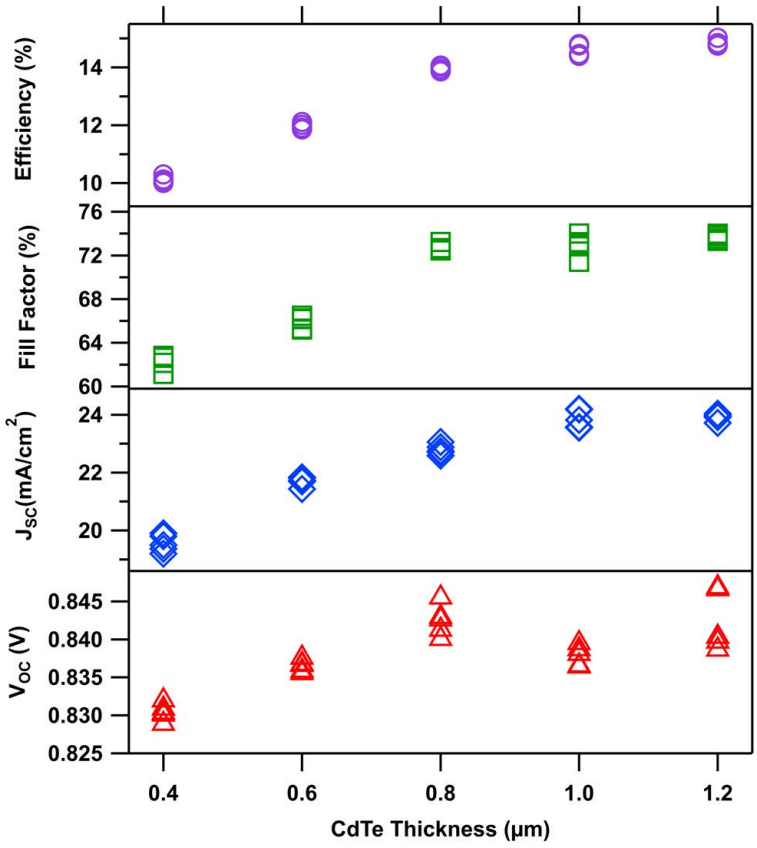

Figure 3.7: J-V parameters of the five best-performing devices at each CdTe absorber thickness.

Table 3.2: J-V parameters of best devices with varied CdTe thickness.

CdTe Thickness (µm)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
0.4	0.831	19.8	62.6	10.3
0.6	0.836	21.8	66.5	12.1
0.8	0.840	23.1	72.6	14.1
1.0	0.840	23.8	74.0	14.8
1.2	0.847	24.0	74.0	15.0

where low and high are determined by the free carrier relaxation time relative to the ac frequency. States which can release their charge in the modulating ac period contribute to the admittance; at low frequencies, deep level trap states contribute to the measured capacitance, and the capacitance model given by Eq. 2.24 no longer applies in its given form [11, 32, 35]. At high-frequencies, effects of series resistance and stray inductance can diminish accurate capacitance measurement [11, 35] (as seen above 300 kHz in CIGS solar cells [35]), and relative accuracy specifications of commercial instruments can degrade to a few percent beyond 100 kHz [80].

Fig. 3.8 (a) shows C^{-2} vs. voltage data for the best-performing 0.4-1.2 µm CdTe devices. Thinner absorbers demonstrated larger capacitance and smaller C^{-2} as expected. At far-forward bias, ∼0.65 V, the data demonstrated slope reduction, which is indicative of voltage sharing by the back contact [81], although this characteristic appeared to be independent of CdTe thickness. The flat portion of the C^{-2} data, where the capacitance is independent of voltage, designates the fully-depleted region of the absorber [32, 81], and was also used as an indication of the electronic thickness of the absorbers. In addition to the expected voltage-dependent depletion, the data demonstrated that depletion was CdTe thickness-dependent: the 0.4 and 0.6 µm devices remained fully-depleted into forward bias, and the extent of full

depletion shifted slightly toward 0 V bias for the 0.8, 1.0, and 1.2 µm devices. A fully-depleted absorber into forward bias is important for electron-reflector incorporation and the creation of a back-surface field, discussed in Chapter 5.

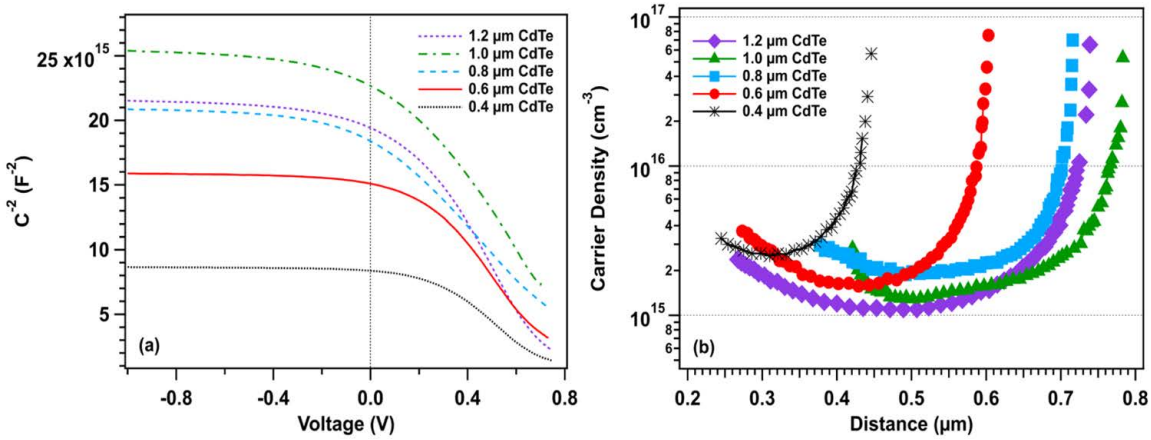

Figure 3.8: (a) C^{-2} vs. voltage curves show the CdTe is depleted into forward bias for the thinnest absorbers, and carrier density curves in (b) show carrier densities in the high-10^{14}-low-10^{15} cm^{-3} range. From Ref. [78].

Modified deep states (where the activation energy $E_a \gg kT$), which are common in polycrystalline CdTe, seem to be present in these devices, as suggested by the relative slope change after the turning point in the C^{-2} vs. voltage plots. The turning point corresponds to the voltage at which the depletion region collapses and an increase in capacitance is measured [32]. Modeling by Li et al. demonstrated that a shallower slope in C^{-2} vs. voltage data after the turning point indicates increased deep state effects [81]. Fig. 3.9 shows the slope for each CdTe thickness, calculated with a linear fit of the data in Fig. 3.8 (a) between the turning point and the maximum voltage point before the onset of voltage-sharing effects, around 0.65 V. The data showed a general increase in negative slope with increased CdTe thickness, and an increase in uncertainty due to the less distinct turning points for thicker CdTe devices. The negative slope increase with greater thickness suggests that the thinner CdTe devices are subject to greater deep state effects.

Fig. 3.8 (b) shows carrier densities in the low 10^{15} cm^{-3} range for all of the devices, as measured at the bottom of the U-shaped carrier density curve. The carrier density is not

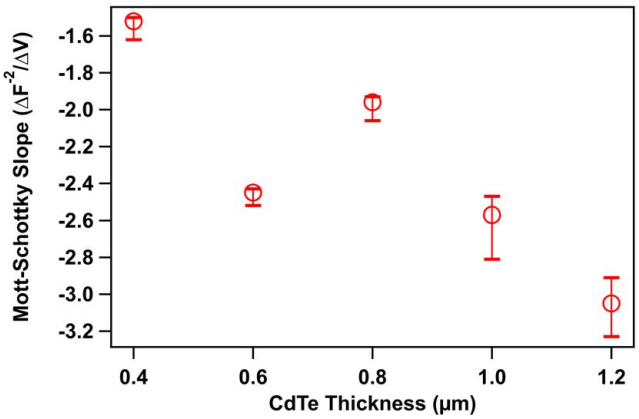

Figure 3.9: Slopes of C^{-2} vs. voltage data for each CdTe thickness device determined by fits to data at voltages beyond the turning point. Increased negative slope with increased CdTe thickness indicates a less contribution from deep states.

reported from the zero voltage point as is sometimes done because the carrier concentration value at 0 V bias is erroneously high for thin absorbers due to the presence of the punch through effect at this voltage [81] (i.e. the effect of a fully-depleted absorber). Even at the bottom of the carrier density curves, carrier concentration values are likely artificially high because thin, fully-depleted absorbers and deep states can falsely shift the middle and right side of the carrier density curve upward [81]. This was observed in Fig. 3.8 (b), where the apparent carrier concentration was highest for the thinnest, 0.4-µm device, and decreased for the thicker devices. Since there was no intentional change in Cu doping for these devices, it is unlikely this carrier concentration shift is accurate. Therefore the data in Figs. 3.8 (a) and (b) suggest a change in deep state contributions with CdTe thickness, with the greatest contributions in the thinnest devices. Thus, the carrier density in these devices is assumed to be artificially high, most notably for the thinnest devices, and the true carrier density is likely in the high 10^{14} cm^{-3} range, which is typical for Cu-doped polycrystalline CdTe devices.

3.4 Performance Loss Analysis

Based on absorber band gap, every PV device has a set of ideal J-V parameters given by the Schockley-Queisser limit [82]. The ideal is not reached because all solar cells are subject to performance reduction due to a variety of loss mechanisms. Of the measured J-V parameters in Fig. 3.7, J_{SC} and fill factor demonstrated the most notable absorber thickness-dependence, therefore loss mechanisms for these two parameters are analyzed in this section.

3.4.1 Fill Factor Losses

Generalized Fill Factor Loss Calculations

Measured fill factor, lower than the ideal fill factor due to mechanistic losses in the solar cell, is most generally described by:

$$FF_{meas} = \alpha FF_0 \tag{3.1}$$

where α is the loss factor such that $0 \leq \alpha \leq 1$, and FF_0 is the ideal fill factor which is dependent on the solar cell absorber material. FF_0 is given by [21]

$$FF_0 = \frac{v_{oc} - ln(v_{oc} + 0.72)}{v_{oc} + 1} \tag{3.2}$$

where v_{oc} is the normalized voltage, empirically given by:

$$v_{oc} = \frac{V_{OC}}{AkT/q}, \tag{3.3}$$

such that Eq. 3.2 is accurate to about four significant digits for $v_{oc} > 10$. In the case of ideal fill factor, the diode quality factor, A, is equal to unity. For a 1.5-eV band gap CdTe device operating under standard test conditions of AM 1.5G spectrum illumination and 25 °C, the ideal V_{OC} and J_{SC} are 1.20 V and 29.3 mA/cm^2 respectively [34], such that the ideal fill factor is 89.8%.

The loss factor, α, can be represented by the product of losses, $\alpha_1\alpha_2\alpha_3\alpha_4...\alpha_i$, where α_i is the fractional loss from a specific mechanism. Here, these losses are separated into four general mechanisms: non-ideal diode, series resistance, shunt conductance, and small "other" losses not accounted for, designated by α_{diode}, α_{series}, α_{shunt}, and α_{other}, respectively. Thus, the loss factor can be rewritten as:

$$\frac{FF_{meas}}{FF_0} = \alpha = \alpha_{series}\alpha_{shunt}\alpha_{diode}\alpha_{other} \tag{3.4}$$

Solar cells typically have parasitic series and shunt resistance losses which are due to a number of physical mechanisms, and contribute to a reduced fill factor. Bulk resistance of the semiconductor material, metallic contacts, and interconnects are typically responsible for increased series resistance, R_S. Leakage across the p-n junction around the cell edge, as well as in non-peripheral areas given the presence of crystal defects and foreign impurities near the junction due to precipitates, can cause a reduced shunt resistance, R_{SH}, [21] or increased shunt conductance, G. The contribution of these parasitic losses to reduced fill factor can be analyzed using a method developed by M. Green [21], outlined below.

The characteristic resistance of a solar cell, defined as

$$R_{CH} = \frac{V_{OC}}{J_{SC}}, \tag{3.5}$$

is used comparatively to determine the extent of the effect of series resistance and shunt conductance on fill factor. This is done by defining normalized resistances $r_s \equiv R_S/R_{CH}$ and $g \equiv 1/GR_{CH}$ for series resistance and shunt conductance respectively. The loss factor due to series resistance is given by the approximate analytical expression:

$$\alpha_{series} \approx 1 - r_s \tag{3.6}$$

and the loss factor due to shunt conductance is given by:

$$\alpha_{shunt} \approx 1 - \frac{(v_{oc} + 0.7)}{v_{oc}}\frac{FF_0}{g} \tag{3.7}$$

where in this case, v_{oc} utilizes A=1 to minimize coupling to the diode quality factor loss term discussed below.

Non-ideal diode losses can originate from reductions in V_{OC} and a diode quality factor greater than unity. Therefore, α_{diode} can be expanded to separate the contributions from reduced V_{OC} and diode quality factor. This expansion is done by judiciously introducing factors of one such that fill factor ratios are represented as a function of V_{OC} and A [34]. The expansion is given by:

$$\alpha_{diode} = \frac{FF(V_{OC}, A)}{FF_0} = \frac{FF_{A=1,V_{OC}}}{FF_0} \frac{FF_{A,V_{OC-ideal}}}{FF_{A=1,V_{OC}}} \frac{FF_{A,V_{OC}}}{FF_{A,V_{OC-ideal}}} \tag{3.8}$$

where A=1 and V_{OC}-ideal are the ideal A and V_{OC} values, and A and V_{OC} are the measured values. Each ratio term in Eq 3.8 corresponds to a physical diode loss mechanism. The first ratio corresponds to reduced V_{OC} independent of the diode quality factor, A. This could be associated with Φ_b, the barrier height, which impacts the V_{OC} with no A dependence, as demonstrated most clearly with V_{OC} written in the form [32]:

$$V_{OC} = \frac{\Phi_b}{q} - \frac{AkT}{q} ln\left(\frac{J_{00}}{J_{SC}}\right). \tag{3.9}$$

The remaining ratios, in order, correspond to loss in fill factor due to a diode quality factor higher than unity, and to reduced V_{OC} with diode quality factor dependence.

The final loss factor in Eq 3.4, α_{other}, is incorporated to cover any additional losses if a differential from FF_0 remains. It does not have a closed form representation, but rather is a derived value calculated such that FF_0 is realized.

Fractional losses are converted to an absolute fill factor scale according to

$$FF_x = \frac{1-\alpha_x}{\sum_i 1-\alpha_i} (FF_0 - FF_{meas}) \tag{3.10}$$

where x is the loss of interest, the quotient term weighs the loss of interest relative to total losses, and the parenthesized term scales to the ideal and measured fill factor differential.

Given the dependence of fill factor losses on J-V quality-parameters A, G, and R_S, determination of these parameters is necessary to perform fill factor loss analysis.

Current-Voltage Analysis Methodology

J-V quality parameters R_s, G, and A are determined using a current-voltage analysis method described by Hegedus and Shafarman [32]. This analysis evaluates the J-V curve in its entirety, utilizing the single exponential diode equation which separates recombination and parasitic losses:

$$J = J_0 exp\left[\frac{q}{AkT}(V - RJ)\right] + GV - J_L \tag{3.11}$$

for the case of constant J_L.

In this method, data from the J-V curve are differentiated and plotted in three different ways such that the J-V quality parameters can be extracted (example in Fig. 3.10). First, dJ/dV is plotted against voltage as shown in Fig. 3.10 (b), and the data are fit to the region near 0 V bias to exploit a negligible derivative of the diode term in Eq 3.11 and to avoid misconstruing effects of voltage-dependent collection on shunt resistance. Given a well-behaved diode with an ohmic shunt term and constant J_L, dJ/dV should be relatively flat in reverse bias such that a fit of this region to the ordinate gives the shunt conductance, G.

Second, for the case where G is non-negligible and voltage dependent, as determined by the fit in Fig. 3.10 (b), dV/dJ is plotted against (1-G$\left(\frac{dV}{dJ}\right)$)/(J+$J_{SC}$-GV) as shown in Fig. 3.10 (c). From Eq 3.11,

$$\frac{dV}{dJ} = R_S + \frac{AkT}{q}\left[\frac{1 - G\left(\frac{dV}{dJ}\right)}{J + J_{SC} - GV}\right] \tag{3.12}$$

and a linear fit to the data gives R_S and A, as determined by the intercept and the slope (= AkT/q) respectively. In Eq. 3.12, J_{SC} replaces J_L for the case of voltage-independent J_L.

The final graph is semi-logarithmic and plots (J+J_{SC}-GV) versus V-RJ as shown in Fig. 3.10 (d), where the value of R_S obtained from the fit to Eq 3.12 is employed. A linear fit to the data, typically present over at least 1-2 orders of magnitude given a good fit to the diode equation, can be performed such that J_0 is determined from the intercept and A by the slope.

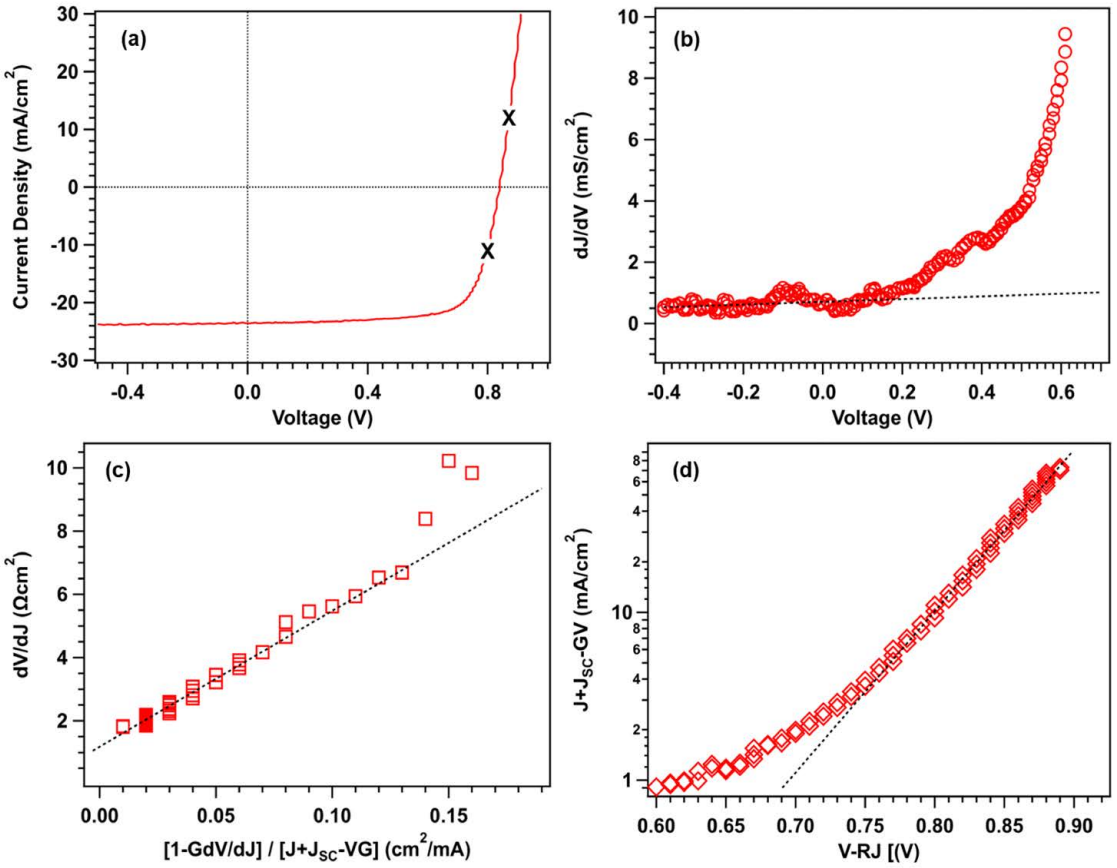

Figure 3.10: J-V analysis example for extracting J-V quality parameters by plotting the diode equation in derivative forms such that linear fits provide the parameters in question. (a) the initial J-V curve, (b) dJ/dV vs. voltage for determination of G, (c) dV/dJ to determine R_S and A, and (d) the semi-log plot of J+J_{SC}-GV to determine J_0 and A.

.

Since A may not be constant with voltage, the two different linear fits of Figs. 3.10 (c) and (d) offer a cross-check on the calculated diode quality factor; an average of the two calculated values is used given reasonable agreement, and in the case of large discrepancies in A, poor diode quality is concluded. Diode quality factor, series resistance, and J_0 are determined under the assumption that the parameters are constant with voltage. This is not always the case as can be seen in deviations from linearity in any of the plots, and demonstrated explicitly by Hegedus and Shafarman [32]. To minimize possible contributions from voltage dependence, linear fits of the data given in Figs. 3.10 (c) and (d) are performed within the voltage region surrounding V_{OC}, with a voltage range extending no further than ΔV to the maximum power point. The range where data is linear in Figs. 3.10 (c) and (d) is indicated by the "X"s in Fig. 3.10 (a).

It is worth noting that this method can inherently produce inconsistencies due to its somewhat subjective nature rooted in fitting region choices. Results tend to be consistent for a single individual performing the analysis, but are less consistent with variation in analysts. All current-voltage analyses presented in this work were performed by the author and utilized a fitting program, CurVA, developed by Markus Gloeckler, which implements the described method to extract J-V quality parameters.

Fill Factor Losses with Varied CdTe Thicknesses

Current-voltage analysis was completed on the five best-performing 0.4-1.2 µm CdTe devices given in Fig. 3.7, and resultant J-V quality parameters are shown in Figs. 3.11 (a), (b), and (c) for series resistance R_S, shunt conductance G, and diode quality factor A, respectively. Series resistance data demonstrated the most spread at each absorber thickness, and seemed to show a slight decrease overall with increased CdTe thickness. Shunt conductance demonstrated less spread in the data at each absorber thickness, and a stronger dependence on CdTe thickness with a factor of 5 decrease in G from 0.4 to 1.2 µm CdTe. Finally, the diode quality factor also showed minimal spread in the data at each absorber thickness, and seemingly increased with decreasing CdTe thickness. However, the extent of this increase

may appear larger than in actuality because some distortion in the 0.4-µm J-V data, as demonstrated in Fig. 3.6, may have generated artificially high diode quality factors.

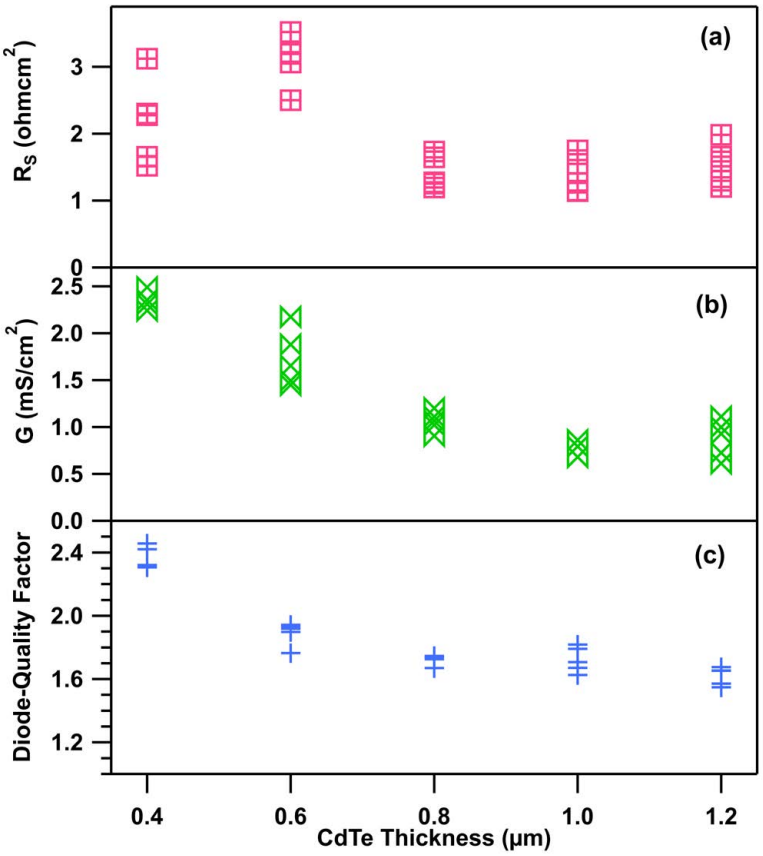

Figure 3.11: J-V quality parameters (a) series resistance, (b) shunt conductance, and (c) diode quality factor as a function of CdTe thickness determined by J-V analysis. From Ref. [78].

The J-V quality parameters of the best-performing 0.4-1.2 µm devices in Fig. 3.11 were used to separate fill factor loss mechanisms as a function of CdTe thickness. The results of the fill factor loss analysis are shown in Fig. 3.12 and listed in Table 3.3. Fill factor notably increased with CdTe thickness, and contributions from some individual loss mechanisms were more thickness-dependent than others. The A-independent component of V_{OC} reduction was invariable with CdTe thickness, contributing ~3% to fill factor loss. If this term is ascribed to barrier height as presented in Eq. 3.9, this loss mechanism should indeed be constant with absorber thickness, as the barrier height was likely unchanged for the different CdTe devices.

The A-dependent component of V_{OC} reduction was somewhat more thickness dependent, with larger contributions in the thinnest devices. Larger A-dependent V_{OC} loss contribution in the thinnest devices could be caused by multiple possible mechanisms; from Eq 3.9, these could be one or any combination of increased A, decreased J_{SC}, and increased J_{00}. These two loss components together indicate that V_{OC} reduction is somewhat absorber-thickness dependent within the CdTe thickness range.

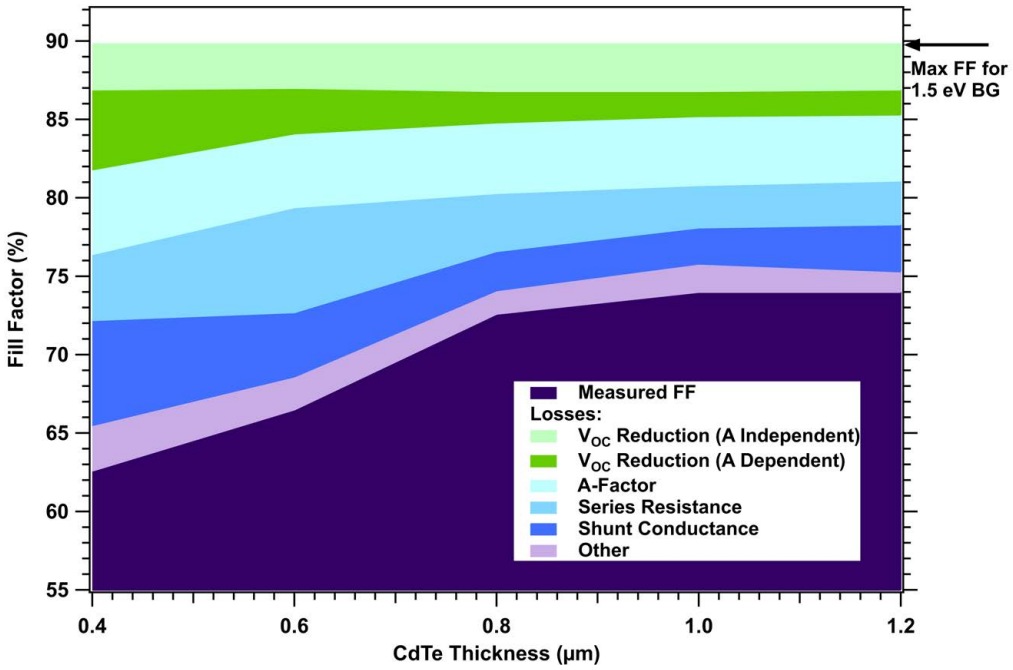

Figure 3.12: Fill factor loss mechanisms of the best-performing 0.4, 0.6, 0.8, 1.0 and 1.2-µm CdTe devices.

The absolute percentage contribution of series resistance and shunt conductance to fill factor losses diminished for thicker absorbers due to the overall decrease in R_S and G as indicated in Fig. 3.11. However, the fractional loss contributions for these mechanisms did not show CdTe thickness dependence, which indicates that although series resistance and shunt conductance values changed with CdTe thickness, they contribute consistently relative to total fill factor loss. The diode quality factor loss mechanism was also dependent on CdTe thickness and among the higher loss-contribution mechanisms. When considered in conjunction with A-dependent V_{OC} reduction, losses tied to increased diode quality factor seemed

Table 3.3: Fill factor losses for 0.4-1.2 µm CdTe devices.

	% Fill Factor				
Mechanism	**0.4 µm**	**0.6 µm**	**0.8 µm**	**1.0 µm**	**1.2 µm**
V_{OC} Reduction (A Independent)	2.9	2.9	3.0	3.0	2.9
V_{OC} Reduction (A Dependent)	5.1	2.9	2.0	1.6	1.6
A Factor	5.4	4.7	4.5	4.4	4.2
Series Resistance	4.2	6.7	3.7	2.7	2.8
Shunt Conductance	6.7	4.1	2.5	2.3	3.0
Other	2.9	2.1	1.5	1.8	1.3
Measured Fill Factor	**62.6**	**66.5**	**72.6**	**74.0**	**74.0**

to be the dominant loss mechanism in these thin CdTe devices. As such, improvements in the diode quality will provide the greatest fill factor improvements.

Poor diode quality can arise from distortions in the J-V curves which are due to voltage-dependent photocurrent, $J_L(V)$, known to reduce fill factor in CdTe devices [83]. To demonstrate the effects of $J_L(V)$ on thin CdTe devices, a comparison of the forward current density, $J_F(V)$, and the solar cell's net current density, J(V), is made utilizing [83]:

$$J(V) = J_F(V) - J_L(V) \tag{3.13}$$

The forward current density is determined by the standard forward diode equation with the measured voltage corrected for series resistance, such that it yields the actual voltage across the absorber:

$$J_F(V) = J_0 exp\left[\frac{q\,(V - RJ)}{AkT}\right] \tag{3.14}$$

where J_0, R, and A are determined by current density-voltage analysis on dark J-V curves, and J is the measured current density.

Eqs. 3.13 and 3.14 were applied to the 0.4 and 1.2 µm devices, with J_F offset by J_{SC}, to highlight the difference in $J_L(V)$ for the thinnest and thickest absorbers. $J_F(V) - J_{SC}$ and J(V) are given in Fig. 3.13 (a) and (b) for the 0.4 and 1.2 µm devices respectively, where the differential corresponds to J_L loss, and is indicated. Voltage-dependent photocurrent was present in both devices, and increased by a factor of approximately 2.5 for the 0.4 µm device. This indicates that all of the thin CdTe devices are subject to fill factor loss due to voltage-dependent photocurrent, although the thinnest devices suffer greater losses due to this effect. It is possible to further quantify the effects of $J_L(V)$ on the given devices through intensity-dependent J-V measurements, or by fitting a lumped circuit model to J-V measurements under one sun intensity as described in [83], although such quantifications were outside the scope of this work.

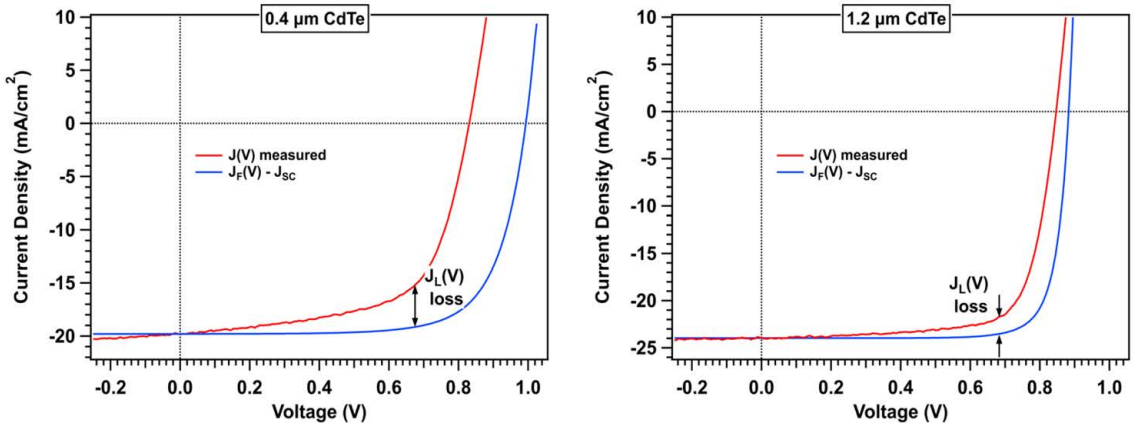

Figure 3.13: Voltage-dependent photocurrent plays a greater role in thinner CdTe devices as demonstrated by the J_L(V) loss for 0.4 µm (a) and 1.2 µm (b) devices.

3.4.2 Current Density Losses

Solar cells are also subject to performance losses through loss mechanisms which reduce the current collected in the device. Different PV technologies may be more likely to suffer from certain current loss mechanisms based on structural design. Techniques to minimize specific loss mechanisms have been implemented in different PV technologies, for example texturing, [21,84–86], anti-reflective coatings [56,87,88], and optical back reflectors [89–91] to

reduce reflection. Due to their many material layers, thin-film PV devices have a multitude of potential current loss mechanisms, the details of which are presented below for CdTe structures based on current analysis methods described in [32].

Generalized Current Density Loss Calculations

Current density losses in CdTe devices are separated into four loss mechanisms: front-layer absorption, reflection, incomplete absorption, and recombination loss. Given the multi-layer optical stack configuration of CdTe solar cells, incident photons must pass through multiple layers before entering the CdTe absorber where carrier generation occurs. These layers reduce the amount of light which reaches the CdTe layer, thus lowering current collection through diminished carrier generation. Front-layer materials can be chosen judiciously to minimize the effect of front-layer absorption, and in the case of CdTe devices, these layers consist of transparent glass, a transparent conducting oxide (TCO) layer, and the nearly transparent MgZnO window layer.

The optical stack also induces current loss through photon number reduction due to reflection at each interface. The individual front-reflection components are combined into a single term, R_F as described in [32]. R_F was determined by measuring reflection on completed devices using a spectrophotometer with an integrating sphere for direct and diffuse collection. A representation of the front reflection and absorption behavior in the superstrate CdTe structure is given in Fig. 3.14, simplified such that non-primary refracted rays and reflections are omitted.

The absorption of each front layer was determined in a multi-step fashion. To separate front absorption losses from one another, reflection and transmission were measured on plain soda-lime glass with low Fe content, TCO on glass (Tec10), and MgZnO deposited on Tec10. The absorption of each stack configuration was then determined by $A(\lambda) = 1 - T(\lambda) - R(\lambda)$ where $A(\lambda)$, $T(\lambda)$, and $R(\lambda)$ are the absorption, transmission, and reflection respectively. Absorption for each individual layer was then determined by calculating the appropriate

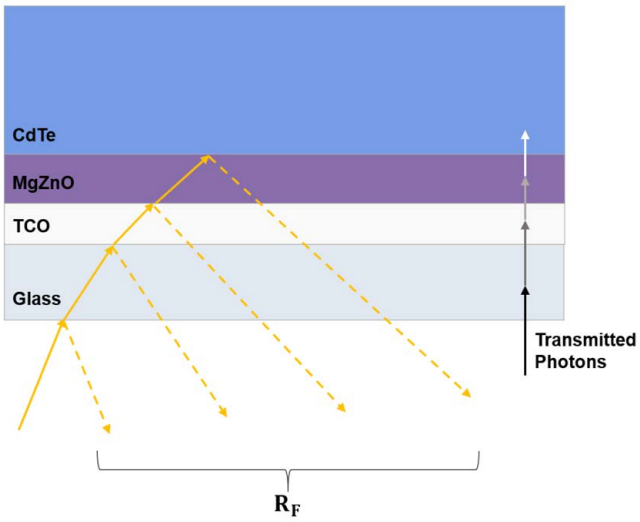

Figure 3.14: Front reflection and transmission evolution through the CdTe optical stack. Reflection occurs at each interface and is grouped into a single term, R_F, and light transmitted through each layer decreases due to reflection and absorption of previous layers.

absorption differentials (eg. TCO absorption was determined by the difference between measured Tec10 and soda-lime glass absorption).

The fraction of photons which reaches each front layer preceding CdTe changes due to the reflection-induced photon loss at each preceding interface, and the refractive indices of the materials at the interface. Therefore, each front-layer absorption term must be corrected for this reflection [32], and is given by

$$A'(\lambda) = \Big[1 - R_F(\lambda)\Big]A(\lambda) = \Big[1 - R_F(\lambda)\Big]\Big[1 - T(\lambda) - R(\lambda)\Big]. \tag{3.15}$$

R_F was used as an estimate for the reflection loss correction factor of all layers because reflection measured on each iterative front structure (glass, Tec10, Tec10/MgZnO) introduced artificial interfaces with air such that the sum of these measured reflections was greater than R_F, which is non-physical. Given the typical front reflection and absorption quantities (approximately 10% and 5% respectively) in the CdTe structure presented, the error in using this estimate is small. For a more precise determination of the reflection-loss correction factor, ellipsometry measurements could be performed on the different materials to determine n

and k values [11]. The error in using R_F as the reflection-loss correction factor proved to be small enough that ellipsometry measurements were not deemed necessary for these devices.

Light which is not absorbed by the absorber or any preceding layers will reach the back contact where it is absorbed and converted to heat. The fraction of light which reaches the back contact is usually fairly small in CdTe devices given its favorable absorption depth. However, for absorber thicknesses less than 2.0 µm, incomplete absorption functions as a notable current-density loss mechanism, especially in ultra-thin CdTe devices. To determine loss due to incomplete absorption, the fraction of incident light which reaches the absorber layer must be calculated. It is given generally by the product of the transmission through all of the preceding layers [32]:

$$T_F(\lambda) = T_G\Big[1 - R_F(\lambda)\Big]\Big[1 - A_{TCO}(\lambda)\Big]\Big[1 - A_E(\lambda)\Big] \tag{3.16}$$

where $T_F(\lambda)$ is the light incident on the absorber layer, and T_G is a grid shadowing factor less than unity for substrate-configured devices, and equal to unity for the given CdTe superstrate configuration. A_{TCO} and A_E are the measured absorption of the TCO/glass and emitter layers respectively.

For the CdTe configurations of interest, this can be implemented to determine the incomplete absorption in CdTe devices:

$$A_{inc}(\lambda) = \Big[1 - R_F(\lambda)\Big]\Big[1 - A_{MgZnO/Tec10}(\lambda)\Big]T(\lambda) \tag{3.17}$$

where A_{inc} is incomplete absorption, $A_{MgZnO/Tec10}$ is the measured absorption of MgZnO on Tec10, and $T(\lambda)$ is the measured transmission of the CdTe film without a back contact.

These optical losses can be plotted as a function of wavelength with measured QE data to provide a visual representation of the loss mechanisms in solar cells. Energies below the band gap are not considered losses, and are labeled sub-band gap light. Any remaining losses are grouped into a general recombination loss mechanism.

Current Density Losses with Varied CdTe Thicknesses

Results of current density loss analysis for the best-performing 0.4 and 1.2-µm devices are given in Figs. 3.15 (a) and (b) respectively, and the corresponding current densities of the given losses are reported in Table 3.4.

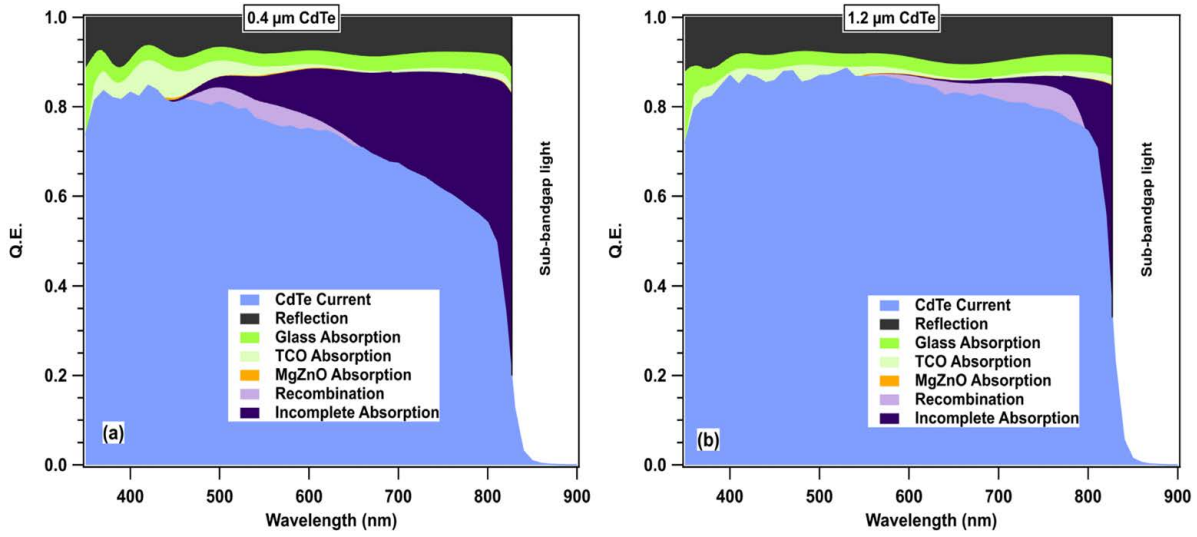

Figure 3.15: Current density loss analysis for 0.4 µm (a) and 1.2 µm (b) devices. Reflection and front-layer absorption losses were unchanged with CdTe thickness, and incomplete absorption loss was the dominant loss mechanism in the 0.4-µm device. From Ref. [78].

Current density is calculated for each of the loss mechanisms according to [14]:

$$J = q \int_0^{\lambda_{BG}} f(\lambda) \frac{\lambda P(\lambda)}{hc} d\lambda \tag{3.18}$$

where f(λ) is the function being integrated (this is equal to the measured QE data for calculation of J_{SC}), λ_{BG} is the absorber band gap wavelength, P(λ) is the spectral power for the standard AM 1.5G spectrum, and hc is the energy per photon. The quotient term is equal to the number of photons at each wavelength in the AM 1.5G solar spectrum. The maximum theoretical J_{SC} is calculated based on 100% QE across the given wavelength range in Fig. 3.15 and the 1.5-eV CdTe absorber band gap.

Table 3.4: Current density losses in 0.4-µm and 1.2-µm CdTe devices.

Mechanism	0.4 µm CdTe J (mA/cm^2)	1.2-µm CdTe J (mA/cm^2)
Reflection	2.3	2.6
Glass Absorption	1.0	1.0
TCO Absorption	0.6	0.4
MgZnO Absorption	<0.1	<0.1
Incomplete Absorption	4.1	0.5
Recombination	0.4	0.5
Device Current Density	**20.4**	**23.7**
Max Current Density	28.7	28.7

Glass and TCO absorption losses were approximately equal for the two CdTe thicknesses due to the nominally identical Tec10 substrates. Reflection loss was also comparable since it depends mostly on the unchanged refractive indices at each optical interface, and negligibly on absorber thickness. Absorption loss in the MgZnO layer is also independent of CdTe thickness and is very small because it is thin and nearly transparent over a wide wavelength range [45].

Measured quantum efficiency and incomplete absorption loss depended significantly on CdTe thickness. Incomplete absorption was the dominant current density loss mechanism in the 0.4-µm CdTe device and constituted the largest loss differential between the 0.4 and 1.2-µm devices; it accounted for 14% of the total current density losses in the 0.4-µm device and only 2% of the total losses in the 1.2-µm device. The dependence of QE and incomplete absorption on CdTe thickness is shown more explicitly in Fig. 3.16. These data, and those in Fig. 3.15 demonstrate the dominant role incomplete absorption plays in reducing J_{SC} for the thinnest devices, and also highlights that at only 1.2 µm of CdTe,

incomplete absorption is a fairly small loss-lower even than that of reflection and glass absorption. Incomplete absorption losses could be minimized with the addition of an optical back reflector layer [92], however, successful incorporation of such a layer in CdTe presently seems minimal. Additionally, reflection losses can, and frequently are, minimized by using an anti-reflective coating at the front [56, 88, 93].

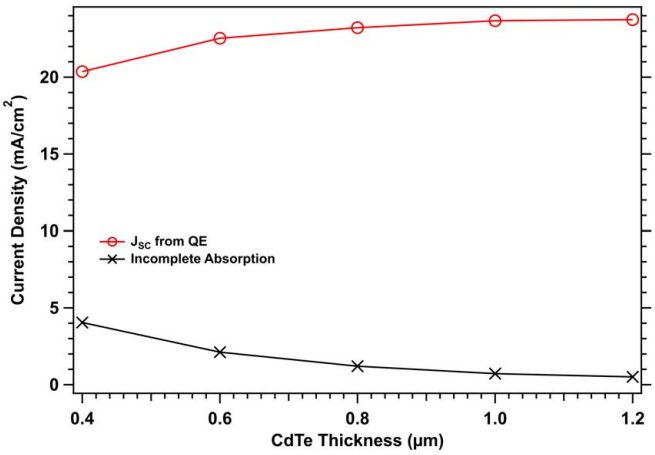

Figure 3.16: J_{SC} calculated from measured QE, and incomplete absorption current density loss as a function of CdTe thickness demonstrate the dominant role incomplete absorption plays in reducing J_{SC} for the thinnest devices.

Numerically, recombination loss was fairly constant with CdTe thickness, although as Fig. 3.15 shows, recombination loss occurred within different wavelength regimes for the different CdTe thicknesses. For the 0.4-µm CdTe device, recombination occurred between approximately 450 and 650 nm while it was prevalent between approximately 550 and 775 nm for the 1.2-µm device. This may indicate that recombination mechanisms vary depending on CdTe absorber thickness.

3.5 Photoluminescence Behavior

3.5.1 Room Temperature Photoluminescence of Thin CdTe

Recombination in thin CdTe devices was investigated further through PL emission spectroscopy and time-resolved photoluminescence (TRPL) measurements. Room-temperature PL emission spectroscopy was measured at open circuit with a 520-nm excitation laser incident on the glass side of the best-performing CdTe devices from Fig. 3.6. The resulting data are given in Fig. 3.17. The PL peak locations at approximately 1.51 eV were independent of CdTe thickness, and given the PL measurement conditions such that the recombination process was near band-to-band [11], the PL peak energies were very near the band gap. The PL band gap-value is in good agreement with the band gap calculated from QE data.

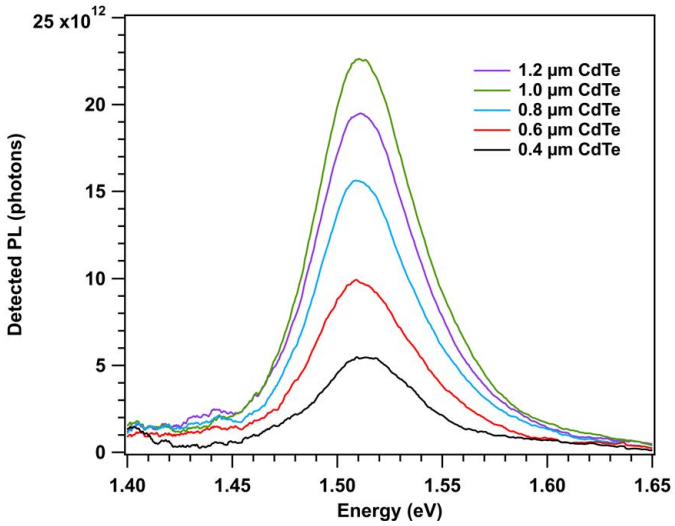

Figure 3.17: Room-temperature photoluminescence emission spectra for the best-performing 0.4-1.2 µm CdTe devices show a general PL emission increase for thicker CdTe.

PL intensity scaled generally with CdTe thickness where 0.4 and 1.0-µm devices demonstrated the lowest and highest peak intensities respectively. Since changes in external luminescence at open circuit can be an indicator of changes in internal optical losses and non-radiative recombination [85], the trend in PL intensity with CdTe thickness could be attributed to these two processes. As demonstrated in the current density loss analysis of these

devices, optical losses are present in each of these thin CdTe devices. The optical losses are more prevalent for the thinnest absorbers due to incomplete absorption, thus optical losses may explain in part the decrease in PL emission with decreasing absorber thickness. The apparent increase in photoluminescence efficiency with CdTe thickness may also be due to non-radiative recombination processes in the devices. However, it is unclear from PL emission spectroscopy alone whether the recombination processes are absorber thickness dependent, or if they just serve to lower the PL emission overall for all of the thin CdTe devices.

3.5.2 Time-Resolved Photoluminescence for Electro-Optical Characterization of Thin CdTe Structures

To further understand possible recombination processes in the thin CdTe devices, single-photon TRPL was measured with 1 mW-photoexcitation from the front and back of the structures [94]. A 44-nm band pass filter centered at 819 nm was used such that the TRPL emission was measured at 800-840 nm. For these measurements, thin CdTe structures were fabricated with varied absorber thickness (0.4-2.0 µm), no intentional Cu doping, and termination of the structure after the semi-transparent 40-nm Te layer such that effects of the MgZnO/CdTe front interface and CdTe/Te back interface could be investigated with independent front and back-side excitation. The thin-film structure is given in Fig. 3.18.

The TRPL decay data for 0.4-2.0 µm CdTe are given in Figs. 3.19 (a) and (b) for glass and Te-side photoexcitation respectively. Tail lifetimes, τ_2, were determined by fitting the slow part of the TRPL decay to a single exponential decay function, and because some tail lifetimes were short, deconvolution of the instrument response was incorporated into the fit. The τ_2 values for glass and Te-side excitations are given in Table 3.5 for each absorber thickness. Glass-side τ_2 demonstrated a systematic dependence on CdTe thickness: lifetimes increased from 0.3 to 2.0 $\pm$ 0.1 ns for 0.4-2.0 µm CdTe. Conversely, with excitation from the Te side, τ_2 values were much lower, $\tau_2 \leq 0.6 \pm 0.1$ ns, and fairly independent of CdTe thickness. As CdTe thickness increases and the p-n junction and back interface are further separated, back and front-interface effects are reduced for front and back-excitation

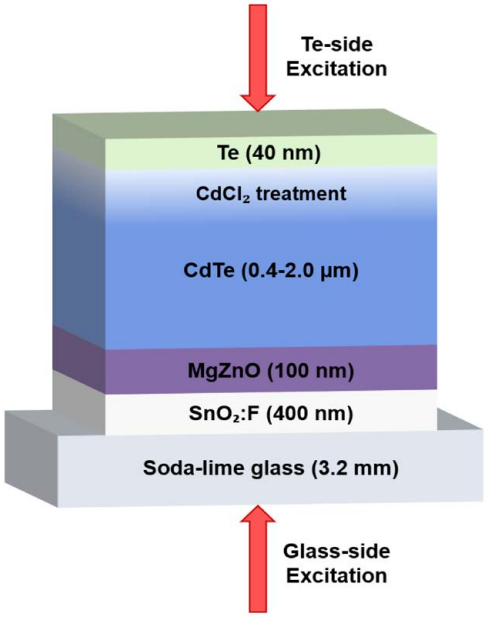

Figure 3.18: CdTe film structure for single-photon TRPL measured independently from the glass and Te-sides.

measurements respectively. Therefore the τ_2 increase for glass-side excitation and unchanged τ_2 for Te-side excitation strongly suggested a significantly higher interface recombination velocity for the CdTe/Te interface than the MgZnO/CdTe interface.

Intragrain and grain-boundary recombination can impact the bulk lifetime [96], for example CdTe bulk lifetime has been associated with grain diameter, where a factor of ten increase in grain diameter led to a factor of ten increase in bulk lifetime [96]. In our thin CdTe structures, changes in τ_2 were not linearly proportional to the minor changes in grain size (Table 3.1), thus it was concluded that the change in grain size with CdTe thickness was not significant enough to explain the trend in glass-side TRPL lifetimes.

To quantify electro-optical properties of the structures, recombination mechanisms which influence the TRPL decay measured from the glass side were considered [95]:

$$\frac{1}{\tau} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_S} + \frac{1}{\tau_{drift}} + \frac{1}{\tau_D} + \frac{1}{\tau_R} + \frac{1}{\tau_{th}} \tag{3.19}$$

where τ is the TRPL lifetime, consisting of τ_1 and τ_2 components for the initial (fast) and tail (slow) parts of the decay respectively. In general, bulk carrier lifetime (τ_{bulk}), interface

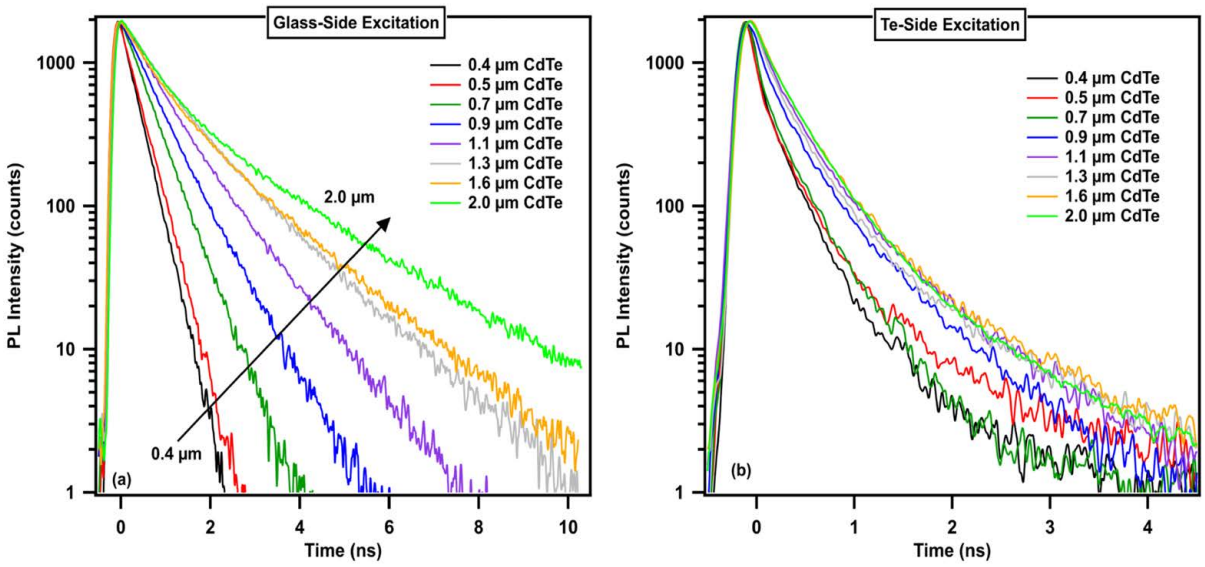

Figure 3.19: Single-photon TRPL decays for glass-side (a) and Te-side (b) photoexcitation with varied CdTe thickness. Comparison of the tail lifetimes' evolution with CdTe thickness for the two excitation directions indicates recombination at the back interface is greater than at the front interface. From Ref [78].

recombination (τ_S), drift (τ_{drift}), diffusion (τ_D), radiative lifetime (τ_R), and thermalization (τ_{th}) contribute to the minority carrier lifetime. The tunneling rate was not included because the 100-nm MgZnO layer is sufficiently thick that the tunneling rate through the wide barrier is considered to be very small [95].

Given the measured changes in τ_2 with CdTe thickness, the τ_2 decay component was used for TRPL analysis [95, 97]:

$$\frac{1}{\tau_2} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_S} + \frac{1}{\tau_{drift}} \tag{3.20}$$

The recombination terms in 3.20 were investigated through the application of two models to the glass-side excitation TRPL data. First, drift was assumed to be negligible and carrier concentration distributed equally such that bulk and interface recombination could be separated according to a double heterostructure model [98, 99]:

Table 3.5: Thin CdTe τ_2 lifetimes from glass and Te-side TRPL photoexcitation.

CdTe Thickness (µm)	Glass-side Lifetime, τ_2 (ns)	Te-side Lifetime, τ_2 (ns)
0.4 ± 10%	0.3 ± 0.1	0.2 ± 0.1
0.5	0.3	0.1
0.7	0.5	0.2
0.9	0.8	0.4
1.1	1.1	0.5
1.2	1.5	0.6
1.6	1.6	0.4
2.0	2.0	0.3

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S}{d} \tag{3.21}$$

where τ_{eff} is the effective, τ_2, lifetime, d is the absorber thickness, and S is the interface recombination velocity for the MgZnO/CdTe interface. For analytical simplification, a single factor of S was used rather than $S_{front} + S_{back}$. The model was applied to the three thickest CdTe films such that drift was considered negligible, and S was attributed to S_{front}. This assumption was fairly reasonable since the 0.2-µm excitation depth into CdTe was considered sufficiently far from the back interface such that contribution from the CdTe/Te interface was judged minimal. A fit of the 1.2, 1.6, and 2.0 µm glass-side τ_2 data to Eq. 3.21 gave $\tau_{bulk} = 6 \pm 2$ ns, and $S_{front} = (6.9 \pm 1.0)$ x10^4 cm/s. For more accurate parameter determinations, measurement of true double-heterostructures would be required.

To take into account the contribution from drift, a model developed by Maiberg et al. [43] was also applied. The model was developed through simulation and analysis of voltage-dependent CIGS TRPL data and the drift-diffusion equation was solved by assuming homogeneous electric field strength and bulk properties, and a large enough electric field such

that the dark current could be neglected. They found that in the case of high injection and assuming $\tau_{b,p} \gg \tau_{b,n}$, $\tau_{b,p}^{-1} \approx 0$ (where $\tau_{b,n}$ and $\tau_{b,p}$ are bulk lifetimes for electrons and holes respectively), the drift-dependent model gives:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{b,n}} + \frac{q\left(\mu_n + \mu_p\right)}{4k_B T}\left(\frac{\Delta V}{d}\right)^2 \tag{3.22}$$

where the effect of separation of photo-excited electron-hole pairs by carrier drift in the diode field is given through the second term. μ_n and μ_p are the electron and hole mobilities, $k_B T/q$ is thermal voltage ~25 mV at room temperature, and ΔV is band bending equal to 0.2 V, determined by T. Song [100]. Because the depletion is in the lower-doped CdTe absorber, ΔV creates the diode field in the CdTe.

Eq. 3.22 predicts quadratic dependence of τ_2^{-1} on $\Delta V/d$, therefore inverse τ_2 glass-side excitation data was plotted as a function of inverse CdTe thickness and fit with a power law model, $\tau_2^{-1} = a + b(\Delta V/d)^c$. Fig. 3.20 shows that the power law fits the data quite well. Fit results were c=1.7 ± 0.9 which is close to the expected c=2, $\tau_{bulk} = 6 \pm 3$ ns, and $\mu_n + \mu_p = 23 \pm 3$ cm^2/Vs. ΔV may have an uncertainty up to ± 0.1 V, therefore a mobility range of $\mu_n + \mu_p = 10 - 100$ cm^2/Vs is reported. The validity of the drift-incorporated model is supported first by agreement between the calculated and literature-reported mobility values for polycrystalline CdTe [101–103], and second by agreement between the calculated bulk lifetimes from fits to Eqs. 3.21 and 3.22.

The power law model fits the data well across the entire absorber thickness range which suggests that the drift field significantly influences the recombination and thus decay rate for these thin CdTe structures. A dominant contribution of drift to tail lifetime, especially for the thinnest absorbers, is reasonable; in thinner absorbers band bending occurs over a narrower region which strengthens the electric field, and concomitantly drift.

An additional set of superstrates were fabricated with the same CdTe thicknesses on glass with no conducting oxide layer to minimize the field effect on charge separation. TRPL decays of these structures demonstrated the same tail lifetime trends with CdTe thickness, but the contribution from the drift term appeared to be much less important. This is

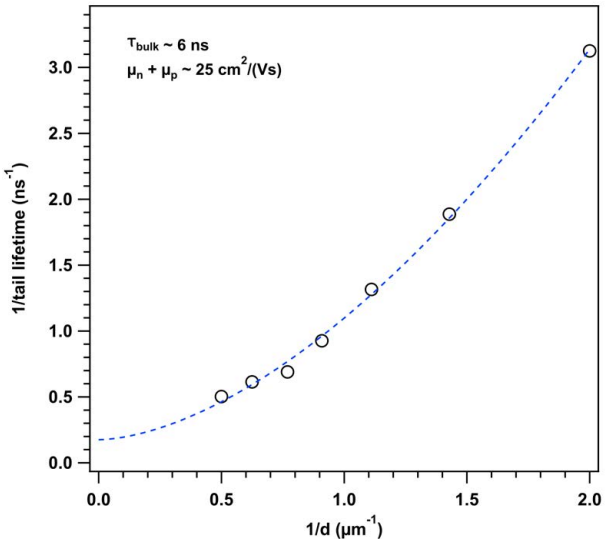

Figure 3.20: Measured TRPL tail lifetimes (open circles) and power law-modeled tail lifetimes with drift incorporation (dashed line) indicate the drift field significantly influences the decay rate in thin CdTe structures.

demonstrated in Fig. 3.21, where data for CdTe deposited on TCO show the quadratic shape attributed to drift, and data for CdTe on glass without TCO show linearity, thus minimal drift dependence. Increase in tail lifetime with CdTe thickness independent of drift effects suggests that surface recombination plays an evolutionary role in TRPL decays with CdTe thickness: recombination at the CdT/Te interface occurs more readily in thin absorbers due to the interface proximity to the front junction, and less readily for thicker absorbers where distance from the front junction is increased.

S_{back}, the interface recombination velocity for the CdTe/Te interface, was not included in the two applied models. Although a value for S_{back} could not be mathematically determined by this data set due to the complex convolution of electro-optical parameters, approximate values can be reported based on physical reasoning. As previously illustrated, τ_2 lifetimes increased with CdTe thickness for glass-side photoexcitation due to decreasing effects of S_{back}, but remained constant for Te-side photoexcitation. One can consider a CdTe absorber of infinite thickness such that S_{back} does not contribute to the TRPL decay for front-side excitation, and the TRPL decay lifetime from Te-side excitation remains constant. With

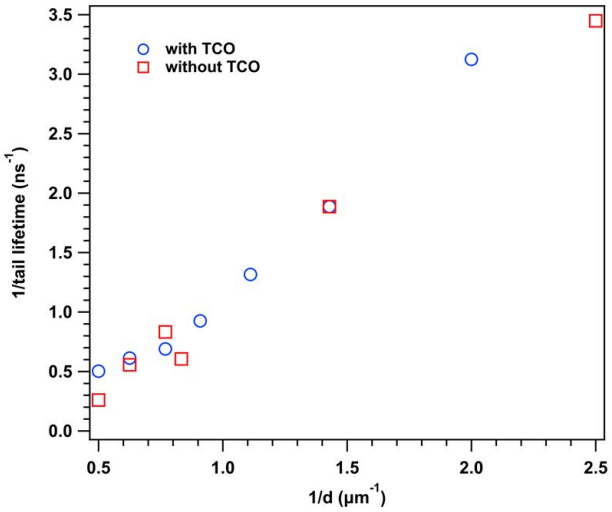

Figure 3.21: Tail lifetimes of CdTe deposited on glass with and without a TCO layer show the general trend of increased τ_2 with CdTe thickness as well as a contribution from drift which is not present without the TCO layer.

this consideration, a proportional relation between front and back-side τ_2 and surface recombination velocities can be made:

$$\frac{\tau_{2,back}^{-1}}{\tau_{2,front}^{-1}} \propto \frac{S_{back}}{S_{front}} \tag{3.23}$$

Different CdTe thicknesses and S_{front} values were used in this tail lifetime and surface recombination velocity proportionality to determine possible values for S_{back}. Based on Eq. 3.21 fit results and the range of values reported in literature [104, 105], S_{front}=1x10^4, 3x10^4, 7x10^4, and 1x10^5 cm/s were incorporated into Eq. 3.23. Measured glass-side τ_2 values were used for $\tau_{2,front}^{-1}$, and for CdTe thicknesses greater than those measured, $\tau_{2,front}^{-1}$ values were calculated from the power law fit. Te-side τ_2 values were used for $\tau_{2,back}^{-1}$ for the measured CdTe thicknesses, and because τ_2 remained approximately constant at 0.5 ns, this value was used for $\tau_{2,back}^{-1}$ for extrapolated absorber thicknesses.

Fig. 3.22 shows S_{back} versus CdTe thickness for the four S_{front} cases with the extrapolated data indicated. S_{back} leveled off for sufficiently thick CdTe absorbers, indicating the "infinite thickness" onset point. It is these values for which S_{back} are reported: 1.2x10^5,

$3.5\text{x}10^5$, $8.3\text{x}10^5$, and $1.2\text{x}10^6$ cm/s for S_{front} values of $1\text{x}10^4$, $3\text{x}10^4$, $7\text{x}10^4$, and $1\text{x}10^5$ cm/s respectively.

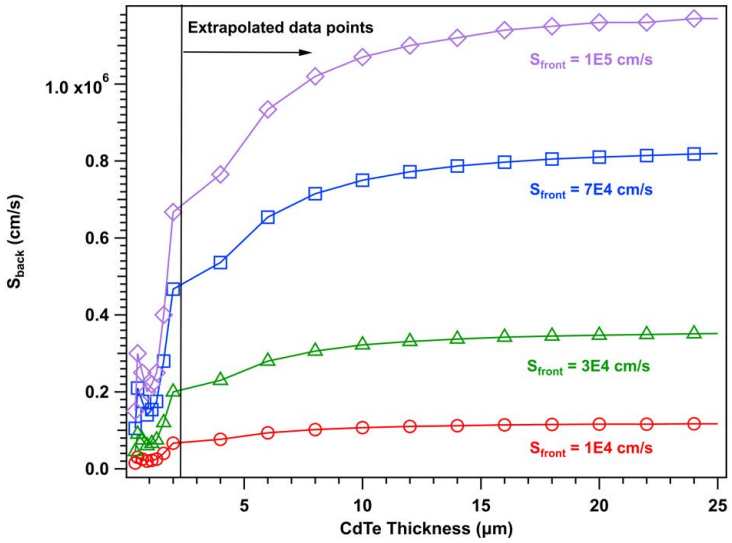

Figure 3.22: S_{back} as determined by S_{front}, a ratio of τ_2 values for glass and Te-side photoexcitation, and extrapolations to "infinite" CdTe thickness.

Given assumptions made in Eqs. 3.21 and 3.22 for fitting TRPL decay data, the electro-optical parameters are S_{front} ~$7\text{x}10^4$ cm/s for the MgZnO/CdTe interface, $10 \leq \mu_n + \mu_p \leq 100$ cm^2/Vs, and $\tau_{b,n}$ ~6 ns. Surface recombination velocity of the CdTe/Te interface could not be explicitly determined based on the data set and given models, but through physical interpretations and reasonable values of S_{front}, a range of S_{back} from $1\text{x}10^5$ to $1\text{x}10^6$ cm/s was determined. Although this range for S_{back} is in good agreement with values reported in literature [102, 106], a more precise value for S_{back} as well as S_{front} could be determined through additional modeling and judicious experimental design such as voltage, wavelength, injection, or temperature-dependent TRPL, and two-photon excitiation TRPL.

Since the CdTe/Te interface has a higher surface recombination velocity than the MgZnO/CdTe interface, it is worth understanding this interface in somewhat more detail. Song et al. showed improvement in CdTe device performance with the incorporation of a thin Te layer at the back due to reduced band bending at the back contact with Te present [55]. However, TRPL measured with front-side excitation on Tec10/100-nm MgZnO/1.0-µm CdTe with no

intentional Cu doping and Te thickness varied from 0 to 60 nm, showed a decrease in tail lifetime with the addition of Te to the back of CdTe. These decays are given in Fig. 3.23 and showed that although varied Te thickness did not have a notable effect on TRPL lifetime for a 20-60 nm thickness range, the presence of Te at the back did change the lifetime: deposition of Te on CdTe reduced the τ_2 lifetime from 1.8 $\pm$ 0.05 ns to 1.1 $\pm$ 0.05 ns. This suggests that Te changes bulk properties.

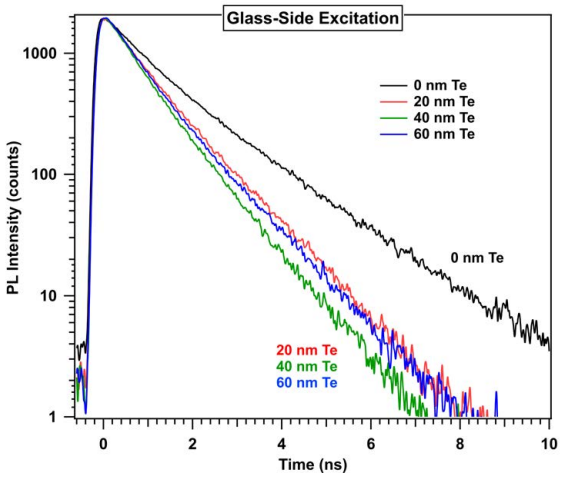

Figure 3.23: TRPL decays measured with photoexcitation from the glass side for varied Te thicknesses.

Previous examination of effects of CdTe stoichiometry on TRPL lifetime demonstrated a decrease in minority carrier lifetime due to increased surface recombination velocity in Te-rich CdTe films [106, 107]. In HSE06 calculations, the Te antisite (Te_{Cd}) and interstitial (Te_i) defects are more energetically favorable than tellurium vacancies (V_{Te}) under Te-rich conditions, and are the deep level defects which were shown to limit minority-carrier lifetime [107]. This suggests that incorporation of the Te layer behind CdTe creates a Te-rich layer and introduces Te_{Cd} defects and/or Te_i defects, and subsequently reduces the minority carrier lifetime. However, the minority carrier lifetime was only somewhat reduced with a Te layer in these structures and seems not to be a limiting performance mechanism since device performance is enhanced with a Te layer at the back [55].

Chapter 4

INCORPORATION OF CdSeTe INTO THIN CdTe ABSORBERS

One of the touted advantages of CdTe technology is that its ∼1.5-eV band gap is well-matched to the standard AM 1.5G solar spectrum. However, for band gaps as low as ∼1.4 eV, there is an associated potential improvement in J_{SC} large enough to offset the V_{OC} and fill factor losses linked to a reduced band gap for an overall device efficiency increase [20]. Band-gap reduction in CdTe-based materials has been demonstrated through selenium alloying, achievable with various fabrication methods including CSS, thermal evaporation, sputtering, and molecular beam epitaxy (MBE) [108–113]. Through the incorporation of a ∼1.4-eV band gap cadmium selenium telluride (CdSeTe) alloy layer in front of the CdTe, significant efficiency improvements in CdTe photovoltaic devices have been achieved, attributed to increased J_{SC} [109, 110, 114–116]. The narrower band-gap CdSeTe preceding CdTe, where the majority of the band offset occurs in the conduction band [117], increases the fraction of incident photons absorbed at low energies, and improves current collection without sacrificing the built-in voltage at the back of the device, shown in the CdTe and CdSeTe/CdTe band diagrams in Figs. 4.1 (a) and (b) respectively. Voltage deficit reduction in CdSeTe/CdTe compared to CdTe devices has also been demonstrated, and is attributed to Se passivation of bulk defects [118]. Increased photovoltaic efficiency with CdSeTe incorporated into CdTe structures has only been demonstrated for absorber thicknesses greater than 4 µm with purposeful inter-diffusion of the CdSeTe and CdTe [109, 110, 114]. This chapter presents the improvements in J_{SC}, V_{OC} deficit, fill factor, and efficiency (highlighted in Fig. 4.2) for thin, 1.5-µm CdSeTe/CdTe bilayer devices through fabrication optimization, material studies, and electronic and electro-optical analyses.

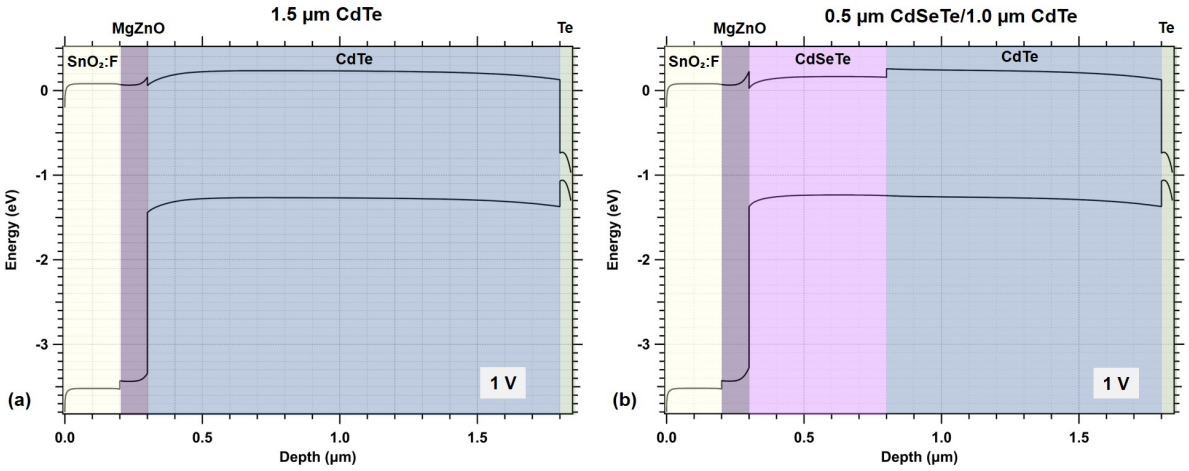

Figure 4.1: (a) 1.5-µm CdTe and (b) 1.0-µm CdSeTe/1.0-µm CdTe band diagrams from SCAPS simulations.

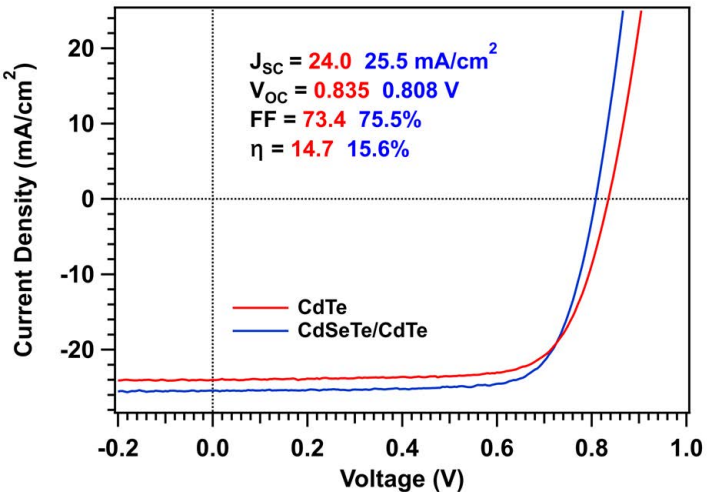

Figure 4.2: 1.5-µm CdSeTe/CdTe and CdTe device J-V curves show the performance increase with the addition of CdSeTe to the absorber, notably through improved J_{SC}.

4.1 Band-Gap Dependence of Performance Parameters

The decrease in semiconductor band gap with the introduction of CdSeTe into CdTe absorbers should have direct and quantifiable effects on V_{OC}, J_{SC}, and fill factor since ideal performance parameters are band-gap dependent, as illustrated in Fig. 4.3 from R. Geisthardt [34].

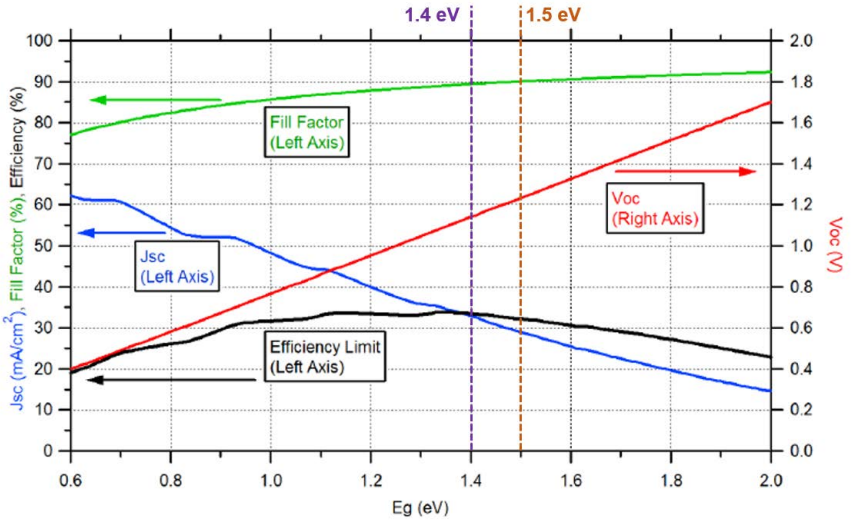

Figure 4.3: J-V performance parameters as a function of absorber band gap for standard test conditions. From Ref. [34].

The ideal open circuit voltage is given by a rearrangement of the standard diode equation at zero current, where parasitic resistances are ignored given the idealized case:

$$V_{OC,ideal} = \frac{kT}{q} ln \left(\frac{J_{SC,ideal}}{J_{0,ideal}} + 1 \right) \tag{4.1}$$

where k is the Boltzmann constant, T is the temperature, $J_{SC,ideal}$ is the ideal short circuit current density, and $J_{0,ideal}$ is the ideal saturation current density. $J_{SC,ideal}$ is determined by the condition that every incident photon with energy greater than the band gap is converted into an electron. Thus, $J_{SC,ideal}$ depends on the photon flux density of sunlight: the solar spectral irradiance density (photons/cm^{2}s) at a given wavelength divided by the individual

photon energy [21]. $J_{SC,ideal}$ for a given material band gap is calculated by integration from zero to a maximum wavelength which corresponds to the material band gap:

$$J_{SC,ideal} = q \int_0^{\lambda_G} N_{ph}(\lambda) d\lambda \tag{4.2}$$

where q is the elementary charge, λ_G is the band gap wavelength, and $N_{ph}(\lambda) = \lambda P(\lambda)/hc$, the spectral photon flux density, dependent on the solar spectral irradiance density, $P(\lambda)$.

$J_{0,ideal}$ can be calculated through thermodynamic considerations: a solar cell can be approximated as a black body which emits radiation through the recombination of electrons and holes, and given J_0's dependence on recombination, $J_{0,ideal}$ can be represented in the form of a black body [34, 82, 119]. Planck's law of black body radiation is given by:

$$B(\lambda, T) = \frac{2hc^2}{\lambda^5} \frac{1}{e^{\frac{hc}{\lambda kT}} - 1} \tag{4.3}$$

where B is the spectral power per unit area for particular radiation frequencies (photons/ cm^2s), h is Planck's constant, c is the speed of light, k is the Boltzmann constant, and T is temperature. Given the temperature and wavelength range in which solar cells radiate, $e^{\frac{hc}{\lambda kT}} \gg 1$ such that to good approximation,

$$\Phi_{BB}(\lambda, T) = \frac{2c}{\lambda^4} e^{\frac{-hc}{\lambda kT}} \tag{4.4}$$

where Φ_{BB} is the black body flux density, calculated by the approximated black body spectral density at a given wavelength divided by the energy of an individual photon at said wavelength.

Thus $J_{0,ideal}$ is given by:

$$J_{0,ideal} = q \int_0^{\lambda_G} \frac{4\pi c}{\lambda^4} e^{\frac{-hc}{\lambda kT}} d\lambda \tag{4.5}$$

where a factor of 2π was introduced to take into account the steradian units of a black body spectra; radiation from a solar cell is assumed to be half of a sphere, or a solid angle of 2π sr. Equation 4.5 can be analytically integrated to give

$$J_{0,ideal} = \frac{4\pi q\,(kT)^3}{h^3c^2}\Big[\frac{(E_g/kT)^2 + 2\,(E_g/kT) + 2}{e^{E_g/kT}}\Big] \tag{4.6}$$

where the band-gap wavelength was substituted by the band-gap energy, E_g.

Therefore the ideal V_{OC} is given by:

$$V_{OC,ideal} = \frac{kT}{q} ln\left(\frac{\int_0^{\lambda_G} N_{ph}(\lambda)d\lambda}{\int_0^{\lambda_G} \frac{4\pi c}{\lambda^4} e^{\frac{-hc}{\lambda kT}} d\lambda} + 1\right) \tag{4.7}$$

,

and has an indirectly proportional relationship with band gap.

The ideal fill factor dependence on band gap is given by Eq. 3.2.

4.2 CdSeTe Fabrication Conditions for Thin Absorbers

CdSeTe was incorporated into the CdTe superstrate structure as a lower band-gap p-type polycrystalline absorber layer between the MgZnO emitter and CdTe layers, as shown in the device structure in Fig. 4.4. For suitable CdSeTe film growth, the Tec10/100-nm MgZnO substrate temperature was raised to ∼540 °C (compared to the ∼480 °C substrate temperature for CdTe deposition) prior to CdSeTe sublimation. CdSeTe was CSS-deposited from a $CdSe_xTe_{1-x}$ source, where band gap is controlled by the molar fraction of CdSe in the source material. Co-sublimation from a CdTe and Se source, where band gap is controlled by selenium flux, is also viable but was not explored in the thin bilayer-absorber studies because co-sublimation produced lower-performing devices compared to single-source sublimation [108]. Top and bottom CdSeTe source temperatures were fixed at 420 °C and 545 °C respectively with sublimation from a CdSeTe source with 20% CdSe unless otherwise indicated, and the CdSeTe thickness was controlled by sublimation time.

Deposition of CdSeTe in the same in-line vacuum system as the CdTe and post-deposition $CdCl_2$ treatment promotes two favorable material properties: a high-quality CdSeTe/CdTe-transitional interface, and band grading control through thermally-driven inter-diffusion of the CdSeTe and CdTe. In the first case, to identify microstructural changes associated

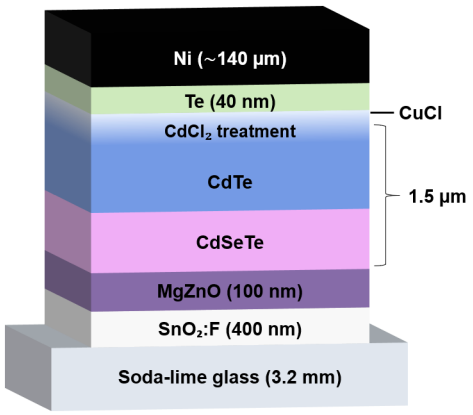

Figure 4.4: CdSeTe/CdTe device structure with a thin, 1.5-µm bilayer absorber.

with the incorporation of CdSeTe, STEM imaging was performed on a FIB-prepared 0.5-µm CdSeTe/1.0-µm CdTe absorber structure with no Ni back contact layer. The bright field STEM image, given in Fig. 4.5 (a) showed that the deposition of CdSeTe did not seem to alter the MgZnO emitter layer: the MgZnO is continuous and conformal with the CdSeTe layer across the imaged cross-section, similar to MgZnO/CdTe, presented in Chapter 3, Fig. 3.5. The thin-absorber grain structure indicated no obvious grain formation differences between the CdSeTe and CdTe layers. The absorber grains were fairly large, and the CdSeTe grain sizes were similar to those measured in thicker (greater than 4 µm) CdSeTe/CdTe absorbers [109, 114, 118]. This could suggest that CdSeTe grain growth may be limited independent of CdSeTe thickness, although grain growth-specific material studies would be needed to evaluate this. The presence of the CdSeTe layer was verified with EDX maps and line scans, the latter of which is given in Fig. 4.5 (b). The line scan, measured from the Te layer (top) to MgZnO layer (bottom) and indicated by the yellow dashed line in Fig. 4.5 (a), showed that selenium extended ∼0.5 µm into the absorber layer, in agreement with the measured as-deposited CdSeTe film thickness, and replaced a fraction of the Te within that layer as expected.

Inter-diffusion of the CdSeTe and CdTe layers can be accomplished through thermally-driven processes initiated after absorber deposition, and the extent of diffusion has been assessed in various studies [109, 114, 118]. For the CSS structures discussed here, the $CdCl_2$

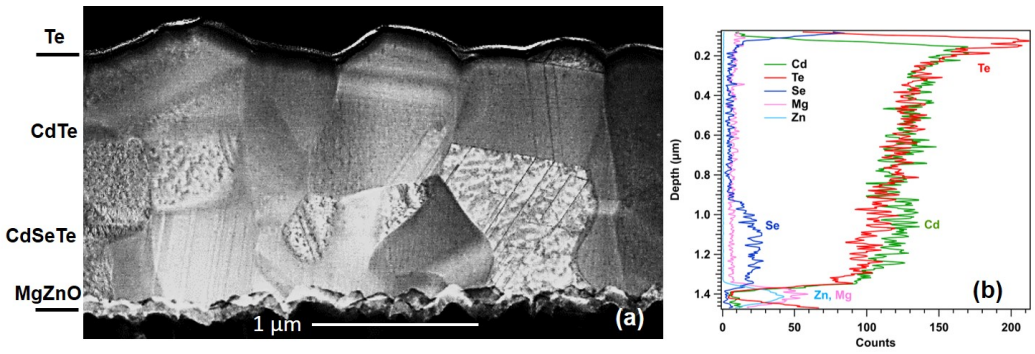

Figure 4.5: (a) Bright-field STEM image of the CdSeTe/CdTe structure shows fairly large absorber grains, and the EDX line scan (yellow dashed line in STEM image) verifies the incorporation of selenium (b).

anneal step serves this purpose in addition to its principle function of driving the $CdCl_2$ into the CdTe material for absorber passivation. To characterize effects of CdSeTe/CdTe inter-diffusion on thin bilayer device performance, $CdCl_2$ anneal time was varied on 0.5-µm CdSeTe/1.0-µm CdTe devices with fixed, previously optimized $CdCl_2$ dose (150-seconds) and Cu treatments (5 seconds CuCl dose, 250-second anneal). The J-V parameter box plot results are given in Fig. 4.6 for anneal times of 180-480 seconds in 60-second increments. The J-V parameters were generally poorest at the anneal extrema, which may indicate inadequate $CdCl_2$ annealing and/or selenium diffusion for shorter times, or over-annealing and/or selenium diffusion for longer times. Since both processes are encompassed by the $CdCl_2$ anneal step, these data alone are insufficient to decouple the two. To quantify the diffusion process, one could perform heat treatments on as-deposited CdSeTe/CdTe absorbers, and analyze material effects. Given the focus of this study on device performance optimization, which requires a $CdCl_2$ treatment, this was not examined for these structures. Although there were no strong trends in J-V parameters in Fig. 4.6 as a function of $CdCl_2$ anneal time, a 240-second anneal time demonstrated the highest efficiencies and was selected for thin CdSeTe/CdTe device fabrication.

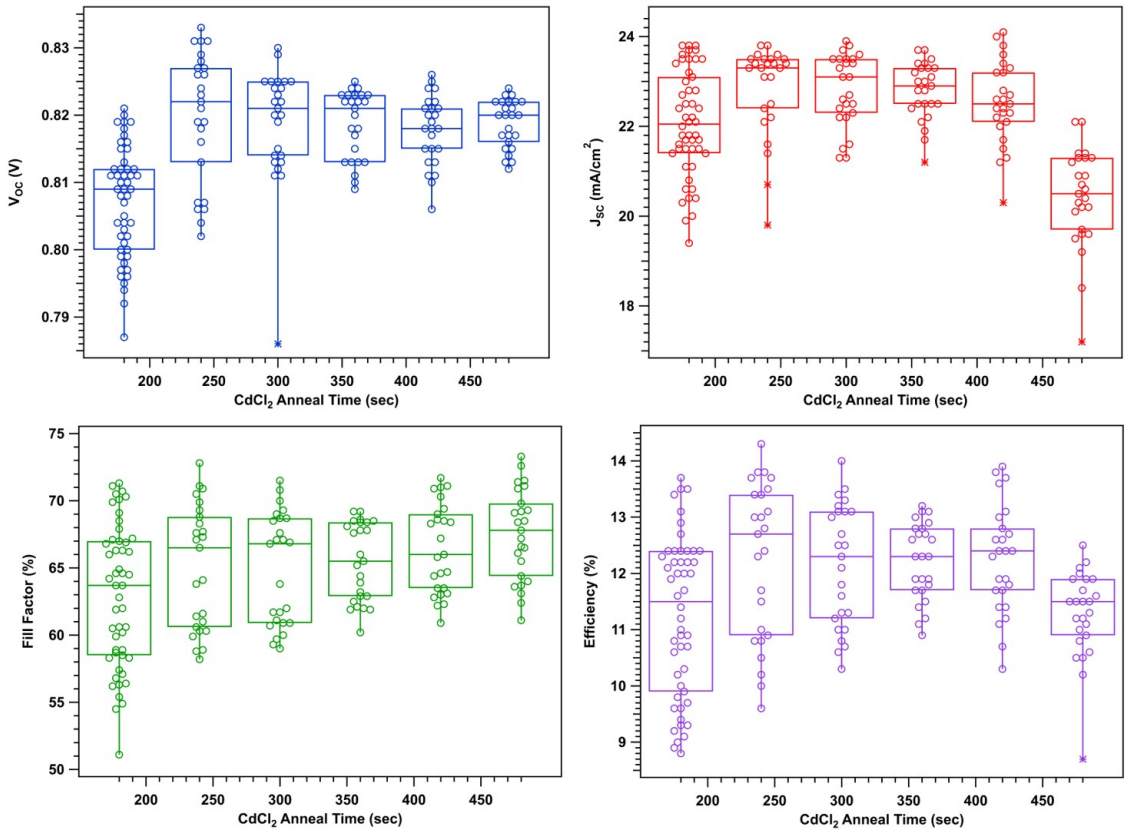

Figure 4.6: J-V parameter box plots of $CdCl_2$ anneal time variation on 0.5-µm CdSeTe/1.0-µm CdTe devices. Each anneal time encompasses 25 devices except for the 180 second anneal, which encompasses 50 devices.

The extent of CdSeTe and CdTe inter-diffusion and confirmation of Se incorporation were examined through TOF-SIMS measurements on a 0.5-µm CdSeTe/1.0-µm CdTe film structure with optimal $CdCl_2$ and Cu treatments and no Ni back contact. The SIMS elemental profiles are given in Fig. 4.7 where the labeled elements correspond to the most abundant isotope except for Se, for which ^{78}Se+ was used to eliminate a mass overlap with ZnO+. Material layer boundaries are included based on measured film thicknesses and STEM and EDX data. The Se profile was fairly symmetric with the majority of the signal in the deposited CdSeTe layer and some extension into the CdTe layer. With the corresponding decrease in the Te:Cd ratio, this verified that the CdSeTe was incorporated into the front of the film structure as intended, and suggested that the amount of selenium diffusion into the CdTe was fairly minimal. Although the transition from the CdSeTe to CdTe layer was not abrupt, it was sufficiently narrow such that the term bilayer is appropriate to describe the absorber.

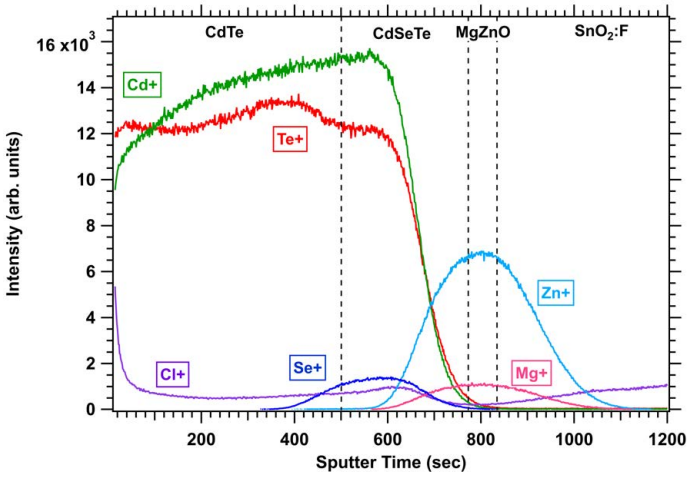

Figure 4.7: TOF-SIMS elemental profiles of 0.5-µm CdSeTe/1.0-µm CdTe show limited Se diffusion into the CdTe and minimal Mg or Zn diffusion into the absorber.

The Mg and Zn profiles in Fig. 4.7 appeared artificially wide because the sputter rate of oxides is slower than that of the absorber material. Therefore the symmetry of the profiles were used to characterize the extent of diffusion into the absorber layer: both Mg and Zn peaks were fairly symmetric, suggesting that minimal diffusion into the absorber occurred.

4.3 Optimization of CdSeTe:CdTe Thickness Ratio

SCAPS-simulated J-V curves of 1.5-µm CdSeTe/CdTe devices with varied CdSeTe and CdTe thicknesses, given in Fig. 4.8, demonstrate that the thickness of the CdSeTe and CdTe absorber layers is an important parameter which impacts device performance. The simulated data indicate that J_{SC} and V_{OC} should be the parameters most dependent on CdSeTe/CdTe thicknesses. There is a predicted increase in J_{SC}, primarily with initial CdSeTe incorporation, and a predicted V_{OC} decrease, most significant for a CdSeTe-only absorber. The resultant efficiency dependence on CdSeTe/CdTe thickness motivates an investigation of the effects of these absorber thicknesses on device properties.

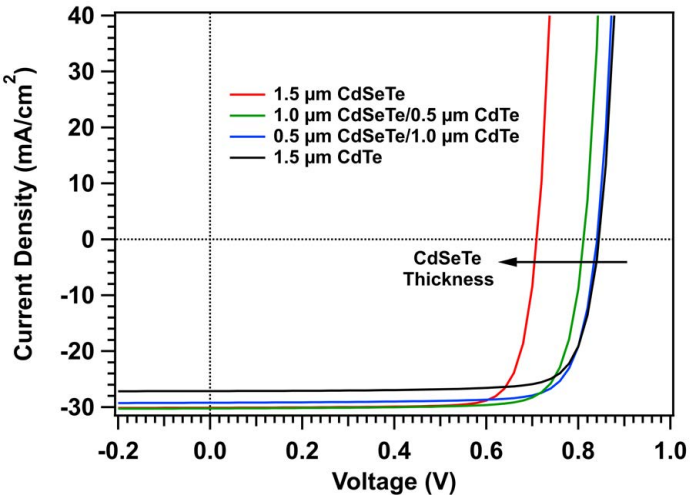

Figure 4.8: SCAPS-simulated J-V data show a decrease in V_{OC} for the greater CdSeTe:CdTe thickness ratio and a corresponding lower efficiency.

To optimize the CdSeTe:CdTe thickness ratio in thin devices, CdSeTe/CdTe absorber devices were fabricated with CdSeTe thickness varied from 0 to 1.5 µm in 0.25-µm increments, with a corresponding change in CdTe thickness such that the total absorber thickness was fixed at 1.5 µm. As the lower band gap CdSeTe constitutes a greater percentage of the absorber thickness, a corresponding decrease in absorber band gap is expected. PL and QE measurements of the best-performing CdSeTe/CdTe thickness devices were used to determine the approximate band gap of each device, and are given in Figs. 4.9 (a) and (b)

respectively. Both the PL emission spectra and QE data demonstrated a shift to lower apparent band gap from ∼1.5 to 1.44 eV with increased CdSeTe:CdTe thickness ratio, where the most pronounced shift occurred for initial incorporation of CdSeTe. PL emission data also demonstrated a general increase in luminescence intensity with greater CdSeTe incorporation, which suggests that CdSeTe reduces defect-mediated radiative recombination and is a more radiatively efficient material than CdTe.

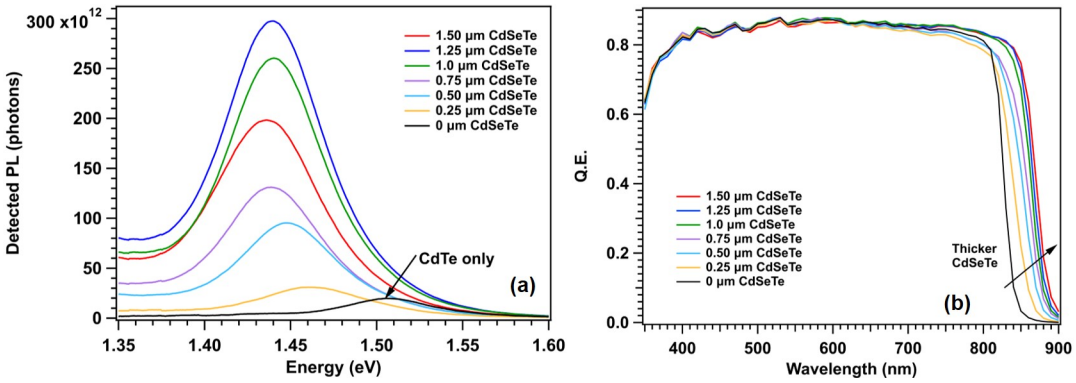

Figure 4.9: PL (a) and QE (b) of best-performing CdSeTe/CdTe thickness devices demonstrate a shift to narrower band gap for a greater CdSeTe:CdTe ratio.

A comparison of the approximate band gaps determined by PL and QE are given as a function of CdSeTe thickness in Fig. 4.10. Band gap uncertainties were approximated based on ∼0.2-µm lateral variation in CdSeTe/CdTe thickness across the device. The band gaps from PL were determined by applying a Gaussian fit to the peak-portion of the data, and the band gaps from QE data were determined by the energy of maximum $|dQE/d\lambda|$. The estimated band gaps demonstrated a clear decrease for thicker CdSeTe, and fairly good agreement, with band gaps determined from PL slightly larger than those determined from QE. Band gaps from PL may be wider because the photoluminescence may not exactly correspond to the band-to-band transition, and the separation of energy levels may not be constant with CdSeTe thickness variation. Band gaps determined by QE are more appropriate for solar-cell analysis, and are employed for band gap-based analysis of devices in this work.

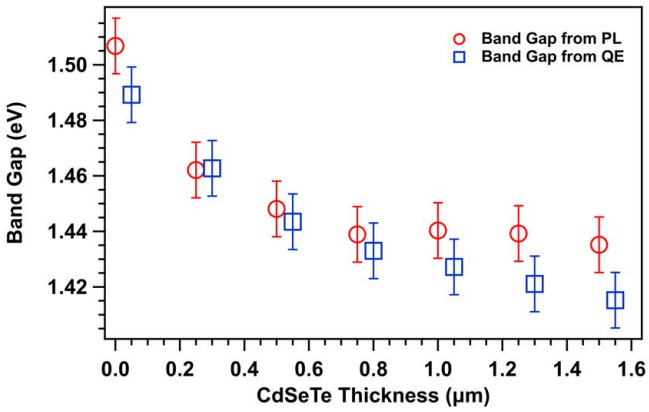

Figure 4.10: Band gaps from PL compared to QE for varied CdSeTe:CdTe thickness ratio shows narrower band gaps for greater CdSeTe thickness contribution and relatively good agreement between the two determination methods.

The J-V curves for selected best-performing devices are given in Fig. 4.11, and the parameters for all best-performing devices are listed in Table 4.1. As SCAPS modeling suggested, V_{OC} demonstrated the greatest dependence on CdSeTe:CdTe thickness ratio and showed consistent reduction with increased thickness ratio, from 837 mV to 755 mV for the 1.5-µm CdTe and 1.5-µm CdSeTe devices respectively. This 82-mV V_{OC} decrease is consistent with the ∼75 meV band gap reduction determined by QE. Measured V_{OC} reduction with increased CdSeTe:CdTe thickness ratio and concomitant band gap shift mirrored ideal V_{OC} band gap dependence as shown in Fig. 4.12, where ideal V_{OC} was determined by Eq. 4.7. The differential between ideal and measured V_{OC} was consistently ∼350 mV, which indicates that the voltage deficit of the CdSeTe/CdTe devices was not CdSeTe/CdTe thickness dependent.

J_{SC} increased with initial incorporation of CdSeTe as expected for a narrowed band gap, but demonstrated no additional improvement beyond a 1:1 CdSeTe:CdTe thickness ratio. This suggests there exists an upper limit of CdSeTe thickness beyond which the CdSeTe contributes no additional photon conversion. Fill factor was highest for 0.5-µm CdSeTe/1.0-µm CdTe, and decreased for both thicker and thinner CdSeTe layers. Fill factor dependence on CdSeTe/CdTe thickness will be discussed in greater detail below. For best performance,

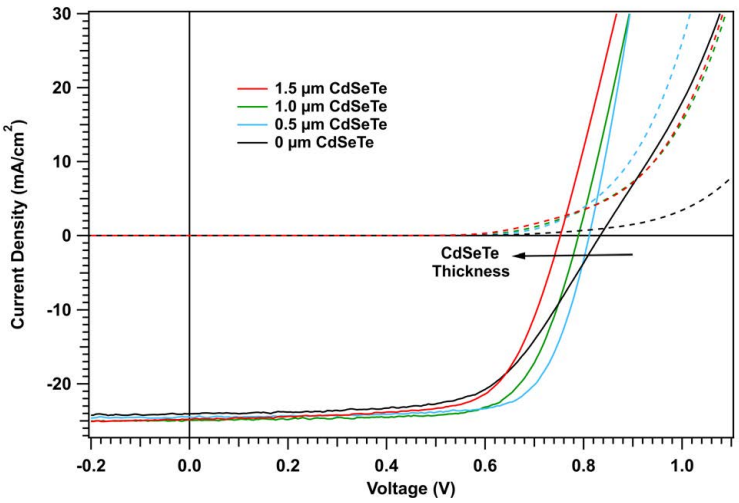

Figure 4.11: J-V curves of best-performing 1.5-µm absorber devices (1.5, 1.0, 0.5, and 0 µm CdSeTe) demonstrate a shift in V_{OC} and J_{SC}.

the data indicated that 1.5-µm CdSeTe/CdTe bilayer absorber devices only required 0.5 µm of CdSeTe.

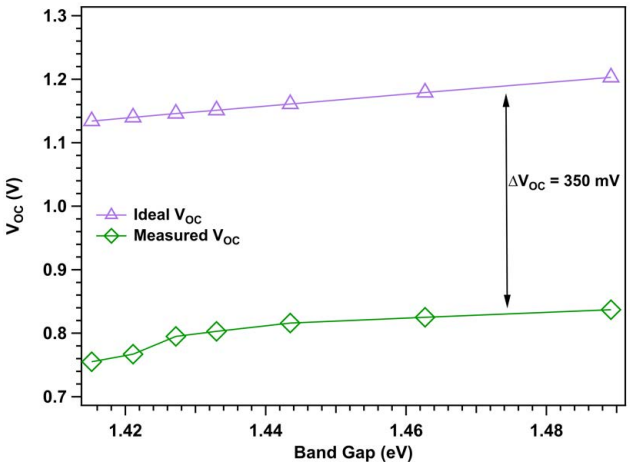

Figure 4.12: Ideal and measured V_{OC} demonstrate the same dependence on band gap with a 350-mV offset which corresponds to the voltage deficit in the devices.

To determine whether the optimal CdSeTe/CdTe thickness ratio was dependent on the CdSeTe material band gap, identical thickness variation experiments were performed utilizing narrower band gap CdSeTe layers; the CdSeTe band gap was lowered via sublimation from 30% and 40% CdSe source material. Box plots of the J-V parameters for the 20, 30, and

Table 4.1: J-V parameters of best-performing 1.5-µm CdSeTe/CdTe devices with varied CdSeTe and CdTe thicknesses.

CdSeTe Thickness (µm)	CdTe Thickness (µm)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
1.50	0.0	0.755	25.0	68.0	12.7
1.25	0.25	0.767	24.9	72.2	13.6
1.0	0.50	0.795	25.0	72.2	14.2
0.75	0.75	0.803	25.1	73.7	14.8
0.50	1.0	0.816	24.4	74.1	14.7
0.25	1.25	0.825	24.0	71.2	14.0
0.0	1.50	0.837	24.1	62.1	12.5

40% CdSe source compositions as a function of CdSeTe thickness are given in Fig. 4.13, where extreme outlier data points were removed.

Generally, the trend in each J-V parameter as a function of CdSeTe thickness was similar independent of CdSe source composition. The V_{OC} decreased with increased CdSeTe thickness, and the J_{SC} increased asymptotically, with both parameter changes due to the band-gap shift caused by the altered thickness ratio. The fill factor demonstrated an optimal thickness range of 0.25-0.75 µm of CdSeTe, and fair variation in fill factors for thicker CdSeTe. Device efficiency data demonstrated a similar trend; 0.5-µm CdSeTe/1.0-µm CdTe was generally the best-performing, and notable performance deterioration occurred in devices with absorber thickness comprised of more than 50% CdSeTe. Devices fabricated with 40% CdSe source material demonstrated the lowest performance due primarily to low fill factors, and a fair amount of variation in both V_{OC} and fill factor at each CdSeTe thickness. Because of their wider band gap, 20% CdSe source material devices demonstrated higher V_{OC} and lower J_{SC} values across the thickness range compared to 30% and 40% CdSe devices. The fill

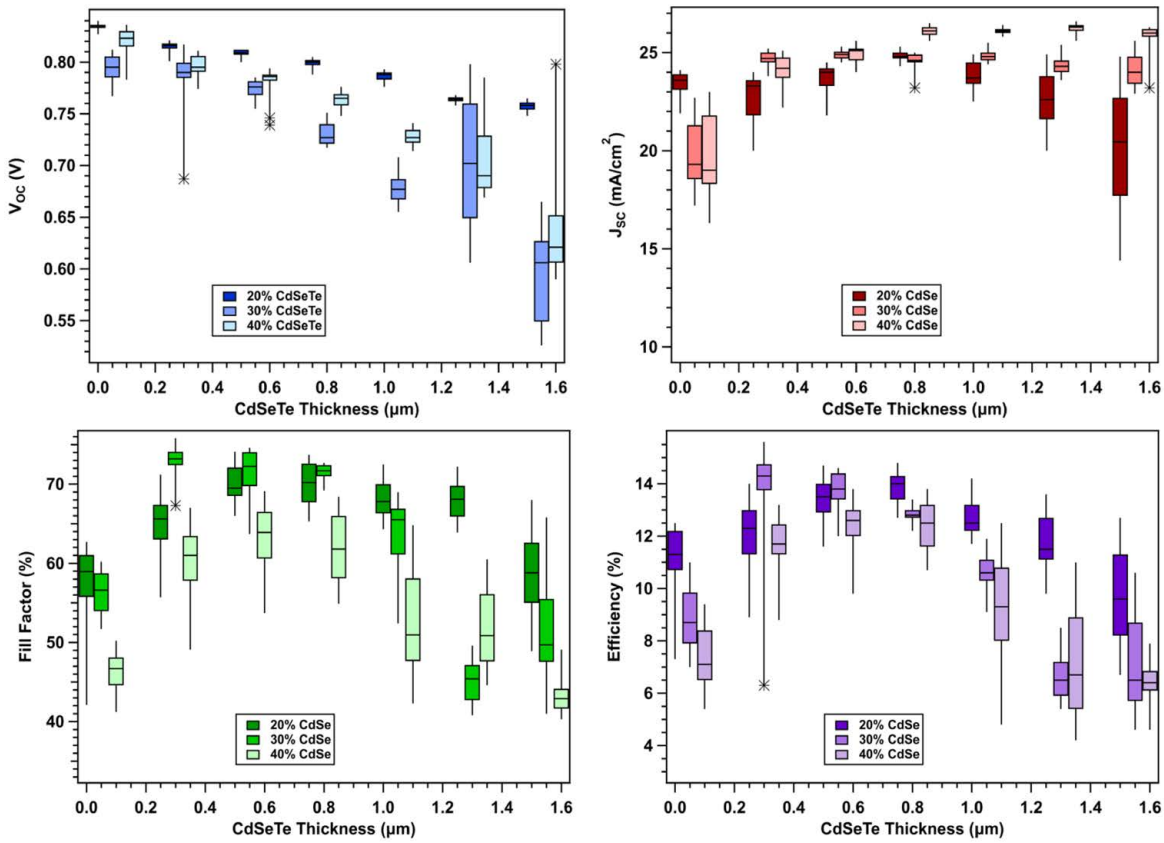

Figure 4.13: J-V parameter box plots for varied CdSeTe/CdTe thickness ratios with 20, 30, and 40% CdSe source material compositions. Extreme outlier data points (fewer than 8 total) were removed.

factors of 20% CdSe source material devices were generally higher than or comparable to the 30% CdSe device fill factors across the entire CdSeTe thickness range. Although 30% CdSe source composition gave the single best-performing device, 20% CdSe source composition device efficiencies were comparable, demonstrated the highest V_{OC}, and excellent substrate uniformity. Since this work is focused on performance enhancement through reduced voltage deficit, optimized CdSeTe/CdTe devices were fabricated with 0.5 µm CdSeTe from 20% CdSe source material and 1.0 µm CdTe.

Fill factor losses were analyzed on the $CdSe_{0.2}Te_{0.8}$/CdTe thickness devices from Table 4.1 using the method from R. Geisthardt described in Chapter 3 [20, 34]. Since the band gap narrowed for thicker CdSeTe, the ideal fill factor decreased from 89.6% to 89.3% according to Eq. 3.2, where band gaps determined from QE measurements were used to calculate ideal fill factor. The losses are shown as a function of CdSeTe thickness in Fig. 4.14 and the corresponding values are given in Table 4.2. The 1.5-µm CdTe device with no CdSeTe could not be reliably analyzed due to large series resistance, and is therefore not included in the data. The non-ideal diode quality factor contributed to fill-factor loss primarily through the reduced voltage, and the A-factor loss component decreased consistently for thicker CdSeTe. Series resistance and V_{OC} reduction constituted the majority of fill factor losses across all CdSeTe thicknesses, and increased slightly for thicker CdSeTe. Therefore despite improved diode quality factor for thicker CdSeTe layers, overall fill-factor loss was minimized for the 0.5-µm CdSeTe/1.0-µm CdTe absorber device.

4.4 Effects of Fabrication Temperature on CdSeTe Properties

Fabrication temperatures in CSS depositions can have a large effect on material properties and device characteristics, which have been well-documented for a variety of materials (CdTe, $CdCl_2$, CdMgTe, and CdSeTe deposited by co-sublimation) [56, 76, 96, 108, 120–123]. In this section, the effects of independent variation in the CdSeTe bottom (source) and top heater temperatures are presented for CdSeTe films and 0.5-µm CdSeTe/1.0-µm CdTe devices with 20% CdSe source composition.

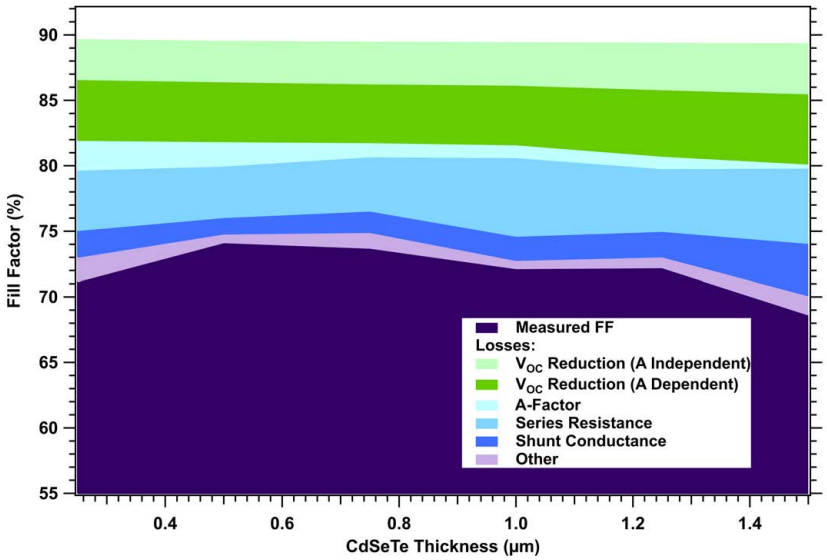

Figure 4.14: Fill factor losses for varied CdSeTe:CdTe thickness ratio with absorber thickness fixed at 1.5 µm. Series resistance and V_{OC} reduction losses are the greatest contributions to fill factor loss.

4.4.1 $CdSe_{0.2}Te_{0.8}$ Source Temperature Variation

Material Characterization

To understand CdSeTe material properties associated with a change in $CdSe_{0.2}Te_{0.8}$ source temperature, ~1.5 µm CdSeTe films were fabricated on Tec10/100-nm MgZnO substrates with a fixed top heater temperature of 420 °C and bottom temperatures of 525, 535, 545, 555, and 565 °C. After CdSeTe deposition the plates were cleaved in half; one half received the optimized $CdCl_2$ treatment while the other remained as-deposited CdSeTe to examine effects of $CdCl_2$ treatment on CdSeTe material. Although a vacuum break was introduced before the $CdCl_2$ treatment unlike the in-line device fabrication process, the $CdCl_2$-treated CdSeTe films showed some $CdCl_2$ residue which indicated that the films received sufficient $CdCl_2$ such that differences between as-deposited and $CdCl_2$-treated CdSeTe could be determined.

SEM images for the as-deposited and $CdCl_2$-treated 1.5-µm CdSeTe films are given in Fig. 4.15 for each of the source temperatures. The films were imaged with 10-kV accelerating

Table 4.2: Fill factor losses for CdSeTe:CdTe thickness ratio devices.

	% Fill Factor					
	CdSeTe Thickness (µm)					
Mechanism	**0.25**	**0.5**	**0.75**	**1.0**	**1.25**	**1.5**
V_{OC} Red. (A Independent)	3.0	3.1	3.2	3.2	3.5	3.8
V_{OC} Red. (A Dependent)	4.6	4.6	4.5	4.6	5.1	5.4
A Factor	2.3	1.9	1.1	1.0	0.9	0.3
Series Resistance	4.6	3.9	4.1	6.0	4.8	5.8
Shunt Conductance	2.0	1.3	1.6	1.8	1.9	4.0
Other	1.9	0.7	1.2	0.6	0.8	1.5
Measured Fill Factor	**71.2**	**74.1**	**73.7**	**72.2**	**72.2**	**68.6**

voltage, 10-mm working distance, and 50,000x magnification, and the samples were coated with 15 nm of gold to minimize charging from the glass during imaging.

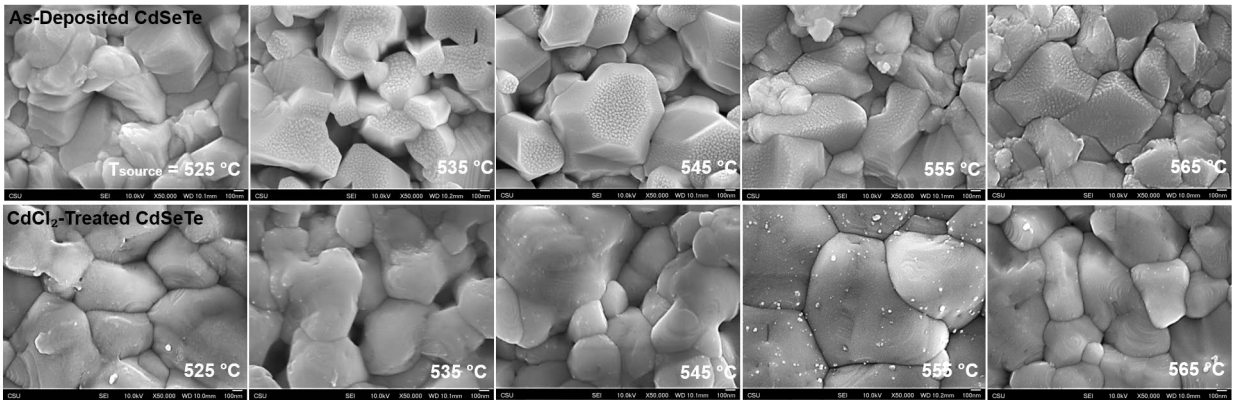

Figure 4.15: SEM images of as-deposited and $CdCl_2$-treated 1.5-µm CdSeTe films with varied CdSeTe source temperature.

The CdSeTe films showed a slight increase in grain size and enhanced coalescence after $CdCl_2$ passivation, a feature also observed in completed CdSeTe/CdTe structures [124]. Post-passivation grain coalescence seemed somewhat greater for higher source temperatures

which may suggest temperature-dependent nucleation and growth properties in CdSeTe. At all temperatures, the as-deposited grains exhibited bubble-like features which disappeared after $CdCl_2$ treatment. EDX mapping and line scan analyses of these regions indicated no elemental variation with the features, and these features cannot presently be attributed to a specific mechanism or material formation. The small bright features which appeared most prominently on the $CdCl_2$-treated 555 °C film were also analyzed with EDX line scans and no detectable elemental differentiation was measured between the feature and the surrounding grain.

Elemental atomic compositions of the CdSeTe source temperature films were determined through EDX analysis, and are given in Figs. 4.16 (a) and (b) for as-deposited and $CdCl_2$-treated films respectively. $CdCl_2$ treatment and CdSeTe source temperature did not appear to alter elemental composition: for as-deposited and $CdCl_2$-treated films, the Cd composition was ∼50%, Te ∼42%, and Se ∼6% independent of source temperature. The Cd/Te composition differential was associated with Se substitution, as expected from the reduced Te composition in the alloy source material. Se composition in the films was less than the 20% composition of the source material, which suggests that elemental flux from the source material is unequal during sublimation.

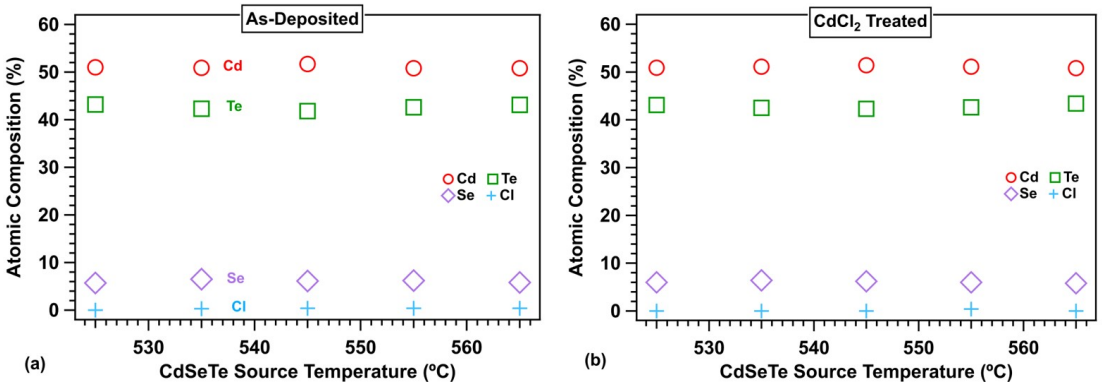

Figure 4.16: Elemental compositions of as-deposited and $CdCl_2$-treated CdSeTe films deposited by 20% CdSe source material with varied CdSeTe source temperature. Se substitutes for Te as expected and there is little change in elemental composition with source temperature.

To investigate band-gap dependence on CdSeTe source temperature, approximate optical band gaps were determined by the Tauc plot method, which relies on measured film transmission [125]. A generalized expression from Tauc's germanium and silicon-based analysis can be used to determine the optical band gap of a material [126]:

$$\Big(\alpha(h\nu)h\nu\Big)^{1/r} = C(h\nu - E_g) \tag{4.8}$$

where $h\nu$ is the energy of incident light, C is a material-related constant, E_g is the optical band gap, $\alpha(h\nu)$ is the optical absorption coefficient, and r denotes the nature of the transition [127]. For direct, allowed transitions, as is the case for CdSeTe, r = 1/2. Neglecting reflection, the optical absorption coefficient was determined by:

$$\alpha(h\nu) = \frac{1}{t} ln \left(\frac{1}{T}\right) \tag{4.9}$$

where t is the film thickness and T is transmission. A judicious graphical representation of Eq. 4.8 allows for determination of approximate optical band gap: a plot of $h\nu$ on the abscissa and $(\alpha h\nu)^2$ on the ordinate should yield a linear region which denotes the absorption edge. This region can be fit and extrapolated to $\alpha = 0$ cm^{-1} (i.e. the abscissa) to yield the approximate band gap.

Transmission was measured on the as-deposited and $CdCl_2$-treated CdSeTe films with an integrating sphere to collect both direct and diffuse light, and the data are given in Fig. 4.17 (a). The as-deposited and $CdCl_2$-treated transmission data absorption edges were comparable at source temperatures of 525, 555, and 565 °C, however for 535 and 545 °C there was a measurable shift to lower energy after $CdCl_2$ treatment. This is also illustrated in the corresponding Tauc band gaps, given in Fig. 4.17 (b). As-deposited films appeared to have slightly wider band gaps than $CdCl_2$-treated films, although the difference was minimal at 525, 555, and 565 °C source temperatures. The optical band gaps were also fairly constant, ∼1.45 eV at these temperatures, consistent with band gaps determined by PL measurement, and the unchanged Se composition measured by EDX. The narrower band gaps of the 535 and 545 °C films after $CdCl_2$ suggests passivation-induced material property changes. Based

on the constant elemental compositions with CdSeTe source temperature measured by EDX, elemental-associated material change such as Se loss is unlikely, but structural and phase-based material changes may be present.

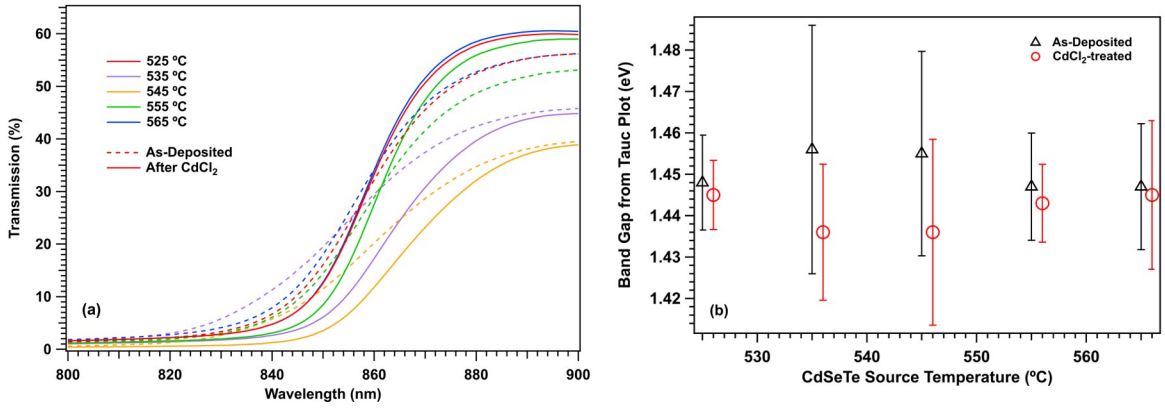

Figure 4.17: Transmission of as-deposited and $CdCl_2$-treated CdSeTe films with varied CdSeTe source temperatures (a) and corresponding Tauc band gaps (b).

Additional material analysis was performed with GAXRD (glancing angle X-ray diffraction) at incidence angles ≤ 3.0 °. Peak positions were determined using a Gaussian fit to the data, and the diffraction planes determined by matching to the PDF reference database. The XRD peaks for each CdSeTe source temperature are given in Figs. 4.18 (a) and (b) for as-deposited and $CdCl_2$-treated films respectively and labeled hkl planes correspond to the $CdSe_{0.1}Te_{0.9}$ cubic zinc blend phase (PDF 04-020-0043) to which the peaks were most closely matched. The relative peak intensities indicate that the dominant orientation of CdSeTe grown on MgZnO was (111), independent of CdSeTe source temperature, with (220) and (311) orientation peaks present in 525, 555, and 565 °C as-deposited films, and at all temperatures for $CdCl_2$-treated films.

As-deposited CdSeTe films fabricated with source temperatures at 535 and 545 °C showed additional peaks which correspond to the hexagonal CdTe phase. The hexagon symbols in Fig. 4.18 indicate the peaks associated with this phase: 2θ positions of 33.1°, 43.1°, 60.0°, and 67.2° correspond to the (102), (103), (203), and (212) diffraction planes. As Fig. 4.18 shows, the CdTe hexagonal phase diffraction peaks were not present after $CdCl_2$ treatment, which

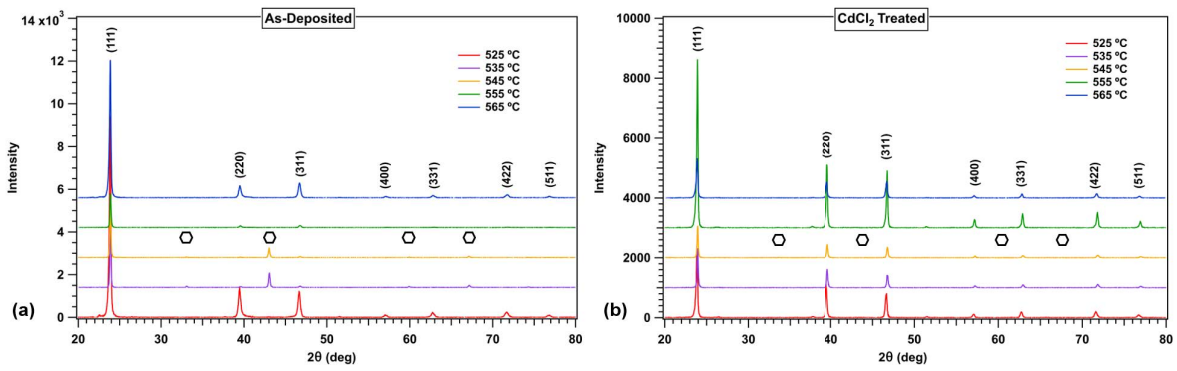

Figure 4.18: GAXRD peaks of as-deposited (a) and $CdCl_2$-treated (b) CdSeTe films with varied CdSeTe source temperatures. Labeled hkl values correspond to the $CdSe_{0.1}Te_{0.9}$ cubic zinc blend phase. Hexagon symbols indicate peak positions for the CdTe hexagonal phase.

indicates that $CdCl_2$ passivation eliminated the CdTe hexagonal phase at these temperatures. This phase elimination may explain the shift in the transmission data absorption edge and optical band gaps between as-deposited and $CdCl_2$-treated films at 535 and 545 °C CdSeTe source temperatures.

Device Characterization

To determine whether variation in the CdSeTe source temperature affected device performance, 0.5-µm CdSeTe/1.0-µm CdTe devices were fabricated with CdSeTe deposited at the same set of source temperatures and constant top temperature. J-V data of the best-performing devices, given in Fig. 4.19, showed some variation across the temperature range, although the changes were fairly small and did not demonstrate an explicit trend with source temperature. J-V parameter box plots (not pictured) showed comparable spread (for example $\sim 4\%$ in efficiency) in data across the twenty-five devices at each source temperature.

QE data and PL emission spectra of the same devices were used to estimate the absorber band gap at each CdSeTe source temperature. QE and dQE/dλ data, given in Fig. 4.20 (a) and inset gave calculated band gaps of 1.48, 1.47, 1.47, 1.46, and 1.47 eV for 525, 535, 545, 555, and 565 °C CdSeTe source temperatures respectively and were in good agreement with band gaps determined from the PL emmission spectra maxima, Fig. 4.20 (b). The slight

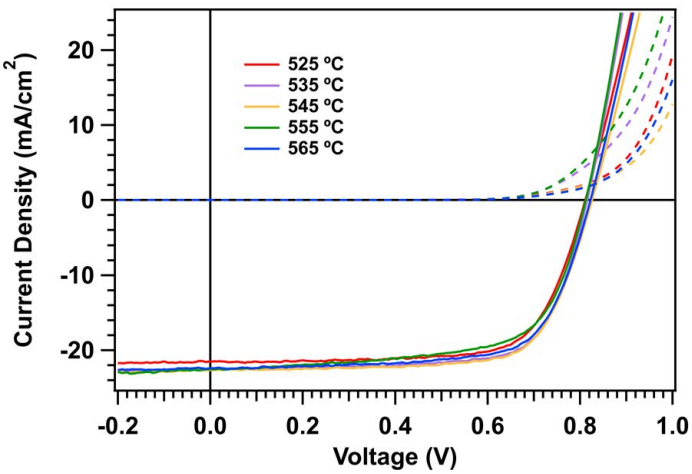

Figure 4.19: J-V curves of best-performing 0.5-µm CdSeTe/1.0-µm CdTe devices with varied CdSeTe source temperature.

increase in absorber band gap for the 525 °C device is likely the cause of the small decrease in measured J_{SC} in that device. Device band gaps were slightly wider than the CdSeTe Tauc plot band gaps as expected due to the inclusion of wider band gap 1.0-µm CdTe in the devices.

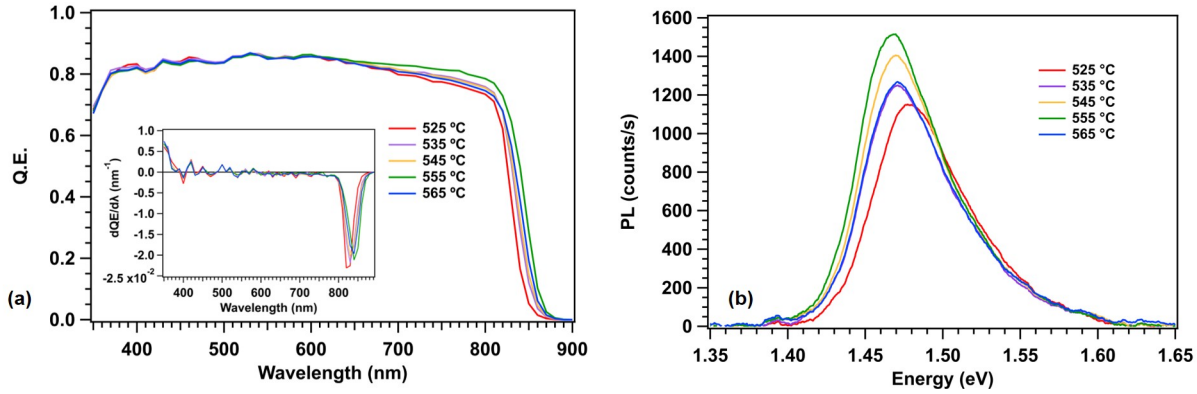

Figure 4.20: QE (a) and PL emission spectra (b) show a slight shift to wider band gap at the lowest CdSeTe source temperature. The inset shows more explicitly the band gaps as determined by dQE/dλ.

The small variations in device J-V data across the source temperature range were consistent with minor variations observed in $CdCl_2$-treated CdSeTe material properties. Based

on slightly higher demonstrated efficiencies, the 545 °C CdSeTe source temperature was considered optimal, although the relatively small J-V parameter deviations observed indicated that favorable 0.5-µm CdSeTe/1.0-µm CdTe device performance can be maintained for a range of $CdSe_{0.2}Te_{0.8}$ source temperatures.

4.4.2 $CdSe_{0.2}Te_{0.8}$ Top Temperature Variation

Material Characterization

Similar to the CdSeTe films described in 4.4.1, a range of top temperatures (420, 460, 480, 500, and 540 °C) and fixed bottom temperature of 575 °C were used to fabricate as-deposited and $CdCl_2$-treated 1.5-µm CdSeTe films on Tec10/100-nm MgZnO to characterize top temperature-dependent CdSeTe properties. SEM imaging of the as-deposited and $CdCl_2$-treated 1.5-µm CdSeTe films (not pictured) showed similar features as those grown with varied source temperature: bubble-like features, which were present on all as-deposited films, were eliminated after $CdCl_2$ treatment, and grains showed improved coalescence after $CdCl_2$ passivation at all temperatures. EDX mapping and line scan analyses indicated the bubble-like features were not elementally-affiliated.

EDX was used to determine atomic composition percentages of Cd, Te, Se, and Cl in each film. These percentages are plotted as a function of CdSeTe top temperature in Figs. 4.21 (a) and (b) for as-deposited and $CdCl_2$-treated films respectively. Cl increased slightly after $CdCl_2$ passivation as expected, and other elemental percentages remained fairly constant before and after passivation. With varied top temperature, Se increased from ∼5% at 420 °C to ∼10% at 540 °C, with a concomitant decrease in Te, which suggests that Se sublimates somewhat more preferentially at higher top temperatures.

The increase in Se composition for higher CdSeTe top temperatures was verified through photoluminescence, transmission, and GAXRD measurements. PL emission spectra of the $CdCl_2$-treated CdSeTe films at each top temperature are given in Fig. 4.22. Due to non-Gaussian spectra, approximate band gaps were determined by the energy of maximum PL

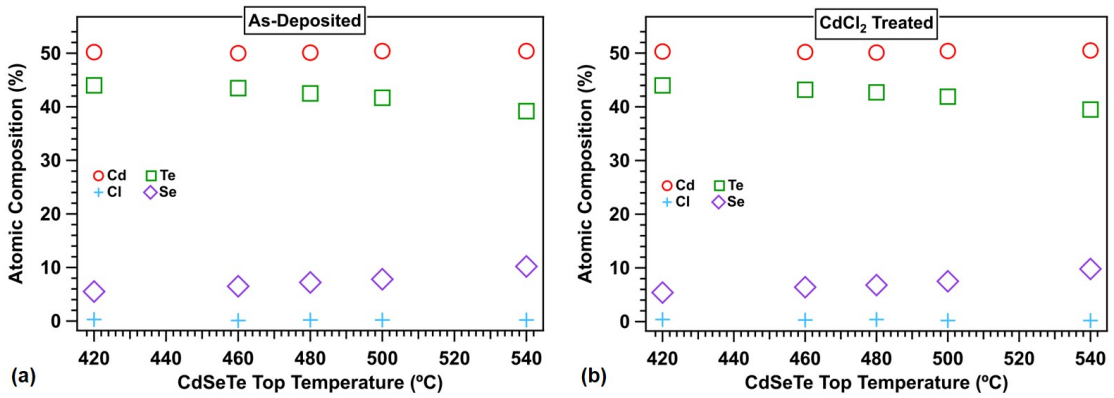

Figure 4.21: Elemental atomic compositions of as-deposited (a) and $CdCl_2$-treated (b) CdSeTe films with varied CdSeTe top temperature. Se composition increases with top temperature and substitutes for Te.

detection. The approximate band gaps decreased in accordance with the increased Se composition measured by EDX: band gaps shifted from 1.46 to 1.45 eV for 420 to 540 °C top temperatures.

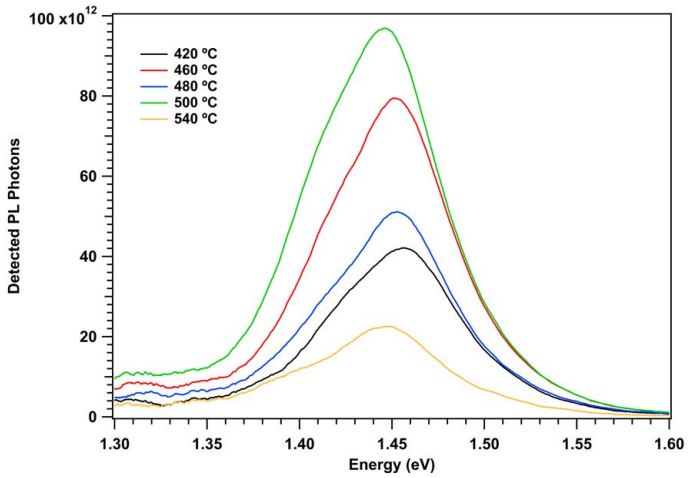

Figure 4.22: PL emission spectra of $CdCl_2$-treated CdSeTe films with varied CdSeTe top temperature. Band gaps narrowed in accordance with the increased Se composition at higher top temperatures.

Transmission data, given in Fig. 4.23 (a) also showed a shift in the CdSeTe absorption edge to lower energy with higher top temperatures. The corresponding Tauc band gaps are given in Fig. 4.23 (b) as a function of CdSeTe top temperature. The band gaps demonstrated

a systematic decrease with higher top temperature, consistent with the PL-determined band gap shifts and increased Se composition measured by EDX. As was observed in CdSeTe films deposited at varied CdSeTe source temperatures, the as-deposited films had a slightly wider band gap than $CdCl_2$-treated films, although the band gaps were in agreement within measured uncertainties.

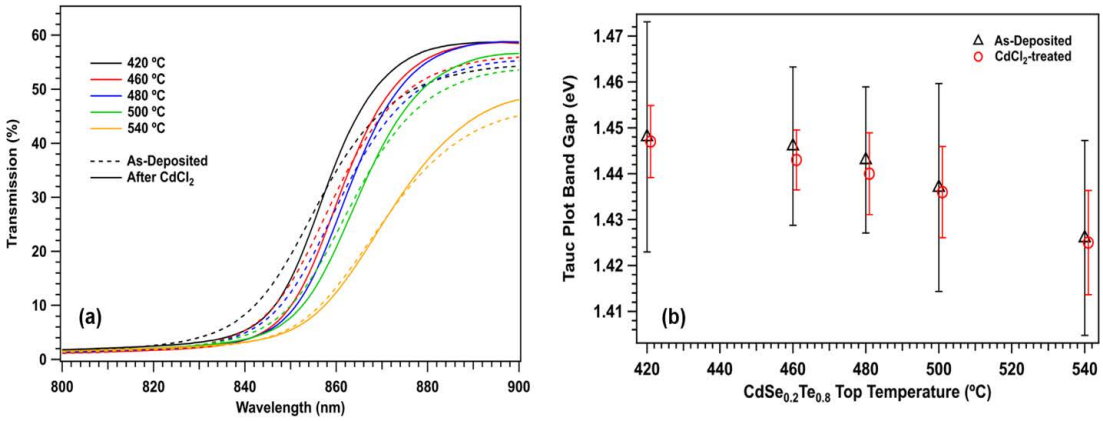

Figure 4.23: (a) Transmission of as-deposited and $CdCl_2$-treated 1.5-µm CdSeTe films show an absorption edge shift to lower energies at higher top temperatures. (b) Tauc band gaps narrowed in accordance with the increased Se concentration at higher top temperatures.

GAXRD was measured on the CdSeTe top-temperature films with glancing angles $< 3.5°$, and the diffraction peaks of the $CdCl_2$-treated films are given in Fig. 4.24 (a). The labeled hkl planes correspond to the $CdSe_{0.1}Te_{0.9}$ cubic zinc blend phase (PDF 04-020-0043) to which the peaks were most closely matched. Relative XRD peak intensities indicated a preferred orientation along the (111) plane with additional orientations along the (220) and (311) planes. Each hkl peak location shifted to greater 2θ for higher top temperatures; Fig. 4.24 (b) demonstrates this shift for the (111) plane. The (111) peak shift from 23.9°to 24.1°corresponds to a shift away from $CdSe_{0.1}Te_{0.9}$ toward $CdSe_{0.2}Te_{0.8}$, which indicates that Se composition increased at higher top temperatures, consistent with EDX measurements and optical band gap determinations.

The as-deposited films showed the same peak location and intensity trends, and the shift in the (111), (220), and (311) peak locations for as-deposited and $CdCl_2$-treated films with

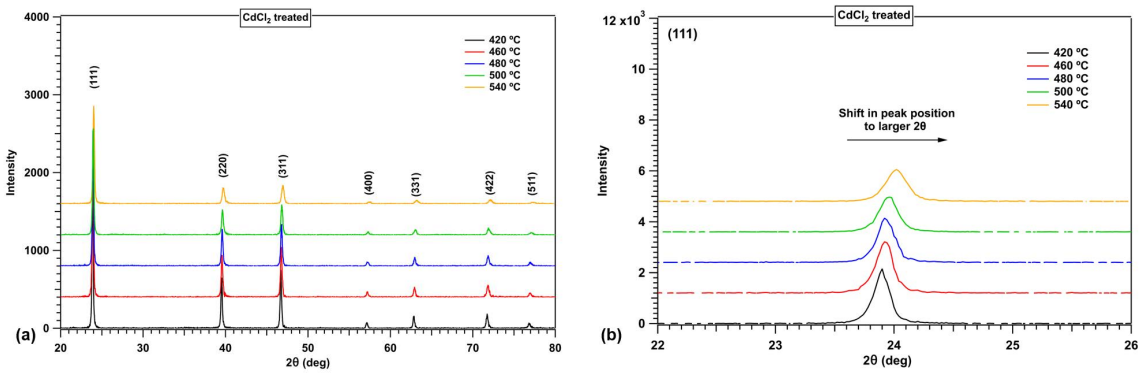

Figure 4.24: (a) GAXRD peaks and identified hkl planes of $CdCl_2$-treated CdSeTe films with varied CdSeTe top temperatures. (b) (111) peak locations demonstrate the 2θ shift for higher top temperatures which occurs at each peak location.

varied top temperature are given in Fig. 4.25. The peak locations, determined by Gaussian fits to the XRD peaks, demonstrate the 2θ shift with CdSeTe top temperature independent of $CdCl_2$ treatment, which indicates a top temperature-dependent change in lattice constant. The as-deposited films generally showed slightly lower 2θ peak locations than those $CdCl_2$-treated, which suggests a slightly lower Se concentration in these films, consistent with the small Tauc band gap differential between as-deposited and $CdCl_2$-treated films.

Given the observed 2θ GAXRD peak shifts there is an expected change in lattice constant, a_0. Lattice constants were calculated for each CdSeTe top temperature as-deposited and $CdCl_2$-treated CdSeTe film using the Nelson Riley method [128]. In this method, calculated lattice coefficients for a given hkl plane, a_{hkl}, are plotted on the ordinate axis, and $\frac{1}{2}\left[\frac{cos^2\theta}{sin\theta} + \frac{cos^2\theta}{\theta}\right]$ is plotted on the abscissa. Cubic-structure lattice coefficients of a given hkl plane were calculated by:

$$a_{hkl} = \frac{\lambda}{2sin\theta}\left(h^2 + k^2 + l^2\right)^{1/2} \tag{4.10}$$

where λ is the incident X-ray beam wavelength, equal to 1.5406 Å for $\lambda_{K\alpha 1,Cu}$. Lattice constants a_0 were determined for each CdSeTe top temperature by linearly fitting the a_{hkl} data and extrapolating to $\theta = 90\ ^\circ$ (where $\frac{1}{2}\left[\frac{cos^2\theta}{sin\theta} + \frac{cos^2\theta}{\theta}\right] = 0$), and are given in Fig. 4.26 as a function of top temperature. The lattice constants for cubic $CdSe_{0.1}Te_{0.9}$ and

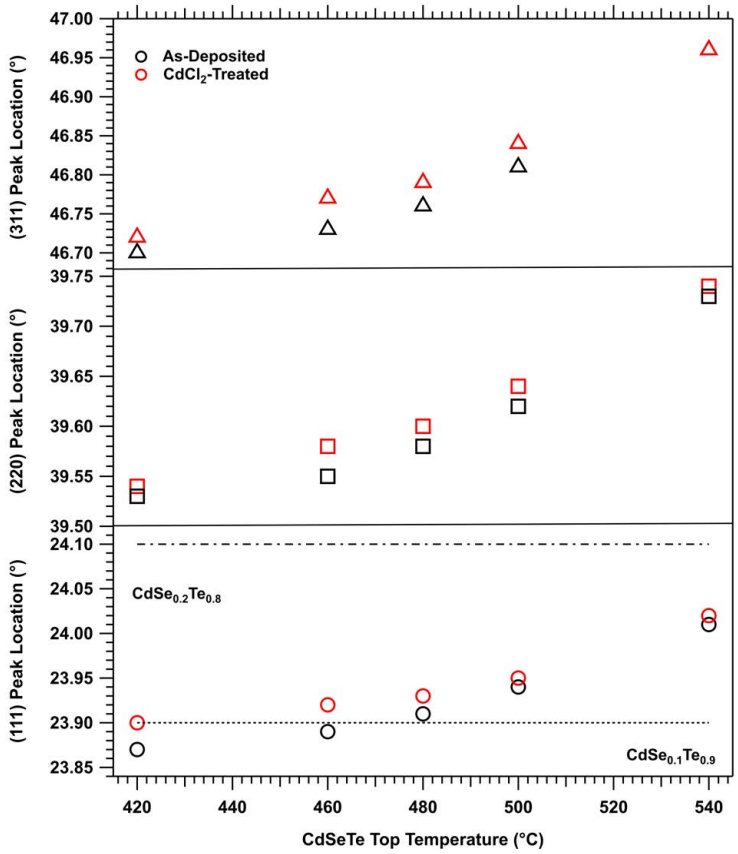

Figure 4.25: GAXRD peak locations for (111), (220), and (311) planes show a shift to greater Se composition with higher CdSeTe top temperatures.

$CdSe_{0.2}Te_{0.8}$, 6.4391 Å and 6.4381 Å respectively, given by the PDF reference database, are also shown in Fig. 4.26. The as-deposited and $CdCl_2$-treated lattice constants were in good agreement, where the reported uncertainties correspond to ± 1 standard deviation. The lattice constants clearly decreased for increasing top temperatures, where at the lowest top temperature there is good agreement with the $CdSe_{0.1}Te_{0.9}$ reference lattice constant, and at higher top temperatures, the calculated lattice constants approached that of the $CdSe_{0.2}Te_{0.8}$ reference. This provides corroborative evidence that Se concentration increases in CdSeTe films fabricated at increased top temperatures, in the 420-540 °C range.

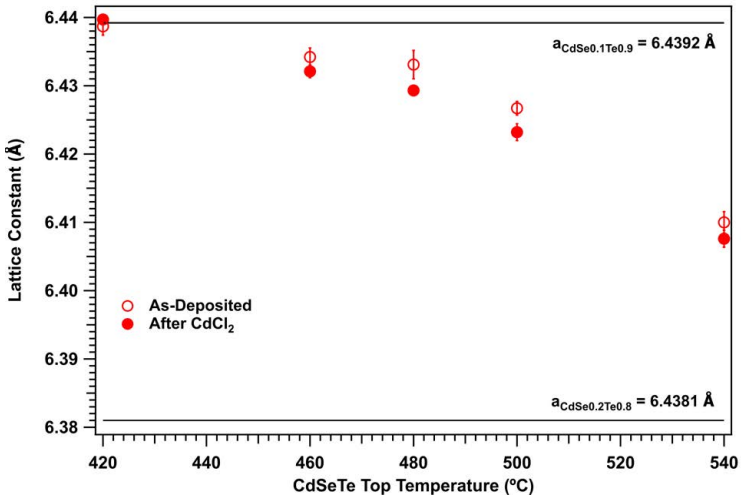

Figure 4.26: Calculated lattice constants for varied CdSeTe top temperature compared to reference $CdSe_{0.2}Te_{0.8}$ and $CdSe_{0.1}Te_{0.9}$ lattice constants indicate increased Se concentration in films fabricated with higher top temperatures.

Device Characterization

The effects of CdSeTe top temperature on device performance in 0.5-µm CdSeTe/1.0-µm CdTe absorber structures were studied with the same CdSeTe top temperature set points of 420, 460, 480, 500, and 540 °C. The measured J-V data and parameters, given in Fig. 4.27 and Table 4.3 respectively, showed some top temperature-dependent device performance. Efficiency generally decreased with higher CdSeTe top temperature due mainly to reduced fill factors; the best-performing device J-V data showed that the maximum power point

decreased for higher top temperatures, and there was notable shunt conductance present in all of the devices. The efficiency difference between the two highest-performing devices (at 480 and 420 °C) was small, and box plots of the J-V parameters, given in Fig. 4.28, for all twenty-five devices at each top temperature showed that the spread in J-V parameter data was greater for the 480 °C data set than the 420 °C data set. Given the general decline in J-V performance parameters with higher top temperature and the fairly small spread in the 420 °C top temperature data, 420 °C was utilized as the CdSeTe top temperature for all successive $CdSe_{0.2}Te_{0.8}$ CSS depositions.

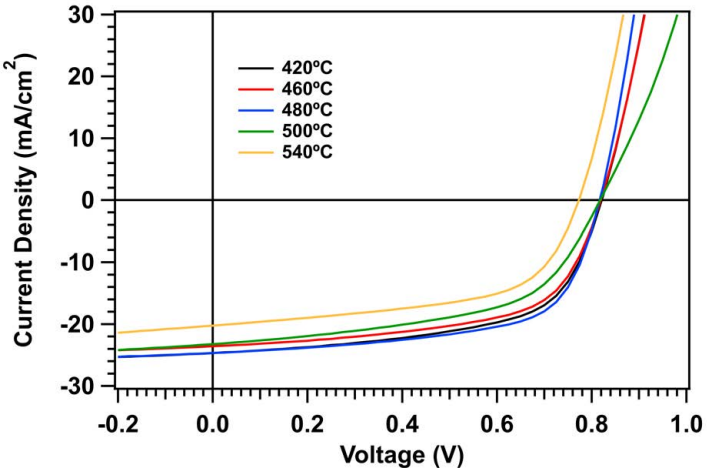

Figure 4.27: J-V curves of best-performing 0.5-µm CdSeTe/1.0-µm CdTe devices with varied CdSeTe top temperature.

The absorber band gaps were 1.45 eV for each device except for the highest top temperature device, where the band gap decreased to 1.43 eV as determined by QE and verified with PL. The ultimate decrease in CdSeTe/CdTe device band gap at high CdSeTe top temperature was in agreement with the decrease in CdSeTe material band gap, although device band gaps did not systematically decrease across the full top temperature range as observed in CdSeTe film band gaps. This may be due to fabrication-based differences between film and device structures such as the extent of CdSeTe/CdTe inter-diffusion in devices, or it could be an effect of changes in CdSeTe source material composition which can occur over time.

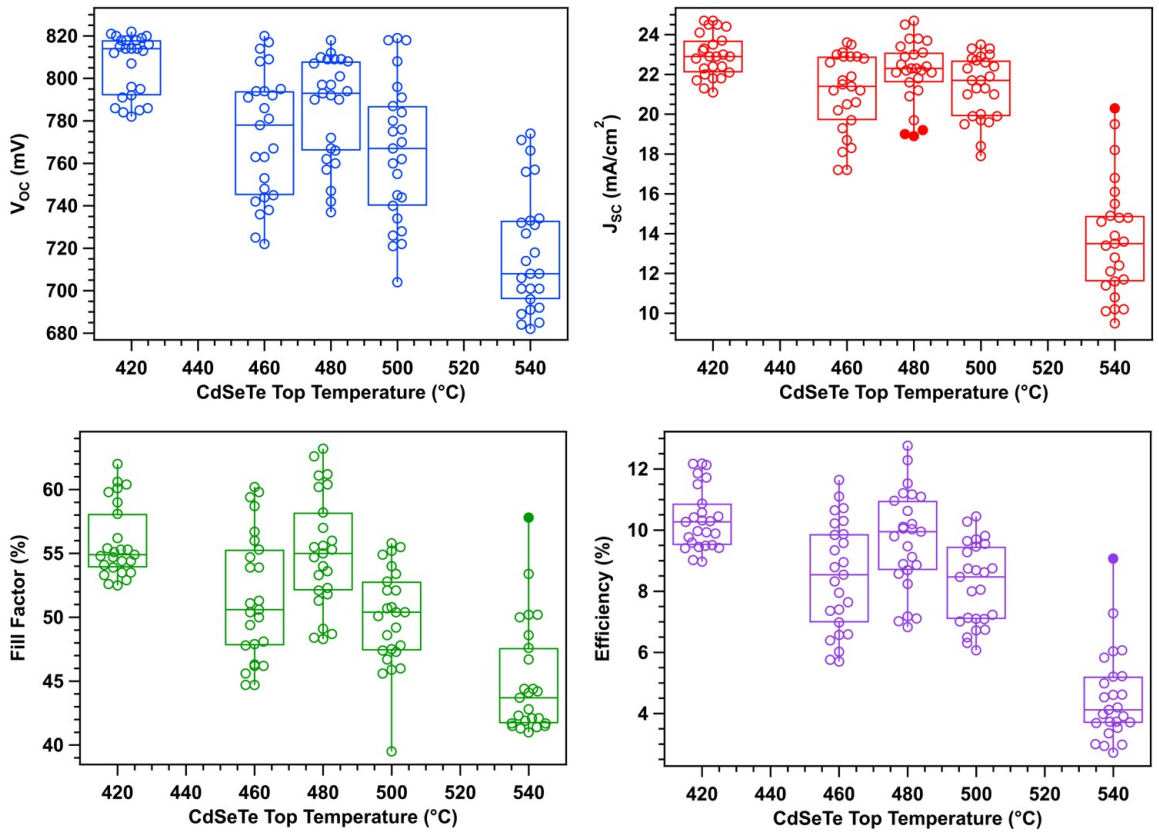

Figure 4.28: J-V parameter box plots of 0.5-µm CdSeTe/1.0-µm CdTe devices with varied CdSeTe top temperature.

Table 4.3: J-V parameters of best-performing CdSeTe/CdTe devices with varied CdSeTe top temperature.

CdSeTe Top Temp (°C)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
420	0.822	24.7	60.1	12.2
460	0.820	23.6	60.2	11.6
480	0.818	24.7	63.2	12.8
500	0.818	23.3	54.9	10.5
540	0.774	20.3	57.8	9.1

Although fabrication temperature-dependent trends were less prominent in CdSeTe/CdTe devices as compared to CdSeTe films, the effects of varied CdSeTe source and top temperatures on CdSeTe material properties informed interpretations of device data, and may provide insight for development of related materials.

4.5 Impacts of CdSeTe on Performance Parameters

4.5.1 CdSeTe Incorporation and Open Circuit Voltage

Since CdSeTe/CdTe bilayer absorbers have a narrower band gap than CdTe absorbers, CdSeTe/CdTe device V_{OC} is expected to decrease in accordance with Eq. 4.7. J-V data comparison between a 0.5-µm CdSeTe/1.0-µm CdTe device and 1.5-µm CdTe device fabricated with the optimized fabrication conditions described in Section 4.2 is shown in Fig. 4.29. The corresponding J-V parameters are listed in Table 4.4 which also provides the mean and standard deviation of the five best-performing devices on each plate.

The V_{OC} of the CdSeTe/CdTe bilayer device was approximately 30 mV lower than that of the CdTe device, although due to band gap differences in the devices, comparison of raw V_{OC} is insufficient. The 0.5-µm CdSeTe/1.0-µm CdTe and 1.5-µm CdTe devices had band gaps of

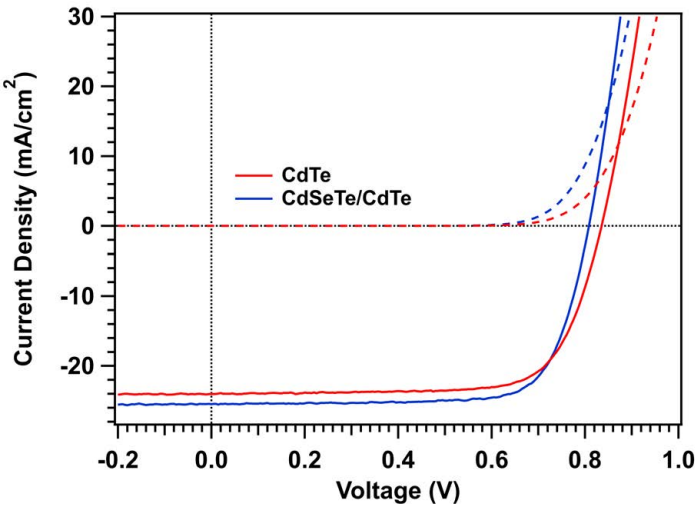

Figure 4.29: J-V comparison of 0.5-µm CdSeTe/1.0-µm CdTe and 1.5-µm CdTe devices demonstrates explicit changes in V_{OC} and J_{SC} with the addition of CdSeTe to the absorber.

1.42 and 1.49 eV respectively as measured by QE, which correspond to ideal V_{OC} values of 1.13 V and 1.19 V. Since there is a 60 mV ideal V_{OC} differential for these single and bilayer absorber devices, it is more appropriate to compare the voltage deficit rather than the V_{OC} of the devices, where voltage deficit is given by $V_{def} = V_{OC,ideal} - V_{OC,measured}$. The voltage deficits of the CdTe and CdSeTe/CdTe devices are listed in Table 4.4; the CdSeTe/CdTe bilayer device demonstrated a 30-mV lower voltage deficit than the CdTe device. Given the dependence of V_{OC} on recombination, a smaller voltage deficit in the CdSeTe/CdTe device may suggest reduced recombination mechanisms with the introduction of CdSeTe.

Recombination was examined through single-photon TRPL measurements on the CdTe and CdSeTe/CdTe devices with excitation incident from the glass side. The TRPL decays are given in Fig. 4.30 and show clear improvement in the tail lifetime, τ_2, with incorporation of CdSeTe into the absorber. The τ_2 lifetimes of the CdTe and CdSeTe/CdTe devices were 1.6 $\pm$ 0.1 ns and 12.6 $\pm$ 0.5 ns respectively, where τ_2 was determined by fitting the tail part of the decay with an x-offset exponential function. τ_2 lifetime is ascribed in part to bulk properties in CdTe devices [39,97], therefore the increase in τ_2 lifetime with the incorporation of CdSeTe may be attributed in part to reduced bulk recombination in CdSeTe/CdTe absorbers. Since longer TRPL lifetimes have been correlated with increased V_{OC} in CdTe and Cu(In,Ga)Se_2

Table 4.4: J-V parameter comparison of 0.5-µm CdSeTe/1.0-µm CdTe and 1.5-µm CdTe devices

Absorber	$\mathbf{J_{SC}}$ **(mA/cm^2)**	$\mathbf{V_{OC}}$ **(mV)**	$\mathbf{V_{def}}$ **(mV)**	**FF (%)**	$\boldsymbol{\eta}$ **(%)**
CdTe	24.0	835	355	73.4	14.7
CdSeTe/CdTe	25.5	808	322	75.5	15.6
	5 Best Devices: Mean ± S.D.				
CdTe	24.2 ± 0.1	835 ± 1	355 ± 1	72.2 ± 0.7	14.6 ± 0.1
CdSeTe/CdTe	25.5 ± 0.1	810 ± 1	320 ± 1	74.0 ± 1.1	15.3 ± 0.2

devices [39, 129, 130], the longer CdSeTe/CdTe lifetime also corroborates the voltage deficit reduction measured in that device.

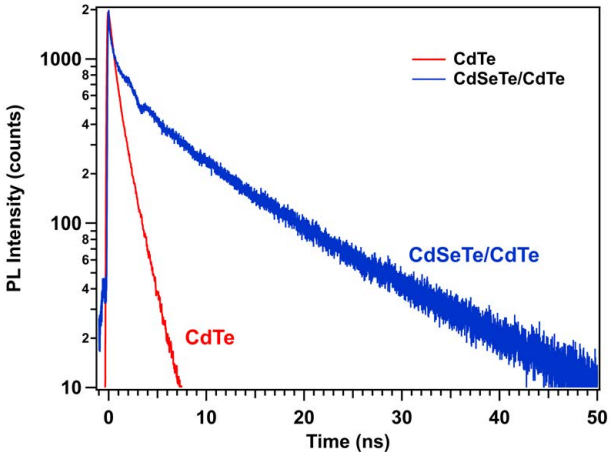

Figure 4.30: Single-photon TRPL of 0.5-µm CdSeTe/1.0-µm CdTe and 1.5-µm CdTe devices shows a clear improvement in lifetime for the bilayer device. From Ref. [131].

The degree of dark and light crossover in the J-V data of Fig. 4.29 also suggests a change in recombination between the single and bilayer-absorber devices. Electron current, which produces the crossover effect when dominant over injected hole current, depends on absorber thickness and bulk recombination strength [79]. With absorber thickness fixed at 1.5 µm for both devices, the change in crossover between the two devices was attributed

to a change in recombination. Fig. 4.29 showed only a small extent of crossover for the CdSeTe/CdTe device, and a somewhat larger extent of crossover in the CdTe device, which suggests that there is somewhat less bulk recombination in the CdSeTe/CdTe bilayer device than the single-absorber CdTe device.

Further evidence of the voltage deficit differential between the single and bilayer-absorber devices was provided by electroluminecence (EL) imaging. Natural log-scaled EL images for the CdTe and CdSeTe/CdTe devices are given in Figs. 4.31 (a) and (b) respectively, and clearly show greater EL intensity for the CdSeTe/CdTe device. Since the natural log of EL intensity is directly proportional to reduced voltage deficit [36,37], the substantial increase in EL intensity with the addition of CdSeTe to the absorber verifies the voltage deficit reduction measured in CdSeTe/CdTe devices.

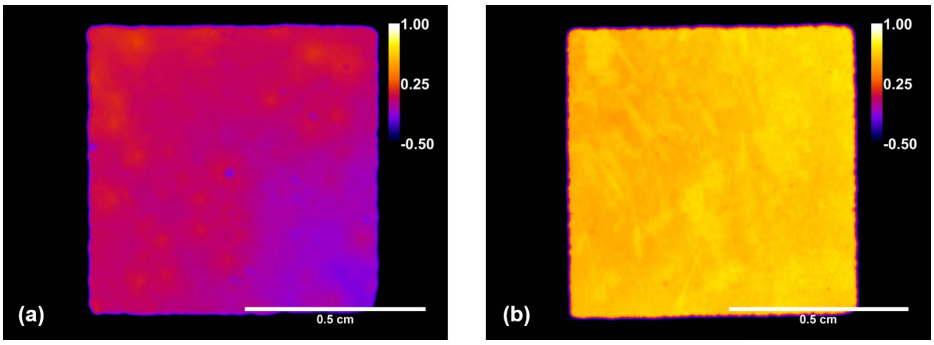

Figure 4.31: EL images of (a) 1.5-µm CdTe and (b) 0.5-µm CdSeTe/1.0-µm CdTe devices show greater electroluminescence for the bilayer-absorber device. From Ref. [131].

Electronic and electro-optical measurements provided independent evaluations of changes to V_{OC} caused by the incorporation of CdSeTe into CdTe absorbers. Measured V_{OC}, calculated voltage deficits, TRPL τ_2 lifetimes, dark/light J-V crossover, and EL intensities all indicated reduced voltage deficit in CdSeTe/CdTe devices. The lower voltage deficit may be due in part to superior bulk material properties of the CdSeTe/CdTe absorber; TRPL measurements and J-V crossover indicated reduced bulk recombination in the bilayer device, and T. Fiducia demonstrated that Se passivates critical bulk defects in CdSeTe/CdTe

absorbers [118]. The reduced voltage deficit may also be explained from a band diagram perspective: band alignment between the 1.42-eV CdSeTe and 1.49-eV CdTe layers will create a conduction-band offset at the CdSeTe/CdTe interface, but the built in potential of CdTe is at least partially maintained so that the V_{OC} differential from ideal is smaller.

4.5.2 Impacts of CdSeTe On Current

J_{SC} of the CdSeTe/CdTe device should increase in accordance with Eq. 4.2 given its narrower, 1.42-eV band gap compared to the 1.49-eV band gap of the CdTe device. Fig. 4.29 and Table 4.4 demonstrate such improvement in J_{SC} from 24.0 to 25.5 mA/cm^2 for the CdTe and CdSeTe/CdTe devices respectively.

Given the increase in J_{SC} with the addition of CdSeTe to the absorber, it is useful to quantify the current collection associated with each absorber layer, as well as changes in the current density loss mechanisms for the single and bilayer devices. Current losses were analyzed following the process outlined in section 3.4.2, and current separation between the CdSeTe and CdTe layers required a multi-step approach. For the CdSeTe/CdTe device, transmission was measured on a 0.5-µm CdSeTe film, corrected for reflection and absorption as described by Eq. 3.16, and was used to determine the fraction of light which reached the CdTe layer. The data were truncated to match the CdTe absorption edge, determined from 1.0-µm CdTe transmission data, such that incomplete absorption was quantifiable. Current collection in CdTe was determined by integrating the corrected CdSeTe transmission data with the standard AM 1.5G spectrum, and CdSeTe current collection corresponded to the difference between measured device QE and the corrected CdSeTe transmission data. The differential between the corrected 1.0-µm CdTe transmission data, offset by the calculated reflection and absorption losses, and the measured QE was attributed to recombination loss, and incomplete absorption was calculated from the remaining loss for energies above the band gap. Results of current loss analysis for 1.5-µm CdTe and 0.5-µm CdSeTe/1.0-µm CdTe absorbers are given in Figs. 4.32 (a) and (b), respectively and the corresponding

calculated current density values for each absorber layer and loss mechanism are given in Table 4.5.

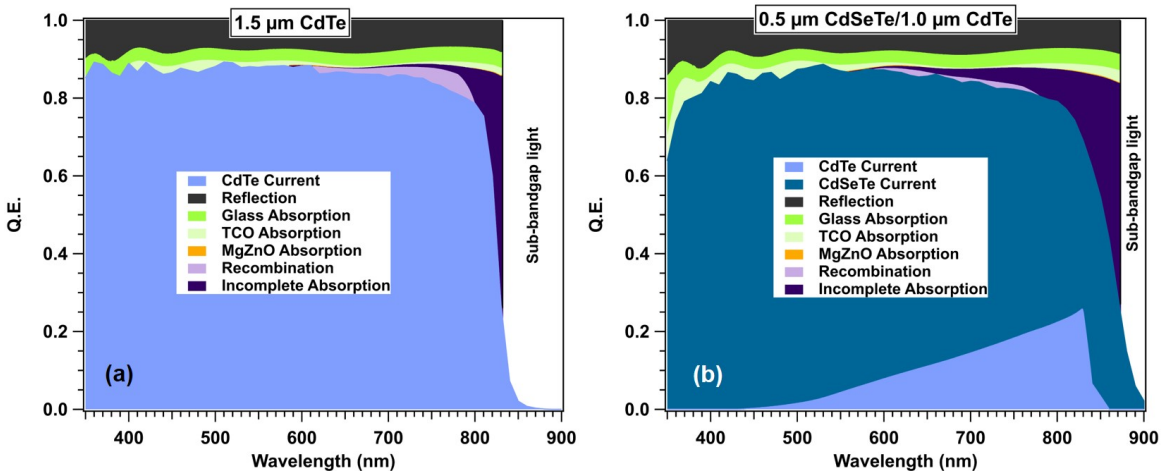

Figure 4.32: Current loss plots of (a) 1.5-µm CdTe and (b) 0.5-µm CdSeTe/1.0-µm CdTe devices show CdSeTe is the dominant current collector. From Ref. [131].

Comparison of the measured QE in Figs. 4.32 (a) and (b) showed increased photon conversion in the long wavelength regime for the CdSeTe/CdTe device corresponding to the lower absorber band gap. Separation of current collected in the CdSeTe and CdTe layers clearly demonstrated that CdSeTe is the dominant current collection layer. In the 0.5-µm CdSeTe/1.0-µm CdTe structure, CdSeTe comprised 88% of the current collection, and 96% with ∼1.0 µm CdSeTe preceding CdTe (not pictured). Glass, TCO, and MgZnO absorption losses were fairly small due to the near-transparency of the layers, and values were comparable for the single and bilayer devices because the window layers were nominally identical for the two structures. Reflection losses were also fairly comparable for the two structures; the difference in measured reflection data for the two devices was small enough that the minor discrepancy in reflection loss was not attributed to the CdSeTe. Reflection accounted for ∼2.5 mA/cm^2, the largest loss mechanism in both devices, however, reflection losses can be reduced with the incorporation of an anti-reflection coating [56, 88, 93]. Although the CdTe and CdSeTe/CdTe absorbers are the same total thickness, incomplete absorption was

Table 4.5: Current density losses in 1.5-µm CdTe and 0.5-µm CdSeTe/1.0-µm CdTe devices.

Mechanism	**CdTe J (mA/cm^2)**	**CdSeTe/CdTe J (mA/cm^2)**
CdTe Current Density	24.6	3.0
CdSeTe Current Density	–	22.9
Reflection	2.3	2.6
Glass Absorption	1.0	1.1
TCO Absorption	0.3	0.5
MgZnO Absorption	<0.1	<0.1
Recombination	0.2	0.1
Incomplete Absorption	0.7	1.5
Device Current Density	**24.6**	**25.9**
Max Current Density	29.0	31.7

slightly larger for the CdSeTe/CdTe device because its narrower band gap increases the overall absorption potential of the absorber, as indicated in Table 4.5.

4.5.3 Impacts of CdSeTe On Fill Factor

Measured J-V parameters in Table 4.4 showed an increase in fill factor from 73.4% to 75.5% between the best-performing 1.5-µm CdTe and 0.5-µm CdSeTe/1.0-µm CdTe devices. Compared to ideal fill factors for these devices, 89.8% vs. 89.3%, the larger ideal-to-measured fill factor differential for the CdTe device (16.4% vs. 13.8%) indicates that the CdTe device suffered greater fill factor losses.

Fill factor losses were analyzed for the best-performing CdTe and CdSeTe/CdTe devices given in Fig. 4.29 and separation of the loss mechanisms are shown graphically and numerically in Fig. 4.33 and Table 4.2 respectively, where the J-V quality parameters, determined

by current voltage analysis, are included in Fig. 4.33. In this analysis the A-factor loss mechanism encompassed the A-factor dependent term in V_{OC}, Eq. 3.9, such that the V_{OC} reduction loss mechanism was attributable to the A-factor independent term, namely, the barrier height. Poorer A-factor, which results from recombination, was the dominant fill-factor loss mechanism in both devices, making up nearly 50% of the total loss in each case. This suggests that although bulk material properties seemed to improve with the addition of CdSeTe, as longer TRPL lifetimes and lower diode quality factor implied, absorber-independent recombination mechanisms, namely recombination at interfaces, remain significant contributors to CdSeTe/CdTe performance reduction. Because the CdTe/Te interface has a fairly high surface recombination velocity as discussed in section 3.5.2, it is possible that the ideality factor loss contribution is similar in the single and bilayer devices because of recombination at the CdTe/Te interface.

The remaining losses were fairly comparable between the CdTe and CdSeTe/CdTe devices; absolute fill factor losses were slightly smaller in the bilayer device such that the relative loss contributions in the devices were similar. Shunt conductance was fairly low in both devices, and contributed least to fill factor loss, and the comparable V_{OC} reduction losses suggested little change to the back barrier height between the device structures. To most effectively reduce fill factor loss in these devices, the voltage deficit must be reduced further, and both bulk and interface recombination must be minimized. This could be accomplished by altering the back-side structure of the device, which is the focus of Chapter 5.

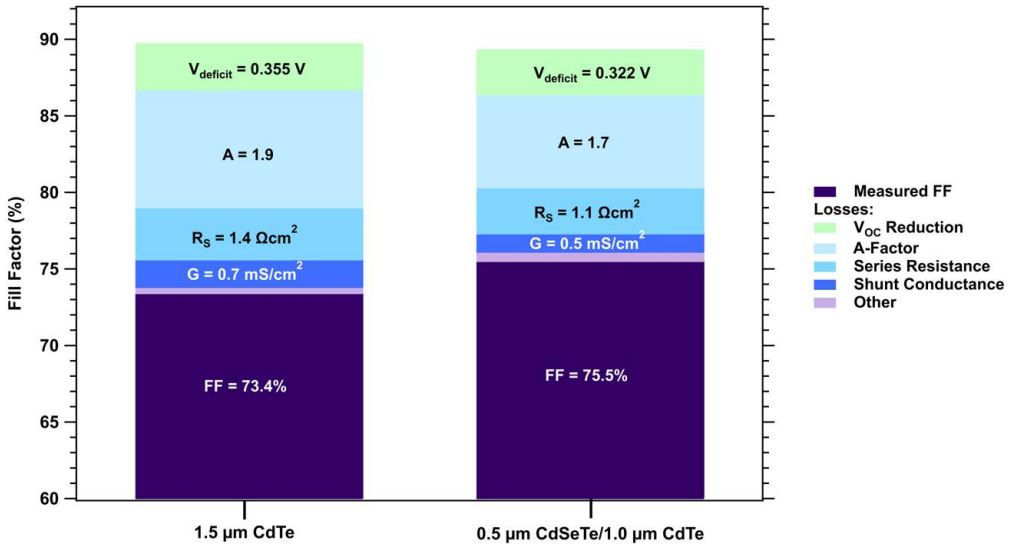

Figure 4.33: Fill factor loss mechanisms for 1.5-µm CdTe and 0.5-µm CdSeTe/1.0-µm CdTe devices.

Table 4.6: Fill factor losses in 1.5-µm CdTe and 0.5-µm CdSeTe/1.0-µm CdTe devices.

	% Fill Factor	
Mechanism	**1.5 µm CdTe**	**0.5 µm CdSeTe/1.0 µm CdTe**
V_{OC} Reduction	3.0	3.0
A Factor	7.7	6.1
Series Resistance	3.4	3.0
Shunt Conductance	1.8	1.2
Other	0.4	0.7
Measured Fill Factor	**73.4**	**75.5**

Chapter 5

INCORPORATION OF CdMgTe INTO CdSeTe/CdTe BILAYER DEVICES

In the past decade, efficiency advances in CdTe-based photovoltaic devices have been realized primarily through notable improvements in J_{SC} and fill factor following device structure modifications such as the incorporation of MgZnO as the n-type front buffer layer, and CdSeTe as a front absorber layer component [56, 104, 109, 114–116, 132–134]. With J_{SC} and fill factor close to their respective single-junction CdSeTe/CdTe theoretical maxima, (the record CdTe-based device demonstrated ∼99% and 88% of the maximum achievable J_{SC} and fill factor values respectively [57]), V_{OC} remains the primary limiting factor in CdTe device efficiency; ∼79% of the maximum V_{OC} has been achieved to date such that CdSeTe/CdTe device efficiency has realized only ∼69% of its potential [57]. Significant V_{OC} loss has been attributed in part to back-surface recombination, which can be reduced through the incorporation of a back-surface field as demonstrated in other PV technologies such as Si, III-Vs, and Cu(In,Ga)Se_2 [135–146]. Modeling has demonstrated that this should also be achievable in CdTe-based PV given an appropriately thin absorber [70,92,147]. This chapter discusses the incorporation of CdMgTe as an electron-reflector layer to create a back-surface field in thin CdSeTe/CdTe devices for targeted V_{OC} improvement. Comparisons between CdMgTe deposition methods are made, and performance improvements compared to previous CdMgTe electron-reflector devices [64, 71, 148] are presented and explained with material, electronic, and electro-optical analyses. Remaining limitations present in the CdMgTe electron-reflector devices are discussed and possible solutions are postulated.

5.1 Electron Reflector Introduction

5.1.1 Electron Reflector Concepts

In photovoltaic devices, acute defects in the crystal structure which are present at surfaces create many allowed states within the forbidden gap such that recombination can efficiently occur at these surfaces [21]. For minority carrier diffusion lengths longer than the absorber thickness, back-surface recombination may be a primary limitation to improved V_{OC}. The back surface recombination rate, R_{bs} can be given by:

$$R_{bs} \approx \frac{n_{bs} p_{bs}}{n_{bs} + p_{bs}} S_{bs} \tag{5.1}$$

where n_{bs} and p_{bs} are the electron and hole carrier densities at the back surface respectively, and S_{bs} is the back-surface recombination velocity. S_{bs} is dependent on the product of surface defect states, N_d, the electron and hole capture cross section, $\sigma_{n,p}$, and thermal velocity, v_{th} ($S_{bs} = N_d \sigma_{n,p} v_{th}$) [100]. One method to reduce R_{bs} is to reduce the carrier density of electrons, holes, or both at the back surface which is achieved through the creation of an electric field. This method is generally referred to as the incorporation of a back-surface field (BSF). Many PV technologies (Si, Cu(In,Ga)Se_2, and III-Vs) have demonstrated improved V_{OC} and device performance through the utilization of a BSF [135–146]; under forward bias the BSF creates a conduction-band barrier to forward electron flow at the back such that electrons are driven away from the back contact and back-surface recombination is reduced. Another method to lower R_{bs}, not discussed in this work, is to reduce surface defect states, often accomplished through chemical or thermal passivation.

The BSF method capitalizes on the interplay between bulk properties and interfaces. It is most effective when back-surface recombination dominates and lowers V_{OC}, i.e. for absorber thicknesses comparable to or less than the diffusion length. The diffusion length is device and material-dependent, but is typically a few microns for CdTe such that CdTe-based absorber thicknesses below 2 µm are ideal for BSFs [147]. Given a thin, fully-depleted

absorber, bulk recombination is correspondingly reduced such that acceptable performance can be maintained in a thin-CdTe device [137]. This is demonstrated by the simulated J-V curves in Fig. 5.1 which compare "thick" (3.0 µm) and "thin" (1.5 µm) CdSeTe/CdTe absorber devices with and without a BSF (via a CdMgTe back layer). The J-V data were produced with 1-D SCAPS modeling and incorporated parameters: MgZnO donor density, $N_D = 1.0x10^{17}/cm^3$, CdSeTe and CdTe acceptor density, $N_A = 2.0x10^{14}/cm^3$, CdSeTe τ = 50 ns, CdTe τ = 25 ns, S_{front} = 1E4 cm/s, and S_{back} = 5E4 cm/s. The simulated J-V data and corresponding parameters listed in Table 5.1 show that although both structures could benefit from the added BSF, the thin absorber with BSF should see the greatest relative improvement to V_{OC} and efficiency.

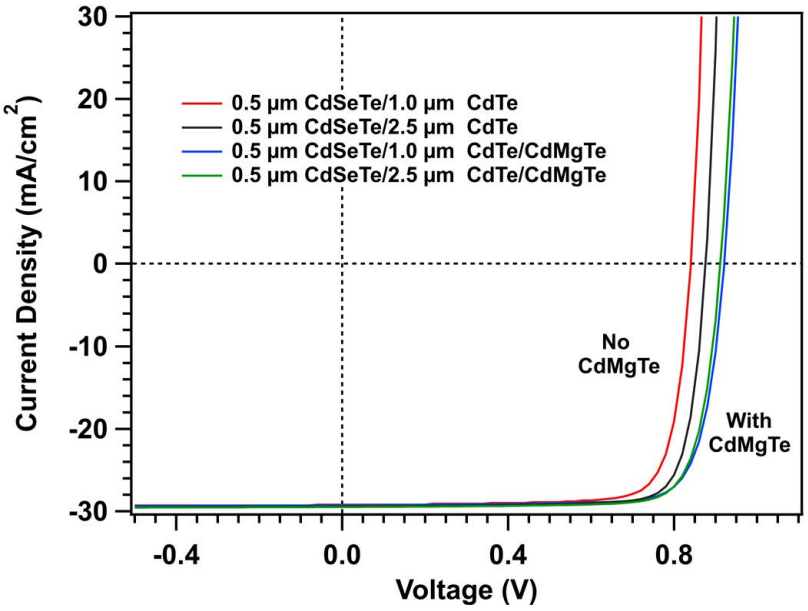

Figure 5.1: SCAPS-simulated J-V curves of CdSeTe/CdTe devices with and without a BSF (via a CdMgTe layer) for "thick" (3.0 µm) and "thin" (1.5 µm) absorbers.

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There are multiple mechanisms which create a BSF and include an expanded band-gap material layer, the addition of a charge layer or reversed back barrier, and a heavily-doped back surface, the descriptions and schematics for which are given in Fig. 5.2 [70, 100]. In the expanded band-gap layer structure the back-barrier height remains fixed with external

Table 5.1: Simulated J-V parameters: incorporation of a BSF on thin and thick absorbers.

Structure	$\mathbf{V}_{OC}$ **(mV)**	$\mathbf{J}_{SC}$ **(mA/cm^2)**	**FF (%)**	η **(%)**	ΔV_{OC} **(mV)**	$\Delta\eta$(%)
Thin Absorber	841	29.2	80.5	19.8	80	1.9
Thin Absorber w/ CMT	921	29.3	80.3	21.7		
Thick Absorber	876	29.4	82.0	21.1	36	0.6
Thick Absorber w/ CMT	912	29.5	80.6	21.7		

bias, but it may vary with applied voltage for the heavily-doped back surface configuration. BSF approaches can be implemented independently or concurrently, and some mechanisms such as thermal annealing and/or adding a buffer layer may reduce both surface defects and surface charge carriers.

In Si devices, the BSF was traditionally created by generating a heavily-doped region at the back of the structure through the incorporation of an aluminum layer alloyed into the Si [21, 137, 138]. Additional BSF methods in Si include the HIT (Heterojunction with InTrinsic layer) structure, boron doping, amorphous and micro-crystalline layers on c-Si, and the dielectric Al_2O_3 layer with negative charge [135–137, 149–152]. In Cu(In,Ga)Se_2 devices, a BSF can be created through band-gap grading in the absorber by increasing the Ga/(Ga+In) ratio toward the back to provide a conduction-band barrier for minority-carrier electrons, or through an Al_2O_3 layer with negative charge [141–143, 150, 151]. III-V devices have implemented wider band gaps and higher doping at the back to create a BSF, for example, AlGaAs and GaInP BSF layers on p-type GaAs absorbers [144–146].

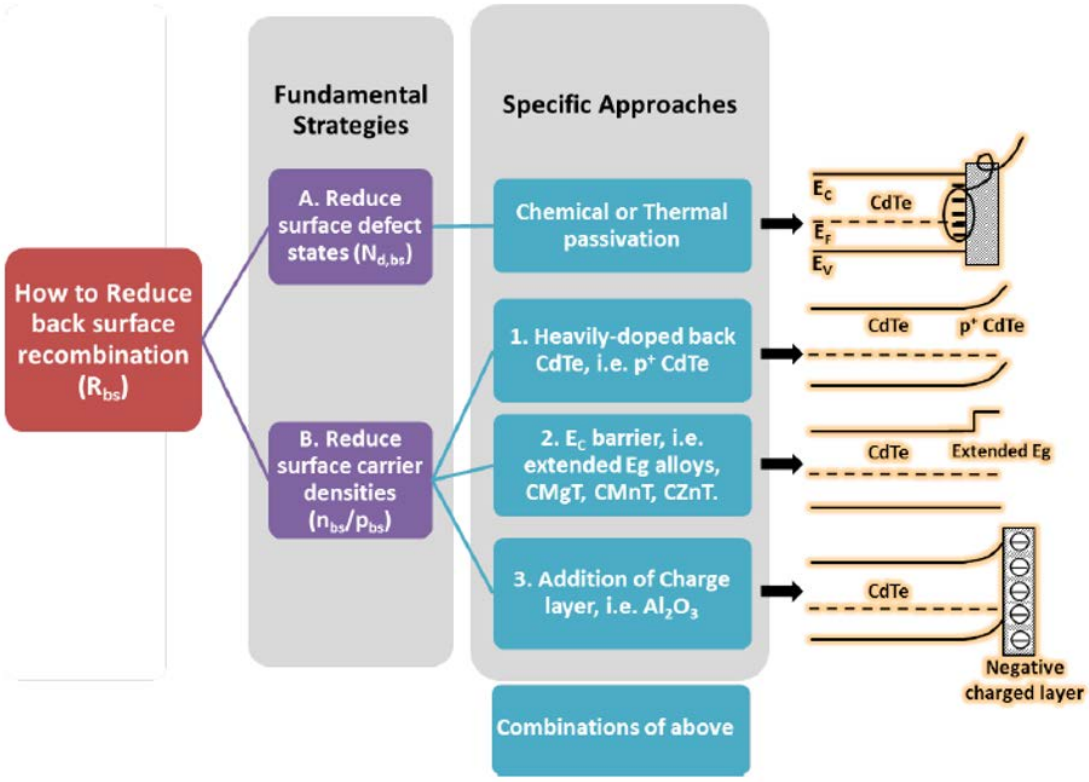

Figure 5.2: Mechanisms for reduction of back-surface recombination include chemical or thermal passivation, a heavily-doped back surface, addition of an expanded band-gap material layer, and the addition of a charge layer (top to bottom). From Ref. [100].

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In CdTe, these approaches for back-surface recombination reduction have been and are currently being explored numerically and experimentally to improve device V_{OC} and performance. Group V doping of CdTe has provided some promising initial results for a heavily-doped back contact, notably through As doping [24–26]. A passivating Al_2O_3 layer incorporated at the back has demonstrated favorable material properties such as longer minority-carrier lifetimes and increased implied V_{OC} (iV_{OC}) [41, 153, 154]. Through numerical simulation and modeling, K.J. Hsiao concluded that the expanded-band gap BSF method was the most efficient and practical mechanism for back-surface recombination reduction and enhanced V_{OC} in CdTe [70, 147], and experimental results have demonstrated some success with CdTe alloys as the expanded band-gap material [64, 71, 148, 155, 156]. Based on K.J. Hsiao's modeling results and the straightforward incorporation of a CdTe alloy material into existing fabrication processes, this research focuses on the introduction of an expanded band-gap material layer at the back to create the BSF and conduction-band offset.

The expanded band-gap method is exhibited most clearly in a band diagram representation of the device structure, and the band diagrams for CdSeTe/CdTe structures with zero and 1-V applied bias are given in Figs. 5.3 (a) and (b) respectively, and compared to CdSeTe/CdTe structures with a CdMgTe BSF layer at zero and 1 V applied bias in Figs. 5.3 (c) and (d) respectively. The bias comparison emphasizes the role of back-surface recombination in forward bias; without the drift field present to sweep electrons to the front junction, they will diffuse toward the back and recombine. The conduction-band offset produced by the expanded band-gap layer serves to reflect electrons from the back surface to reduce back-surface recombination, thus it is referred to as the electron-reflector layer throughout the rest of this work.

5.1.2 Electron Reflector Material Selection

The fundamental requirements for an expanded band-gap electron-reflector layer are a wider band gap energy than that of the absorber to get a conduction-band offset, and minimal lattice mismatch between the absorber and electron-reflector material to limit interface

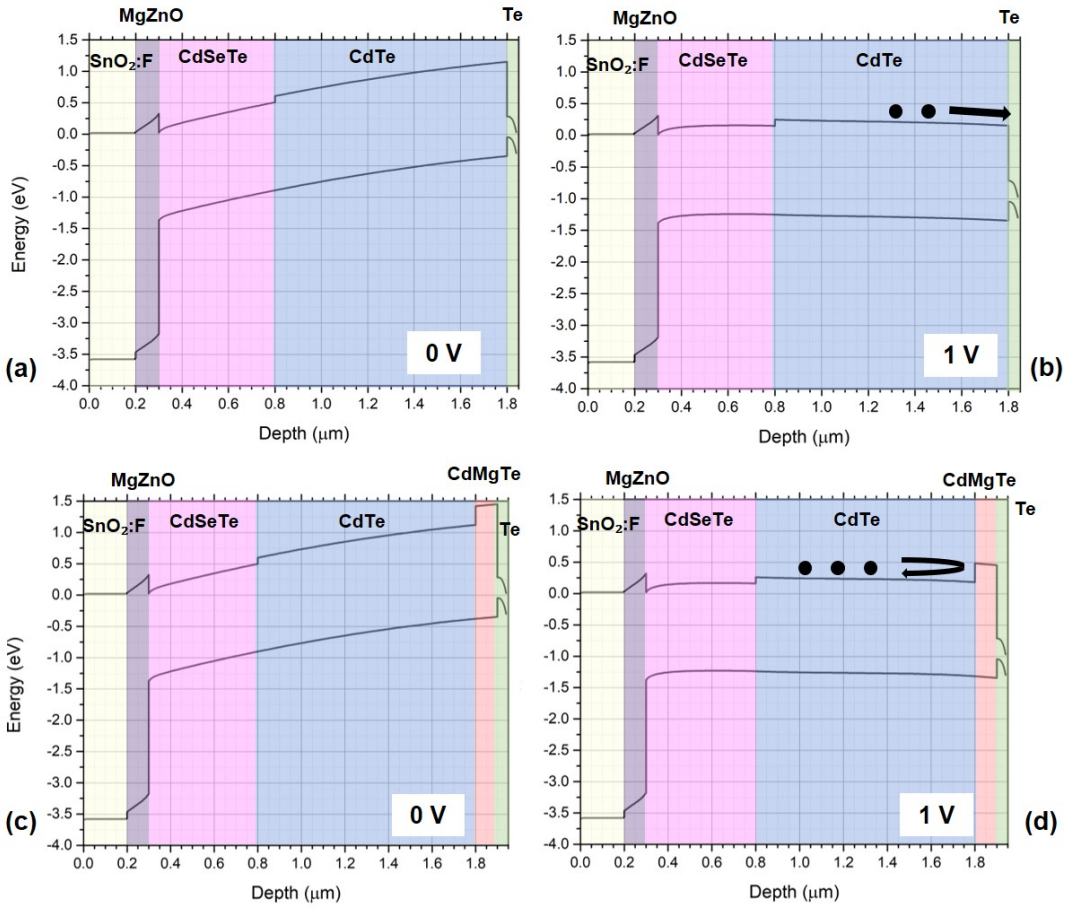

Figure 5.3: Band diagrams of CdSeTe/CdTe structures with 0 and 1 V applied bias (a) and (b) respectively, compared to CdSeTe/CdTe/CdMgTe structures with 0 and 1 V applied bias (c) and (d) respectively to demonstrate the conduction-band offset-induced electron reflector behavior.

recombination by reducing deep-level defect sites which allow photogenerated charge carriers to easily recombine. Fig. 5.4 provides the band-gap energy and lattice constants of materials typically used in thin-film devices [19] and shows that ZnTe and MgTe are good candidates for CdTe alloys for the electron reflector-layer because of their fairly closely-matched lattice constant with CdTe, and their wider band gaps. The ternary alloys $Cd_{1-x}Zn_xTe$ and $Cd_{1-x}Mg_xTe$ are produced by combining the ZnTe or MgTe binary compound with CdTe respectively, where the Zn or Mg atom replaces the Cd cation. As shown in Fig. 5.4, MgTe has a lattice constant most closely matched with CdTe, and has a wider band gap than ZnTe such that less alloying is required to fabricate a CdMgTe layer with the proper expanded band gap.

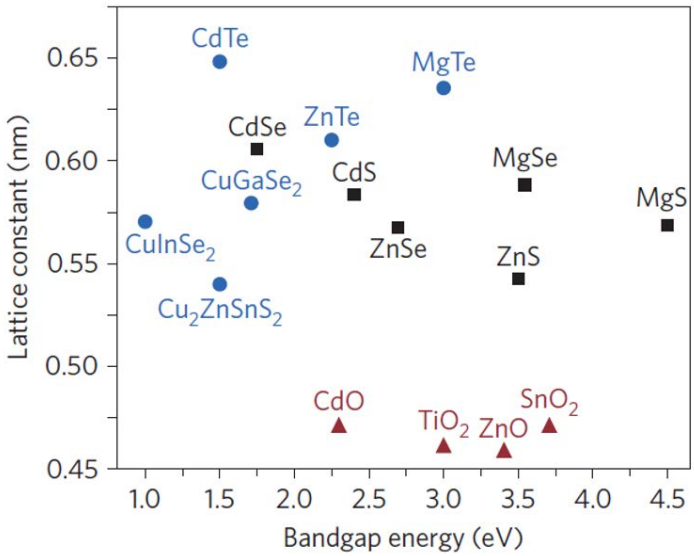

Figure 5.4: Lattice constants and band gap energies of typical materials in thin-film solar cells. MgTe and ZnTe are the most favorable electron reflector candidates for CdTe devices because of their fairly well-matched lattice constants to CdTe and wider band gap energies. From Ref. [19].

Worth noting are band-alignment drawbacks for CdTe/CdMgTe. As described above, the conduction-band offset is necessary for successful reflection of electrons away from the back surface to reduce back-surface recombination. However, numerical modeling and experimental results reported in literature indicate that the CdTe/CdMgTe band offset is split

between the valence and conduction bands such that there is a valence-band hole barrier between the CdTe and CdMgTe. The conduction-band and valence-band offset (CBO and VBO respectively) split is not well-agreed upon: calculated VBO/CBO percentage ratios of 30/70 [157–160] and 50/50 [161] have been reported, while a 15/85 ratio was determined experimentally [117]. Given the range of reported VBO/CBO ratios and K.J. Hsiao's simulation-based demonstration that a 0.2 to 0.3-eV conduction-band offset from 1.5-eV band-gap CdTe would improve device V_{OC} and efficiency [70], the target CdMgTe band gap for this work was 1.8-1.9 eV.

CdZnTe, unlike CdMgTe, has a slightly reversed valence-band barrier at the CdTe/CdZnTe interface [162, 163] which makes it more favorable for band alignment and hole collection. Initial investigation of CSS-deposited CdZnTe as an electron reflector on 1.0-µm CdTe absorbers demonstrated device V_{OC}s and efficiencies below 790 mV and 10% respectively for CdZnTe band gaps of 1.63, 1.72, and 1.84 eV. Compared to initial CdMgTe device data, the CdZnTe devices had somewhat lower performances and no indication of electron-reflector behavior. This, in conjunction with the favorable lattice constant and band-gap properties of MgTe and demonstrated success of CdMgTe thin-film deposition through close-space sublimation (CSS), sputtering, MBE, and co-evaporation [117, 123, 155, 157, 159, 160, 164–167], directed the focus on CdMgTe as the electron-reflector layer in this work.

5.1.3 Fabrication Methods for CdMgTe

P-type polycrystalline CdMgTe was deposited by CSS and RF magnetron sputtering in this work. In CSS, the CdMgTe was co-sublimated from Mg and CdTe sources using the deposition system described in [71, 123], where the band gap is controlled by Mg flux via the Mg source temperature. Deposition occurs in a separate high-vacuum system from that of the absorbers, in an argon environment with <0.01% O_2 to minimize oxidation, and after deposition, substrates are cooled in the vacuum system before removal. For sputtered CdMgTe, the CdMgTe film was deposited in an ultra-high purity Ar environment from a 4-inch diameter CdMgTe target with 3-inch target-to-substrate distance. As in CSS, after

deposition, substrates are cooled in the vacuum system before removal. Band gap can be controlled by target composition, pressure, and sputter power. In this work target composition was ∼20% Mg, 30% Cd, 50% Te by atomic percent, determined by EDX measurement on the target material, and pressure and sputter power were systematically varied (15 and 18 mTorr and 60 and 75 W respectively) to realize the targeted 1.8 to 1.9-eV CdMgTe band gap. The proper band gap was achieved with an RF sputter power of 75 W and 18 mTorr pressure. To maintain film quality, the range of pressure and sputter power was somewhat limited; high pressures can significantly reduce deposition rate, low pressures can lead to undesirable ion bombardment, and low power may lead to poor film quality. Therefore the realization of a greater CdMgTe band-gap range may necessitate a sputter target with a different Cd/Mg composition.

There are a number of processing-based difficulties associated with CdMgTe that can be addressed by CSS and sputter-deposition techniques, where each fabrication method offers its own advantages. The CdMgTe processing difficulties include high hygroscopy of CdMgTe, a Gibbs free energy favorable for MgTe to react with oxygen and form MgO [71], and loss of Mg in the CdMgTe when subject to high processing temperatures [122, 148, 165, 168, 169]. The processing advantages of sputter deposition proved more favorable to address these CdMgTe-specific complexities.

The greatest advantage of sputter-deposited CdMgTe is that substrate temperatures as low as room temperature are achievable. This facilitates retention of $CdCl_2$ passivation performed before CdMgTe deposition, a historically difficult material limitation in these structures; performance reduction in CSS-deposited CdMgTe devices has been attributed to temperature-induced Cl passivation loss in CdTe at temperatures exceeding 400 °C [49, 71]. Low substrate-temperature sputter deposition ultimately avoids the $CdCl_2$ passivation loss vs. magnesium retention obstacle in CSS CdMgTe; the necessity of a post-CdMgTe $CdCl_2$ treatment in CSS-deposition causes thermal diffusion of Mg into the absorber layer and localized Mg loss in the CdMgTe with associated reduced device performance [64, 148]. Mitigating solutions are presented and discussed in section 5.2.

Sputter deposition of CdMgTe is also favorable for reproducibility; the sputtered CdMgTe optical band gap was highly repeatable given the same operating pressure, power, process gas, and substrate temperature. This is in contrast with CSS-deposited CdMgTe for which the band gap of the CdMgTe film often fluctuated over extended time periods such that weekly re-calibration of the CdMgTe band gap was required.

Although not completely uniform across the substrate, the sputtered CdMgTe band gap was fairly uniform compared to CSS-deposited CdMgTe. This is highlighted in the contour plots of an especially variable CSS CdMgTe film and sputter-deposited CdMgTe film given in Figs. 5.5 (a) and (b) respectively. Band gaps were determined by Tauc plot fits to CdMgTe film transmission data in 25 locations across the substrate in accordance with device positions. While satisfactory for small-scale research requirements, for scalability to industrial fabrication, both deposition methods, CSS especially, would necessitate modifications. In CSS, non-uniformities could be minimized by deposition at higher pressures to increase the scatter of Mg vapor flow, or changes to the source geometry such that a larger volume is available for vapor intermixing [123]. Sputtering may require system-geometry alterations such as the utilization of rotation magnet sputtering [170].

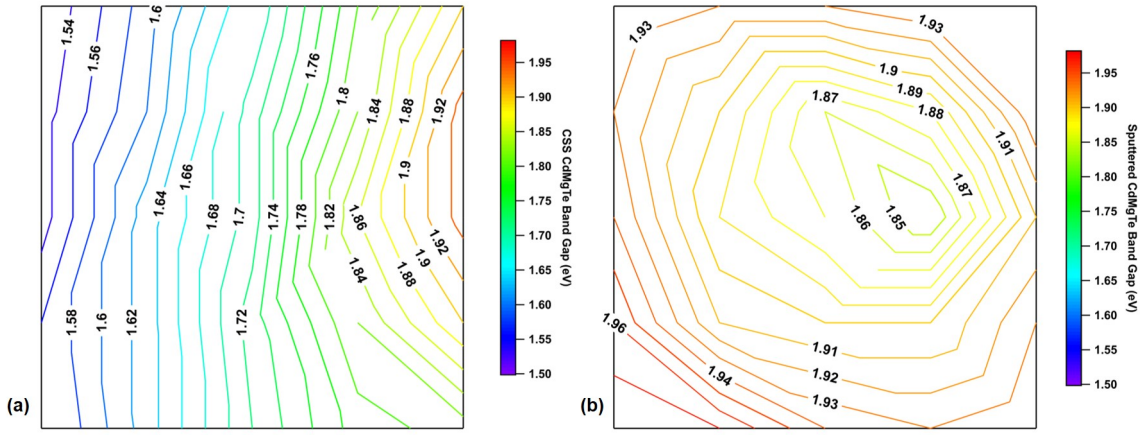

Figure 5.5: Band gap contour plots of CSS and sputter-deposited CdMgTe films (a) and (b) respectively, over the typical 8-cm substrate.

The most notable disadvantage of sputtered CdMgTe is that the deposition rate is much slower than that of co-sublimation (approximately 0.1-0.4 nm/sec vs. 5 nm/sec). Therefore

CSS-deposited CdMgTe is more scalable for manufacturing and enables the pursuit of slightly larger experimental data sets. However, this disadvantage in sputtered CdMgTe is weighted somewhat less heavily because it is centered around manufacturing concerns rather than the CdMgTe material properties most relevant in this work.

Both deposition systems utilized low-oxygen environments to minimize the formation of MgO although some oxidation can be present at the film surface due to vacuum breaks. For CSS, surface oxidation could be reduced by co-sublimation of CdMgTe in the same vacuum system as the absorber and passivation depositions, however initial experiments which implemented this configuration resulted in significantly slower deposition rates and a 3% absolute reduction in device performance as compared to the separate CSS system.

Independent of CdMgTe fabrication method, the thicknesses of the CdMgTe electron reflector and CdSeTe/CdTe absorber layers were separately optimized for the CdMgTe electron-reflector device structure. CdMgTe thicknesses of 50, 100, 150, and 200 nm were chosen based on modeling results by K.J. Hsiao which predicted little change in V_{OC} with thickness greater than 200 nm [70]. The measured light J-V data, given in Fig. 5.6, indicated that a 100-nm CdMgTe layer was optimal for device performance, and that performance reduction occurred with thicker CdMgTe, primarily through V_{OC} and fill factor. Given these data, a 100-nm CdMgTe layer was employed for all CdMgTe electron-reflector structures.

The absorber configuration was also optimized for the CdMgTe electron-reflector structure. Absorber thicknesses of 0.5-µm CdSeTe/0.5-µm CdTe, 0.5-µm CdSeTe/1.0-µm CdTe, and 0.5-µm CdSeTe/1.5-µm CdTe were fabricated with 100-nm CdMgTe at the back, and J-V data (not pictured) indicated that the 0.5-µm CdSeTe/1.0-µm CdTe devices were the most repeatable and highest-performing.

Two additional absorber/electron reflector configurations were also investigated to examine an alternative electron-reflector structure presented by K.J. Hsiao [70, 147], namely bulk band-gap reduction. In both structures, the CdSeTe layer served as the reduced bulk band-gap material. First, a thin CdTe (250 nm) layer was deposited at the back of a 1.25-µm

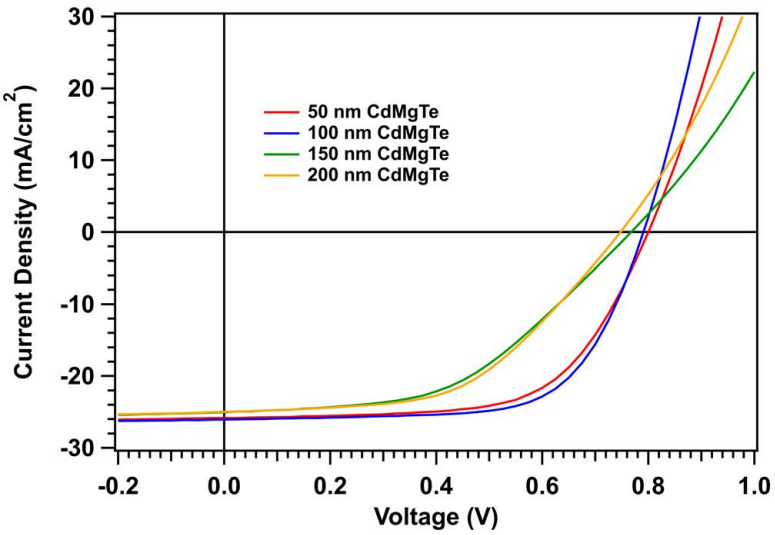

Figure 5.6: Light J-V curves of CdMgTe with varied thickness on 0.5-µm CdSeTe/1.0-µm CdTe absorbers shows an optimal thickness of 100 nm.

CdSeTe absorber such that the CdTe served as the "electron reflector" material. Resultant device performance was ∼12% (data given in Chapter 4, Fig. 4.12) and suggested no electron-reflector behavior. Second, thin CdMgTe with varied thickness (50, 100, and 150 nm) was deposited on 1.5-µm CdSeTe absorbers, and device performance was similarly limited. Device efficiencies did not exceed 11% due to V_{OC} and fill factor values below 720 mV and 57% respectively. Based on these initial mediocre results, possibly attributable in part to the difficulty of Cu-doping CdSeTe because of the copper acceptor formation energy increase at higher Se concentration [171], the bulk band-gap reduction configuration using a CdSeTe absorber was not pursued. All successive CdMgTe electron-reflector structures were fabricated on 0.5-µm CdSeTe/1.0-µm CdTe absorbers, henceforth referred to as CdSeTe/CdTe.

5.2 CSS-Deposited CdMgTe

5.2.1 Effects of Substrate Temperature on CSS CdMgTe Electron-Reflector Structures

To minimize $CdCl_2$ passivation loss in the CdSeTe/CdTe absorber and maintain magnesium and the CdMgTe band gap within the electron-reflector layer, substrate temperatures during CSS CdMgTe deposition were varied. CdSeTe/CdTe absorber devices were passivated with the optimized $CdCl_2$ treatment described in section 4.2 with subsequent CSS-CdMgTe deposition. Substrate temperature was controlled by dwell time in the CSS preheat source, and temperatures of 490, 452, 405, 362, 285, 200, and 130 °C were achieved for preheat times of 180, 150, 120, 90, 60, 30, and 0 seconds. Substrate temperatures were measured by a pyrometer in-situ, and the preheat time range was chosen to encompass high, CdMgTe-damaging temperatures [49, 122] and the lowest achievable temperature. The device structures for the non-CdMgTe containing reference and the CdMgTe electron-reflector devices are given in Fig. 5.7 (a) and (b) respectively. The Te layer was evaporated directly onto the CdMgTe to serve as both an oxidation-limiting buffer layer and back-valence-band-offset mitigation layer, and was followed by the Cu doping treatment described in section 4.2.

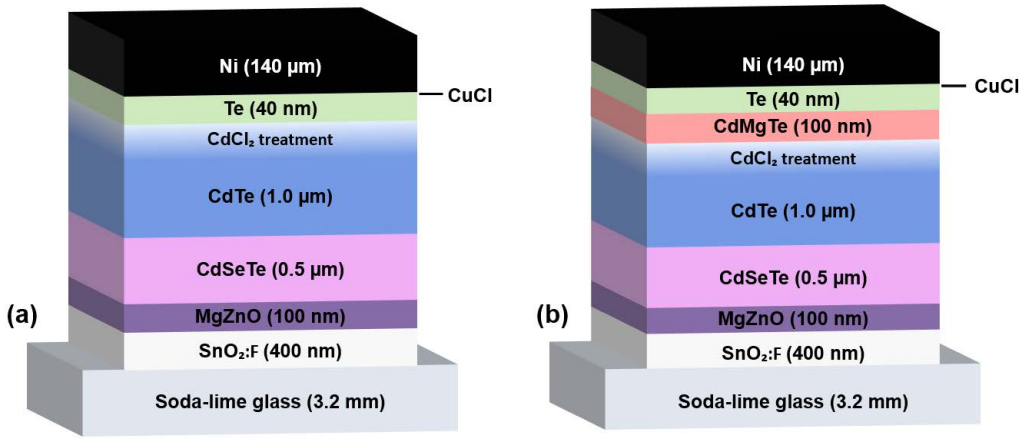

Figure 5.7: Device structures of the CdSeTe/CdTe reference devices (a) and CdSeTe/CdTe devices with CdMgTe CSS-deposited at different substrate temperatures (b).

To verify that the CSS-deposited CdMgTe band gap was maintained for all substrate temperatures, the Tauc plot method was applied to the temperature-varied CdMgTe transmittance data. The CSS-CdMgTe Tauc band gaps as a function of substrate temperature are given in Fig. 5.8 and demonstrated small variation over the temperature range, well within the desired CdMgTe band gap. Uncertainty in band gap, although fairly small, suggests that some lateral band gap change may occur over the device area.

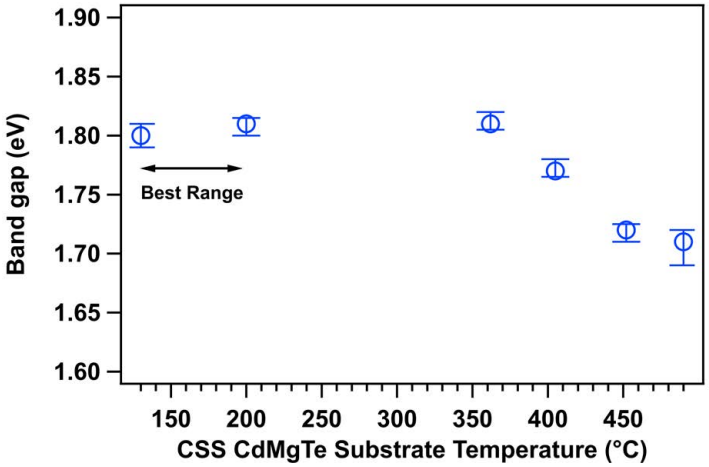

Figure 5.8: CSS-deposited CdMgTe band gap as a function of substrate temperature demonstrated small variation over the temperature range, well within the desired CdMgTe band gap. The best range indicates the combination of desired band gap and minimized temperature.

J-V characterization of devices fabricated with varied CSS substrate temperature demonstrated poor performance due to reductions in all J-V parameters. The best-performing devices improved slightly (from less than 1% to 2%) for lower substrate temperatures, although improvement appeared limited below approximately 285 °C.

Quantum efficiency, measured on all devices, is given in Fig. 5.9 for high, medium, and low substrate temperatures of 490, 362, and 285 °C for clarity. All trends discussed held for the full set of substrate temperatures. Photovoltaic conversion was poor for the highest substrate temperature, with notable reduction in the short to mid-wavelength range, suggestive of $CdCl_2$ passivation loss in the absorber and magnesium diffusion towards the front of the device [148]. For lower substrate temperatures, the quantum efficiency improved,

with enhanced photon conversion across all wavelengths, and especially in the short to mid-wavelength range which may indicate improved $CdCl_2$ retention and/or reduced magnesium diffusion.

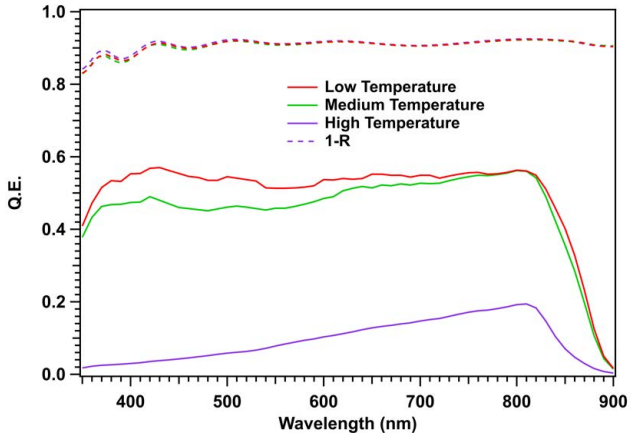

Figure 5.9: Quantum efficiency (solid lines) and 1-reflection (dashed lines) of best-performing CSS-deposited CdMgTe devices at substrate temperatures of 490, 362, and 285 °C showed improved photon conversion at lower substrate temperatures.

Dependence of $CdCl_2$ passivation retention on substrate temperature in CSS-CdMgTe deposition was also suggested by room-temperature PL and TRPL measurements. Room-temperature photoemission spectra, given in Fig. 5.10 (a) demonstrated a clear increase in photoemission intensity at lower substrate temperatures: there was no discernible peak for high temperature, a measurable peak for medium temperature, and a much higher peak at low substrate temperature. Since improved photoluminescence implies reduced defect-mediated radiative recombination [11] and PL emission is known to disappear for poor or no $CdCl_2$ passivation (as demonstrated in the Fig. 5.10 (a) inset), the PL data suggest that $CdCl_2$ passivation was poor and the absorber defect-ridden at high substrate temperatures, and that at lower substrate temperatures many defects were passivated through $CdCl_2$ retention.

Normalized single-photon TRPL decays given in Fig. 5.10 (b) demonstrated consonant trends: the slow part of the decay, the τ_2 lifetime, improved from ~2 ns to 15 ns with lower substrate temperatures, where τ_2 lifetimes were determined by fitting the tail of the TRPL

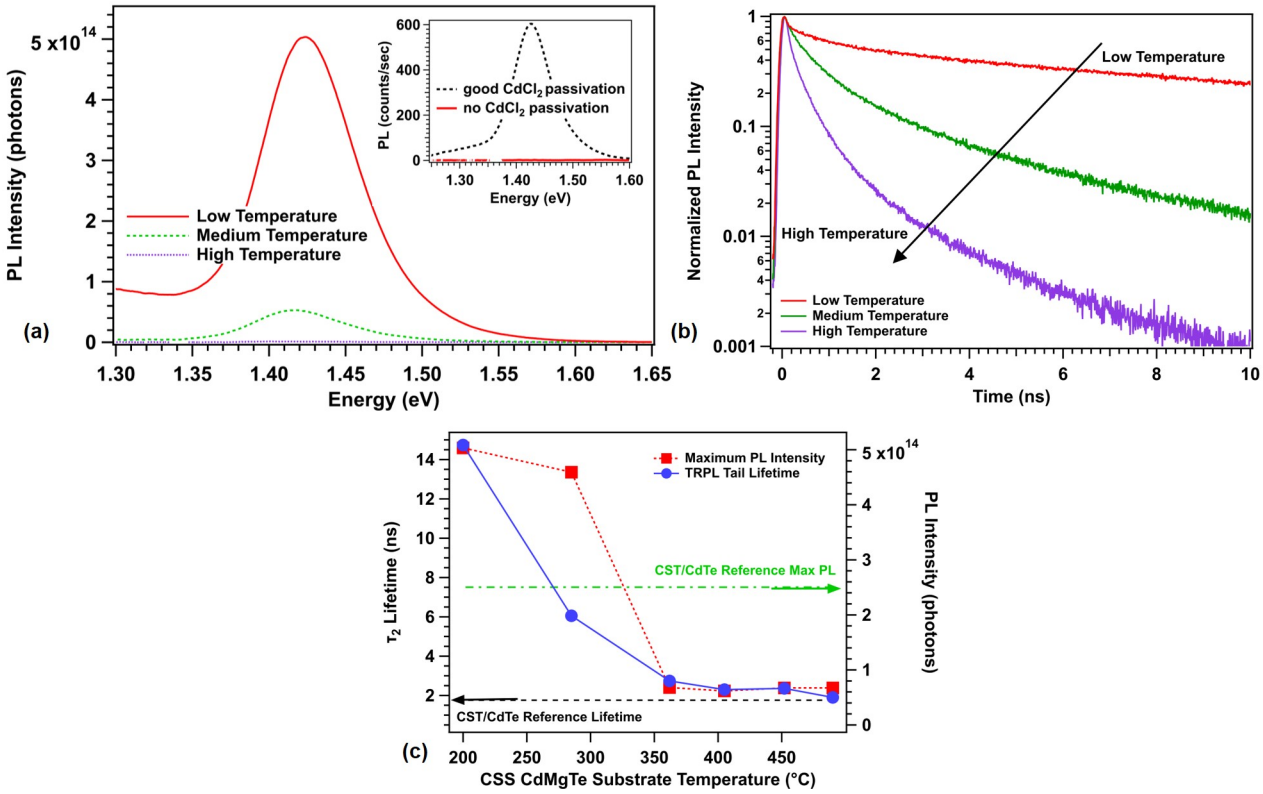

Figure 5.10: Room-temperature PL emission spectra (a) and TRPL decays (b) and their respective maxima and τ_2 lifetimes (c) show improvement with lower CSS-CdMgTe substrate temperatures. The inset in (a) demonstrates that little to no PL emission can be related to poor or insufficient $CdCl_2$ passivation.

decay data with an x-offset single exponential function. The increase in PL intensity and TRPL τ_2 lifetime at lower substrate temperatures is explicitly demonstrated in Fig 5.10 (c) for all temperatures. Given known improvement of CdTe bulk properties with sufficient $CdCl_2$ passivation [48, 172], correlation between τ_2 TRPL lifetimes and bulk recombination [39, 97], and improvement in τ_2 associated with $CdCl_2$ passivation [173, 174], the increase in τ_2 demonstrated in Figs. 5.10 (b) and (c) suggests better $CdCl_2$ passivation retention in devices with CdMgTe CSS-deposited at lower substrate temperatures.

$CdCl_2$ passivation was more explicitly investigated through TOF-SIMS measurements of film structures with CdMgTe CSS-deposited on CdSeTe/CdTe at substrate temperatures of 490 and 200 °C, and a well-passivated CdSeTe/CdTe sample was measured to provide a reference level for sufficient passivation. The chlorine profiles, given in Fig. 5.11, demonstrated that for a 200 °C substrate temperature the chlorine level was comparable to that of the reference throughout the absorber, whereas chlorine was significantly reduced throughout the absorber for a 490 °C substrate. This verified the initial interpretation of QE, PL, and TRPL data: higher substrate temperatures for CSS CdMgTe deposition on a $CdCl_2$-treated absorber reduce or eliminate $CdCl_2$ passivation, and likely cause the poor current collection, defect-limited photoluminescence, and shorter lifetimes in these devices. Alternatively, implementing a lower substrate temperature can maintain $CdCl_2$ passivation such that electronic and material properties improve. These data support previous experiments in which TEM and EDX images showed chlorine driven out of passivated absorbers for CSS-CdMgTe substrate temperatures above 400 °C [49, 123].

Despite good PL emission and τ_2 TRPL lifetimes, and maintenance of $CdCl_2$ passivation at lower substrate temperatures, J-V performance was poor for devices at all temperatures, and QE improved to only a limited extent. The reflection data in Fig. 5.9 were typical of well-behaved devices with ∼10% reflection across the wavelength range, which suggests device performance was not optically limited. The low quantum efficiency may be attributable to temperature-dependent material properties. First, in addition to $CdCl_2$ passivation loss at high substrate temperatures, temperature-dependent magnesium diffusion into the absorber

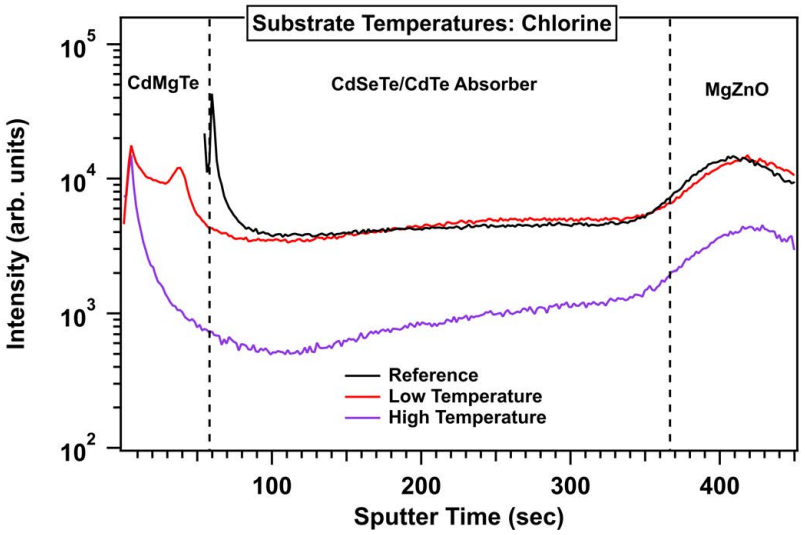

Figure 5.11: Cl SIMS profiles for 490 and 200 °C CSS-CdMgTe substrate temperatures compared to a non-CdMgTe-containing CdSeTe/CdTe reference demonstrates that $CdCl_2$ passivation can be maintained at low temperatures.

was observed in CdMgTe-containing structures. Fig. 5.12 provides magnesium SIMS profiles of the same film structures from Fig. 5.11. Magnesium diffusion into the absorber was present in both CdMgTe samples, but was more extensive for the 490 °C substrate compared to the 200 °C substrate. This diffusion likely alters absorber properties and device performance.

Second, for somewhat lower substrate temperatures (400 °C), non-uniform CSS CdMgTe film coverage with separated, un-coalesced surface grains has been documented [71]. It was suggested that this was associated with the start of columnar grain growth due to limited surface mobility of deposited atoms and fast condensation on the surface [71]. This observation, in tandem with the demonstrated temperature dependence of $CdCl_2$ retention, provides a possible explanation of the poor device performances within the investigated CSS substrate temperature range. At high substrate temperatures where CSS CdMgTe film quality may be superior, device performance seems to be limited by the loss of $CdCl_2$ passivation and extensive magnesium diffusion throughout the absorber layer, and at low substrate temperatures where $CdCl_2$ passivation is maintained, the device performance may be somewhat limited by non-uniform CdMgTe films.

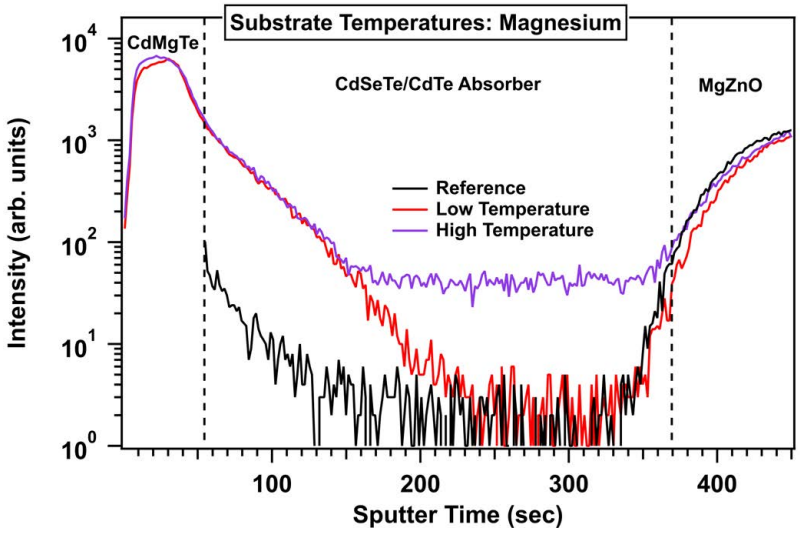

Figure 5.12: Mg SIMS profiles for 490 °C and 200 °C CSS-CdMgTe substrate temperatures compared to a non-CdMgTe-containing CdSeTe/CdTe reference. There is proper CdMgTe deposition at the back, and some Mg diffusion into the absorber layer which is more extensive for the 490 °C substrate.

5.2.2 Methods to Reduce Oxidation in CSS-Deposited CdMgTe Electron-Reflector Structures

In addition to $CdCl_2$ and magnesium-retention complications in CdMgTe, oxidation is a persistent difficulty. The Gibbs free energy favorability for MgTe to react with oxygen to form MgO combined with the vacuum break following CdMgTe deposition create opportunity for the CdMgTe film surface to oxidize before a buffer layer is deposited. Evidence of CdMgTe oxidation in CdTe/CdMgTe photovoltaic devices has been documented through paired TEM and EDX measurements and XPS [71, 148]. MgO, which appeared to form primarily at the film surface, has a large band gap (∼6.72 eV or greater) and ∼2.8 eV electron affinity such that a large valence-band offset would form at the back of the device and likely reduce fill factor and minimize effectiveness of the electron-reflector design [148, 175].

To minimize CdMgTe oxidation, chemical and material-based solutions were investigated through the independent use of a hydrochloric etch on the CdMgTe film surface and a CdTe

cap layer deposited on the CdMgTe. Results of the hydrochloric etch on CSS-CdMgTe are presented and discussed in section 5.3.2. The CdTe cap was investigated because of its previously reported success in limiting CdMgTe oxidation and improving device performance [64, 148]. The device structure is given in Fig. 5.13 where the 50-nm CdTe capping layer was CSS-deposited in the absorber vacuum system immediately after CdMgTe deposition. These structures were constrained in $CdCl_2$ treatment sequence since substrate temperatures were necessarily high (∼475 °C) for CSS-CdTe cap deposition: $CdCl_2$ passivation would not be retained for a single $CdCl_2$ treatment preceding the CdTe cap. Therefore a single $CdCl_2$ treatment following the CdMgTe/CdTe cap was implemented in these device structures. Given previous J-V characterization of CdTe-capped CSS CdMgTe devices which demonstrated slight performance improvement (0.4% absolute efficiency) for CSS-CdMgTe substrate temperature reduced from 405 to 285 °C [176], these devices were fabricated with the minimum 130 °C CSS CdMgTe substrate temperature.

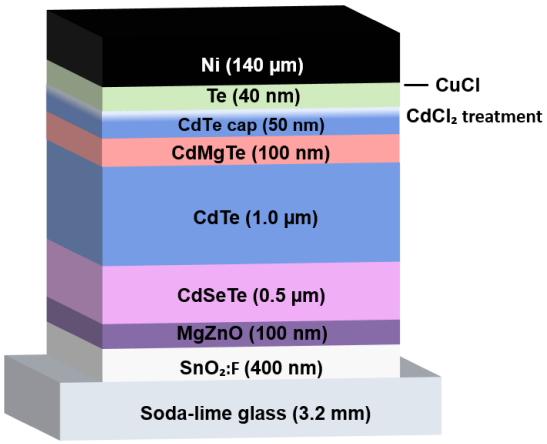

Figure 5.13: Device structure of a CdTe cap on CdMgTe to reduce CdMgTe film oxidation.

The CdTe-cap device demonstrated respectable device performance, but also presented material-based limitations. Light J-V data and parameters for the best-performing CdMgTe/CdTe cap device are compared to the CdSeTe/CdTe reference in Fig. 5.14. Although the CdTe cap on CSS-CdMgTe did not improve device performance compared to the non-CdMgTe-containing reference, it exceeded CdMgTe electron-reflector efficiencies previously reported [71, 148, 155]. The V_{OC}-driven performance reduction in the CdMgTe/CdTe cap

device was attributed to localized magnesium loss and diffusion from the CdMgTe layer into the CdSeTe/CdTe absorber based on SIMS and TEM/EDX measurements. The magnesium SIMS profiles for the CdTe-capped CSS-CdMgTe structure compared to the non-CdMgTe-containing reference are given in Fig. 5.15. The CdMgTe/CdTe cap profile showed notable magnesium diffusion into the absorber and a reduced level of magnesium within the CdMgTe layer (as compared to the back-side magnesium level in Fig. 5.12) which suggests magnesium loss in the CdMgTe via thermally-driven diffusion into the absorber due to the high-temperature CdTe cap and $CdCl_2$ treatments post-CdMgTe deposition. Oxygen profiles (not pictured) demonstrated no oxidation reduction in the CdMgTe as compared to the previously discussed CdMgTe structures.

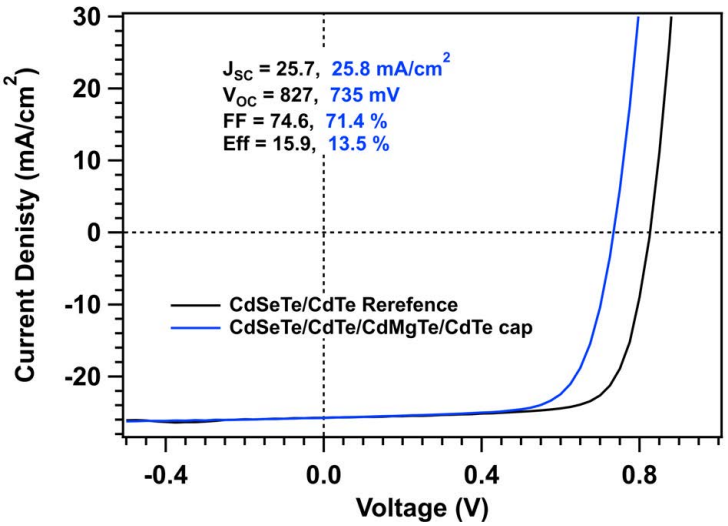

Figure 5.14: Light J-V curves of the best-performing CSS-CdMgTe/CdTe cap device compared to the CdSeTe/CdTe reference.

The magnesium loss in the CdMgTe layer appeared localized, as measured by TEM and EDX line scans given in Figs. 5.16 (a) and (b) respectively. The film cross section was FIB-prepared for EDX measurement (close to 300-nm thick), but the CdMgTe layer and non-uniformities were observable in the TEM image such that paired TEM-EDX characterization could be performed. EDX line scans were measured across the CdMgTe layer in

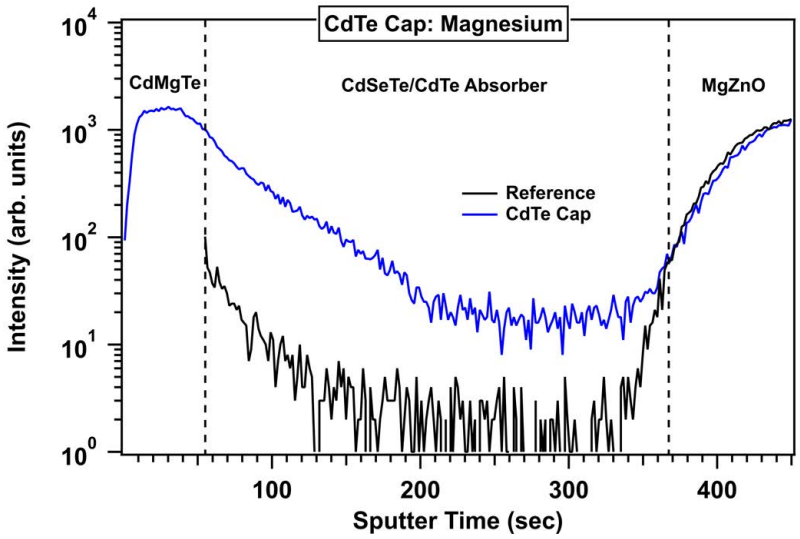

Figure 5.15: Magnesium SIMS profiles of the CdTe-capped CSS CdMgTe and CdSeTe/CdTe reference structures show magnesium loss in the CdMgTe layer and diffusion into the absorber.

regions with and without apparent CdMgTe, corresponding to line scans 1 and 2 respectively. Line scan 1 showed a peak in magnesium corresponding to the CdMgTe layer, while no detectable magnesium signal was measured by line scan 2. An affiliated oxygen peak was measured by line scan 1, which indicated that the CdTe cap did not effectively prevent oxidation of the CdMgTe layer. This is likely due to the vacuum break between the deposition of these two layers. The observed localized magnesium loss in the CdMgTe layer can induce spatially-dependent band gap variation, interface non-uniformities, and resultant increased recombination centers which likely explain the reduced V_{OC} in the CdTe-capped CdMgTe devices. Previous work has also associated device performance reduction with thermally-driven magnesium loss in CdMgTe absorbers [122] and localized magnesium loss in CdMgTe/CdTe cap structures [148]. Although the CdMgTe/CdTe cap electron-reflector configuration offered some efficiency improvements, the high temperatures and concomitant magnesium diffusion necessary to fabricate this structure inherently limit further performance improvements.

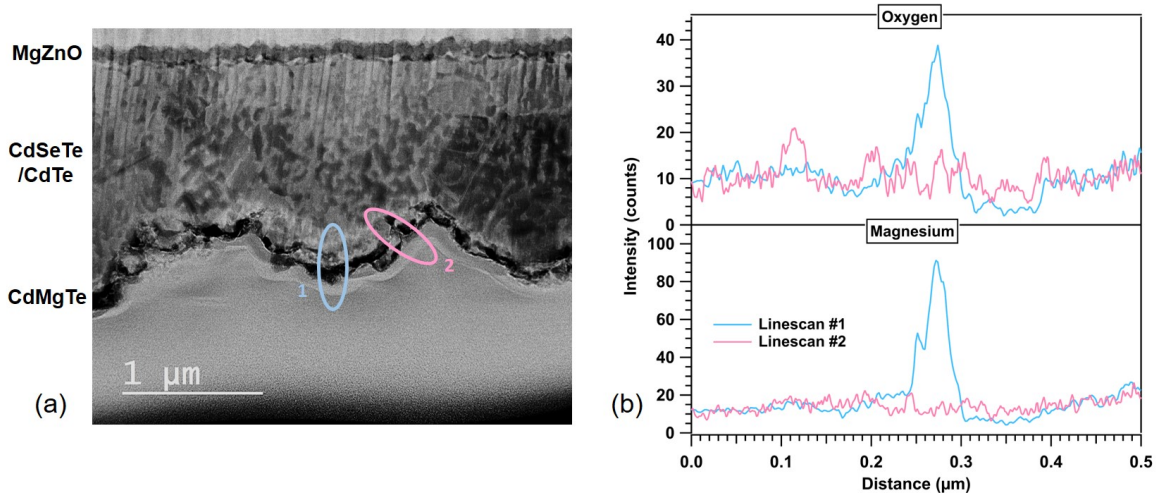

Figure 5.16: TEM cross section (a) and oxygen and magnesium line scans (b) across the CdMgTe layer showed localized magnesium loss and no notable oxidation reduction with the CdTe cap configuration.

5.3 RF Sputter-Deposited CdMgTe

5.3.1 Substrate Temperature Variation: Sputtered CdMgTe

To circumvent the $CdCl_2$ retention vs. magnesium loss problem in CSS-CdMgTe devices, CdMgTe electron-reflector devices were fabricated with an RF-sputtered CdMgTe layer with the substrate maintained at lower temperatures throughout CdMgTe deposition. CdMgTe was sputter-deposited on $CdCl_2$-treated CdSeTe/CdTe absorbers at room temperature, 100, 150, 200, and 250 °C, where the temperature range overlapped with low CSS-CdMgTe temperatures. Temperatures were set and controlled by an Omega PID controller with two redundant connections and stabilized for fifteen minutes before deposition. 150, 200, and 250 °C were quite stable, less than +/-2 °C throughout deposition, although greater temperature variation was observed for the 100 °C set point which may be attributable to non-optimized PID settings at that temperature. The room-temperature substrate, which had no applied temperature, saw an increase from ~20 to 25 °C throughout the deposition due to the sputter-induced energy increase. The 40-nm Te layer was evaporated onto the

CdMgTe and followed by Cu doping and application of the Ni back electrode. The sputtered CdMgTe device structure is that given in Fig. 5.7 (b).

Light J-V data of the best-performing CdMgTe devices at each substrate temperature are given in Fig. 5.17 and compared to the CdSeTe/CdTe reference. Table 5.2 provides the corresponding J-V parameters, and Fig. 5.18 gives J-V parameter box plots of all twenty-five devices at each substrate temperature. In Figs. 5.17 and 5.18, substrate temperature-dependent performance was observable: the mid-level (150 and 200 °C) temperature devices demonstrated highest performances and uniformity, followed closely by room temperature devices. 250 °C substrate devices showed a reduction in both device performance and uniformity, which was reduced further still for the 100 °C devices, although this was attributed in part to the non-negligible variation in applied temperature at that set point. Given the substrate temperature-dependent CSS CdMgTe data discussed in 5.2.1, the 250 °C sputtered device temperature may be high enough to induce some initial chlorine loss and/or magnesium diffusion such that device performance is slightly reduced. The highest CdMgTe device efficiency in this data set was achieved with a 150 °C substrate temperature, and exceeded that of the CdSeTe/CdTe reference. The efficiency improvement was due mainly to an increase in J_{SC}, and although measured V_{OC} values were close, the CdMgTe device V_{OC} did not exceed that of the reference which indicated that electron-reflector behavior was not fully realized.

Temperature-dependent J-V (J-V-T) was measured on sputtered CdMgTe devices (substrate temperatures equal to room temperature, 150 °C, and 250 °C) and compared to a CdSeTe/CdTe reference, and data are given in Figs. 5.19 (a)-(d). Thermoelectric cooling using a Peltier device, with liquid nitrogen-assisted cooling for temperatures below ∼268 K, was used to drive and monitor the device temperature during measurement. The temperature range generally extended from 298 to 223 K but varied slightly, dependent on J-V behavior: device performance deterioration (typically through poor fill factor) to a degree where data were no longer reliable dictated the selection of minimum measurement temperature. All CdMgTe device data showed rollover at low temperatures as expected, and

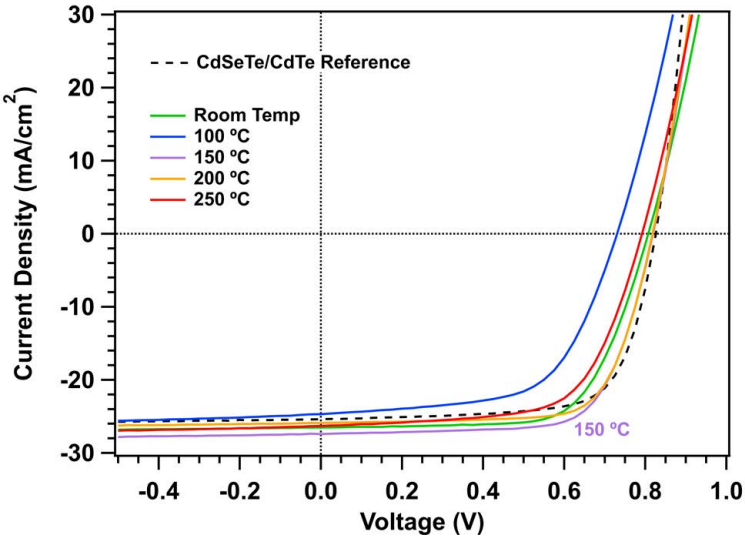

Figure 5.17: Light J-V curves for best-performing CdMgTe devices sputter-deposited at varied substrate temperatures.

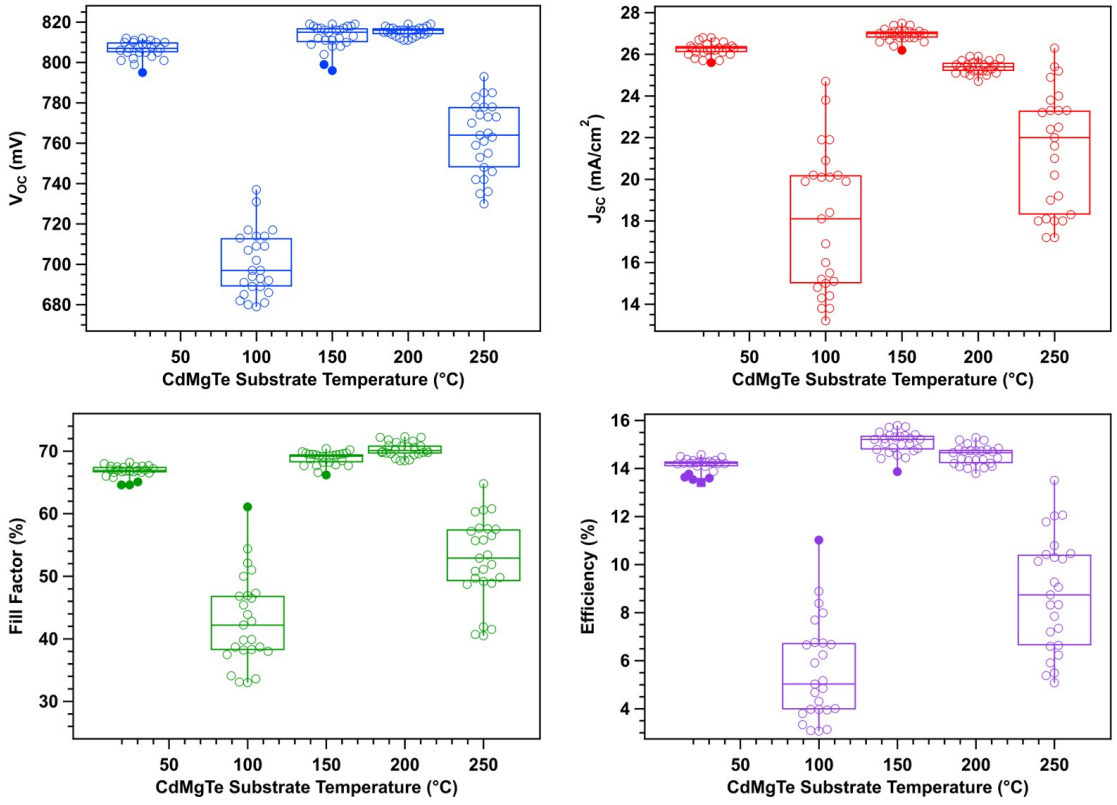

Figure 5.18: Room-temperature J-V parameter box plots of CdMgTe devices sputter-deposited at varied substrate temperatures.

Table 5.2: J-V parameters of best devices with varied substrate temperatures of sputtered-CdMgTe

Substrate Temperature (°C)	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor (%)	Eff (%)
Reference	0.826	25.4	71.3	15.0
Room Temperature	0.808	26.5	68.0	14.6
100	0.731	24.7	61.1	11.0
150	0.819	27.4	70.4	15.8
200	0.818	25.9	72.2	15.3
250	0.793	26.3	64.8	13.5

the room temperature and 250 °C CdMgTe data showed notable spread in J_{SC} and power quadrant data, whereas the 150 °C CdMgTe device data showed much less spread. With decreasing measurement temperature, the room temperature and 250 °C devices demonstrated an earlier onset of device degradation than the 150 °C device such that a slightly narrower temperature range was measurable in the former devices. The CdSeTe/CdTe reference data, although they showed minimal spread in the power quadrant, exhibited two rollover locations as lower temperatures were approached. The first in the power quadrant, in agreement with the CdMgTe devices rollover region, the second in the first quadrant, as observed in CdS/CdTe J-V-T data [71,75,177]. This may suggest different temperature-dependent front and back-barrier changes in CdMgTe and non-CdMgTe containing devices [32], although such differences were not quantified in this work.

V_{OC} should demonstrate a linear dependence on temperature, with an increase of approximately 2 mV per Kelvin decrease in CdTe devices. Fig. 5.20 shows the V_{OC} vs. temperature and linear fits to the data for each device from Fig. 5.19. The CdSeTe/CdTe reference device demonstrated non-linearity at lower temperatures which has been associated with low-temperature tunneling-assisted recombination [178], and may coincide with

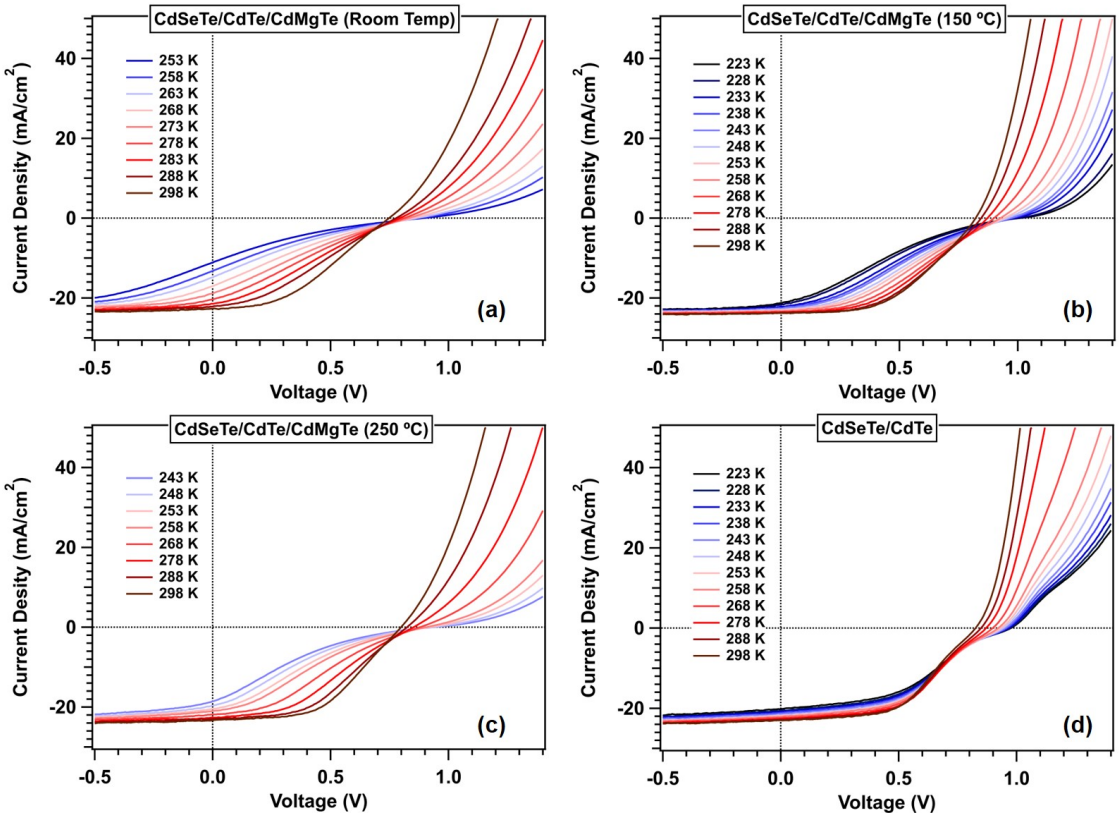

Figure 5.19: J-V-T curves of sputter-deposited CdMgTe devices with varied substrate temperatures compared to a CdSeTe/CdTe reference.

the atypical rollover behavior seen in the J-V data of Fig. 5.19 (d). The CdMgTe-containing devices maintained linear dependence of V_{OC} on temperature within their respective temperature ranges, where the 150 °C CdMgTe device V_{OC} vs. temperature demonstrated linearity within the widest measurement temperature range. This device achieved a measured V_{OC} in excess of 1 volt, which corroborates room temperature J-V data in that a 150 °C substrate temperature is optimal for sputtered CdMgTe deposition.

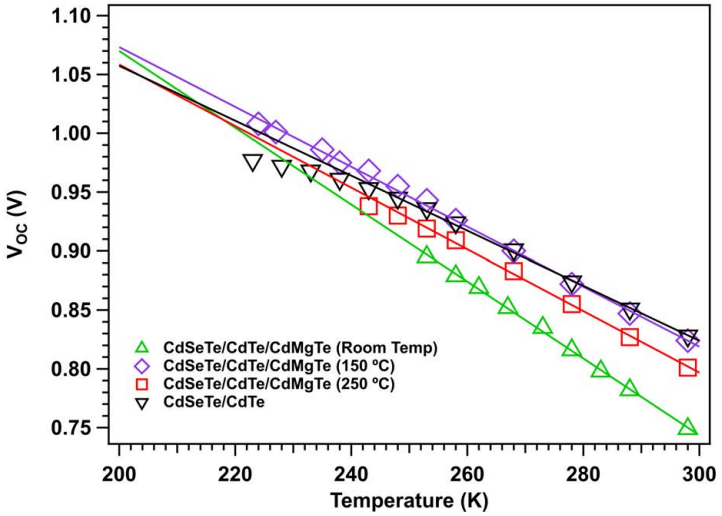

Figure 5.20: V_{OC} vs. temperature of CdMgTe devices deposited at varied substrate temperatures showed fairly linear behavior in the measurement temperature range. The CdSeTe/CdTe reference deviated from linearity at low temperatures.

Given the dependence of device performance on sputtered CdMgTe substrate temperature, and material-based dependencies on substrate temperature for CSS-deposited CdMgTe discussed in section 5.2.1 and [71,156,176], additional material characterization with scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDX), and glancing-angle X-ray diffraction (GAXRD) was performed on CdMgTe films sputter-deposited on TecSB at the above discussed substrate temperatures. TecSB glass was chosen as a substrate because its emissivity is close to that of CdTe such that sputtered CdMgTe film properties should be comparable to those in devices, although CdMgTe could be deposited on a Tec10/MgZnO/thin CdTe substrate for film characterization more fully representative of a device structure.

Planar SEM of the CdMgTe films, given in Fig. 5.21 with substrate temperatures indicated, was imaged with an accelerating voltage of 10 kV at a working distance of 10 mm. The sputtered CdMgTe grain structure and size demonstrated visible differences with substrate temperature. Room-temperature films had small, densely-packed and fairly uniform grains and at 100 °C, the CdMgTe film began to demonstrate larger underlying grain structure with additional small growth. The grain size and structure was most non-uniform at 150 °C: larger grains began to appear in what seemed to be the initial stages of grain coalescence with smaller grains packed in between. The non-uniform CdMgTe grain sizes were also apparent at 200 °C with small grains that remained present between larger ones and more distinct large-grain boundaries than those at 150 °C. Finally, at the highest substrate temperature of 250 °C the grain structure appeared more uniform with a slight decrease in average grain size. The observed variation in grain size and structure may be associated in part with differences in CdMgTe film thickness (Table 5.3) due to disparate deposition rates, but are not attributable to thickness variation alone; 100 and 250 °C films demonstrated differences in grain morphology despite equivalent thickness. Based on SEM grain information, the 150 and 200 °C-CdMgTe devices may have demonstrated better performance because of larger CdMgTe grain sizes.

Table 5.3: SEM and EDX Quantification of Varied Temperature CdMgTe Films.

Substrate Temperature (°C)	Film Thickness (µm)	Avg. Grain Size (nm)	**Composition: Atomic %** Cd	Te	Mg	O
Room Temperature	0.6	40-65	22	38	15	24
100	1.25	45-100	26	50	17	8
150	1.6	60-225	26	50	17	7
200	1.95	40-150	26	50	17	7
250	1.25	30-120	28	49	18	5

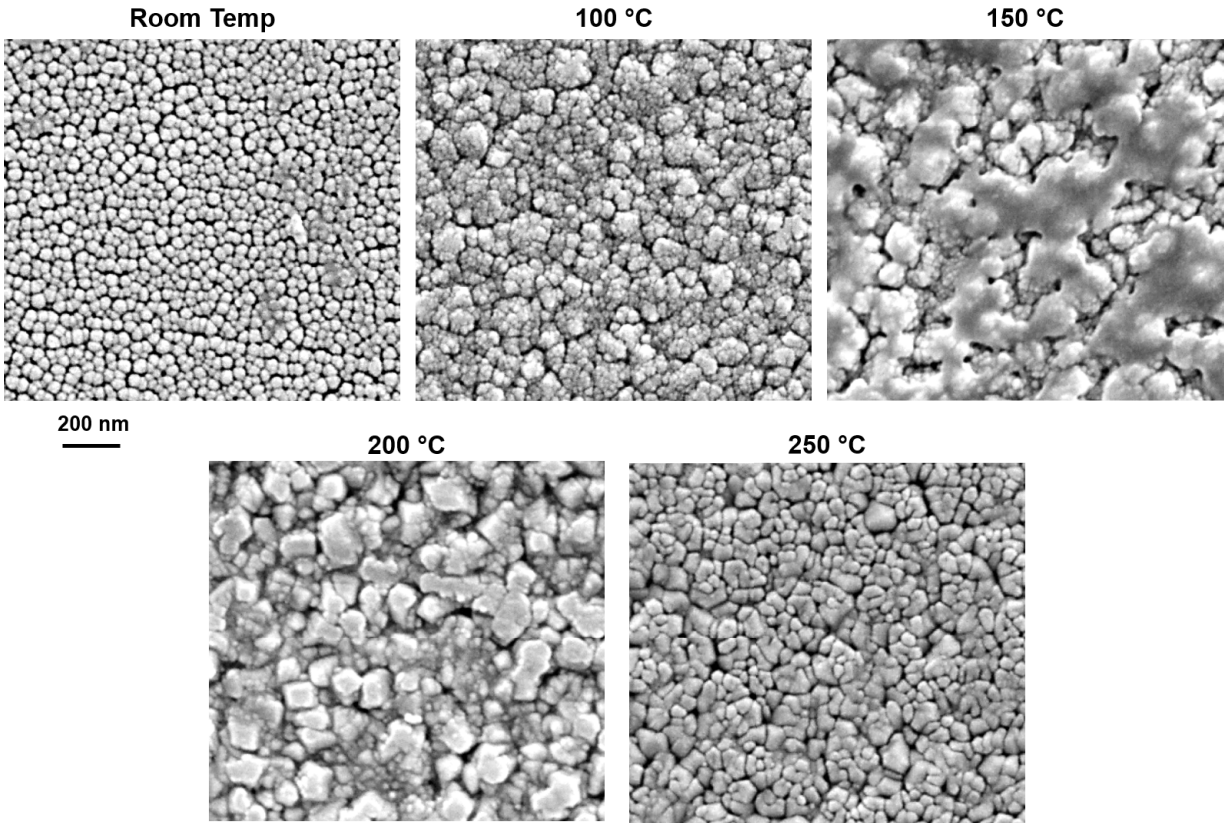

Figure 5.21: Planar SEM of CdMgTe films sputter-deposited with varied substrate temperature.

EDX maps of the SEM regions showed no detectable spatially-dependent elemental variation in any of the films, including the small-grain regions between larger ones. The elemental composition of the films at each temperature are given in Table 5.3, and on average cadmium comprised ∼25 atomic percent, and tellurium ∼50%. The small changes in magnesium and oxygen composition across substrate temperatures, apart from room temperature, were within EDX detection uncertainty such that sputtered CdMgTe film composition was not obviously substrate-temperature-dependent. The room-temperature film appeared to be the outlier with slightly lower cadmium, lower tellurium, and higher oxygen compositions. The increase in oxygen and decrease in tellurium suggests that MgTe likely reacted to form MgO. Given the lack of elemental temperature dependence in the other films and the reduced time the room temperature sample spent under vacuum (the temperature stabilization step was unnecessary), the elemental composition difference in the room temperature film was attributed to vacuum environment differences rather than substrate temperature. Despite structural non-uniformities at some temperatures, the CdMgTe elemental composition was fairly uniform with ∼15% magnesium composition such that no localized band gap variation was suspected.

GAXRD was measured on the same set of films reported in Table 5.3 using a Cu K-α (λ = 1.5406 Å) X-ray source and 2° incidence angle. The GAXRD spectra are given in Fig. 5.22 and labeled with the matched hkl diffraction planes of cubic $Cd_{0.85}Mg_{0.15}Te$ (PDF 04-023-7918). The data show that the CdMgTe films became more crystalline along the (111) plane with increasing substrate temperature. Peaks in room temperature data were only somewhat discernible from background, at $2\theta \approx 24°$, 40°, and 45°. The XRD peaks of the 100 ℃ film were somewhat more pronounced with a dominant (220) plane peak and secondary (111) and (311) plane peaks. For increasingly higher temperatures, the (220) and (311) peaks were reduced and the (111) peak intensity increased such that at 250 ℃ the CdMgTe film demonstrated the greatest crystallinity, with the (111) peak intensity more than three orders of magnitude greater than the (220) and (311) peaks.

Although the (111) orientation of the CdMgTe films became more dominant with increasing substrate temperature, no notable peak shifts in 2θ were observed. This indicates that the magnesium content in the films remained nominally unchanged with substrate temperature [123], in agreement with the EDX-determined elemental compositions.

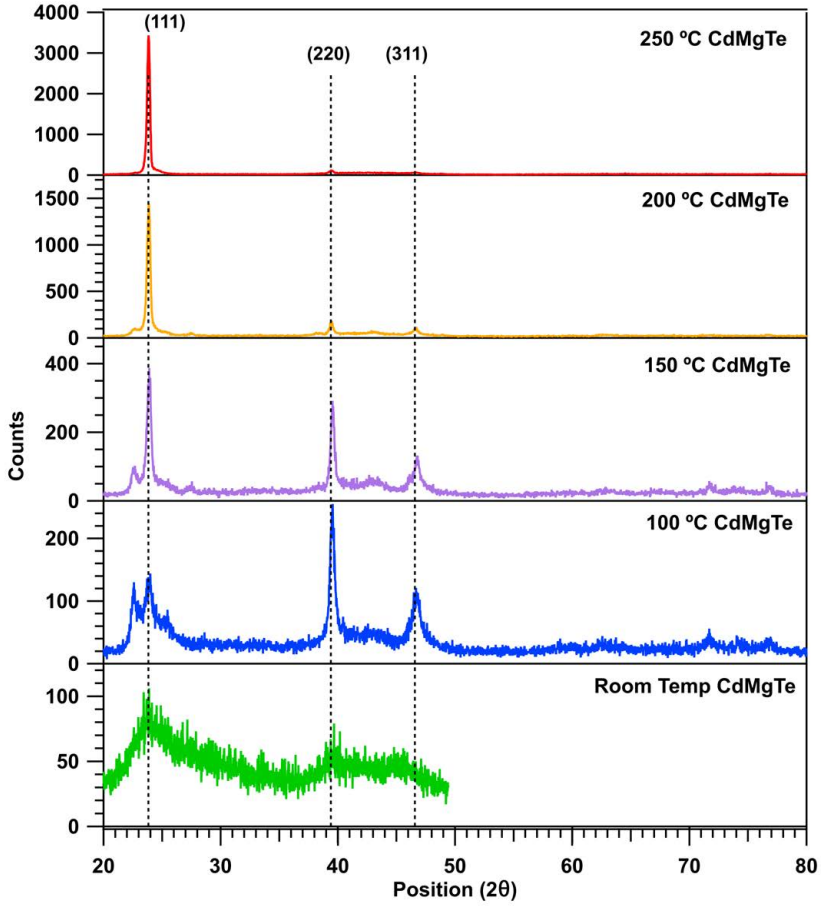

Figure 5.22: GAXRD spectra of CdMgTe sputter-deposited on TecSB at varied substrate temperature show increased crytallinity at higher temperatures.

5.3.2 Back Contact Variation

Cu Doping Optimization

The 100-nm CdMgTe layer behind the absorber presents an additional material layer through which Cu must diffuse to properly dope the absorber. Therefore the Cu-doping treatment, previously optimized to a 5-second Cu dose and 250-second anneal on CdSeTe/CdTe absorbers, was systematically varied for devices which had CdMgTe at the back. The same Cu treatment variation was also applied to CdSeTe/CdTe devices without CdMgTe to reliably separate effects of Cu doping and CdMgTe. Two Cu dose times of 200 and 300 seconds were employed with subsequent anneal times of 250, 500, and 750 seconds for each dose time, where times were selected based on a pursued balance between the hypothesized need for extended treatment times for CdMgTe devices and non-radiative recombination and reduced carrier lifetimes which can occur with increased Cu incorporation [179]. Box plots of the resultant J-V parameters are given in Fig. 5.23, where filled boxes correspond to CdMgTe-containing devices, and unfilled to the CdSeTe/CdTe reference devices.

In CdMgTe devices, all parameters demonstrated a clear improvement with longer Cu anneal time. Data showed that a longer Cu dose time offered the most substantial benefits given the shortest anneal time. The J-V parameter differential between the 300 and 200-second dose time was reduced with the 500 second anneal, and at the longest anneal time of 750 seconds, the 200 second dose-time devices outperformed those which were exposed to 300 seconds of CuCl sublimation. In contrast, the CdSeTe/CdTe reference devices showed slightly lowered V_{OC} and J_{SC} values and considerably reduced fill factor with longer anneal time such that device performance visibly decreased with longer Cu treatment. The opposing trends, most notably in anneal time, indicate that an extended Cu treatment is necessary for improved efficiency in devices with a CdMgTe electron-reflector layer. PL emission spectra (not pictured) showed the greatest photoluminescence for the CdMgTe devices with the longest Cu treatment times, which suggests non-radiative recombination associated with increased Cu may have remained limited within the explored Cu treatment

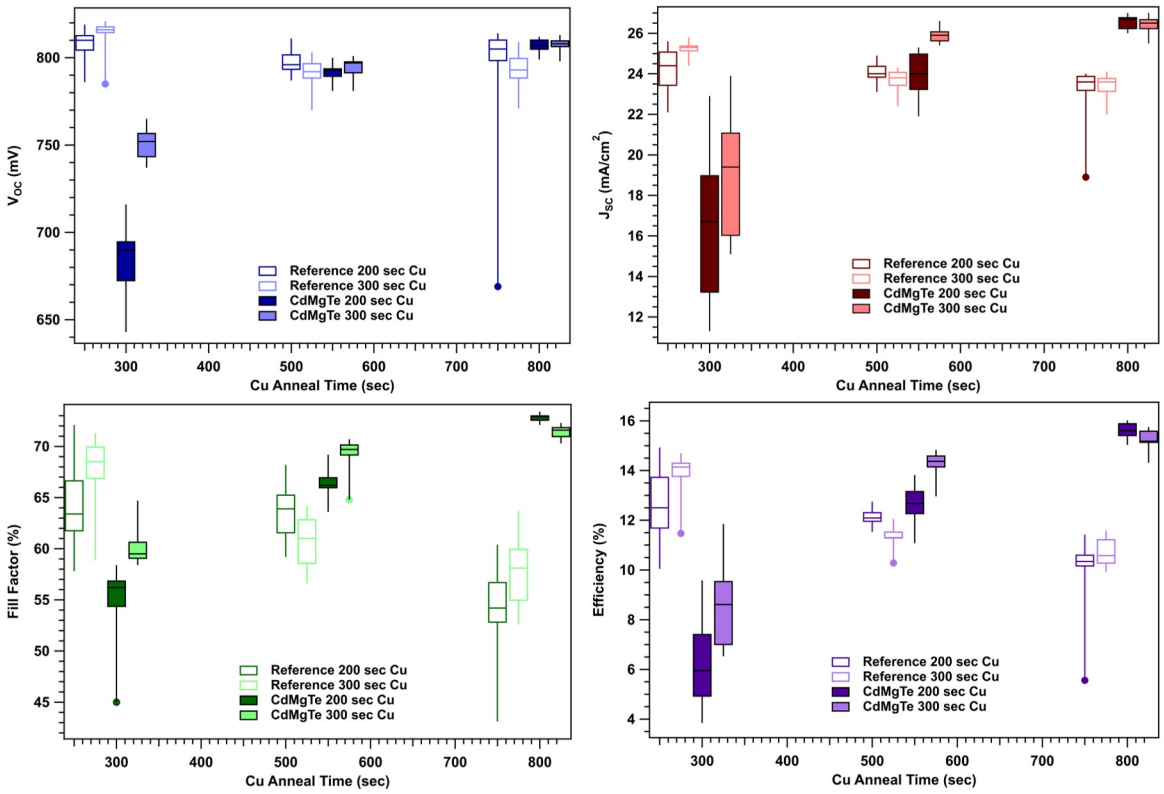

Figure 5.23: J-V parameter box plots of varied Cu doping treatment of CdMgTe-containing devices compared to CdSeTe/CdTe references.

range. To more specifically determine the optimal balance between increased Cu incorporation and minimized non-radiative recombination in the CdMgTe devices [179], additional experiments and analyses including dose and anneal temperature variation, low-temperature photoluminescence, TRPL, and external radiative efficiency would likely be required.

Electroluminescence images of the best-performing CdMgTe devices at each Cu condition, given in Fig. 5.24, showed clear improvement in EL intensity, and thus voltage deficit, with longer Cu anneal time. The EL images also emphasized the narrowed V_{OC} differential between 300 and 200-second dose times with increasing anneal time.

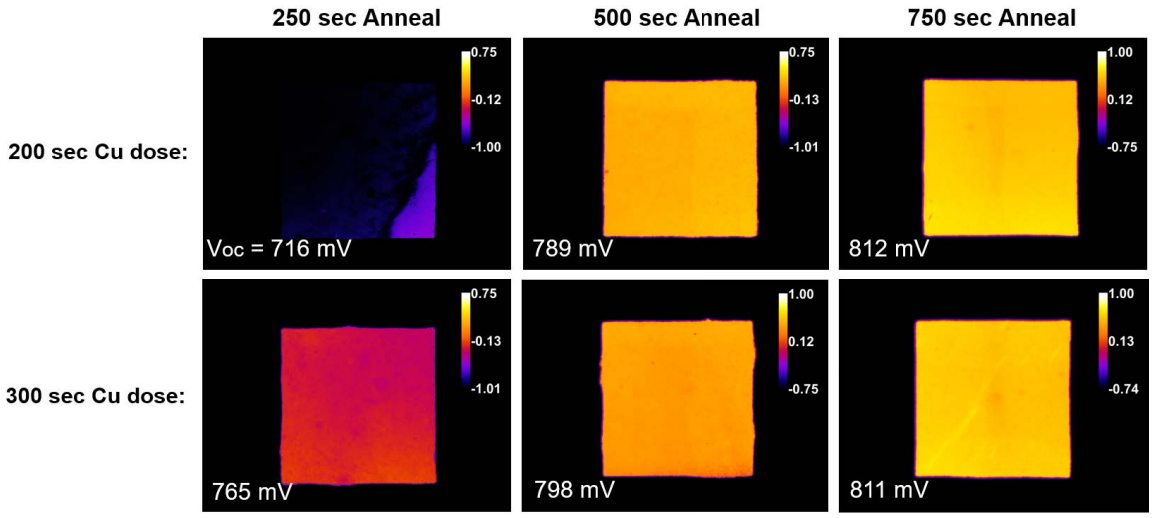

Figure 5.24: Electroluminescence images of best-performing CdMgTe devices with varied Cu doping show notable improvement in EL intensity and associated V_{OC} at longer Cu treatments.

Within the investigated anneal time range, longer anneal times promoted substantial CdMgTe-device-performance improvement such that the highest-performing CdMgTe electron-reflector device to date was achieved with an efficiency of 16.0%, V_{OC} = 812 mV, J_{SC} = 26.9 mA/cm^2, and fill factor = 73.3%. The asymptotic trend in J-V parameters with anneal time suggested that longer Cu anneal times would not be notably beneficial to device performance. Thus the 200-second Cu dose and 750-second anneal was implemented as the optimized Cu doping treatment for CdMgTe devices, and the previously optimized 5-second

dose, 250-second anneal treatment was maintained for thin CdSeTe/CdTe devices without CdMgTe.

Successes and limitations associated with Cu-doped CdTe-based absorbers are well documented [179–184] but previous experimental studies of Cu-doped CdMgTe are limited [64,71]. As demonstrated in Fig. 5.23, the CdSeTe/CdTe asborber can be sufficiently doped through the CdMgTe layer such that favorable device performances are achieved. To determine whether Cu doping through the CdMgTe layer was necessary, i.e. whether the CdMgTe material benefits from Cu doping, CdSeTe/CdTe/CdMgTe structures were fabricated with Cu doping before or after the CdMgTe/Te deposition. For the structures which were Cu-doped through the CdMgTe/Te layers, the 200-second Cu dose and 750-second anneal treatment was employed, and for the structures on which Cu doping preceded the CdMgTe deposition, the 5-second Cu dose and 250-second anneal was employed. J-V data for the two configurations are given in Fig. 5.25 (a) for both room temperature and 150 °C CdMgTe substrate temperatures and compared to a CdSeTe/CdTe reference. The corresponding J-V parameters are listed in Table 5.4.

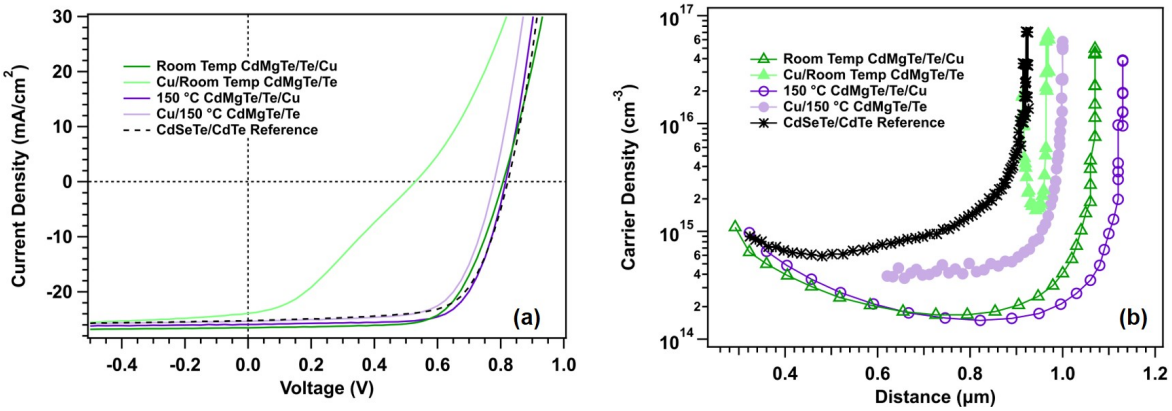

Figure 5.25: (a) J-V and (b) carrier density curves of best-performing CdMgTe devices with Cu-doping preceding and following CdMgTe/Te deposition.

The CdMgTe devices which were Cu-doped after CdMgTe and Te depositions demonstrated diode behavior and performance parameters comparable to the optimized devices

Table 5.4: J-V parameters of best-performing devices with varied CdMgTe/Cu doping order

Structure	V_{OC} (mV)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
R.T. CdMgTe/Te/Cu	808	26.5	68.0	14.6
Cu/R.T. CdMgTe/Te	530	23.9	32.5	4.1
150 °C CdMgTe/Te/Cu	816	25.9	71.2	15.1
Cu/150 °C CdMgTe/Te	780	25.4	68.5	13.6
CdSeTe/CdTe Reference	823	25.2	68.6	14.3

given in Fig. 5.23. The 150 °C substrate CdMgTe device also had slightly better performance than the room-temperature device through higher V_{OC} and fill factor, in agreement with the substrate temperature device data presented in section 5.2.1. In both the 150 °C and room-temperature substrate cases, devices which were Cu-doped preceding CdMgTe sputter deposition demonstrated reduced performance primarily due to lowered V_{OC}, which is suggestive of insufficient Cu doping. This was especially apparent in the room-temperature CdMgTe substrate device: V_{OC} was quite low and the diode curve exhibited a slight kink, suggestive of a back-barrier formation [185]. Carrier density profiles given in Fig. 5.25 (b) show that the devices with Cu doping through the CdMgTe demonstrated carrier densities in the 10^{14} cm^{-3} range, and widths close to the absorber thickness, typical of properly-doped CdTe devices. Devices in which Cu doping preceded the sputtered CdMgTe demonstrated artificially high carrier concentrations over a narrow range, more extremely in the room temperature substrate case. The carrier density and J-V data indicate that in these CdMgTe electron-reflector structures, the CdMgTe material benefits from Cu doping such that performance improvement can be realized.

Post-Sputtered CdMgTe Treatments

As introduced in section 5.2.2, a HCl etch on the CdMgTe layer was investigated to reduce oxidation and contaminants at the CdMgTe surface and was incorporated in both CSS-CdMgTe and sputtered-CdMgTe structures. For CSS CdMgTe, the CdMgTe was deposited at a substrate temperature of 130 °C on a $CdCl_2$-treated CdSeTe/CdTe absorber and etched in a 10% HCl solution in deionized (DI) water for 5 seconds followed by a DI water rinse [186, 187]. A milder, 0.5% HCl solution in DI water was used as the etchant for 5 seconds on sputtered CdMgTe. To prevent further oxidation in both cases, a 40-nm Te buffer layer was evaporation-deposited at room temperature onto the etched CdMgTe film.

The light J-V data and parameters for the best-performing strong and mild HCl-etched CdMgTe devices are compared to a typical un-etched CdMgTe device in Fig. 5.26. The J-V data showed improvement in device performance predominantly through V_{OC} for the 0.5% HCl-etched sputtered CdMgTe device as compared to the 10% HCl-etched CSS CdMgTe device. This improvement may stem in part from the advantageous sputter deposition of CdMgTe, but can also be attributed in large part to magnesium retention in the CdMgTe layer. This is demonstrated in Fig. 5.27 (a) which shows the magnesium SIMS profiles for the same 10% and 0.5% HCl-etched CdMgTe structures. The 0.5% HCl etch structure demonstrated maintenance of magnesium in the CdMgTe layer whereas the 10% HCl etch proved too aggressive; magnesium was removed from the CdMgTe layer to a level comparable to a non-CdMgTe CdSeTe/CdTe reference and may have caused film damage to the CdTe surface. Despite good device performance with a milder etch, the oxygen SIMS profiles shown in Fig. 5.27 (b) indicated that CdMgTe oxidation was not reduced as intended. This is likely due to a chemical reaction ($MgTe + H_2O + CdCl_2 \rightarrow MgO + CdTe + 2HCl$) which has a favorable Gibbs free energy such that MgO will form given the presence of MgTe, H_2O, and $CdCl_2$ [71]. Considering the seemingly unavoidable formation of MgO given the device structure and HCl etch solution, and nominally equivalent diode behavior and performance between an un-etched and 0.5%-etched CdMgTe device, the extra device preparation step with a HCl etch of CdMgTe was deemed unnecessary and not pursued further.

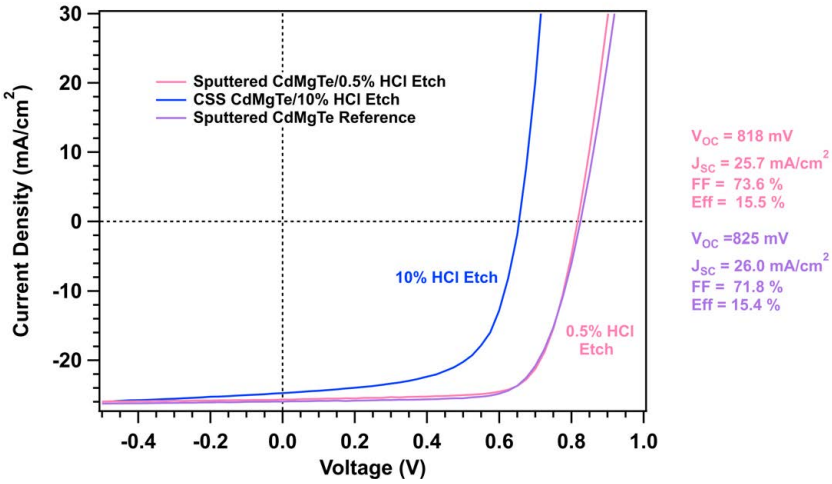

Figure 5.26: Light J-V curves of a 0.5% HCl-etched sputtered CdMgTe device demonstrates comparable device performance to a typical un-etched CdMgTe device, and notable performance improvement over the 10% HCl-etched CSS-CdMgTe device.

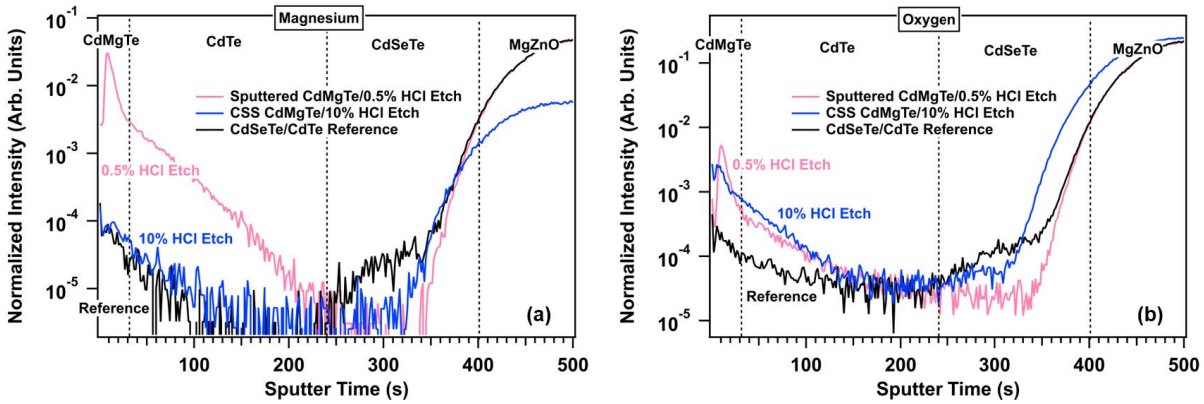

Figure 5.27: Magnesium (a) and oxygen (b) SIMS profiles of HCl-etched CdMgTe structures show magnesium maintenance in the CdMgTe with a 0.5% etch but no clear reduction in oxidation.

In the pursuit of reduced oxidation, a 50-nm CdTe cap on a sputtered CdMgTe layer was also investigated. The best device demonstrated low performance (V_{OC} = 767 mV, J_{SC} = 25.1 mA/cm^2, fill factor = 65.4%, and efficiency = 12.6%), some reduced photon conversion of approximately 5% in the mid-to long wavelength ranges as measured by QE, and low photoluminescence (not pictured). Given material characterization of CdTe-capped CSS CdMgTe devices, the sputtered CdMgTe/CdTe cap devices also likely suffered performance reduction due in large part to temperature-induced magnesium degradation in and diffusion from the CdMgTe layer, with no decrease in oxide formation. As in the CSS-CdMgTe case, the CdTe cap structure was not pursued further.

Given the continued need to curb MgO formation at the CdMgTe surface, and the demonstrated importance of optimized Cu doping conditions for high-efficiency CdMgTe electron reflector-devices, the order of Cu and Te depositions following CdMgTe was also examined. A direct comparison was made by fabricating two structures with different back contact configurations after the sputtered CdMgTe layer: a 40-nm Te buffer layer evaporated directly onto the CdMgTe with subsequent Cu treatment versus Cu treatment directly following CdMgTe with subsequent Te deposition. The 200-second Cu dose and subsequent 750-second anneal treatment was employed for Cu doping. The resultant J-V data and corresponding parameters are given in Fig. 5.28.

Better device performance was demonstrated for Te deposited directly onto the sputtered CdMgTe with subsequent Cu doping. Performance improvement was driven by the differentials in V_{OC} and fill factor, where V_{OC} improved from 789 to 810 mV and fill factor from 70.8% to 74.4%. The improvement in fill factor in the Te/Cu device stemmed from an increase in the maximum power point and reduced series resistance, which decreased from 2.2 to 1.1 Ωcm^2 for the Cu/Te and Te/Cu structures respectively.

The initial hypothesized cause of improved V_{OC} was that the Te layer deposited directly onto CdMgTe acted as an oxidation-limiting layer in addition to its intended back valence-band-offset mitigation. To verify this, TOF-SIMS was measured on the sputtered

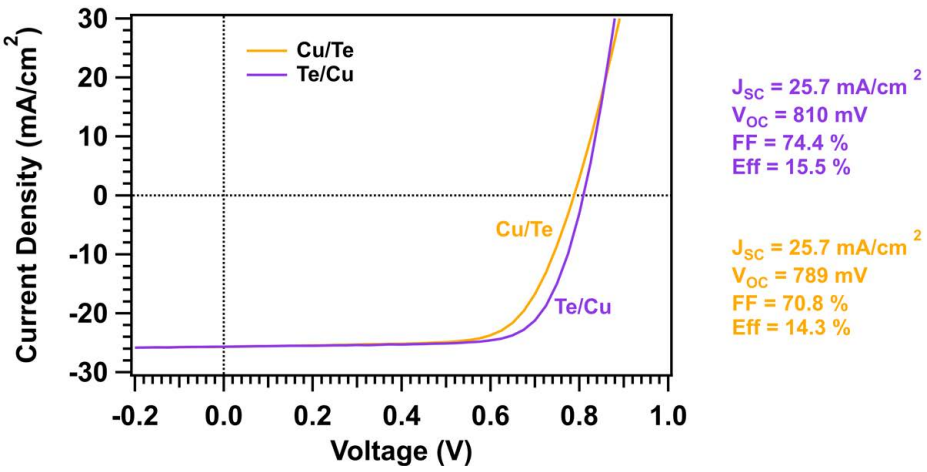

Figure 5.28: Light J-V curves of sputtered CdMgTe devices with Cu/Te order variation show some improvement with a Te/Cu back-contact order. From [188].

CdMgTe structures with Te/Cu and Cu/Te order variation and compared to a non-CdMgTe-containing CdSeTe/CdTe absorber structure. The oxygen SIMS profiles, given in Fig. 5.29 (a) showed high, apparently equivalent levels of oxygen at the back of both CdMgTe structures as compared to the CdSeTe/CdTe reference. The magnesium profiles, given in Fig. 5.29 (b) indicated that magnesium was retained in the CdMgTe layer equally well for the Cu/Te and Te/Cu back structures, but that there was a difference in diffusion into the absorber. The Cu/Te structure showed more extensive diffusion and higher levels of magnesium in the absorber (and corresponding oxygen signatures due to CdMgTe proclivity for MgO formation) than the Te/Cu structure. Due to the somewhat elevated temperatures of the CSS Cu deposition and anneal, the magnesium diffusion was likely thermally-driven, and somewhat inhibited by the Te buffer layer in the Te/Cu configuration. Therefore, the Te/Cu back structure likely improved device performance because Te additionally acts as a buffer layer which minimizes thermally-driven diffusion of magnesium from the CdMgTe into the absorber. Given association between magnesium diffusion and reduced V_{OC} in CdMgTe electron-reflector devices observed in this work, the V_{OC}-induced device-performance reduction in the Cu/Te back configuration may be attributed to increased back-to-front side magnesium diffusion in those structures.

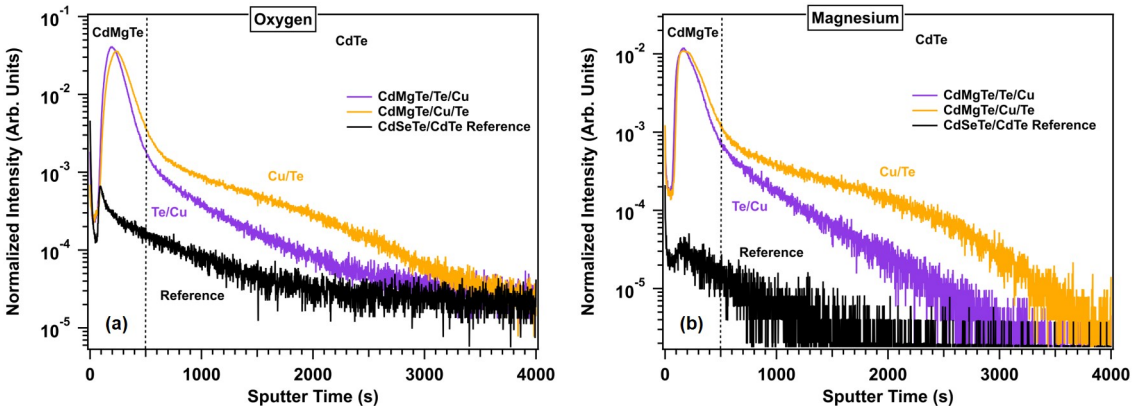

Figure 5.29: SIMS oxygen (a) and magnesium (b) profiles with Te and Cu order variation on sputtered CdMgTe demonstrate less magnesium diffusion from the CdMgTe into the absorber for CdMgTe/Te/Cu configuration.

Time-resolved photoluminescence (TRPL) measurements corroborated the Te/Cu configuration as more favorable than Cu/Te. Single-photon TRPL measured with 50 µW laser excitation from the front side of each device, given in Fig. 5.30, showed an increase in tail lifetime from the Cu/Te to Te/Cu configuration. τ_2 lifetimes of 2.1 ± 0.03 ns, 2.5 ± 0.03 ns, and 1.0 ± 0.02 ns for the CdSeTe/CdTe reference, CdMgTe/Te/Cu, and CdMgTe/Cu/Te devices respectively were determined with single exponential fits to the tail of the TRPL decays. Since τ_2 is typically associated with bulk and interface recombination [174], and bulk differences between Cu/Te and Te/Cu samples are evident in SIMS profiles, the longer τ_2 lifetime for Te/Cu was attributed in part to reduced bulk recombination. Given reported correlation between TRPL lifetime and V_{OC} in Cu-doped CdTe devices [129], this also corroborates the improvement in measured V_{OC} for these devices.

5.4 Comparisons Between CSS and Sputter-Deposited CdMgTe

As discussed in section 5.1.3, there are many fabrication-induced material differences between CSS and sputter-deposited CdMgTe. Given the final optimized structure and fabrication conditions for the two CdMgTe deposition methods, this section presents direct comparisons between the CSS and sputter-deposited CdMgTe electron-reflector structures.

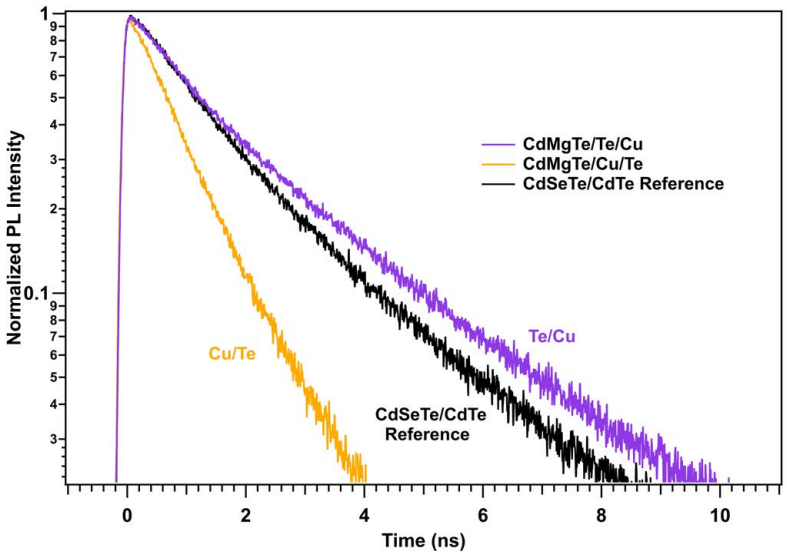

Figure 5.30: Single-photon TRPL decays show longer lifetimes for Te/Cu compared to Cu/Te on sputtered CdMgTe.

The best-performing devices for CSS and sputter-deposited CdMgTe electron-reflector structures were CSS-CdMgTe/CdTe cap/$CdCl_2$/Te/Cu and $CdCl_2$/sputtered-CdMgTe/Te/Cu on Tec10/100 nm MgZnO/0.5 µm CdSeTe/1.0 µm CdTe. Light J-V data are compared for the two CdMgTe devices and the best-performing CdSeTe/CdTe reference device in Fig. 5.31, and Table 5.5 provides the corresponding J-V parameters. The CdMgTe data showed a clear improvement in device performance, predominantly through greater V_{OC}, for the sputtered CdMgTe electron-reflector device.

Table 5.5: J-V parameters of best-performing CSS and sputter-deposited CdMgTe devices and CdSeTe/CdTe reference device.

Device	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
Sputtered CdMgTe	812	26.9	73.3	16.0
CSS CdMgTe	735	25.8	71.4	13.5
CdSeTe/CdTe Reference	829	27.6	72.7	16.6

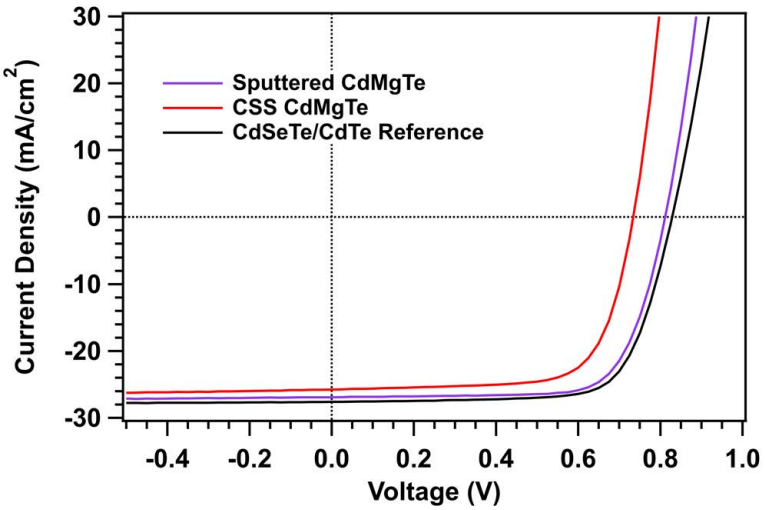

Figure 5.31: Light J-V data of the best-performing CSS and sputter-deposited CdMgTe devices show notable V_{OC} improvement with sputtered CdMgTe.

Although the best-performing reference device had a slightly higher efficiency than the sputtered CdMgTe device, the latter demonstrated superior uniformity and J-V parameters for all devices across the substrate. J-V parameter box plots of the three configurations are given in Fig. 5.32, where the sputtered CdMgTe and CdSeTe/CdTe box plots encompass full-plate device data and CSS CdMgTe encompasses half-plate data. The V_{OC} data mirrored the best device data from Table 5.5: CSS CdMgTe devices demonstrated markedly reduced V_{OC} and sputtered CdMgTe device V_{OC}s were only slightly lower than the reference. J_{SC} values were comparable between the sputtered CdMgTe and reference devices, and were lower with considerable spread in CSS CdMgTe devices. The sputtered CdMgTe plate showed excellent fill factor and efficiency uniformity, while the CSS CdMgTe and reference plates showed poorer uniformity. The sputtered CdMgTe plate uniformity could be due to CdMgTe spatial band gap variation that offsets spatial variation present in other material layers. Although the best sputtered CdMgTe device performance and V_{OC} were slightly lower than that of the CdSeTe/CdTe reference, the parameter differential was fairly small and overall plate efficiency was superior, which suggests that the sputtered CdMgTe structure works in some part as an electron-reflector device, but complete effectiveness remains somewhat limited.

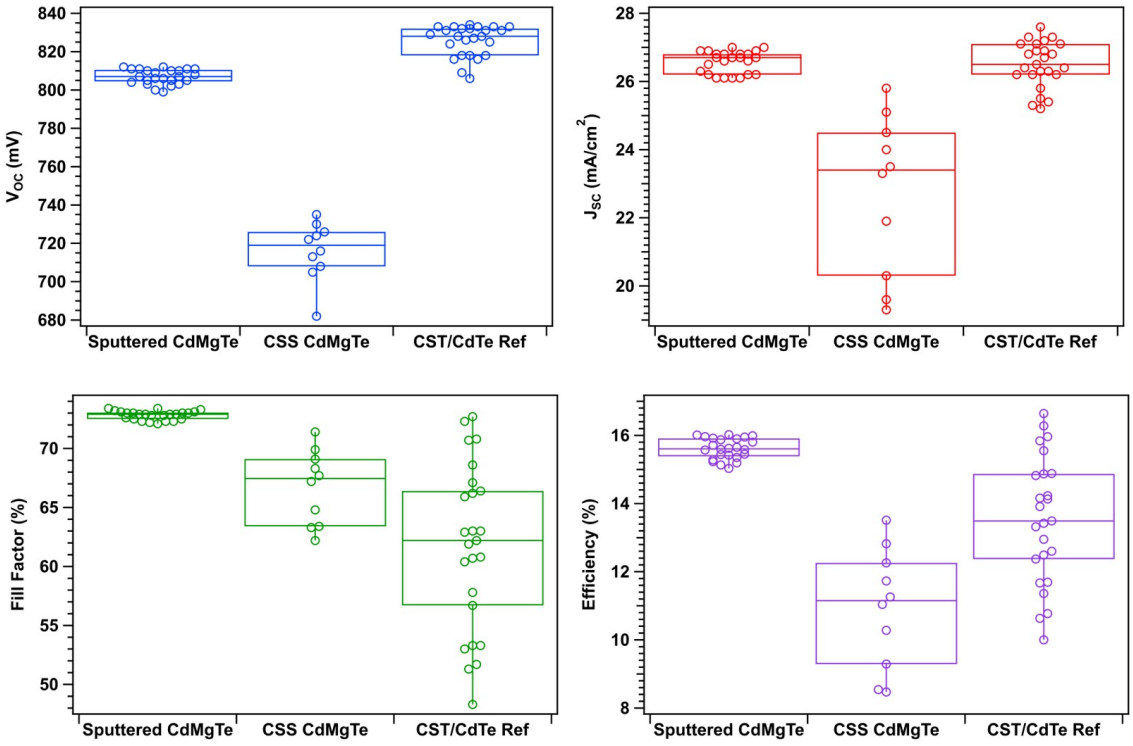

Figure 5.32: J-V parameter box plot comparison of CSS and sputtered CdMgTe devices and CdSeTe/CdTe reference. Sputtered CdMgTe and CdSeTe/CdTe box plots encompass full-plate device data, CSS CdMgTe encompasses half-plate data.

Electroluminescence images provided a clear visual representation of the voltage deficit differential between the three device structures and are given in Fig. 5.33. EL of the CSS CdMgTe device was visibly poorer than the sputtered CdMgTe and reference devices such that a different scale was necessary for image clarity. Given the proportional relationship between the natural log of EL intensity and reduced voltage deficit, the CSS CdMgTe device had a greater voltage deficit than the other devices, in agreement with V_{OC} measured by J-V. The sputtered CdMgTe and CdSeTe/CdTe reference had comparable EL intensities, affiliated with their similar V_{OC}s and the sputtered CdMgTe device demonstrated superior uniformity.

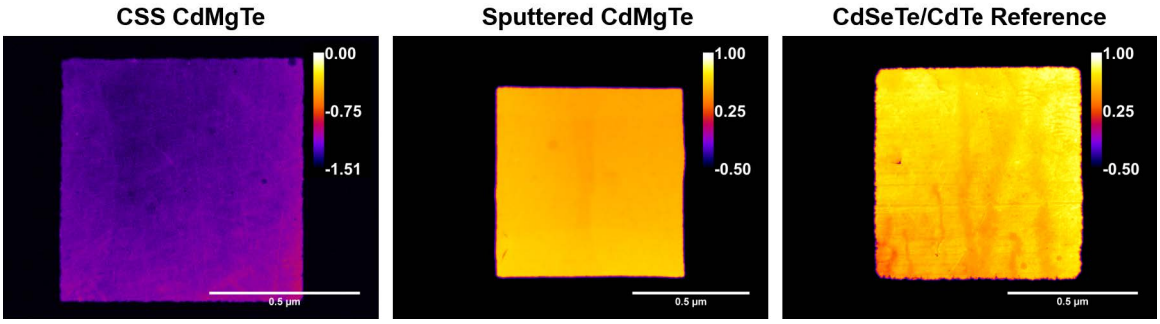

Figure 5.33: Electroluminescence images of CSS and sputtered CdMgTe devices and the CdSeTe/CdTe reference show visible voltage reduction and poorer uniformity in the CSS-CdMgTe device.

Sputtered CdMgTe device performance improvement compared to CSS-CdMgTe through V_{OC} is attributed primarily to magnesium retention in the CdMgTe layer and limited magnesium diffusion into the absorber. Magnesium behavior in the CSS and sputter-deposited CdMgTe structures was directly compared with magnesium SIMS profiles, given in Fig. 5.34, where a CdSeTe/CdTe structure is provided for comparison. The reduced magnesium level in the CdMgTe layer for CSS-deposited CdMgTe, which has also been observed in TEM/EDX imaging in this work and others [148], likely creates localized narrowed band gaps and accompanied reduction in electron-reflector effectiveness. In the sputtered CdMgTe structure, magnesium was well-maintained, and limited diffusion into the absorber was detected. The

difference in magnesium behavior is attributed to temperature: minimal elevated temperature processes follow CdMgTe sputter deposition whereas high-temperature post-CdMgTe CdTe cap and $CdCl_2$ CSS depositions are necessary for a working CSS-CdMgTe electron-reflector device.

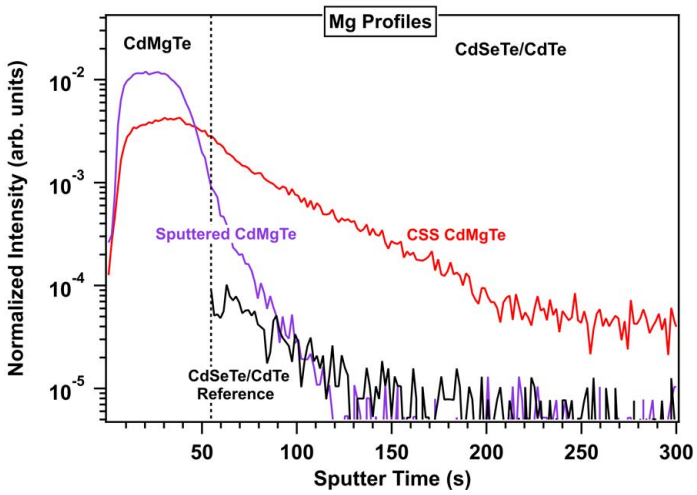

Figure 5.34: Magnesium SIMS profiles of CSS and sputter-deposited CdMgTe electron-reflector structures compared to the CdSeTe/CdTe reference show magnesium loss and extensive diffusion for CSS-deposited CdMgTe. From [188].

Insight into recombination differences for CSS vs. sputtered CdMgTe was garnered through single-photon TRPL measurements with ∼50 µW front-side excitation. The normalized TRPL decays for CSS and sputter-deposited CdMgTe electron-reflector devices are given in Fig. 5.35 with a CdSeTe/CdTe reference for comparison. The sputtered-CdMgTe device had a tail lifetime, $\tau_2 = 2.5 \pm 0.2$ ns, about double that of the CSS CdMgTe device structure, $\tau_2 = 1.2 \pm 0.1$ ns which indicates that less recombination occurred in sputtered CdMgTe devices. The lifetime differences in the CdMgTe devices may be associated with bulk recombination given the known diffusion of magnesium into the absorber for CSS-CdMgTe deposition. Extensive diffusion of magnesium into the absorber would alter bulk properties and may create a graded conduction-band edge between the CdTe and CdMgTe rather than the abrupt conduction-band offset desired for electron reflection.

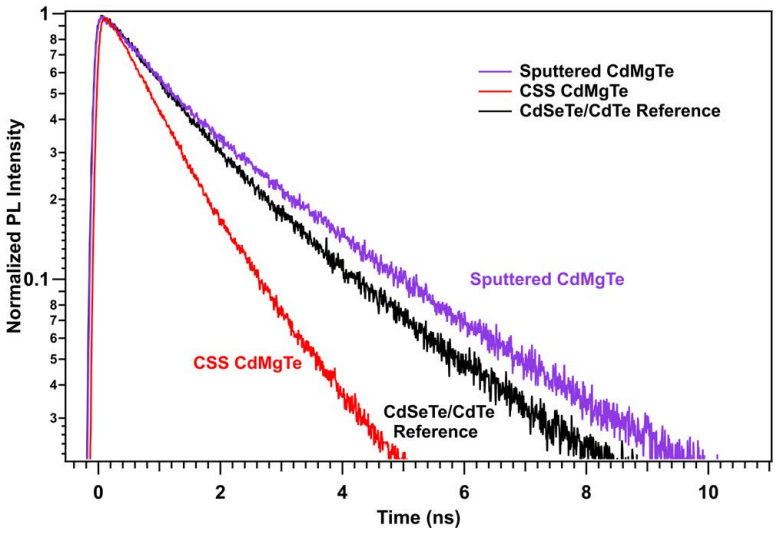

Figure 5.35: Single-photon TRPL decays of CSS and sputter-deposited CdMgTe electron-reflector devices show longer tail lifetime for the sputtered-CdMgTe device.

Notable differences in the CSS and sputtered CdMgTe devices also appeared in admittance characterization, as shown by the Mott-Schottky plots and carrier density profiles in Figs. 5.36 (a) and (b) respectively for the devices listed in Table 5.5. Capacitance-voltage data were measured at 100 kHz frequency, and phase angles were near 90° such that capacitance and conductance could be reliably separated. Both CdMgTe devices demonstrated constant capacitance with voltage before the onset of depletion region collapse (∼0.2-0.4 V), unlike the CdSeTe/CdTe reference device whose voltage-dependent slope suggested spatially-varying space charge density, in accordance with Eq. 2.24. The CSS-CdMgTe device demonstrated larger capacitance in reverse bias and anomalous data beyond the depletion-edge voltage as compared to the sputtered CdMgTe and reference devices. The sputtered CdMgTe device exhibited the most abrupt capacitance increase at the depletion region collapse around 0.2 V which indicates a fairly distinct depletion edge and fully-depleted absorber into low forward bias as desired for electron reflectors.

The carrier density profiles in Fig. 5.36 (b) corroborate device characteristics suggested in the Mott-Schottky data. The CSS-CdMgTe device carrier density was not reliably decipherable whereas the sputtered CdMgTe and CdSeTe/CdTe reference devices demonstrated

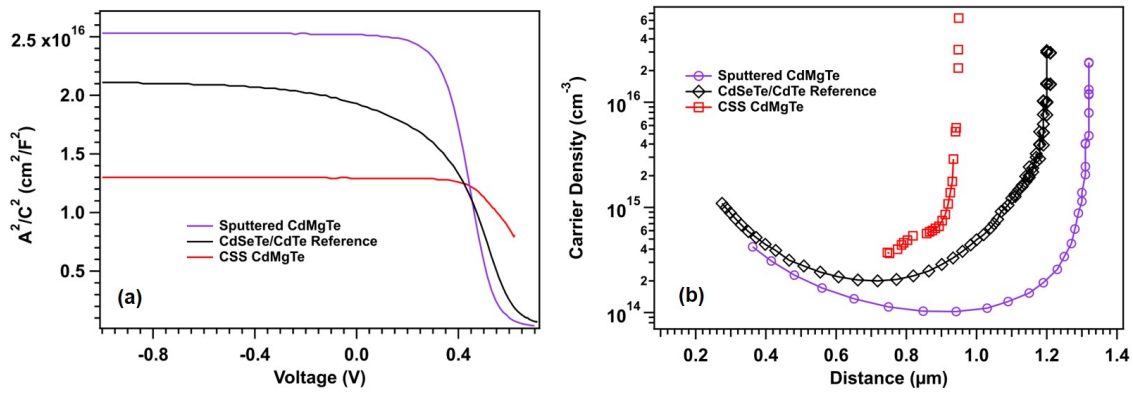

Figure 5.36: Mott-Schottky plots (a) and carrier density profiles (b) of CSS and sputtered CdMgTe devices and the CdSeTe/CdTe reference. Sputtered CdMgTe data indicate better doping in that device.

carrier densities in the 10^{14} cm^{-3} range, typical of Cu-doped CdTe, and the sputtered CdMgTe device had a somewhat wider apparent depletion width. The well-behaved carrier density data of the sputtered-CdMgTe device as compared to the CSS-CdMgTe device emphasizes the superiority of the sputtered CdMgTe device structure.

SIMS chlorine profiles in Fig. 5.37, in concert with magnesium profiles in 5.34, highlight the major advantage of sputter-deposited CdMgTe. The comparable chlorine levels in the reference and sputtered-CdMgTe absorbers demonstrate the achievable $CdCl_2$ retention with sputtered CdMgTe whereas the notable temperature-driven chlorine loss in the absorber $CdCl_2$-treated before CSS CdMgTe deposition emphasizes the necessity for $CdCl_2$ treatment post-CSS CdMgTe deposition. However, the high-temperature $CdCl_2$ process after CdMgTe deposition induces localized magnesium loss in the CdMgTe layer and extensive diffusion into the absorber such that carrier lifetime and performance are reduced. The magnesium loss and diffusion is less detrimental to device performance than $CdCl_2$ loss, thus CSS-CdMgTe electron-reflector structures are necessarily fabricated with $CdCl_2$ treatment post-CdMgTe deposition for best performance. Lower temperatures in sputtered CdMgTe render this problem obsolete; $CdCl_2$ passivation and magnesium are appropriately maintained with a corresponding maintenance of device performance.

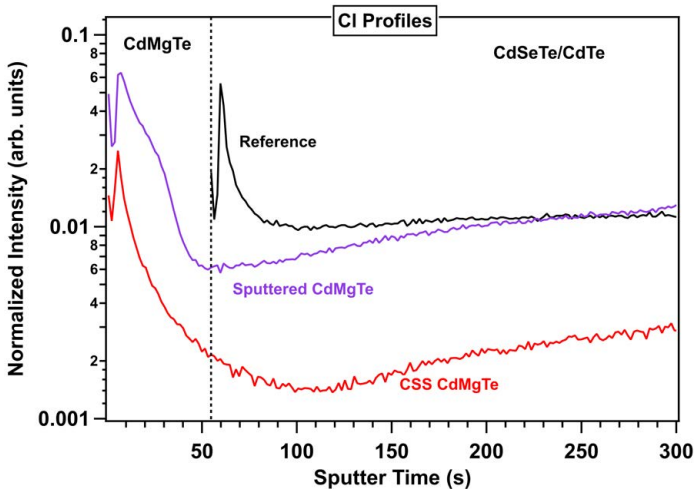

Figure 5.37: Chlorine SIMS profiles of CSS and sputter-deposited CdMgTe electron-reflector structures compared to the CdSeTe/CdTe reference show the extent to which $CdCl_2$ passivation can be maintained or lost in the sputtered and CSS-deposited CdMgTe structures respectively. From [188].

J-V, SIMS, electroluminescence, admittance, and TRPL measurements indicate that given current fabrication systems, sputtered CdMgTe is the more advantageous choice for CdMgTe electron-reflector structures because of higher device efficiencies and V_{OC}s, superior uniformity, and reduced material deficiencies.

5.5 Remaining Electron Reflector Limitations

An increase in V_{OC} with the incorporation of a CdMgTe electron-reflector layer serves as the primary metric for successful electron reflection, therefore the J-V data in Table 5.5 for the best-performing CdMgTe electron-reflector and reference devices indicate that the CdMgTe devices have not demonstrated a high level of electron-reflector behavior. The CdMgTe and non-CdMgTe-containing device V_{OC}s suggested that electron reflection is enacted somewhat successfully for the sputtered CdMgTe-incorporated structure, but the significant improvements expected based on simulation have not been realized due to at least two limitations.

One of these limitations is magnesium oxidation at the CdMgTe back surface that also extends somewhat into the CdMgTe layer. As SIMS data in section 5.3.2 indicate, despite various methods to reduce CdMgTe oxidation (CdTe cap, HCl etches, and an evaporated Te buffer layer directly following CdMgTe deposition), oxidation remains stubbornly present in all device structures. The presence of MgO inherently limits device performance because of its wide band gap-(∼6.72 eV [148,175]) induced back valence-band offset. CdMgTe oxidation could be minimized by the utilization of an in-line fabrication system where the vacuum break between the CdMgTe and following layer are eliminated. Such a configuration would also need to employ a low-temperature deposition for the post-CdMgTe material given the demonstrated negative effects of thermally-driven magnesium loss in the CdMgTe layer. This type of fabrication system configuration has not been developed, therefore the extent to which these changes would enhance device performance are not fully known.

An additional limitation is related to the valence-band offset/conduction-band offset ratio. As discussed in section 5.1.2, the desired band offset between the absorber and electron-reflector material would be a positive conduction-band offset to reflect electrons away from the back surface to reduce back-surface recombination velocity, and zero or positive valence-band offset to enhance hole transport to the back contact for collection. To determine the valence and conduction-band offsets, X-ray photoelectron spectroscopy (XPS) was measured on three film structures such that the Kraut method could be applied [189]. The three structures, given in Figs. 5.38 (a), (b), and (c) correspond to CdMgTe bulk, CdTe bulk, and CdTe/CdMgTe deposited on Tec10/100 nm MgZnO, where the CdMgTe was sputter-deposited. The CdMgTe bulk sample was deposited on a thin CdTe layer so that the band gap and material properties were nominally equivalent to those present in device structures. Given the shallow analysis depth of XPS (∼5 nm), an ∼3-nm CdMgTe layer was deposited on CdTe in the CdTe/CdMgTe structure such that the interface effects could be probed. To reduce oxidation, the samples were fabricated within 24 hours of measurement and stored in vacuum-sealed bags in an Ar-environment glove box.

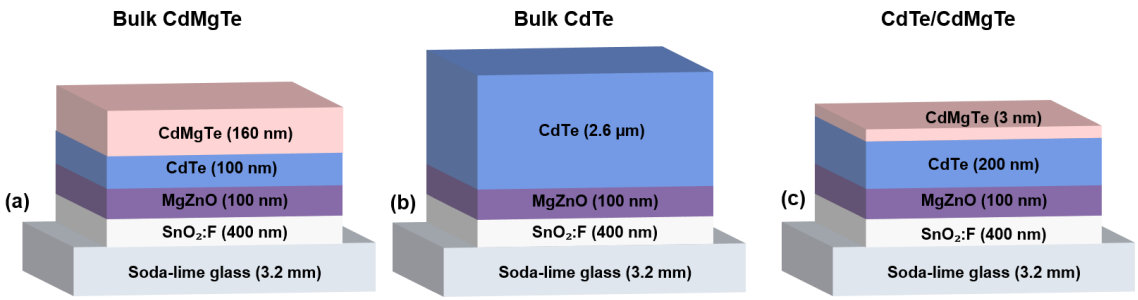

Figure 5.38: Film structures (not to scale) for XPS measurements: CdMgTe bulk (a), CdTe bulk (b), and CdTe/CdMgTe interface (c).

Following the Kraut method [189], the valence-band offset between two materials is generally given by:

$$\Delta E_V = (E^A_{CL} - E^A_{VBM}) - (E^B_{CL} - E^B_{VBM}) - \Delta E_{CL}(i) \tag{5.2}$$

where ΔE_V corresponds to the valence-band differential between materials A and B at the heterojunction interface, and E^A_{CL} and E^B_{CL} are the core level binding energies of materials A and B respectively, measured on their respective bulk structures. E^A_{VBM} and E^B_{VBM} are the valence band maxima energies of materials A and B respectively, determinable from valence band spectra measured on their respective bulk structures, and ΔE_{CL}(i) is the core level binding energy difference of layers A and B, given by $\Delta E_{CL}(i) = E^A_{CL}(i) - E^B_{CL}(i)$, measured from the interface structure.

High-resolution scans of the core levels and valence-band maximum binding energies were run at a pass energy of 23.5 eV with a 0.1-eV step and were corrected by the measured C1s peak shift to 284.8 eV. The core level peaks were determined by applying a Shirley-type background in CasaXPS and Voigt fit (given by dashed lines in Fig. 5.39) to the peak region. For the CdMgTe bulk structure (material A), the Mg1s core level binding energy peak was used, and E^{CdMgTe}_{CL}= 1303.3 ± 0.1 eV as shown in Fig. 5.39 (a). The Cd 3d5/2 peak was used for the CdTe bulk and E^{CdTe}_{CL}= 404.9 ± 0.1 eV, pictured in Fig. 5.39 (b). The Mg1s and Cd 3d5/2 peak binding energies for the CdTe/CdMgTe interface structure, given in Figs. 5.39 (c) and (d) respectively, were 1303.7 ± 0.15 eV, and 405.1 ± 0.1 eV such that

$\Delta E_{CL}(i)$=898.6 ± 0.25 eV. The valence-band-maxima energies for the CdTe and CdMgTe bulk materials were determined by fitting the leading edge of the Cd valence band data to the baseline [189, 190]. These energies were determined to be E_{VBM}^{CdMgTe}= 20 ± 20 meV and E_{VBM}^{CdTe}= 40 ± 20 meV, and are shown as insets in Figs. 5.39 (a) and (b) respectively.

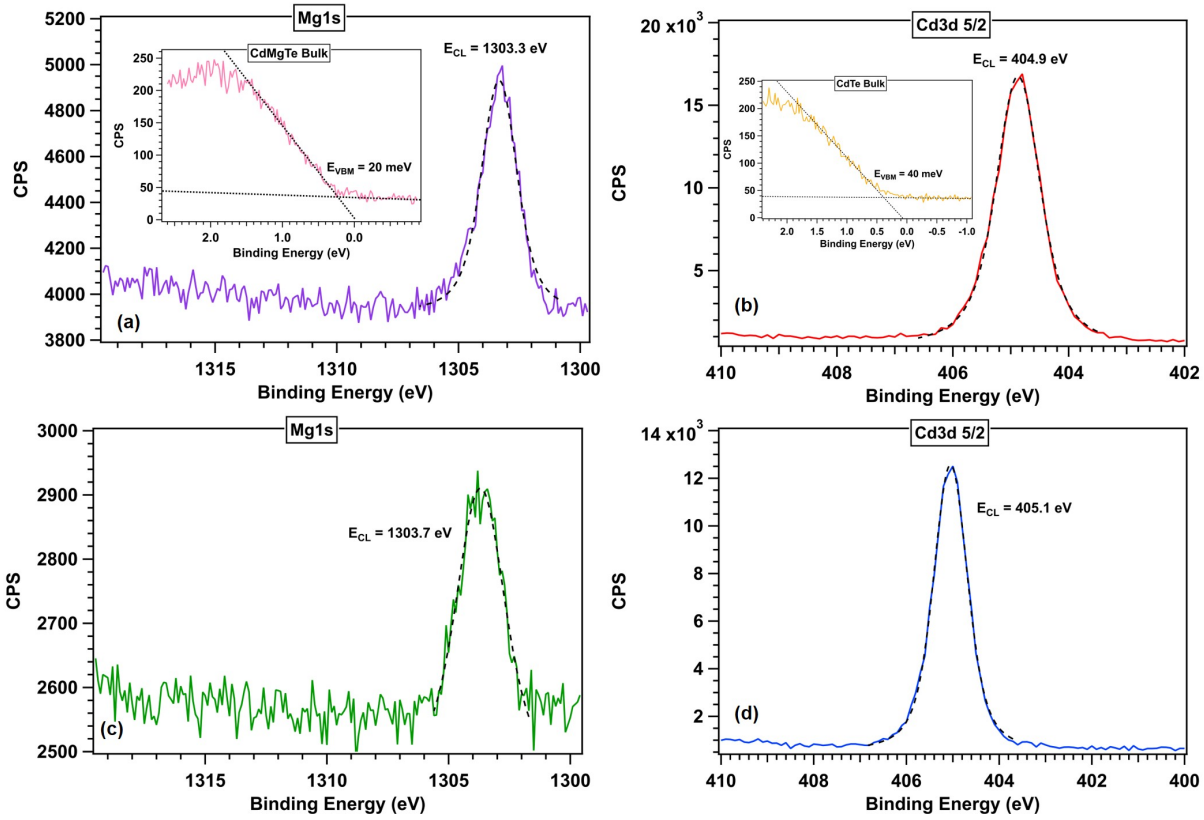

Figure 5.39: XPS spectra for (a) the CdMgTe bulk Mg1s core level and valence band (inset), (b) CdTe bulk Cd3d 5/2 core level and valence band (inset), and CdTe/CdMgTe interface Mg1s and Cd3d 5/2 core levels (c) and (d) respectively.

Incorporating the fit results from the XPS spectra into Eq. 5.2 with reasonable uncertainty estimates, ΔE_V = -50 to -100 meV. A range for the valence-band offset is provided rather than a single value due to the inherent uncertainty in the measurement and fits; XPS data of the valence band edge were noticeably noisy such that fit-based determination of the valence band maxima values had somewhat large uncertainty, as is common in this method [117]. This uncertainty could be reduced through the use of ultraviolet photoelectron

spectroscopy (UPS), which provides higher resolution spectra due to a much smaller achievable energy range [191]. Given the unavailability of a UPS measurement system at the time of this work, higher resolution data were not attainable. Uncertainty could also be reduced by implementation of a different method which bypasses the valence band maxima fitting in the Kraut method. This technique utilizes a deep core level shared by both materials as a constant reference point to track binding energy shifts, and has certain material constraints not necessarily satisfied by these structures [117].

Given the valence-band offset, the conduction-band offset can be determined according to:

$$\Delta E_C = E_g^{CdMgTe} - E_g^{CdTe} - \Delta E_V \tag{5.3}$$

where E_g^{CdMgTe} and E_g^{CdTe} correspond to the CdMgTe and CdTe band gaps. The CdMgTe and CdTe optical band gaps were 1.87 $\pm$ 0.05 and 1.48 $\pm$ 0.02 eV respectively, determined by Tauc plot analysis of transmission data measured on a $\sim$600 nm CdMgTe film on 100 nm CdTe, and $\sim$200 nm CdTe film. Given these data, the conduction-band offset was determined to be 290-340 meV. Again, a range is given due to the uncertainty in the determination of the valence-band offset and band gaps. These data reveal that the CdTe/CdMgTe band offset is split between the valence and conduction bands, with approximately 20% contribution from the valence-band offset and 80% contribution from the conduction-band offset. This ratio falls within the range of ratios reported in literature: somewhat lower than the 50/50 [161] and 30/70 ratios [157–160] suggested by calculation, and slightly higher than the experimentally-determined 15/85 ratio [117]. The negative valence-band offset somewhat limits the effectiveness of the CdMgTe electron-reflector structure: hole transport to the back contact is slightly impeded and electron reflection is decreased due to a reduced conduction-band offset. Band-based engineering would be required to mitigate this limitation and could involve adjustments to CdMgTe doping or the selection of another electron-reflector material, which may be accompanied by its own set of band alignment or lattice constant-based disadvantages.

Other limitations which may remain in the CdMgTe electron-reflector structures include non-optimized CdMgTe passivation which would require fabrication-based solutions, and suspected low CdMgTe carrier concentration (simulations indicate that increased carrier concentrations in the electron-reflector layer should improve V_{OC} and performance [192]) which could be addressed through additional doping work. Finally, the necessity for a thin absorber in electron-reflector structures fundamentally limits performance due to the close proximity of the front junction and high-recombination back surface, and reduced photon absorption and concomitant current collection.

Chapter 6

CONCLUSIONS

CdTe-based solar cells have greatly evolved over the past decade through modifications to their thin-film structures via incorporation of new layers and adjustments to key layers. These changes have been accompanied by large gains in performance, although the voltage deficit in CdTe remains an outstanding limitation to further efficiency improvements (only ~79% of the maximum V_{OC} has been achieved to date, as compared to ~99% and 88% for J_{SC} and fill factor respectively, such that CdSeTe/CdTe device efficiency has realized only ~69% of its potential [57]). This work focused on reducing the voltage deficit in CdTe-based devices by introducing new material layers into thin CdTe-absorber structures. Absorber thicknesses less than 2 µm (more than half the thickness of typical CdTe-based absorbers) were pursued for the ultimate incorporation of an electron-reflector layer which relies on thin, fully-depleted absorbers to reduce voltage deficit. Such thin layers are also advantageous for manufacturing time and cost savings, and bifacial and semi-transparent structures for next-generation solar cell development.

Fabrication optimization and a solid understanding of thin CdTe device structures was necessary before additional layers were introduced. The $CdCl_2$ passivation and Cu-doping treatments were optimized on 0.4-1.2 µm CdTe absorber devices and electron microscopy imaging revealed favorable film characteristics in these structures. These included MgZnO layer continuity, CdTe grains which extended throughout the absorber, and a Te layer conformal to the CdTe, which together indicated that thin CdTe devices should have respectable efficiencies. The efficiencies of the 0.4-1.2 µm CdTe devices were in fact quite good given the limited thickness; efficiency reached 15.0% with a 1.2-µm CdTe absorber. The 0.4 and 0.6 µm devices remained fully-depleted into forward bias, and the extent of full depletion shifted slightly toward 0 V bias for the 0.8, 1.0, and 1.2 µm devices, determined through capacitance measurements. Although CdTe thickness-dependent performance losses were observed

in these devices, the quantified losses were not large enough to induce poor performance at any of the CdTe thicknesses. For the 1.0-µm CdTe device the losses were fairly small, the absorber close to fully depleted in forward bias, and the performance fairly high such that 1.0-µm CdTe absorbers were used as the foundation for advanced structure changes.

A CdSeTe alloy layer was introduced as an additional absorber material preceding CdTe to improve device performance through increased J_{SC} due to additional photon conversion from the slightly lower, 1.4-eV CdSeTe band gap. Performance improvements had been observed in thicker, ∼4-µm absorbers which incorporated CdSeTe, but this work expanded the understanding and extent of that improvement in a number of ways. First, it was demonstrated that performance improvement was achievable for thin, 1.5-µm absorber devices with no intentional inter-diffusion of the CdSeTe and CdTe such that the two layers together could be labeled a bilayer absorber. Next, this work also demonstrated the importance of the CdSeTe thickness. Performance reduction was consistently observed for CdSeTe thickness greater than the CdTe thickness, independent of the 20%, 30%, and 40% CdSe composition in the CSS CdSeTe source material. 0.5-µm CdSeTe/1.0-µm CdTe absorbers demonstrated the highest efficiencies, reaching 15.6%, and when compared to 1.5-µm CdTe devices, exhibited improvements beyond performance. Longer TRPL tail lifetimes suggested better bulk properties with CdSeTe, and current-loss analysis showed that CdSeTe is the dominant absorber, accounting for 88% of current collection in 0.5-µm CdSeTe/1.0-µm CdTe devices. In addition to increased J_{SC} with the incorporation of CdSeTe, J-V and electroluminescence data demonstrated that CdSeTe/CdTe bilayer devices reduced the voltage deficit by 30 mV due to the 100-meV narrower band gap of CdSeTe compared to CdTe as well as passivating effects of selenium.

To further decrease the voltage deficit, a back-surface field design was implemented in the CdSeTe/CdTe device structure. Multiple mechanisms exist to create a back-surface field in CdTe, and this work pursued such a field through an electron-reflector structure. A wide band-gap (∼1.8 eV) CdMgTe layer was deposited behind the CdTe to create a conduction-band offset such that electrons would be reflected from the recombination-prone

back surface given fully-depleted absorbers in forward bias. CdMgTe was incorporated into the CdSeTe/CdTe device structure through CSS and sputter depositions, but sputter deposition proved more favorable to address the material complexities of CdMgTe (temperature-induced magnesium diffusion balanced with $CdCl_2$ passivation, doping, and MgO formation), and produced higher-performing CdMgTe electron-reflector devices. Low substrate temperatures achievable in sputtered CdMgTe deposition was the greatest advantage over CSS-CdMgTe. In CSS, SIMS profiles showed notable chlorine loss in absorbers $CdCl_2$-treated before CSS CdMgTe deposition, but also significant magnesium diffusion and loss from and in the CdMgTe layer with $CdCl_2$ treatment after CSS-CdMgTe and associated performance reduction. Lower substrate temperatures in sputtered CdMgTe very nearly eliminated this problem; $CdCl_2$ passivation and magnesium were appropriately maintained with a corresponding maintenance of device performance.

An examination of Cu doping on sputtered CdMgTe electron-reflector devices revealed that the CdMgTe material required extrinsic doping and that given the addition of the CdMgTe layer at the back, an extended Cu treatment was required to diffuse Cu through the CdMgTe to properly dope the absorber. Sputtered CdMgTe electron-reflector devices demonstrated good device performance: 16.0% efficiency was achieved with CdMgTe on 0.5-µm CdSeTe/1.0-µm CdTe absorbers, the highest-known CdMgTe electron-reflector device performance to date. The CdMgTe and non-CdMgTe-containing device V_{OC}s suggested that electron reflection was enacted partially successful for the sputter CdMgTe-incorporated structure, but the significant improvements expected based on simulation have not been realized due to at least two limitations. First is the conduction-band/valence-band offset ratio. XPS measurment analysis indicated that this ratio was approximately 80/20. The negative valence-band offset somewhat limits the effectiveness of the CdMgTe electron-reflector structure: hole transport to the back contact is slightly impeded and electron reflection is decreased due to a reduced conduction-band offset. Another limitation was magnesium oxidation at the CdMgTe surface and somewhat into the material. Despite techniques investigated to mitigate oxidation formation (HCl etch, CdTe cap layer, Te buffer layer), a

small amount of MgO remained present in all structures. The wide, ∼6.72-eV MgO band gap inherently limits device performance through the induced back valence-band offset.

Many avenues can be pursued to achieve further reduction of CdTe voltage deficits. Within the electron-reflector structure, continued use of CdMgTe as the electron-reflector layer would require a means to reduce or eliminate MgO formation (perhaps through an in-line vacuum deposition system which must also operate at low temperatures), and a way to reduce or eliminate the negative valence-band offset. This could include band-based engineering through adjustments to CdMgTe doping or the selection of another electron-reflector material although use of a different electron-reflector material would likely be accompanied by its own set of band-alignment or lattice constant-based disadvantages. The necessity for a thin absorber in electron-reflector structures fundamentally limits performance due to the close proximity of the front junction to the high-recombination back surface, and reduces photon absorption and concomitant current collection, which strongly suggests exploration of additional methods for back-surface field incorporation. Mechanisms include heavy doping at the back, the addition of a charge layer, and chemical or thermal passivation. These require fabrication-based solutions, and initial exploration of these mechanisms through additional passivation, As doping, and Al_2O_3 layers presently demonstrate promise.

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